

Compal confidential

Schematics Document

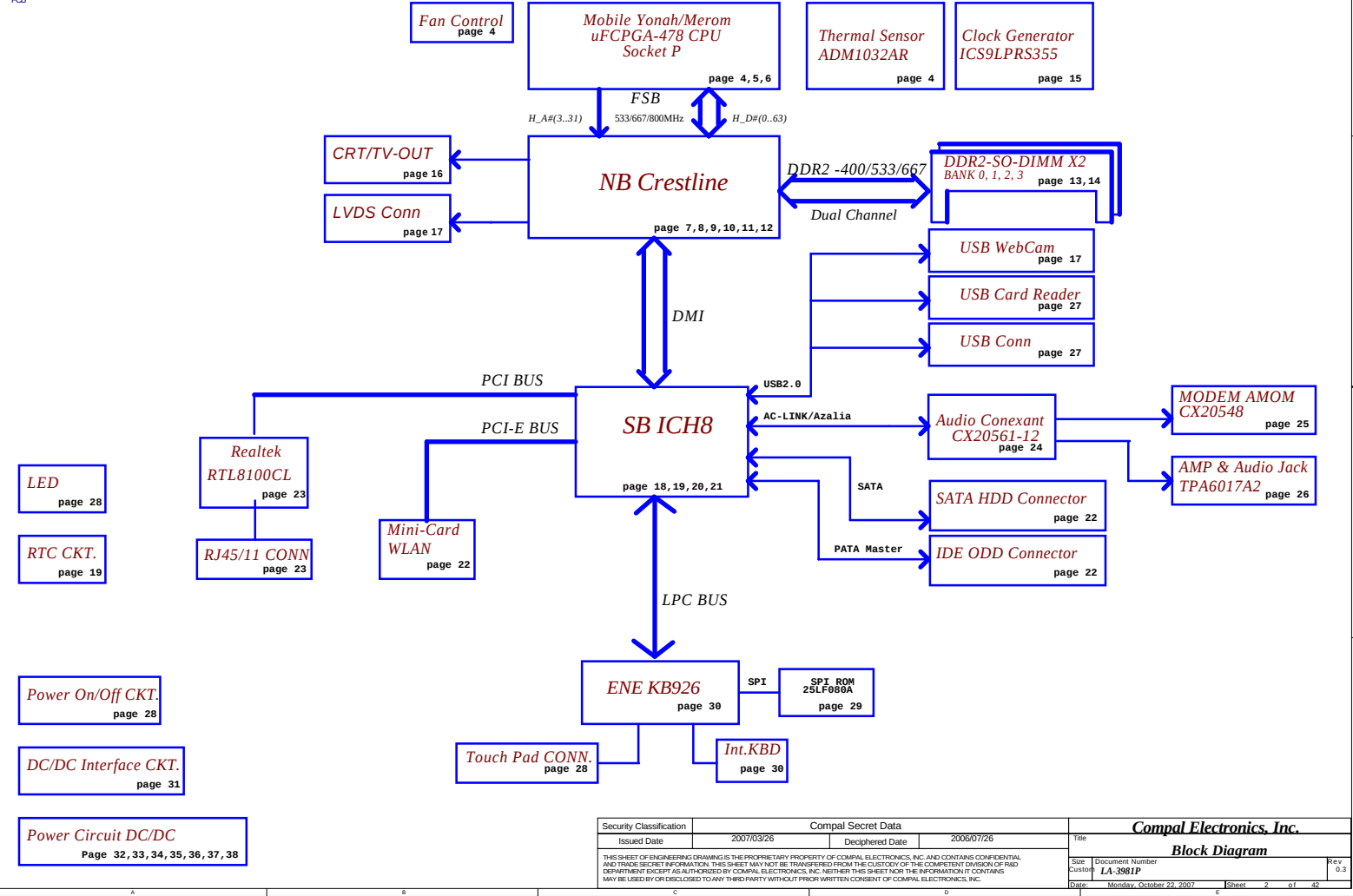
Mobile Merom uFCPGA with Satna Rosa Platform

2007-08-02
REV:0.2

Security Classification	Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/07/26	
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				Document Number LA-3981P
				Rev 0.3
				Date Monday, October 22, 2007
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LEON 1.0 (Merom +Crestline+ICH8)



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Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD22	0	A

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

SMBUS Control Table

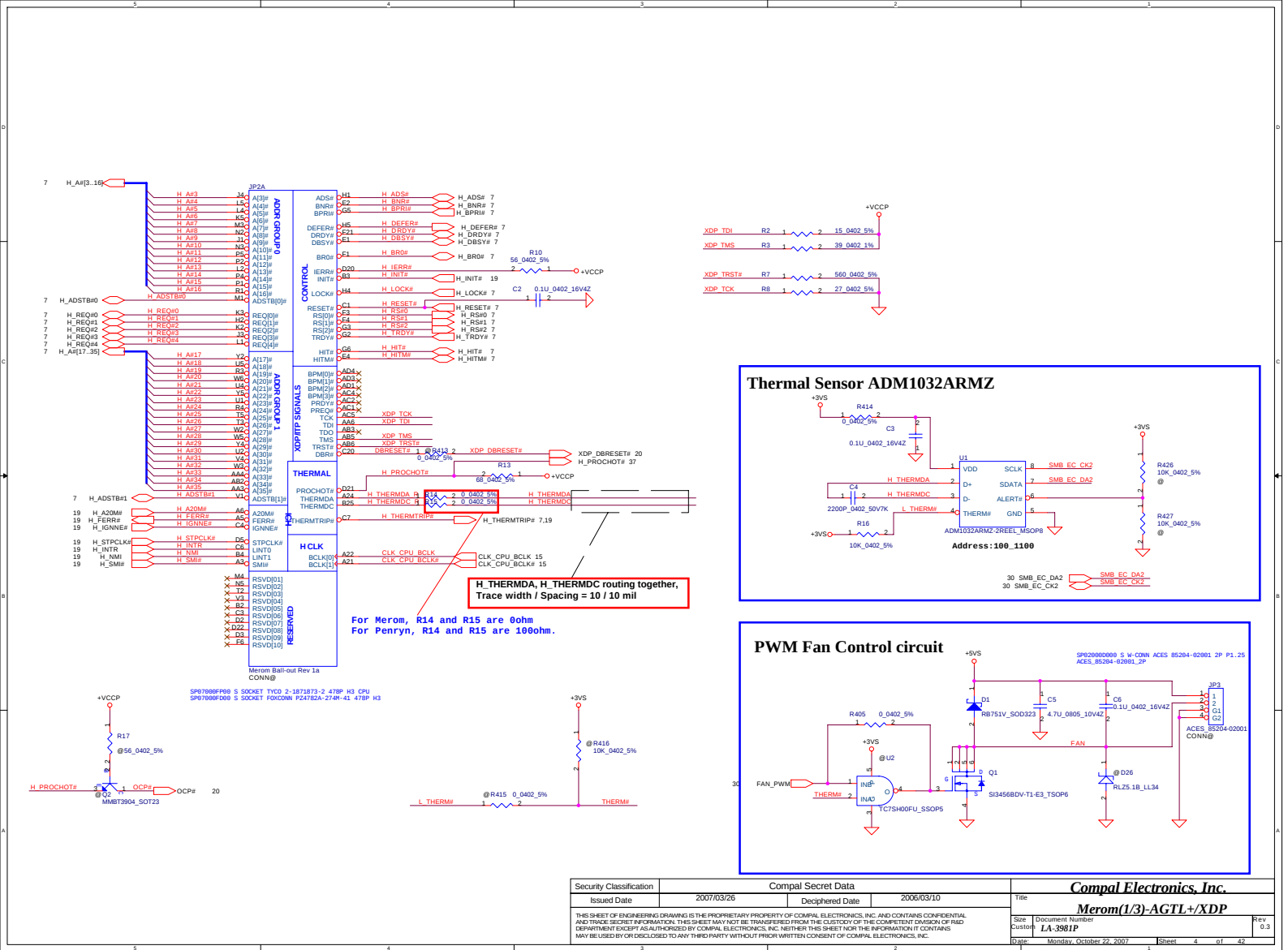
	SOURCE	INVERTER	BATT	SERIAL EEPROM	TEMPERATURE SENSOR (CPU) ADM1032	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB925	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH8	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Crestline	X	X	X	X	X	X	X	V

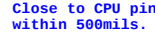
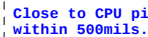
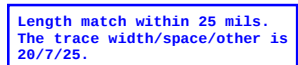
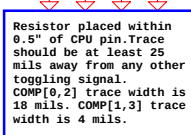
BOM: 43151732L01(965GM) & 443151732L02(960GML) with card reader

BOM: 43151732L03(965GM) & 43151732L04(960GML) without card reader

Jump-Short: PJP?

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CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.
COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

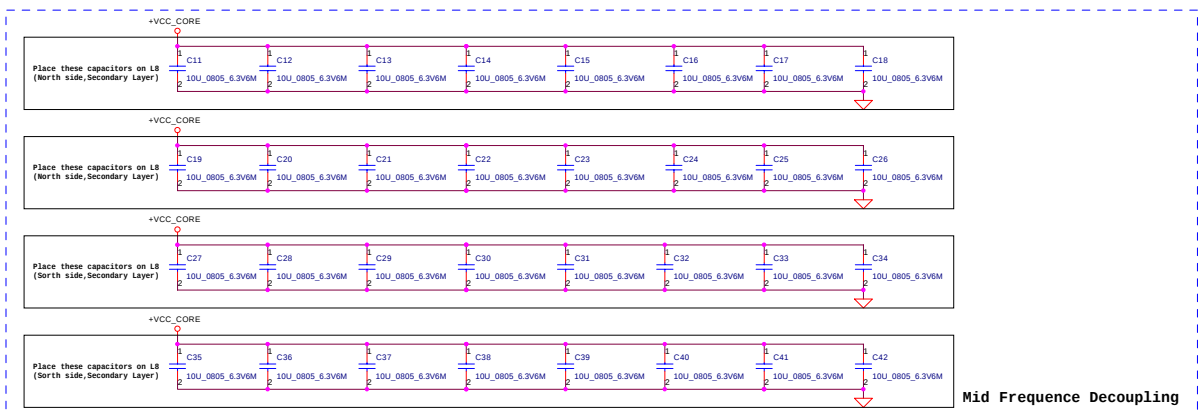
Length match within 25 mils.
The trace width/space/other is
20/7/25.

Close to CPU pin
within 500mils.

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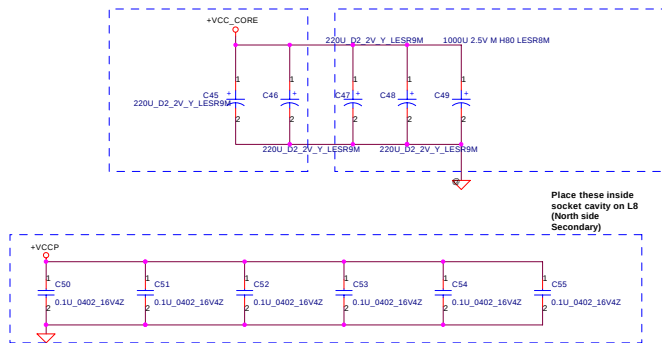
JP20		
A4	VSS[001]	VSS[082]
A6	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A18	VSS[006]	VSS[087]
A22	VSS[007]	VSS[088]
A26	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B8	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B13	VSS[012]	VSS[093]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C2	VSS[017]	VSS[098]
C4	VSS[018]	VSS[099]
C11	VSS[019]	VSS[100]
C14	VSS[020]	VSS[101]
C16	VSS[021]	VSS[102]
C18	VSS[022]	VSS[103]
C2	VSS[023]	VSS[104]
C2	VSS[024]	VSS[105]
C2	VSS[025]	VSS[106]
D1	VSS[026]	VSS[107]
D4	VSS[027]	VSS[108]
D8	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D16	VSS[030]	VSS[111]
D18	VSS[031]	VSS[112]
D19	VSS[032]	VSS[113]
D22	VSS[033]	VSS[114]
D26	VSS[034]	VSS[115]
E2	VSS[035]	VSS[116]
E6	VSS[036]	VSS[117]
E11	VSS[037]	VSS[118]
E14	VSS[038]	VSS[119]
E16	VSS[039]	VSS[120]
E19	VSS[040]	VSS[121]
E21	VSS[041]	VSS[122]
E24	VSS[042]	VSS[123]
F2	VSS[043]	VSS[124]
F6	VSS[044]	VSS[125]
F8	VSS[045]	VSS[126]
F11	VSS[046]	VSS[127]
F16	VSS[047]	VSS[128]
F19	VSS[048]	VSS[129]
F22	VSS[049]	VSS[130]
F26	VSS[050]	VSS[131]
G2	VSS[051]	VSS[132]
G26	VSS[052]	VSS[133]
G4	VSS[053]	VSS[134]
G11	VSS[054]	VSS[135]
G16	VSS[055]	VSS[136]
G26	VSS[056]	VSS[137]
H6	VSS[057]	VSS[138]
H8	VSS[058]	VSS[139]
H21	VSS[059]	VSS[140]
H24	VSS[060]	VSS[141]
I2	VSS[061]	VSS[142]
J2	VSS[062]	VSS[143]
J6	VSS[063]	VSS[144]
K1	VSS[064]	VSS[145]
K4	VSS[065]	VSS[146]
K26	VSS[066]	VSS[147]
K28	VSS[067]	VSS[148]
L2	VSS[068]	VSS[149]
L6	VSS[069]	VSS[150]
L1	VSS[070]	VSS[151]
L24	VSS[071]	VSS[152]
M2	VSS[072]	VSS[153]
M6	VSS[073]	VSS[154]
M22	VSS[074]	VSS[155]
M26	VSS[075]	VSS[156]
N2	VSS[076]	VSS[157]
N14	VSS[077]	VSS[158]
N23	VSS[078]	VSS[159]
N26	VSS[079]	VSS[160]
N28	VSS[080]	VSS[161]
P2	VSS[081]	VSS[162]
		VSS[163]

Merom Ball-out Rev 1a
CONN

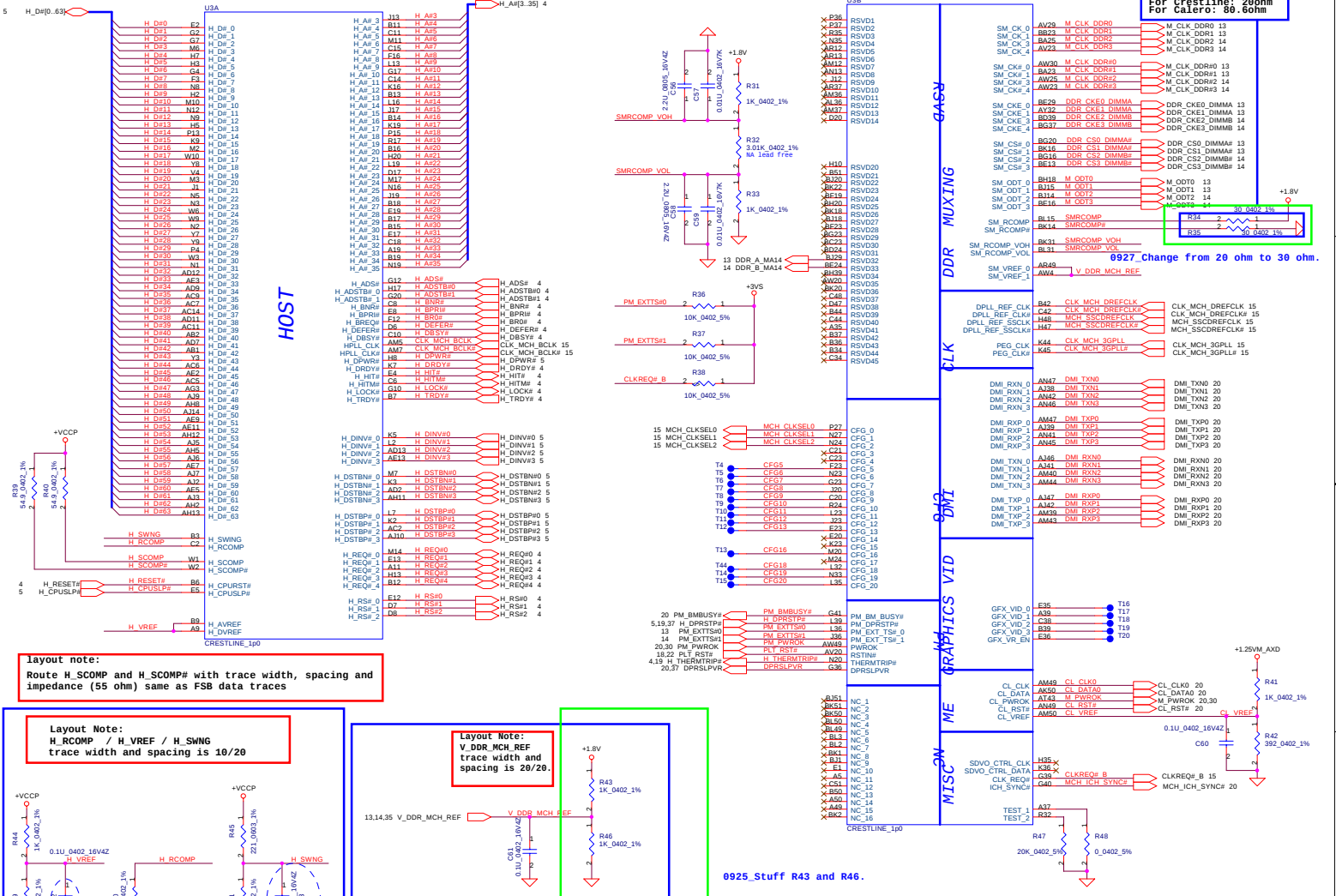


Near CPU CORE regulator

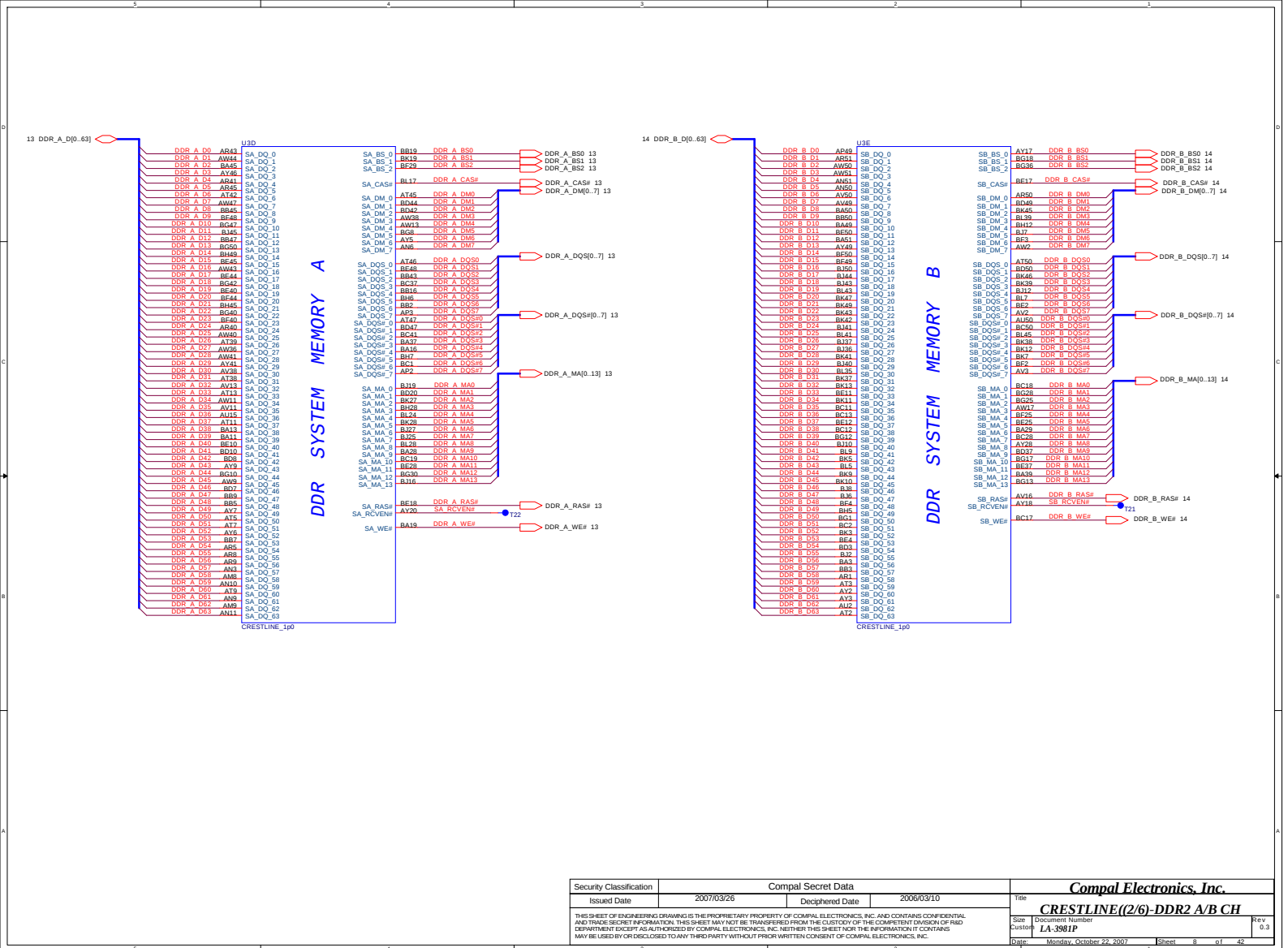
ESR <= 1.5m ohm
Capacitor > 1980uF



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Issued Date	2007/03/26	Deciphered Date	2006/03/10	Doc Number	CRESTLINE(1/6)-AGTL+DMI/DDR2
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Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIe)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved 00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[13:12] (XOR/ALLZ)	
CFG[15:14]	Reserved 0 = Disabled 1 = Enabled *
CFG16 (FSB Dynamic ODT)	
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

CFG[17:3] have internal pull up

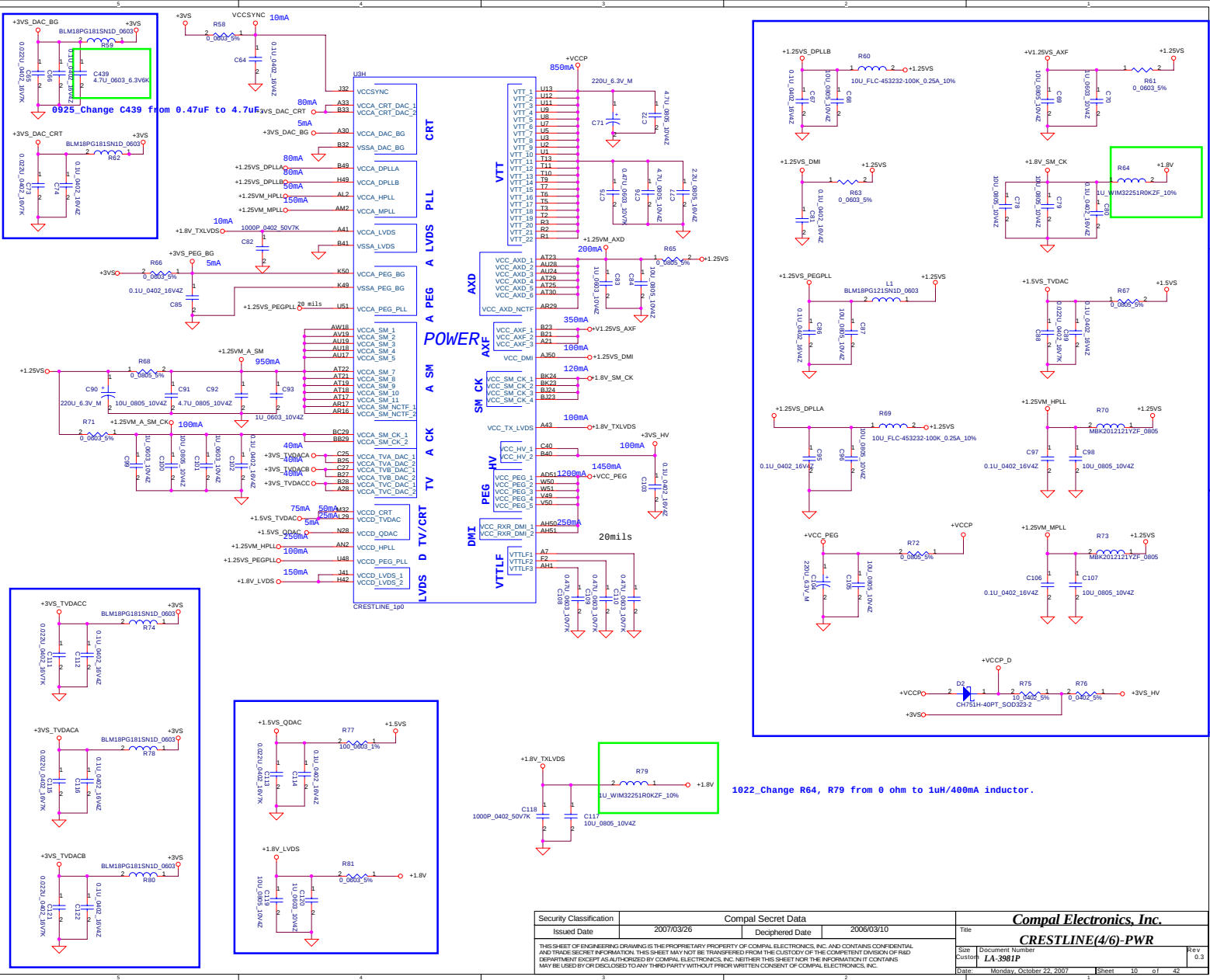
CFG[19:18] have internal pull down

For Crestline: 2.4kohm
For Calero: 1.5kohm

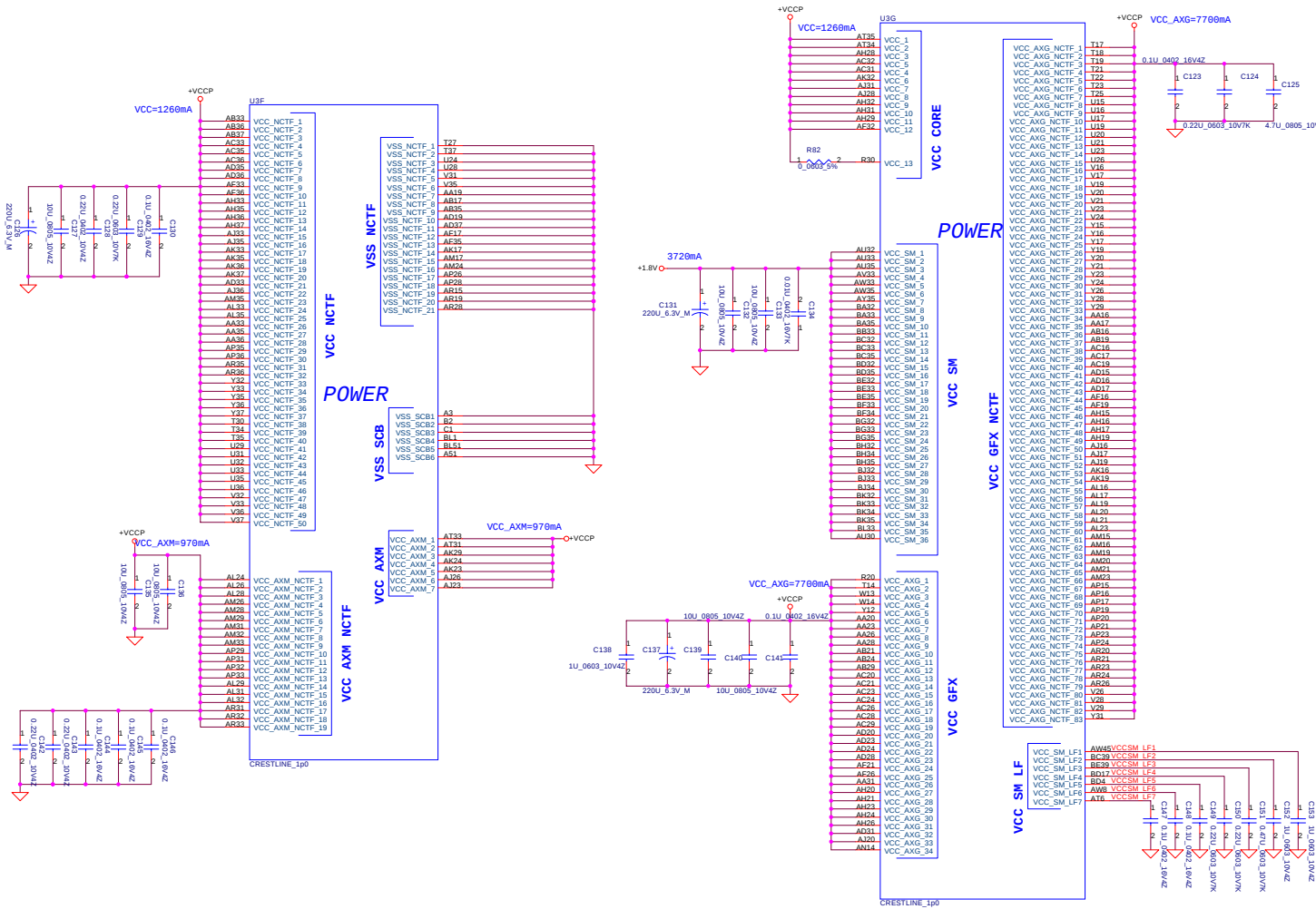
PEGCOMP trace width
and spacing is 20/25 mils.

For Crestline: 1.3kohm
For Calero: 255ohm

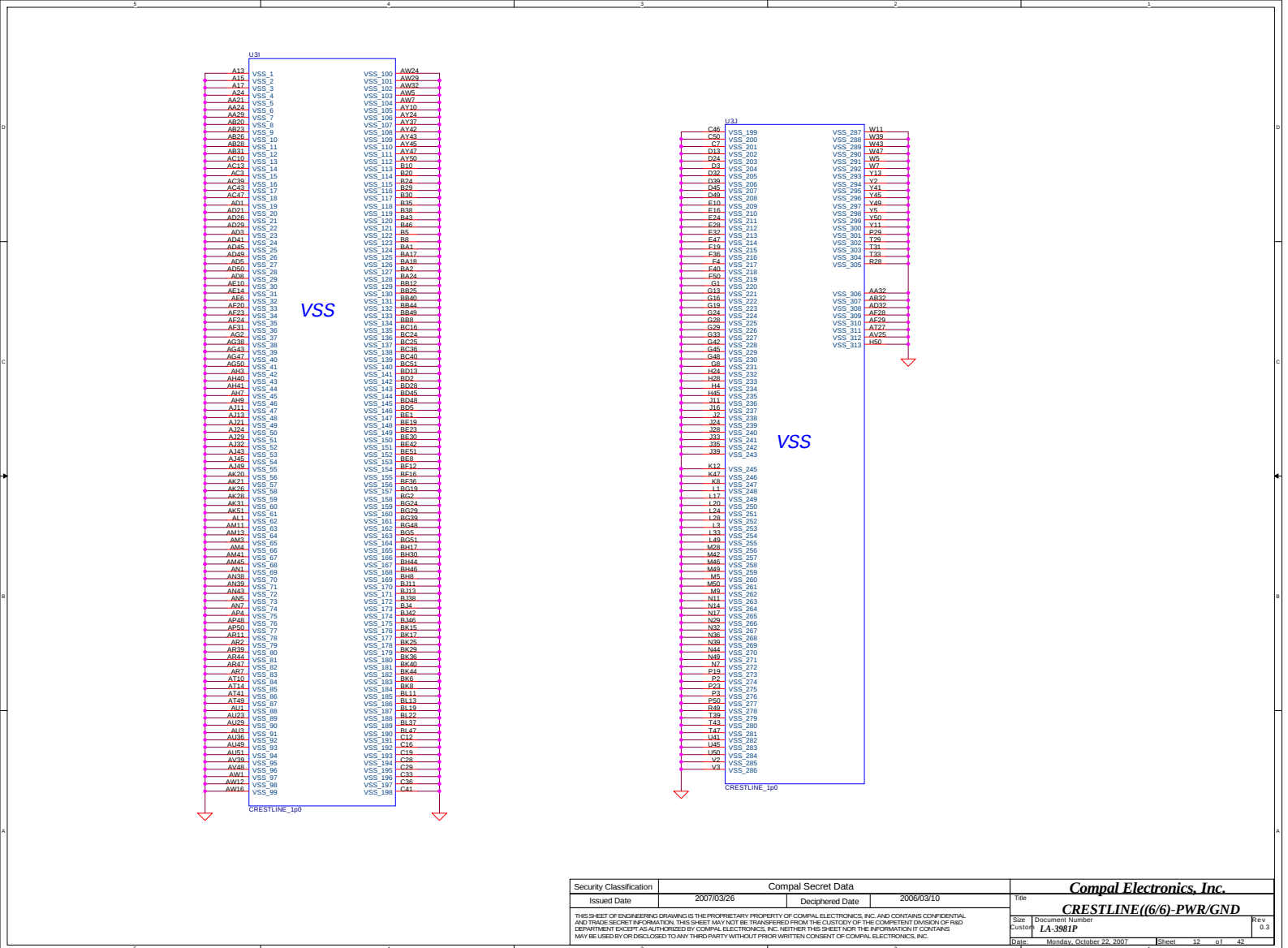
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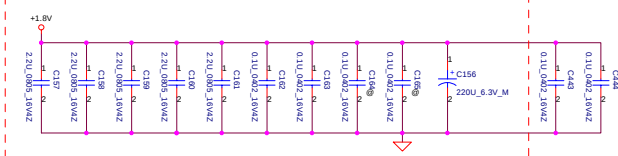
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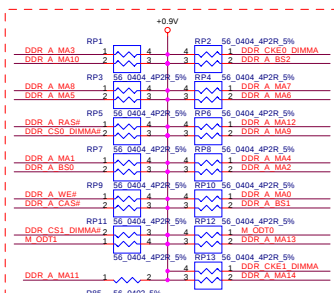
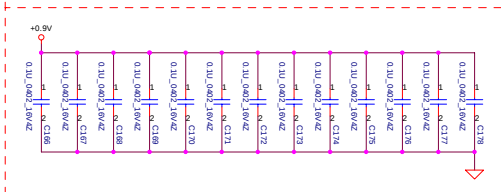
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8 DDR_A_DQS#0[0..7]
8 DDR_A_DQ[0.63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
7.8 DDR_A_MA[0..14]

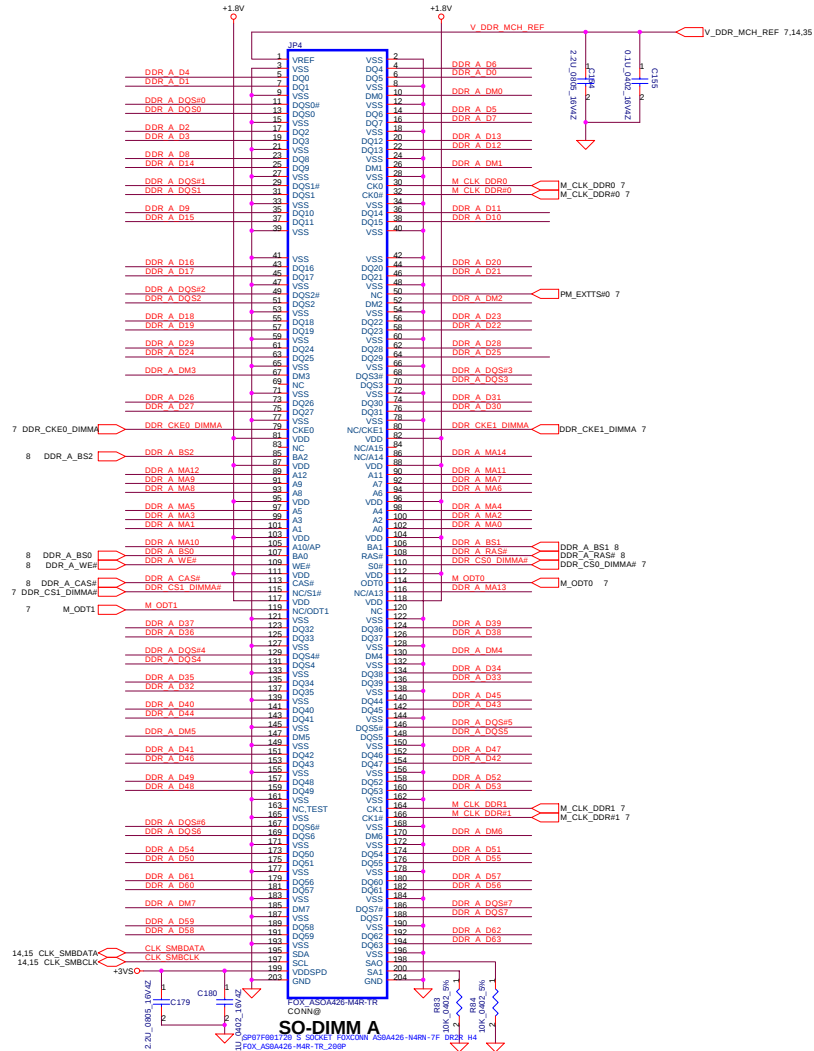
Layout Note:
Place near JP34



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



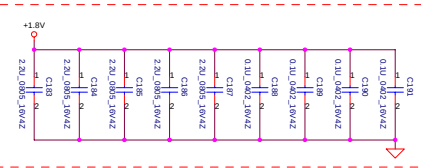
Layout Note:
Place these resistor closely JP34,all trace length Max=1.5"



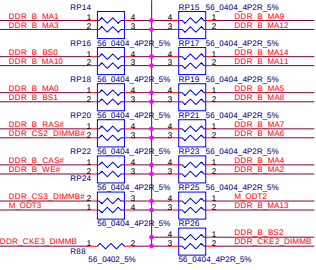
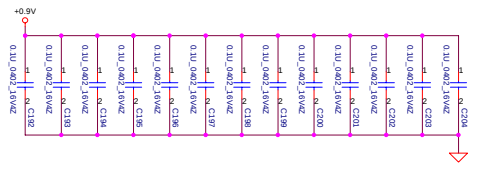
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	Title	DDR-II-SODIMM SLOT1
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8 DDR_B_DQS# [0..7]
8 DDR_B_DQ [0..63]
8 DDR_B_DM [0..7]
8 DDR_B_DQS# [0..7]
7.8 DDR_B_MA [0..14]

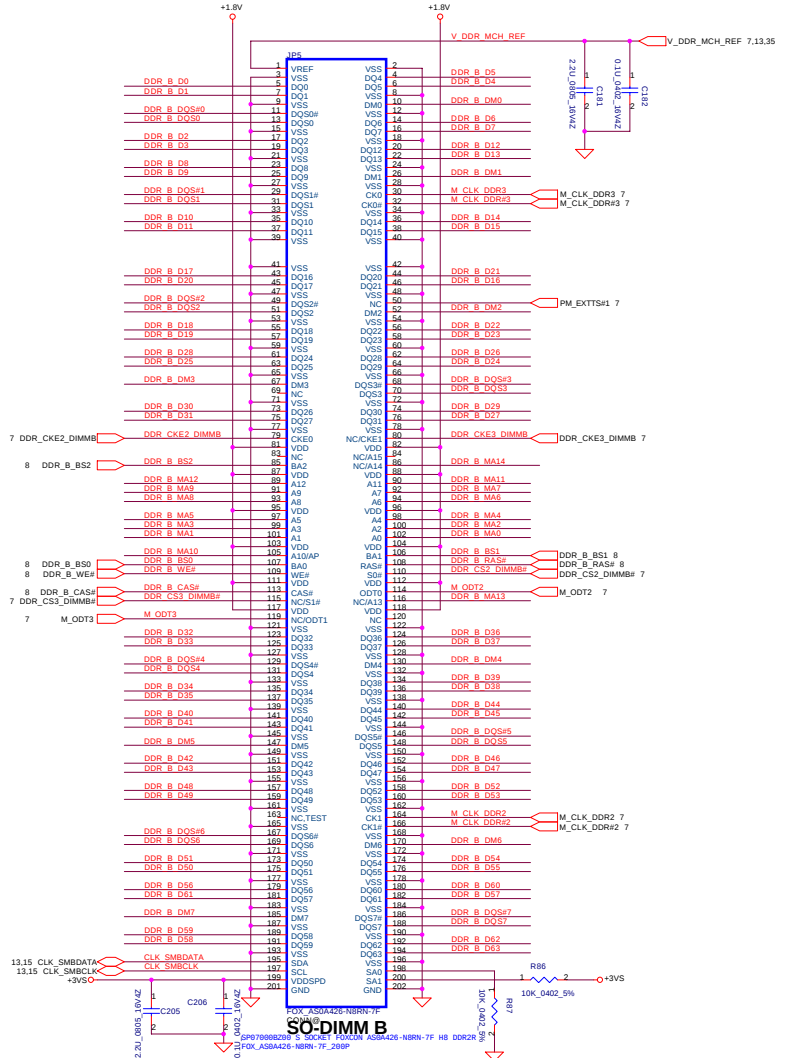
Layout Note:
Place near JP10



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

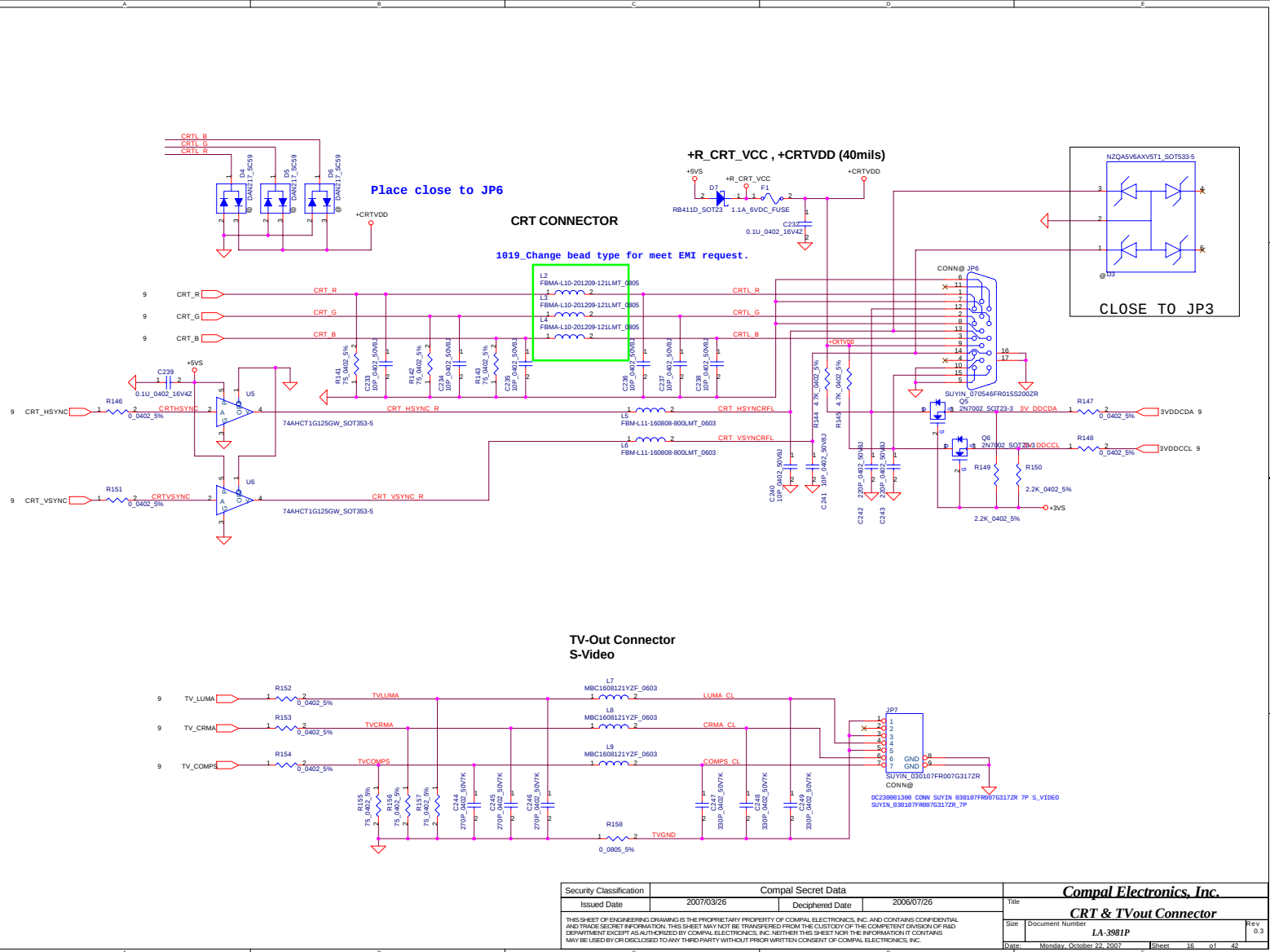


Layout Note:
Place these resistor
closely JP10, all
trace length Max=1.5"

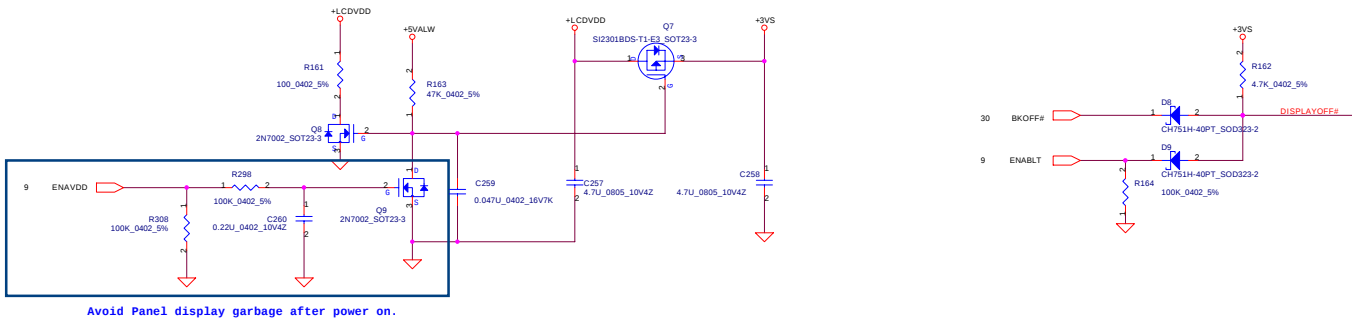
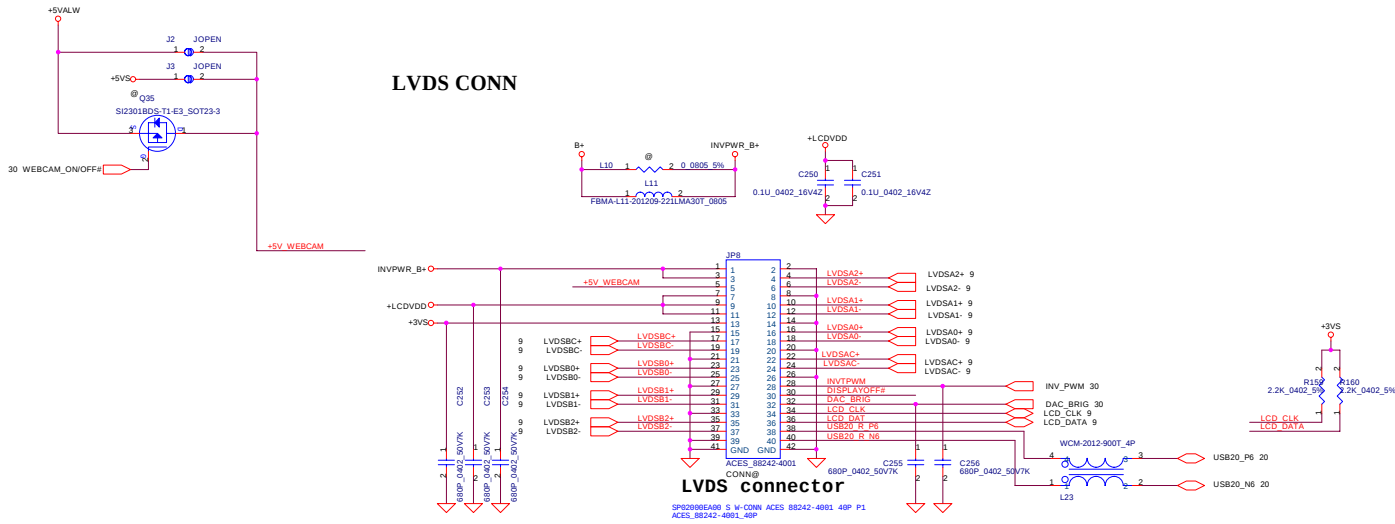


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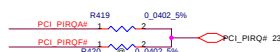
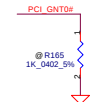
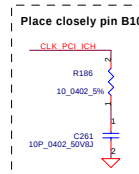
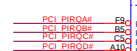
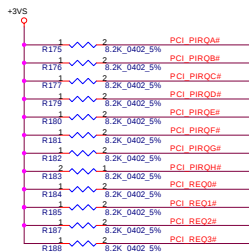
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Issued Date	2007/03/26	Deciphered Date	2006/03/10	Clock generator		
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					LA-391P	0.3
Date: Monday, October 22, 2007				Sheet	15	of 42



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				CRT & TVout Connector	
Size		Document Number		LA-3981P	
Date		Monday, October 22, 2007		Sheet 18 of 42	
				Rev 0.3	



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				LA-3881P	Rev 0.3
				Date	Monday, October 22, 2007
				Sheet	17 of 42



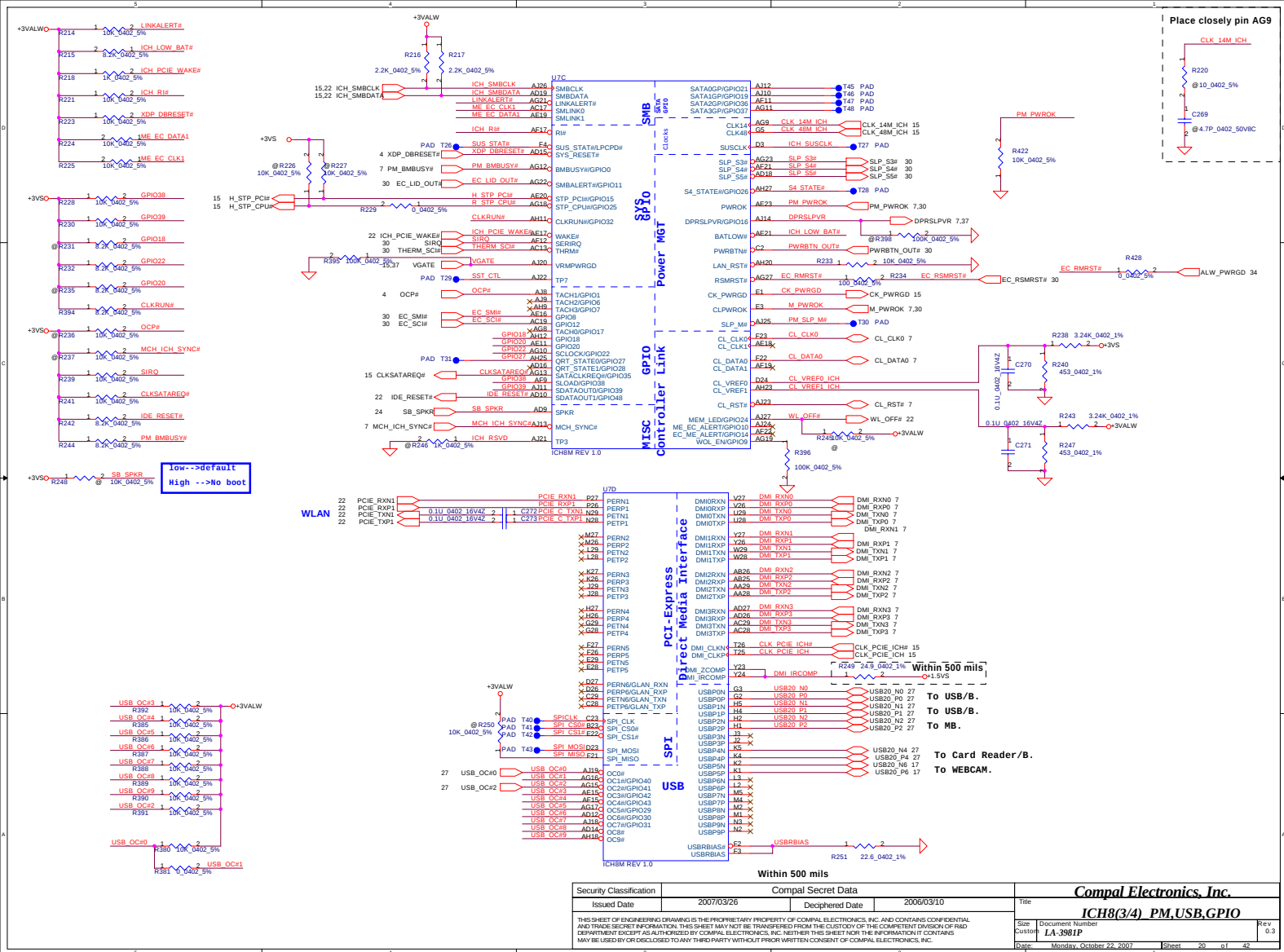
Boot BIOS Strap		
PCI_GNT0#	SPL_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

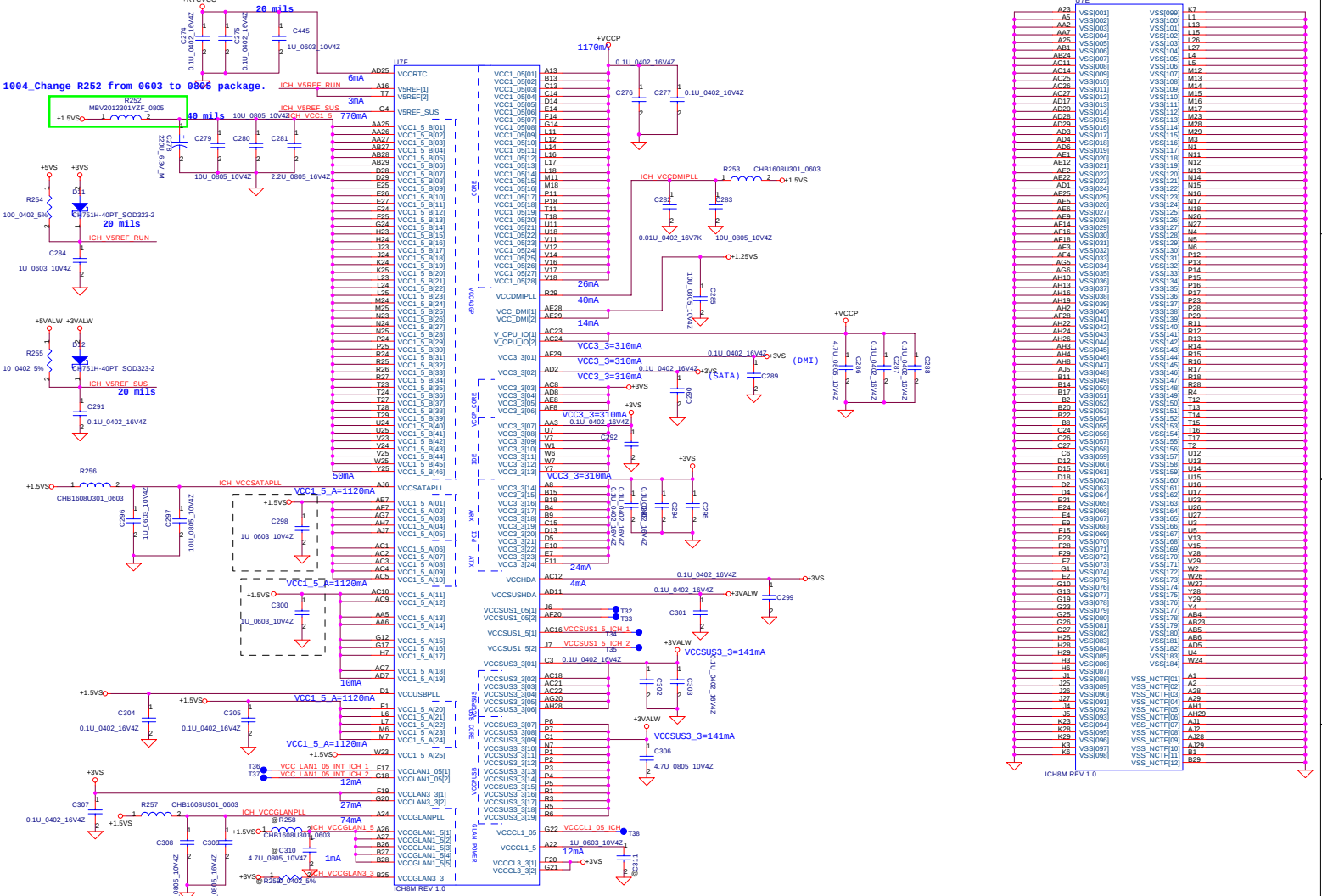
A16 swap override Strap

*Low= A16 swap override Enable High= Default	
PCI_GNT3#	

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Issued Date	2007/03/26	Deciphered Date	2006/03/10	Title Size: Document Number LA-3881P
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				Rev. 0.3

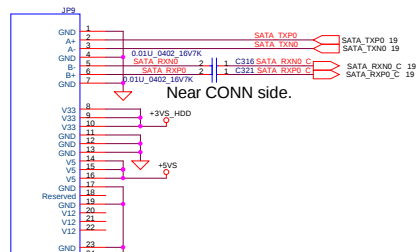
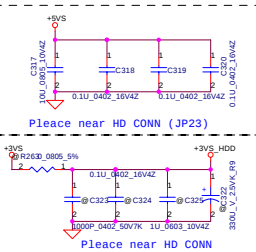
Security Classification		Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	Compal Electronics, Inc. ICH8(2/4) LAN,HD,IDE,LPC	
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				A4	LAN_3981P
Date	Monday, October 22, 2007			Sheet	1 of 42





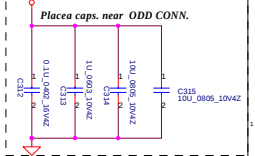
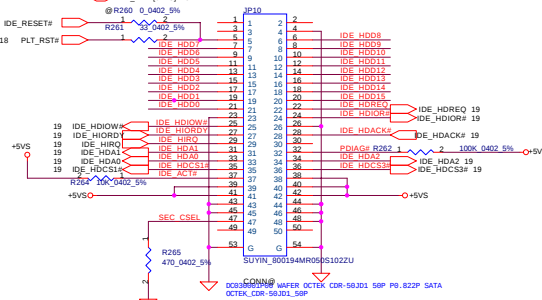
Security Classification		Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	Doc Number	LA-3801P
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HDD Connector

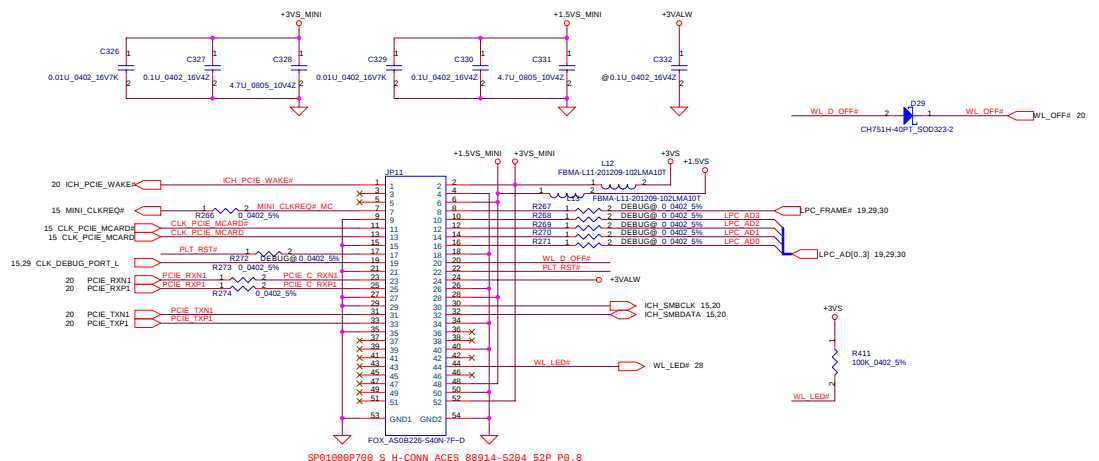


CONN@
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CD-ROM Connector

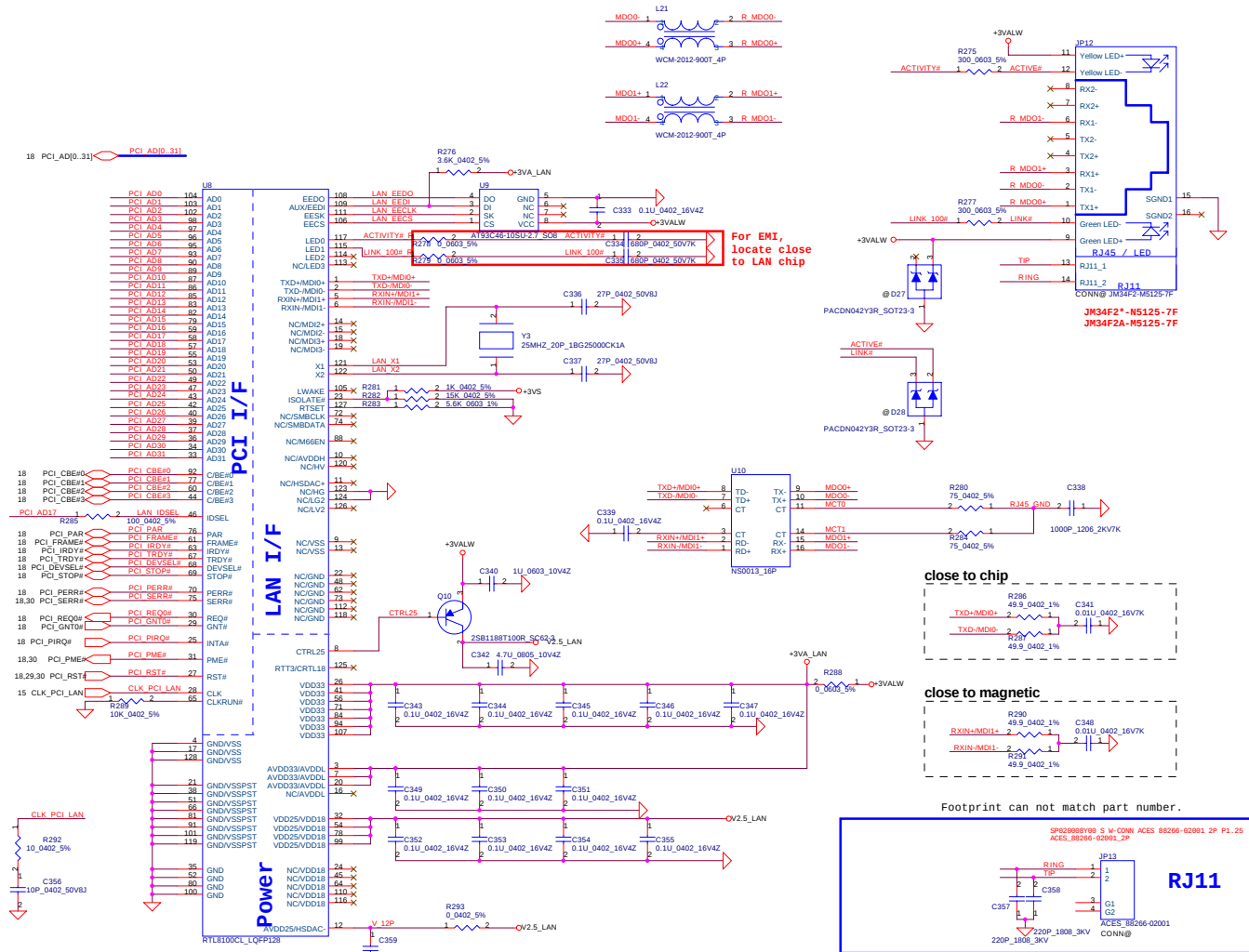


Mini-Express Card---WLAN



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Issued Date		Deciphered Date		HDD/ODD/Mini Card CONN.	
2007/03/26		2007/08/29		LA-3981P	
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		Documents Number		0.3	
		Date		Monday, October 22, 2007	
		Sheet		22 of 42	

Cloase to JP12.



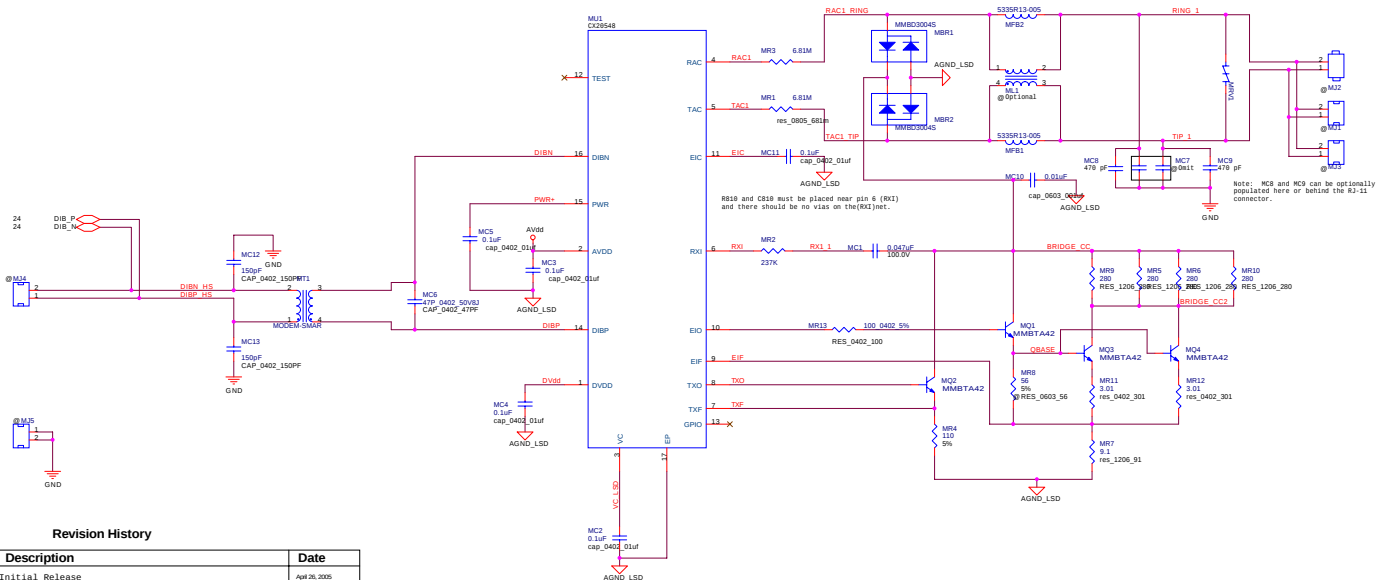
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Compal Electronics, Inc.

LAN-8100CL

LA-3981P

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Issued Date	2007/03/26	Deciphered Date	2006/03/10	AMOC codec		
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Date				Montague, October 27, 2007	Sheet	34 of 42

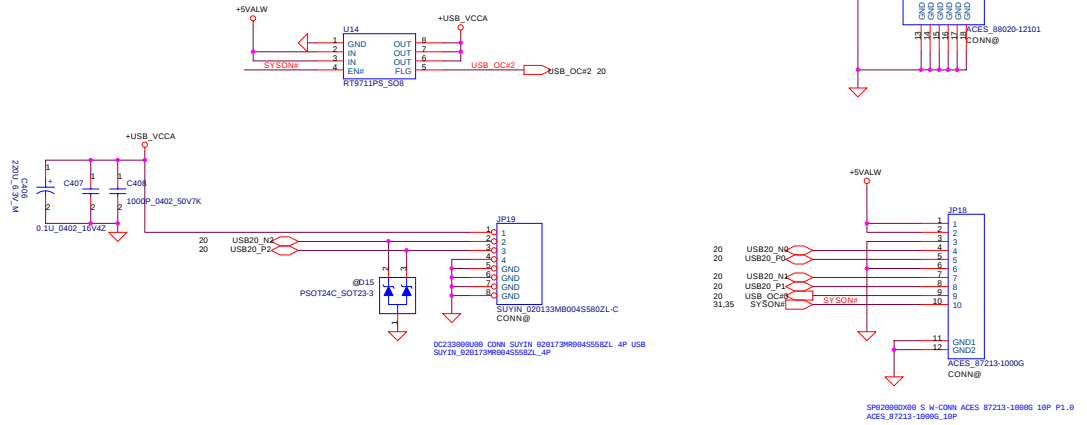


Revision History

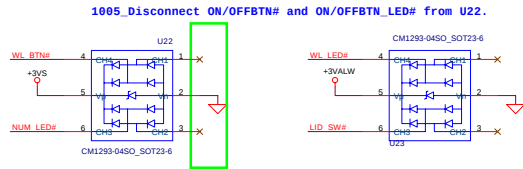
REV	Description	Date
0	Initial Release	April 26, 2005
1	No changes to schematic. PCB updated to -003. Updated footprints and corrected via spacing errors.	August 18, 2005
2	Changed MC8 and MC9 pads. No schematic changes. PCB updated to -005.	November 1, 2005
3	Added MR11 and MR12. PCB updated to -007.	November 18, 2005
4	Added MR13. PCB updated to -009.	January 3, 2006
4.01	AVL update only.	April 20, 2006

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Doc No.	LA-3881P	Rev	0.3
Date	Monday, October 22, 2007	Sheet	25 of 45

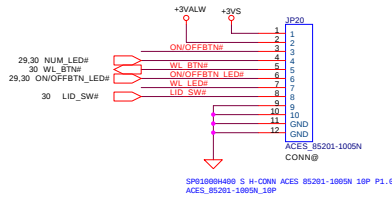
USB Port



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Size		Document Number		Rev	
1		LA-3981P		0.3	
Date		Monday, October 22, 2007		Sheet	
1		27		42	



M/BtoS/B



POWER LED(Left 1)

Battery Charge LED(Left 2)

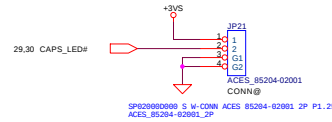
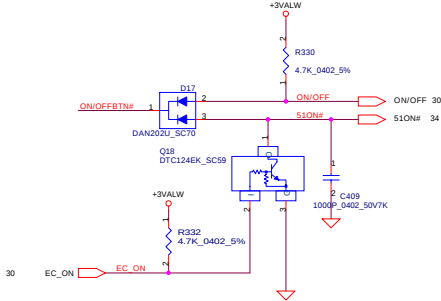
HDD LED(Left 3)

0927_Change R329, R331, R333 (75 ohm), R335 (33 ohm) to 27 ohm.

Wireless ON/OFF LED(Left 4)

Power ON/OFF

M/B to SB(Caps Lock LED)



On (WL_ON#=L) -> Blue
Off (WL_ON#=H) -> Amber

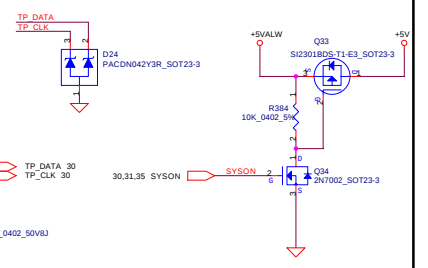
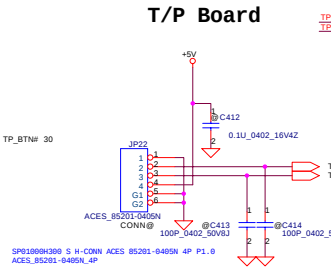
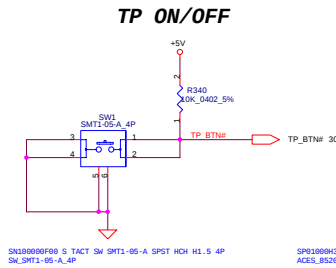
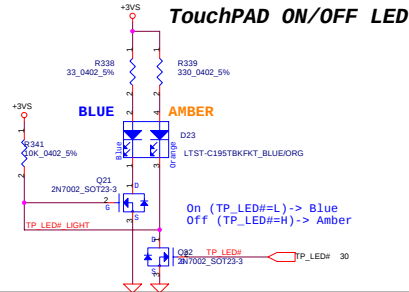


D21, D25, D23 Footprint can not match part number.

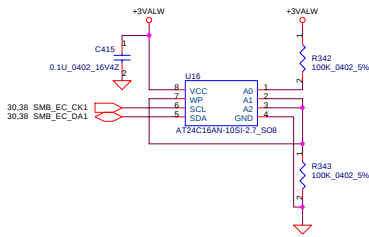
TouchPAD ON/OFF LED

TP ON/OFF

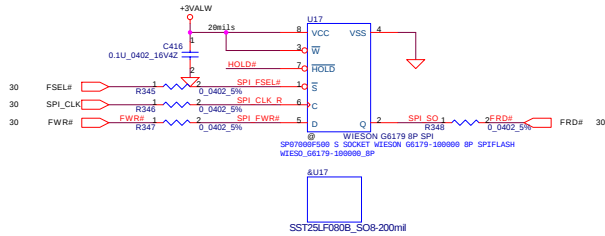
T/P Board



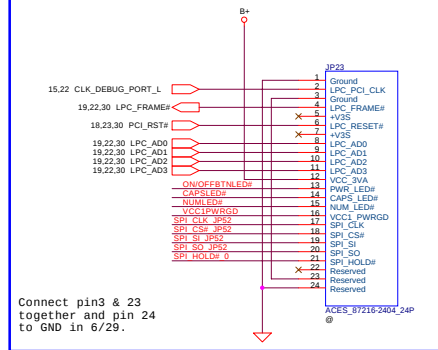
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Issued Date	2007/03/26	Deciphered Date	2006/07/26	Title
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Size		Document Number		Rev
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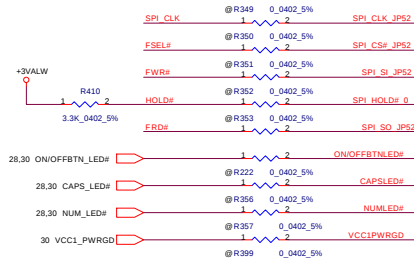
SPI ROM



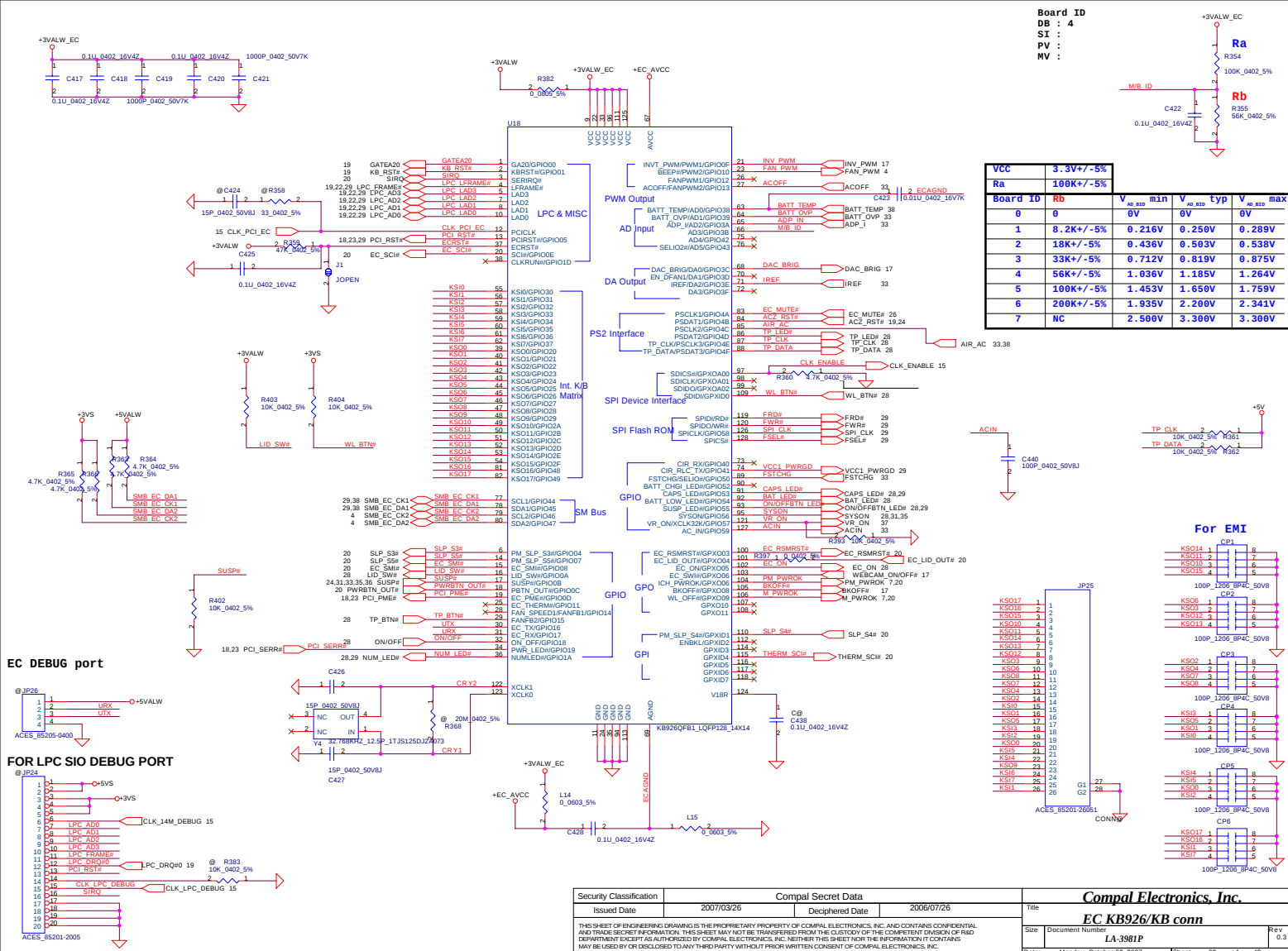
LPC Debug Port

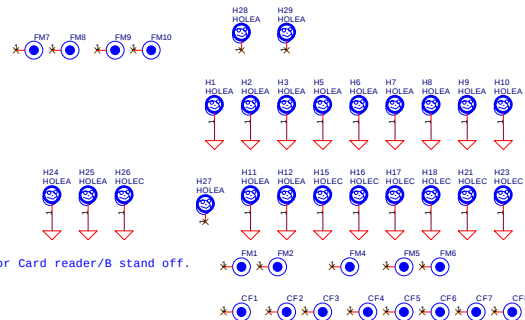
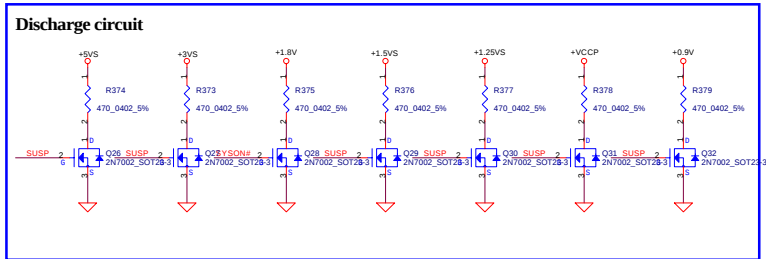
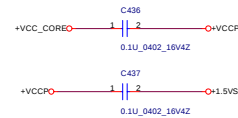
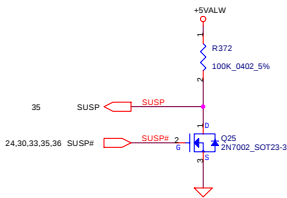
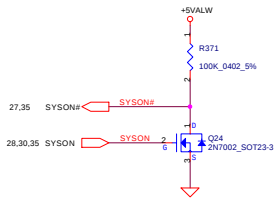
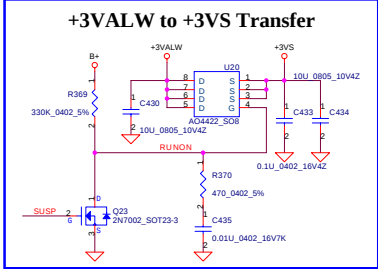
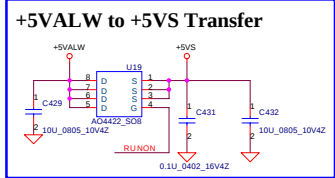


Connect pin3 & 23
together and pin 24
to GND in 6/29.

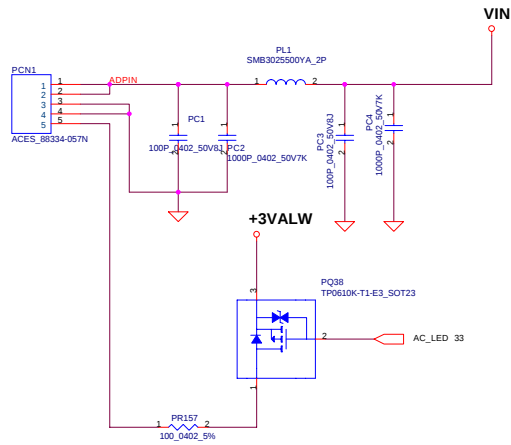


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				Rev	0.3
				Date	Monday, October 22, 2007
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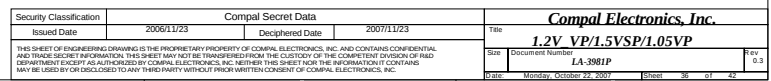


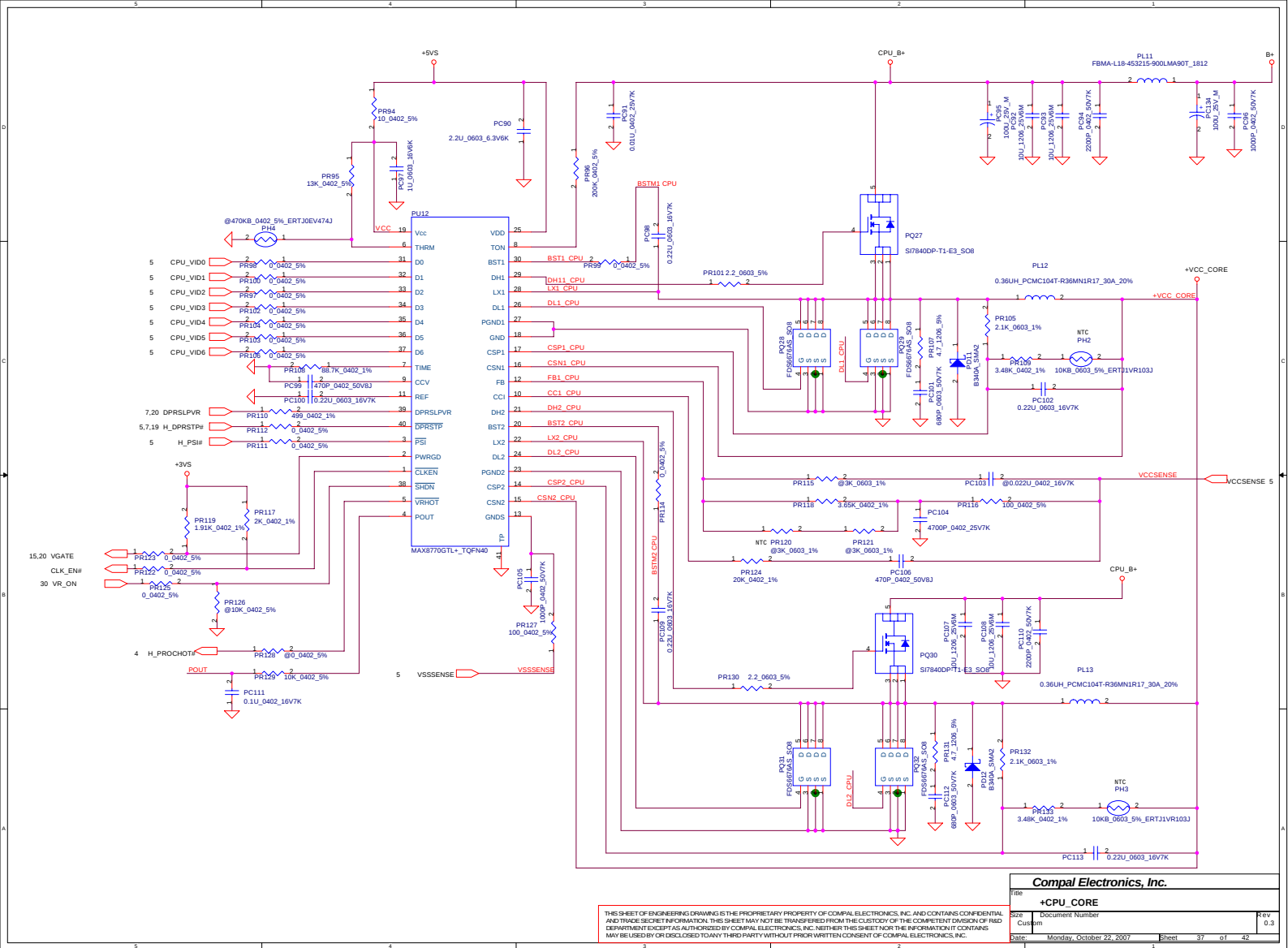
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Issued Date	2007/03/26	Deciphered Date	2006/07/26	DC/DC Interface
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				Document Number LA-3981P	
				Date: Monday, October 22, 2007	Sheet 32 of 42

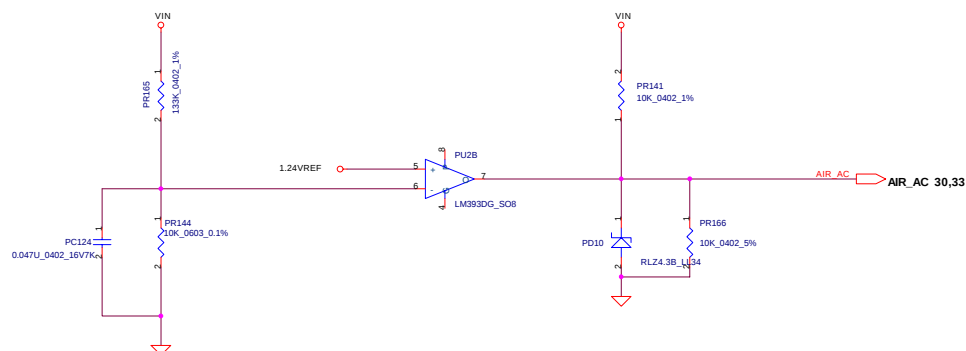
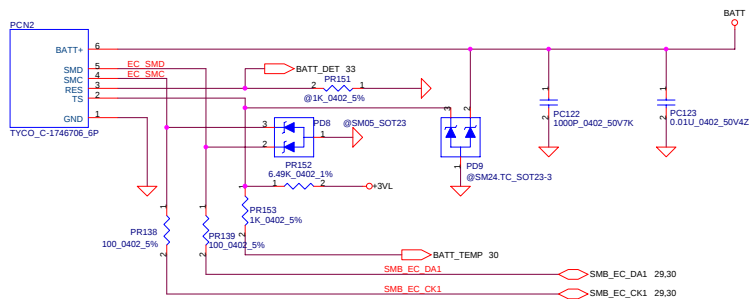
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				Size	Document Number
				Date	Monday, October 22, 2007
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Compal Electronics, Inc.			
File	+CPU_CORE		
Size	Document Number	Rev	
Cust		0.9	
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				Date: Monday, October 22, 2007	Sheet 42 of 38

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Issued Date	2006/02/28	Deciphered Date	2007/02/28	Title
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Version Change List (P. I. R. List) for HW Circuit

Item	Change item	Page	Date	Phase
1	Change C262 and C263 From 15pF to 12pF	19	7/16	DB --> SI
2	Reserved R245 and Add R422	20	7/16	DB --> SI
3	Add D29 prevent leakage issue	22	7/16	DB --> SI
4	Reserved diode D30 D31 for ESD	26	7/16	DB --> SI
5	Reserved R423 for coat down plan	24	7/24	DB --> SI
6	Remove Q12-Q17, R323 R324 R327 R328 R417 R418	26	7/30	DB --> SI
7	Change EXT MIC port B to port C	24	7/31	DB --> SI
8				DB --> SI
9				DB --> SI
10				DB --> SI
11				DB --> SI
12				DB --> SI
13				DB --> SI
14				DB --> SI
15				DB --> SI
16				DB --> SI
17				DB --> SI
18				DB --> SI
19				DB --> SI
20				DB --> SI
21				DB --> SI
22				DB --> SI
23				DB --> SI
24				DB --> SI
25				DB --> SI
26				DB --> SI
27				DB --> SI
28				DB --> SI
29				DB --> SI

Version Change List (P. I. R. List) for HW Circuit

Item	Change item	Page		Date	Phase
1	Change R296 R337 R value	24	Follow conexant new design rule	8/6	SI --> PV
2	Add R424 R425 1000ohm on MIC_EXT_R and MIC_EXT_L	26	Follow conexant new design rule	8/6	SI --> PV
3	Change PIRQ from F to A	18	Choose R419 then control PIRQ A	8/14	SI --> PV
4	Connect PCI_SERR# to EC GPIO pin.	18	Connect PCI_SERR# to EC GPIO pin.	8/31	SI --> PV
5	Modify PC BEEP circuit.	20	Modify PC BEEP circuit.	8/31	SI --> PV
6	For support Intel Penryn CPU.	04	Reserve R426 and R427 for support Intel Penryn CPU.	9/3	SI --> PV
7	For ESD request.	28	Add U22 and U23 for ESD request.	9/3	SI --> PV
8	For EMI request.	26	Add L24-L27	9/5	SI --> PV
9	Change C391, C393, C395, C396 from 0.47uF to 0.047uF.	26	Change C391, C393, C395, C396 from 0.47uF to 0.047uF	9/7	SI --> PV
10	Add R417 and R418 to fine-tune Vp-p.	26	Add R417 and R418 to fine-tune Vp-p.	9/7	SI --> PV
11	For ESD request.	20	Add U22 and U23 for ESD request.	9/7	SI --> PV
12					SI --> PV
13					SI --> PV
14					SI --> PV
15					SI --> PV
16					SI --> PV
17					SI --> PV
18					SI --> PV
19					SI --> PV
20					SI --> PV
21					SI --> PV
22					SI --> PV
23					SI --> PV
24					SI --> PV
25					SI --> PV
26					SI --> PV
27					SI --> PV
28					SI --> PV
29					SI --> PV
30					SI --> PV
31					SI --> PV
32					SI --> PV
33					SI --> PV
34					SI --> PV
35					SI --> PV
36					SI --> PV
37					SI --> PV
38					SI --> PV

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Issued Date	2007/03/26	Deciphered Date	2007/02/28	Title
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Version Change List (P. I. R. List) for HW Circuit

Item	Change item	Page	Date	Phase
1	Solve Vref miss when entry S3 mode.	7	9/25	PV --> MV
2	Solve wave ripple on CR1 and TV.	10	9/25	PV --> MV
3	Solve RTC timing too exceed.	18	9/25	PV --> MV
4	Reduce IN1_MIC noise.	24	9/25	PV --> MV
5	Solve S3 resume fail when use Micron DDR module.	35	10/05	PV --> MV
6	Solve pop noise when entry or resume from S3.	24	9/27	PV --> MV
7	Solve EMI fail for Memory module.	7	9/27	PV --> MV
8	Fine-tune LED brightness.	28	9/27	PV --> MV
9	ICH 1.5V power rail 700mA current requirement.	21	10/04	PV --> MV
10	Solve can not power on when stuff U22.	28	10/05	PV --> MV
11	For EMI request.	16	10/19	PV --> MV
12	To avoid too easy to open solder for CLR2P.	15	10/19	PV --> MV
13	Solve acoustic noise issue.	10	10/22	PV --> MV

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			Date	LA-3801P
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