

Compal Confidential

Cougar 2.0

Schematics Document

Intel Cedar Trail Processor/ Tiger point

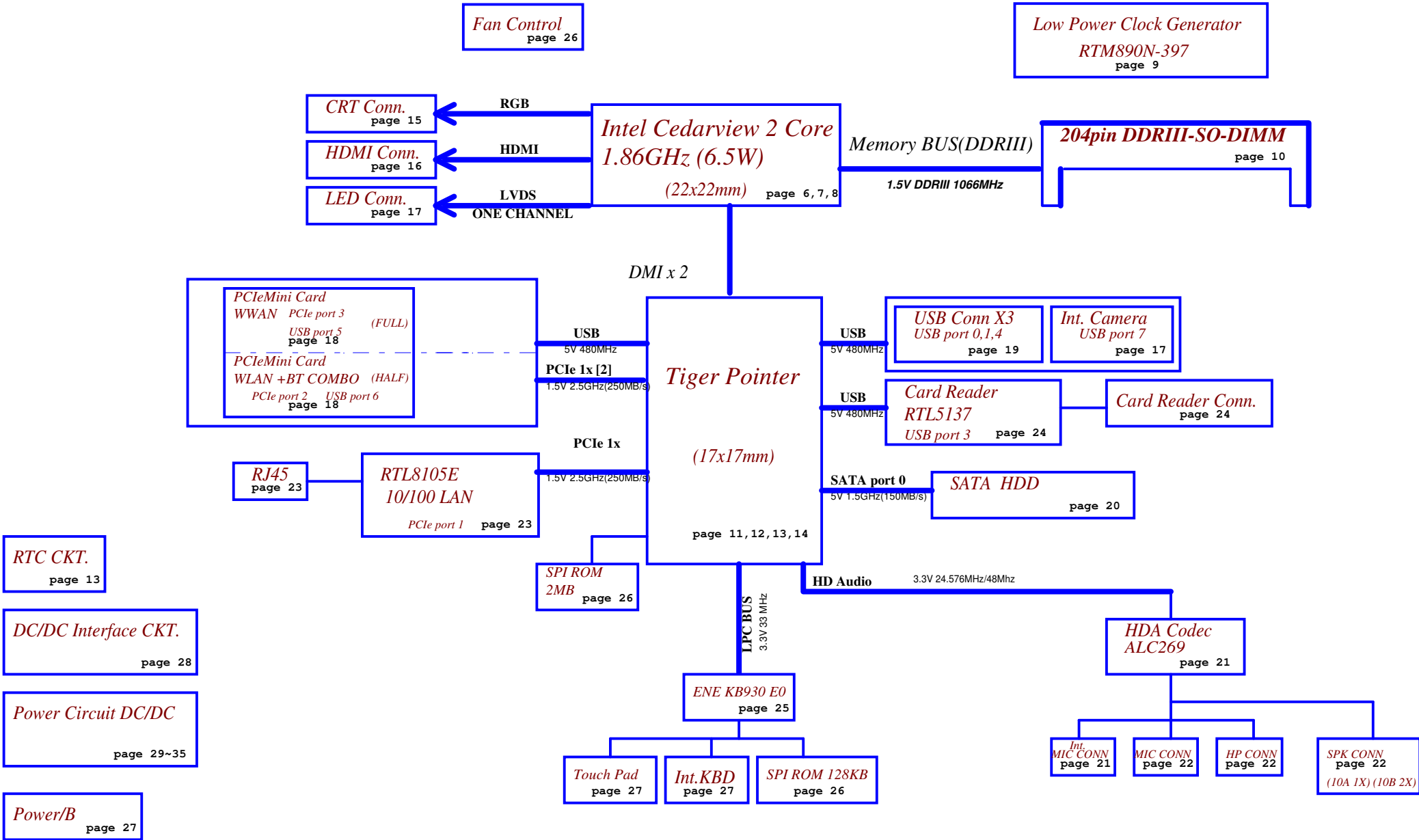
2011-11-07

LA-6858P REV:1.0

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Model Name : Cougar 2.0
Project Code : QBU00



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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+GFX_CORE	GFX support voltage	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	VCCP switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	OFF	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON
+3VS_PRIME	3.3V power rail for CPU and PCH	ON	OFF	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

Function	Mini PCI-E SLOT			Display		Clock gen	
description							
explain	Wi-Fi	WWAN	3G	CRT	HDMI	Tpye	
BTO	WLAN@	WWAN@	3G@	CRT@	HDMI@	low@	normal@

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 010X b

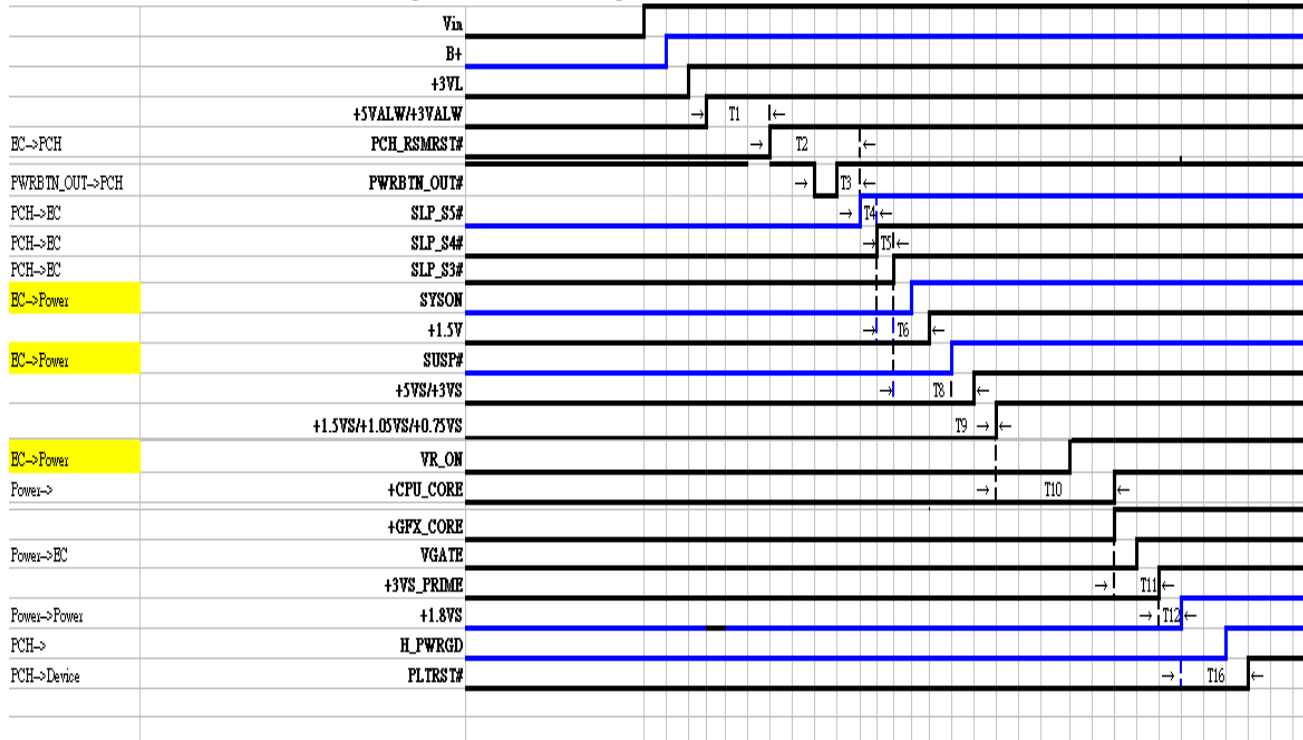
EC SM Bus2 address

NM10 SM Bus address

Device	Address
Clock Generator (SLG8SP56VTR)	1101 001Xb
DDR DIMMA	1010 000Xb
WWAN/WLAN	

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QBU00 Power ON sequence

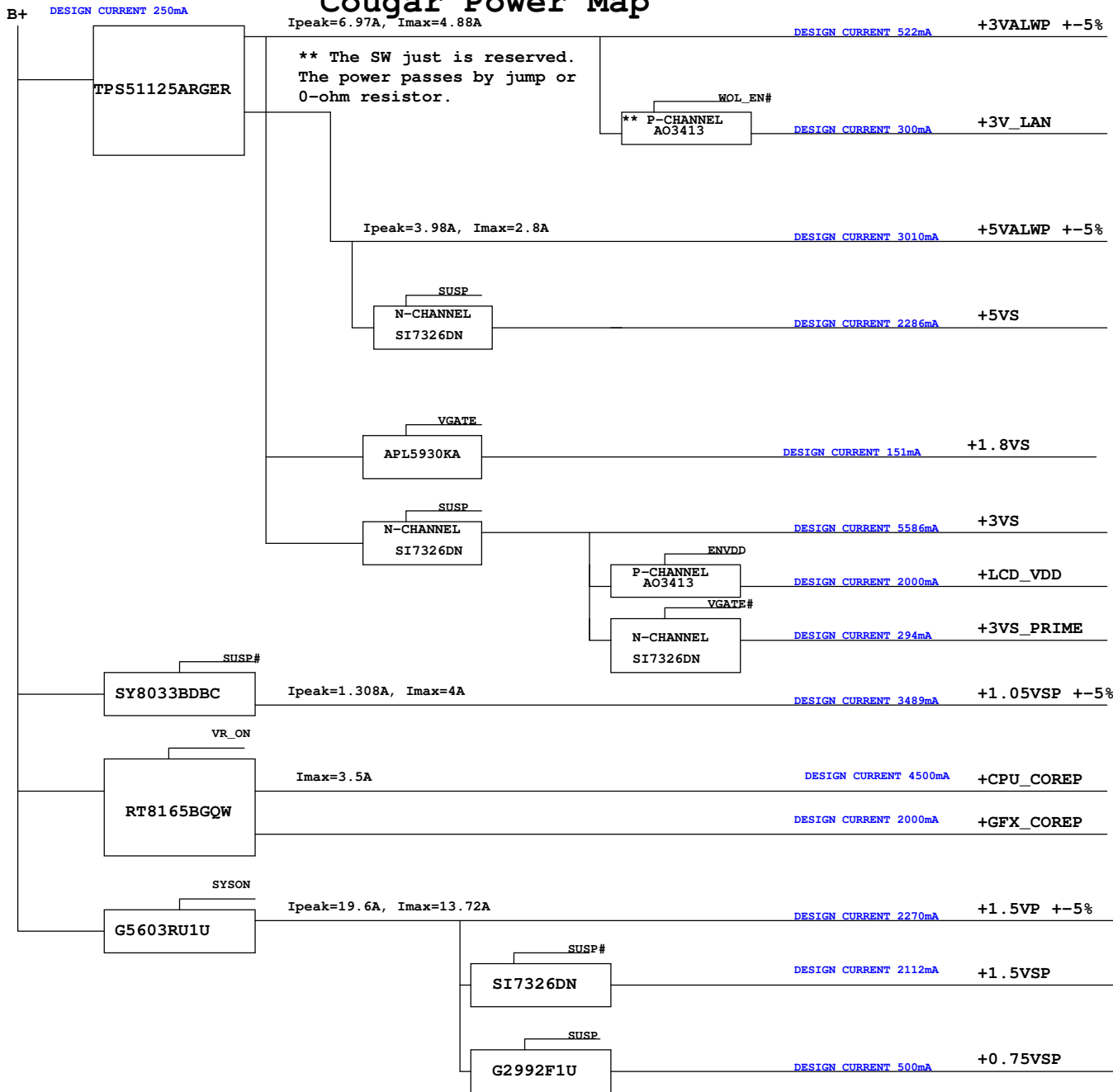


Power-on Sequence

Time	Description	Expected
T1	+5V/3VALW to PCH_RSMRST# inactive	>0ms
T2	PCH_RSMRST# inactive to SLP_S5# inactive	<110ms
T3	PWRBTN_OUT# inactive to SLP_S5# inactive	>0ms
T4	SLP_S5# inactive to SLP_S4# inactive	28.992us ~ 64.088us
T5	SLP_S4# inactive to SLP_S3# inactive	28.992us ~ 64.088us
T6	SLP_S4# inactive to +1.5V active	>0ms
T8	SLP_S3# inactive to +5VS inactive	>0ms
T9	+1.5VS active to +1.05VS active	>0ms
T10	+1.05VS active to +CPU_CORE	>0ms
T11	+CPU_CORE active to +3.3V_PRIME	>0ms
T12	+3.3V_PRIME active to +1.8VS	3.3-1.8<700mV
T16	H_PWRGD inactive to PLTRST# inactive	34<RTCCLK<41

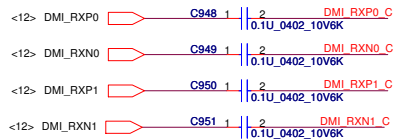
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			Power sequence	
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Cougar Power Map

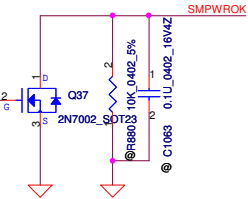


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+1.5V pull up must be placed within 500 mils from Cedarview



<28> SYSON#



<10> DDR_A_MA[0..15]
<10> DDR_A_DQS[0..7]
<10> DDR_A_DM[0..7]
<10> DDR_A_DQS[0..7]
<10> DDR_A_D[0..63]

DDR_A_MA0 AK14
DDR_A_MA1 AK16
DDR_A_MA2 AJ14
DDR_A_MA3 AJ18
DDR_A_MA4 AK18
DDR_A_MA5 AH18
DDR_A_MA6 AJ18
DDR_A_MA7 AJ18
DDR_A_MA8 AJ20
DDR_A_MA9 AH20
DDR_A_MA10 AJ12
DDR_A_MA11 AK21
DDR_A_MA12 AJ21
DDR_A_MA13 AJ8
DDR_A_MA14 AH22
DDR_A_MA15 AJ22

N2800@
U1
QB0Y B2 1.86G

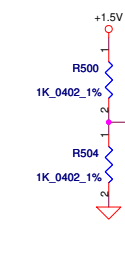
U1B N2600@
Cedarview
REV = 1.10

DDR3_DQ0 Y30 DDR_A_D0
DDR3_DQ1 Y29 DDR_A_D1
DDR3_DQ2 AC30 DDR_A_D2
DDR3_DQ3 AC31 DDR_A_D3
DDR3_DQ4 W31 DDR_A_D4
DDR3_DQ5 W28 DDR_A_D5
DDR3_DQ6 AB28 DDR_A_D6
DDR3_DQ7 AB30 DDR_A_D7
DDR3_DQ8 AA24 DDR_A_D8
DDR3_DQ9 AA22 DDR_A_D9
DDR3_DQ10 AE27 DDR_A_D10
DDR3_DQ11 AE26 DDR_A_D11
DDR3_DQ12 AD27 DDR_A_D12
DDR3_DQ13 AD25 DDR_A_D13
DDR3_DQ14 AD27 DDR_A_D14
DDR3_DQ15 AD23 DDR_A_D15
DDR3_DQ16 AE29 DDR_A_D16
DDR3_DQ17 AE29 DDR_A_D17
DDR3_DQ18 AJ30 DDR_A_D18
DDR3_DQ19 AD28 DDR_A_D19
DDR3_DQ20 AD30 DDR_A_D20
DDR3_DQ21 AD30 DDR_A_D21
DDR3_DQ22 AG30 DDR_A_D22
DDR3_DQ23 AJ29 DDR_A_D23
DDR3_DQ24 AE24 DDR_A_D24
DDR3_DQ25 AG24 DDR_A_D25
DDR3_DQ26 AD22 DDR_A_D26
DDR3_DQ27 AC21 DDR_A_D27
DDR3_DQ28 AG25 DDR_A_D28
DDR3_DQ29 AG21 DDR_A_D29
DDR3_DQ30 AE21 DDR_A_D30
DDR3_DQ31 AE21 DDR_A_D31
DDR3_DQ32 AD13 DDR_A_D32
DDR3_DQ33 AD11 DDR_A_D33
DDR3_DQ34 AG8 DDR_A_D34
DDR3_DQ35 AG7 DDR_A_D35
DDR3_DQ36 AG13 DDR_A_D36
DDR3_DQ37 AE13 DDR_A_D37
DDR3_DQ38 AD10 DDR_A_D38
DDR3_DQ39 AE8 DDR_A_D39
DDR3_DQ40 AH2 DDR_A_D40
DDR3_DQ41 AD2 DDR_A_D41
DDR3_DQ42 AD3 DDR_A_D42
DDR3_DQ43 AD3 DDR_A_D43
DDR3_DQ44 AH4 DDR_A_D44
DDR3_DQ45 AE4 DDR_A_D45
DDR3_DQ46 AE2 DDR_A_D46
DDR3_DQ47 AD4 DDR_A_D47
DDR3_DQ48 AD7 DDR_A_D48
DDR3_DQ49 AD6 DDR_A_D49
DDR3_DQ50 AA6 DDR_A_D50
DDR3_DQ51 AB5 DDR_A_D51
DDR3_DQ52 AE8 DDR_A_D52
DDR3_DQ53 AE5 DDR_A_D53
DDR3_DQ54 AA8 DDR_A_D54
DDR3_DQ55 AB2 DDR_A_D55
DDR3_DQ56 AB4 DDR_A_D56
DDR3_DQ57 LW4 DDR_A_D57
DDR3_DQ58 V3 DDR_A_D58
DDR3_DQ59 AC2 DDR_A_D59
DDR3_DQ60 AB3 DDR_A_D60
DDR3_DQ61 Y2 DDR_A_D61
DDR3_DQ62 W1 DDR_A_D62
DDR3_DQ63 AA30 DDR_A_D63
DDR3_DQ64 AA31 DDR_A_D64
DDR3_DQ65 AB25 DDR_A_D65
DDR3_DQ66 AF29 DDR_A_D66
DDR3_DQ67 AE22 DDR_A_D67
DDR3_DQ68 AG10 DDR_A_D68
DDR3_DQ69 AF4 DDR_A_D69
DDR3_DQ70 AB6 DDR_A_D70
DDR3_DQ71 Y3 DDR_A_D71
DDR3_DQ72 AA31 DDR_A_D72
DDR3_DQ73 AB25 DDR_A_D73
DDR3_DQ74 AF29 DDR_A_D74
DDR3_DQ75 AE22 DDR_A_D75
DDR3_DQ76 AG10 DDR_A_D76
DDR3_DQ77 AF4 DDR_A_D77
DDR3_DQ78 AB6 DDR_A_D78
DDR3_DQ79 Y3 DDR_A_D79
DDR3_DQ80 AA31 DDR_A_D80
DDR3_DQ81 AB25 DDR_A_D81
DDR3_DQ82 AF29 DDR_A_D82
DDR3_DQ83 AE22 DDR_A_D83
DDR3_DQ84 AG10 DDR_A_D84
DDR3_DQ85 AF4 DDR_A_D85
DDR3_DQ86 AB6 DDR_A_D86
DDR3_DQ87 Y3 DDR_A_D87

<10> DRAMRST#
<10> M_CLK_DDR2
<10> M_CLK_DDR3
<10> M_CLK_DDR3

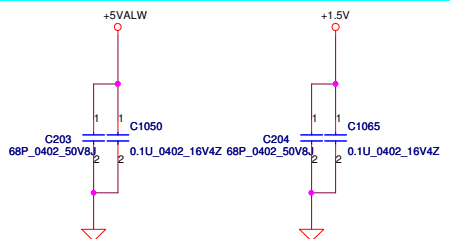
<9> CLK_CPU_MPLL_C
<9> CLK_CPU_MPLL_C

<33> SM_PWROK

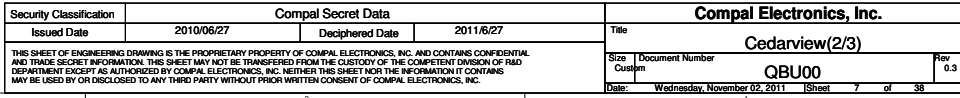


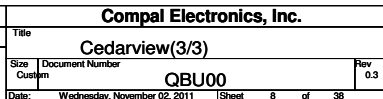
<7> XDP_DBREST#

<13> PCH_POK



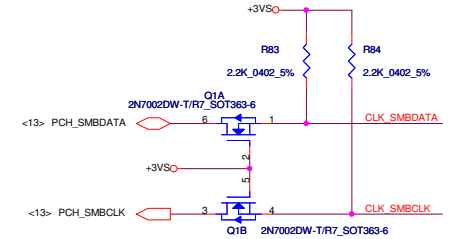
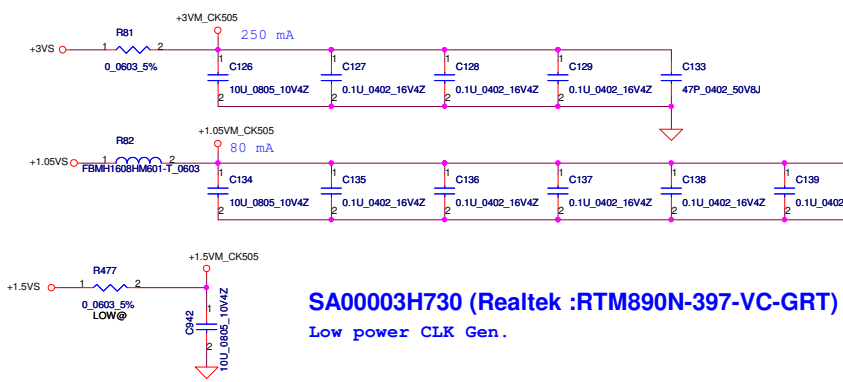
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FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								

	Normal Power	Low Power
R477	@	Stuff
R478	Stuff	@
R479	Stuff	@
R480	@	Stuff
R483	@	Stuff



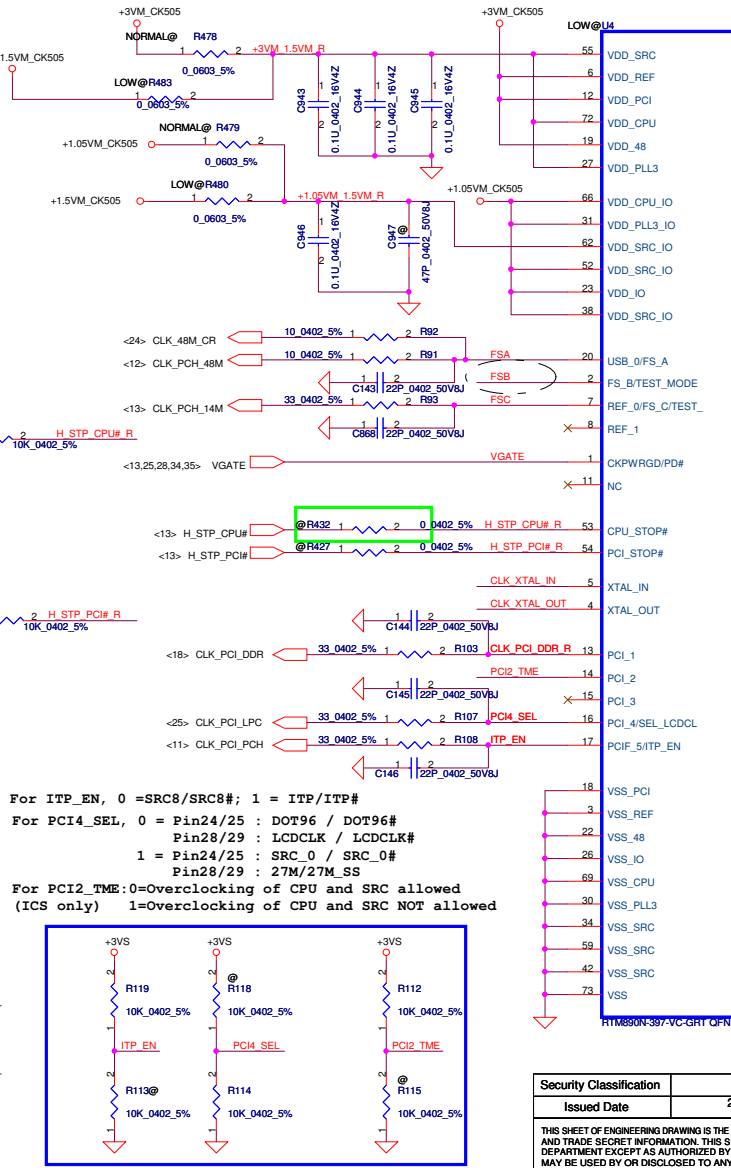
2011.04.29 Reserve R305, C392 for RF

SRC PORT LIST

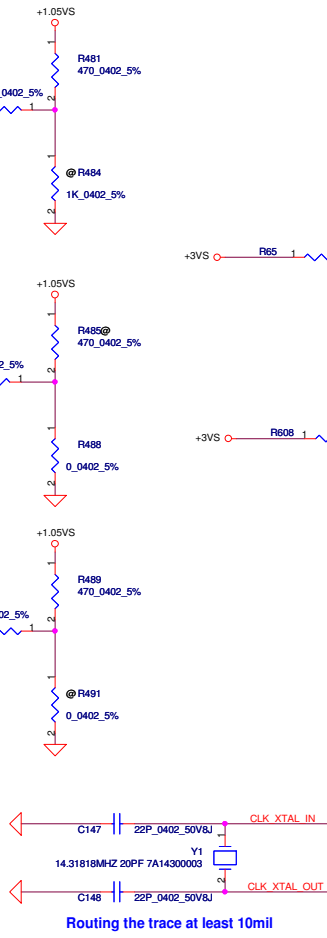
PORT	DEVICE
SRC0	CPU_DREFCLK
SRC2	
SRC3	CPU_EXP
SRC4	PCIE_SATA
SRC6	PCIE_WLAN
SRC7	
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_PCH
SRC11	PCIE_WWAN

REQ PORT LIST

PORT	DEVICE
REQ_3#	
REQ_4#	
REQ_6#	PEIC_WLAN
REQ_7#	
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PEIC_WWAN
REQ_A#	



SDA	9	CLK_SMBDATA	CLK_SMBDATA <10,18>
SCL	10	CLK_SMBCLK	CLK_SMBCLK <10,18>
CPU_0	71	CLK_CPU_HPLCLK	CLK_CPU_HPLCLK <7>
CPU_0#	70	CLK_CPU_HPLCLK#	CLK_CPU_HPLCLK# <7>
CPU_1	68	CLK_CPU_MPLL_C	CLK_CPU_MPLL_C <6>
CPU_1#	67	CLK_CPU_MPLL#_C	CLK_CPU_MPLL#_C <6>
SRC_0/DOT_96	24	CPU_DREFCLK	CPU_DREFCLK <7>
SRC_0#	25	CPU_DREFCLK#	CPU_DREFCLK# <7>
LDCLK/27M	28	CPU_SSCDREFCLK	CPU_SSCDREFCLK <7>
LDCLK#/27M_SS	29	CPU_SSCDREFCLK#	CPU_SSCDREFCLK# <7>
SRC_2	32	2011.06.29 Swap CLK Gen output for CPU_SSCDREFCLK and CPU_DREFCLK	
SRC_2#	33		
SRC_3	35	CLK_CPU_EXP	CLK_CPU_EXP <6>
SRC_3#	36	CLK_CPU_EXP#	CLK_CPU_EXP# <6>
SRC_4	39	CLK_PCIE_SATA	CLK_PCIE_SATA <11>
SRC_4#	40	CLK_PCIE_SATA#	CLK_PCIE_SATA# <11>
SRC_6	57	CLK_PCIE_WLAN	CLK_PCIE_WLAN <18>
SRC_6#	56	CLK_PCIE_WLAN#	CLK_PCIE_WLAN# <18>
SRC_7	61		
SRC_7#	60		
SRC_8/CPU_ITP	64	CPU_ITP	0.0402_5% R880@ T77
SRC_8#/CPU_ITP#	63	CPU_ITP#	0.0402_5% R883@ T78
SRC_9	44	CLK_PCIE_LAN	CLK_PCIE_LAN <23>
SRC_9#	45	CLK_PCIE_LAN#	CLK_PCIE_LAN# <23>
SRC_10	50	CLK_PCIE_PCH	CLK_PCIE_PCH <12>
SRC_10#	51	CLK_PCIE_PCH#	CLK_PCIE_PCH# <12>
SRC_11	48	CLK_PCIE_WWAN	CLK_PCIE_WWAN <18>
SRC_11#	47	CLK_PCIE_WWAN#	CLK_PCIE_WWAN# <18>
CLKREQ_3#	37		
CLKREQ_4#	41		
CLKREQ_6#	58	WLAN_CLKREQ#	WLAN_CLKREQ# <18>
CLKREQ_7#	65		
CLKREQ_9#	43	LAN_CLKREQ#	LAN_CLKREQ# <23>
CLKREQ_10#	49		
CLKREQ_11#	46	WWAN_CLKREQ#	WWAN_CLKREQ# <18>
USB_1/CLKREQ_A#	21		

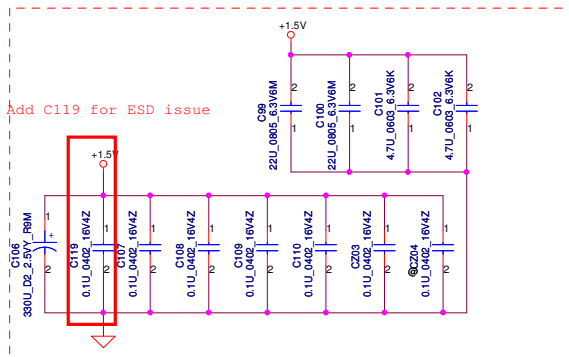


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Issued Date	2010/06/27	Clock Generator CK505
Deciphered Date	2011/6/27	Size Document Number
		QBU00
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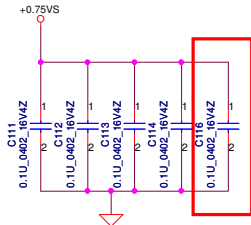
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<6> DDR_A_D[0..63]
<6> DDR_A_DM[0..7]
<6> DDR_A_DQS[0..7]
<6> DDR_A_MA[0..15]

Layout Note:
Place near JDDR1

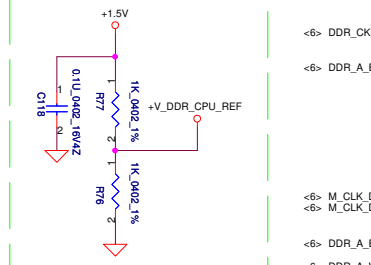
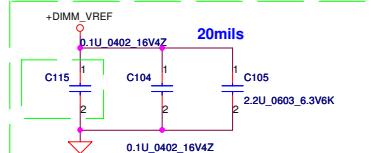
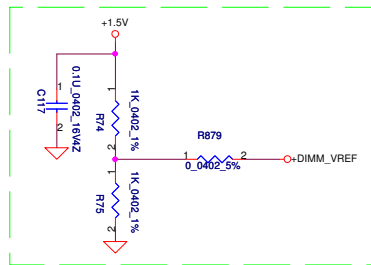
2011.06.14 Add C119 for ESD issue



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.75VS



2011.06.14 Add C116 for ESD issue



<6> DDR_CKE2
<6> DDR_A_BS2
<6> M_CLK_DDR2
<6> M_CLK_DDR#2
<6> DDR_A_BS0
<6> DDR_A_WE#
<6> DDR_A_CAS#
<6> DDR_CS3#

DVT# SA0 change to
pull high +3VS

+3VS

10K 0.402 5%

0.1U 0.0402 16V4Z

0.1U 0.0402 16V4Z

0.1U 0.0402 16V4Z

0.1U 0.0402 16V4Z

0.1U 0.0402 16V4Z

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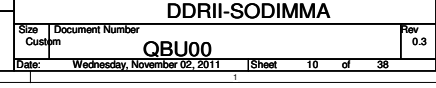
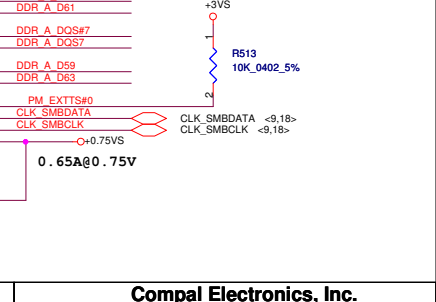
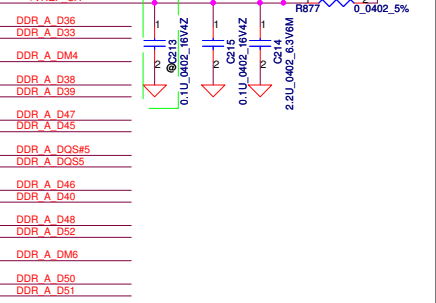
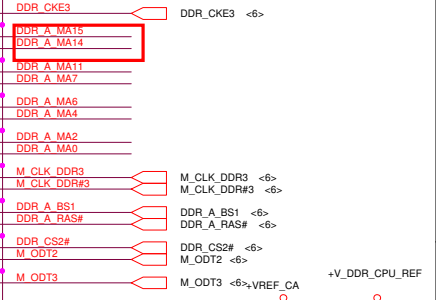
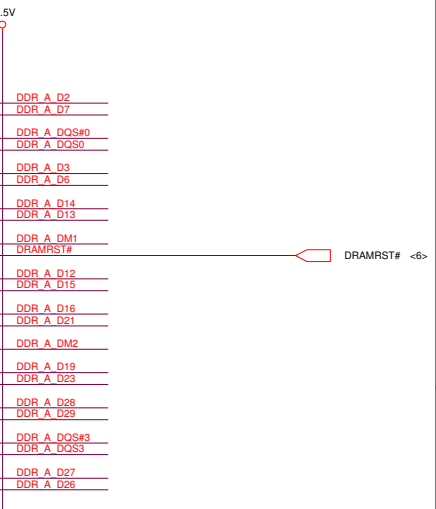
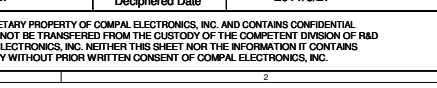
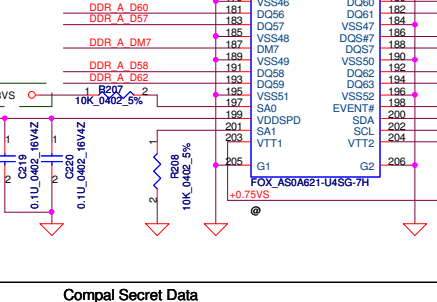
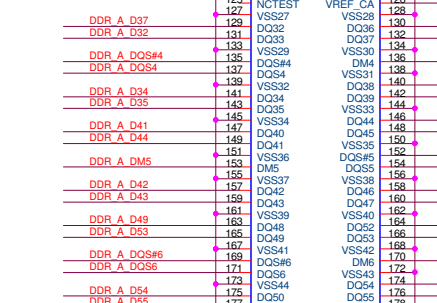
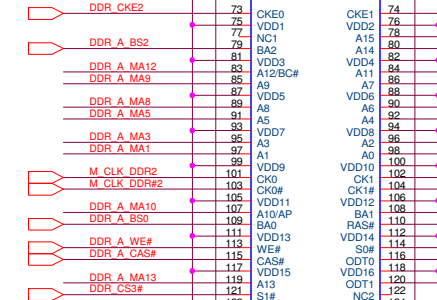
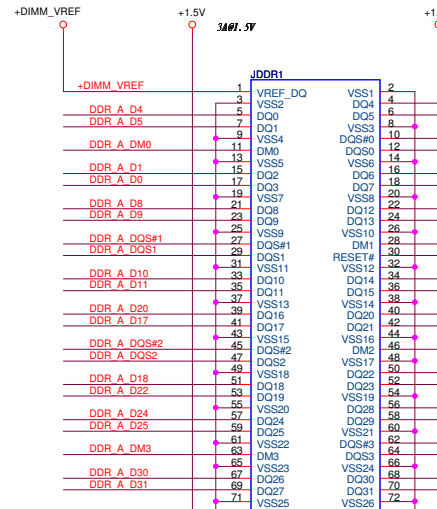
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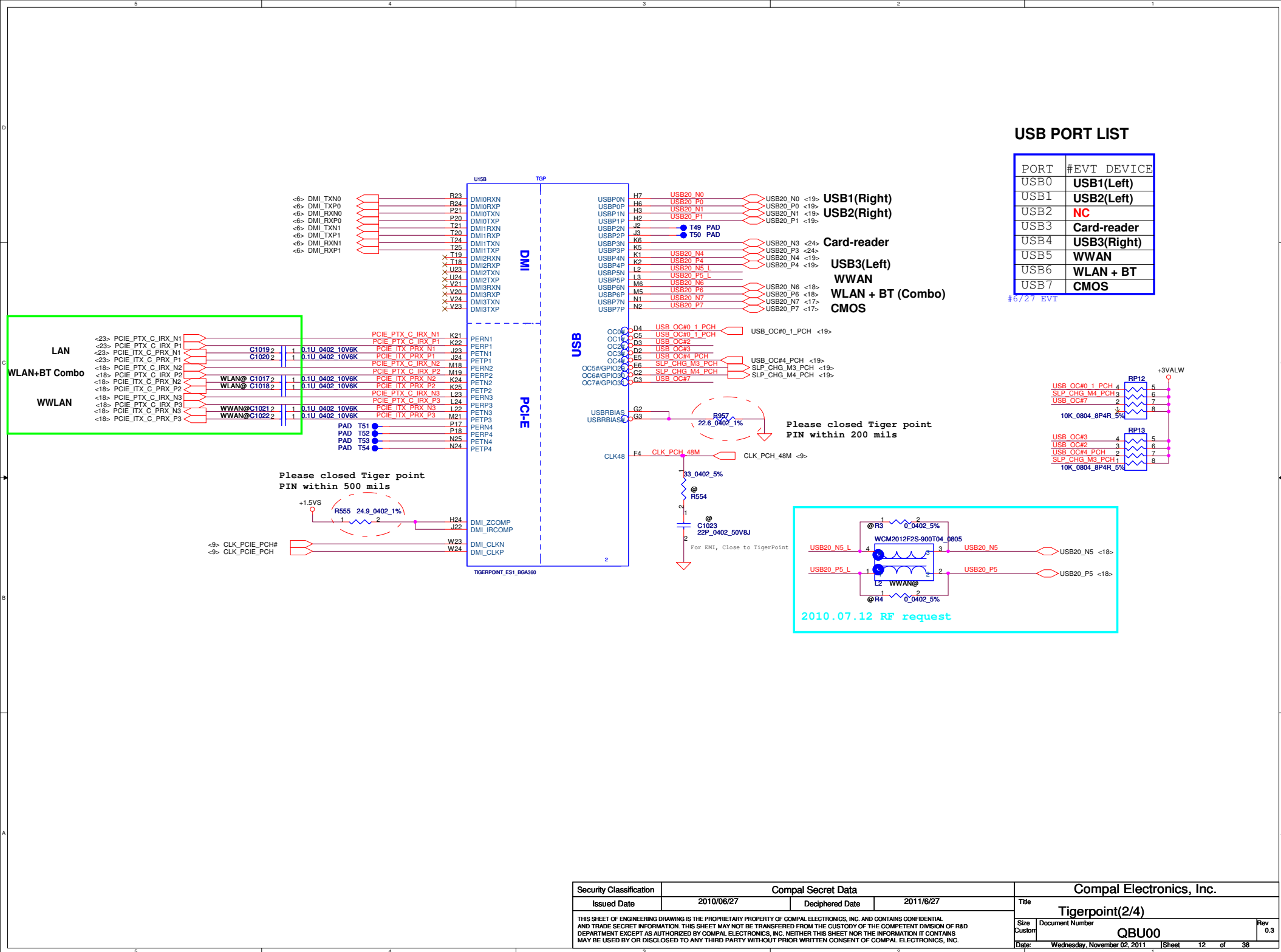
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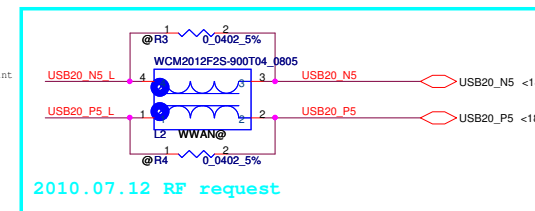
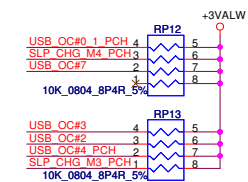
Security Classification	Compal Secret Data		Title	
Issued Date	2010/06/27	Deciphered Date	2011/6/27	DDR II-SODIMMA
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				Document Number QBU00
				Rev 0.3
				Date: Wednesday, November 02, 2011
				Sheet 10 of 38

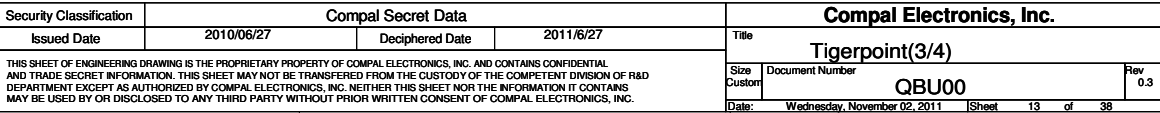


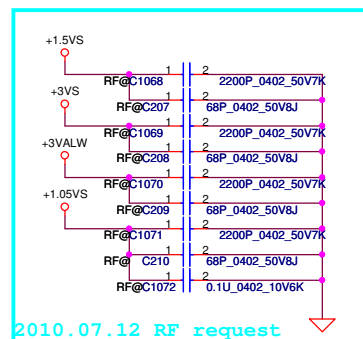
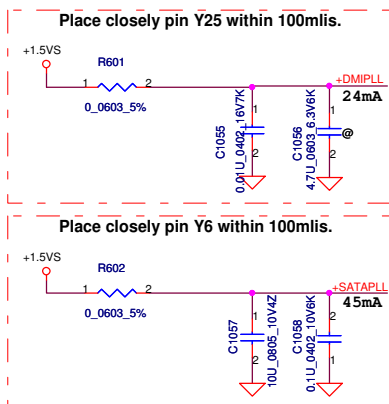
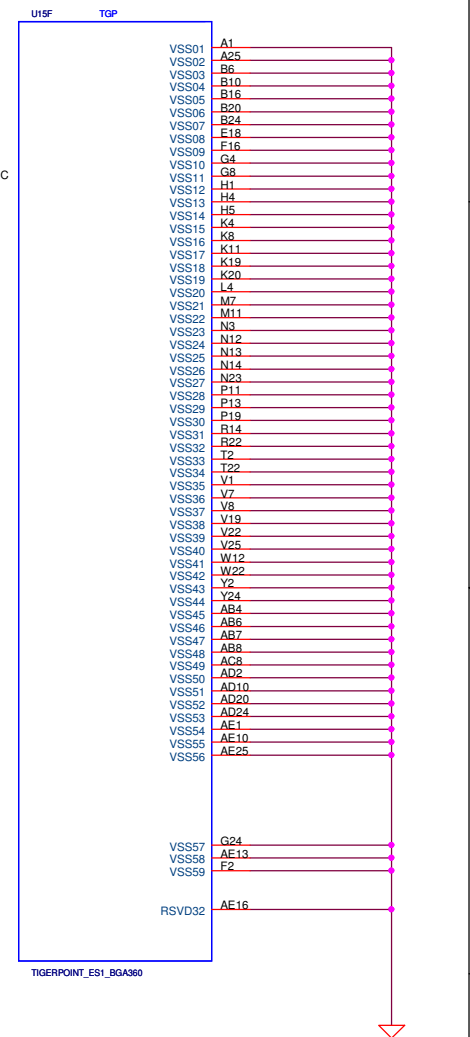
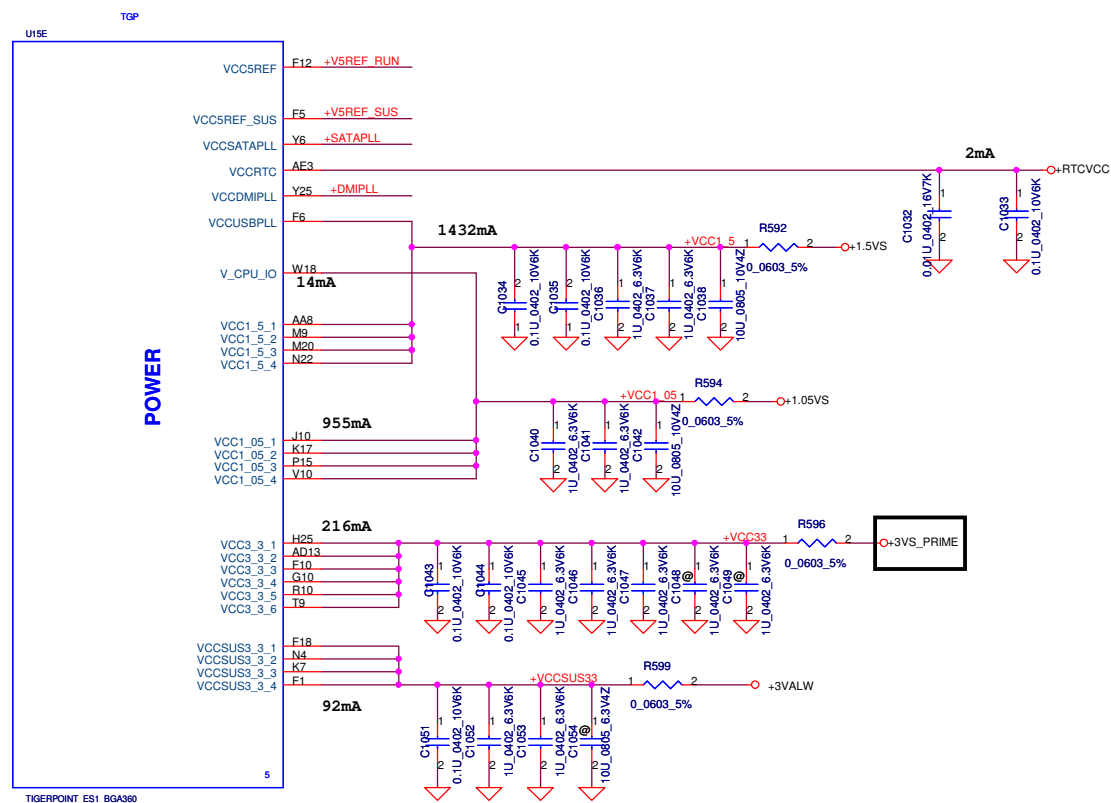
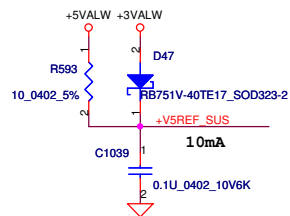
USB PORT LIST

PORT	#EVT DEVICE
USB0	USB1(Left)
USB1	USB2(Left)
USB2	NC
USB3	Card-reader
USB4	USB3(Right)
USB5	WWAN
USB6	WLAN + BT
USB7	CMOS

#6/27 EVT

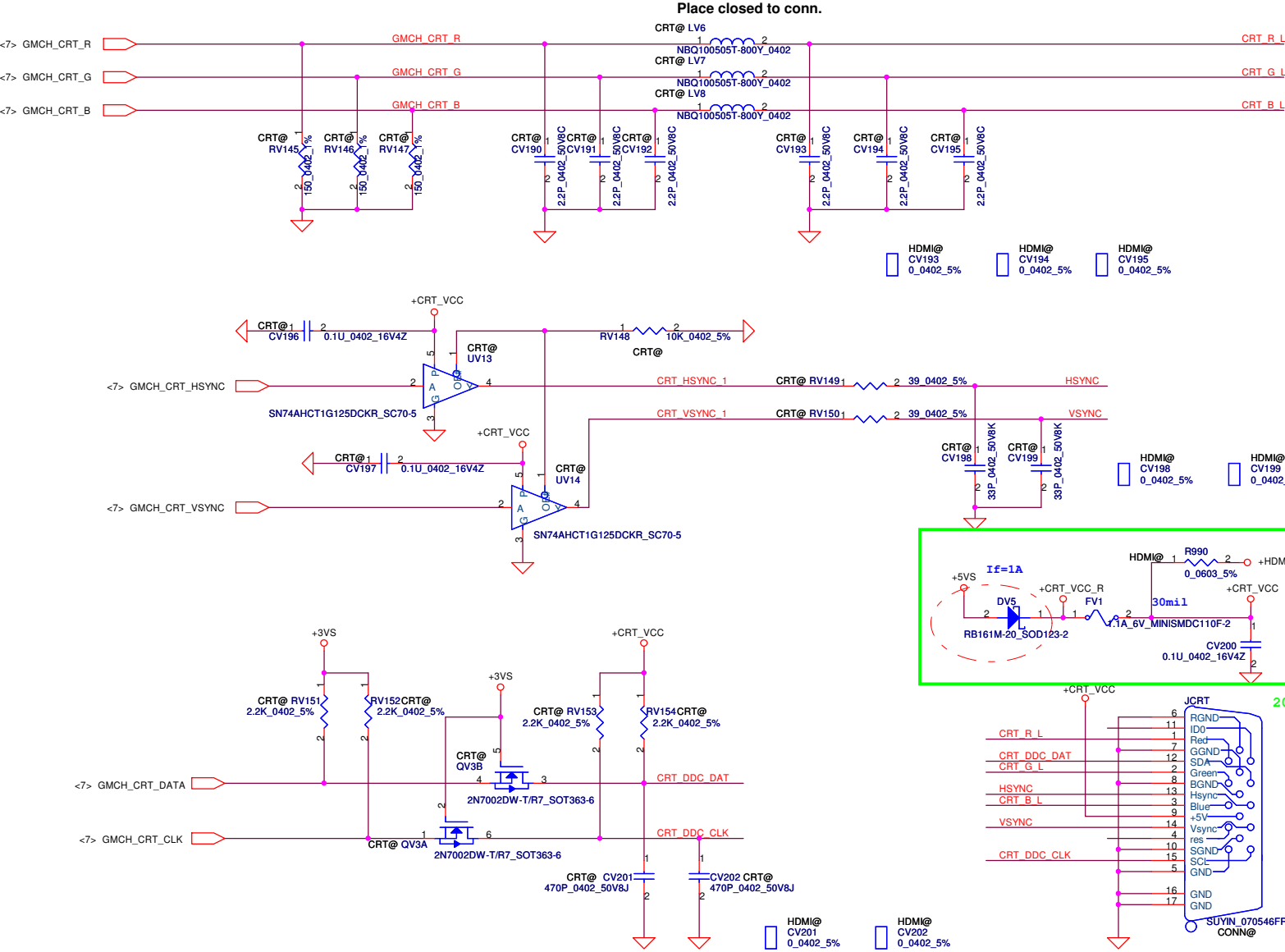






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Issued Date	2010/06/27	Deciphered Date	2011/6/27	Title Tigerpoint(4/4)		
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				Custom	QBU00	0.3
				Date:	Wednesday, June 29, 2011	Sheet 14 of 38

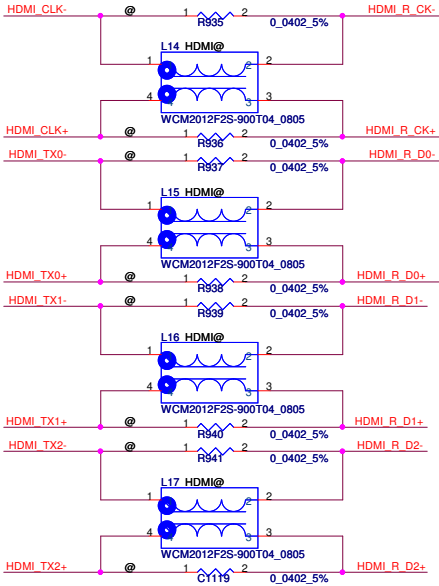
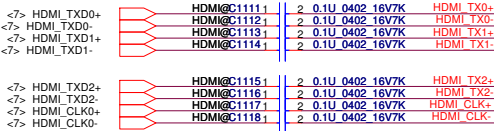
CRT CONNECTOR



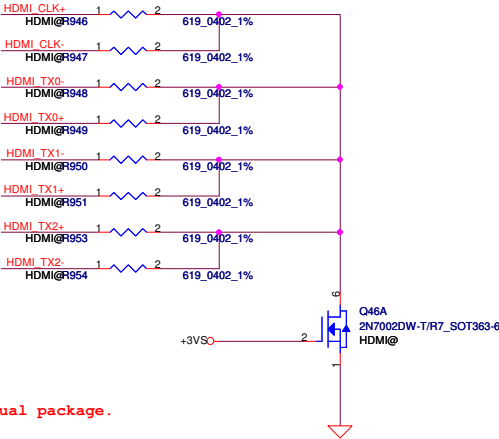
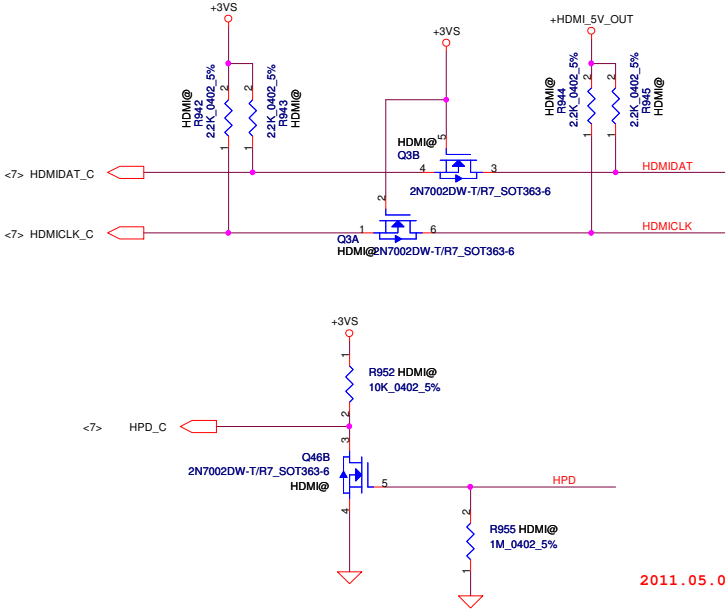
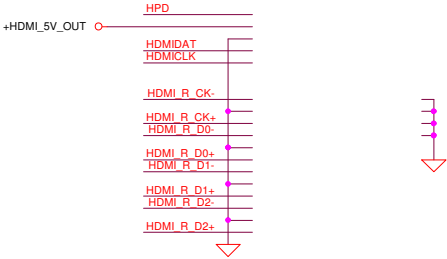
2011.05.10 Co-lay with HDMI port

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Size		Document Number		Rev	
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HDMI CONNECTOR



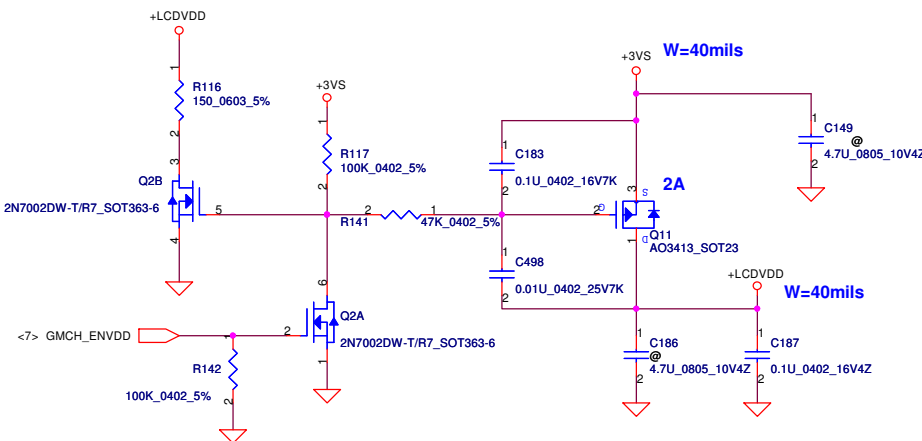
< HDMI Connector >



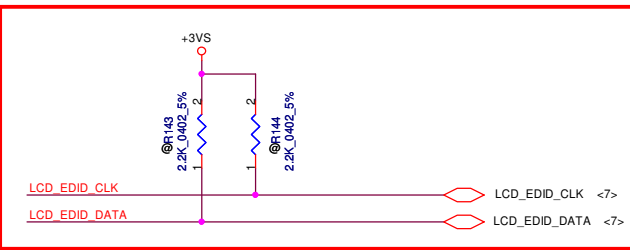
2011.05.04 Change Q42,Q43 to dual package.

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				Size	Document Number
				QBU00	
Date: Wednesday, November 02, 2011				Sheet	16 of 38

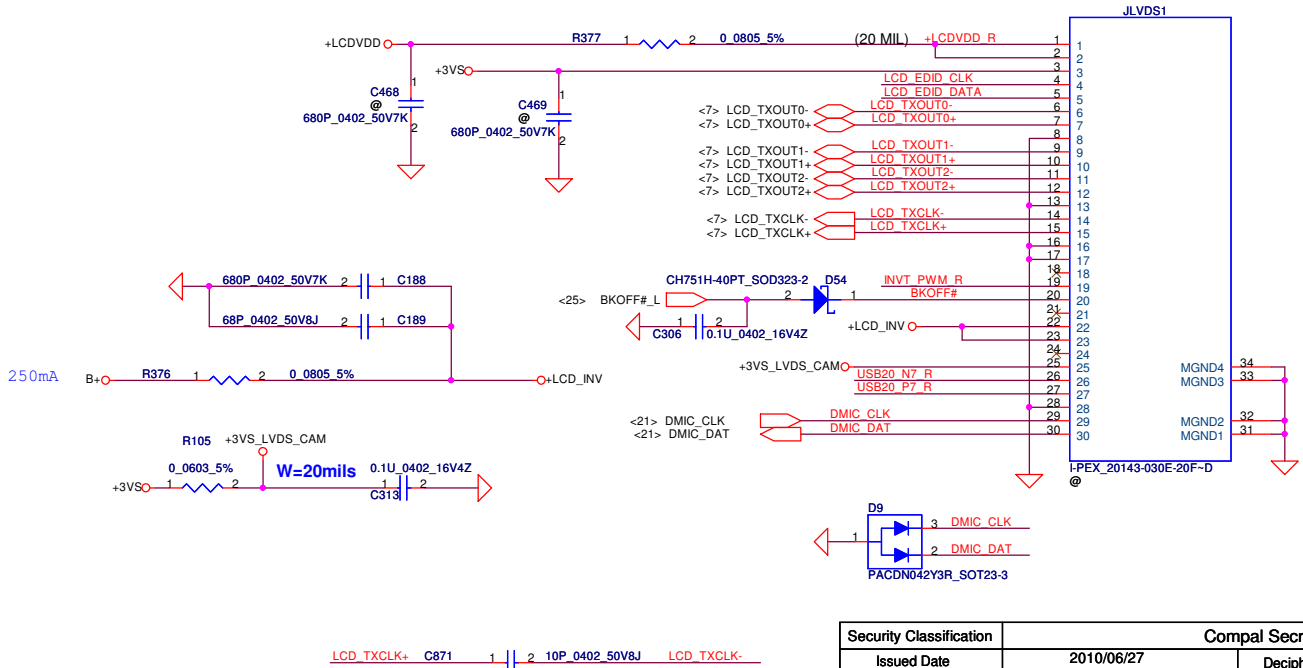
LCD POWER CIRCUIT



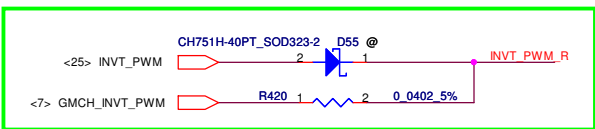
2011.05.22 Remove EDID pull up resistors for Intel issue



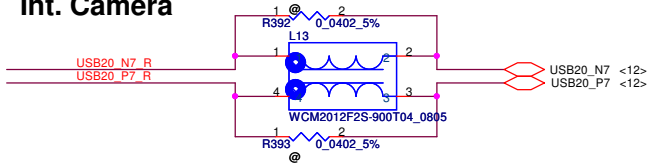
LED/PANEL BD. Conn.



2011.05.20 LCD brightness will controlled by CPU (DPST)

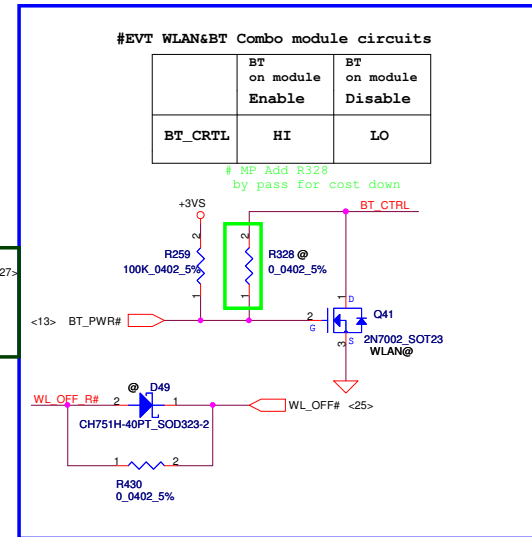


Int. Camera

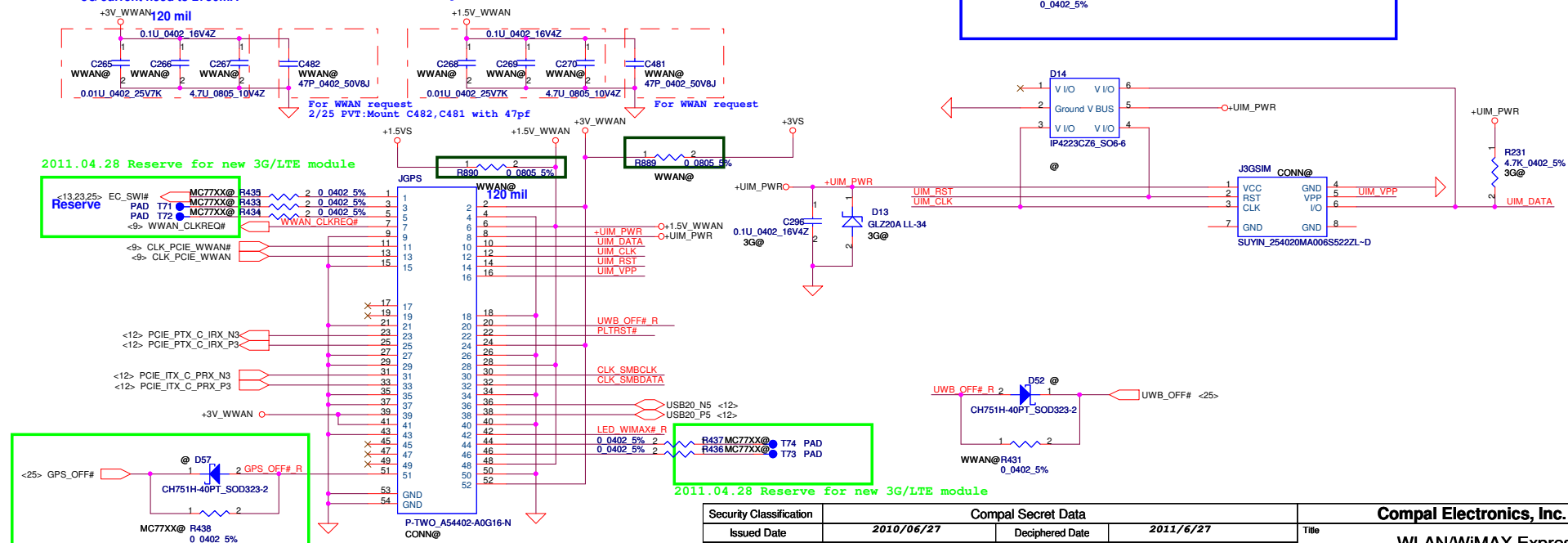


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Size		Document Number		Rev	
Date		Wednesday, November 02, 2011		Sheet 17 of 38	

```
2/25 PVT:Mount C479,C480 with 47pf
3/16 PVT:Add BOM Config of C481,C482 to WLAN@
```



3G current need to 2750mA 3/16 PVT:Add BOM Config of C481,C482 to 3GGPS@

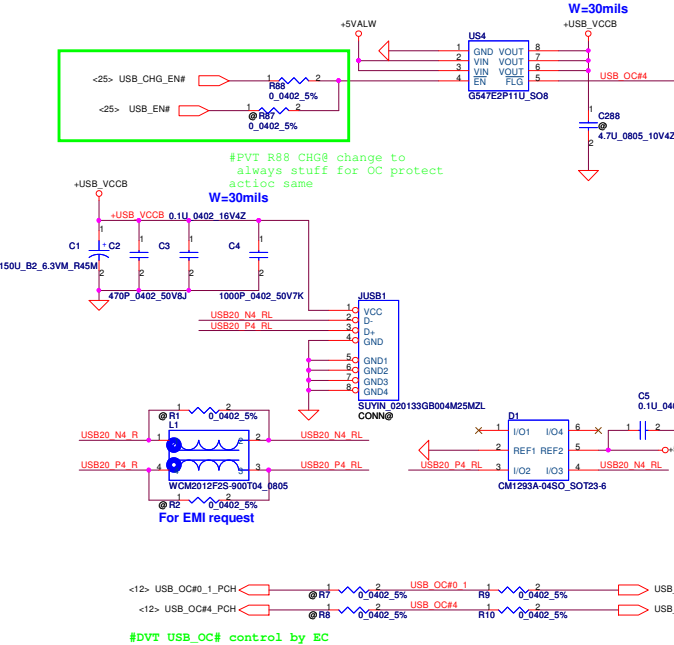
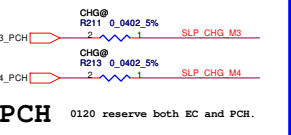
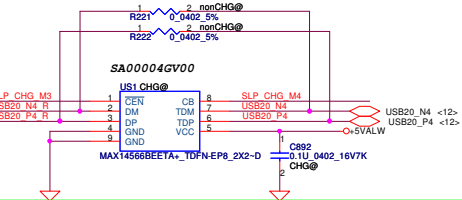


2011.04.28 Reserve for new 3G/LTE module

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				Date:	Monday, November 07, 2011	Sheet 18 of 38

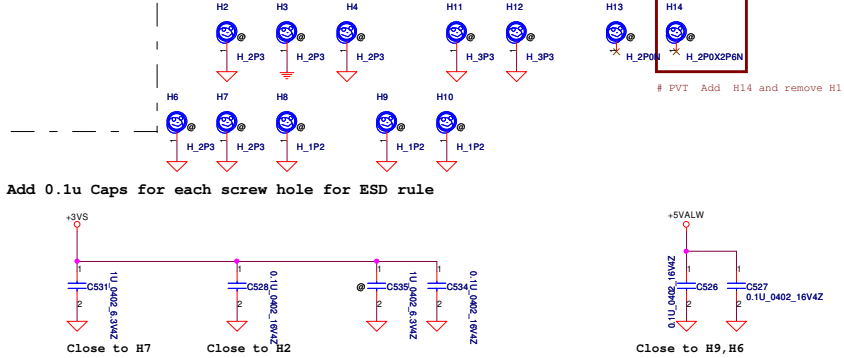
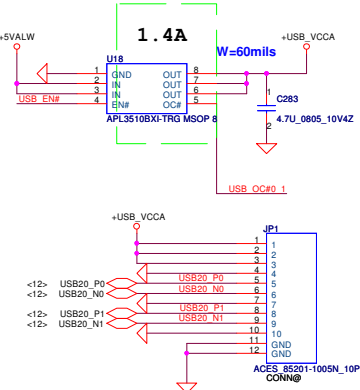
USB Sleep & Charge
Auto-Mode
Mode3

MAX14566B		
CB0 SLP_CHG_M4	CB1 (CEN#) SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

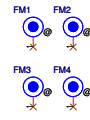


For EMI request
2/3 DVT: Change D38,D37 from PRTR5V002X_SOT143-4 to CM1293A-0480_SOT23-6

USB CONN

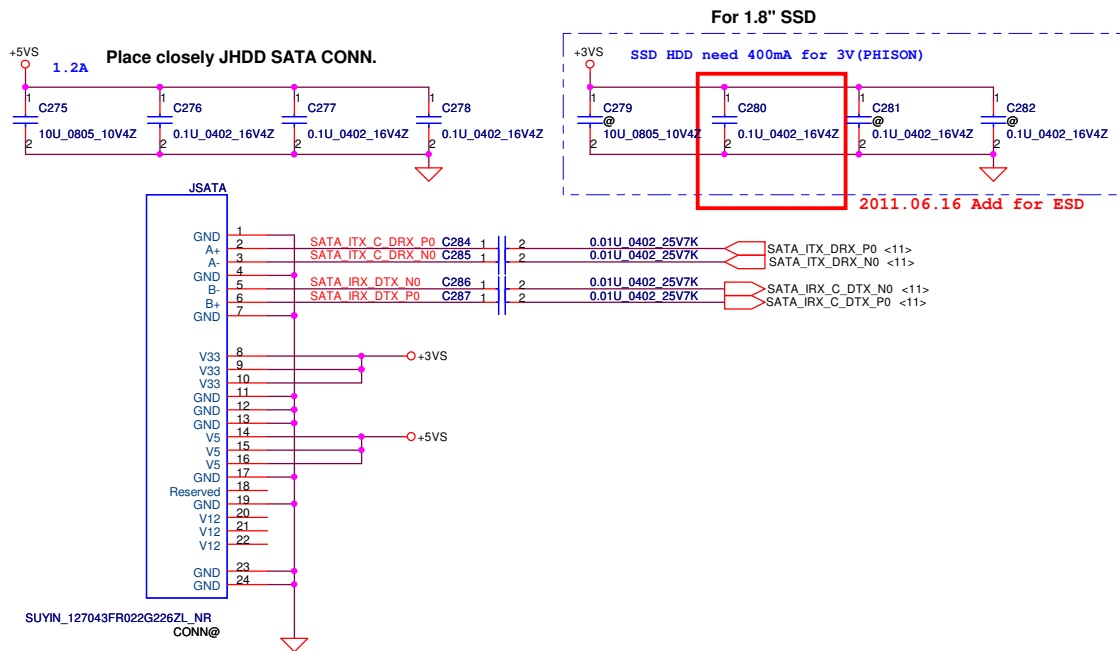


FIDUCIAL_C40M80



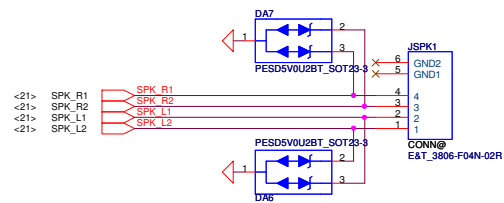
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/06/27	Deciphered Date	2011/6/27	Title	USB Conn
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SATA Conn.

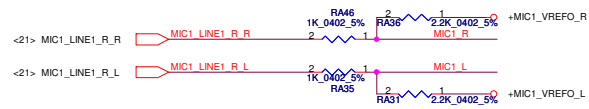


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Size		Document Number			Rev
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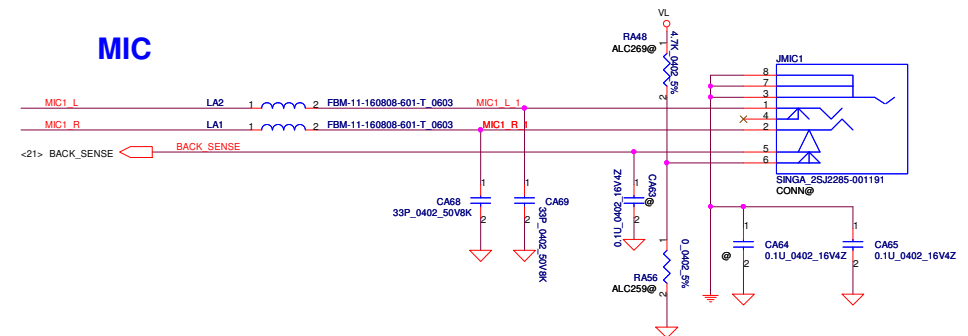
SPEAKER



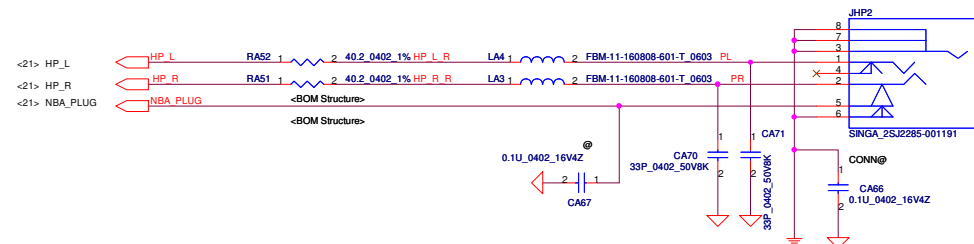
Ext.MIC/LINE IN JACK



MIC

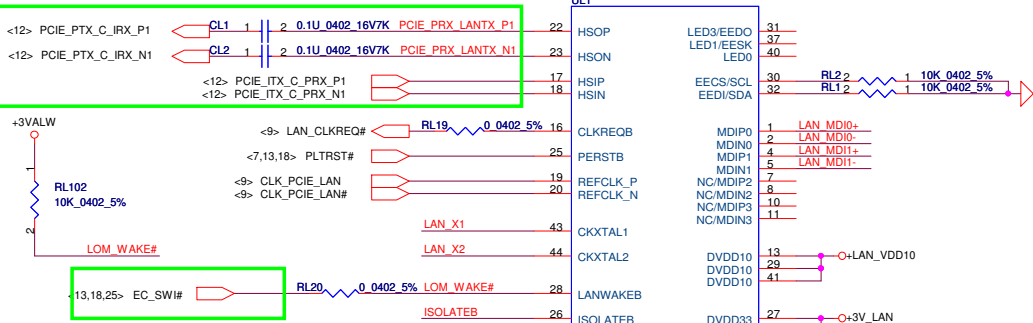


Head phone

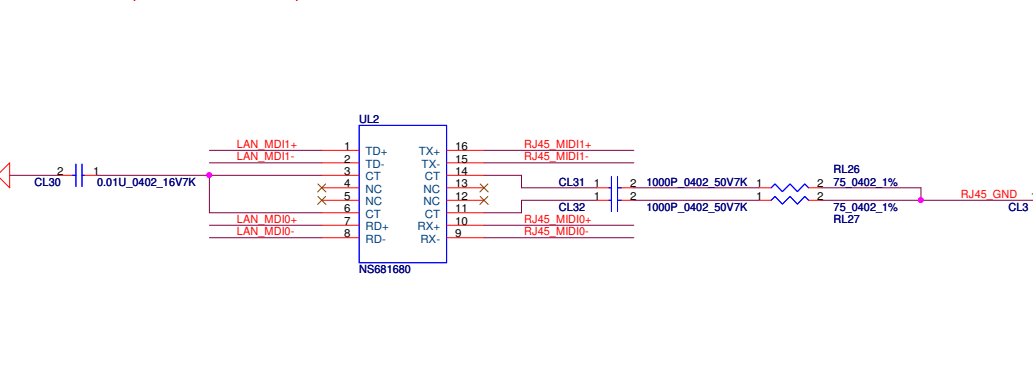
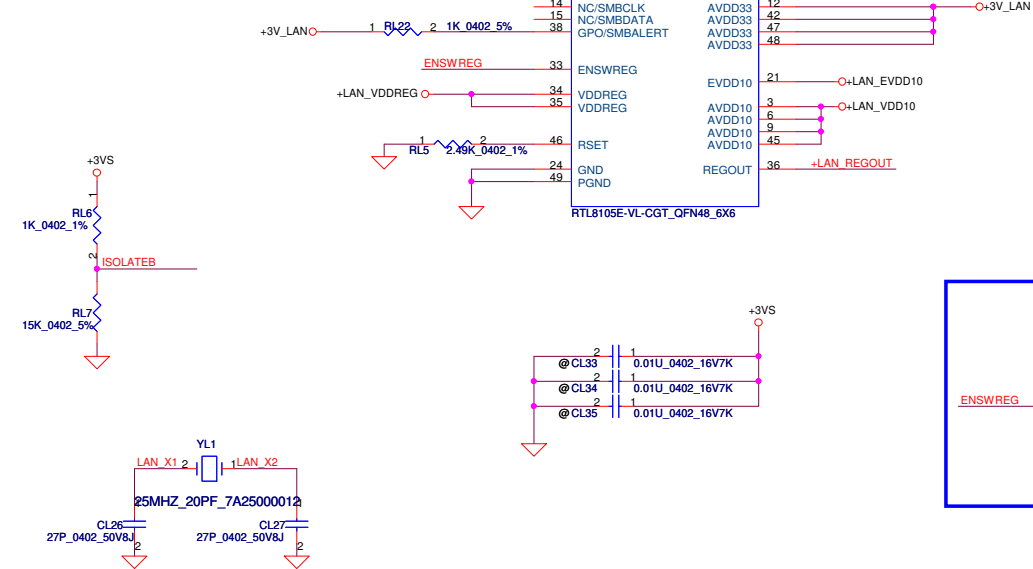


Security Classification		Compal Secret Data		Compal Electronics, Inc. Audio Jack MIC/HP	
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				Size	Document Number
				Custom	QBU00 Date: <u>Wednesday, November 02, 2011</u> Sheet <u>22</u> of <u>38</u>
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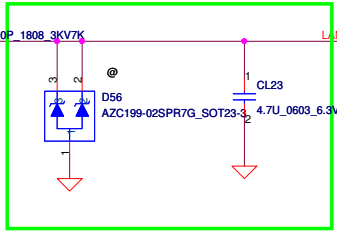
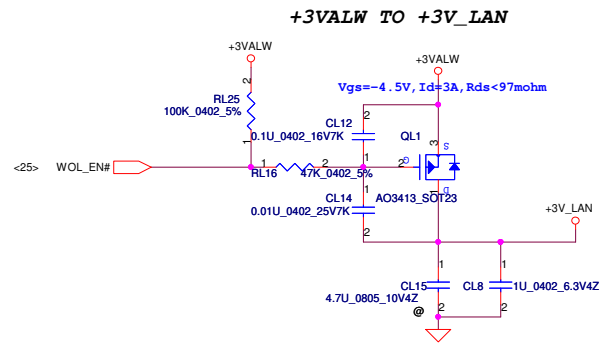
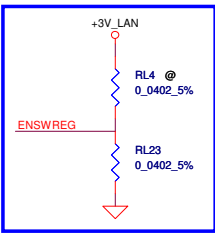
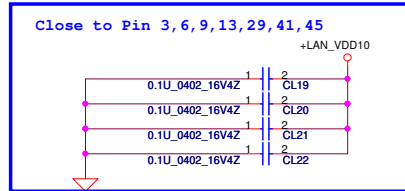
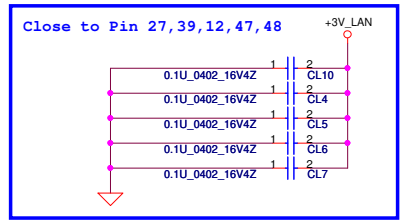
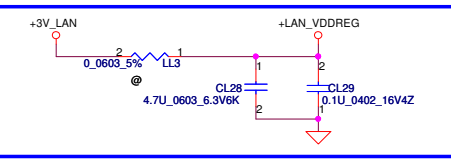
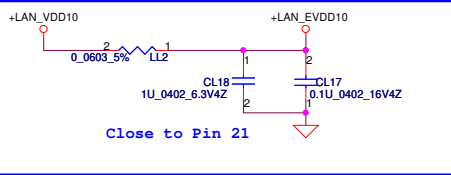
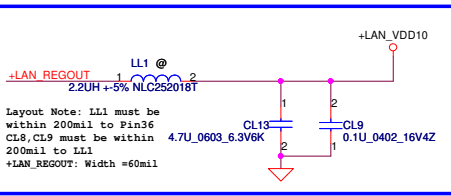
2011.04.20 Change to port 1



2011.04.26 Change control signal to EC_SWI#



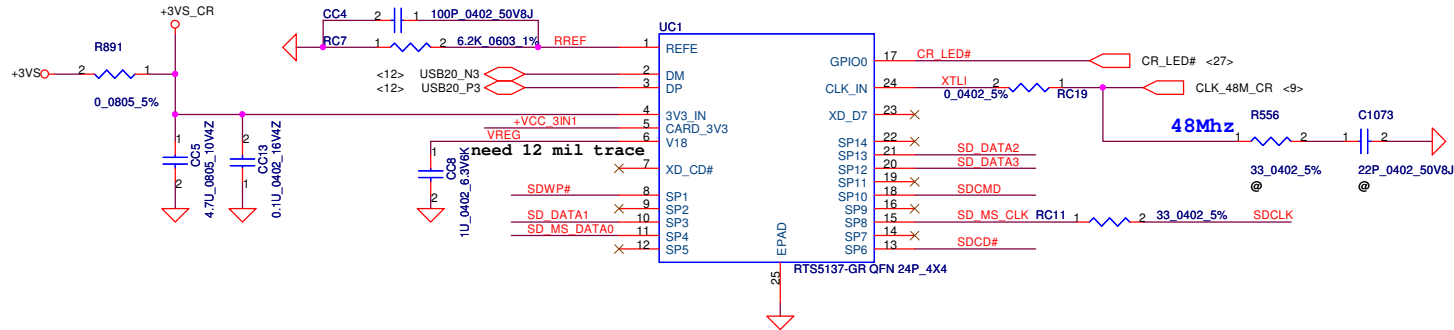
3/10 Change CL13 0805-->0603



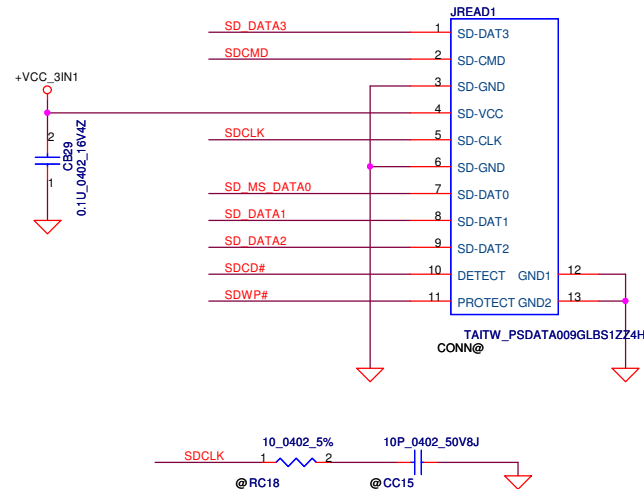
2011/04/18 Add D56 for ESD request

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	XD_CD#		
SP1	XD_RDY#	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS
	XD_D7		

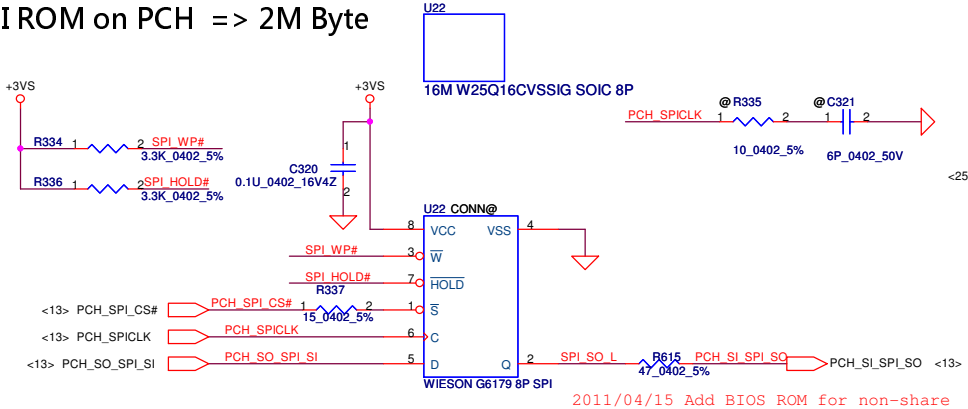


2 in 1 Card Reader

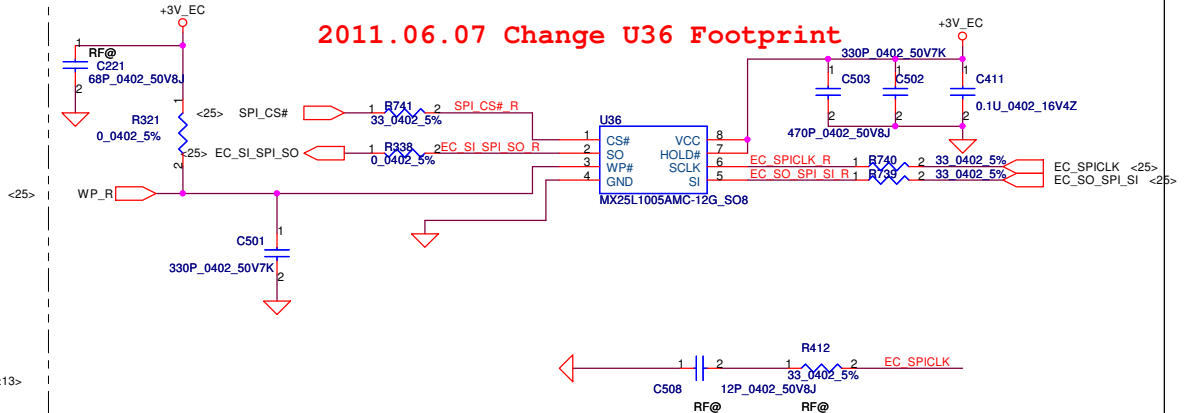


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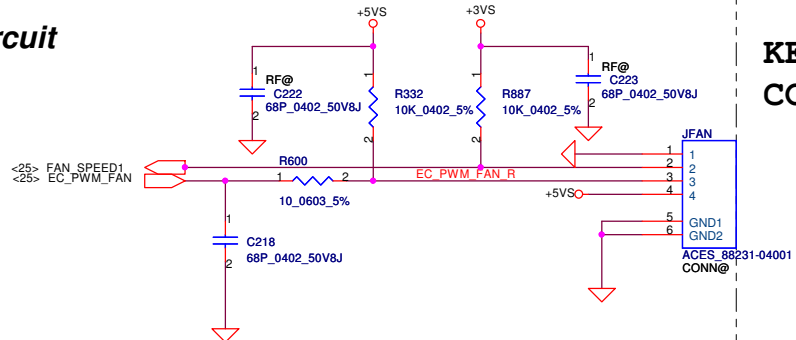
SPI ROM on PCH => 2M Byte

**SPI Flash (1Mb*1)**

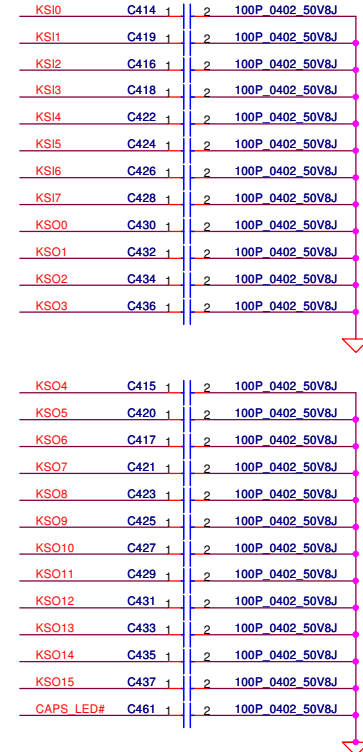
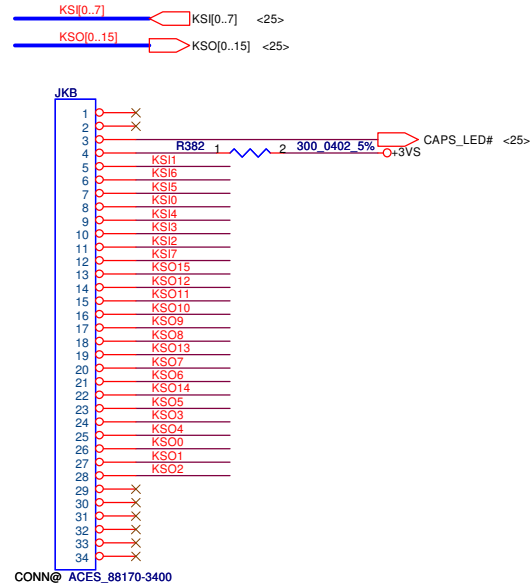
2011.06.07 Change U36 Footprint



FAN Control Circuit

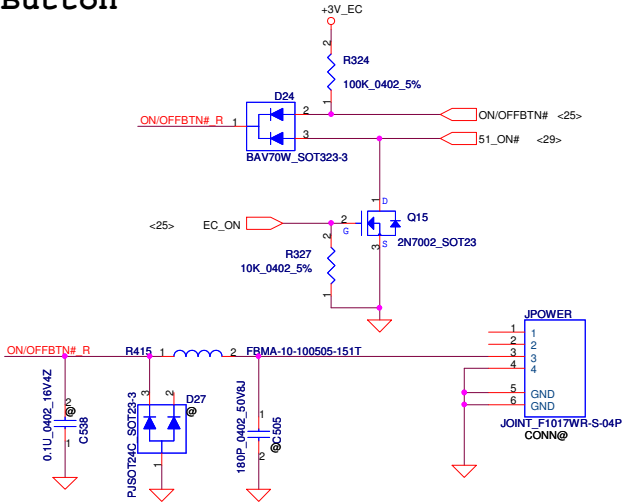


KEYBOARD
CONN.

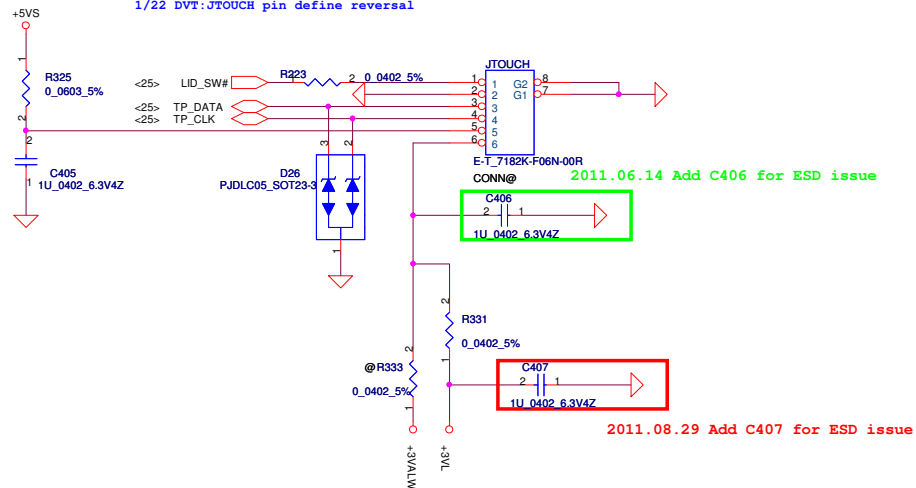


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Issued Date	2010/06/27	Deciphered Date	2011/6/27	SPI ROM//KB//FAN/Debug Poart	
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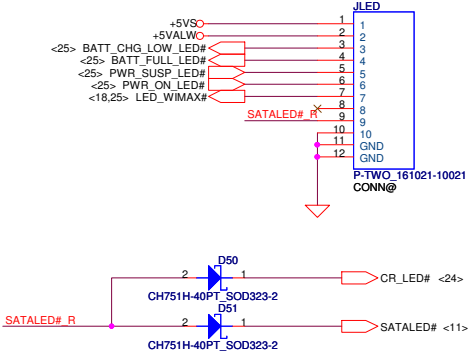
Power Button



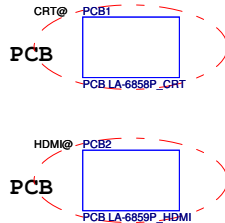
Touch/B Connector



LED Conn

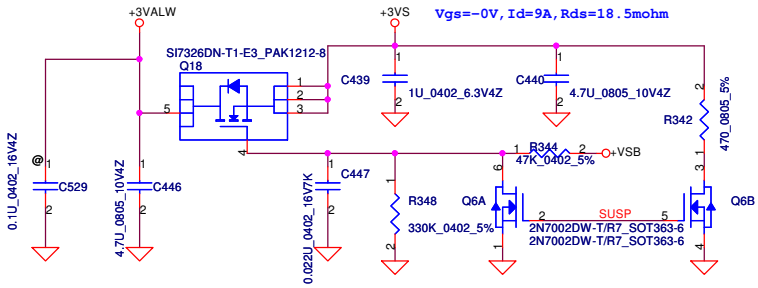


ISPD

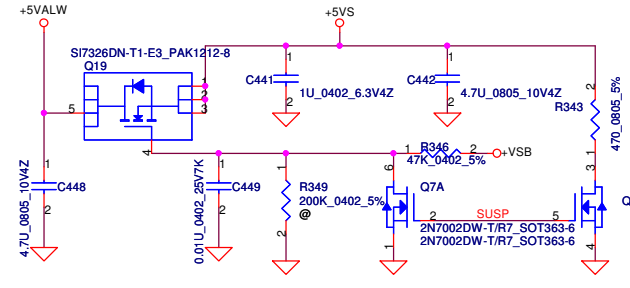


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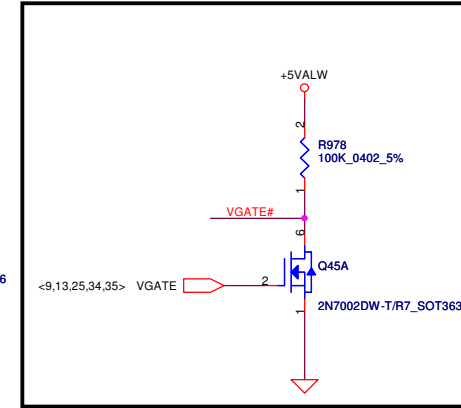
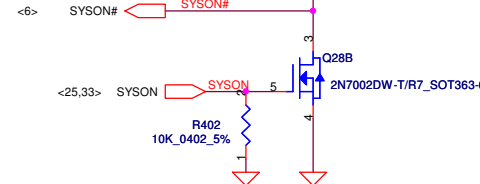
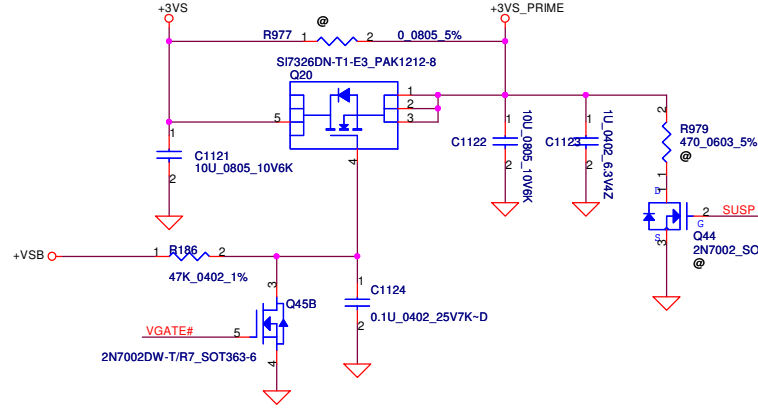
+3VALW TO +3VS



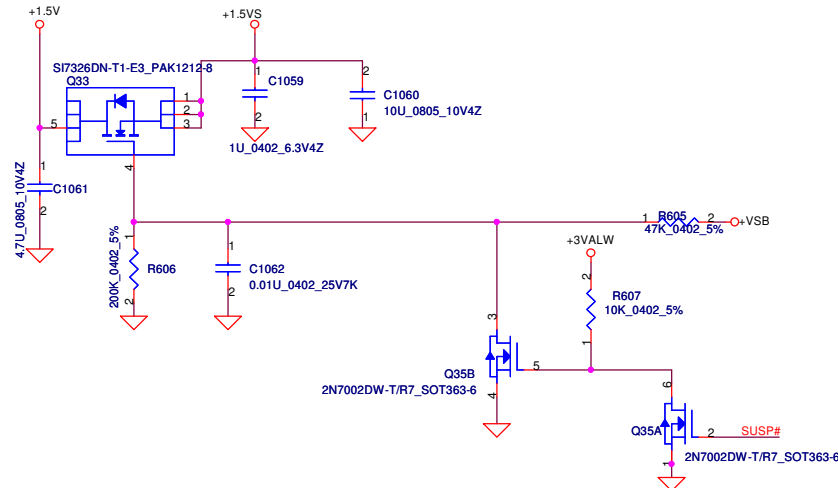
+5VALW TO +5VS



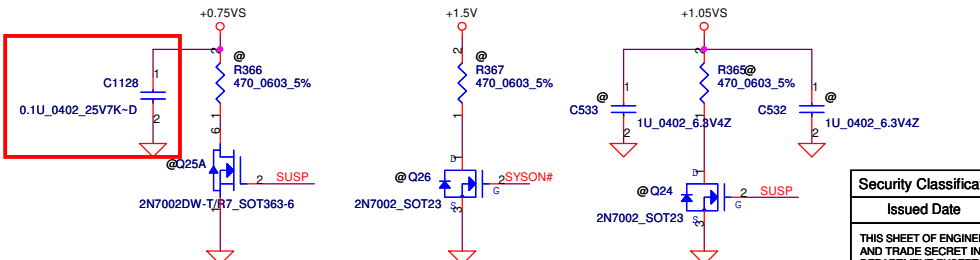
+3VS TO +3VS_PRIME



+1.5V TO +1.5VS

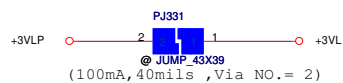
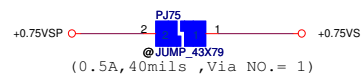
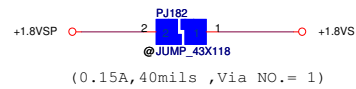
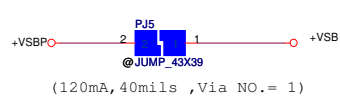
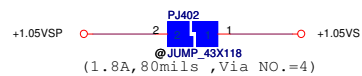
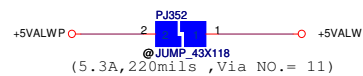
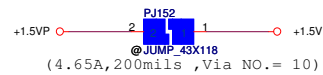
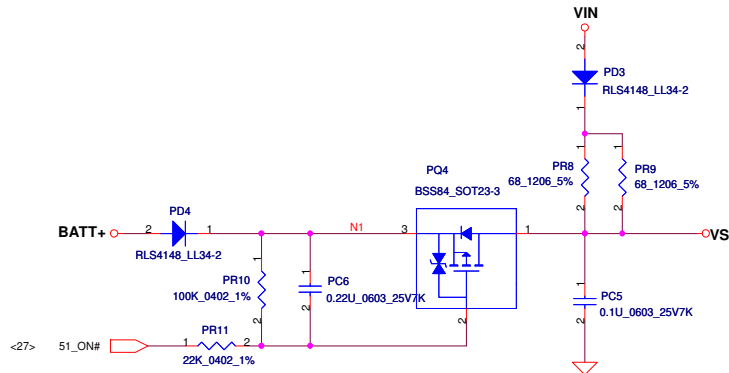
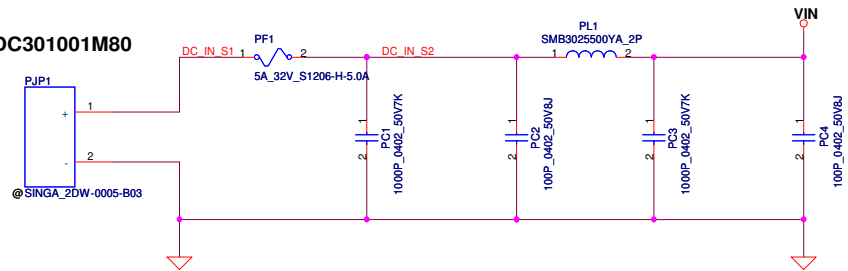


2011.06.14 Add C1128 for ESD issue

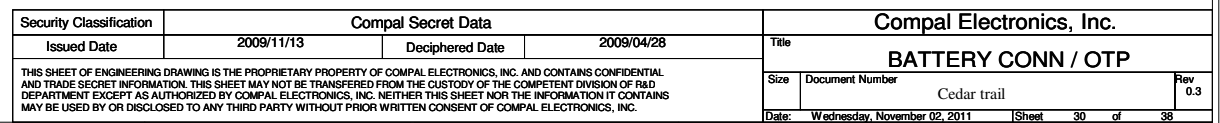
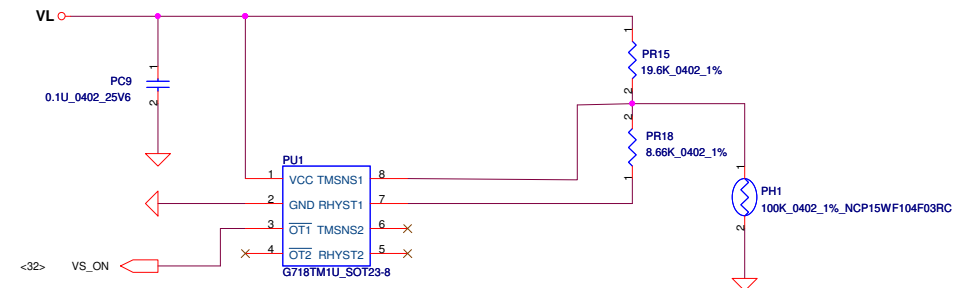
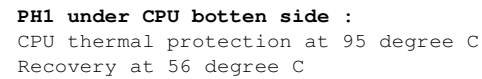


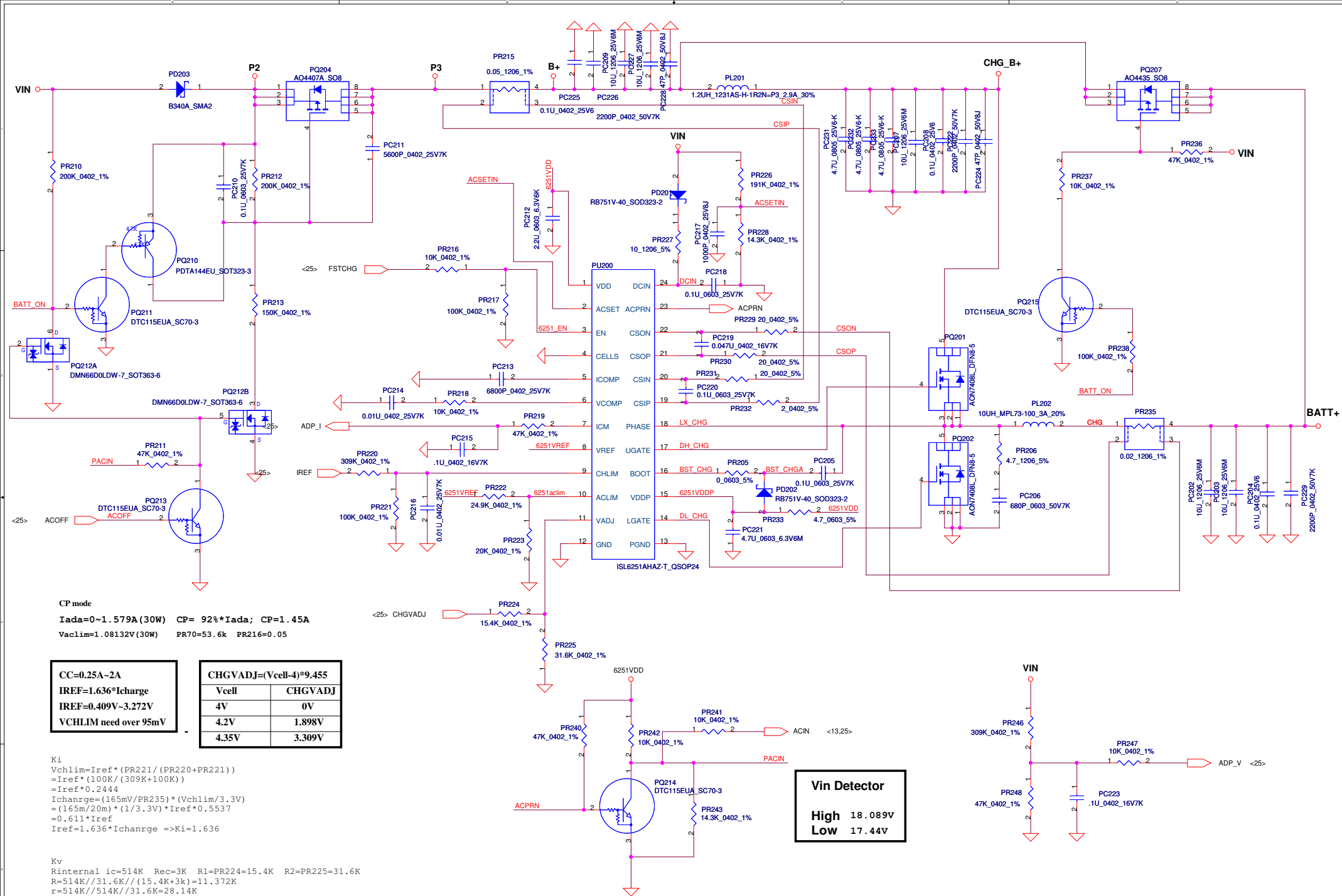
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Issued Date	2009/04/07	Deciphered Date	2012/10/21	Title	
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DC301001M80



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Ki

$V_{chlim}=I_{ref} * (PR221 / (PR220 + PR221))$

$=I_{ref} * (100K / (309K + 100K))$

$=I_{ref} * 0.2444$

$I_{charge} = (165mV / PR235) * (V_{chlim} / 3.3V)$

$= (165m / 20m) * (1 / 3.3V) * I_{ref} * 0.5537$

$= 0.611 * I_{ref}$

$I_{ref} = 1.636 * I_{charge} \Rightarrow Ki = 1.636$

Kv

Internal $i_c=514K$ $Rec=3K$ $R1=PR224=15.4K$ $R2=PR225=31.6K$

$R=514K // 31.6K // (15.4K + 3K) = 11.372K$

$r=514K // 514K // 31.6K = 28.14K$

$V_{cell}=0.175 * V_{adj} + 3.99V$

$4.2V = 0.175 * V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$

$V_{adj} = V_{ref} * (R / (R + 514K)) + CALIBRATE * (r / (r + 514K))$

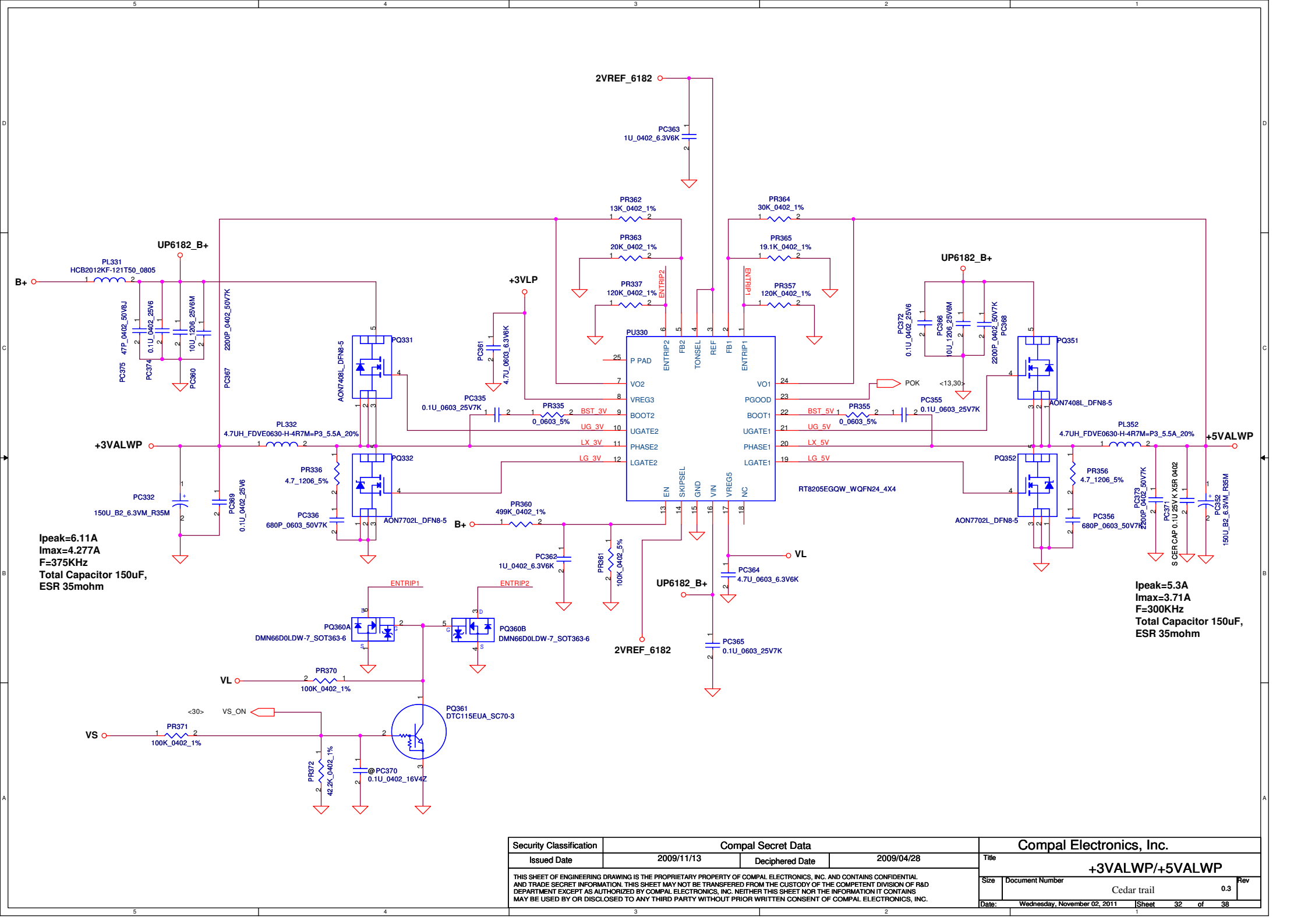
$1.1483 = CALIBRATE * 0.6046 \Rightarrow CALIBRATE = 1.899$

$1.899 = (4.2 - (V_{cell} + A * 0.175)) * Kv = (4.2 - (4.2 + A * 0.175)) * Kv$

$A = V_{ref} * (R / (R + 514K)) = 0.052$

$Kv = 9.455$

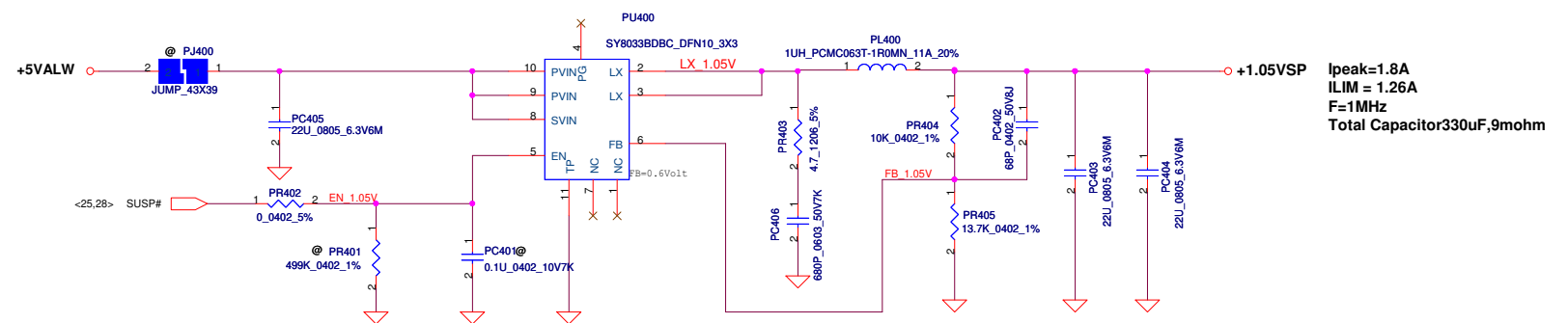
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Ipeak=6.11A
Imax=4.277A
F=375KHz
Total Capacitor 150uF,
ESR 35mohm

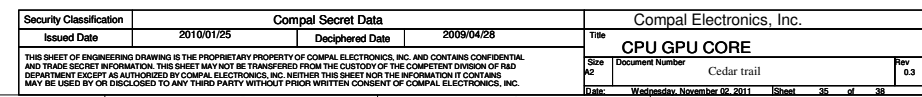
Ipeak=5.3A
Imax=3.71A
F=300KHz
Total Capacitor 150uF,
ESR 35mohm

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Compal Electronics, Inc.			
Title +1.8VSP/+1.05VSP			
Size Custom	Document Number Cedar trail		Rev 0.3



PIR (Product Improve Record)

QBU00 LA-6858P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01.	04/ 26	06	Delete C948,C949,C950,C951	ES2 CPU only support 2 pairs DMI
02.	04/ 26	06	Add DDR_A MA15 signal in CPU side	Cedar Trail platform supports MA0-MA15 total sixteen address signals
03.	04/ 26	07	Reserve 0 ohm for DDC_SCL / SDA , HPD, BREF1P5V, BREFREXT connect to GND.	Follow Intel V1.0 check list to disable HDMI
04.	04/ 26	07	Add CRT DAC,SYNC signals and add RV155,RV156,RV157 150 ohm pull down resistor for CRT DAC signal.	Follow Intel V1.0 check list to enable RGB I/F
05.	04/ 26	08	Reserve 0 ohm for VCCADP / VCCADP_SFR connect to GND	Follow Intel V1.0 check list to disable HDMI
06.	04/ 26	08	Add R1004,C166 for +VCCDIO / R535,C1125 for +VCC_CRT_DAC	Follow Intel V1.0 check list to enable RGB I/F
07.	04/ 26	10	Add MA15 signal for SODIMM connector	Cedar Trail platform supports MA0-MA15 total sixteen address signals
08.	04/ 26	11	Stuff R544	System will change to non-share ROM design, PCH STRAP2/1 will be 01
09.	04/ 26	12	Change PCIe port arrangement	Follow BIOS team's request to re-arrang PCIe port for power saving.
10.	04/ 26	13	Use BOM option for R931,R932,R933,R934	Follow Intel V1.0 check list to disable HDMI
11.	04/ 26	13	Add J2 and C1087 for PCH GPIO12	BIOS will use GPIO12 for clean password function.
12.	04/ 26	13	Add R566,R567,R618 10K pull high resistors for PCH SPI I/F	System will change to non-share ROM design
13.	04/ 26	15	Add CRT circuit	Follow Intel PDG and V1.0 check list to implement CRT circuit
14.	04/ 26	19	Change USB charger(US1) solution to MAX14566B	Follow A51 common design
15.	04/ 26	19	Reserve US2 bus switch	Support BIOS team's new debug card.
16.	04/ 26	19	Change US4 USB power switch to 2A	Support USB charge V1.1 SPEC--->support 1.8A
17.	04/ 26	23	Change LOM_WAKE# control signal to EC_SWI#	LOM WAKE# will connect to PCH directly and change net name to "EC_SWI#"
18.	04/ 26	25	Change KBC to KB930/KB9012	Follow EC team KB930/KB9012 common design
19.	04/ 26	26	Add U22 -->2MB SPI ROM	System will change to non-share ROM design
20.	04/ 28	18	Reserve 0 ohm and test points in JGPS pin1/3/5/44/46/51	Cougar 2.0 will support new 3G/LTE module
21.	04/ 29	25	Delete C211,C212,C216,C217	RF team has no necessity
22.	04/ 29	07	Delete 220p caps for sideband signals.	EMC team has no necessity
23.	04/ 29	09	Delete C940,C941	RF team has no necessity
24.	04/ 29	09	Delete C1067,C1066	RF team has no necessity
25.	04/ 29	09	Reserve R305,C392 for SMBus_CLK	Reserve R-C for RF team's requirement
26.	04/ 29	17	Delete C227,C228,C290,C230,C231,C232,C1074,C1075	RF team has no necessity
27.	04/ 29	18	Delete C307,C298,C297	RF team has no necessity
28.	05/ 03	07	Add R984 0 ohm resistor for XDP pin17	Reserve 0 ohm for XDP when XDP connector no use.
29.	05/ 04	16	Change Q42,Q43 to dual package	Save layout space and cost
30.	05/ 06	07	Add R989 (0 ohm) for XDP signal	Reserve 0 ohm for XDP when XDP connector no use.
31.	05/ 10	15	Delete D53,F1,C1110	Share 5V with CRT circuit.
32.	05/ 10	07	Change XDP un-define net name	Follow naming rule

QBU00 LA-6858P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01.	06/ 07	07	Remove XDP connector	XDP debug port is no necessary in PVT
02.	06/ 07	08	Keep +VCCADP_1.05, +VCCADP_SFR power rail even disable DDI interface	Intel correct their DDI disable guideline
03.	06/ 07	26	Change U36 Symbol and footprint	Fix DFB issue
04.	06/ 10	13	Change J1 to JCMOS, J2 to JPW	Follow A51 jumper naming rule
05.	06/ 10	19	Remove US2 USB bus switch	PVT won't reserve USB debug port
06.	06/ 14	08	Stuff 1u (C1007,C1008,C1009) on GFX_CORE	To solve ESD issue
07.	06/ 14	28	Add 0.1u (C1128) on +0.75VS power rail	To solve ESD issue
08.	06/ 14	10	Add 0.1u (C116) on +0.75VS power rail	To solve ESD issue
09.	06/ 14	10	Add 0.1u (C119) on +1.5V power rail	To solve ESD issue
10.	06/ 14	10	Add 0.1u (C406) on +1.5V power rail	To solve ESD issue
11.	06/ 14	27	Add 1u (C406) on touch pad power rail	To solve ESD issue
12.	06/ 15	13	Change PCH SPI I/F pull high to +3VS	To solve S3/S5 +3VS power plan leakage issue
13.	06/ 16	20	Stuff 0.1u (C280) on +3VS power rail	To solve ESD issue
14.	06/ 18	07	Add R1009, R1010 for DDI1_DDC_SCL/SDA	Follow Intel DDI disable guideline

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PIR (Product Improve Record)

QBU00 LA-6858P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01.	06/ 29	09	Swap CLK Gen output for CPU_SCDREFFCLK and CPU_DREFCLK	Intel recommend CPU_SSCDREFFCLK use SSC CLK

QBU00 LA-6858P SCHEMATIC CHANGE LIST
REVISION CHANGE: 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01.	08/ 29	07	Change R975 from 10ohm to 0 ohm	Follow Intel CRB design.
02.	08/ 29	25	Un-stuff R312,R313	KS01,KS02 of KB930 don't need to pull high.
03.	08/ 29	27	Add 1u(C406) on touch pad power rail.	To solve ESD issue

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			QBU00		0.3
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
2011/06/14		32	PR336, PR356 to 1206 4.7ohm; PC336, PC356 to 0603 680pF	For EMI Solution
2011/06/14		35	PR526, PR528, PR569, PR571 to @ PR506, PR516 to 1206 4.7ohm; PC506, PC516 to 0603 680pF	For EMI Solution
2011/06/14		33	PU150 change to RT8209MGQW	
2011/06/14		33	PR157 change to S RES 1/16W 7.87K +-1% 0402	For OCP Solution
2011/06/14		35	PC550 to @	Reserve PC550 location and change it to 5.3mm cap (SF000003Z00) for ME solution
2011/06/21		35	PC536 to 42.2K	Change PR536 to 42.2Kohm to meet Cedar Trail loadline spec
2011/06/27		35	PH505, PR542, PR543, PH504, PR559, PR560 to @ PR545, PR558, PR530, PR567 to 0ohm PR541 to 3.62K, PR544 to 1.69K, PR556 to 10K PR557 to 2K, PR536 to 39K	For Cedar Trail loadline spec
2011/06/27		35	PR582, PR583 to 35.7K	For CPU & GFX OCP Solution
2011/06/27		35	PL503 to 2.2uH	Base on GFX_Core ripple & dynamic test result
2011/06/27		35	PR584 to 0_0402_5%	For AP Code material
2011/11/1		29	PF1 change to SART 5A_32V_S1206-H-5.0A	For burn out issue
2011/11/1		30	PF2 change to Cooper 7A_32V_TR/3216FF-R	For burn out issue
2011/11/1		32	PU330 change to RT8205EGQW	For burn out issue
2011/11/1		35	PC550 change to Lelon 68uF 5.3H	For acoustic issue

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				Custom	PEQAE LA-7291P M/B	0.3
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