

	1	2	3	4	5	6	7	8		
A	TABLE OF CONTENTS			Revisions			Approvals			
				REV	ECN NO.	Description Of Change	DATE	DFTG.	ENGR.	REL.
B	PAGE 4 - CLOCK GENERATOR 5-7 - BANIAS PROCESSOR 8-12 - MONTARA-GM 13-16 - DDR 17 - TV ENCODER 18 - CRT 19 - LVDS 21-23- ICH4-M 24 - HDD CONNECTOR 25 - CD-ROM CONNECTOR 26 - USB PORT 27 - LAN CONTROLLER 28 - LAN POWER 29- RJ45 CONN 30- CHIVAS II 31 - FLASH ROM & IR 32- 1394 CONTROLLER			PAGE 33- KEYBOARD CONNECTOR & TOUCH PAD 34 - LID SWITCH/LEDS 35 - CARDBUS CONTROLLER 36 - PCMCIA CARD 37- PC CARD CONNECTOR 38 - MINI PCI 39 - AC97 CODEC 40 - VR & MIC JACK 41 - AMP 42- MDC I/F 43 - THERMAL SENSOR & FAN CONTROLLER 44 - DECOUPLING CAPS 45 - DRILL HOLE 46 - HIGH SPEED 47 - PULL UPS 48-56 - POWER						
D										
F							Engineer Engr. Name Drawn by Drawer Name R&D CHK DOC CTRL CHK MFG ENGR CHK TITLE Cricket 2.0 (UMA) Size A3			

Engineer <i>Engr. Name</i>	INVENTEC Cricket 2.0 (UMA)	Size A3
Drawn by <i>Drawn Name</i>		
R&D CHK <i>DOC CTRL CHK</i>		
MFG ENGR CHK		

The following signals should have 10 mil spacing and must be routed 20 mil from any other trace.

MCH_HXRCOMP 10- 1 R725 27.4 1% 2

MCH_HYRCOMP 10- 1 R724 27.4 1% 2

Layout Note: MCH_HXSWING, MCH_HYSWING
10 mil trace, 20 mil space

H_A#(31:3)	46-5		
H_A#(3)	P23		HA#3
H_A#(4)	T25		HA#4
H_A#(5)	T28		HA#5
H_A#(6)	R27		HA#6
H_A#(7)	U23		HA#7
H_A#(8)	U2		HA#8
H_A#(9)	R24		HA#9
H_A#(10)	U28		HA#10
H_A#(11)	V28		HA#11
H_A#(12)	U27		HA#12
H_A#(13)	T27		HA#13
H_A#(14)	V27		HA#14
H_A#(15)	U2		HA#15
H_A#(16)	V26		HA#16
H_A#(17)	V24		HA#17
H_A#(18)	V23		HA#18
H_A#(19)	W23		HA#19
H_A#(20)	W25		HA#20
H_A#(21)	Y29		HA#21
H_A#(22)	AA2		HA#22
H_A#(23)	W24		HA#23
H_A#(24)	W23		HA#24
H_A#(25)	W2		HA#25
H_A#(26)	Y27		HA#26
H_A#(27)	AA28		HA#27
H_A#(28)	W28		HA#28
H_A#(29)	AB27		HA#29
H_A#(30)	Y26		HA#30
H_A#(31)	AB28		HA#31

Figure 1: Block diagram of the HREQ and HADSTB signals. The diagram shows a 4-bit bus H_REQ[4:0] connected to five multiplexers. The first multiplexer selects between H_REQ[0] (R28) and H_REQ[1] (P25) to produce HREQ0#. The second multiplexer selects between H_REQ[2] (R23) and H_REQ[3] (R25) to produce HREQ1#. The third multiplexer selects between H_REQ[4] (T23) and H_REQ[0] (R28) to produce HREQ2#. The fourth multiplexer selects between H_REQ[1] (P25) and H_REQ[2] (R23) to produce HREQ3#. The fifth multiplexer selects between H_REQ[3] (R25) and H_REQ[4] (T23) to produce HREQ4#. The H_REQ[0] (R28) signal is also connected to HADSTB0# and HADSTB1#. The H_REQ[1] (P25) signal is connected to HADSTB0#. The H_REQ[2] (R23) signal is connected to HADSTB1#. The H_REQ[3] (R25) signal is connected to HADSTB1#. The H_REQ[4] (T23) signal is connected to HADSTB1#.

CLK_MCH_BCLK#	46-A-	AD29	HCLKN
CLK_MCH_BCLK#	46-A-	AE29	HCLKP
MCH_HYRCOMP	10-	H28	HYRCOMP
		K28	HYSWING
MCH_HXRCOMP	10-	B20	HXRCOMP
		B18	HXSWING

H_DSTBN#0	66-5	J28	H0DSTBN#0
H_DSTBN#1	66-5	C27	H0DSTBN#1
H_DSTBN#2	66-5	E22	H0DSTBN#2
H_DSTBN#3	66-5	D18	H0DSTBN#3
H_DSTBP#0	66-5	D26	H0DSTBP#0
H_DSTBP#1	66-5	E21	H0DSTBP#1
H_DSTBP#2	66-5	E18	H0DSTBP#2
H_DSTBP#3	66-5	J25	H0DSTBP#3
H_DINV#0	66-5	B25	DINV#0
H_DINV#1	66-5	G29	DINV#1
H_DINV#2	66-5	G19	DINV#2
H_DINV#3	66-5		DINV#3
H_CPURST#	66-6-5	F15	CPURST#

K21	H0VREF0
J21	H0VREF1
J17	H0VREF2
Y28	H0CCVREF
Y22	

Timing diagram showing HUB_PD(10:0) and HAVREF signals. The HUB_PD(10:0) signal is a 16V signal with a 46-21 ns delay. The HAVREF signal is a high-frequency signal. The diagram shows HUB_PD(0) to HUB_PD(10) and their corresponding HAVREF signals.

HUB_PD	Signal	Value
HUB_PD(0)	U7	H1 0
HUB_PD(1)	U4	H1 1
HUB_PD(2)	U3	H1 2
HUB_PD(3)	V3	H1 3
HUB_PD(4)	W2	H1 4
HUB_PD(5)	W6	H1 5
HUB_PD(6)	V6	H1 6
HUB_PD(7)	W7	H1 7
HUB_PD(8)	T3	H1 8
HUB_PD(9)	V5	H1 9
HUB_PD(10)	V4	H1 10

HUB_PSTRB	46-21-	W3	PSTRBS
HUB_PSTRB#	46-21-	V2	PSTRBF
HUB_HLZCOMP	10-	T2	HLZCOMP
SWING	10-	U2	PSWING
HLVREF	10-	W1	HLVREF

ITL_MONTARA_GM_FCBGA_732P_T

16V2 0.1UF_16V +V1.2S MCH

HUB_HLZCOMP 10- 1 R730 2 27.4 1%

HOST

H00F	K22	H D(0)
H01F	H27	H D(1)
H012F	K25	H D(2)
H013F	L24	H D(3)
H04F	J27	H D(4)
H045F	G28	H D(5)
H05F	L27	H D(6)
H056F	L23	H D(7)
H057F	L25	H D(8)
H058F	J24	H D(9)
H09F	H26	H D(10)
H010F	K26	H D(11)
H011F	K23	H D(12)
H012F	G27	H D(13)
H013F	K49	H D(14)
H014F	J23	H D(15)
H015F	H26	H D(16)
H016F	F25	H D(17)
H017F	F26	H D(18)
H018F	B27	H D(19)
H019F	H23	H D(20)
H020F	E27	H D(21)
H021F	G25	H D(22)
H022F	F28	H D(23)
H023F	G27	H D(24)
H024F	G24	H D(25)
H025F	C28	H D(26)
H026F	B26	H D(27)
H027F	G22	H D(28)
H028F	F26	H D(29)
H029F	E26	H D(30)
H030F	G23	H D(31)
H031F	B28	H D(32)
H032F	B21	H D(33)
H033F	G21	H D(34)
H034F	C24	H D(35)
H035F	F23	H D(36)
H036F	D22	H D(37)
H037F	C25	H D(38)
H038F	E24	H D(39)
H039F	G20	H D(40)
H040F	H24	H D(41)
H041F	F23	H D(42)
H042F	B22	H D(43)
H043F	B23	H D(44)
H044F	F23	H D(45)
H045F	F21	H D(46)
H046F	C20	H D(47)
H047F	C21	H D(48)
H048F	G18	H D(49)
H049F	E19	H D(50)
H050F	E20	H D(51)
H051F	G17	H D(52)
H052F	D20	H D(53)
H053F	F19	H D(54)
H054F	C19	H D(55)
H055F	F17	H D(56)
H056F	B19	H D(57)
H057F	G16	H D(58)
H058F	E16	H D(59)
H059F	C16	H D(60)
H060F	E17	H D(61)
H061F	D16	H D(62)
H062F	C18	H D(63)

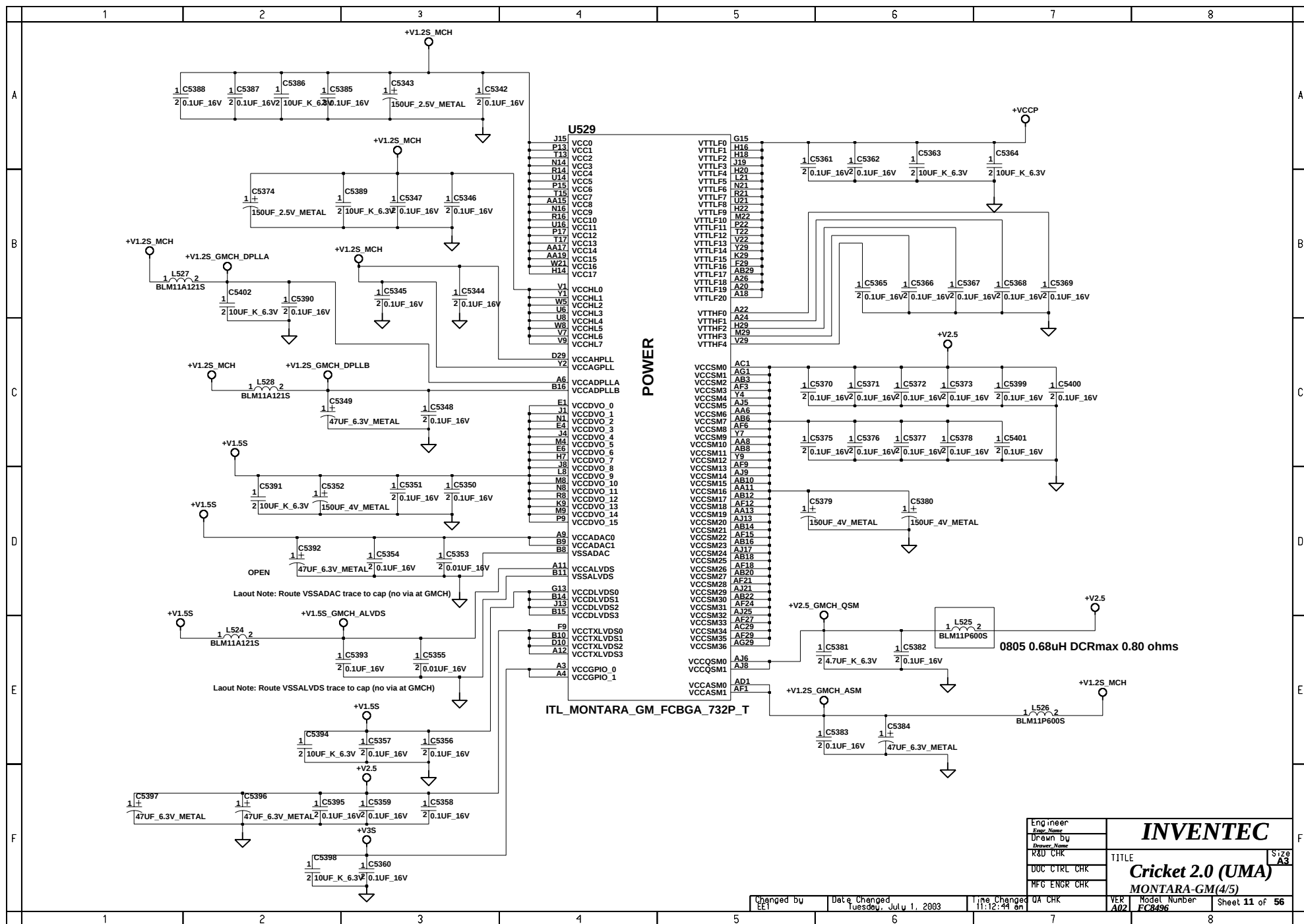
Diagram illustrating the H-RS(0,2) network architecture. The network consists of 12 stages, each represented by a 2x2 switch. The stages are labeled with input and output ports:

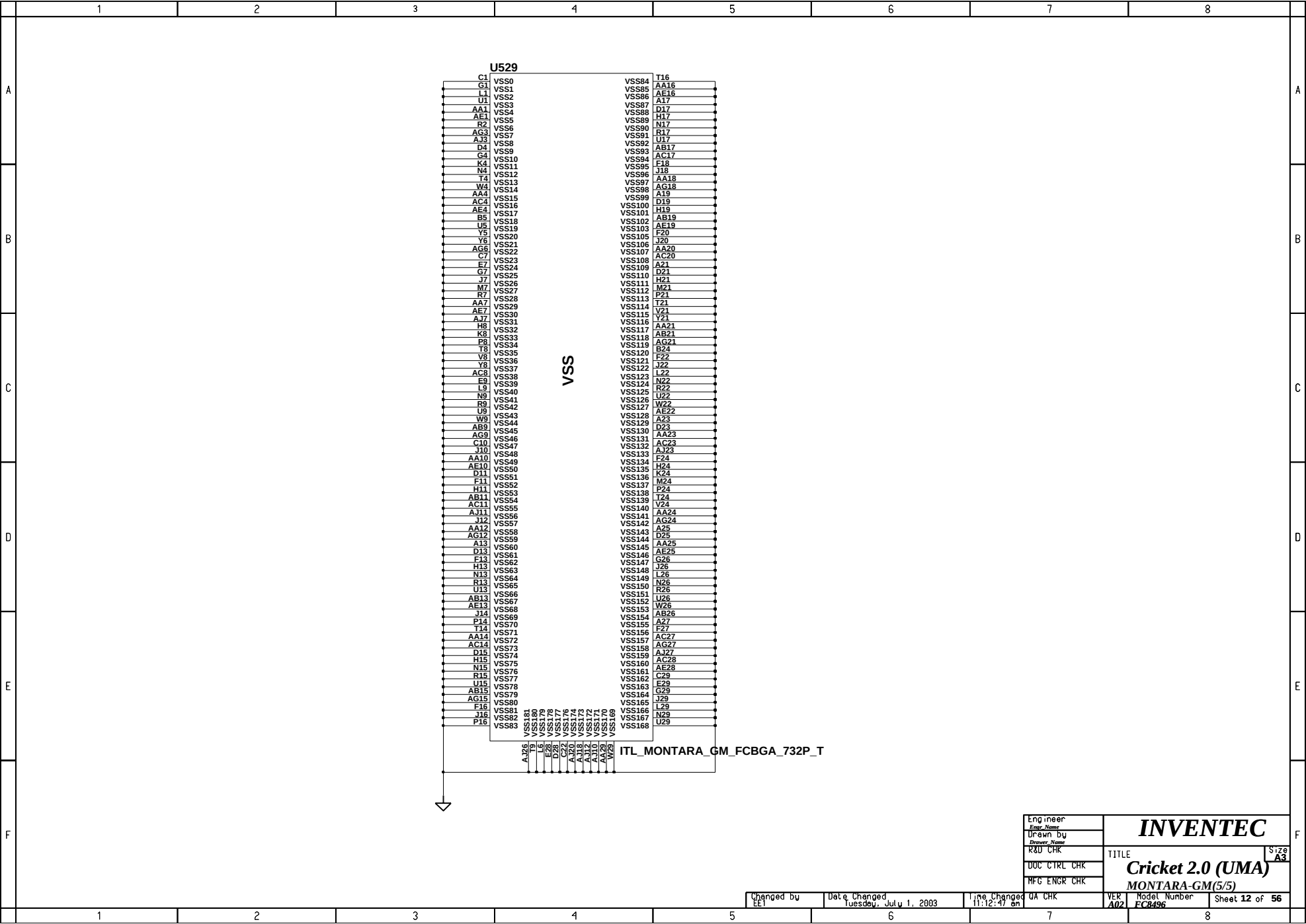
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- H TRDY# (Input 2)
- DRDY# (Input 3)
- DEFER# (Input 4)
- HITM# (Input 5)
- HIT# (Input 6)
- H LOCK# (Input 7)
- BREQ0# (Input 8)
- BNR# (Input 9)
- BPRI# (Input 10)
- H DBSY# (Input 11)
- RS1# (Input 12)
- RS2# (Input 13)
- H RS(0) (Output 1)
- H RS(1) (Output 2)
- H RS(2) (Output 3)

The diagram shows the flow of data through these stages, with a final output labeled H_RS(0,2).

Engineer <i>Your Name</i>			
Drawn by <i>Drawer Name</i>			
K&D CHK	TITLE	Size A3	
UDL CHL CHK	<i>Cricket 2.0 (UMA)</i> <i>MONTARA-GM(3/5)</i>		
MFG ENGR CHK			
QA CHK	VER A02	Model Number FC8496	Sheet 10 of 56

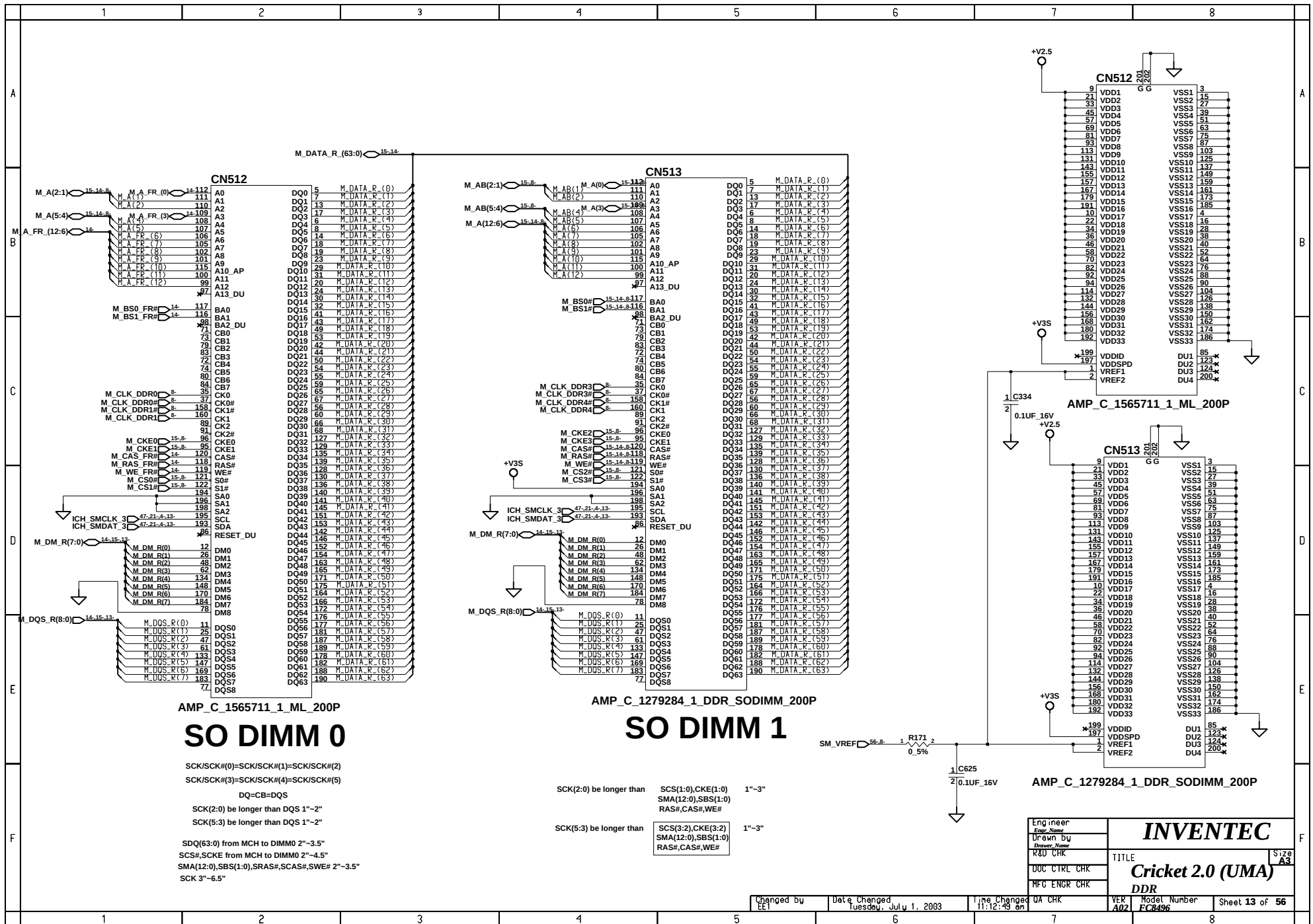
Changed by EE1		Date Changed Tuesday, July 1, 2003	Time Changed 11:12:42 am	QA CHK	VER A02	Model Number EC8496	Sheet 10 of 56
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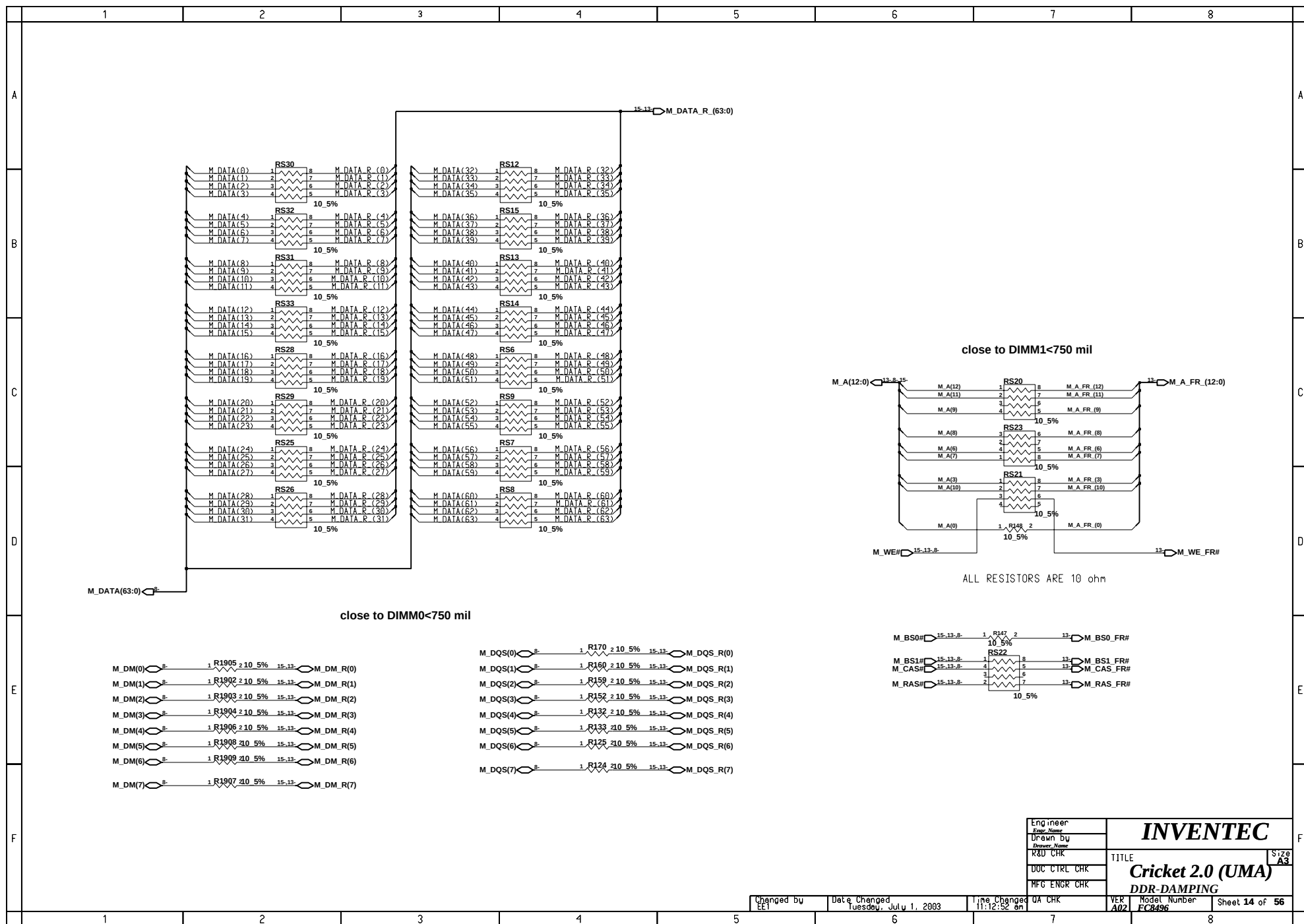


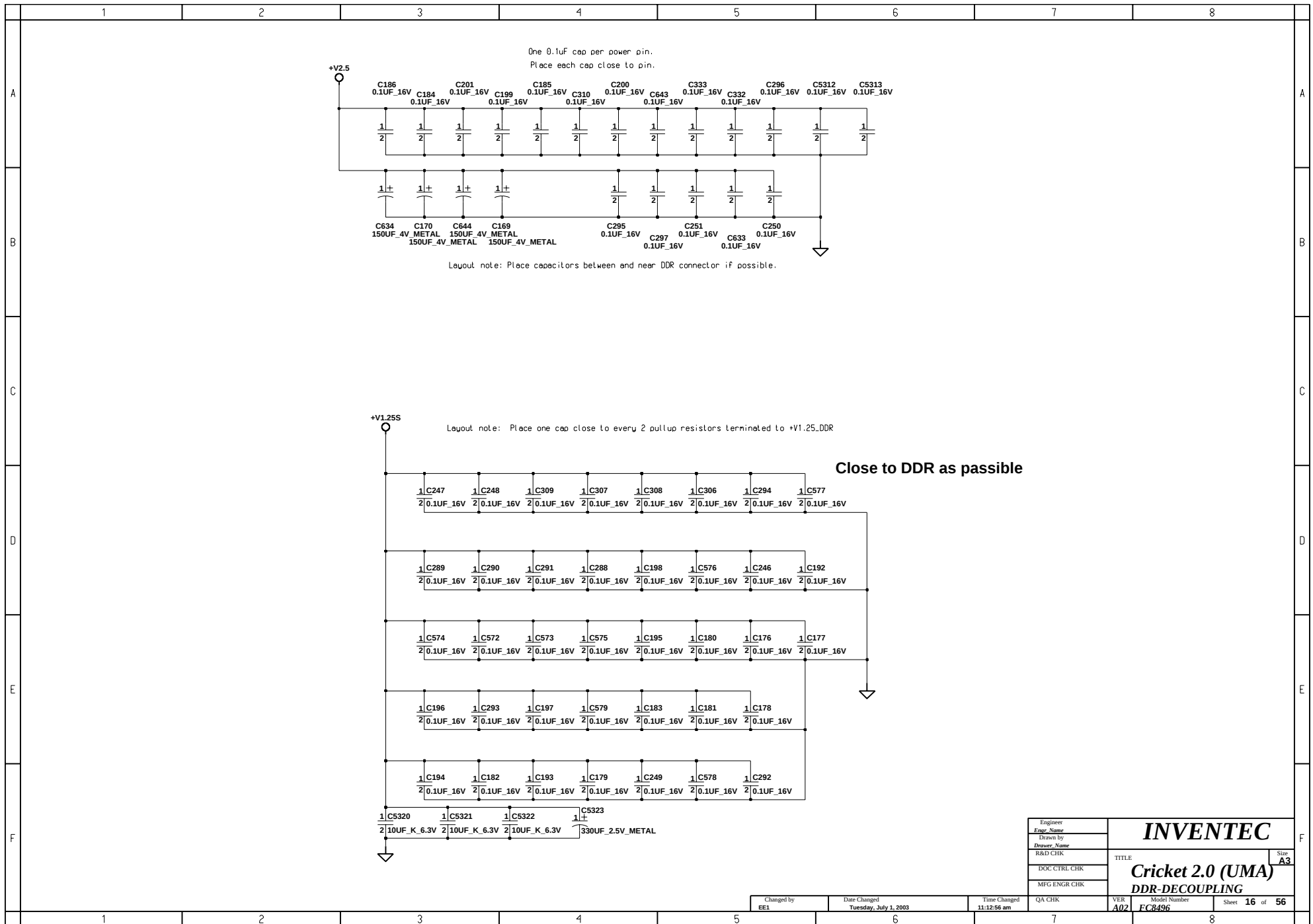


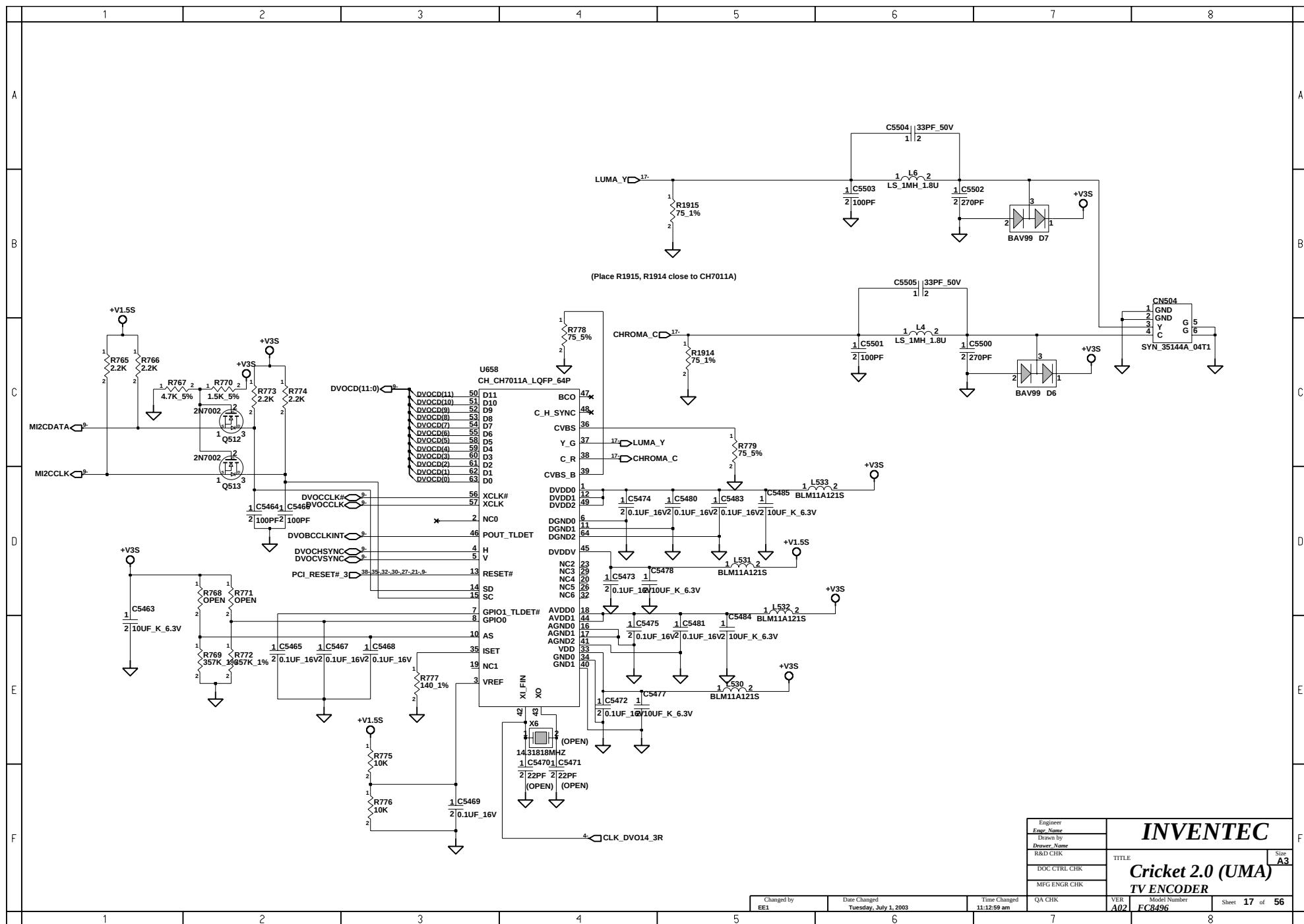
Engineer	INVENTEC		
Drawn by			
Checker			
Rev'd			
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MFG ENGR CHK	Model Number	MONTARA-GM(5/5)	
VER	A02	Sheet 12 of 56	

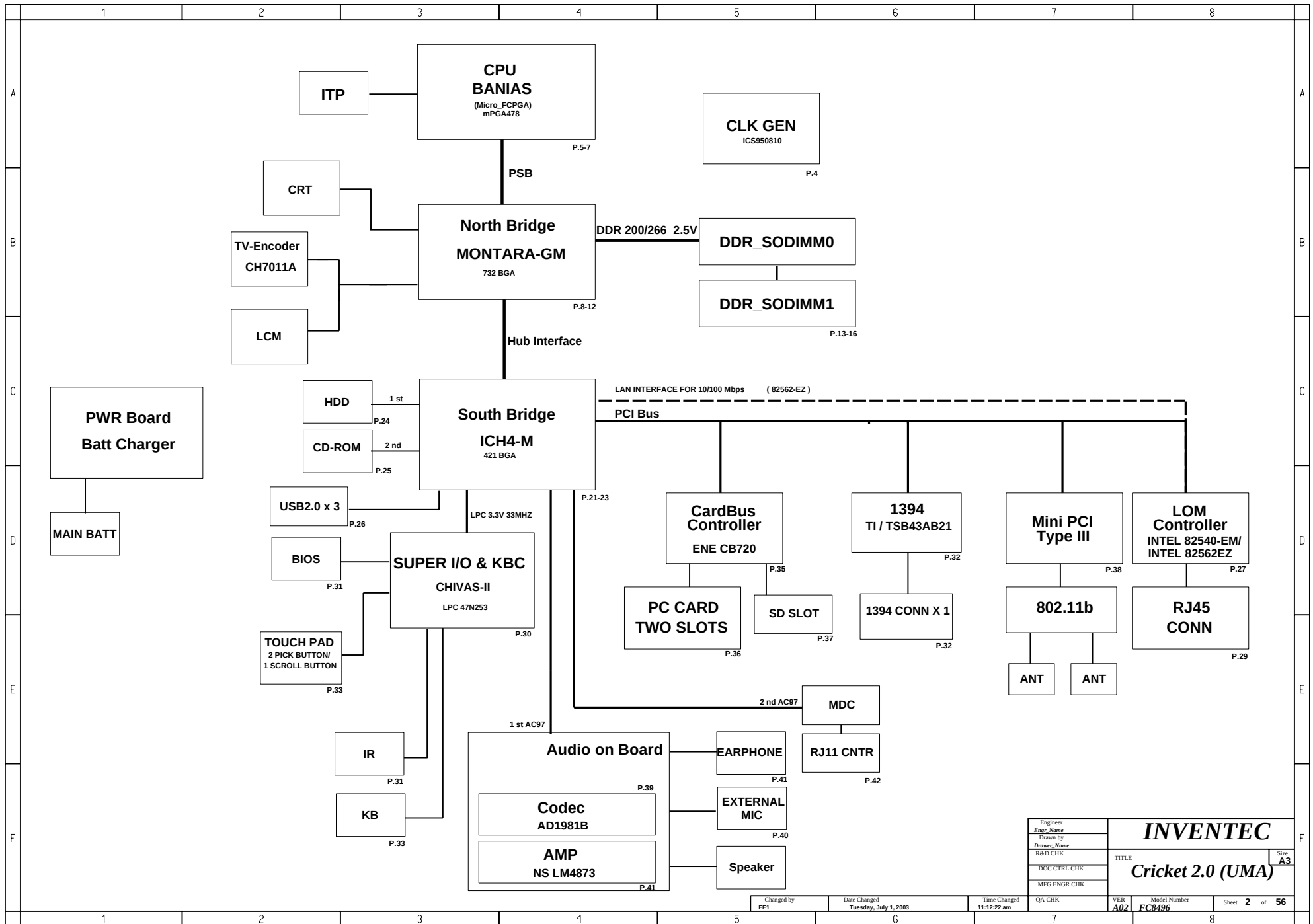
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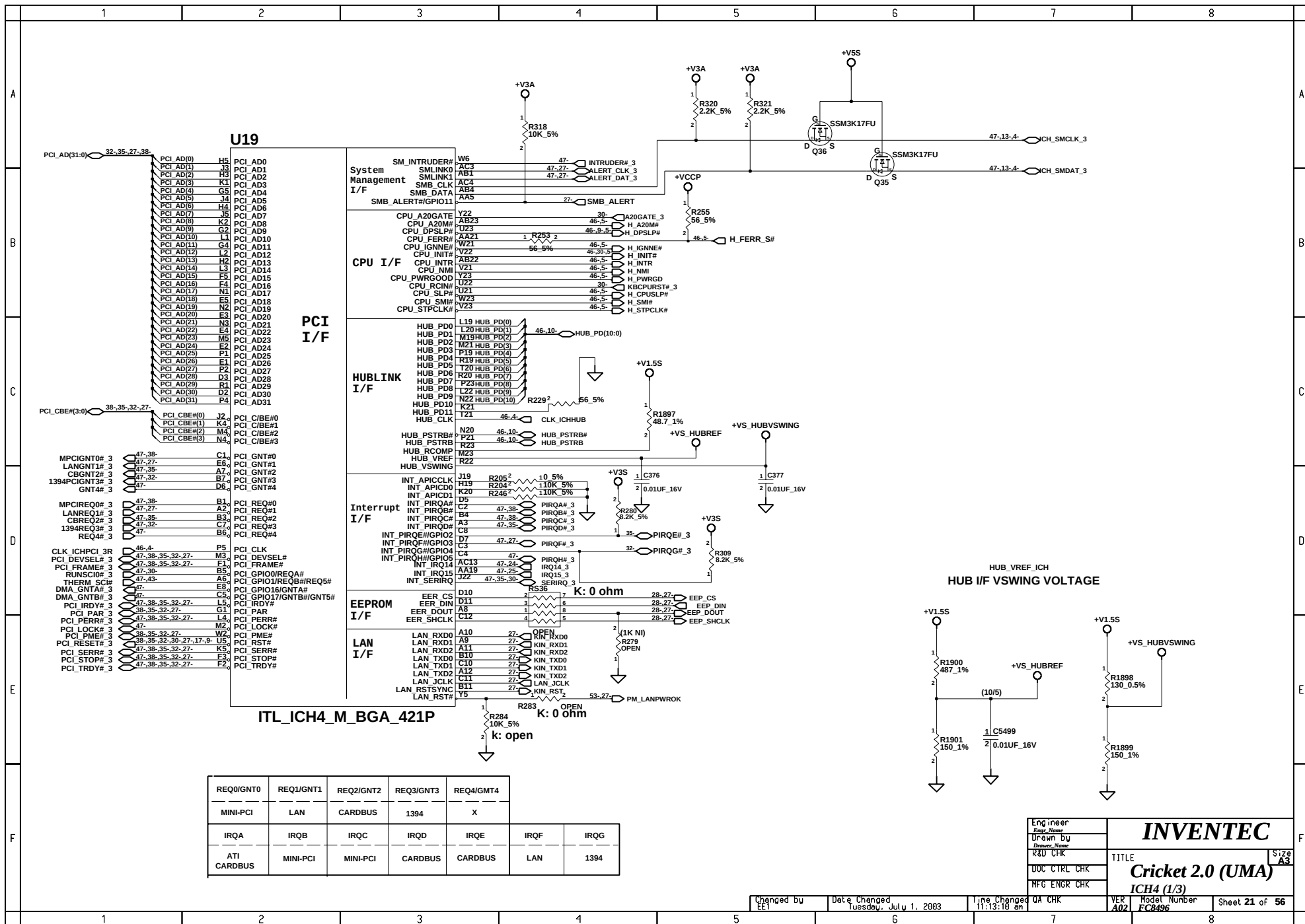
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Drawn by Drawn. Name			
R&D CHK			
DOC CTRL CHK			
MFG ENGR CHK			
QA CHK	VER A02	Model Number FCB496	Sheet 2 of 56

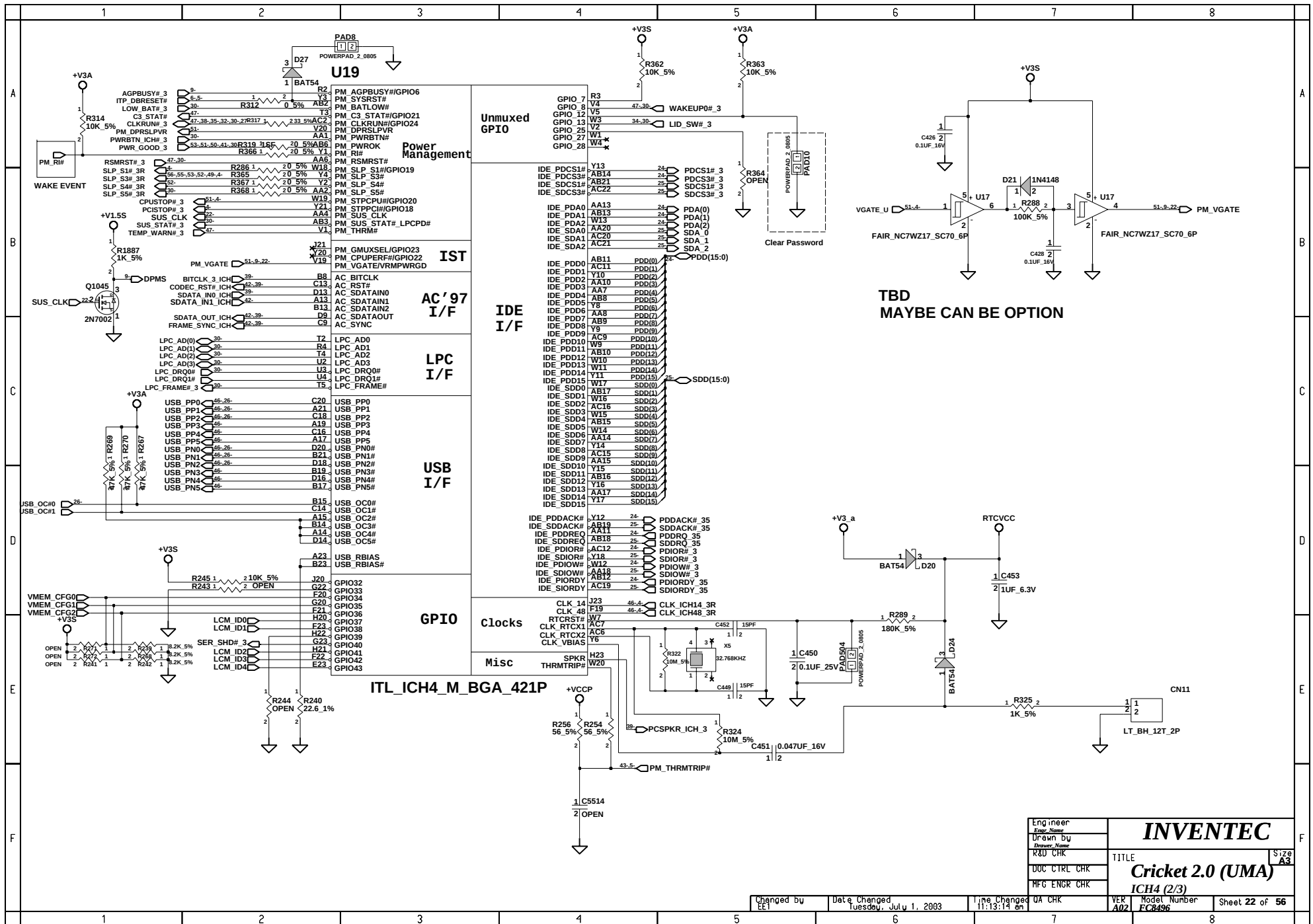
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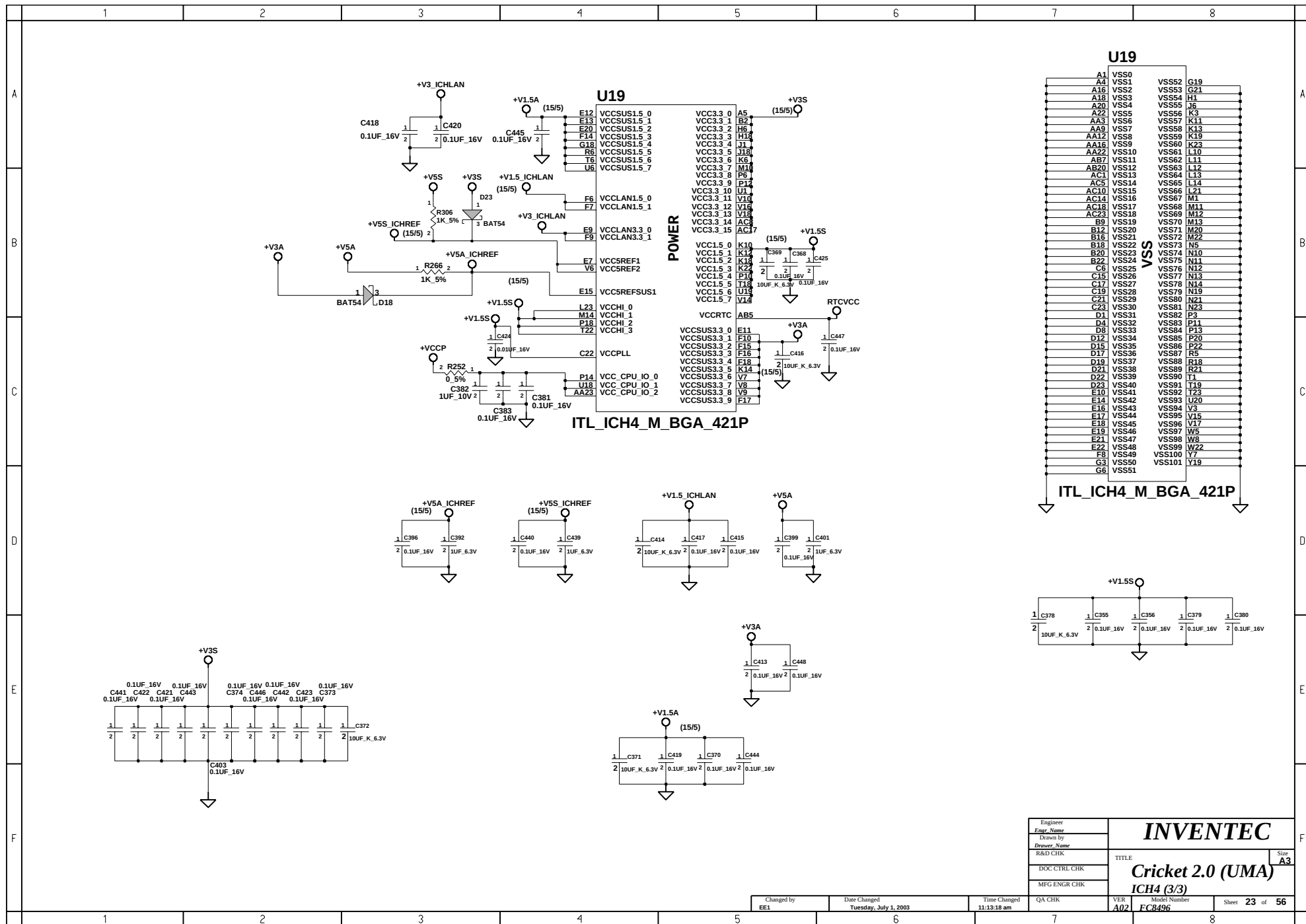
	1	2	3	4	5	6	7	8									
A									A								
B									B								
C									C								
D									D								
E									E								
F									F								
				Changed by EE1		Date Changed Tuesday, July 1, 2003		Time Changed 11:13:09 am		QA CHK		VER A02		Model Number ECB496		Sheet 20 of 56	
	1	2	3	4	5	6	7	8									

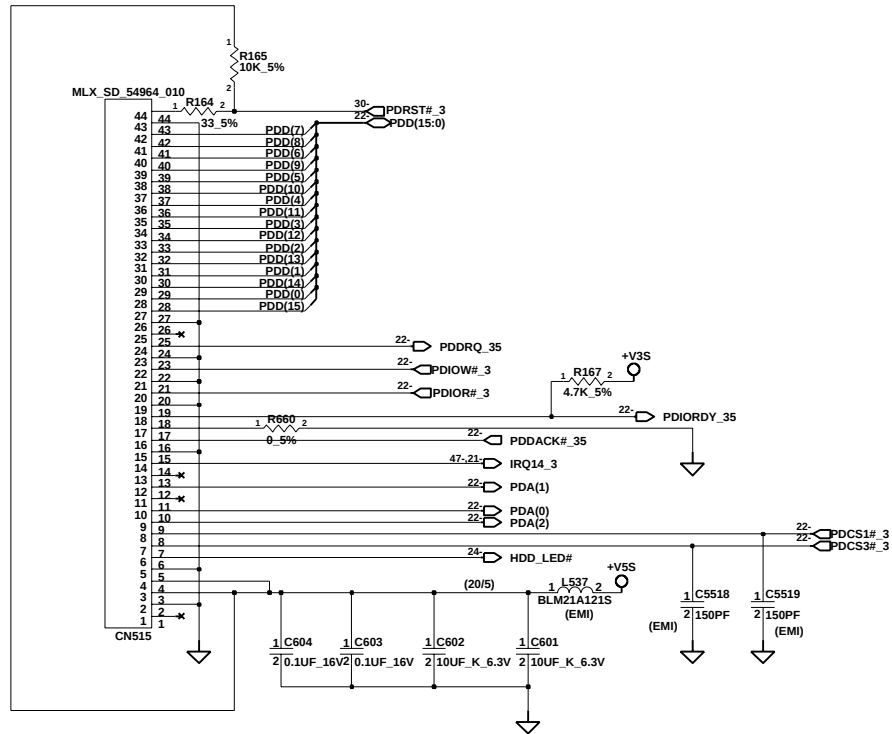
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Engineer <i>Engr. Name</i>		INVENTEC		
Drawn by <i>Drawer. Name</i>				
R&D CHK				
DOC CTRL CHK				
MFG ENGR CHK		TITLE		Size A3
		Cricket 2.0 (UMA)		
		CRT INTERFACE		

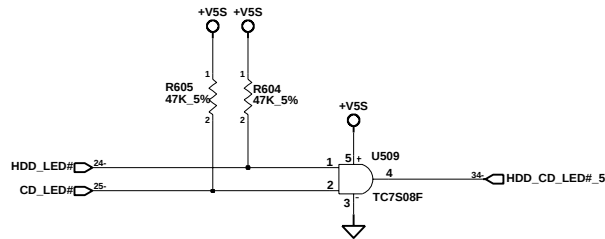






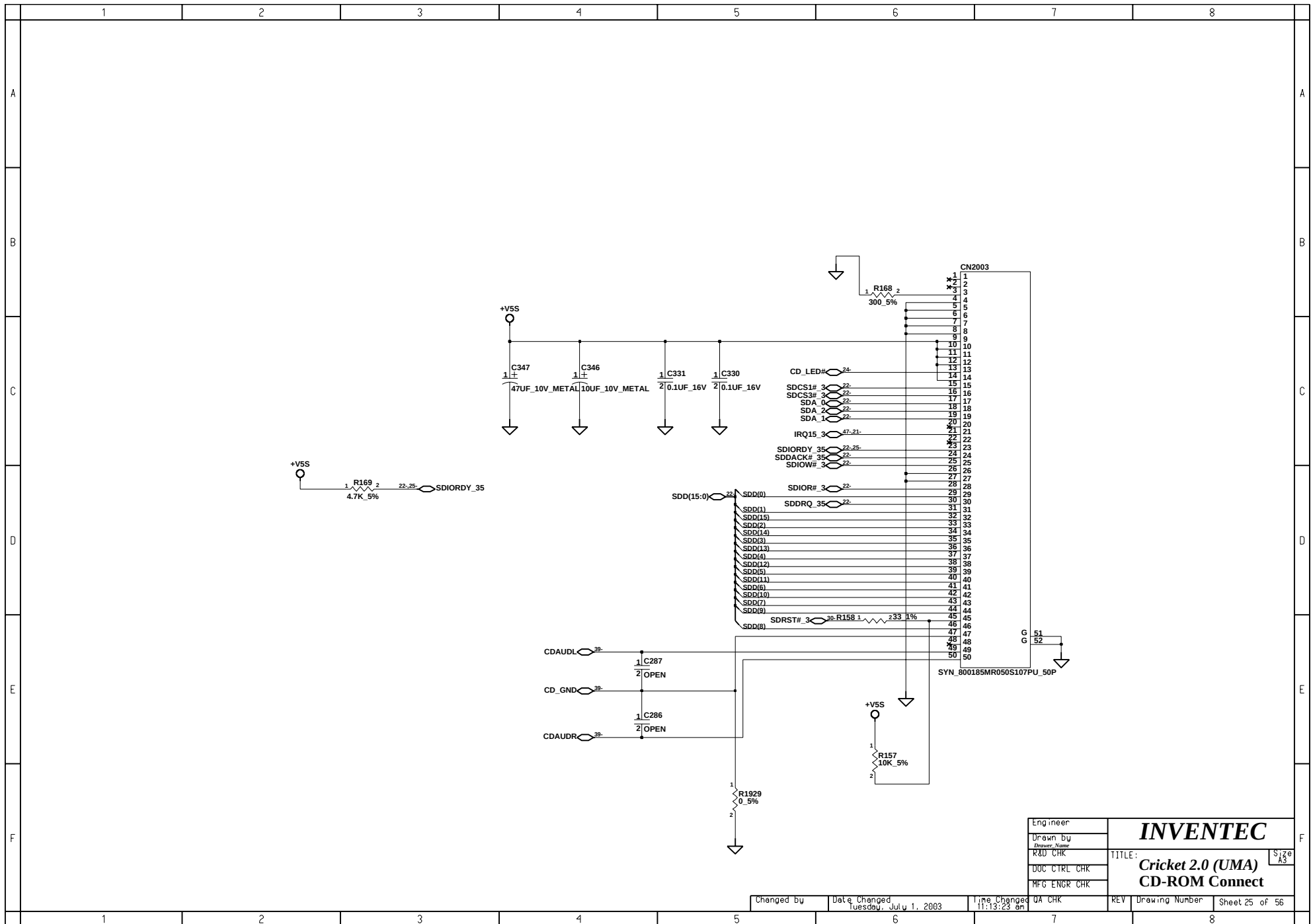


SIGNAL NAME	TRACE WIDTH (MILS)
+V5S	60
HDDPWR	60
+V5S_SBAY	60
SBAYPWR	60



Engineer	INVENTEC TITLE: Cricket 2.0 (UMA) HDD CONNECTOR	Size A3
Drawn by		
Drawer Name R&D CHK		
DOC CTRL CHK		
MFG ENGR CHK		

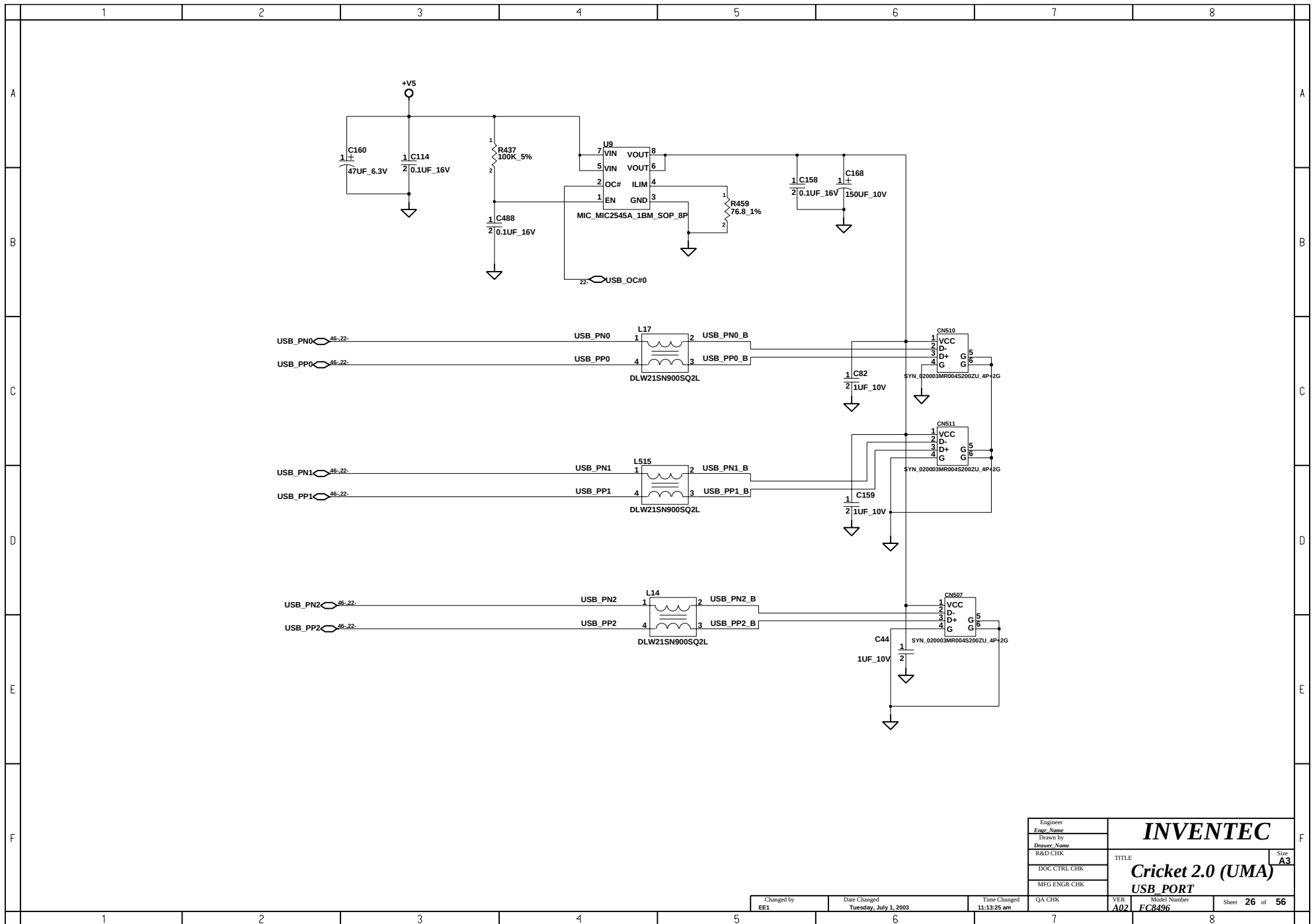
Changed by	Date Changed Tuesday, July 1, 2003	Time Changed 11:13:21 am	Rev'd	Drawing Number	Sheet 24 of 56
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Engineer	INVENTEC		
Drawn by	R&D CHK		
DOC CTRL CHK	MFG ENGR CHK		
REV	UA CHK		

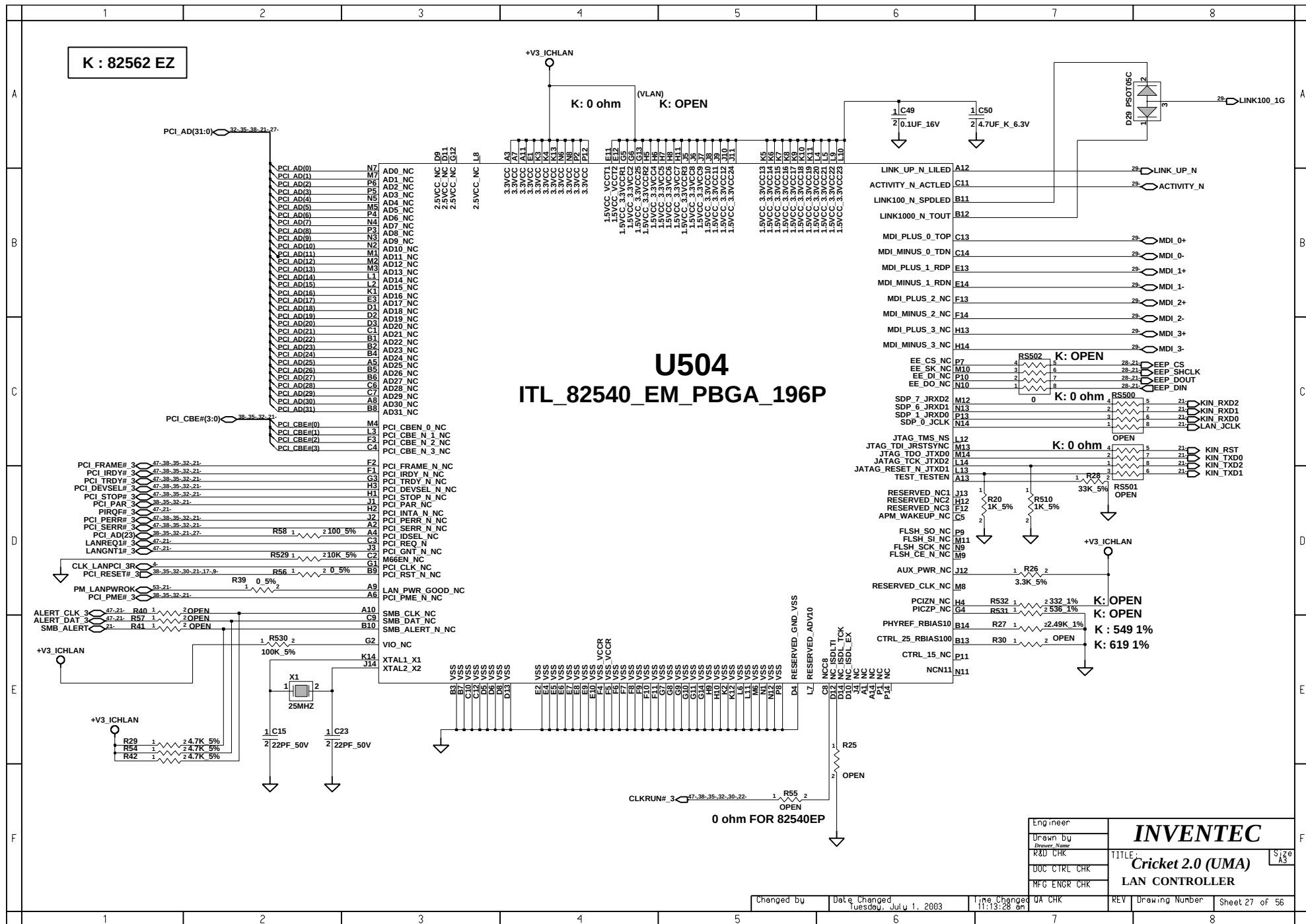
TITLE: **Cricket 2.0 (UMA)**
CD-ROM Connect

Changed by	Date Changed	Time Changed	REV	Drawing Number	Sheet 25 of 56
	Tuesday, July 1, 2003	11:13:23 am			



Engineer	INVENTEC TITLE: Cricket 2.0 (UMA) USB PORT			Size A3
Engr. Name				
Drawn by				
Drawn Name				
R&D CHK				
DOC CTRL CHK	VER A02 Model Number FCB496			Sheet 26 of 56
MFG ENGR CHK				

Changed by EE1	Date Changed Tuesday, July 1, 2003	Time Changed 11:13:25 am
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1 2 3 4 5 6 7 8

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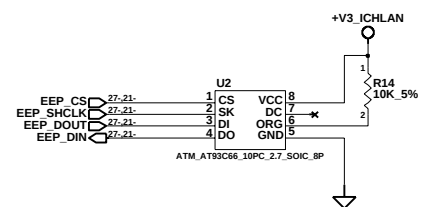
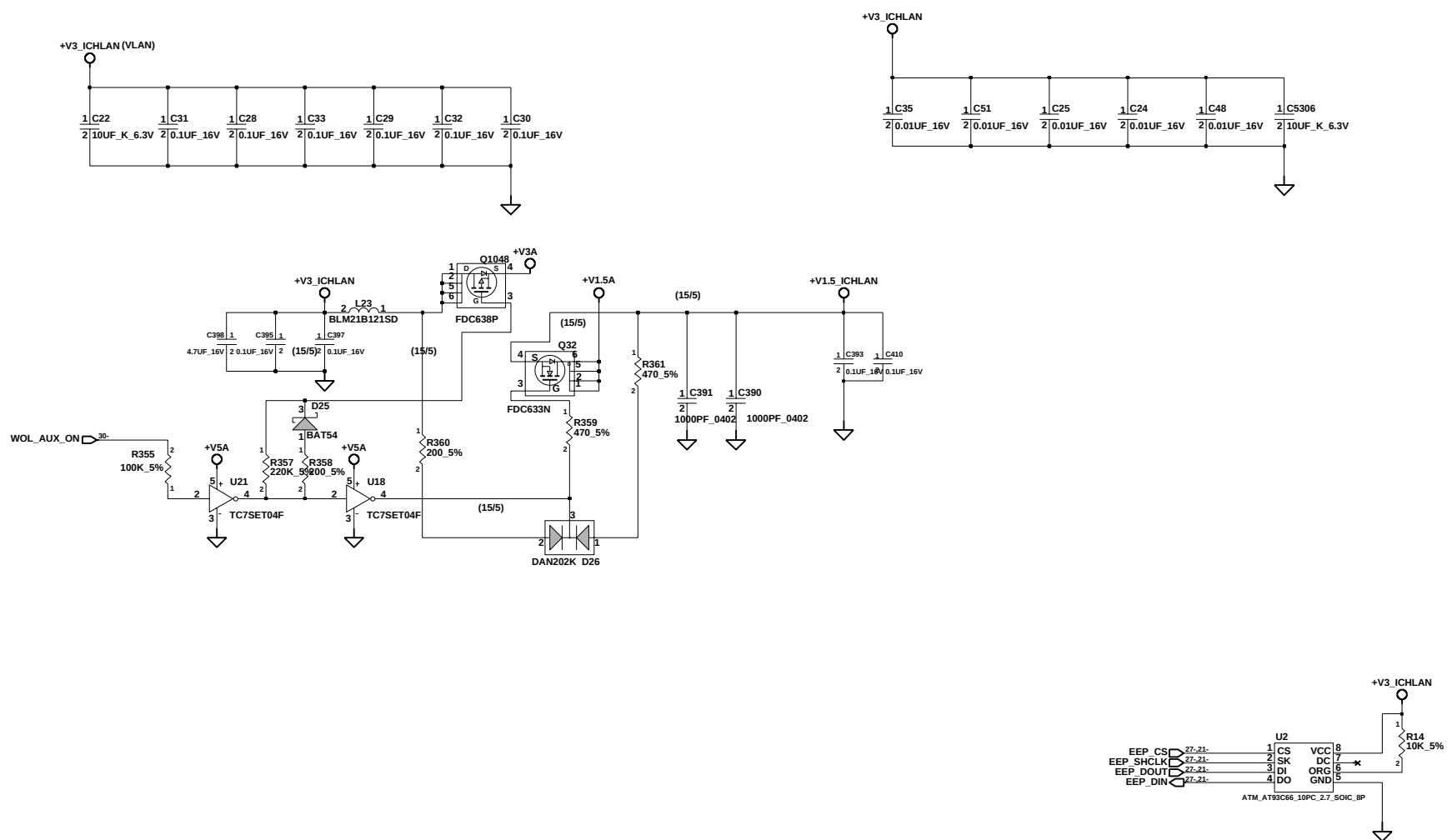
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C

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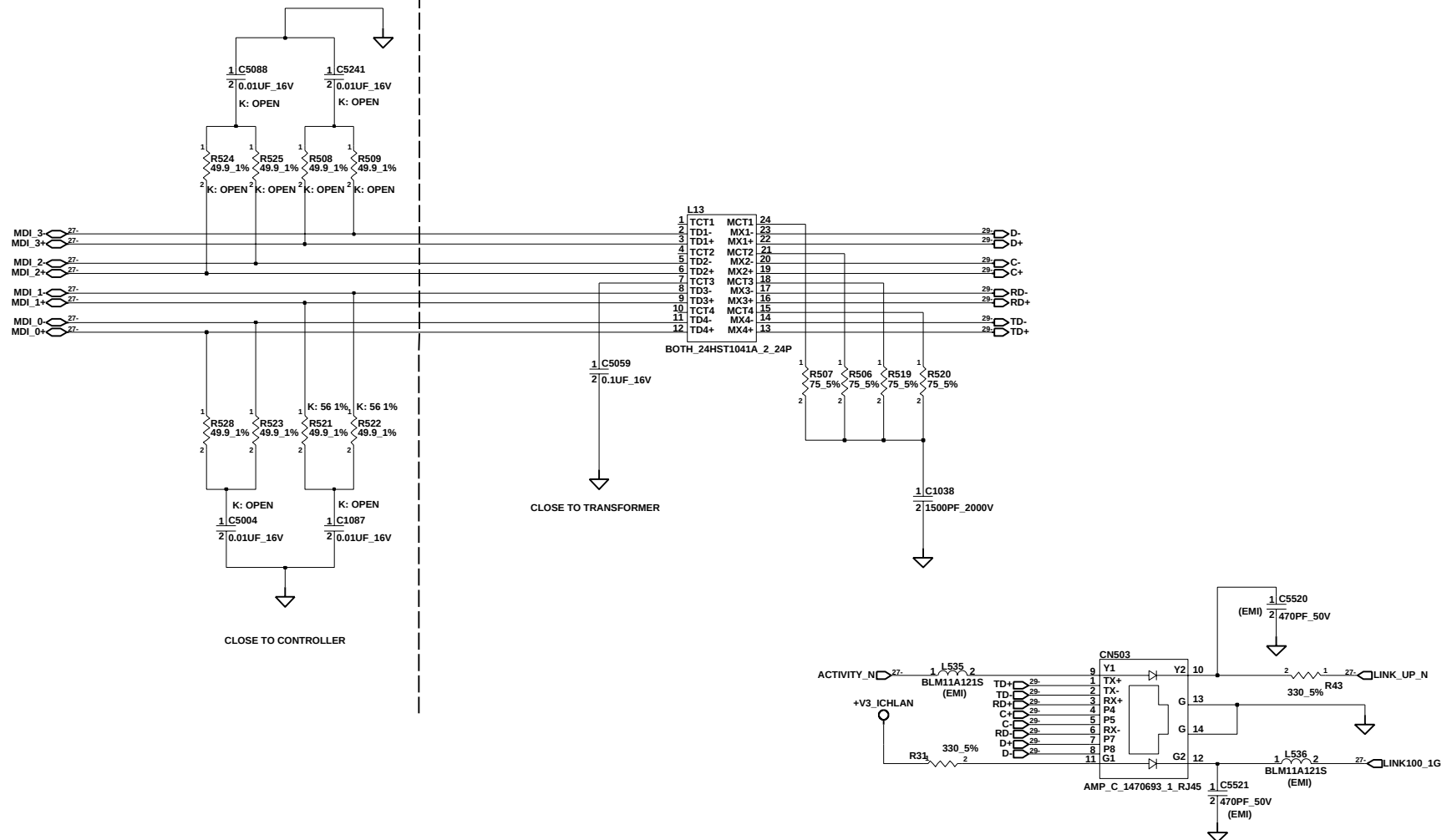
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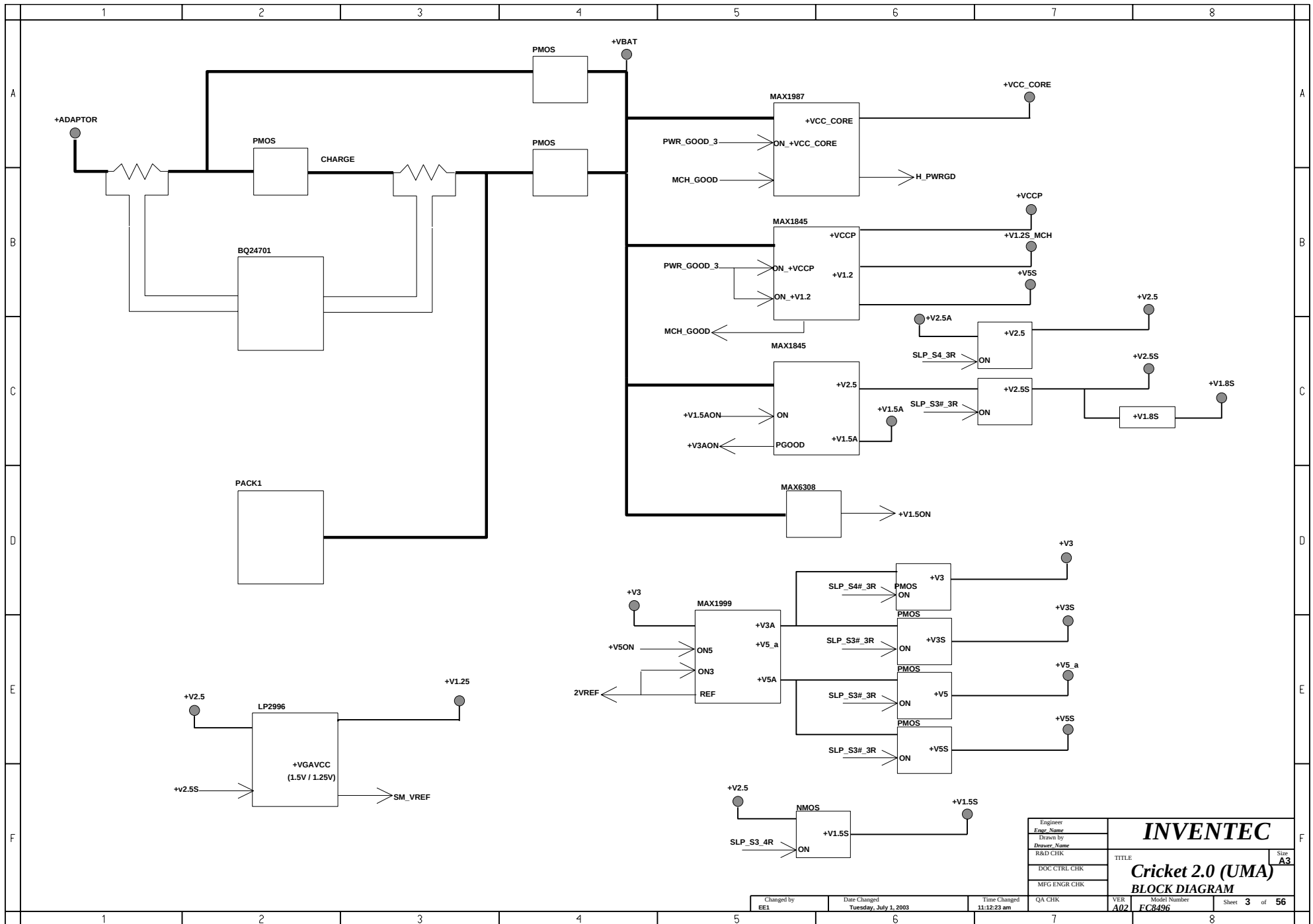


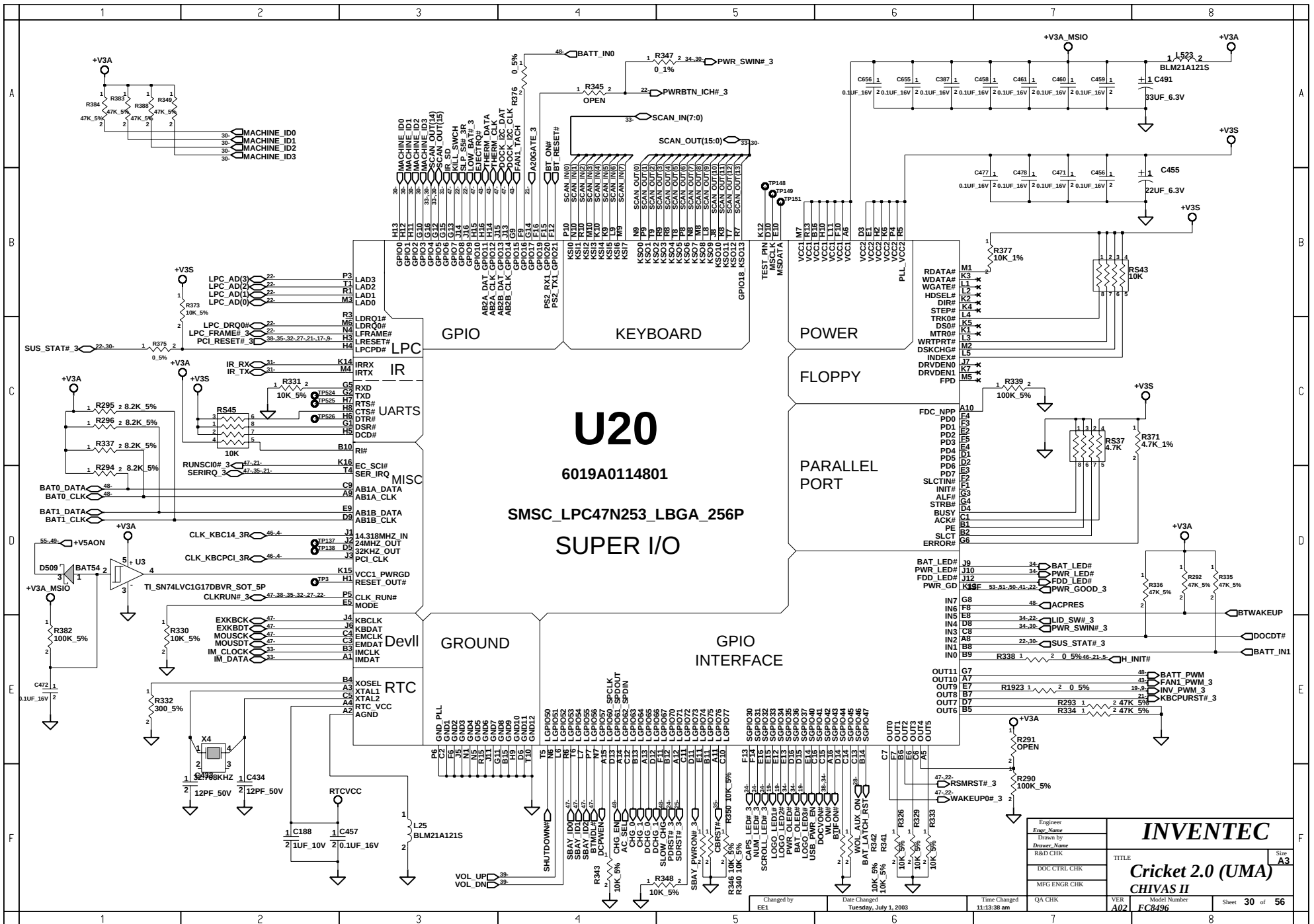
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Drawn by Drawer Name						
R&D CHK						
DOC CTRL CHK	TITLE Cricket 2.0 (UMA) LAN POWER					
MFG ENGR CHK						
QA CHK	Model Number VER FC8496	Sheet 28 of 56				

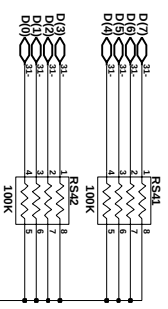
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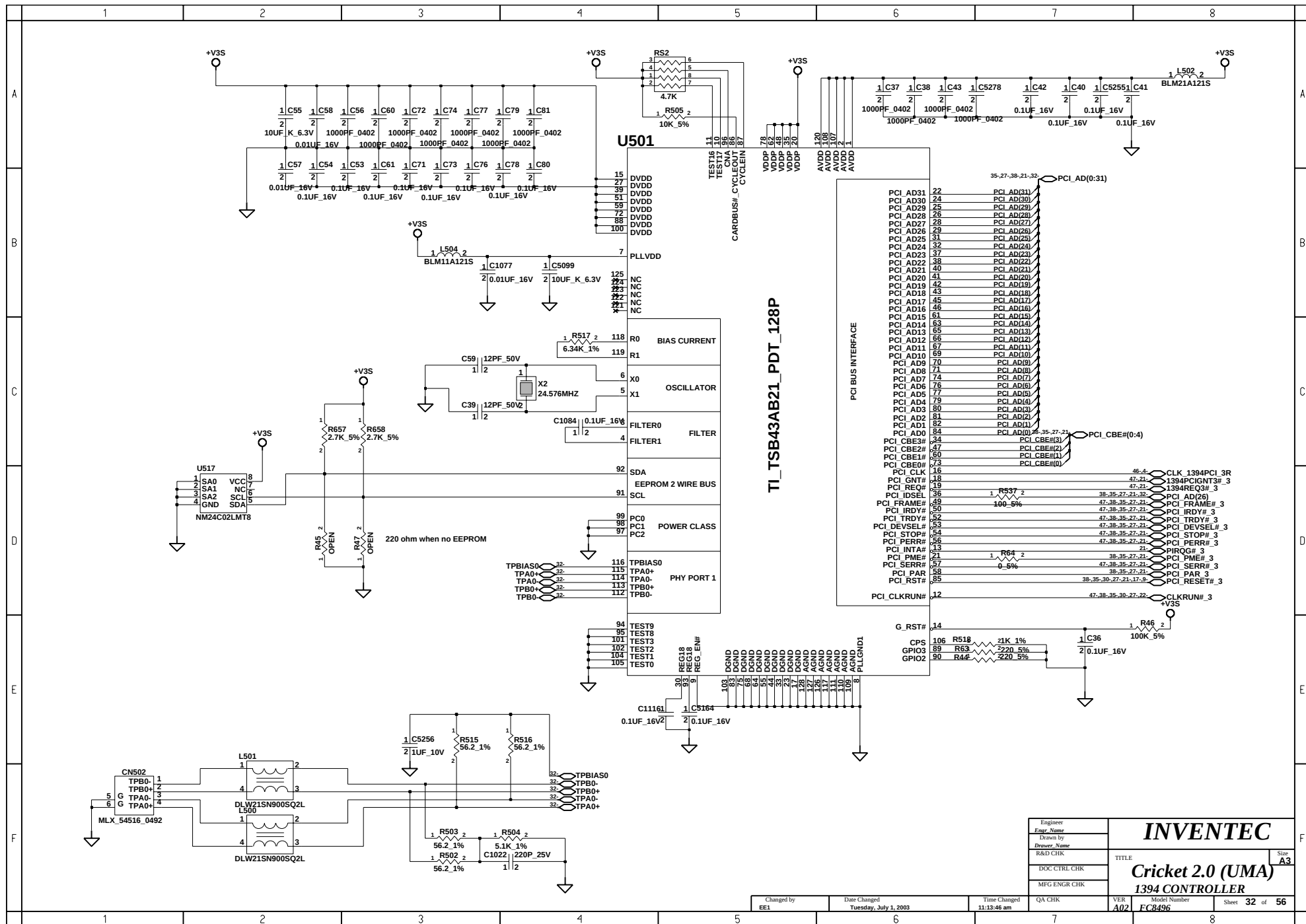
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Drawn by <i>Drawn Name</i>			
R&D CHK			
DOC CTRL CHK			
MFG ENGR CHK			
Changed by EE1	Date Changed Tuesday, July 1, 2003	Time Changed 11:13:34 am	QA CHK A02
Model Number FC8496	Sheet 29	of 56	

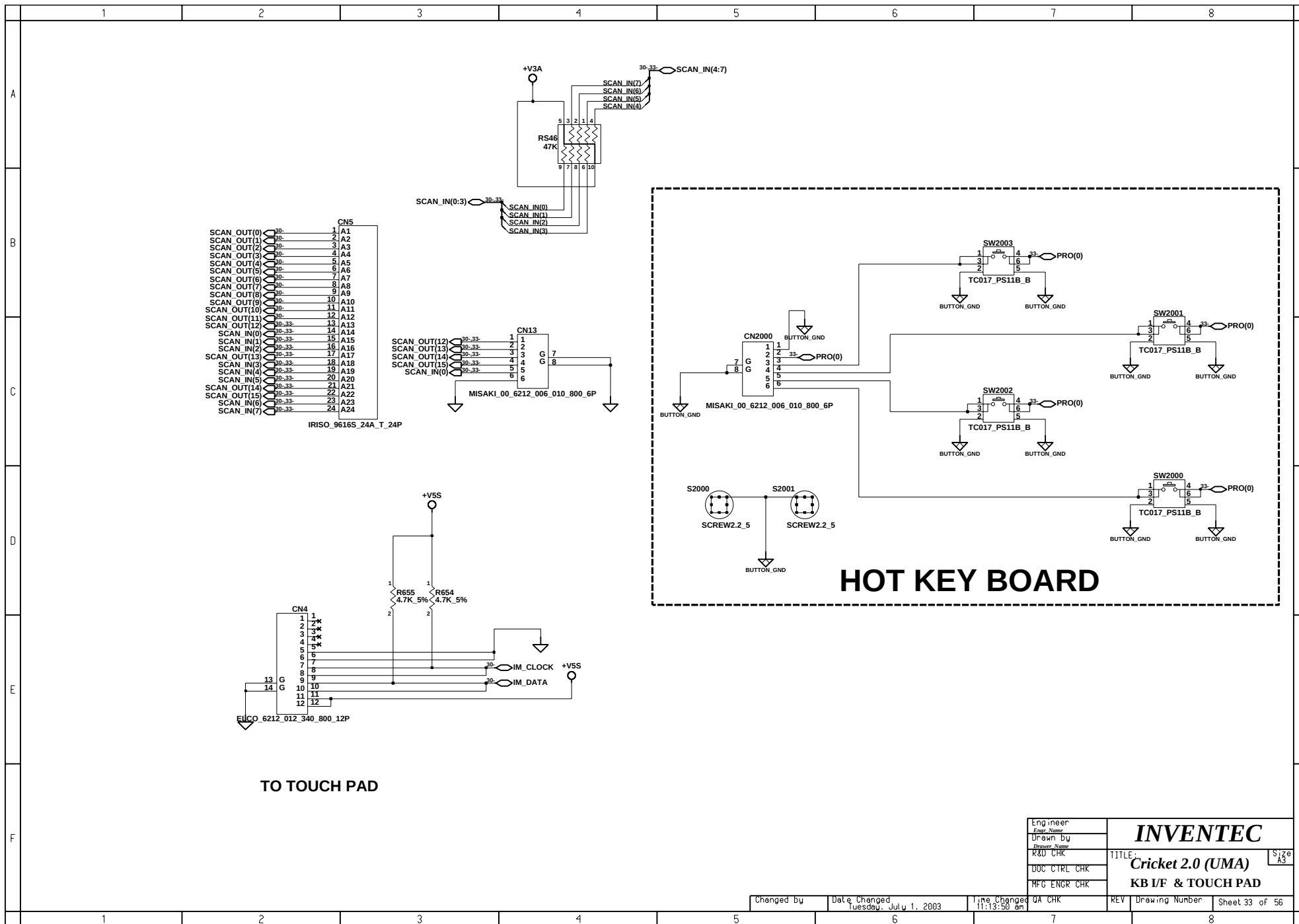


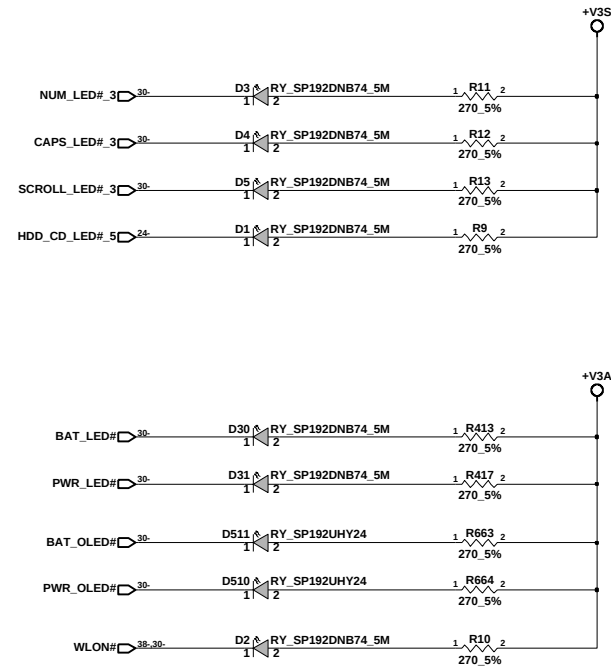
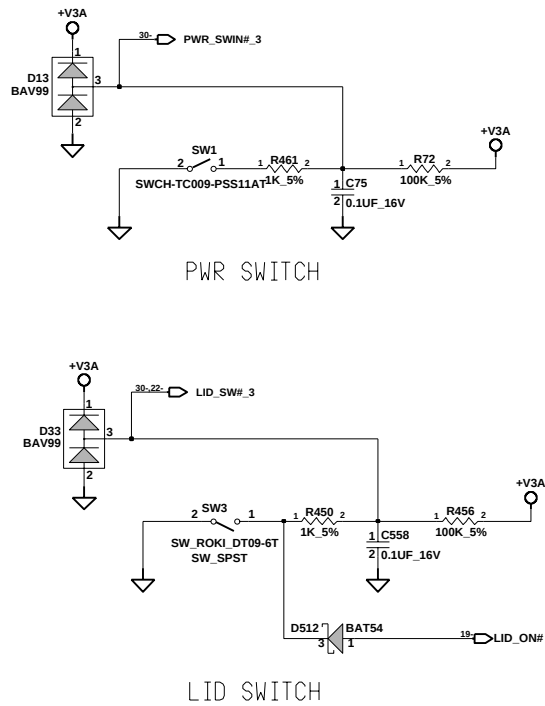




Engineer <i>Eng. Name</i>	INVENTEC Cricket 2.0 (UMA) FLASH ROM & IR	Serial AS
Designed by <i>Designer Name</i>		
Read CPM		
DOC CTRL CHK		
MRG ENCR CHK		
QA CHK		
VER <i>A07</i>	Accepted Number	Sheet 31 of 56
ECR6496		

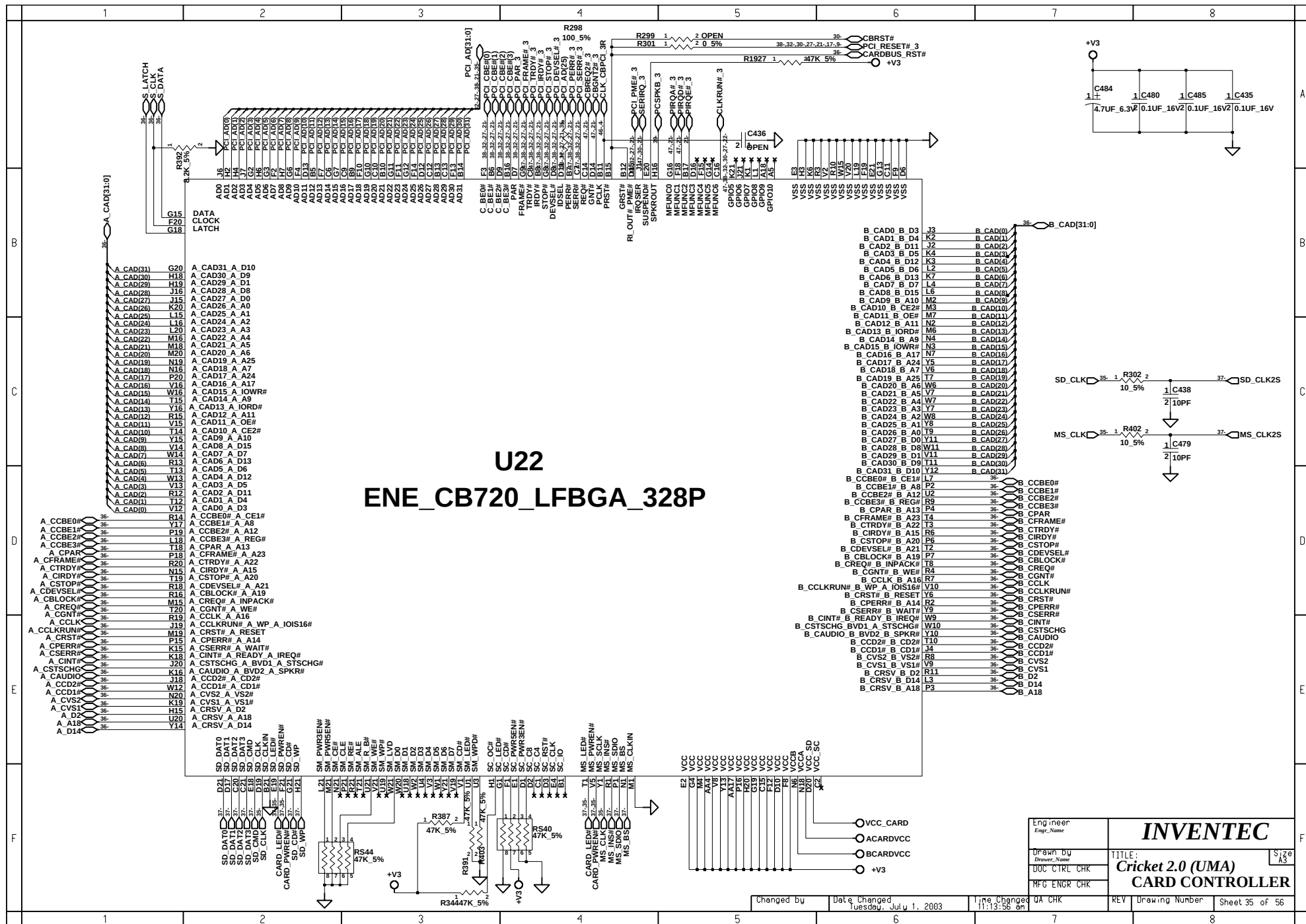


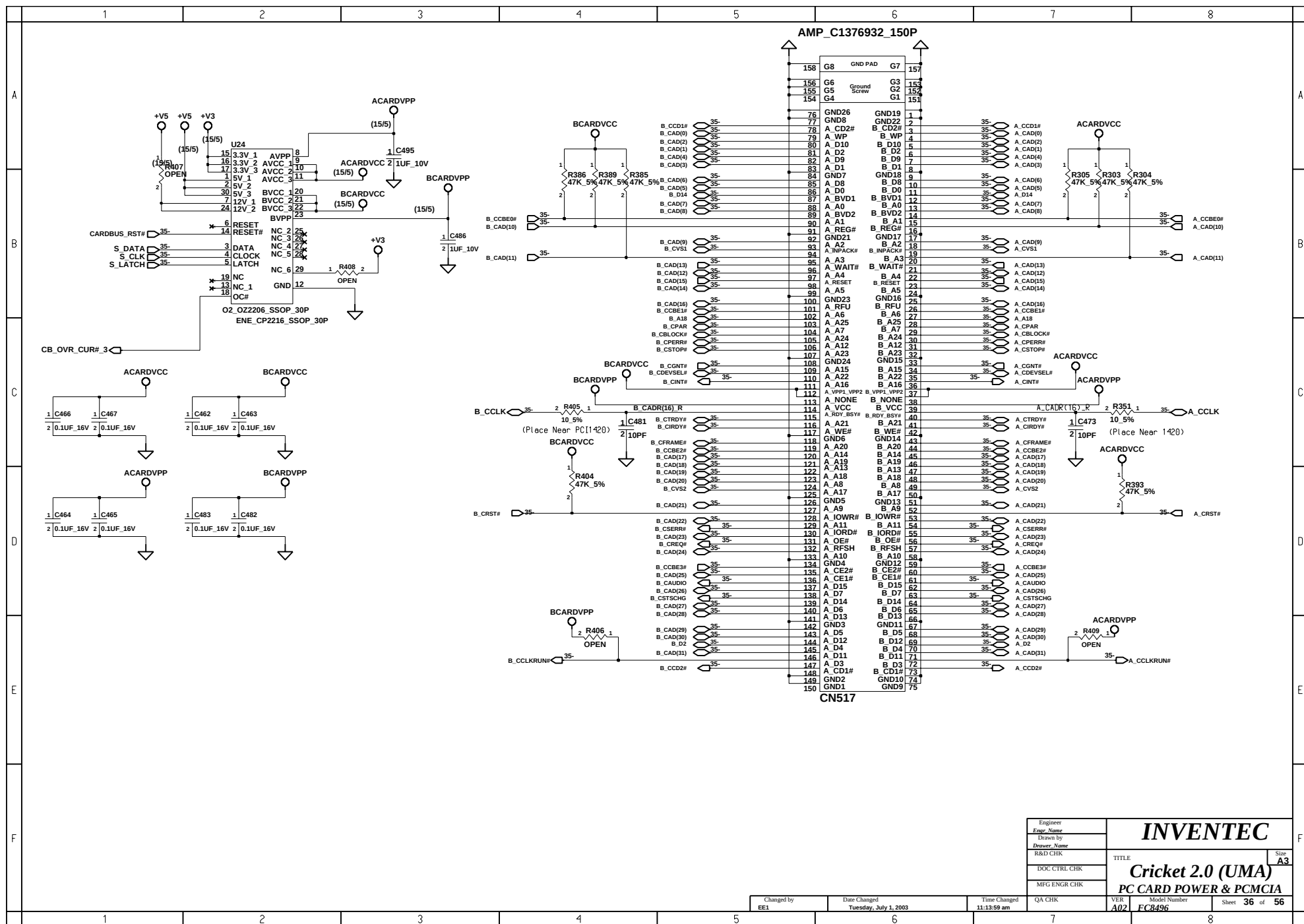


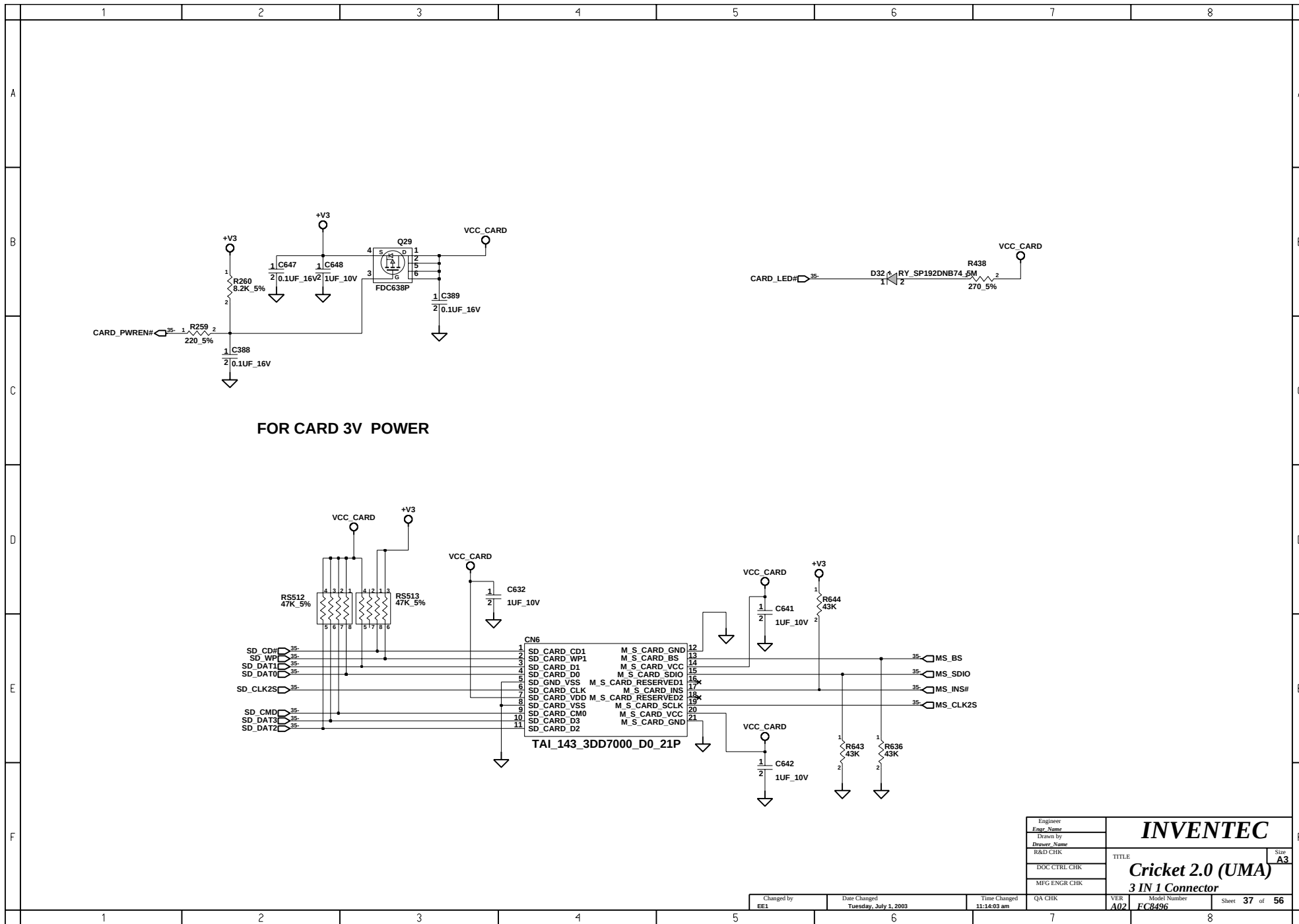


Engineer	INVENTEC		
Drawn by	TITLE: Cricket 2.0 (UMA)		Size
DOC CTRL CHK	MFG ENGR CHK		A3
REV	UA CHK	Drawing Number	Sheet 34 of 56

Changed by	Date Changed Tuesday, July 1, 2003	Time Changed 11:13:53 am
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Engineer Engy. Name	INVENTEC TITLE Cricket 2.0 (UMA) 3 IN 1 Connector		
Drawn by Drawer. Name			
R&D CHK			
DOC CTRL CHK			
MFG ENGR CHK			
Changed by EE1	Date Changed Tuesday, July 1, 2003	Time Changed 11:14:03 am	QA CHK
VER A02	Model Number EC8496	Sheet 37	of 56

1 2 3 4 5 6 7 8

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A

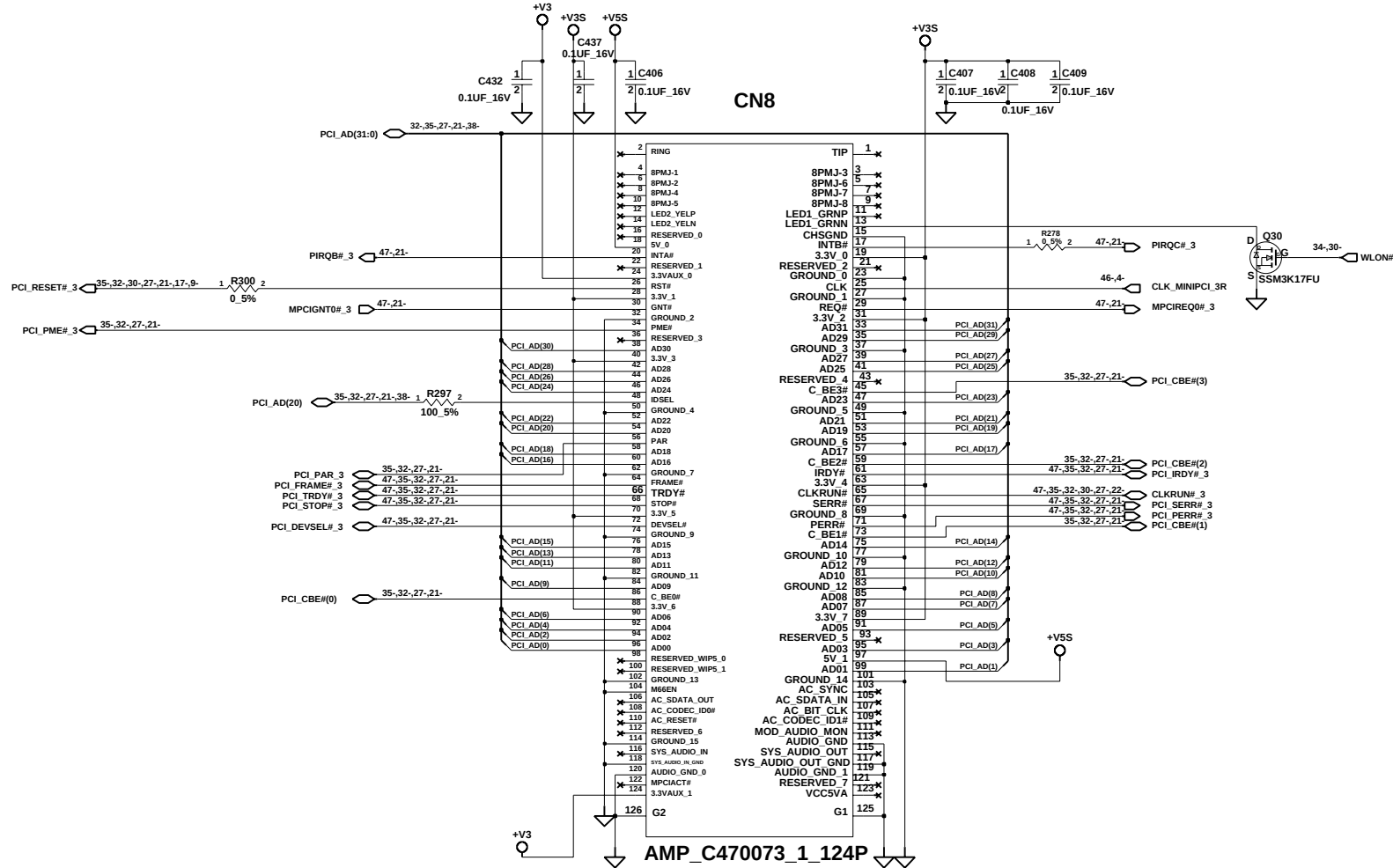
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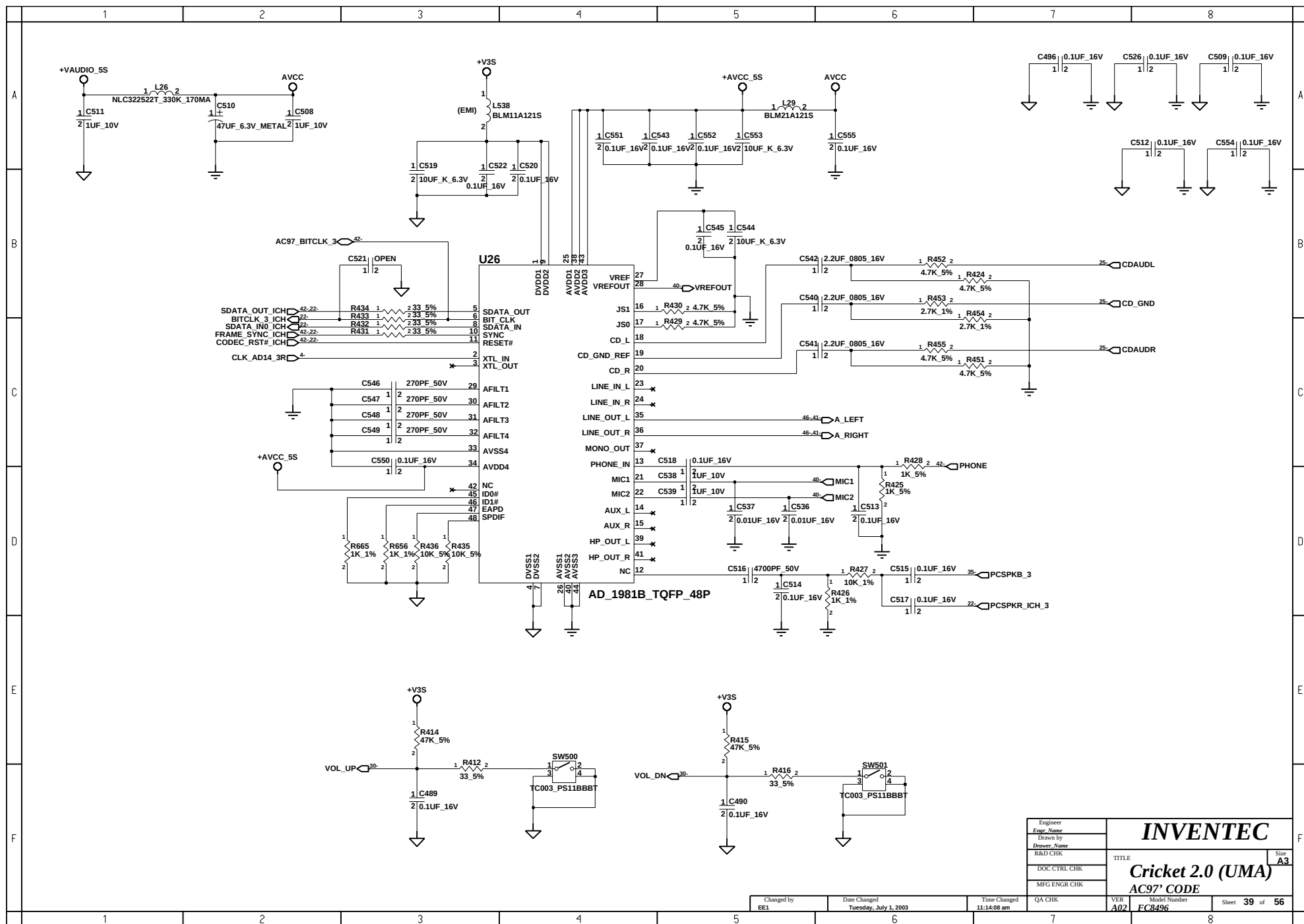
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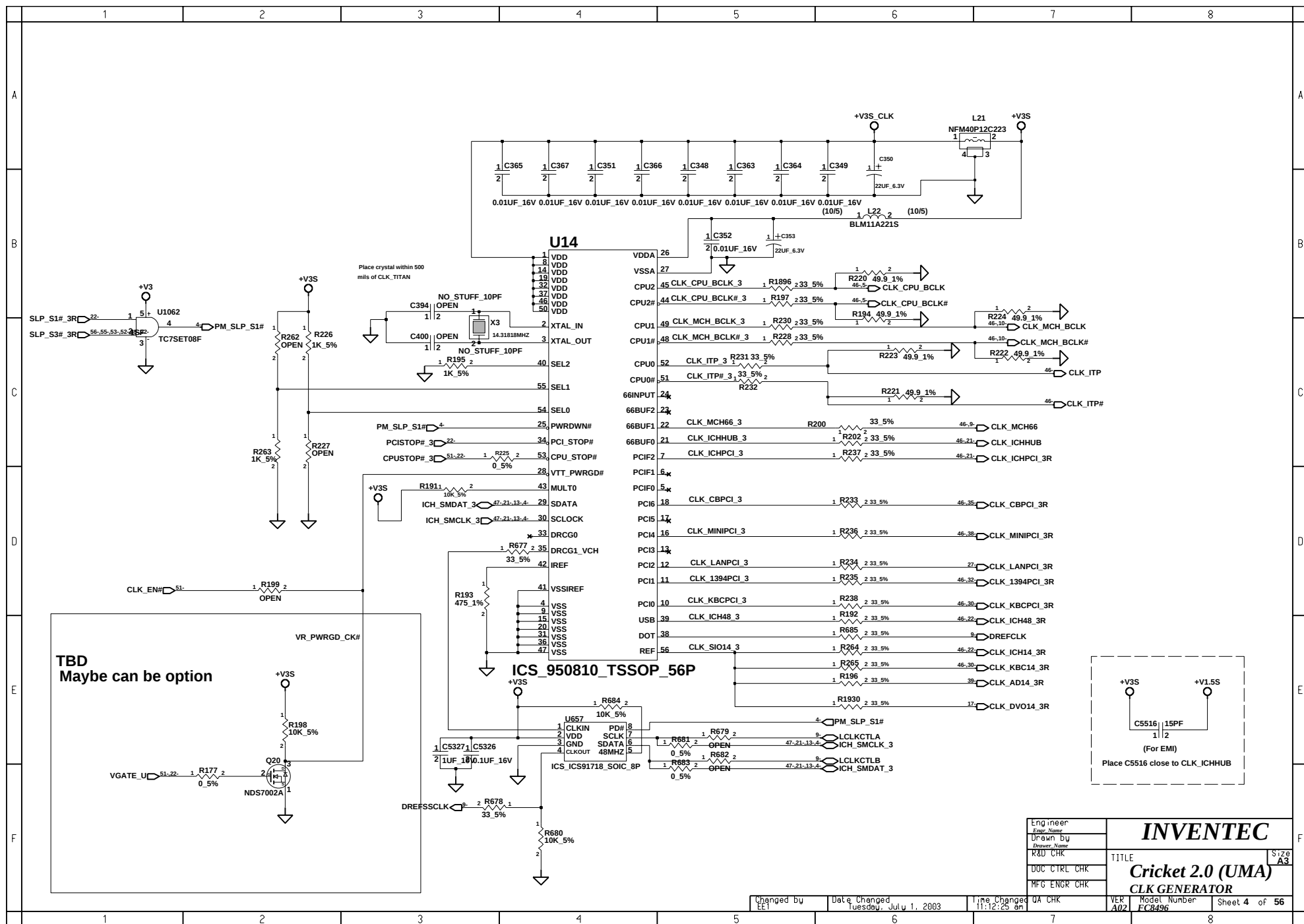


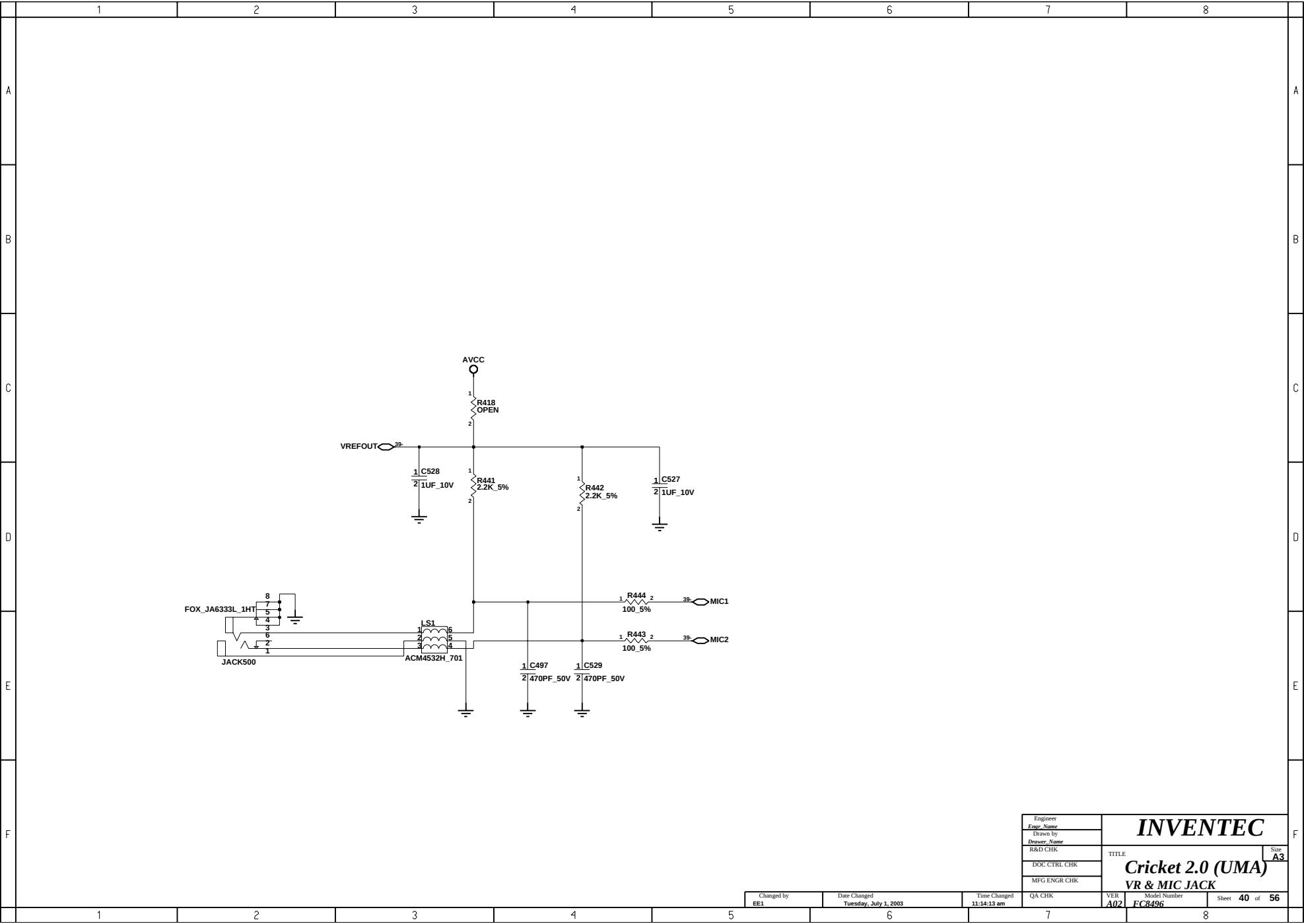
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Drawn by			
Rev'd	TITLE: Cricket 2.0 (UMA)		
DOC CTRL CHK	MINI PCI		
MFG ENGR CHK			

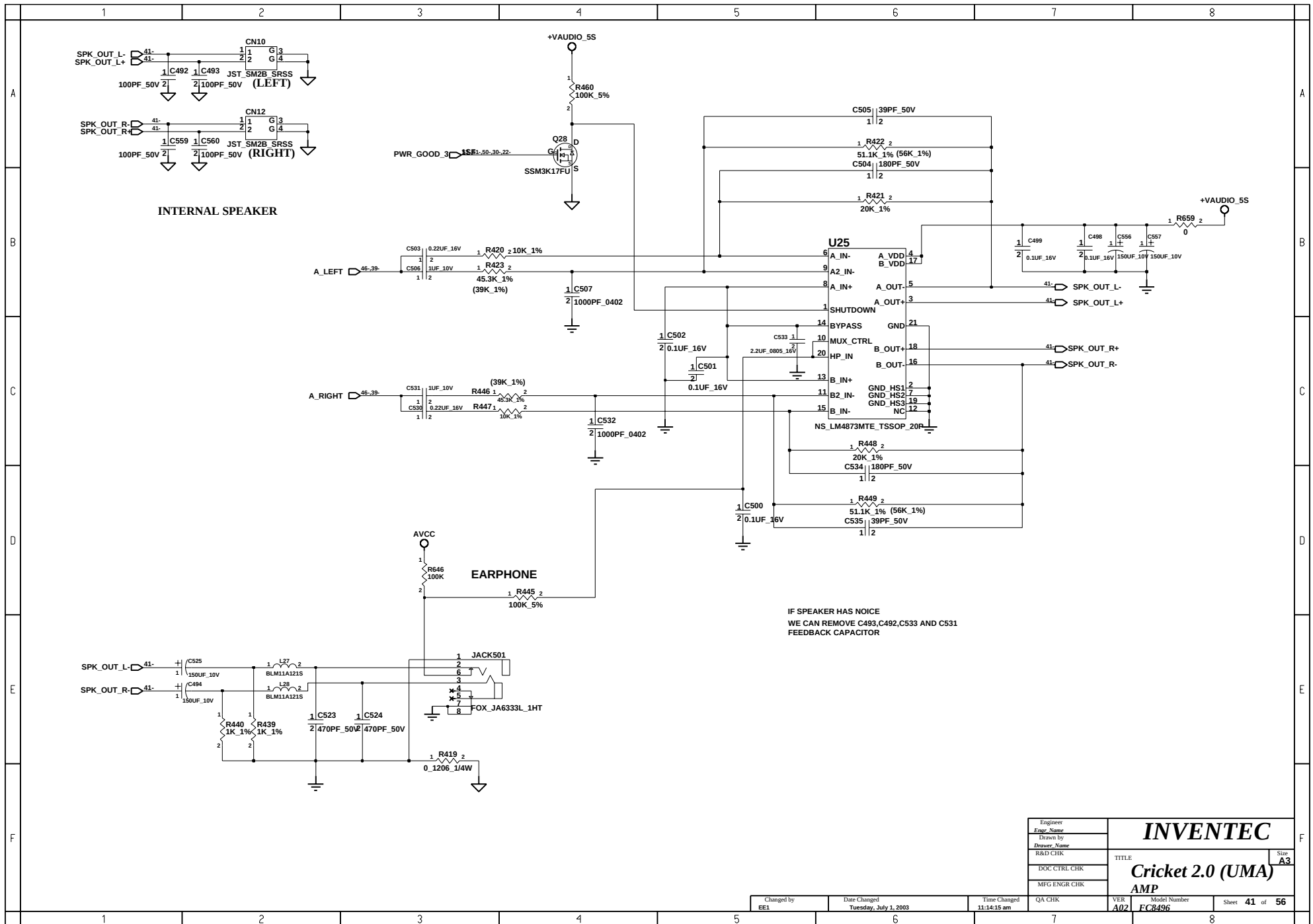
Changed by	Date Changed	Time Changed	Rev	Drawing Number	Sheet 38 of 56
	Tuesday, July 1, 2003	11:14:05 am	UA CHK		

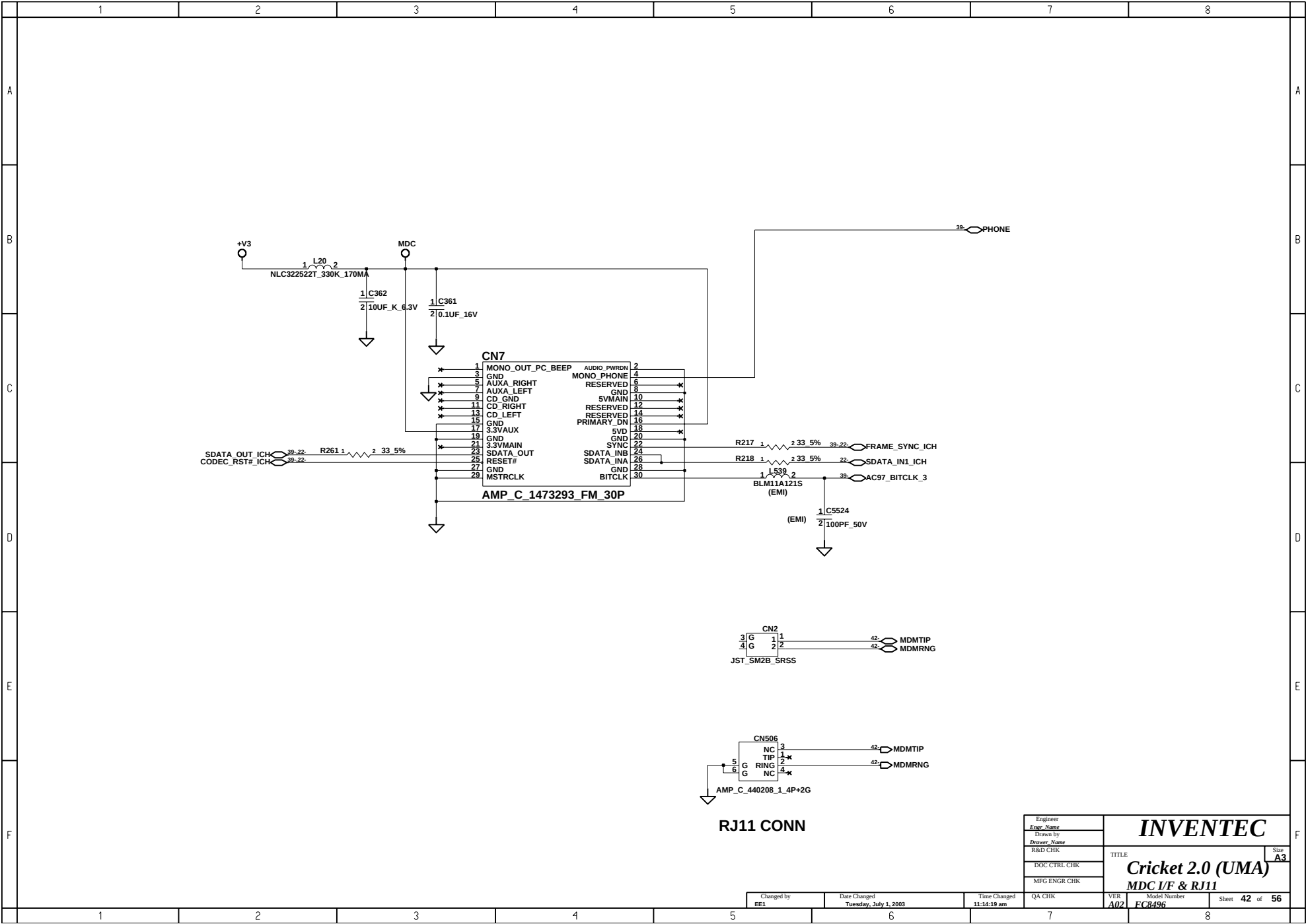
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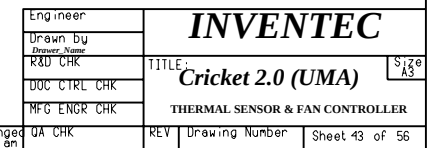


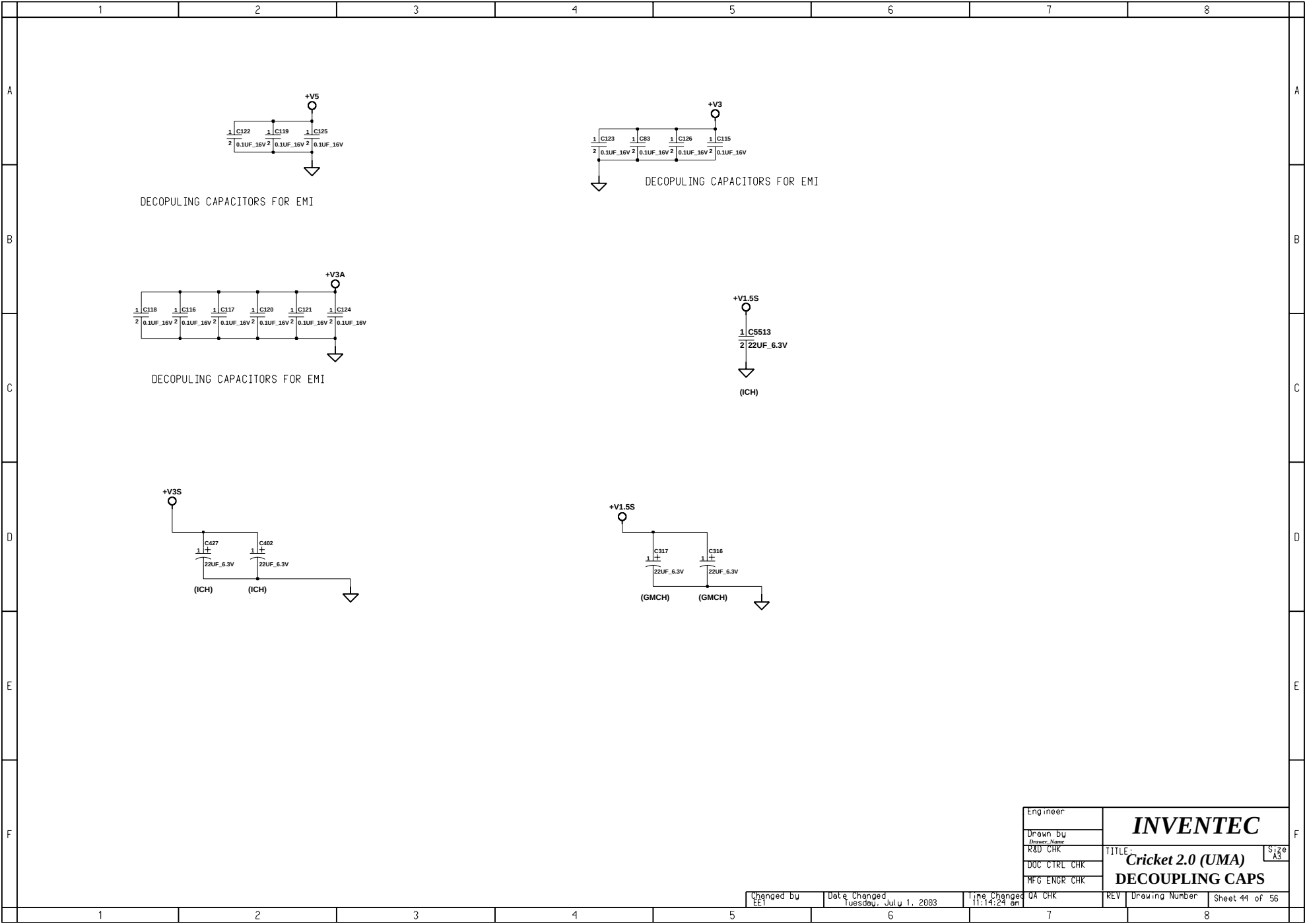




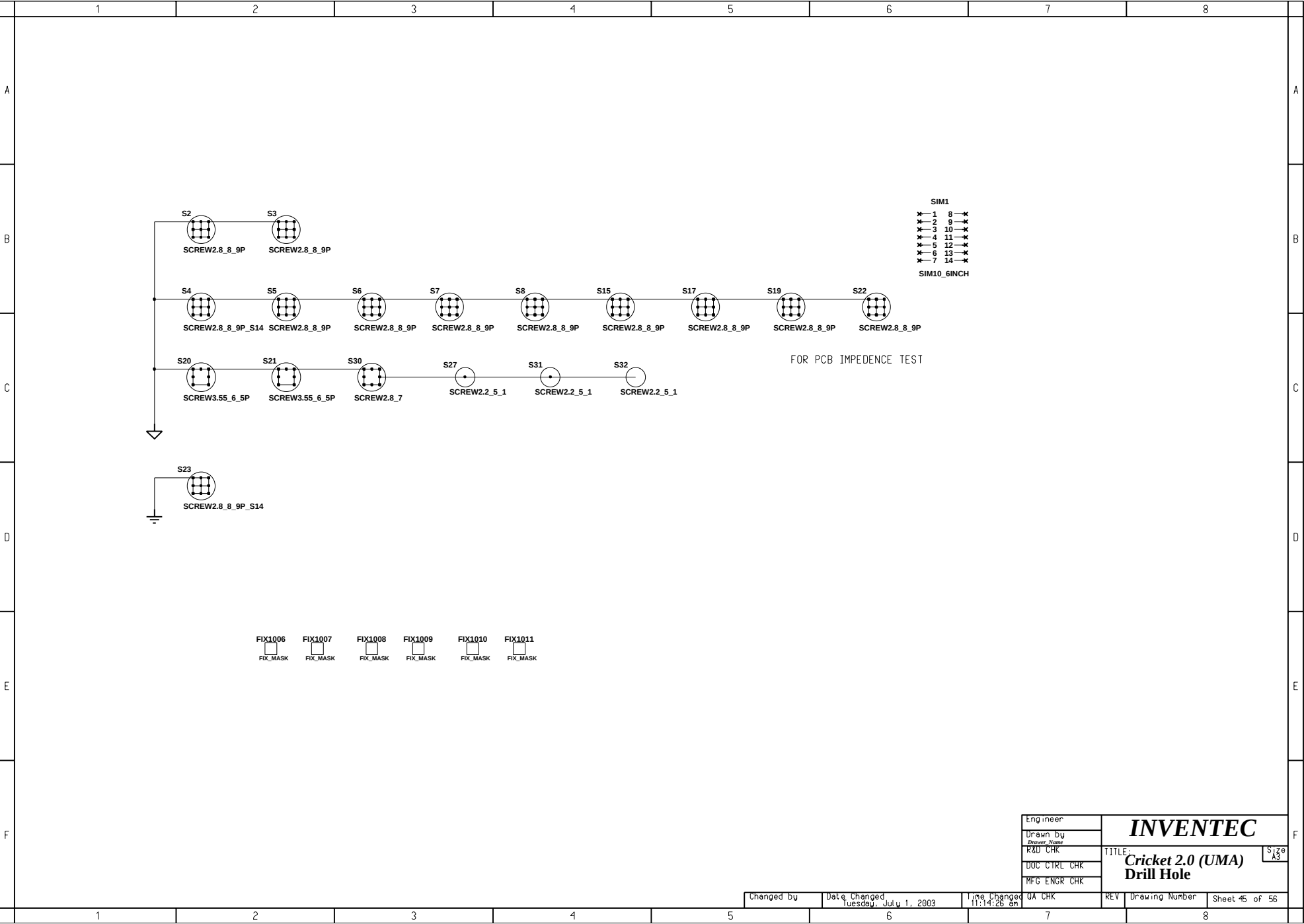


Engineer Engr_Name	INVENTEC		
Drawn by Drawer_Name			
R&D CHK			
DOC CTRL CHK			
MFG ENGR CHK			
TITLE		Size A3	
Cricket 2.0 (UMA)			
MDC I/F & RJ11			
Changed by EE1	Date Changed Tuesday, July 1, 2003	Time Changed 11:14:19 am	QA CHK
VER A02	Model Number ECB496	Sheet 42 of 56	



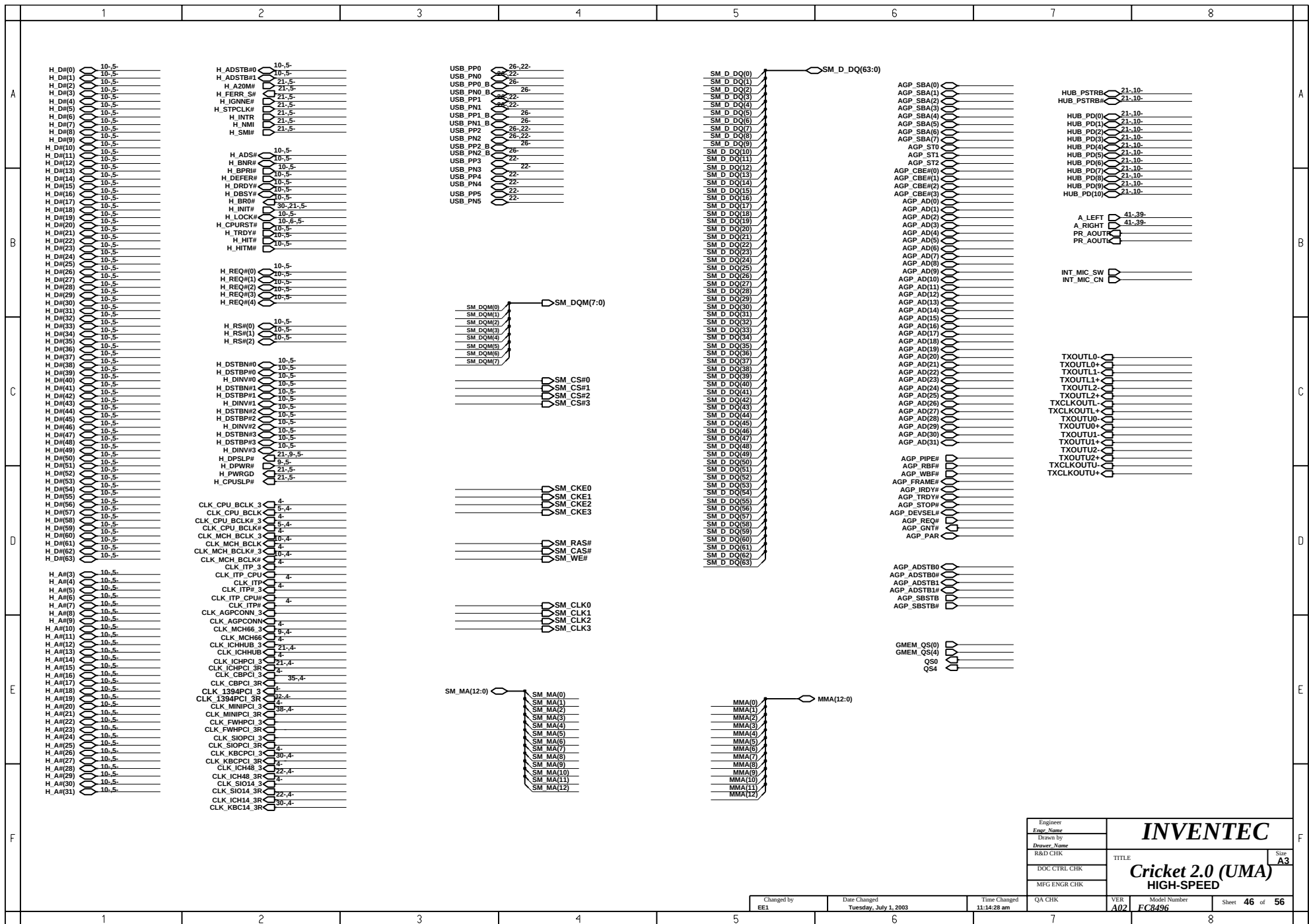


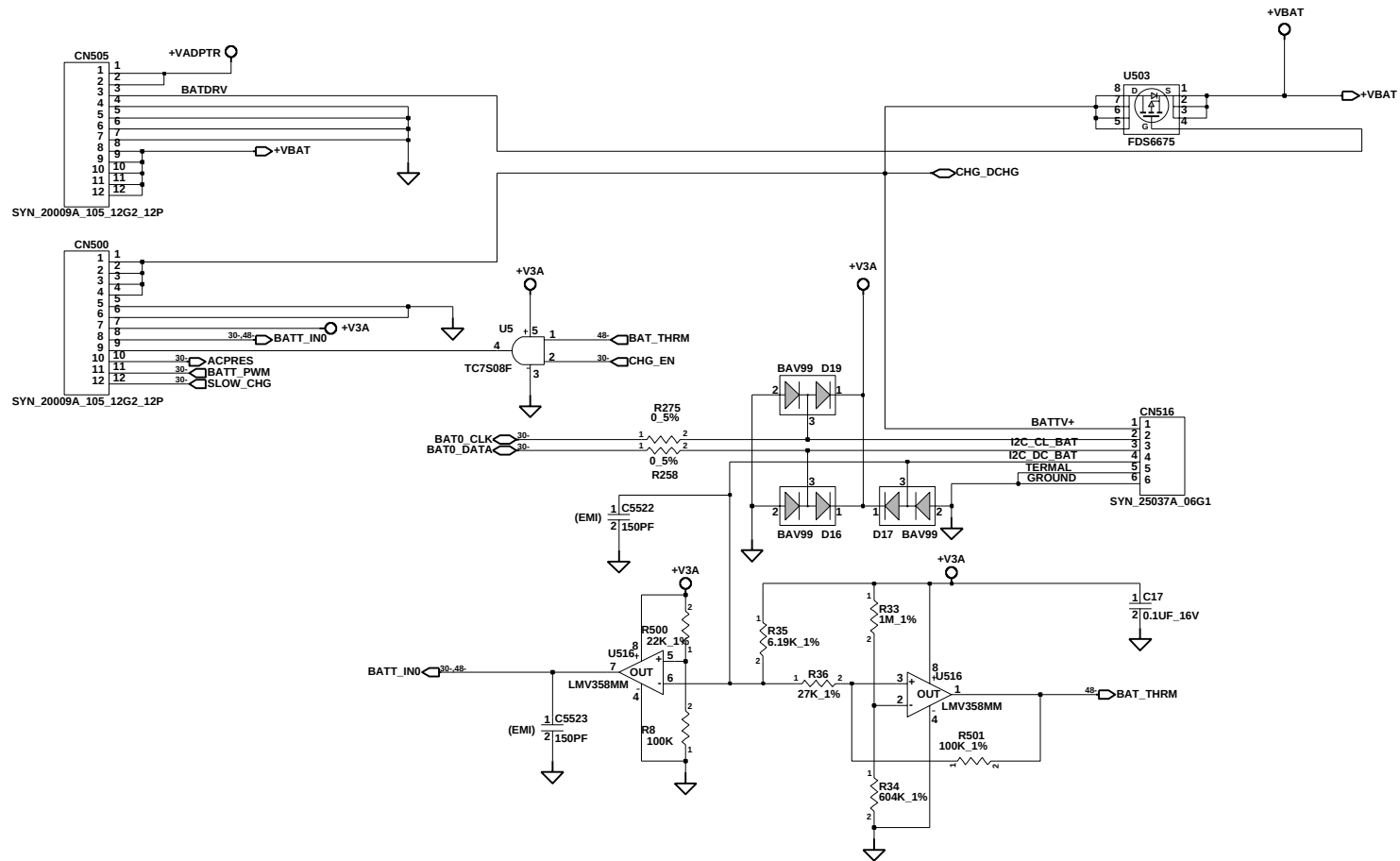
Engineer	INVENTEC Cricket 2.0 (UMA) DECOUPLING CAPS		
Drawn by			
R&D CHK			
DOC CTRL CHK			
MFG ENGR CHK			
Changed by	Date Changed	Time Changed	REV
EET	Tuesday, July 1, 2003	11:14:24 am	UA CHK
Drawing Number	Sheet 44 of 56		



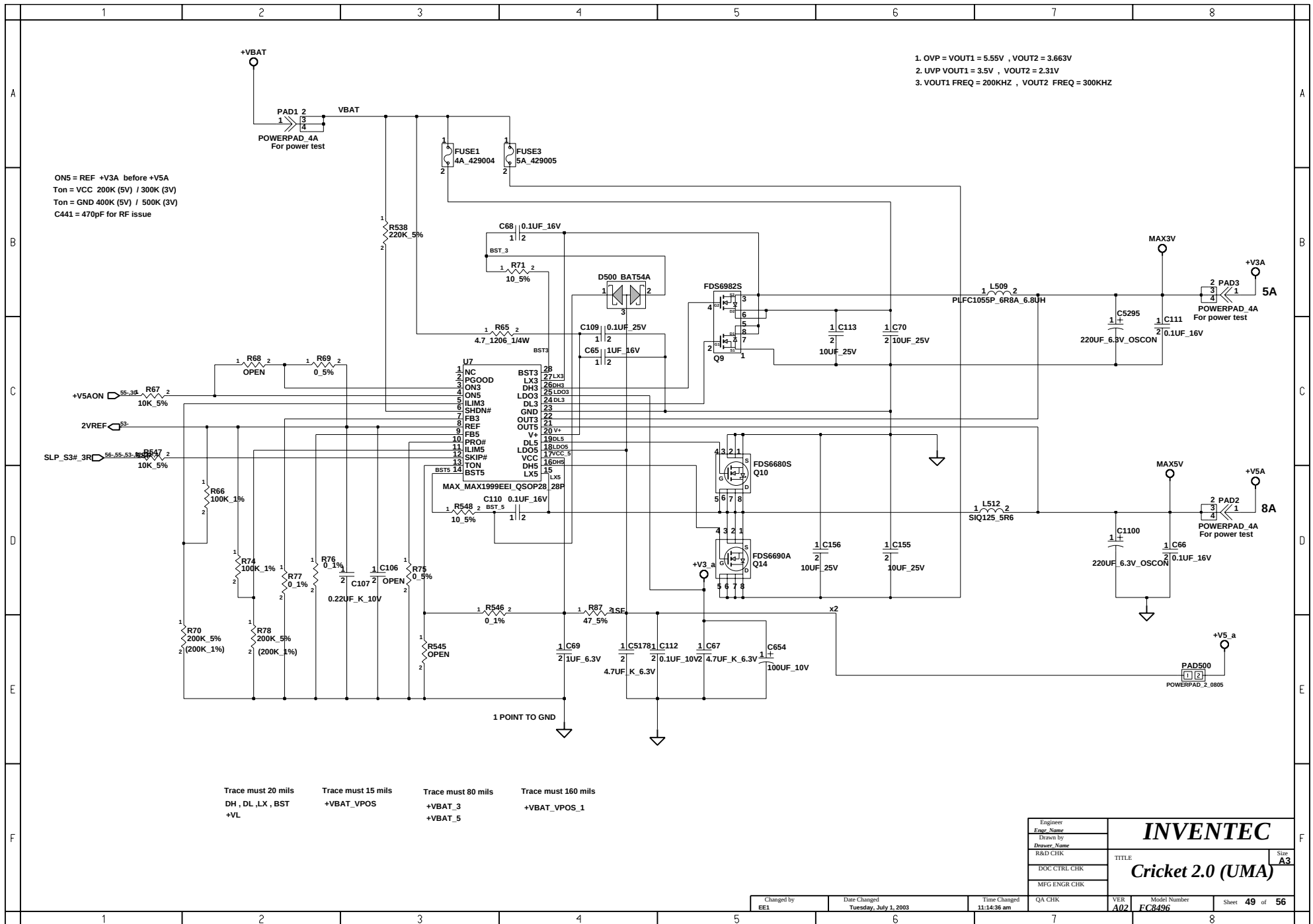
Engineer	INVENTEC TITLE: Cricket 2.0 (UMA) Drill Hole Size A3		
Drawn by			
R&D CHK			
DOC CTRL CHK			
MFG ENGR CHK	REV	Drawing Number	Sheet 45 of 56
Changed by	Date Changed	Time Changed	UA CHK

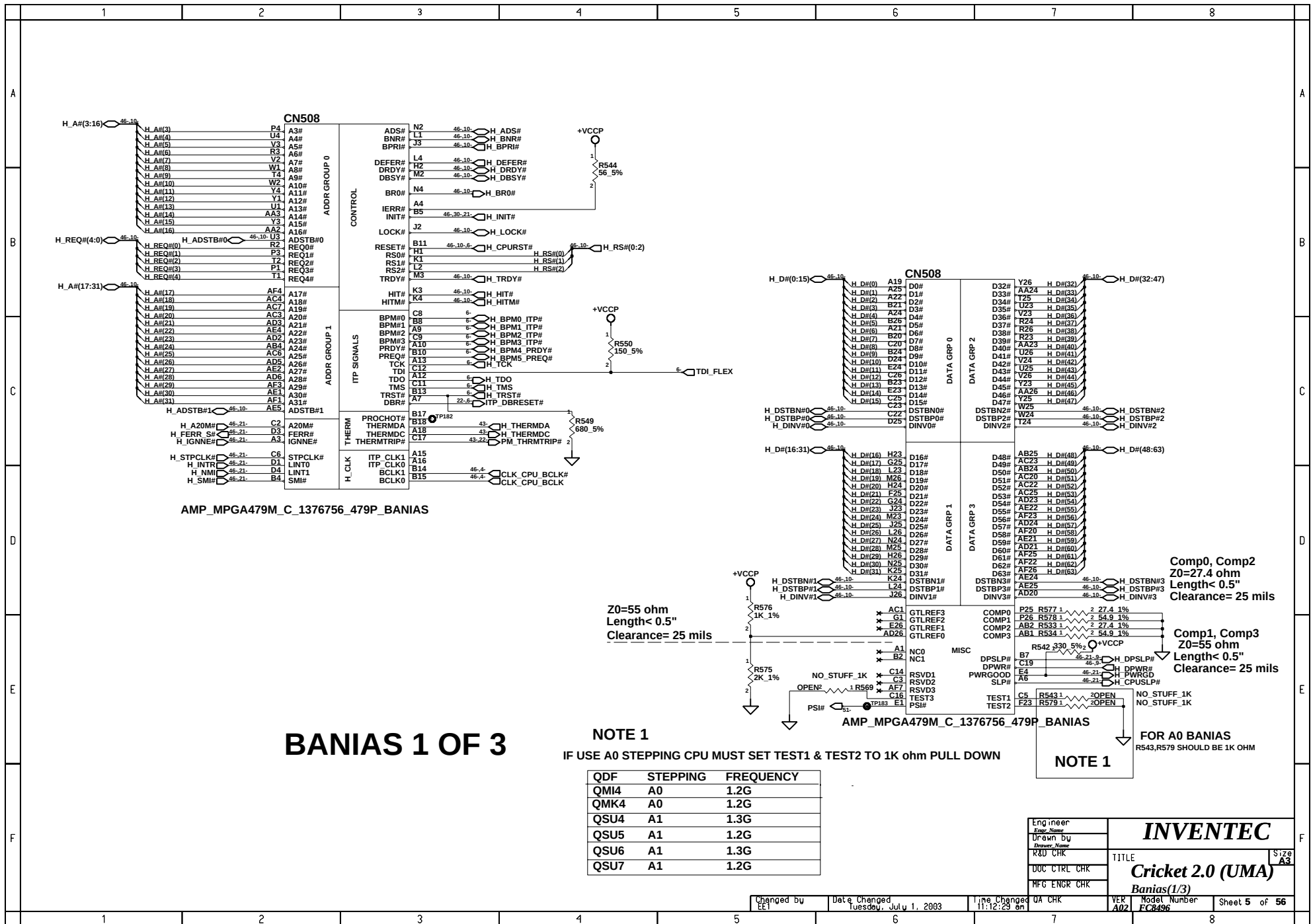
Tuesday, July 1, 2003 11:14:26 am

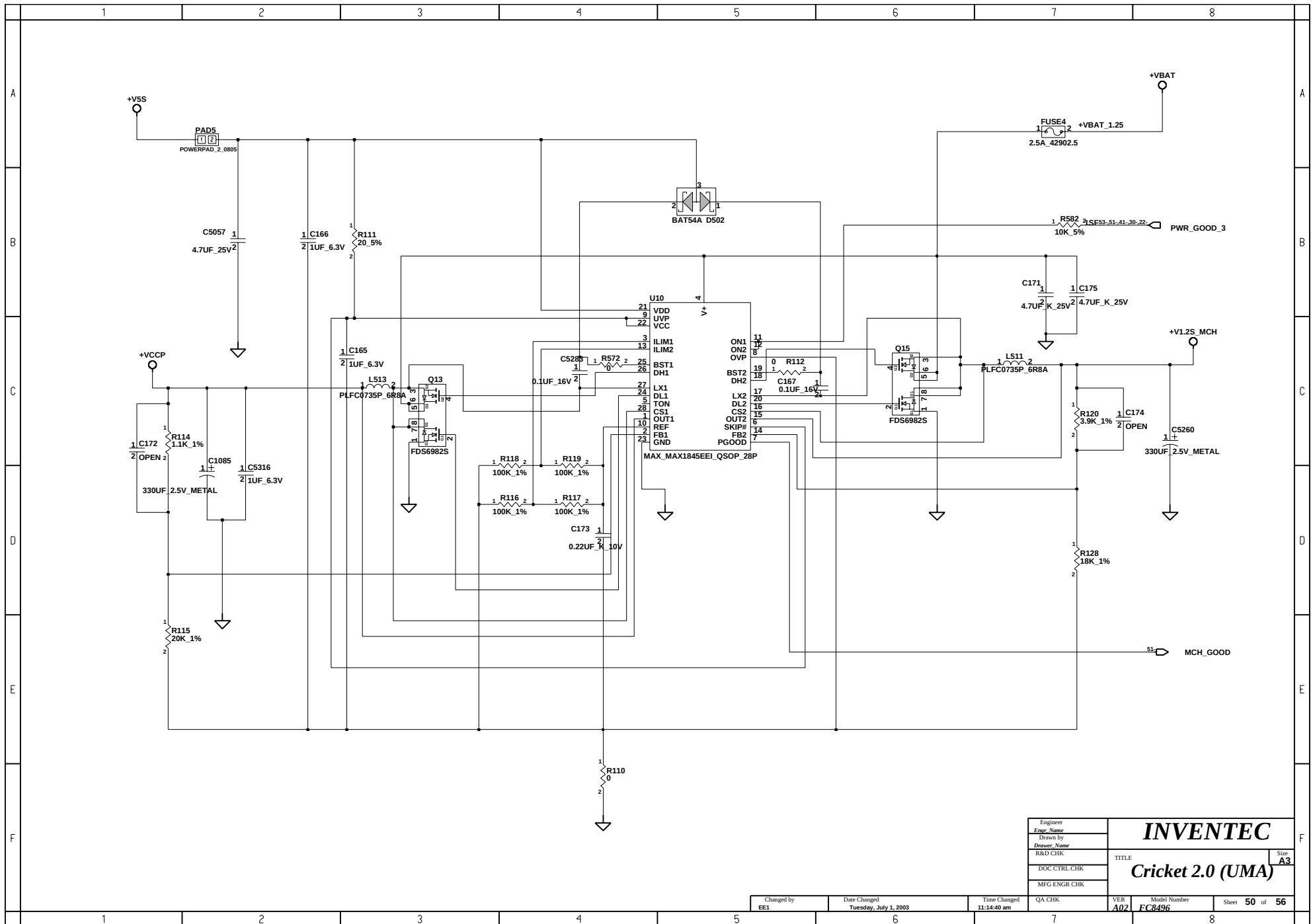




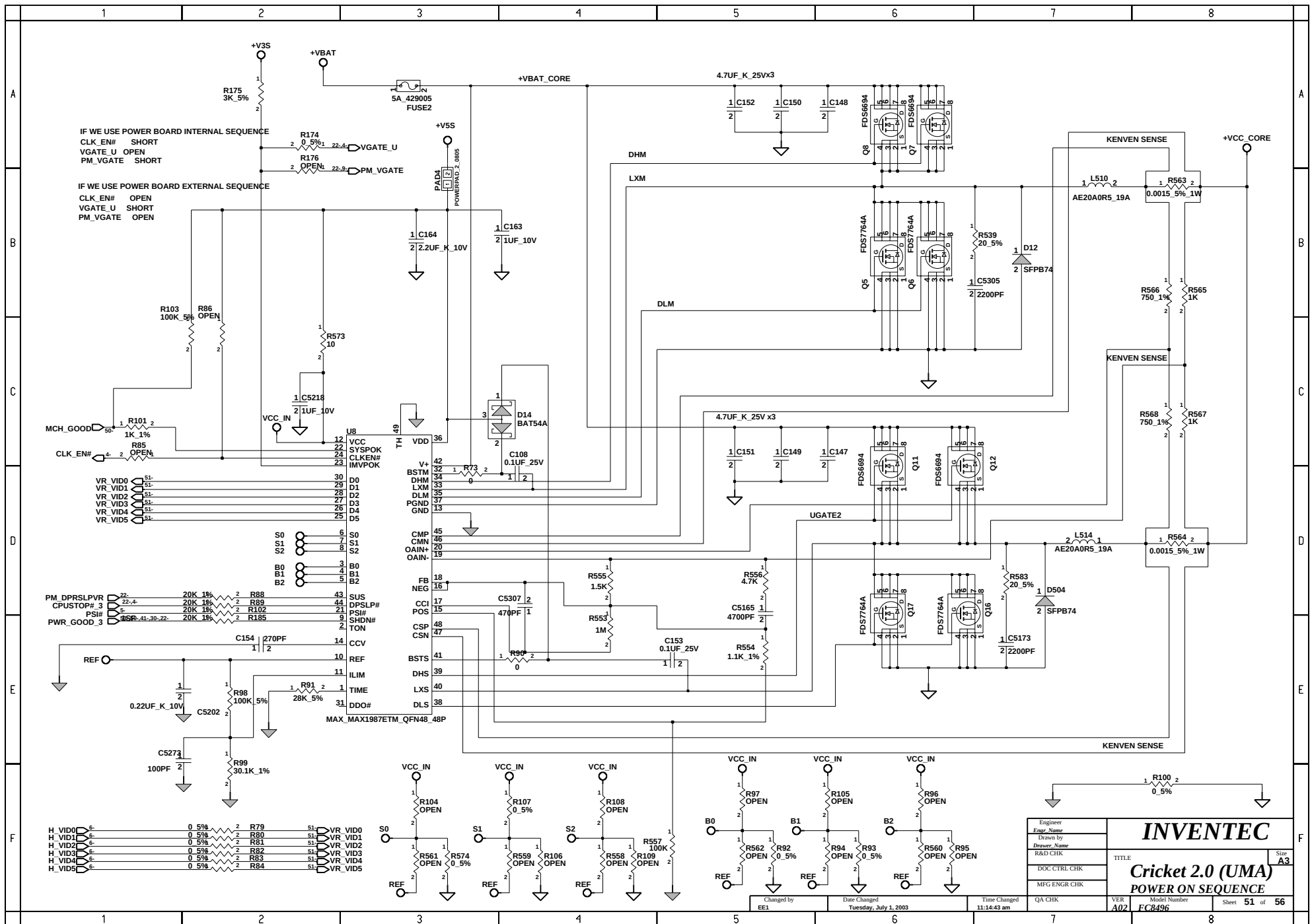
Engineer Engr. Name	INVENTEC TITLE: Cricket 2.0 (UMA) POWER (1/6)	
Drawn by Drawn. Name		
R&D CHK		
DOC CTRL CHK		
MFG ENGR CHK		
Changed by EE1	Date Changed Tuesday, July 1, 2003	Time Changed 11:14:33 am
QA CHK	VER A02	Model Number ECR496
Sheet 48 of 56		Size A3

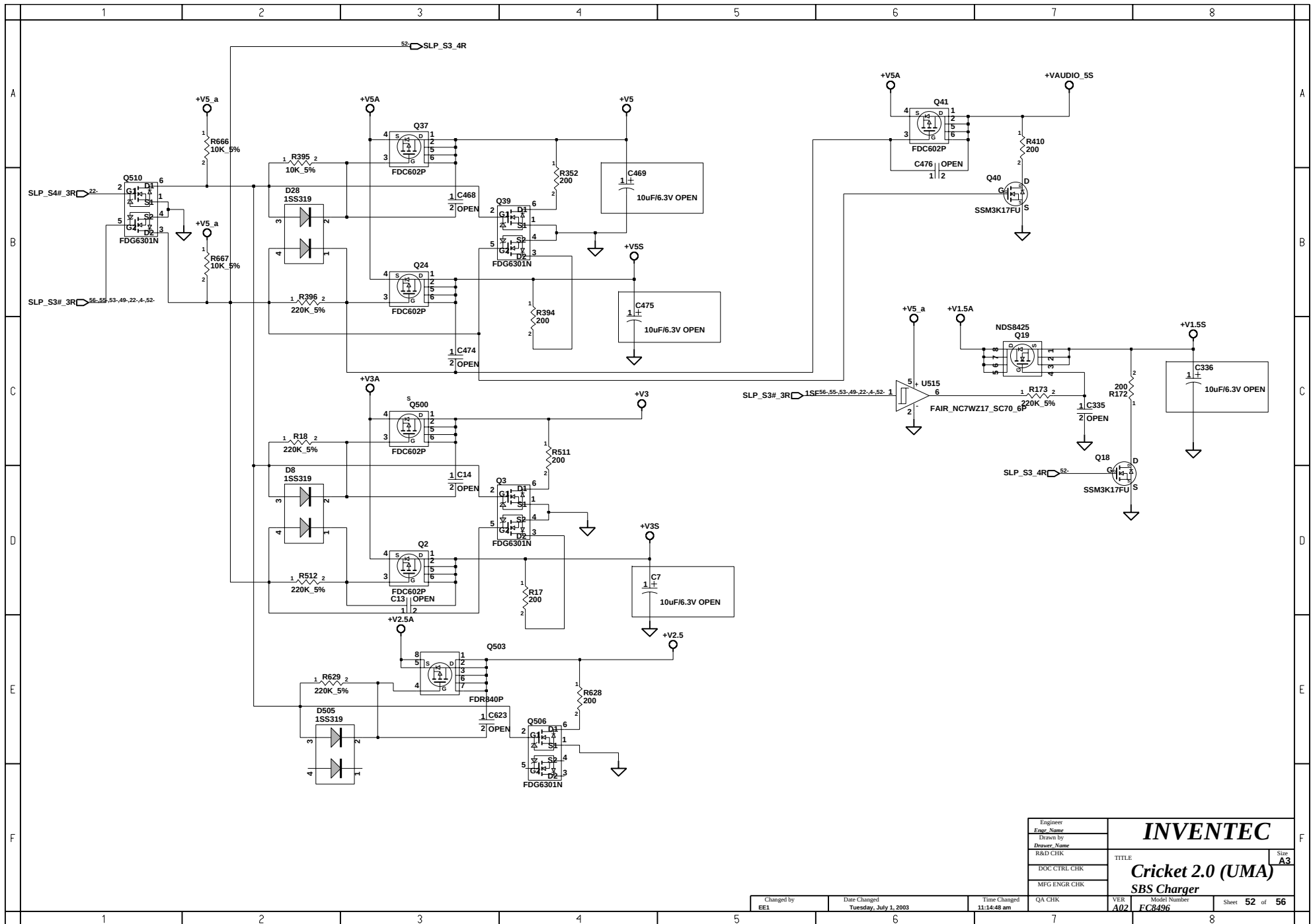






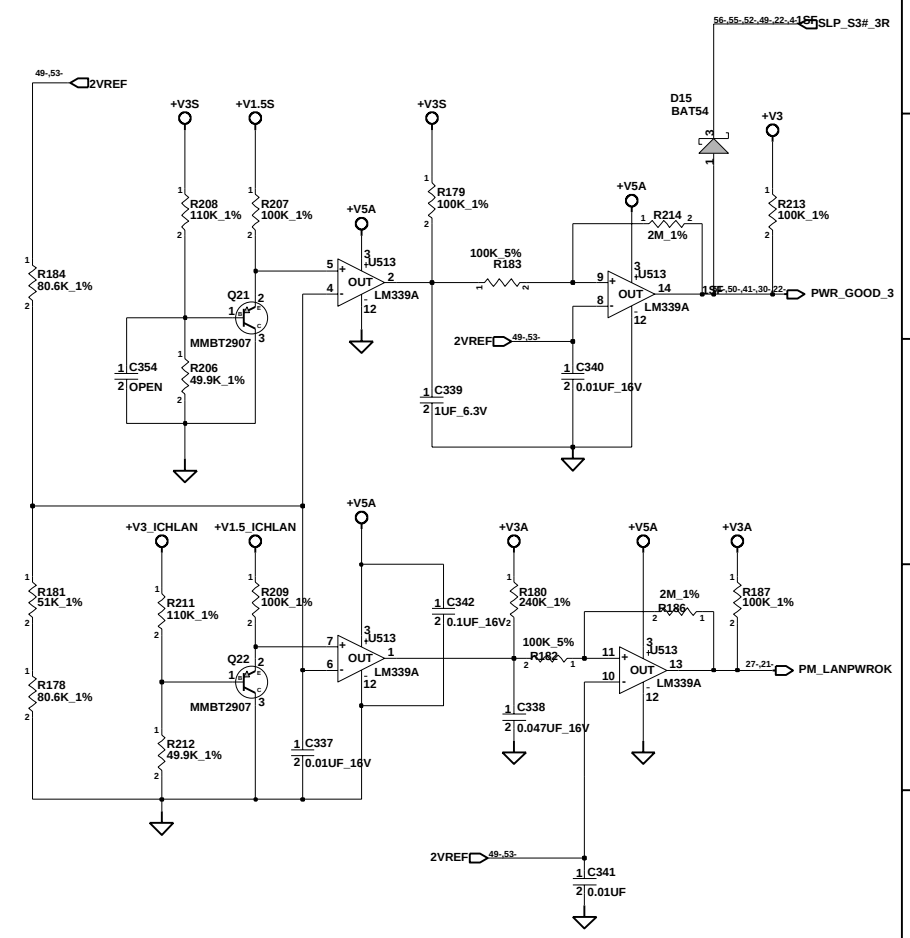
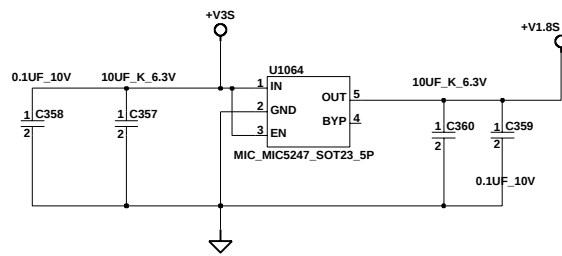
Engineer <i>Engr. Name</i>	INVENTEC TITLE: Cricket 2.0 (UMA) Size: A3		
Drawn by <i>Drawn. Name</i>			
R&D CHK			
DOC CTRL CHK			
MFG ENGR CHK			
Changed by EE1	Date Changed Tuesday, July 1, 2003	Time Changed 11:14:40 am	QA CHK VER: A02 Model Number: FCR496 Sheet: 50 of 56



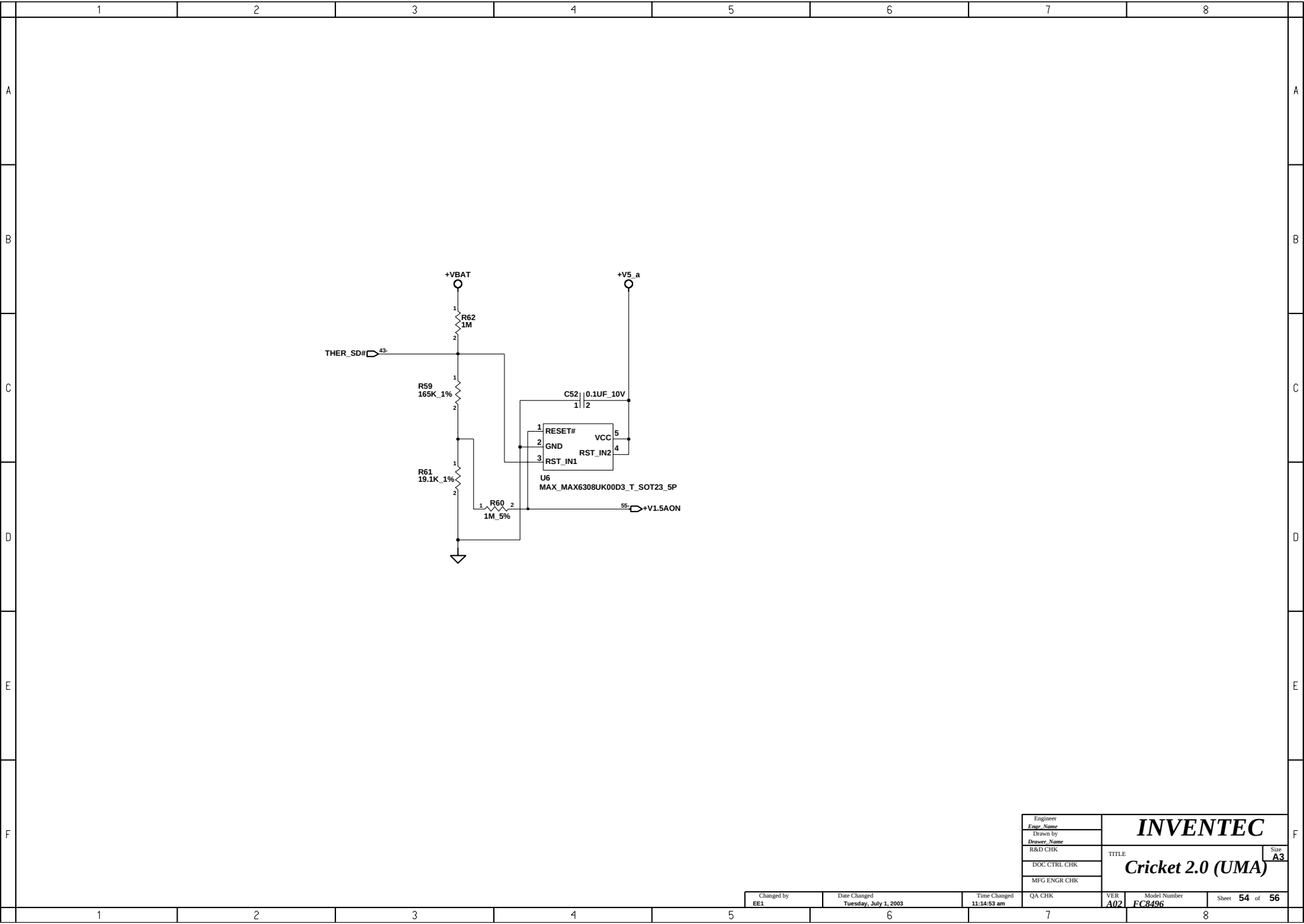


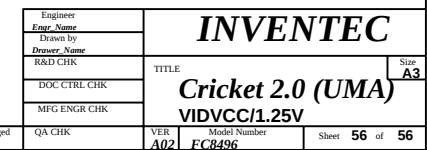
Engineer <i>Engr. Name</i>		INVENTEC TITLE Cricket 2.0 (UMA) SBS Charger			Size A3	
Drawn by <i>Drawn. Name</i>						
R&D CHK						
DOC CTRL CHK						
MFG ENGR CHK						
QA CHK		VER A02	Model Number FC8496	Sheet	52	of 56

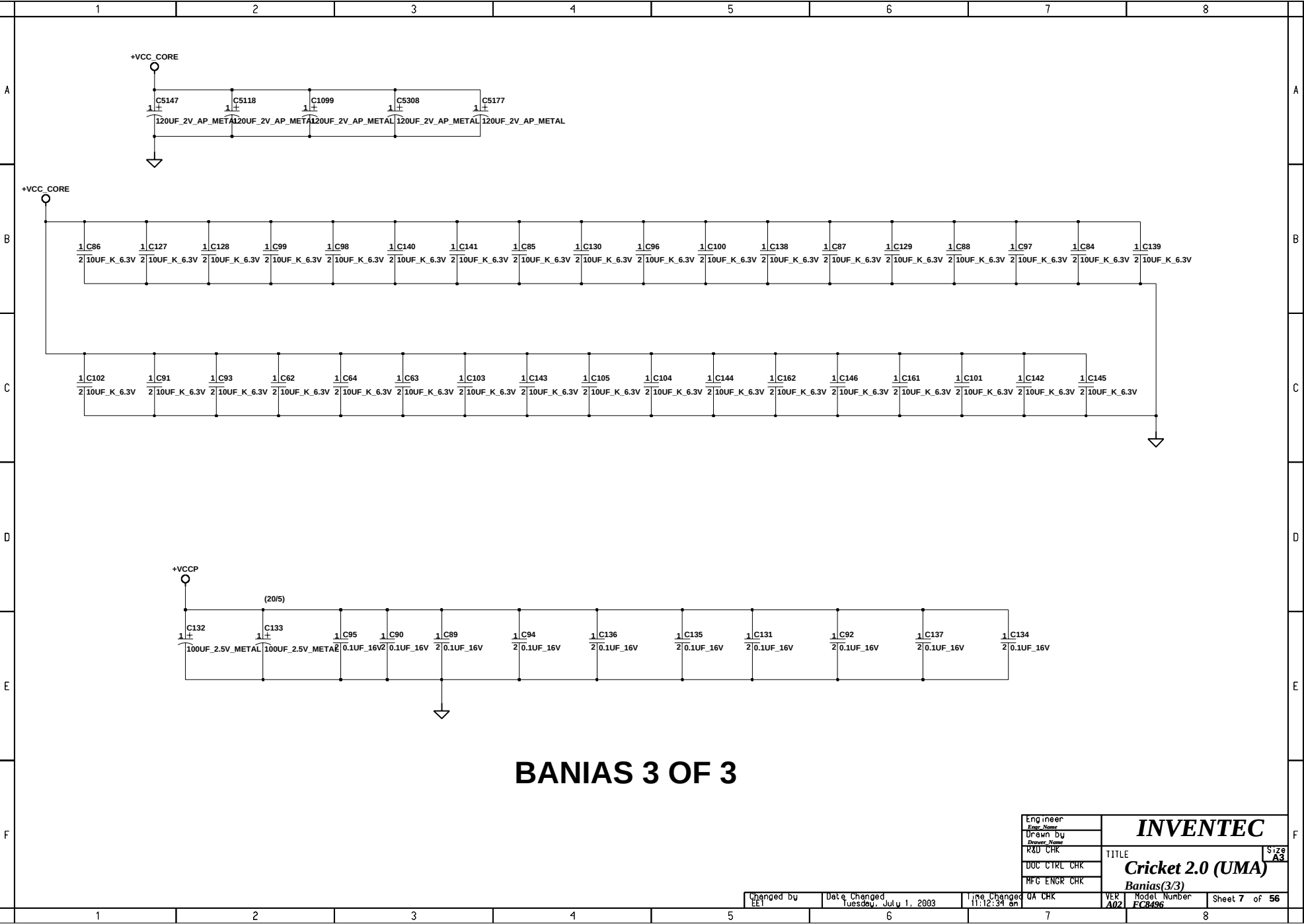
Changed by EE1	Date Changed Tuesday, July 1, 2003	Time Changed 11:14:48 am	QA CHK	VER A02	Sheet 52 of 56
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Engineer		INVENTEC TITLE: Cricket 2.0 (UMA) Size: A3
Engr_Name		
Drawn by		
Drawn_Name		
R&D CHK		
DOC CTRL CHK		
MFG ENGR CHK		
QA CHK	VER A02	Model Number FCB496
Changed by EE1	Date Changed Tuesday, July 1, 2003	Time Changed 11:14:51 am
Sheet 53 of 56		



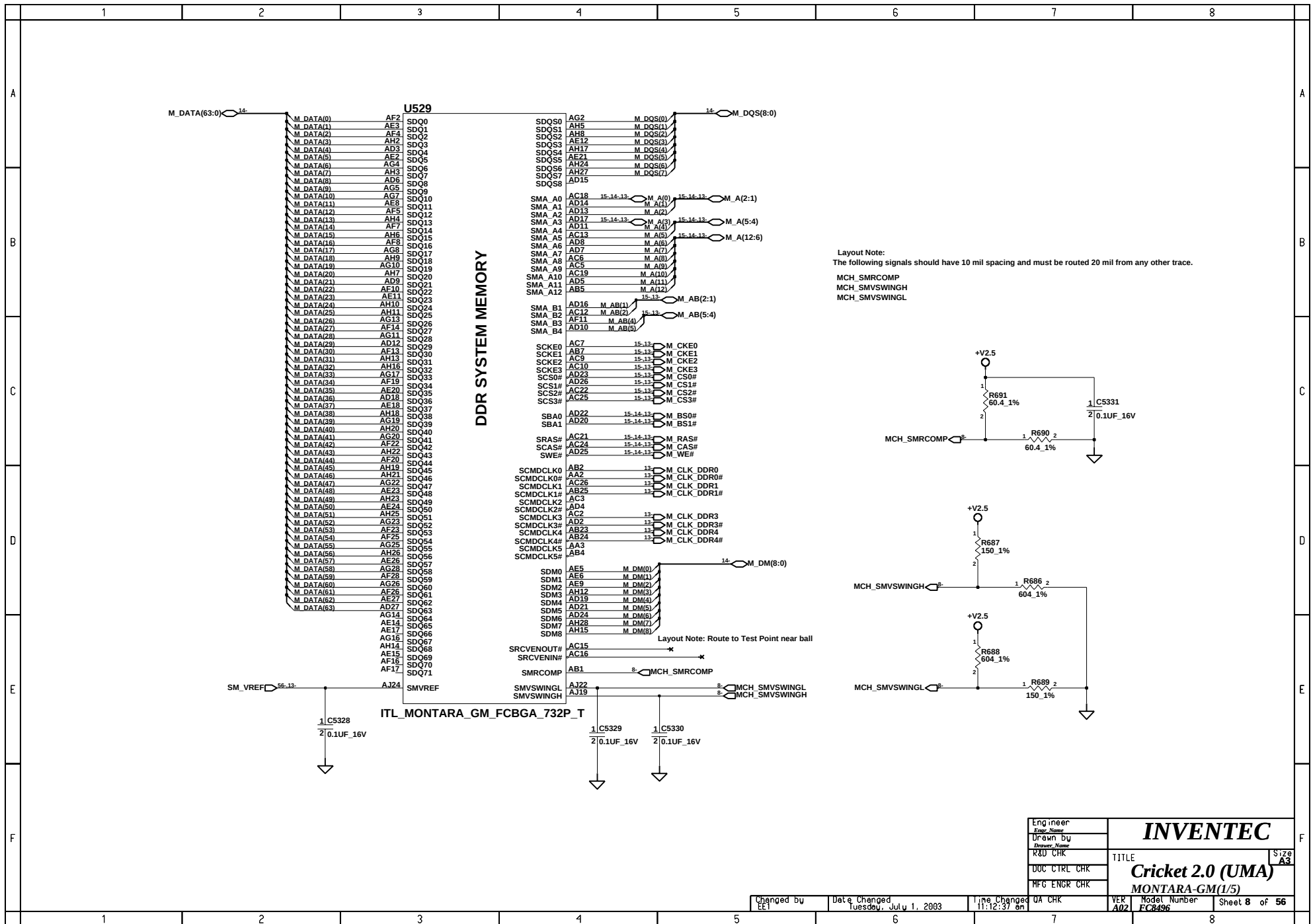




BANIAS 3 OF 3

Engineer	INVENTEC		
Drawn By			
Checker			
QA CHK			
DOC CTRL CHK			
MFG ENGR CHK	TITLE Cricket 2.0 (UMA) Banias(3/3)		
VER			
Model Number	Sheet 7 of 56		
ECR496			

Changed by	Date Changed	Time Changed
EE1	Tuesday, July 1, 2003	11:12:34 am



Engineer		INVENTEC TITLE Cricket 2.0 (UMA) MONTARA-GM(1/5)	S/28 A3
Drawn by			
Checker			
DOE CTRL CHK			
MFG ENGR CHK			
Changed by	EE1	Date Changed	Tuesday, July 1, 2003
Time Changed	11:12:37 am	UA CHK	
VER	A02	Model Number	FCB496
Sheet 8	of 56		

