

Compal Confidential

HTW00 LA-2871 Schematics Document

Intel Dothan with 915PM(GM)/910GML + DDRII + ICH6M

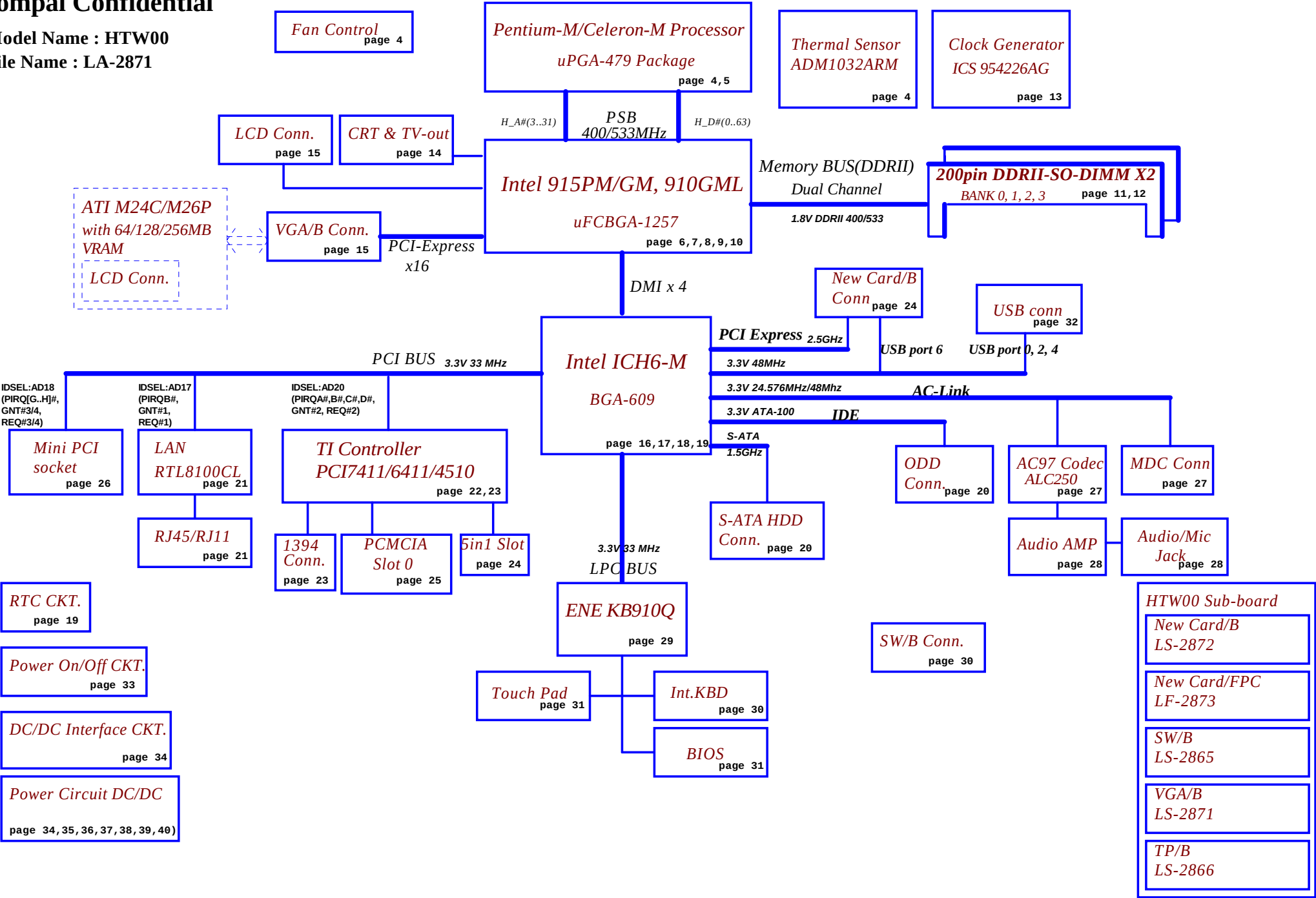
2005-08-22

REV: 1.0

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Model Name : HTW00
File Name : LA-2871



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
1394	D0	AD20	2	A,B,C,D
LAN	D1	AD17	3	F
CARD BUS	D4	AD20	2	A,B,C,D
5IN1	D4	AD20	2	A,B,C,D
Mini-PCI	D2	AD18	1	G,H

KB910 I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
SM1 24C16	A0H	1 0 1 0 0 0 0 X b
SM1 SMART BATTERY	16H	0 0 0 1 0 1 1 X b
SM2 ADM0132 CPU THERMAL MONITOR	98H	1 0 0 1 1 0 0 X b
SM2 GMT G781-1 VGA THERMAL MONITOR	9AH	1 0 0 1 1 0 1 X b

ICH6M SM Bus address

Device	Address
Clock Generator (ICS 954226)	1101 001Xb
DDRII DIMM0	1001 000Xb
DDRII DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

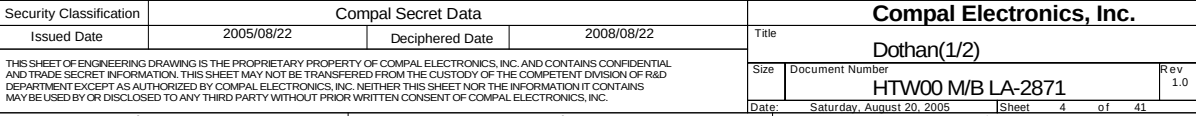
SKU ID Table

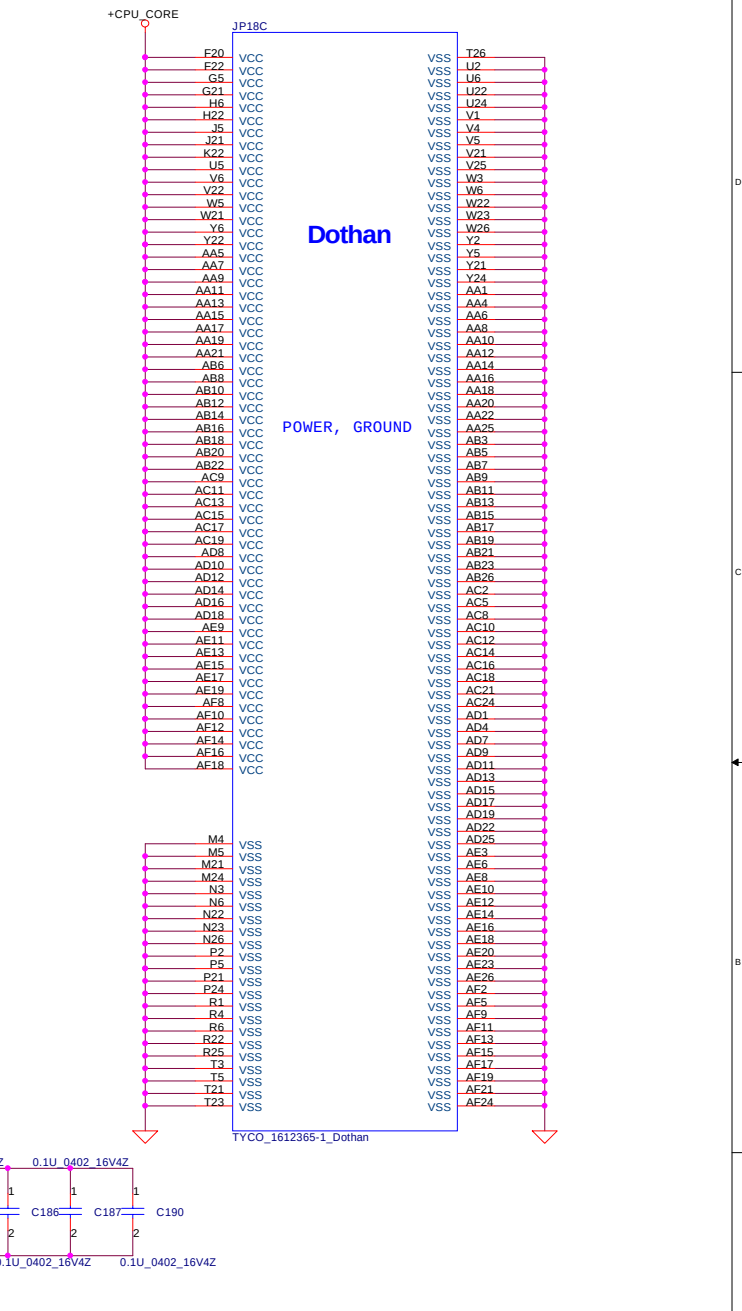
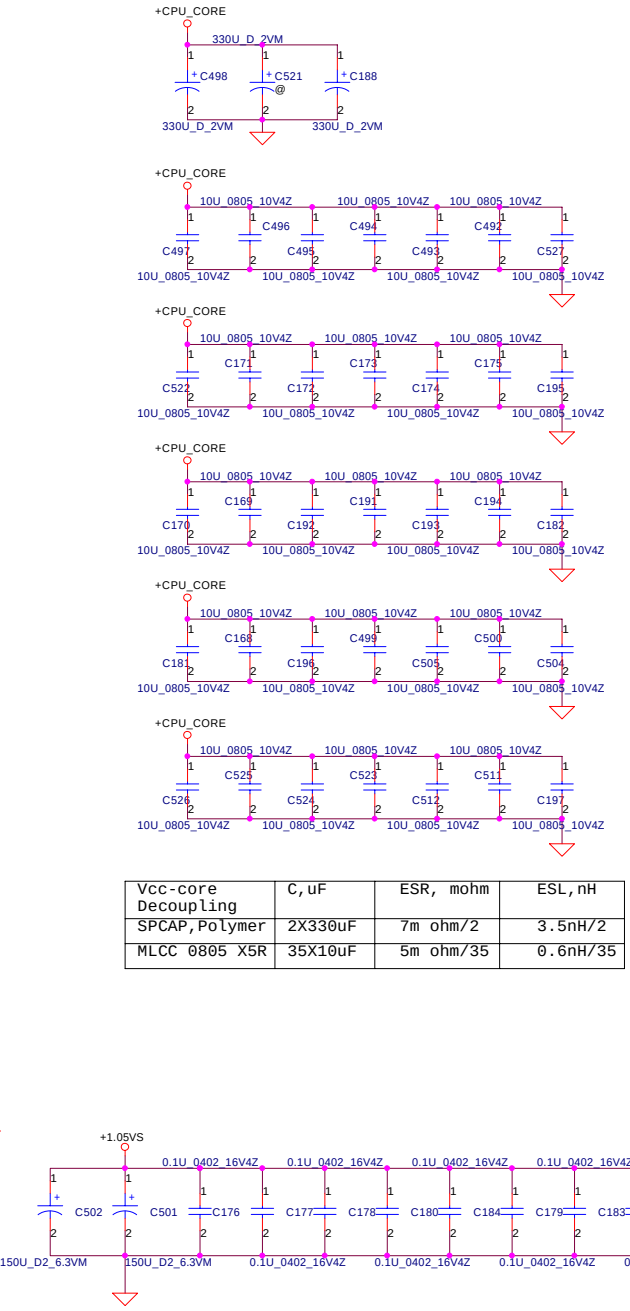
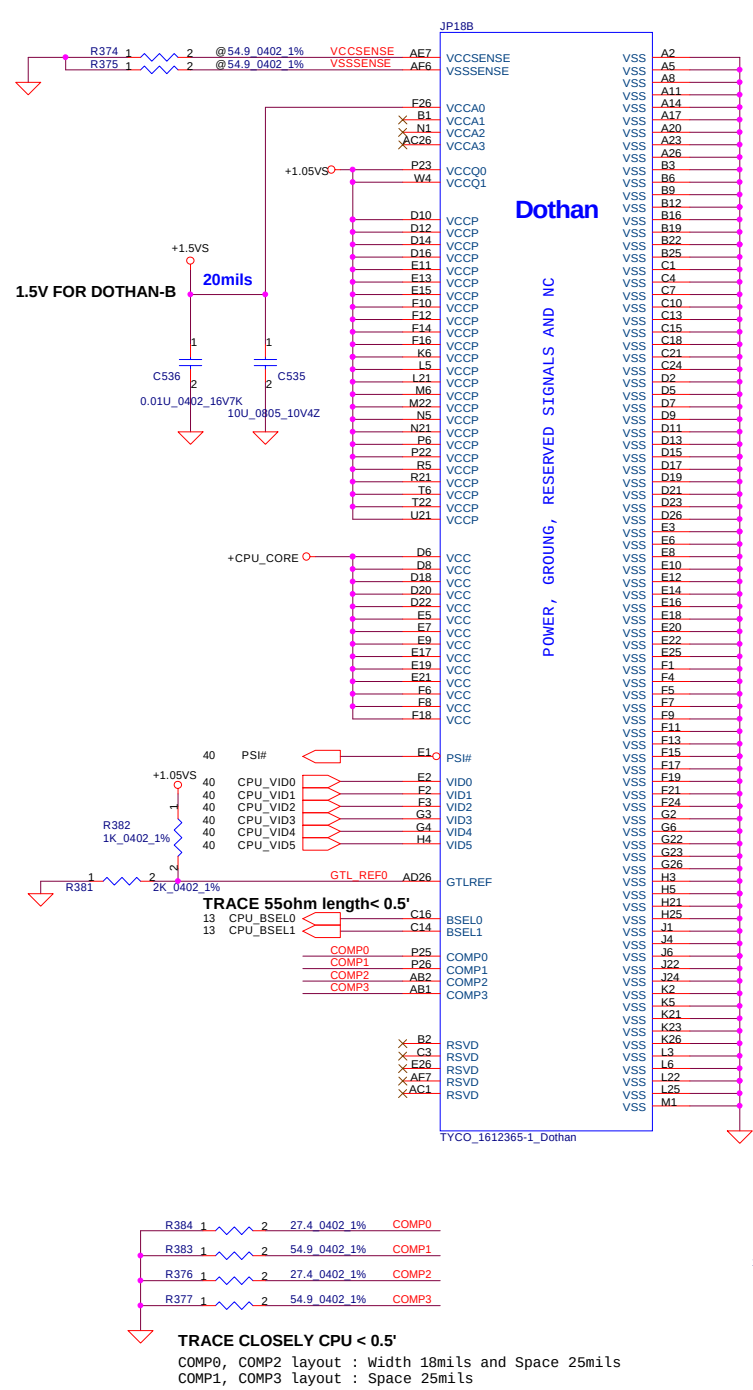
SKU ID	SKU
0	
1	
2	
3	
4	
5	
6	
7	

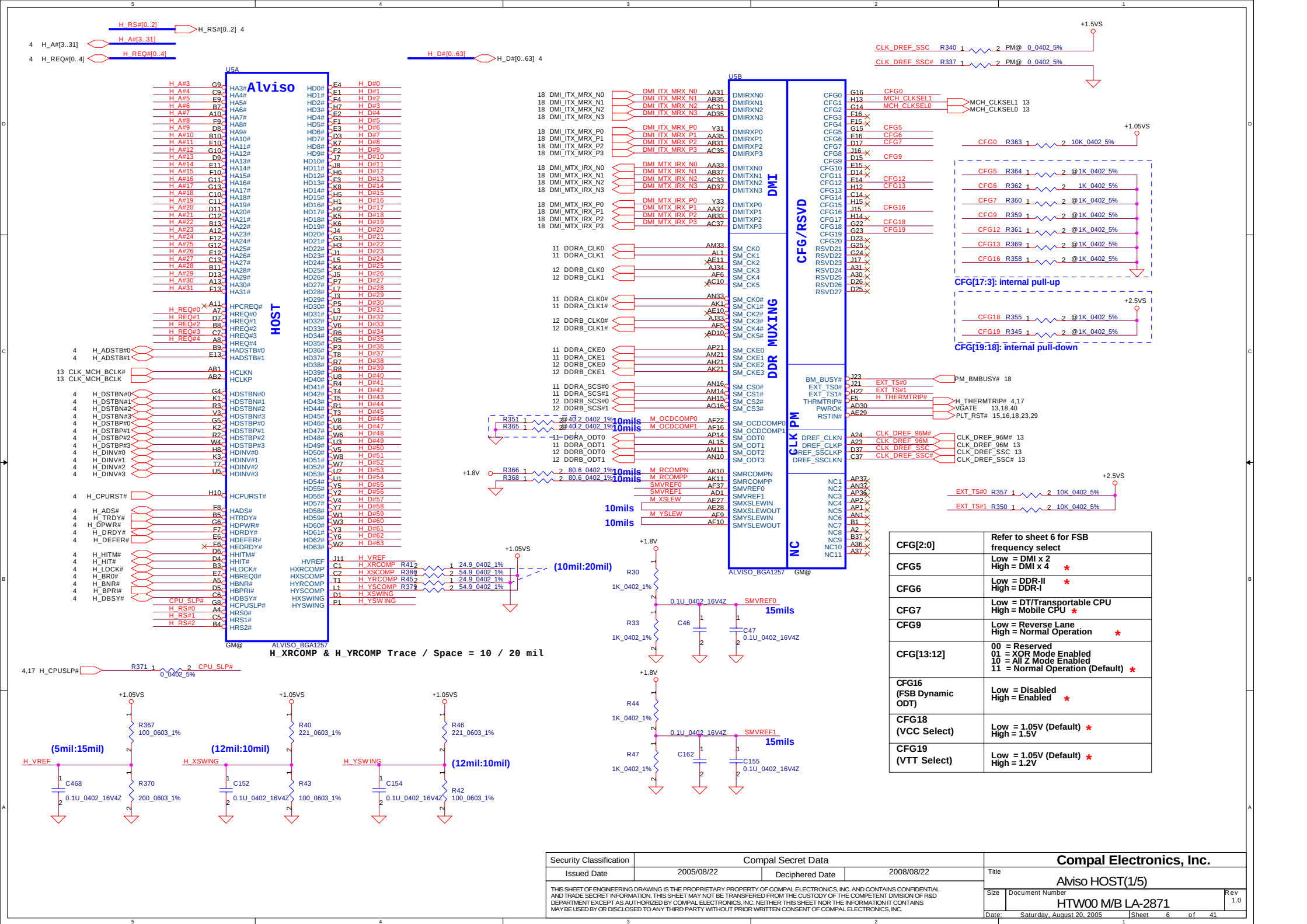
BTO Option Table

BTO Item	BOM Structure
VGA	6M@
Card Reader	5IN1@
Giga LAN	8100C@ 8110S@
New Card	NEWCARD@
IEEE1394	1394@
TV Tuner	TUNER@
INT MIC.	MIC@
KILL SW	WLAN@
CIR	CIR@
HWEQ	EQ@ NOEQ@

(TBD)

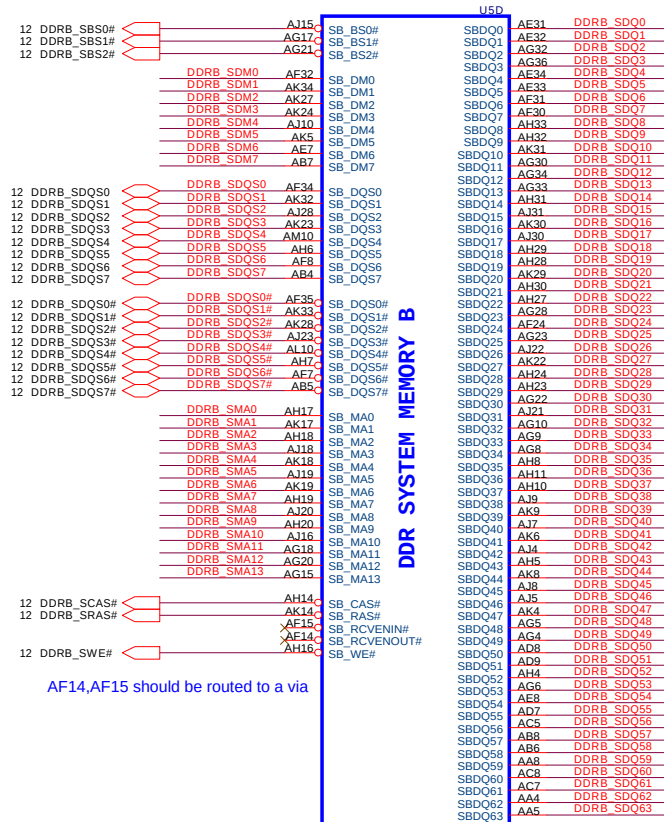
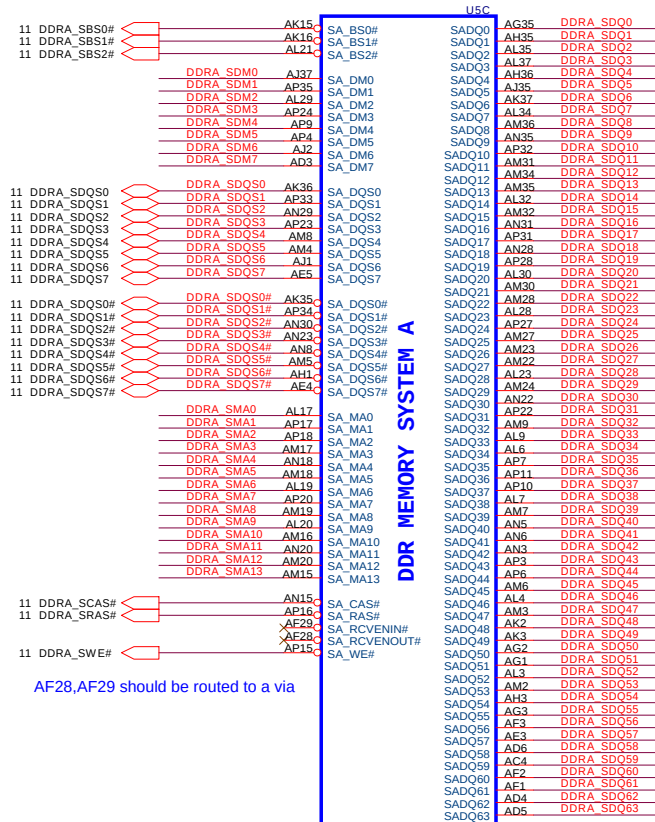


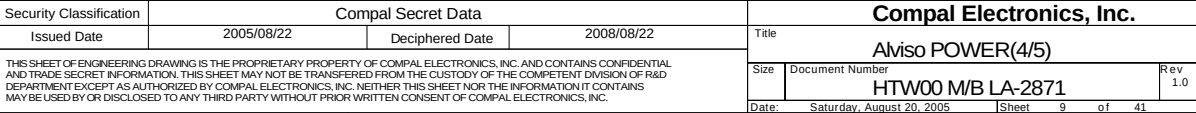


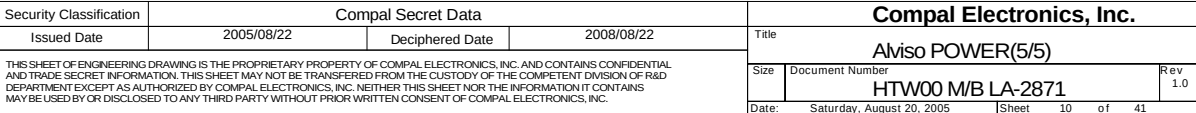


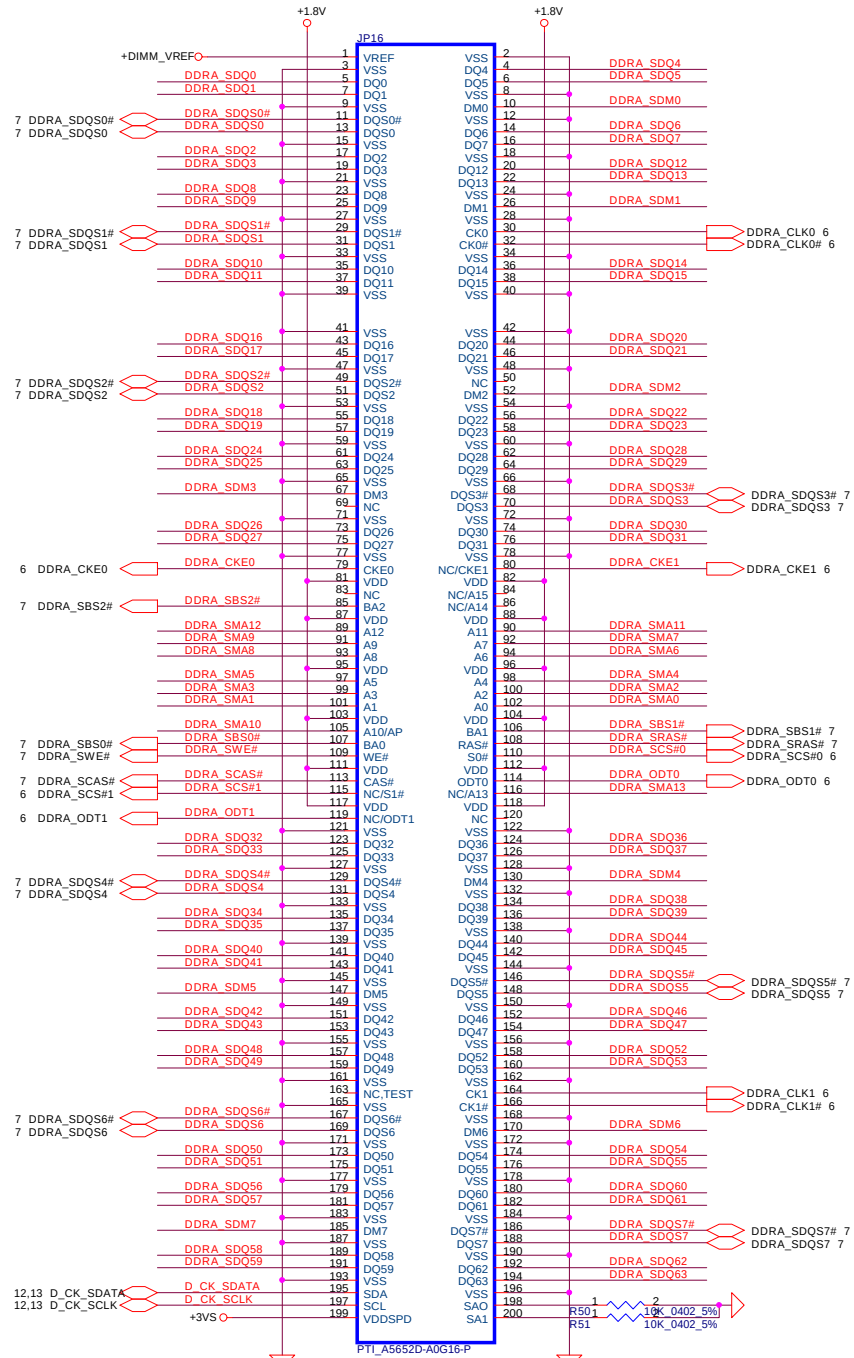
11 DDRA_SDQ[0..63]  DDRA_SDQ[0..63]
11 DDRA_SDM[0..7]  DDRA_SDM[0..7]
11 DDRA_SMA[0..13]  DDRA_SMA[0..13]

12 DDRB_SDQ[0..63]  DDRB_SDQ[0..63]
12 DDRB_SDM[0..7]  DDRB_SDM[0..7]
12 DDRB_SMA[0..13]  DDRB_SMA[0..13]

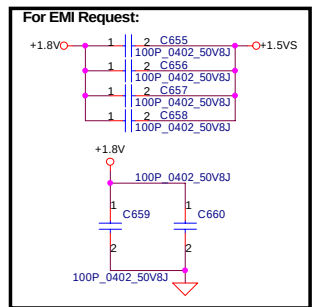
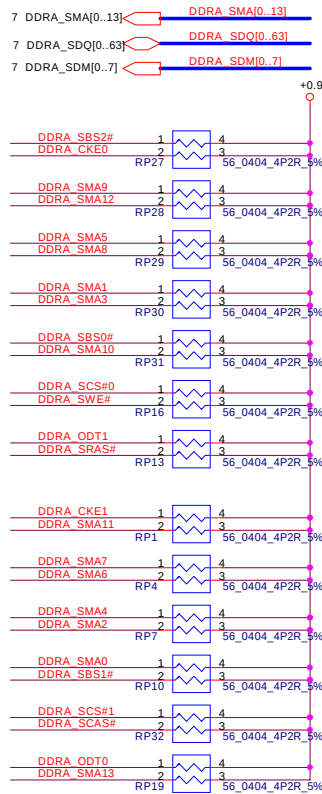
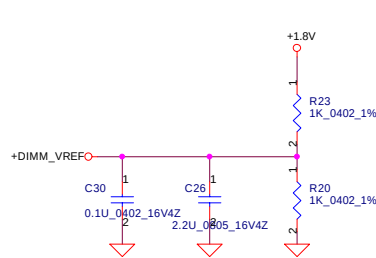




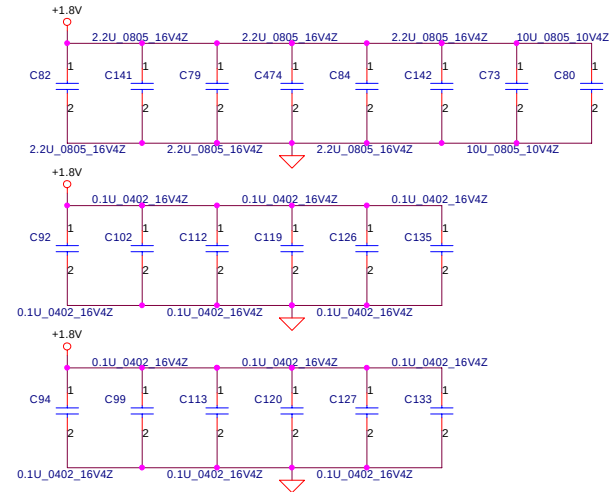




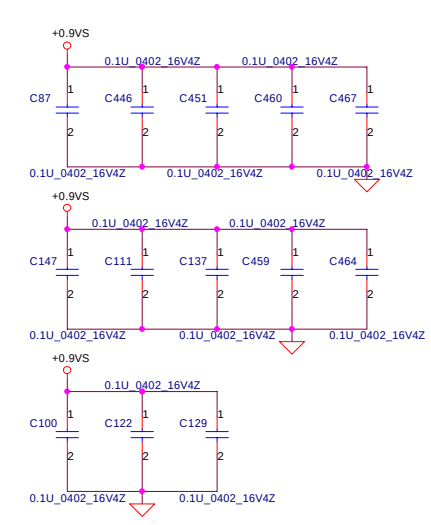
DIMM0 STD H:5.2mm (BOT)



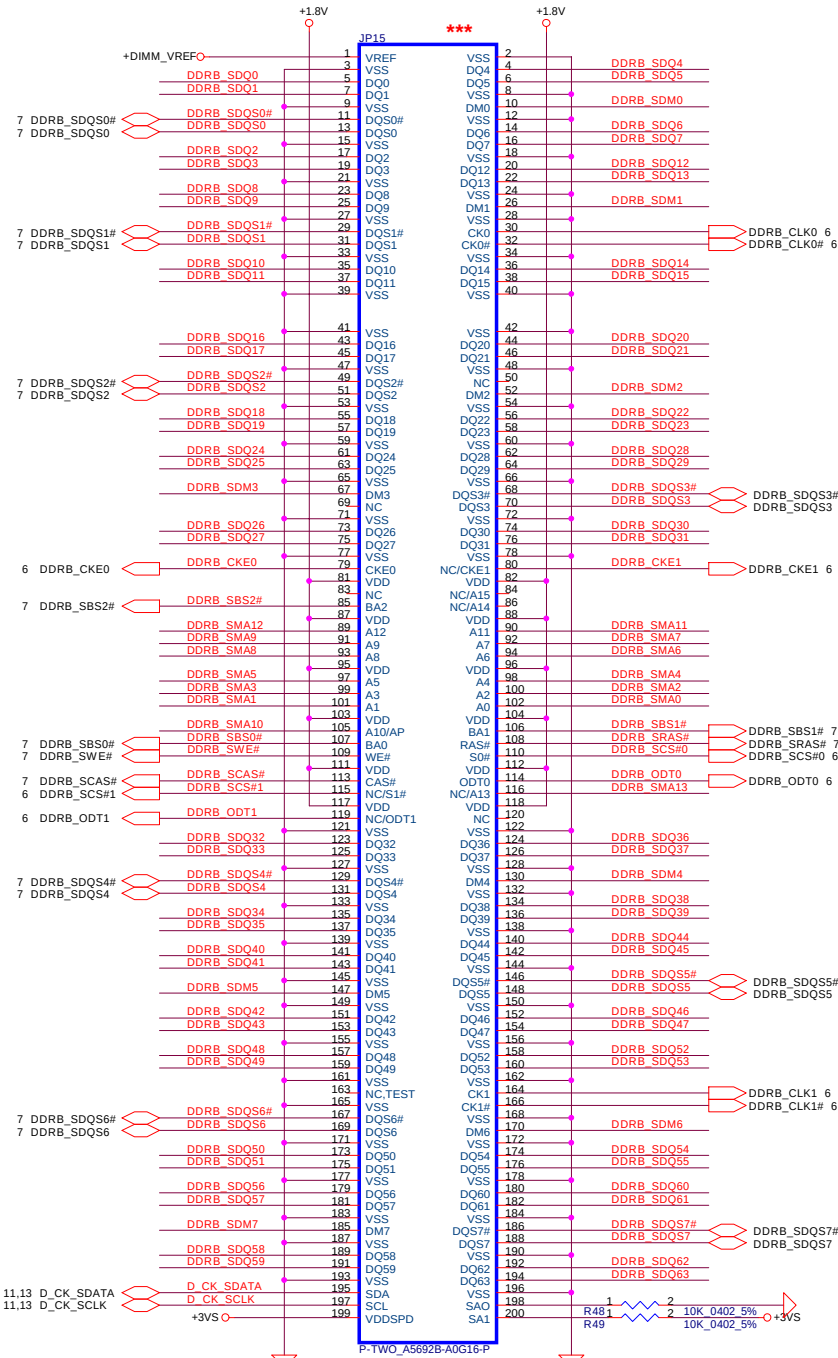
Layout note : Place one 0.1u cap close to every DDR-SODIMM pin
one 2.2u cap close to every 2.0 0.1u cap



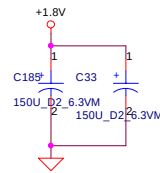
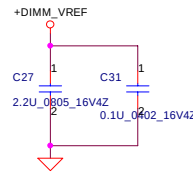
Layout note :
Place one cap close to every 2 pull up resistors termination to +0.9VS



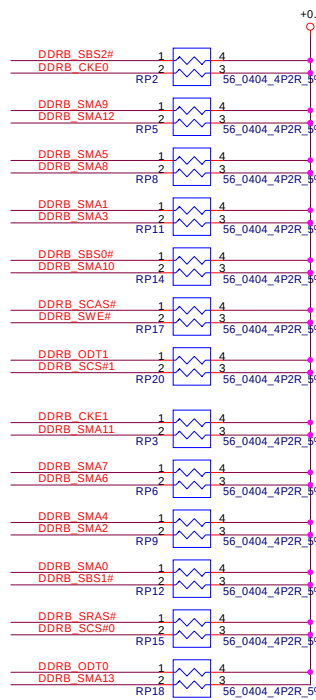
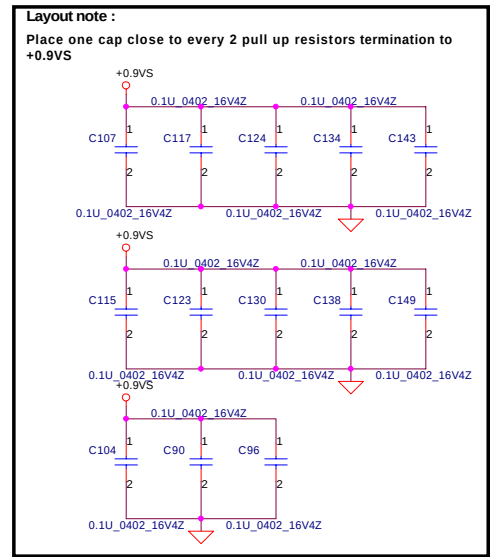
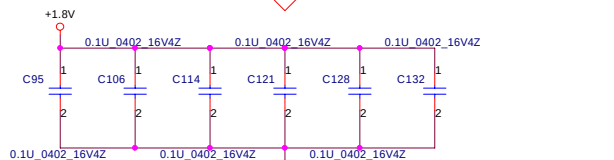
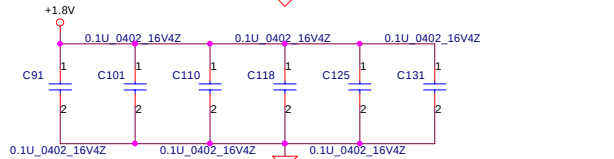
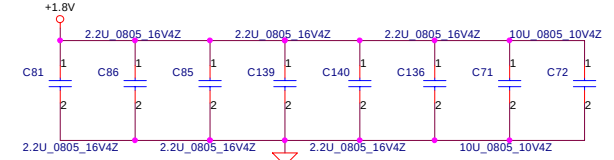
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DIMM1 STD H:9.2mm (BOT)

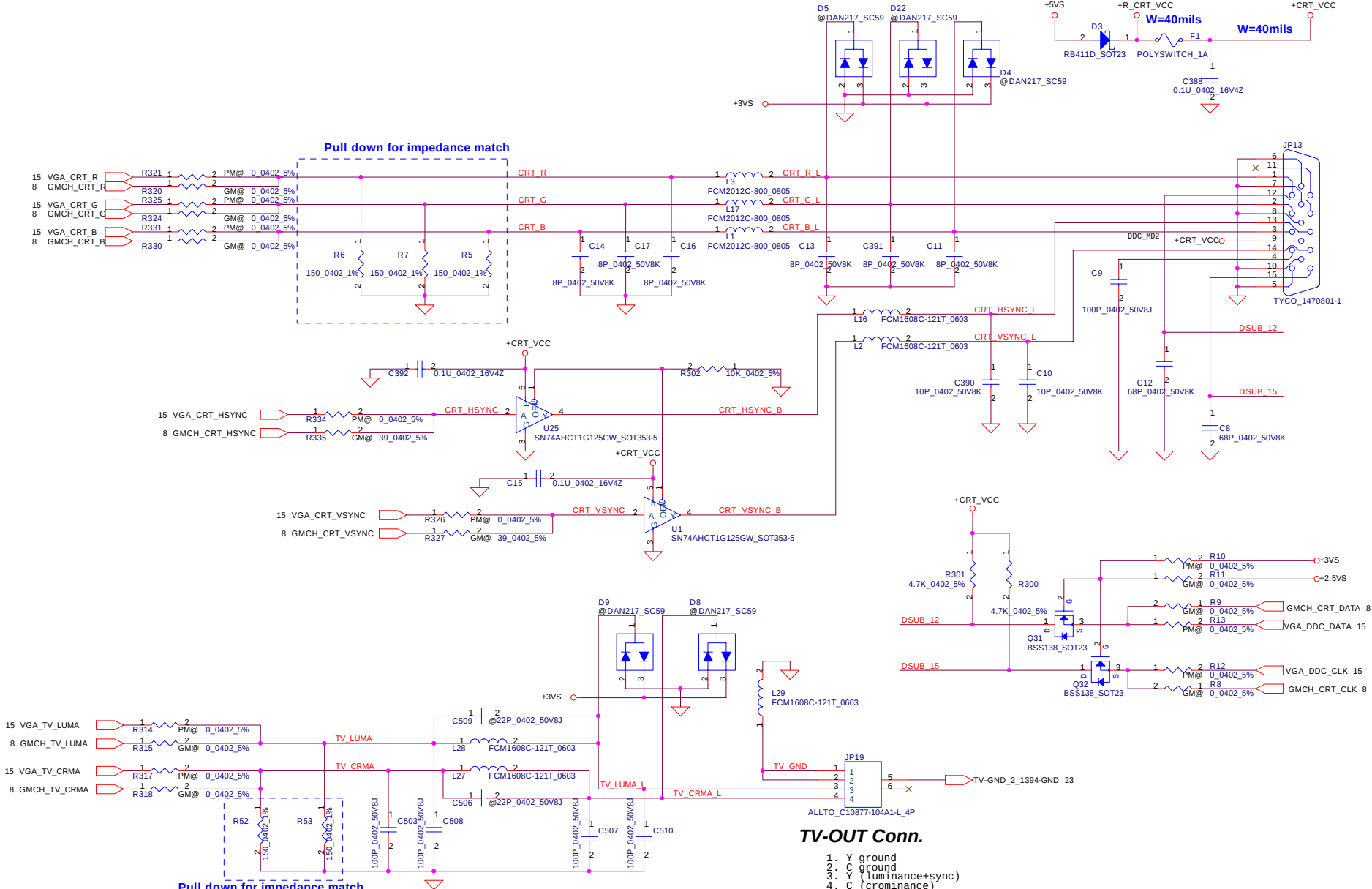


Layout note : Place one 0.1u cap close to every DDR-SODIMM pin
one 2.2u cap close to every 2 0.1u cap



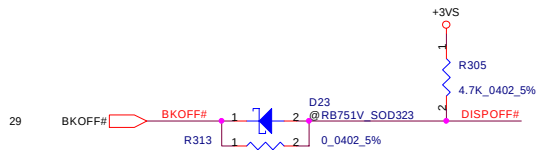
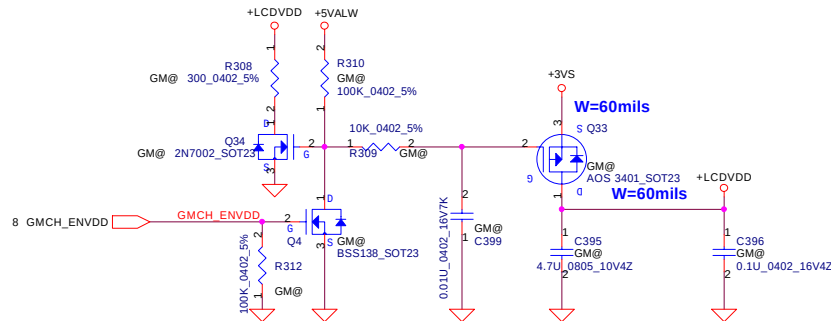
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CRT Connector

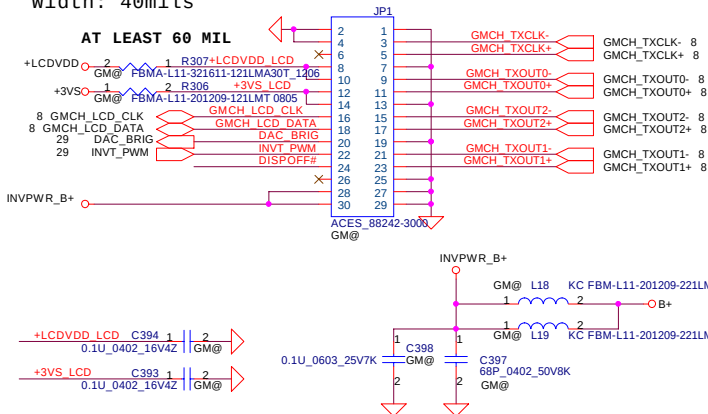


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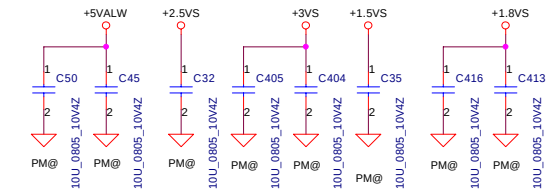
LCD POWER CIRCUIT



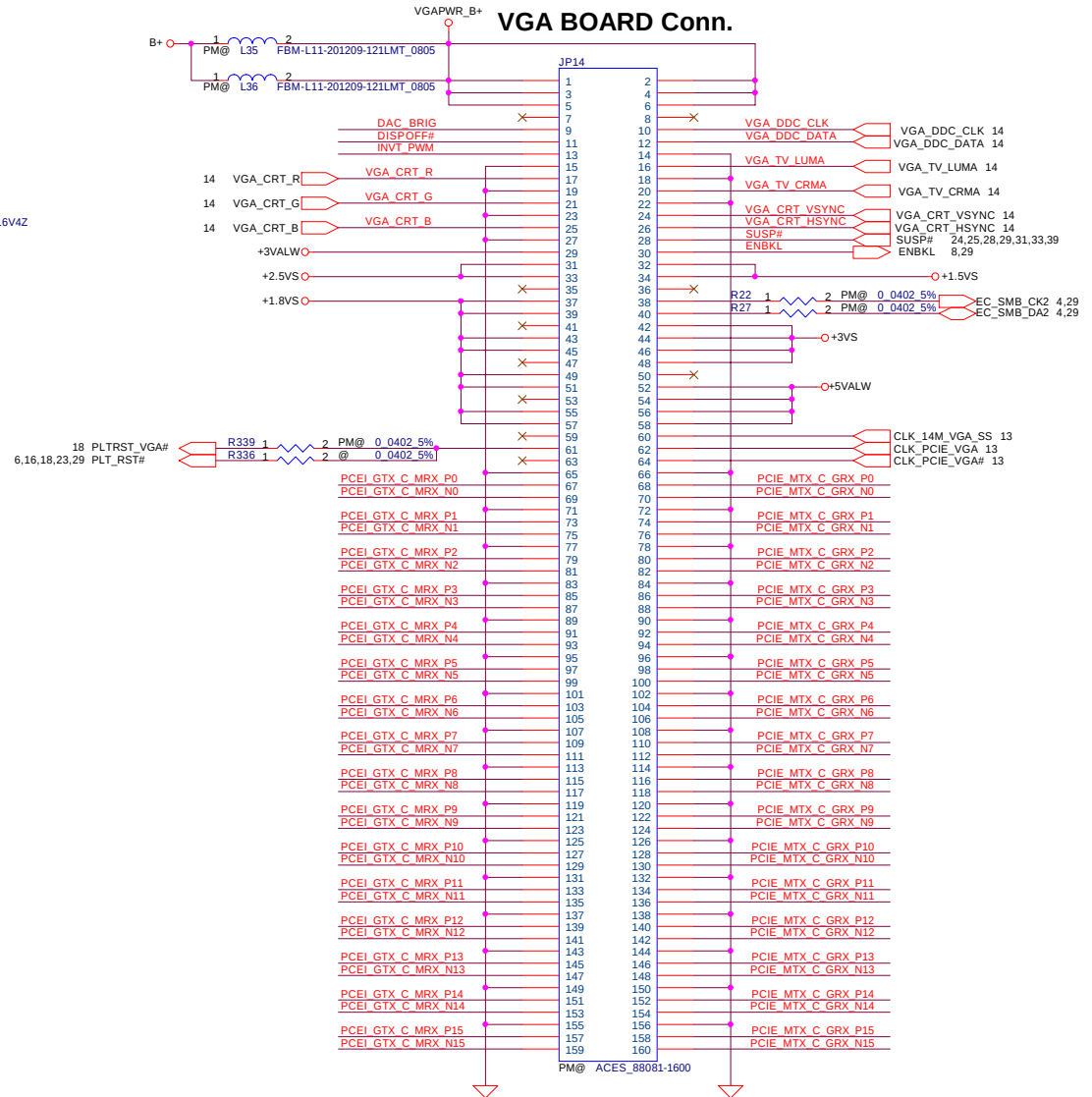
Width: 40mils



8 PCEI GTX_C_MRX_N[0..15] PCEI GTX_C_MRX N0..15
8 PCEI GTX_C_MRX_P[0..15] PCEI GTX_C_MRX P0..15
8 PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX N0..15
8 PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX P0..15

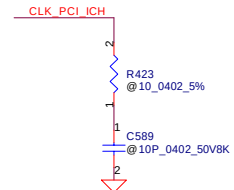
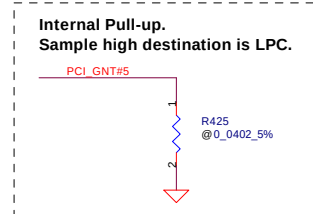
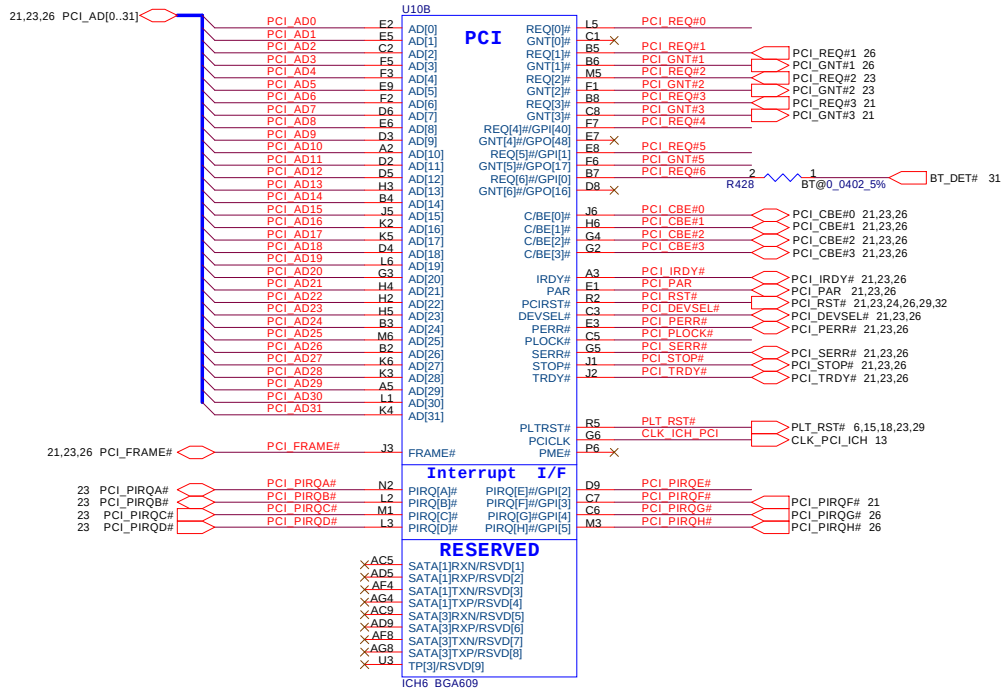
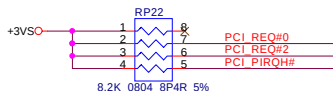
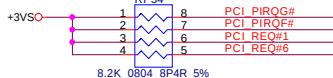
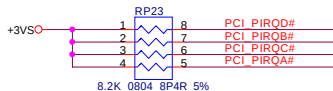
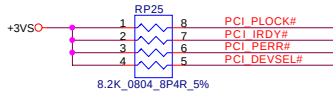
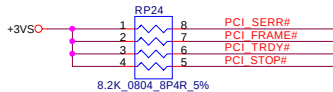


VGA BOARD Conn.



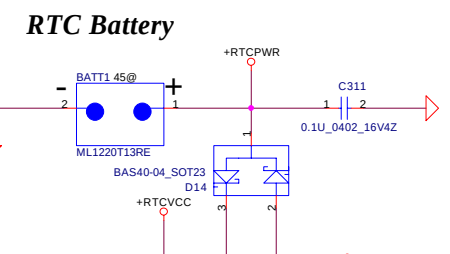
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2008/08/22		2008/08/22		VGA / LCD CONN.	
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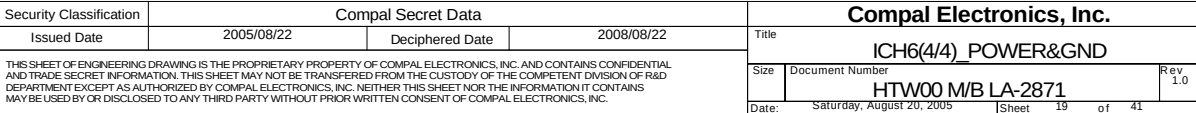


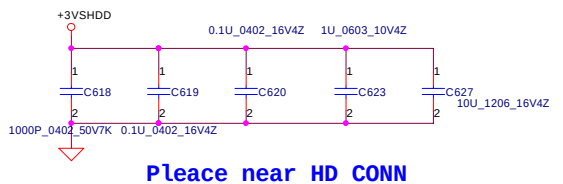
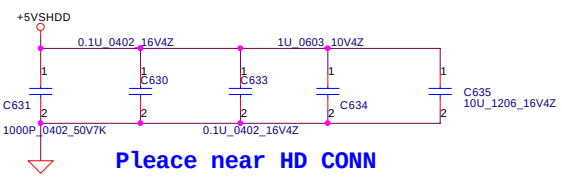
ICH6-M
(R3:SA828010890)
(R1:SA8280108B0)

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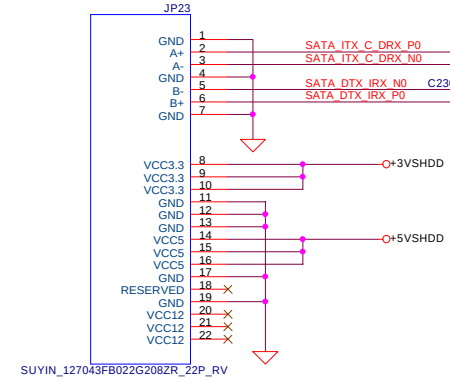


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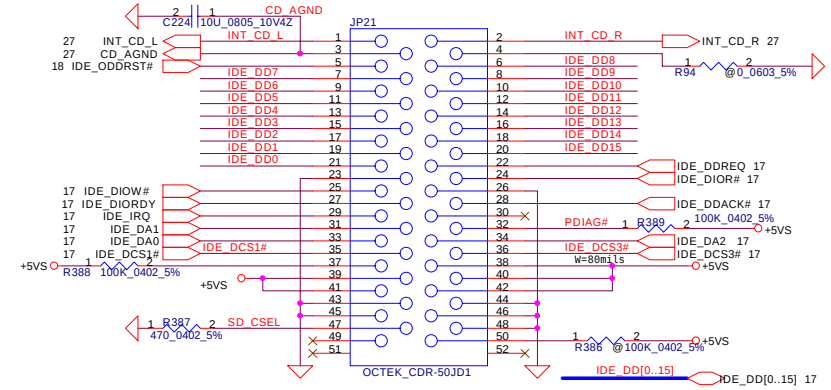




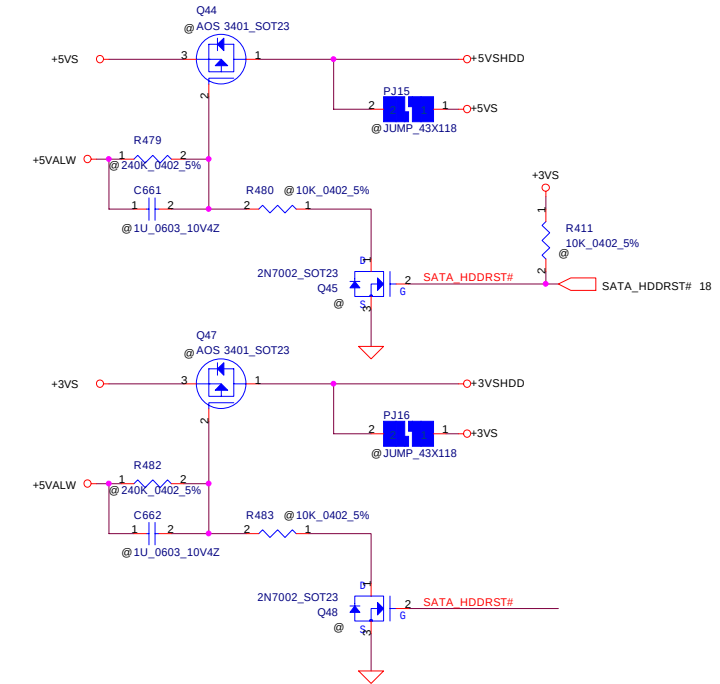
S-ATA HDD Conn.



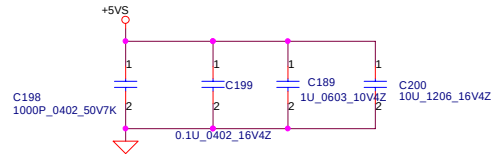
CDROM CONN



Reserve for SATA HDD RESET

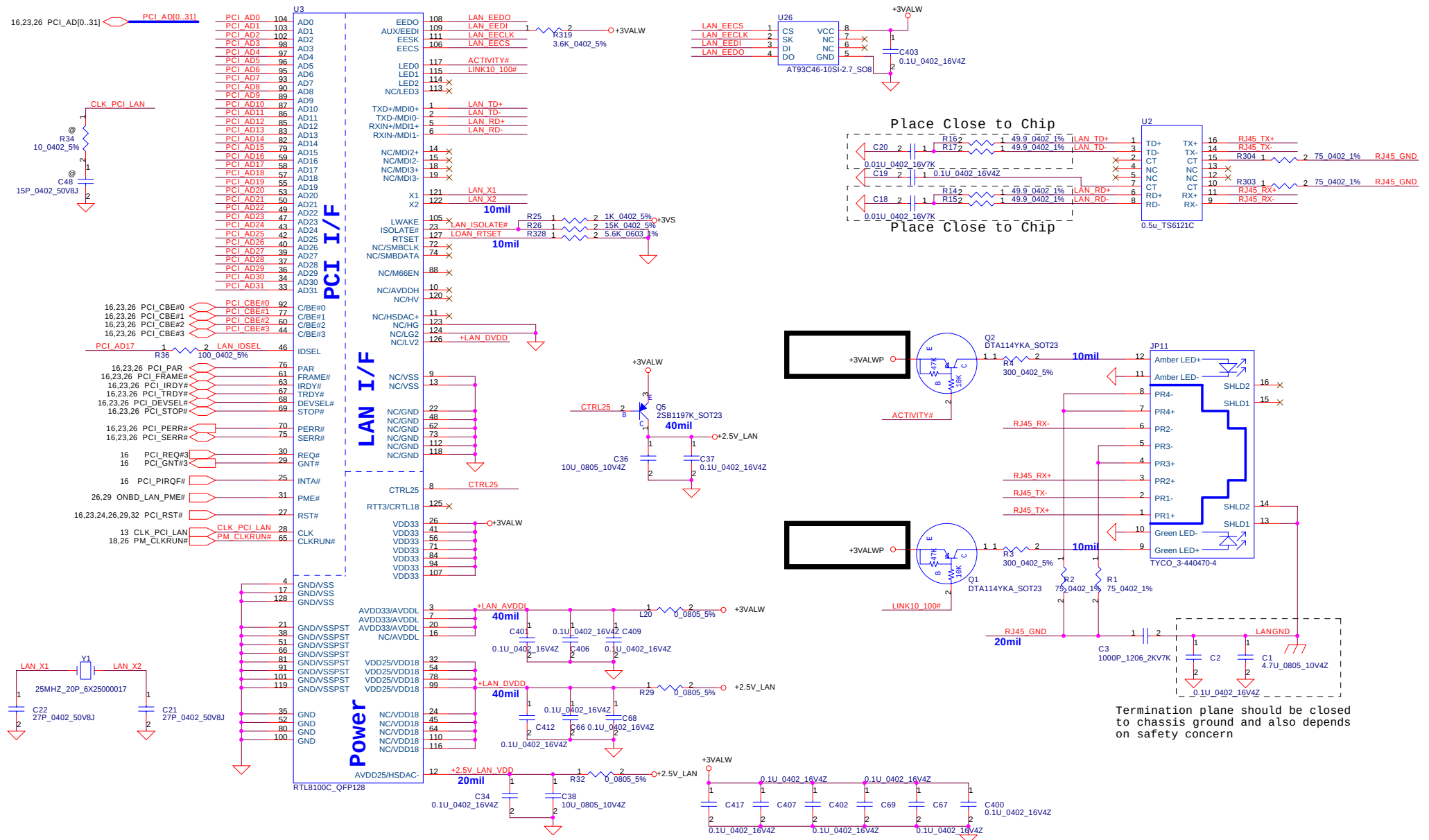


Placea caps. near CDROM CONN.

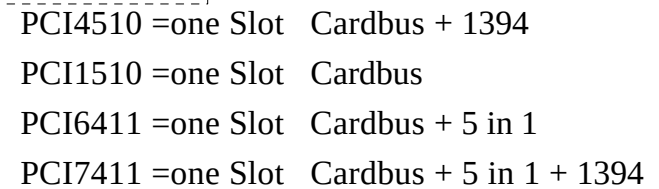


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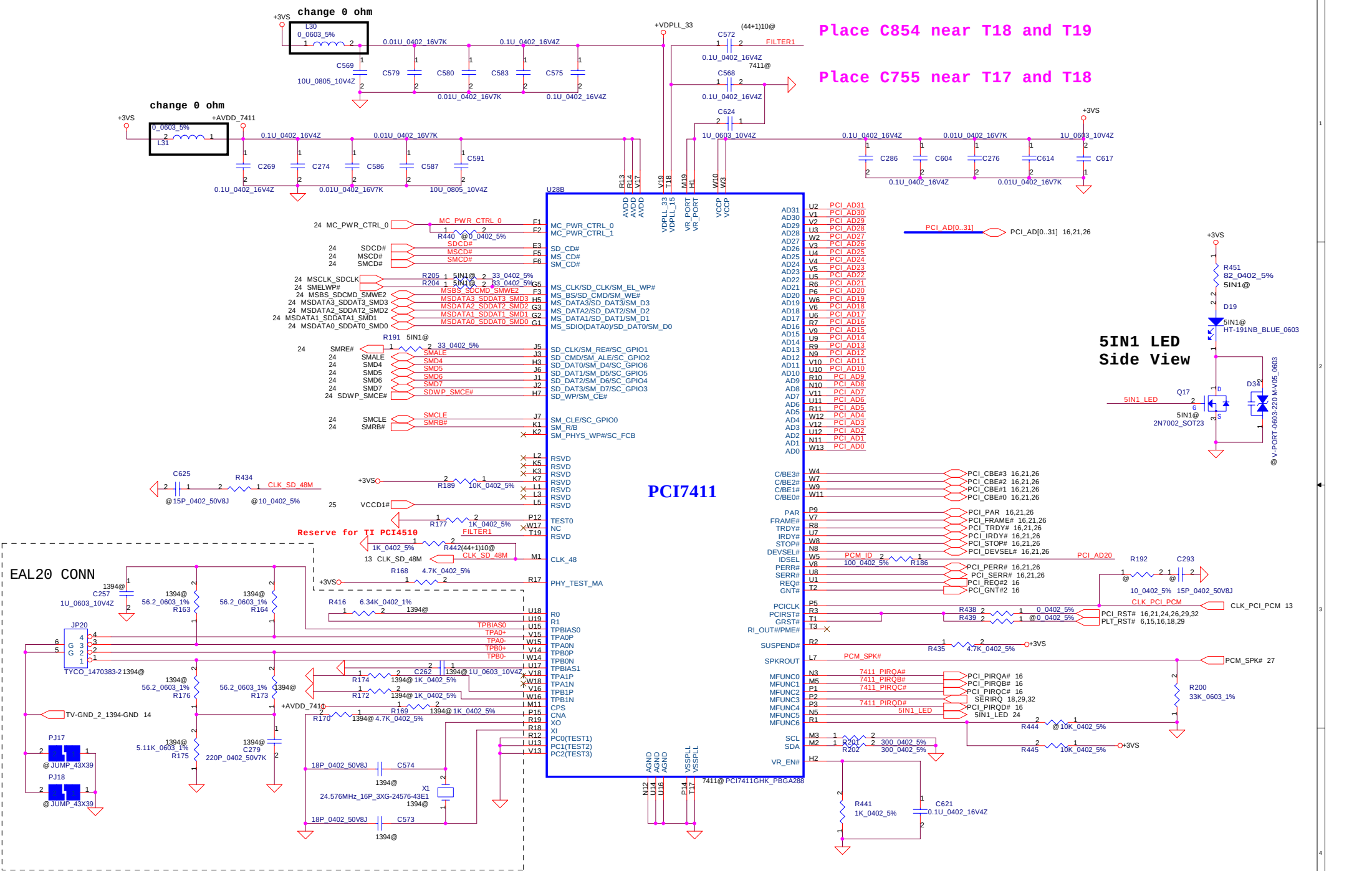
LAN RTL8100C(L)



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				Custom	1.0
				Document Number	
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PCI1510 & PCI6411 UNMOUNT THOSE PARTS

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Size		Document Number		Rev	
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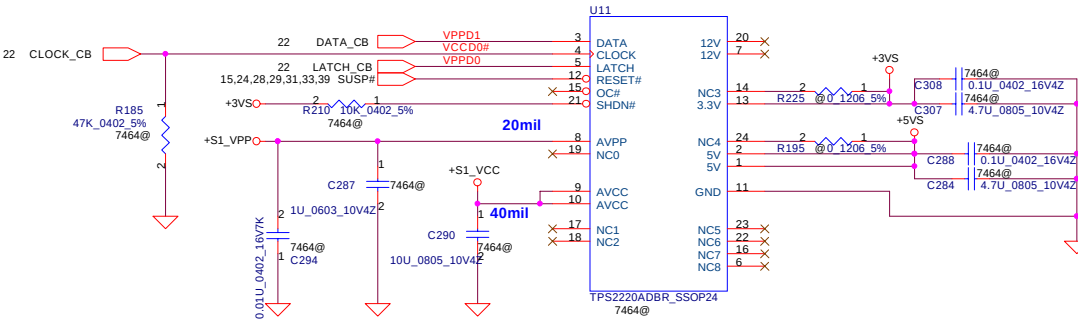


1

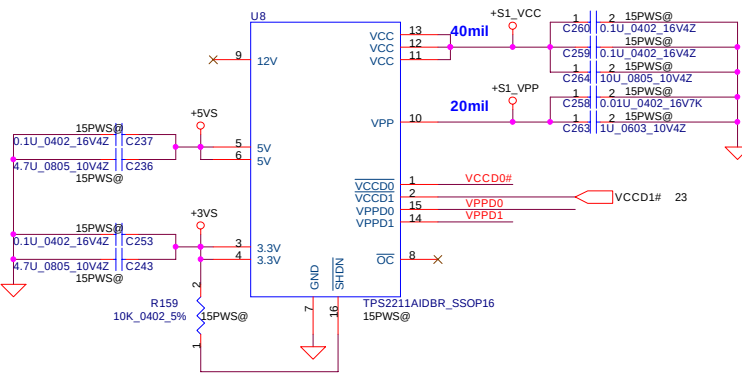


Power Switch for PCMCIA

Power Switch for PCMCIA (PCI7411 & PCI6411 only)



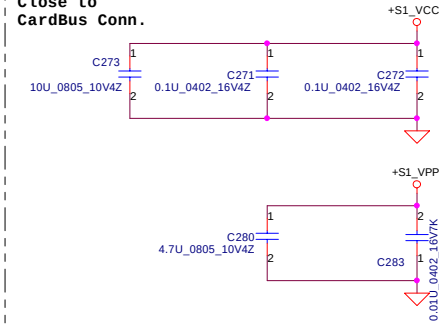
Power Switch for PCMCIA (PCI1510 & PCI4510 only)



CardBus Socket



Close to
CardBus Conn.



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INT_CD_L INT CD L2 20K_0402_5% 1 CD L

INT_CD_R INT CD R2 20K_0402_5% 1 CD R

CD_AGND 2 R262 20K_0402_5% 1 CD GNA

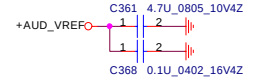
2 R246 0_0402_5% 1

2 R261 6.8K_0402_5% 1

2 R257 6.8K_0402_5% 1

2 R267 6.8K_0402_5% 1

bypass EQ when $\overline{\text{NBA_PLUG}} = \text{High}$

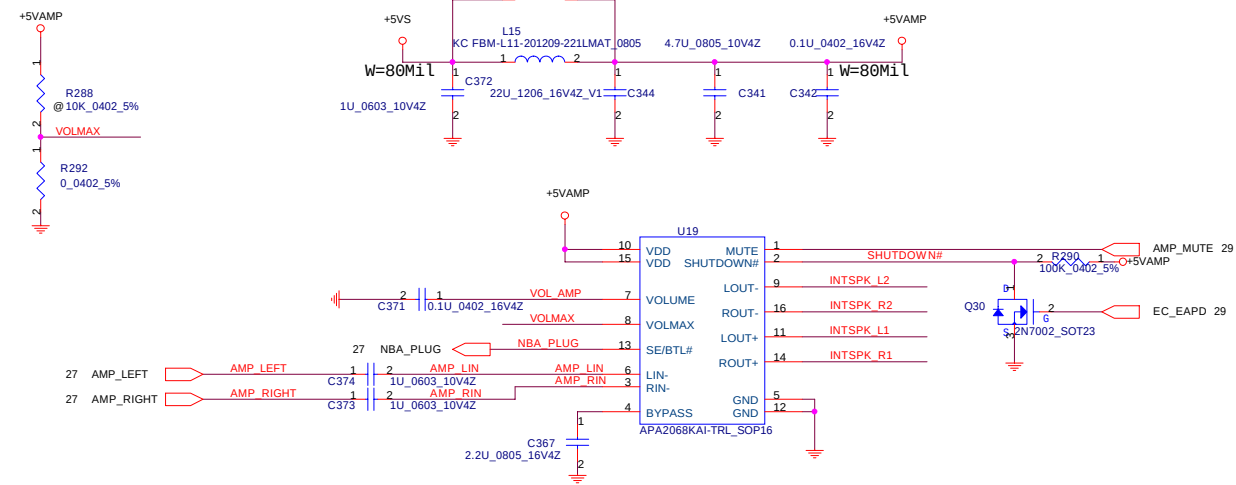


Place these components
close to Codec

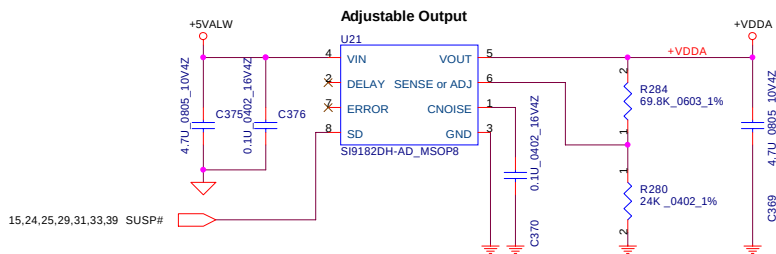
[illegible]

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				HTW00 M/B LA-2871		
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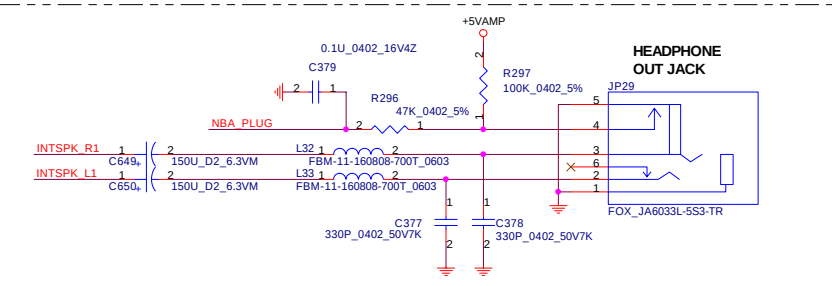
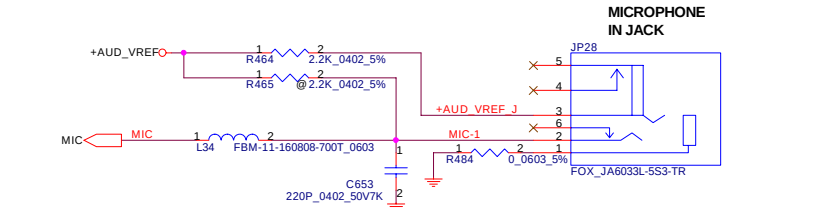
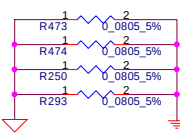
Audio AMP



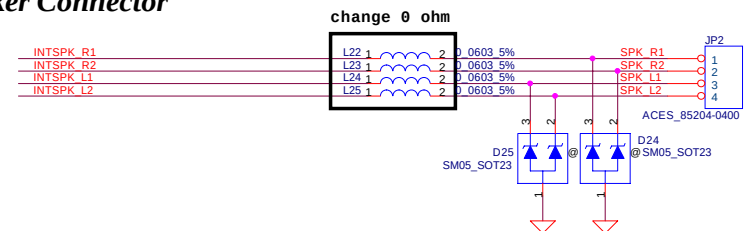
Regulator for CODEC



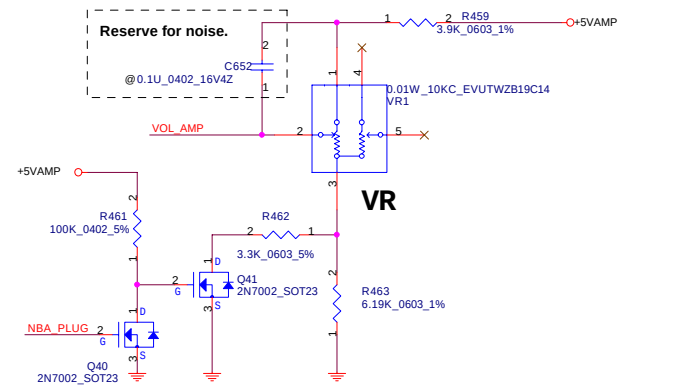
Moat Bridge



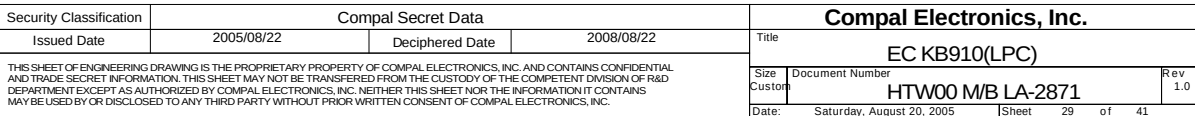
Speaker Connector



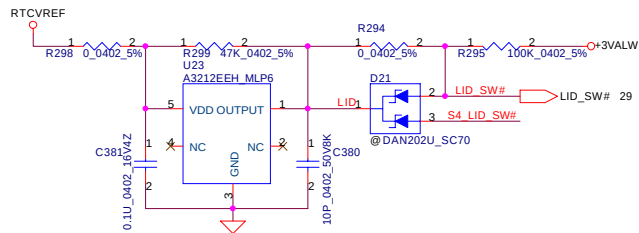
Variable Resistor



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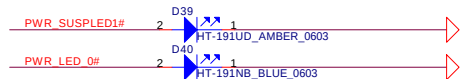
Lid SW



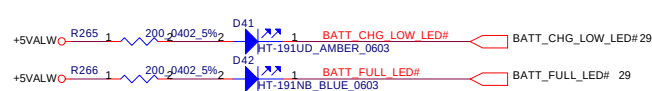
WL&BT LED



POWER/ON(Green Pin2,1) Suspend (Amber Pin3,4) LED



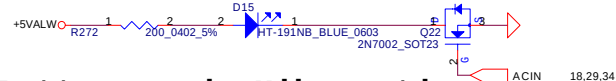
BATTERY CHG(Green Pin2,1) BATTERY LOW(Amber Pin3,4) LED



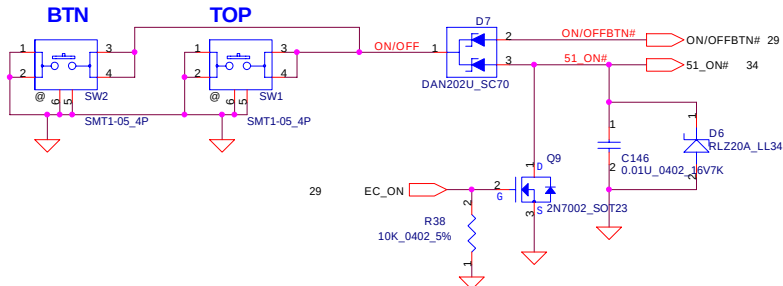
HDD LED



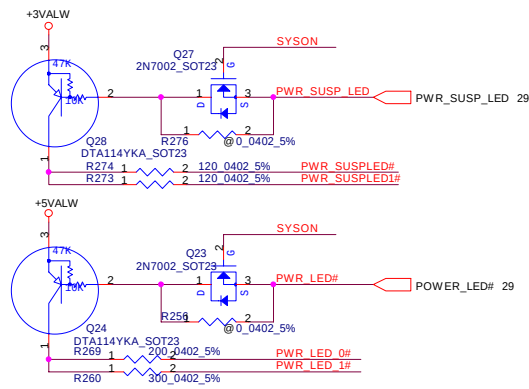
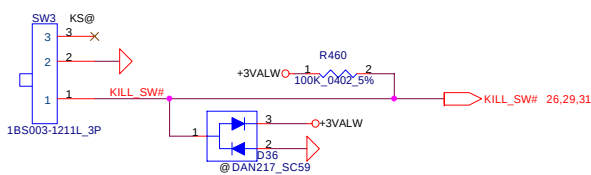
AC IN LED



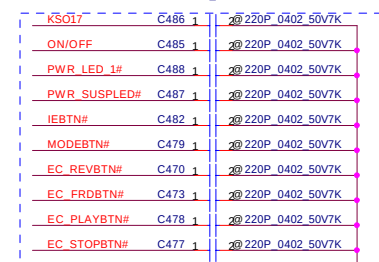
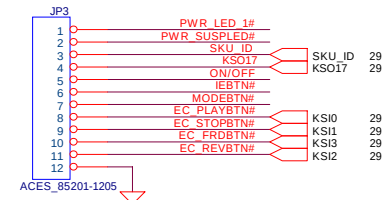
ON/OFF BUTTON for debug only



Kill SWITCH

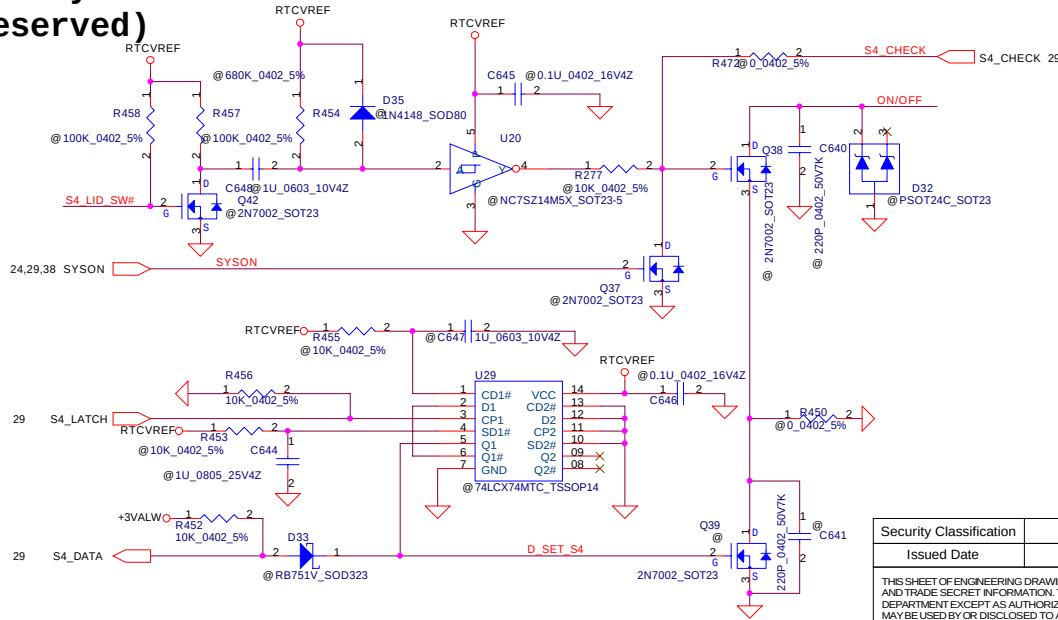


SW/LED Connector

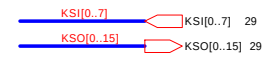
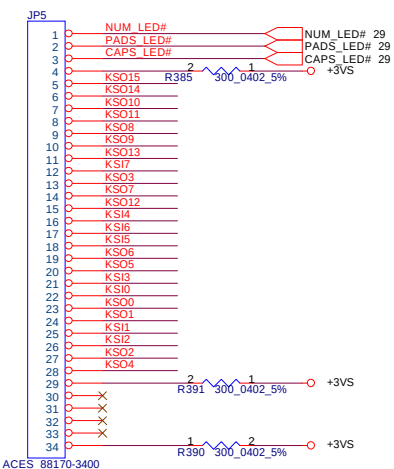


For EMI Request

Battery mode Hibernation (Reserved)



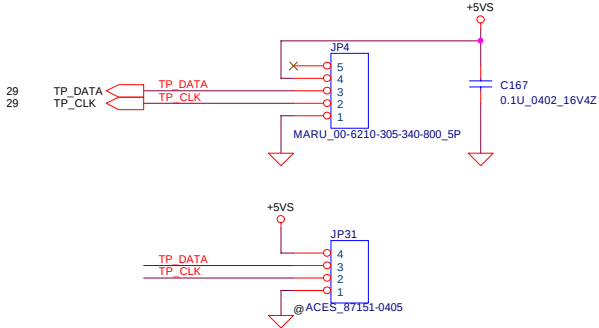
KEYBOARD CONN.



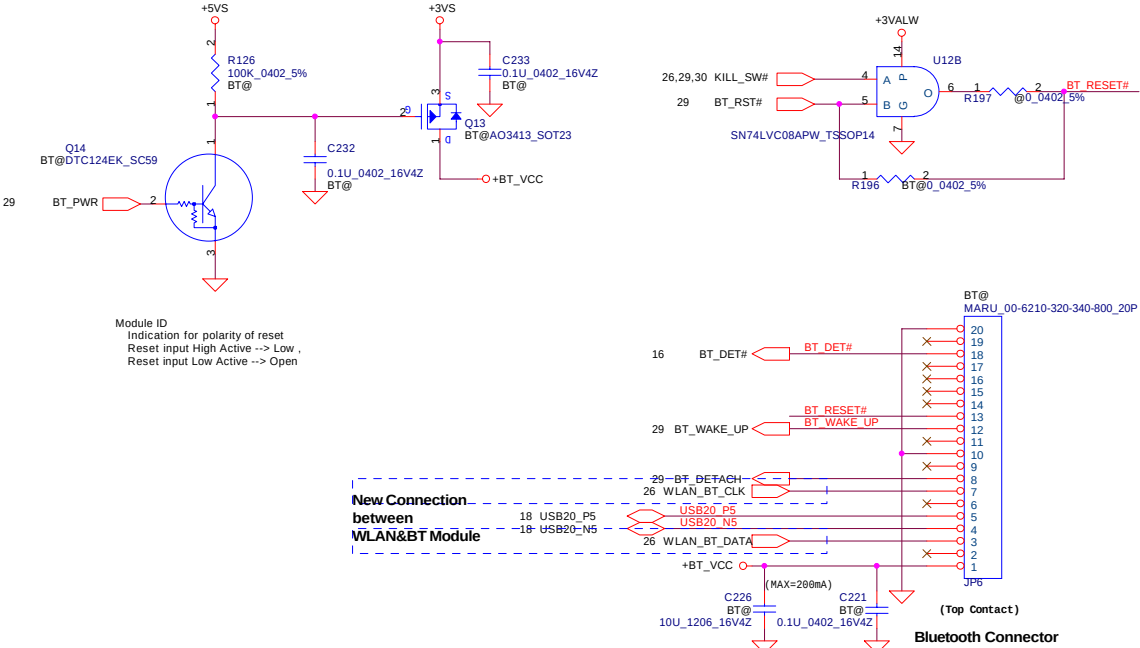
For EMI Request

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Issued Date		Deciphered Date		S4R/LID/KS/KB/LED/SW-B Conn	
2005/08/22		2008/08/22		HTW00 M/B LA-2871	
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		Sheet		30 of 41	

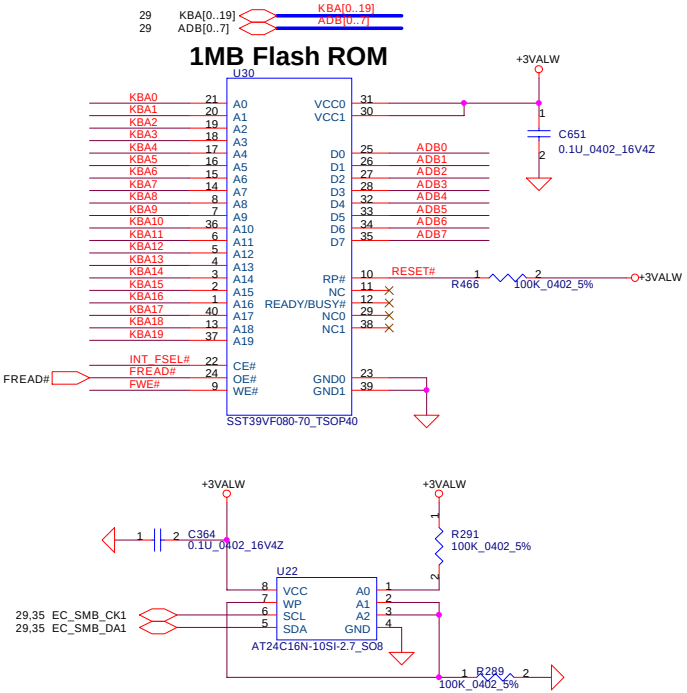
TP CONN.



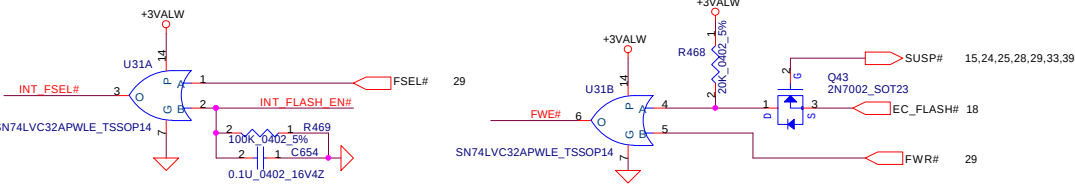
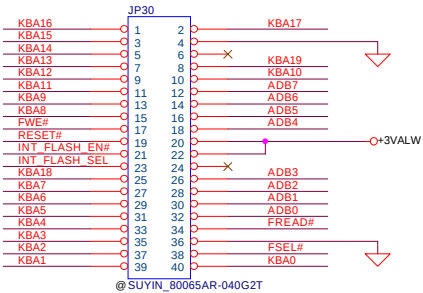
BlueTooth Interface



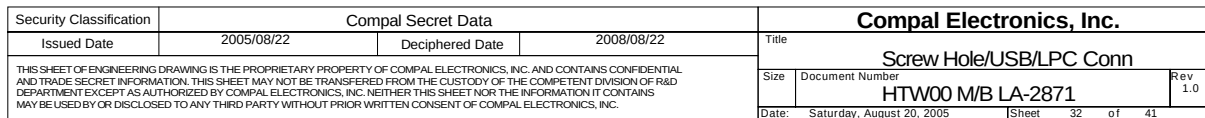
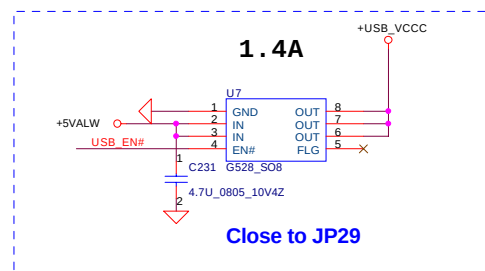
1MB Flash ROM



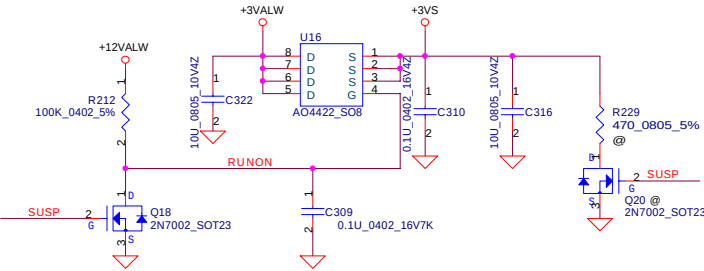
1MB ROM Socket



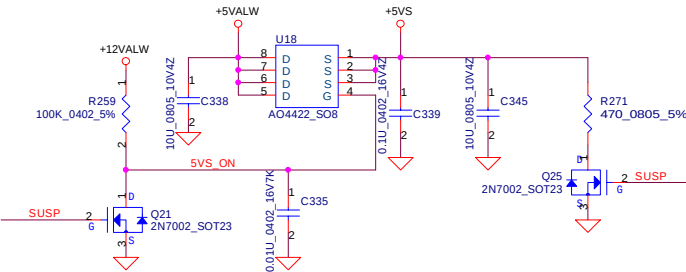
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				1MB BIOS/ TP Conn/ BT Conn
				Size
				Document Number
				HTW00 M/B LA-2871
				Rev
				1.0
				Date
				Monday, August 22, 2005
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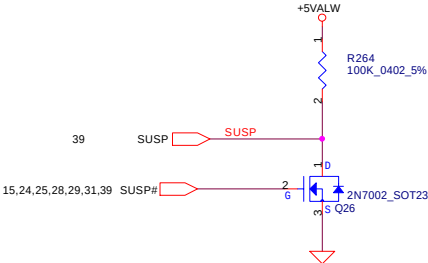
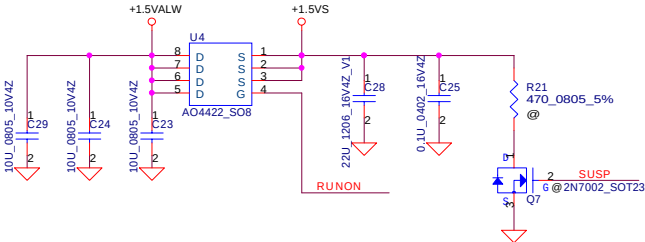
+3VALW to +3VS Transfer



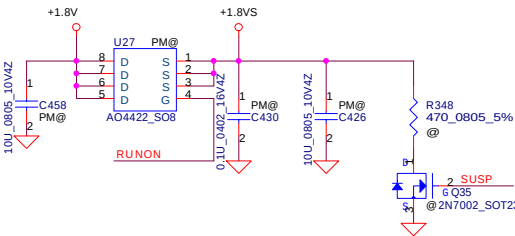
+5VALW to +5VS Transfer



+1.5VALW to +1.5VS Transfer

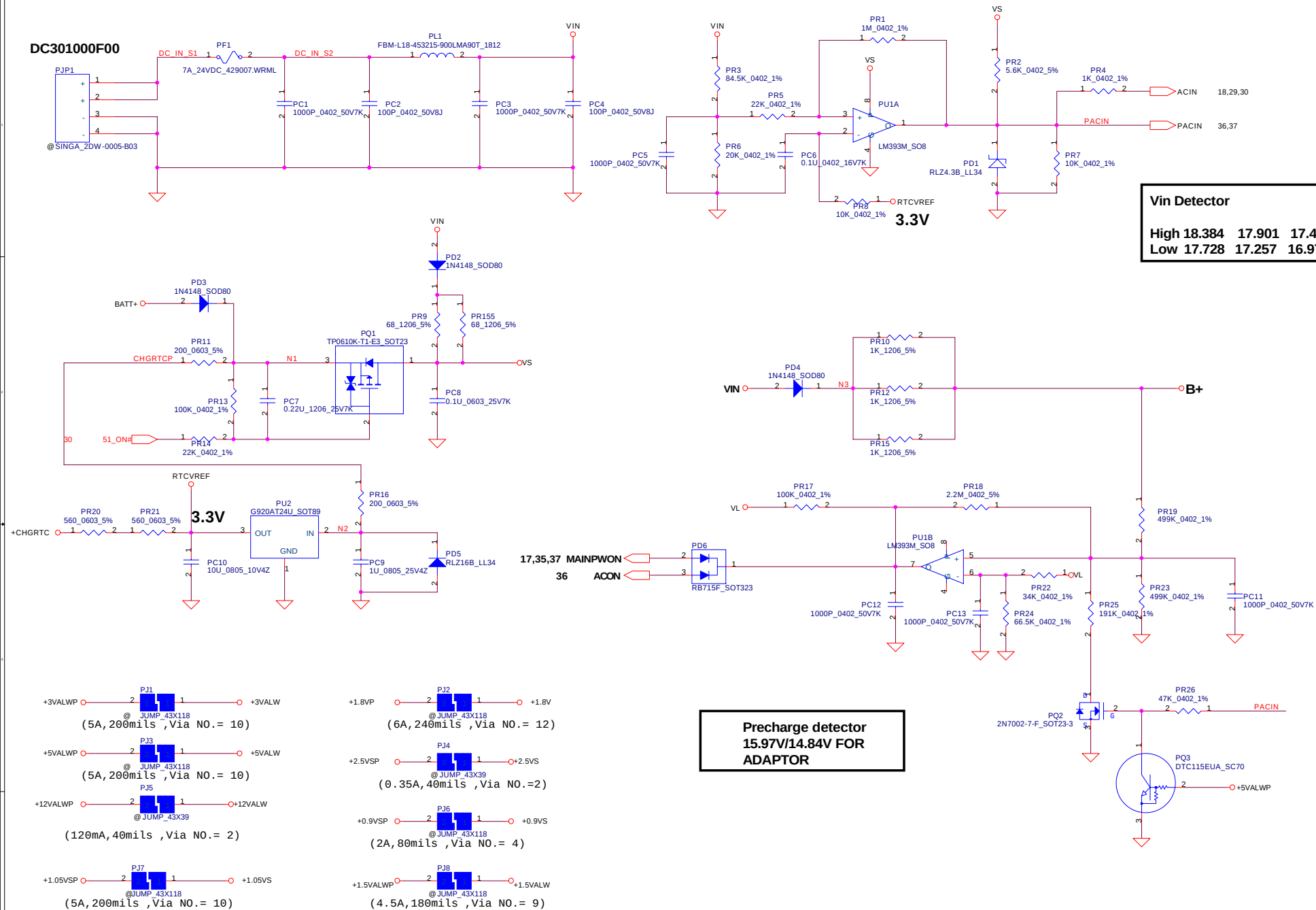


+1.8V to +1.8VS Transfer



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				Size	Document Number	Rev
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DC301000F00

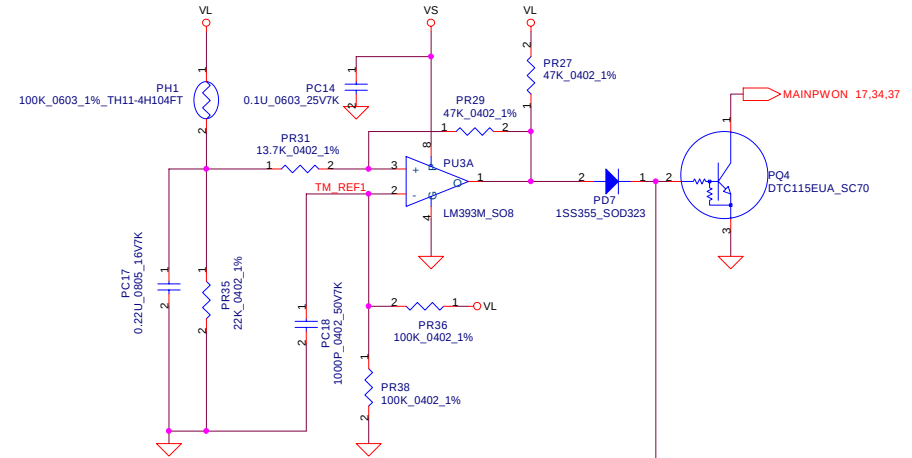
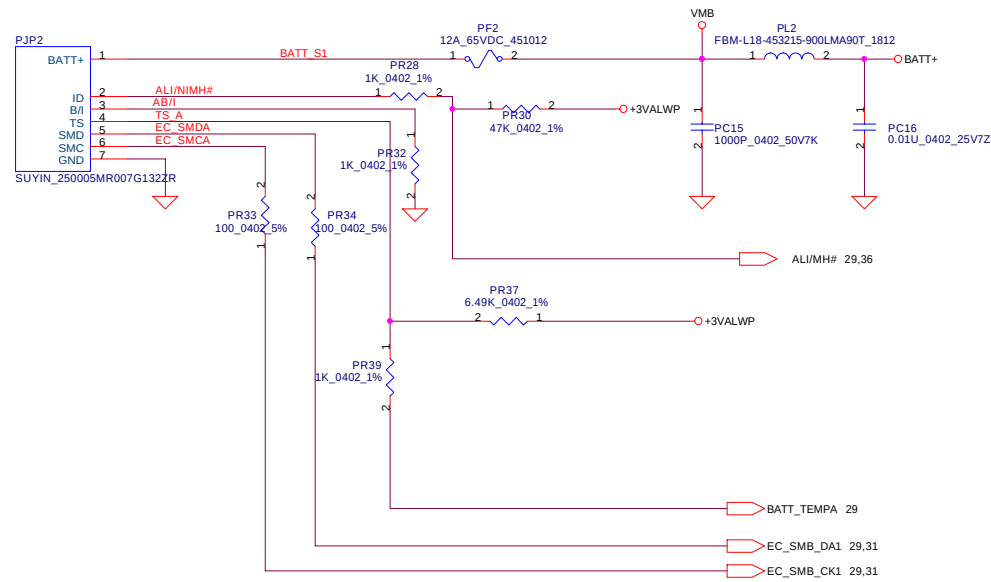


Vin Detector			
High	18.384	17.901	17.430
Low	17.728	17.257	16.976

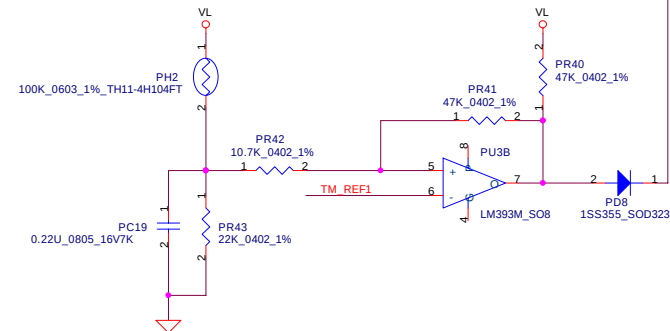
**Precharge detector
15.97V/14.84V FOR
ADAPTOR**

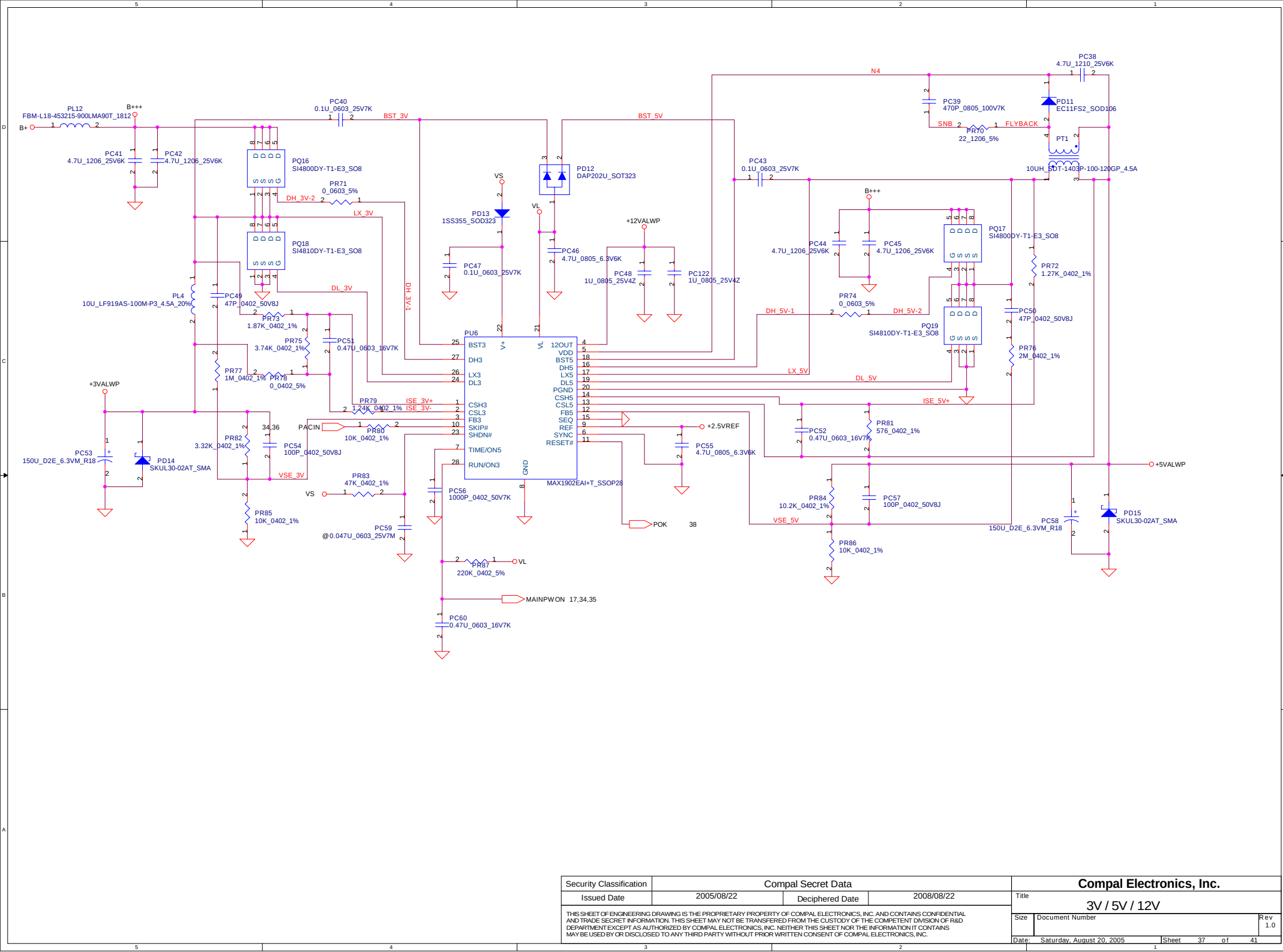
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Issued Date	2005/08/22	Deciphered Date	2008/08/22	Title	DCIN & DETECTOR
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PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C

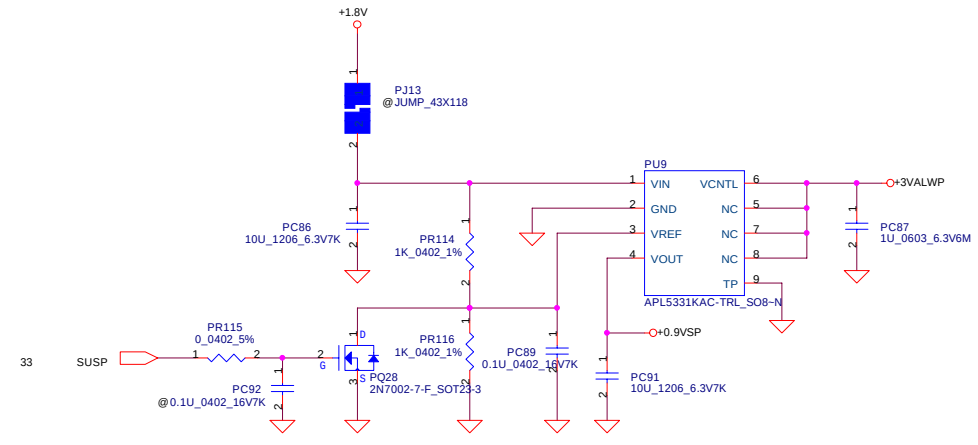
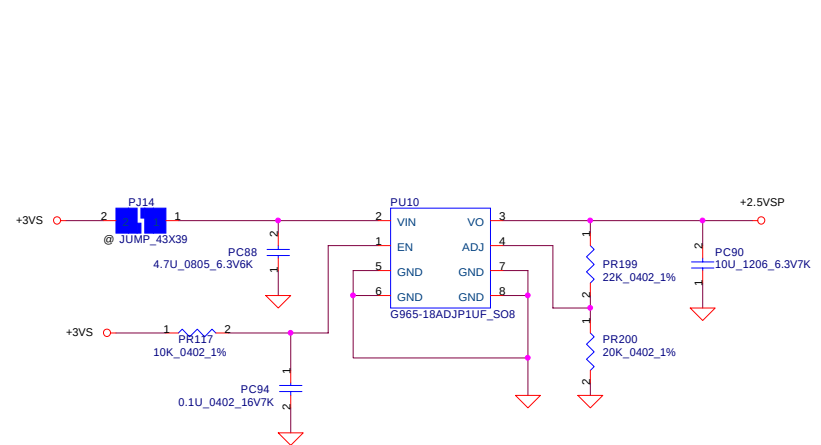
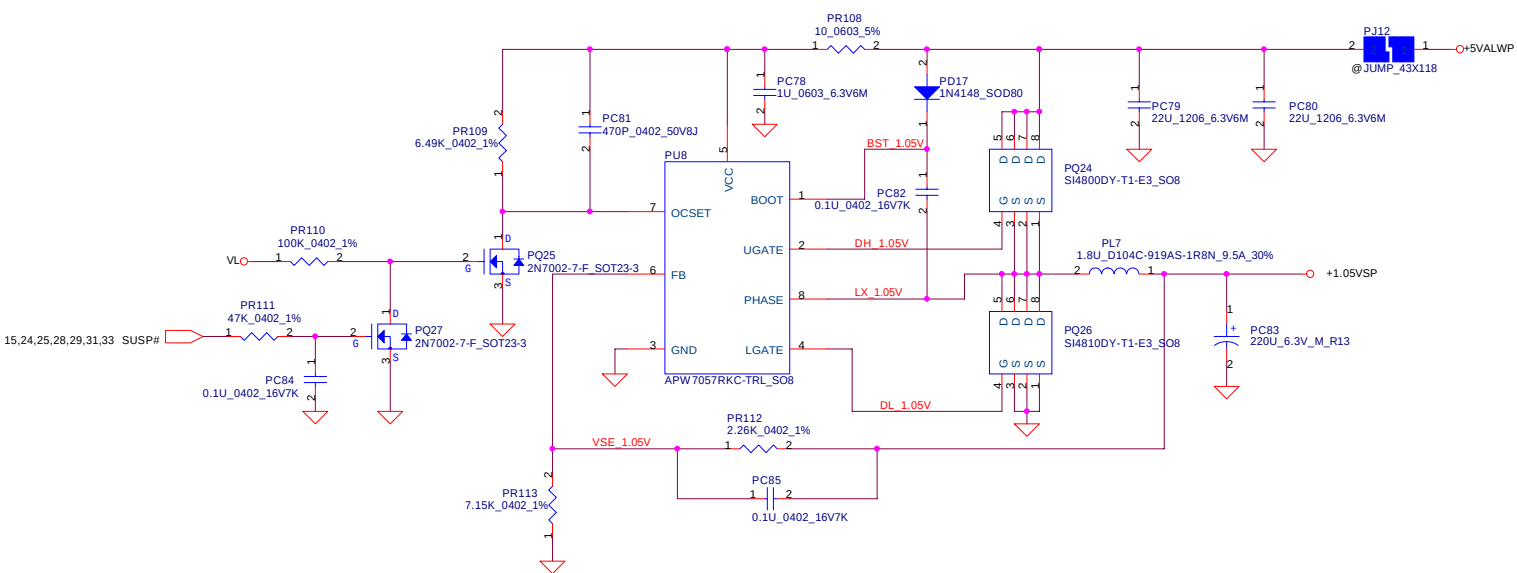


PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C

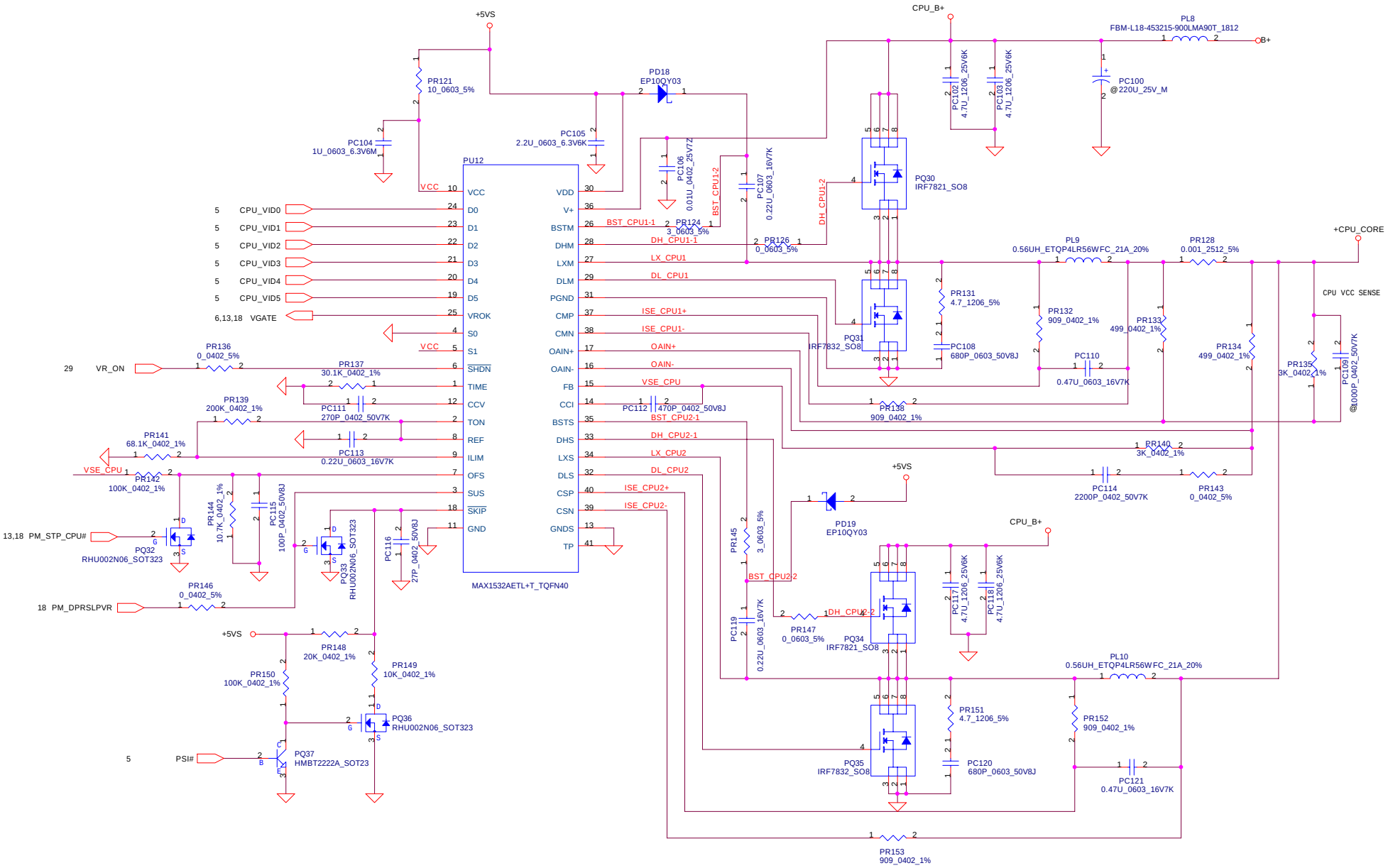




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POWER PIR LIST

	page	Reason for change	Modify list
DVT	36,37,38,40	For EMI request to reduce the power board band	Add bead PL11,PL12,PL13(SM010020720), add snubber 4.7ohm(SD001470B80)PR131,PR151 and 680P(SE024681J80)PC108,PC120 on CPU CORE
	47	Reduce the high frequency noise	Add booster resistor 3ohm(SD013300B80) PR90,PR91 on 1.8V/1.5V and PR124,PR145 on CPU CORE
	34	Add design margine	Change PC38 to 4.7U_1210(SE065475K80)
PVT			Add 68ohm(SD011680A80) PR155 and change PR9 to 68ohm
	39	Change +2.5VSP enable signal for HW request	Change +2.5VSP enable signal to +3VS
	40	For EMI request to reduce CPU power board band	Change PQ30,PQ34 to IRF7821(SB578210010); PQ31,PQ35 to IRF7832(SB578320010)
	40	For cost down	del PC100 and PR122,PR123,PR125,PR127,PR129,PR130

HW PIR LIST

HTW00 LA-2871 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	5/30	P29	ADD PULL DOWN 100K_0402_5% R475 ON SUSP#	TO PREVENT SUSP# FLOATING
2	5/30	P29	ADD PULL DOWN 100K_0402_5% R476 ON SYSON	TO PREVENT SYSON FLOATING
3	6/14	P17	CHANGE C241,C251 FROM 18PF TO 15PF	FINE TUNE RTC TIMING
4	7/01	P30	CHANGE LED TYPE FROM SIDE VIEW TO TOP VIEW	UPDATE LED LIBRARY
5	7/01	P30	CHANGE KB CONNECTOR EMI CAPS TO MOUNT	FOR EMI REQUEST
6	7/01	P27	ADD SPK_SEL CONNECTION BETWEEN EC AND CODEC	FOR CODEC EQ SELECTION FOR SPEAKER
7	7/01	P29	ADD MB_ID R477,R478 ON PIN88	FOR EC MB IDENTIFY
8	7/01	P17	CHANGE SATA DC COUPLING CAPS CAPACITANCE TO 3.9nf	TO MEET INTEL CRB RECOMMAND VALUE
9	7/01	P30	CHANGE LED RESISTOR R265, R266, R270, R272, RESISTANCE	TO INCREASE LED BRIGHTNESS
10	7/01	P20	ADD SATA HDD POWER CONTROL CIRCUIT	TO RESERVE BACKUP SOLUTION FOR SATA HDD RESET
11	7/01	P28	ADD R484 FOR MIC JACK GROUND PIN CLEAN	TO IMPROVE MIC SOUND QUALITY
12	7/01	P28	CHANGE U21 LDO POWER SOURCE FROM +5VALW TO +5VS	FOR POWER TRACE LAYOUT IMPROVE

HTW00 LA-2871 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	8/6	P28	CHANGE U21 PIN 4 FROM +5VS TO +5VALW	TO PREVENT NOISE FROM HDD SPIN UP
2	8/6	P15	CHANGE R306, R307 FROM RES TO BEAD	FOR EMI REQUEST
3	8/6	P21	CHANGE U2 FROM H-50P (H=2mm) TO TS6121C (H=4mm)	FOR COST POINT OF VIEW
4	8/6	P23	CHANGE D19 LED COLOR FROM GREEN TO BLUE	CUSTOMER SPEC CHANGE
5	8/6	P09	ADD R488 0_0603 BETWEEN +2.5VS_CRTDAC TO +2.5VS	TO IMPROVE CRT VIDEO QUALITY
6	8/6	P29	ADD PULL HIGH RES R487 ON PIN176 FOR WW/JPN# SELECT	TO CONTROL M/B CONFUIRATION
7	8/6	P30	CHANGE D15,D18,D40,D42 LED COLOR FROM GREEN TO BLUE	CUSTOMER SPEC CHANGE

HTW00 LA-2871 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	8/22	P20	CHANGE C661,C662,Q44,Q45,Q47,Q48,R411,R479,R480,R482 ,R483 FROM MOUNT TO RESERVE	REMOVE SATA-HDD POWER RESET FUNCTION FOR SW REQUEST
2	8/22	P18 P28	CHANGE D38,R485 FROM MOUNT TO RESERVE CHANGE R459 RESISTANCE FROM 4.53K TO 3.9K CHANGE R463 RESISTANCE FROM 4.22K TO 6.19K CHANGE R462 RESISTANCE FROM 4.87K TO 3.3K	TO REDUCE HEAD PHONE GAIN SETTING
3	8/22	P31	CHANGE JP4 AND JP6 VENDOR FROM ACES TO MANUNIX	FOR CUSTOMER'S REQUEST
4	8/22	P31	RESERVE JP31	FOR TEST ABILITY

PROPRIETARY NOTE				
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Issued Date	2005/08/22	Deciphered Date	2008/08/22	
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