

QHRAE

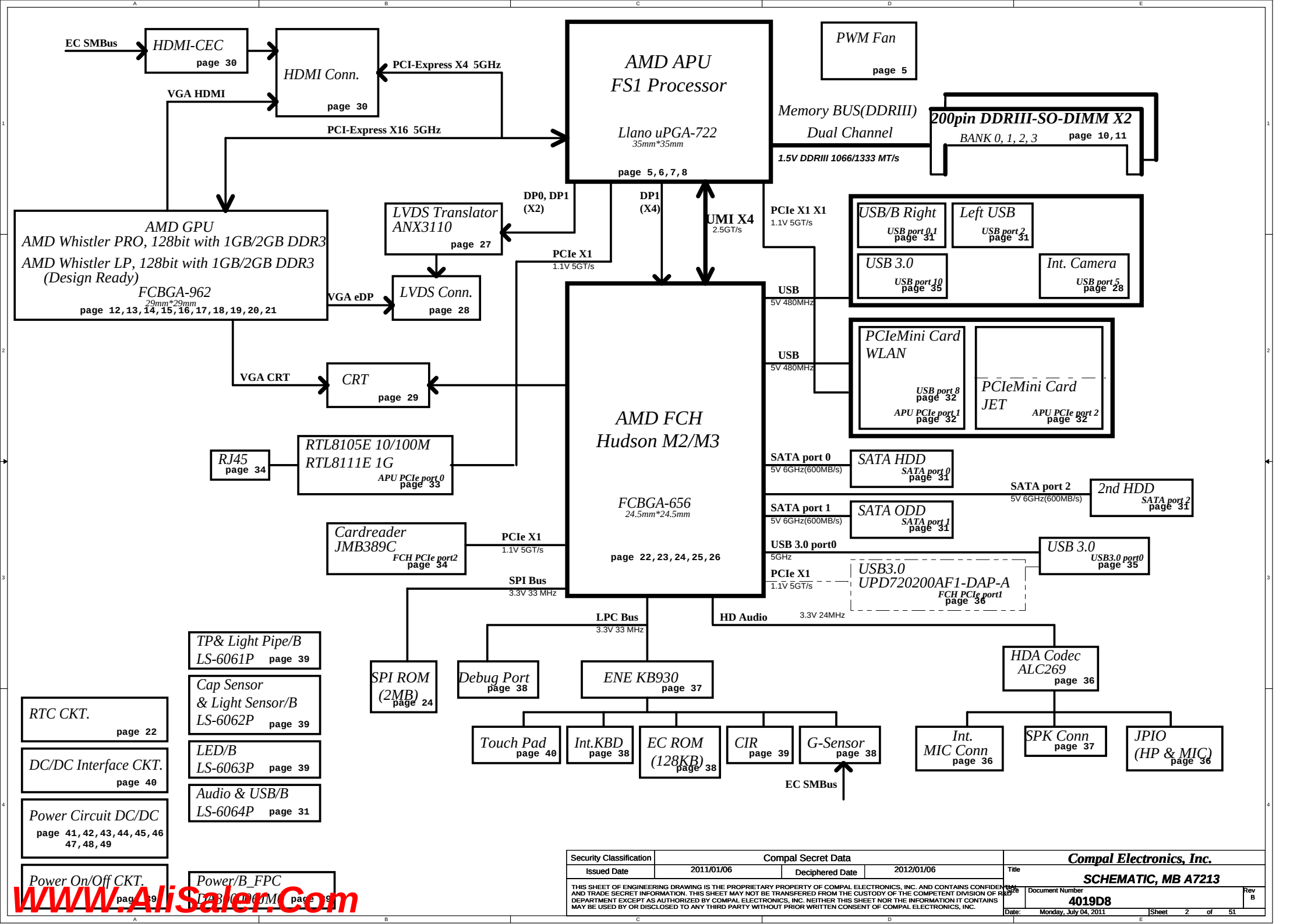
Superior 10AS/10ASG

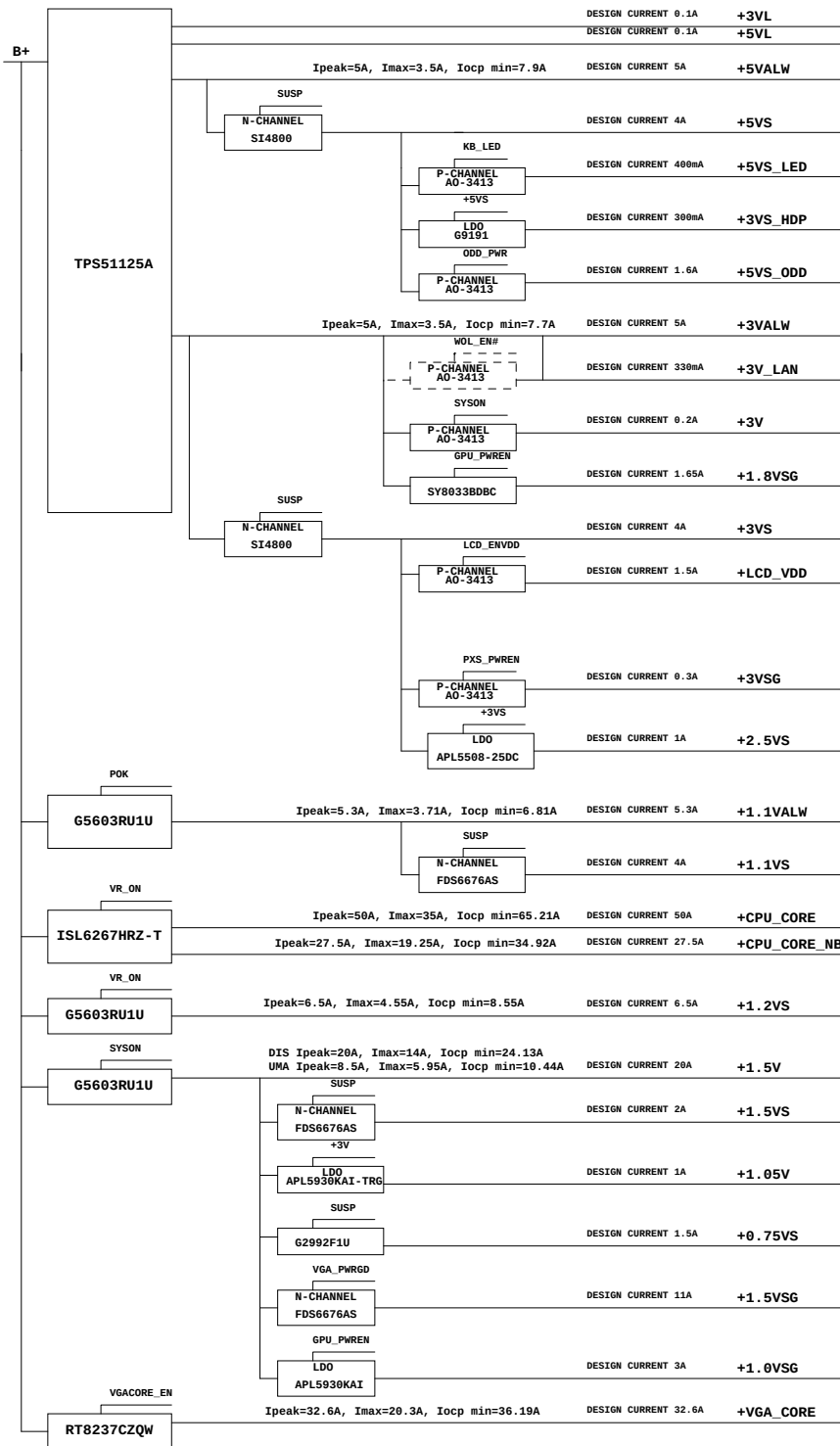
LA-7213P REV 1.0 Schematic

AMD Llano FS1 Processor / Hudson M2/M3
Whistler Pro

2011-04-30 Rev 1.0

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				Date	Monday, July 04, 2011
				Sheet	1 of 51





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				Date	Monday, July 04, 2011
				Sheet	3 of 51

Voltage Rails (0 MEANS ON X MEANS OFF)

power plane State	+RTCVC	B+	+5VL +3VL	+5VALW +3VALW +1.1VALW +VSB	+1.5V +3V +1.05V	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +CPU_CORE +CPU_CORE_NB +VGA_CORE +3VSG +1.8VSG +1.5VSG +1.0VSG
S0	0	0	0	0	0	0
S1	0	0	0	0	0	0
S3	0	0	0	0	0	X
S5 S4/AC	0	0	0	0	X	X
S5 S4/ Battery only	0	0	0	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X	X

BTO Option Table

Function	HDMI				SKU		
description	HDMI				SKU		
explain	UMA PowerXpress	Discrete	COMMON	CEC	UMA	PowerXpress	Discrete
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	UMA@	UMA@+VGA@+PXS@	VGA@+DIS@

Function		LAN		CIR	KB Light
description		LAN		CIR	KB Light
explain		10/100M	GIGA	CIR	KB Light
BTO		8105E@	8111E@	CIR@	KBL@

Function		G-SENSOR	Cam & Mic	Panel		
description		G-SENSOR	Cam & Mic	Panel (DIS@)		
explain		G-SENSOR	Cam & Mic	3D LVDS	eDP	Non-3D & EDP
BTO		GSENSOR@	CAM@	3D@+NOEDP@	EDP@	NO3D@+NOEDP@

Function	GPIO for PowerXpress		Chipset			
description	PowerXpress (PXS@)		FCH		GPU	
explain	PowerXpress Enable	Crossfire Enable	Hudson-M3		Whistler Pro	
BTO	PXSEN@	CROSSEN@	HUDM3R1@	HUDM3R3@	WHPROR1@	WHPROR3@

Function	PowerXpress		Renesas USB3.0	FCH		EC	
description	PowerXpress (PXS@)		Renesas USB3.0	FCH		EC	
explain	BACO mode	Non-BACO	Renesas USB3.0	Hudson-M2	Hudson-M3	KB-930	KB-9012
BTO	BACO@	NOBACO@	RENE@	M2@	M3@	KB930@	KB9012@

FCH SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	WLAN		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b
Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	CPU Thermal Sensor	98 H	1001 1001 b
+3VS	GPU Thermal Sensor	41 H	0100 0001 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	Light Sensor	52 H	0101 0010 b
+3VS	3D - Bootloader	C0 H	1100 0000 b
+3VS	3D - Slave	C0 H	1100 0000 b

STATE	SIGNAL	SLP_S3#	SLP_S5#
Full ON		HIGH	HIGH
S1(Power On Suspend)		HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH
S4 (Suspend to Disk)		LOW	HIGH
S5 (Soft OFF)		LOW	LOW
G3		LOW	LOW

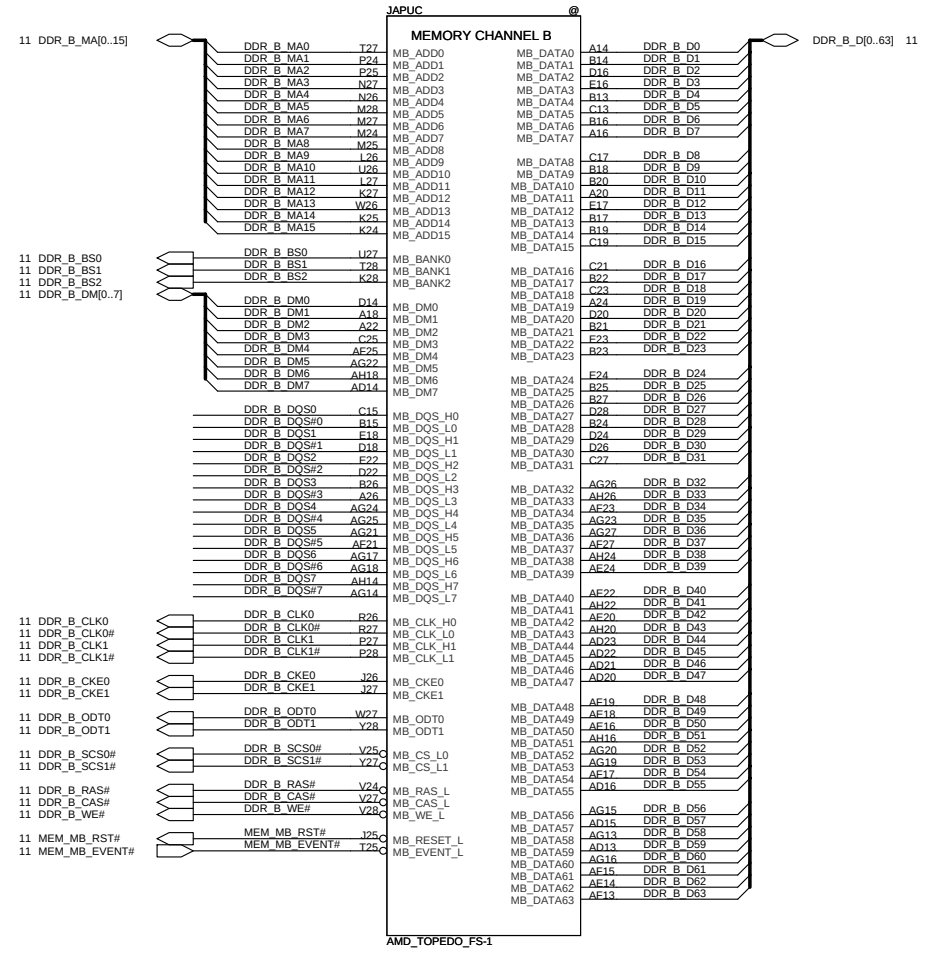
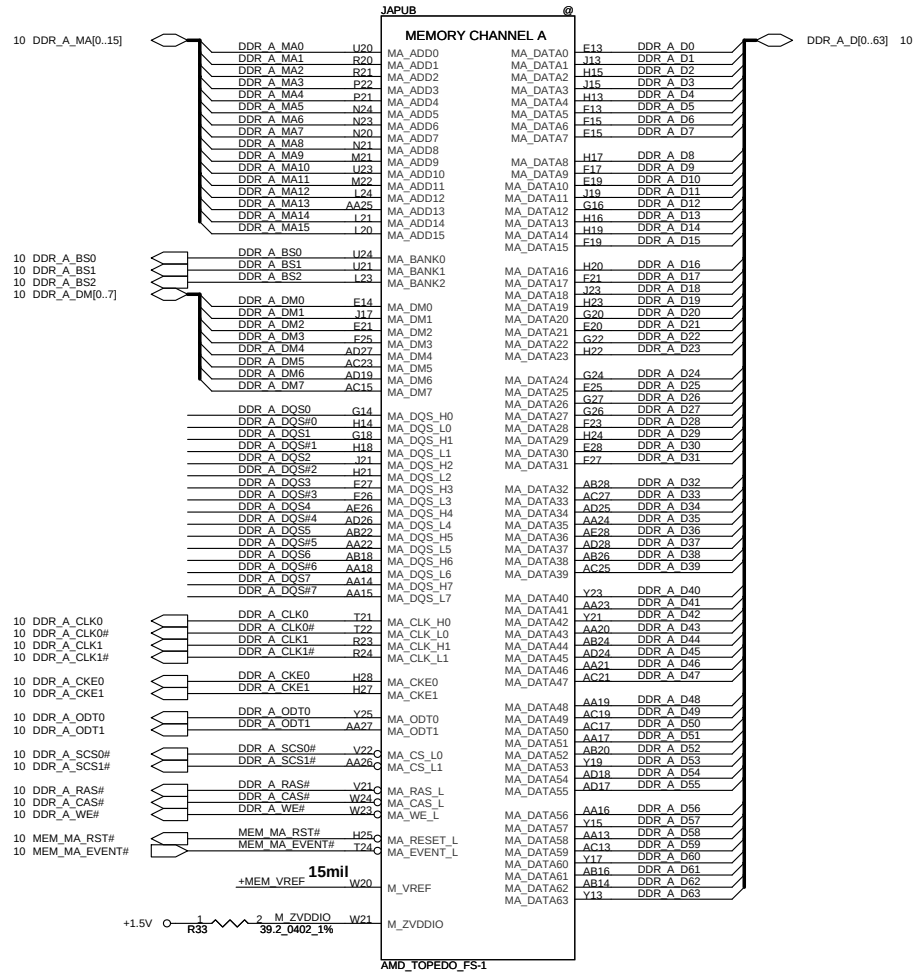
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								Custm		4019D8		B	
								Date:		Monday, July 04, 2011		Sheet	

10 DDR_A_DQS[0..7]

10 DDR_A_DQS# [0..7]

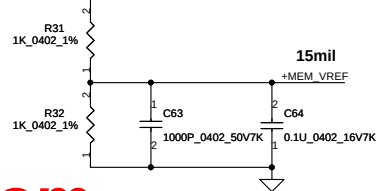
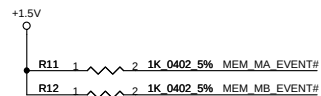
11 DDR_B_DQS[0..7]

11 DDR_B_DQS# [0..7]

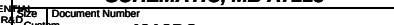


EVENT# pull high

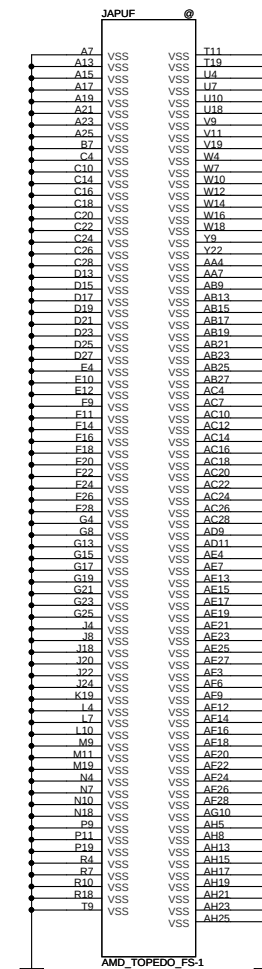
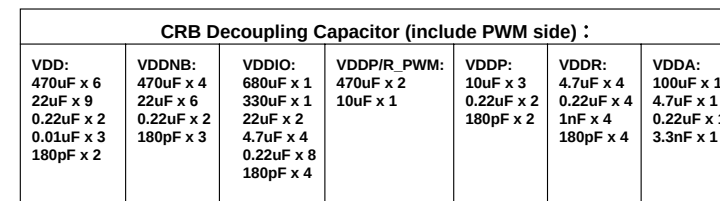
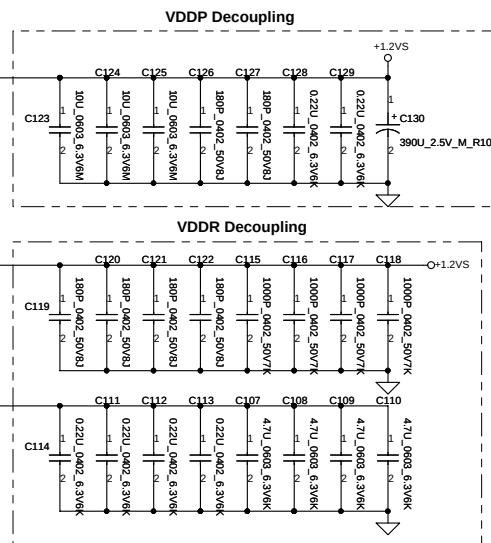
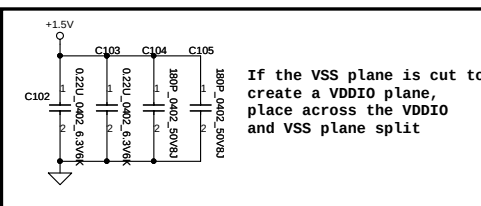
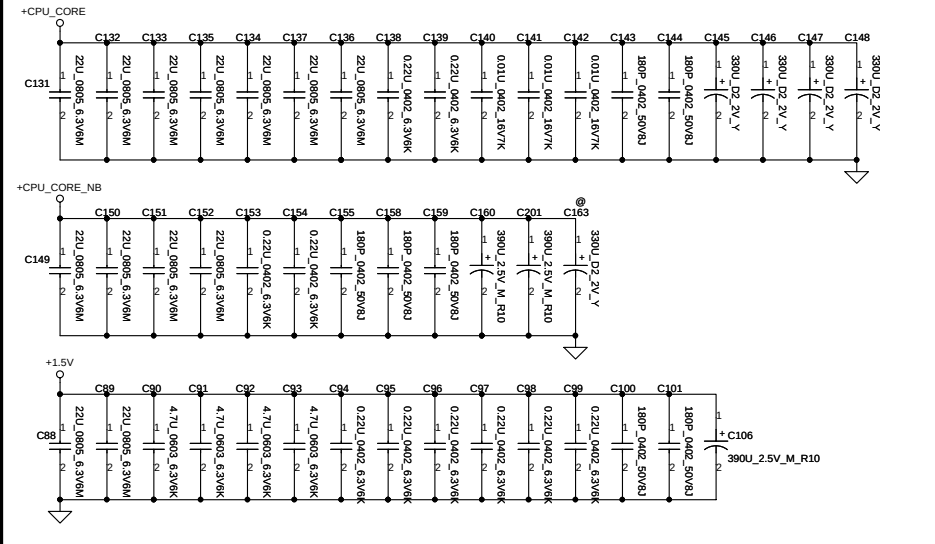
0.75V Reference Voltage



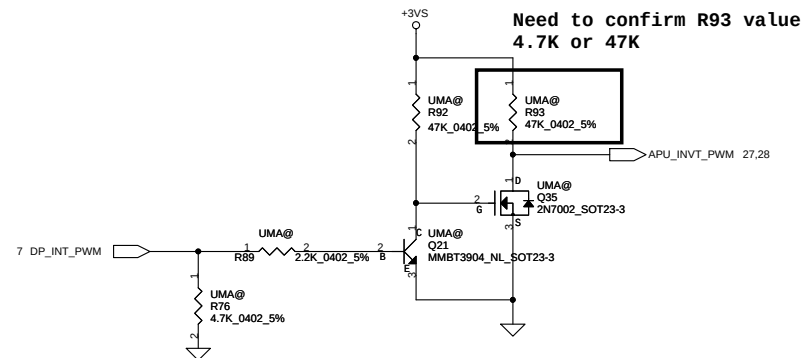
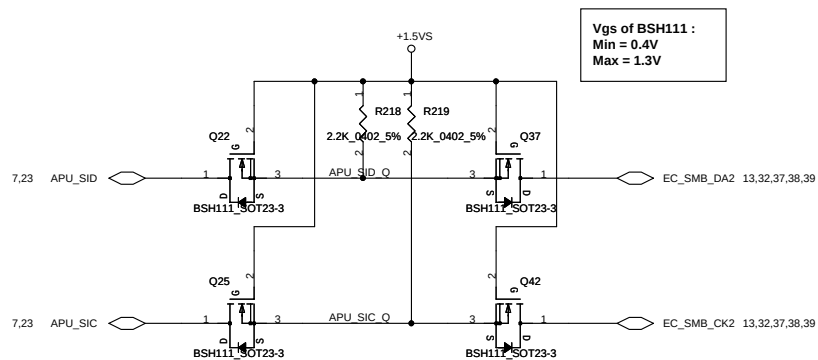
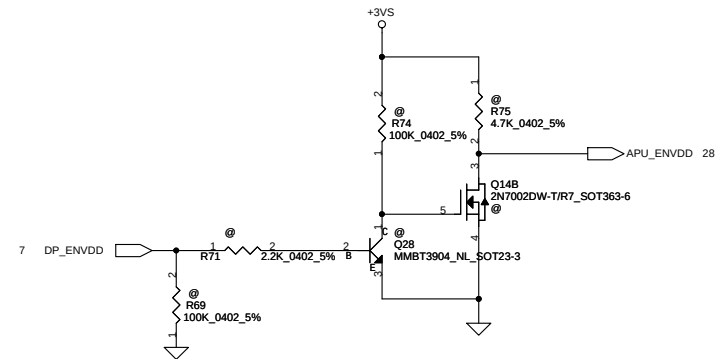
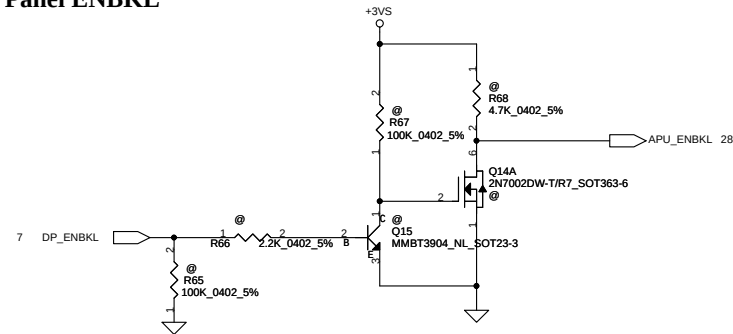
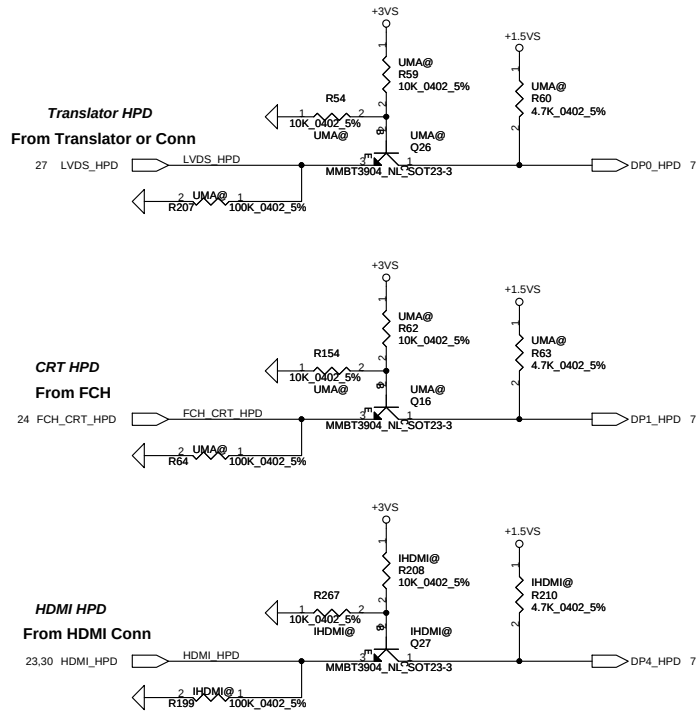
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				4019D8	Rev B
				Monday, July 04, 2011	Sheet 6 of 51



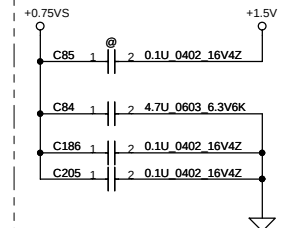
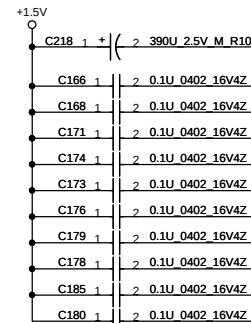
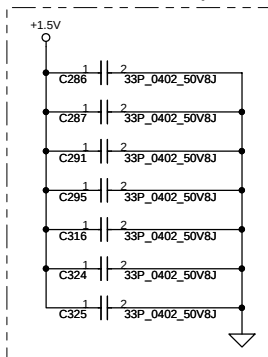
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				4019D8	
Date:	Monday, July 04, 2011	Sheet	7	of	51



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				Date:	Monday, July 04, 2011	
				Sheet	8	of 51

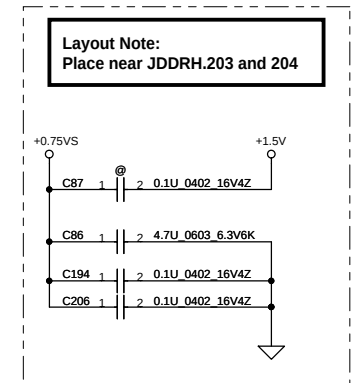
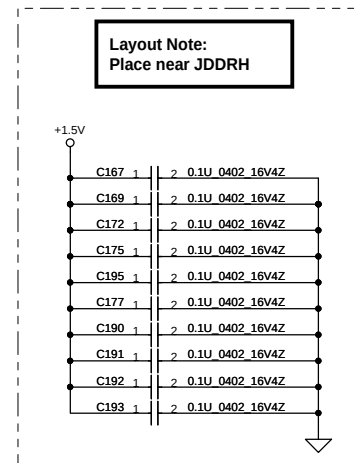
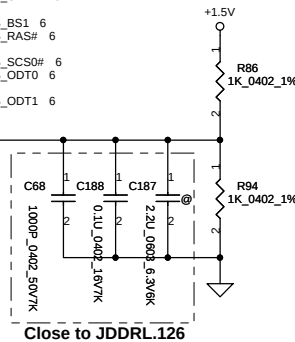
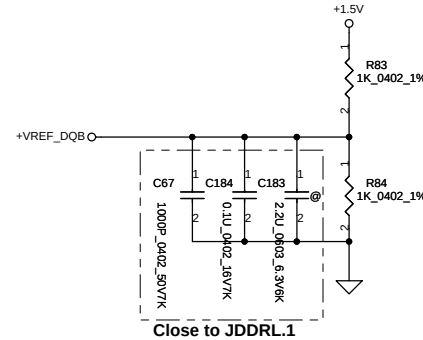
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				4019D8	
				Date: Monday, July 04, 2011	Sheet 9 of 51



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DDR3 SO-DIMM B Standard Type

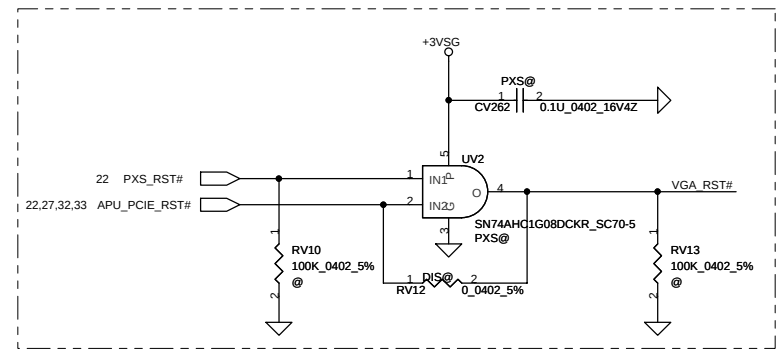
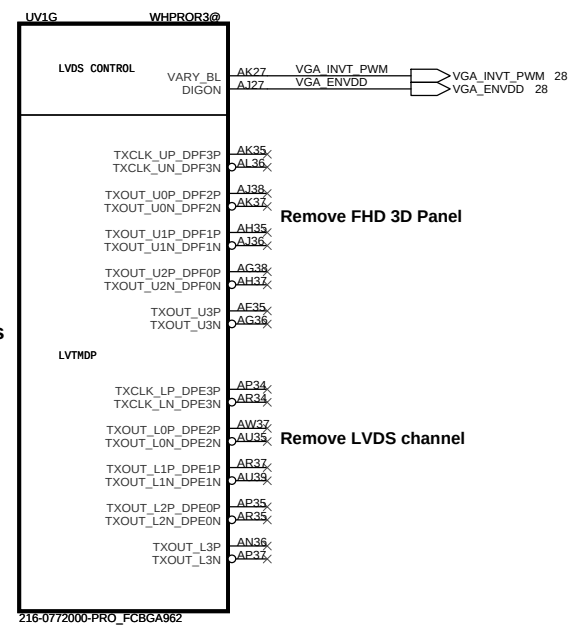
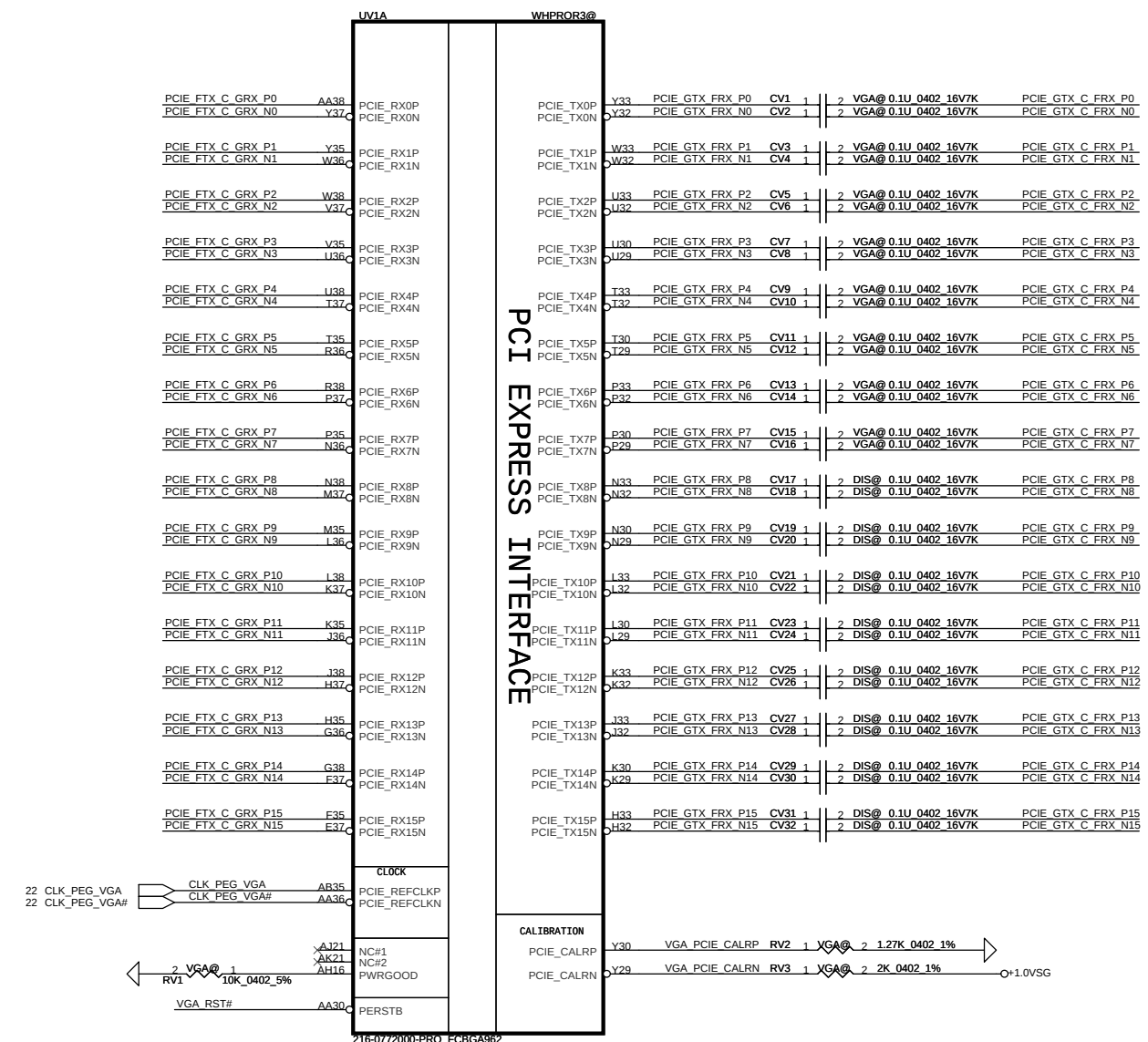


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								Custom	4019D8			B			
								Date: Monday, July 04, 2011				Sheet	11	of	51

5 PCIE_FTX_C_GRX_P[0..15] PCIE_FTX_C_GRX_P[0..15]
5 PCIE_FTX_C_GRX_N[0..15] PCIE_FTX_C_GRX_N[0..15]

PCIE GTX_C_FRX_P[0..15] PCIE GTX_C_FRX_P[0..15] 5
PCIE GTX_C_FRX_N[0..15] PCIE GTX_C_FRX_N[0..15] 5

VGA_INVT_PWM 1 2
VGA_ENVDD 1 2
RV4 10K_0402_5%
RV5 10K_0402_5%



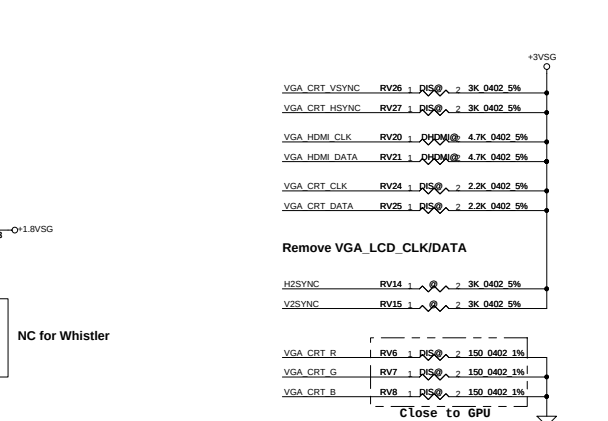
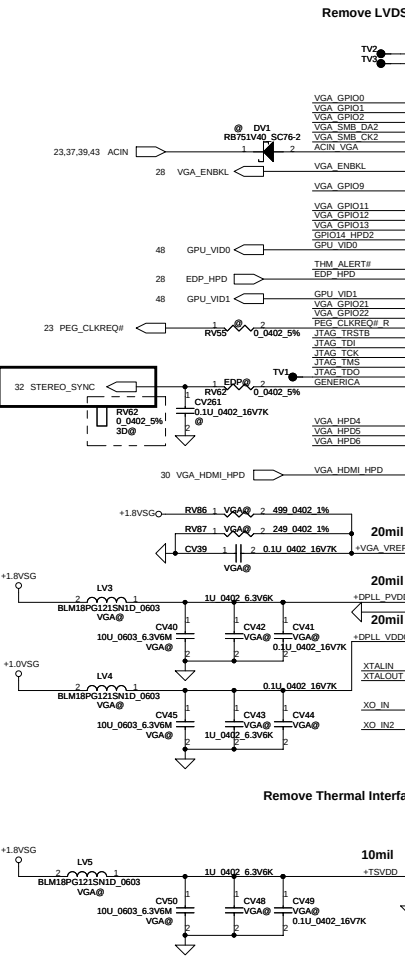
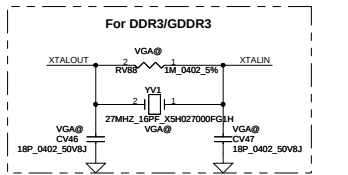
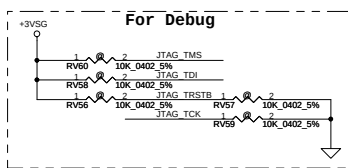
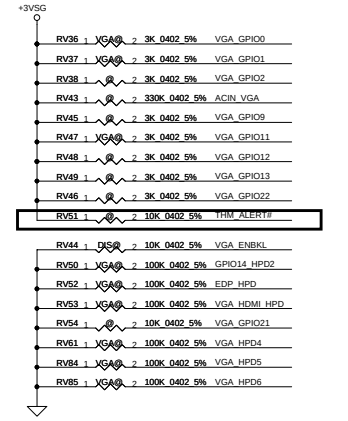
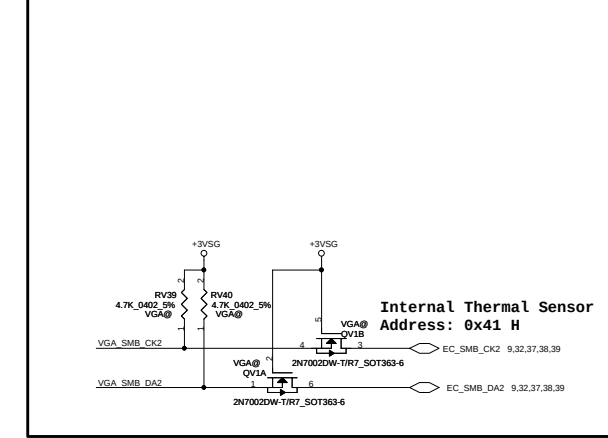
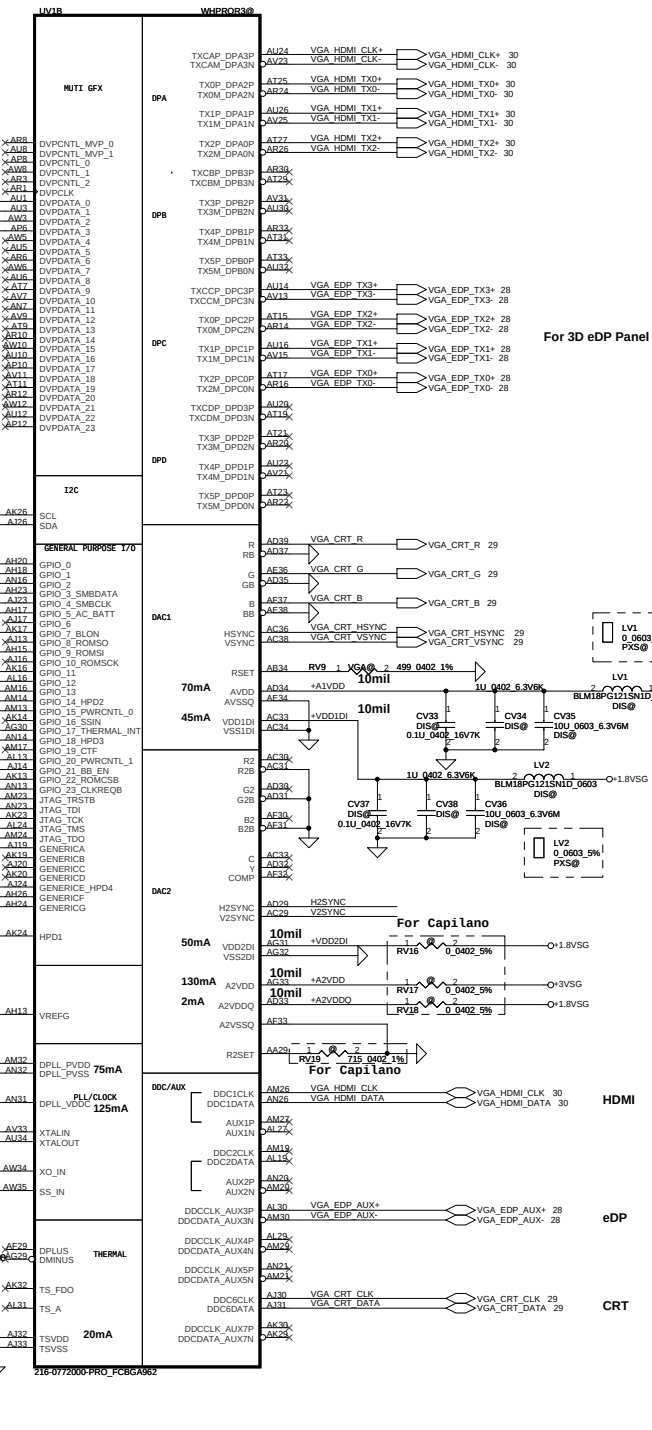
22 CLK_PEG_VGA CLK_PEG_VGA AB35
22 CLK_PEG_VGA# CLK_PEG_VGA# AA36
VGA_RST# AA30
VGA_RST# AA30

CLOCK
PCIE_REFCLKP PCIE_REFCLKN
CALIBRATION
VGA_PCIE_CALRP RV2 1 1.27K 0402 1%
VGA_PCIE_CALRN RV3 1 2K 0402 1%
PERSTB

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				Date	Monday, July 04, 2011
				Sheet	12 of 51

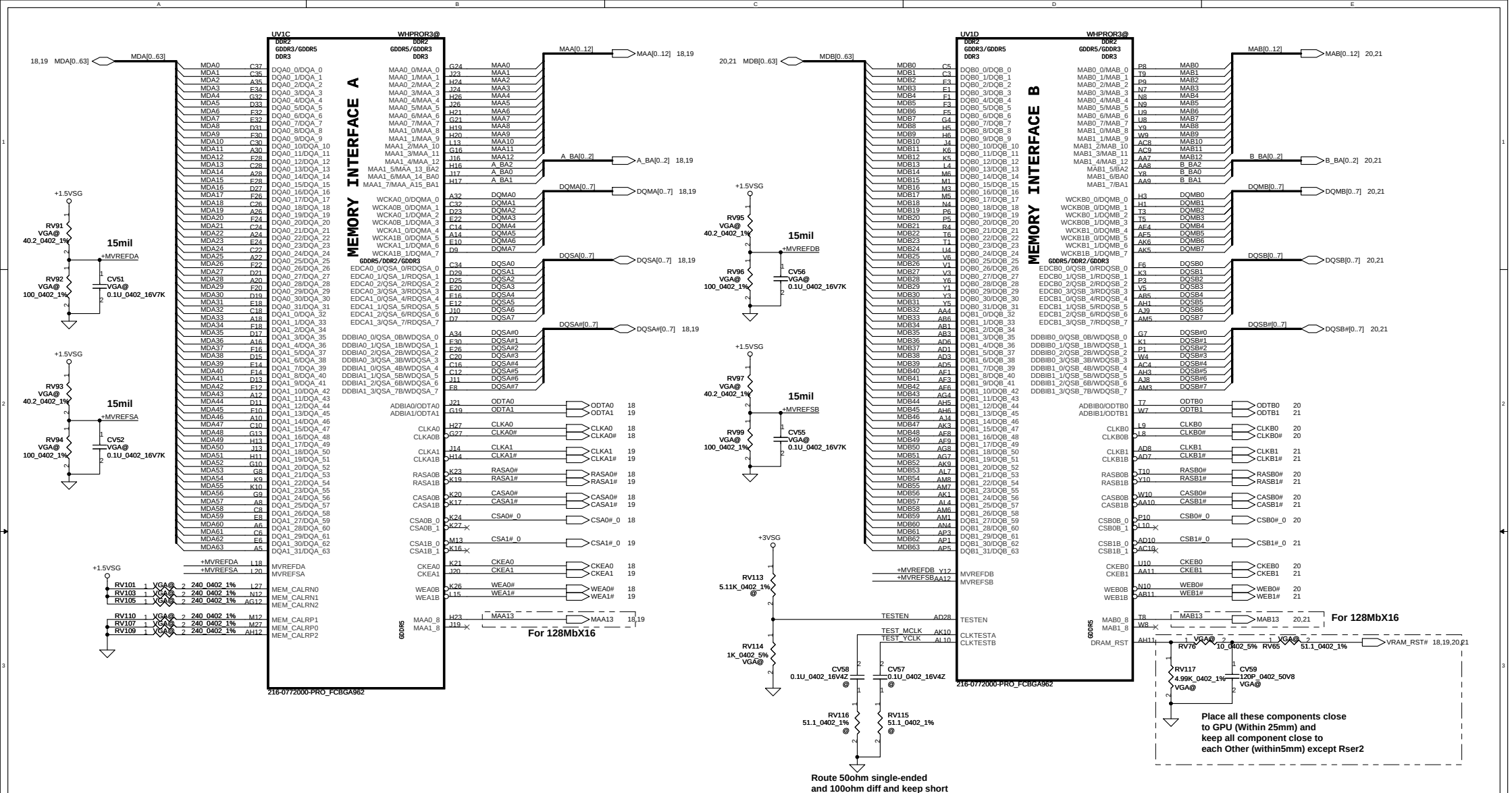
Strap Name	Pin Name	Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN_V2SYN	HSYNC	VIP Device Strap Enable indicates to the software driver (internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines (internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable (internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable (internal PD) 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
CONFIG[2]	GPIO13	GPIO13,12,11 (config 2,1,0) : (internal PD) a) If BIOS_ROM_EN = 1, then Config[3:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	001
CONFIG[1]	GPIO12		
CONFIG[0]	GPIO11		
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device (internal PD) 1: Enable 0: Disable	0
AUD[1]	HSYNC	00: No audio function; 01: Audio for DisplayPort and HDMI if adapter is detected	11
AUD[0]	VSYN	11: Audio for both DisplayPort and HDMI	
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYN	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	NC
	GENLK_CLK		
	GPIO8		
	GPIO21		

Don't have this strap for Whistler

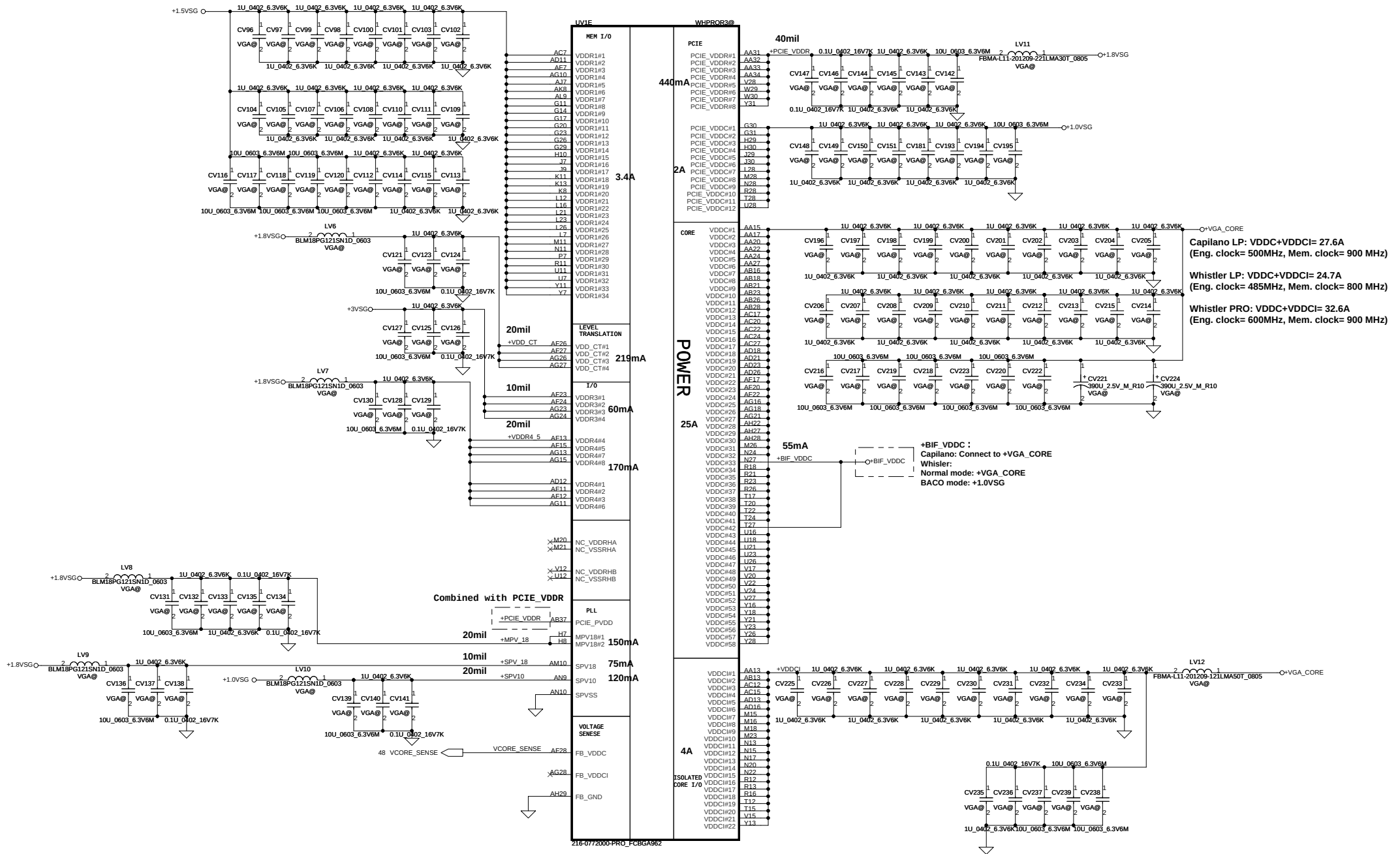


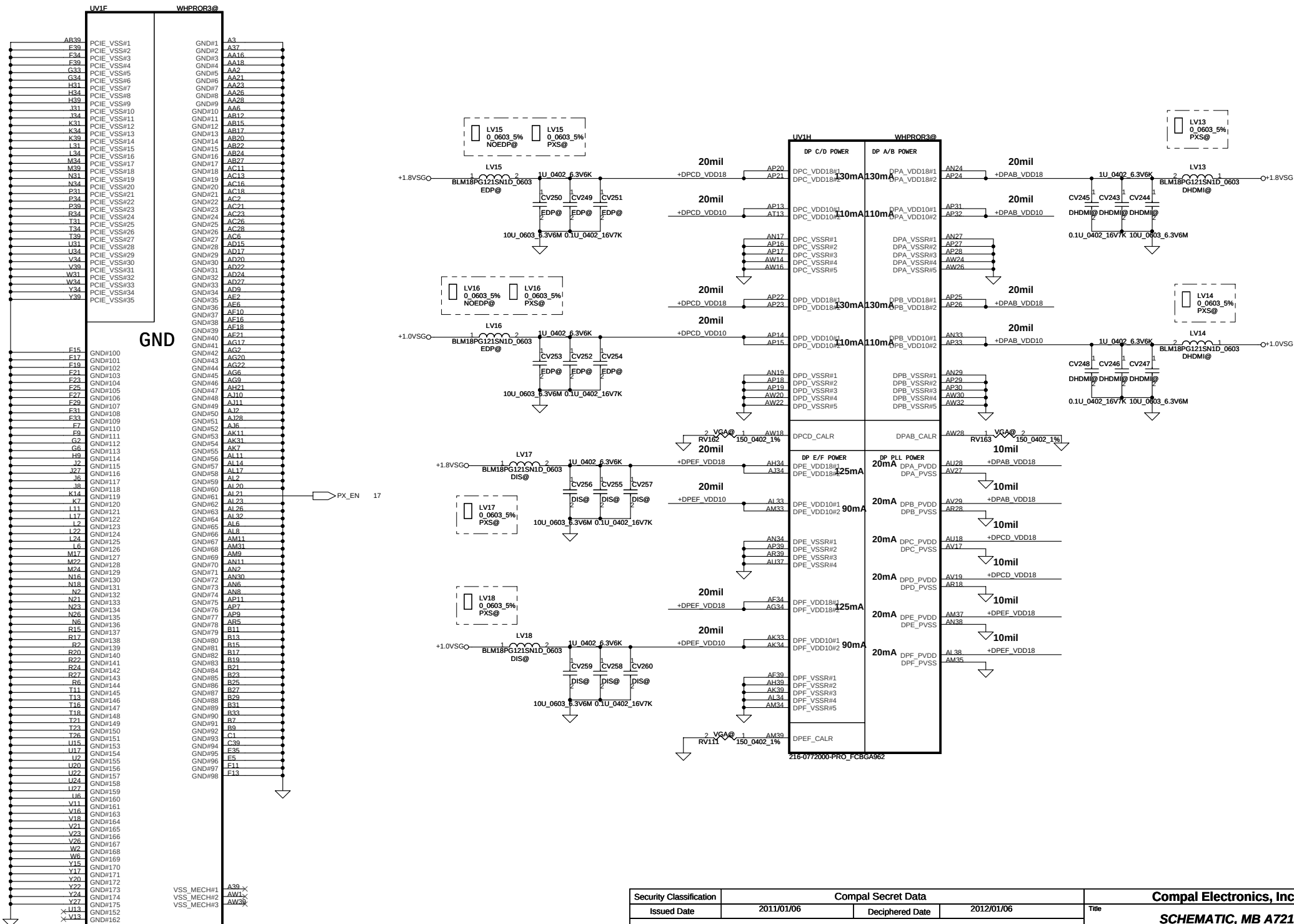
VRAM STRAP						
(VRAM_ID[0:3] internal pull-down)						
Location	DDR3 Type	Part Number	VRAM_ID0	VRAM_ID1	VRAM_ID2	VRAM_ID3
VRAM						
Samsung (1GB)	64Mx16 900MHz	K4W1G1646C-BC11	0	0	0	0
HYNIX (1GB)	64Mx16 900MHz	H5TQ1G3DFR-11C	1	0	0	0
Samsung (2GB)	128Mx16 900MHz	K4W2G1646C-HC11	0	1	0	0
HYNIX (2GB)	128Mx16 900MHz	H5TQ2G63BFR-11C	1	1	0	0

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		Date		Monday, July 04, 2011	
		Sheet		13 of 51	

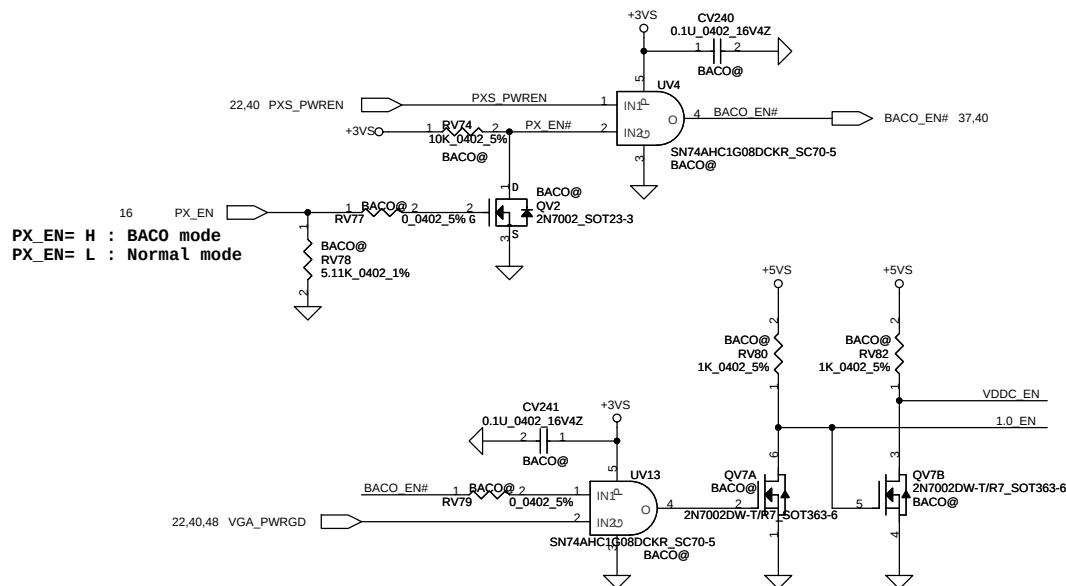


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				Date	Monday, July 04, 2011
				Sheet	14 of 51



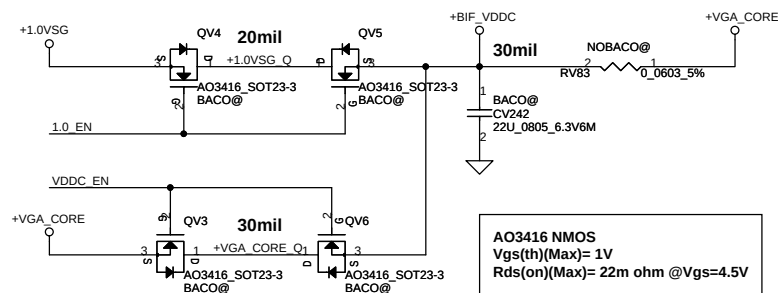


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				Date: Monday, July 04, 2011	Sheet 16 of 51



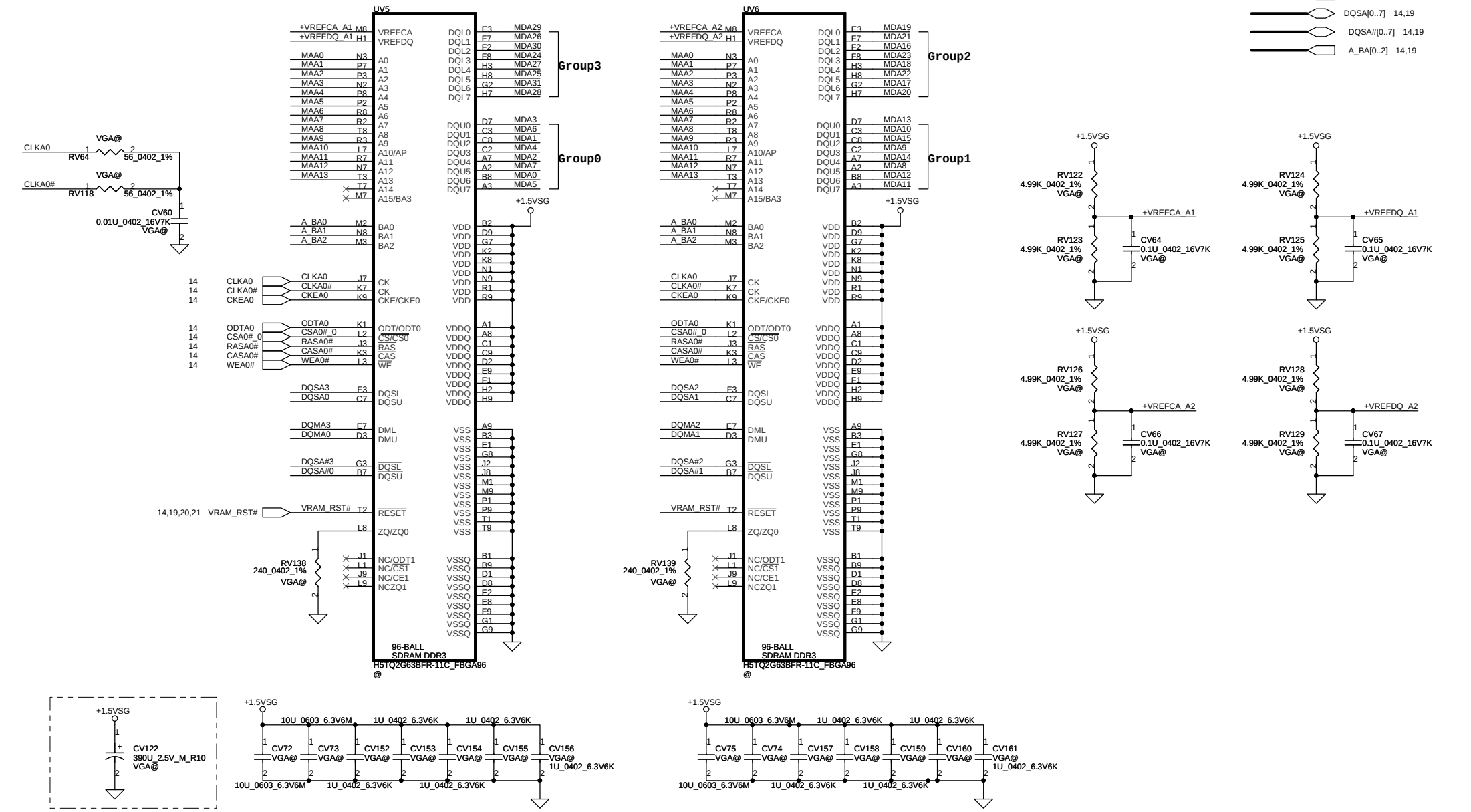
BACO mode:
+VGA_CORE: off
+1.5VSG: off
+BIF_VDDC= +1.0VSG

Normal mode:
+BIF_VDDC= +VGA_CORE



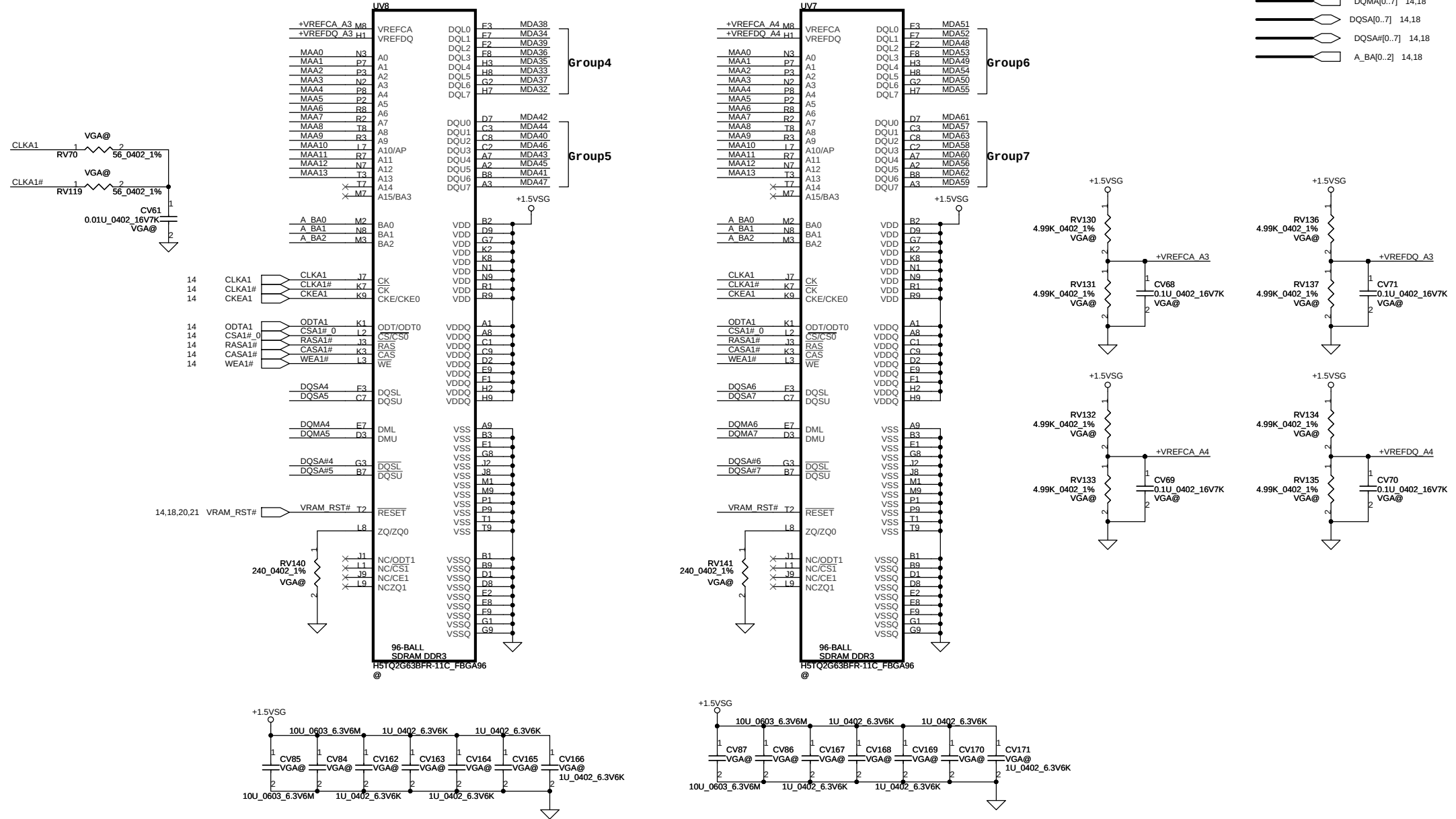
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				Date	Monday, July 04, 2011
				Sheet	17 of 51

Memory Partition A - Lower 32 bits



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				Rev	B
				Date	Monday, July 04, 2011
				Sheet	18 of 51

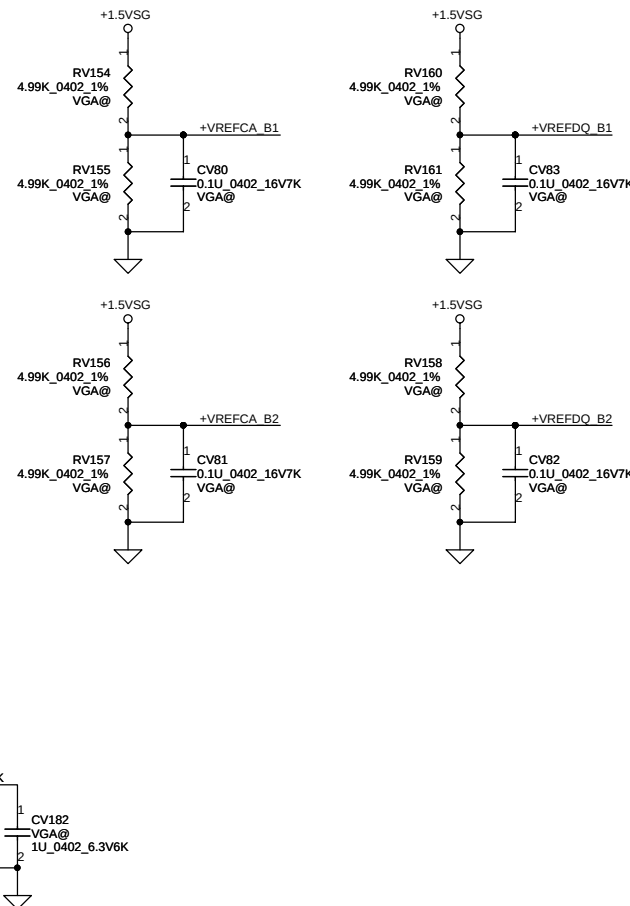
Memory Partition A - Upper 32 bits



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				Rev	B
				Date:	Monday, July 04, 2011
				Sheet	19 of 51

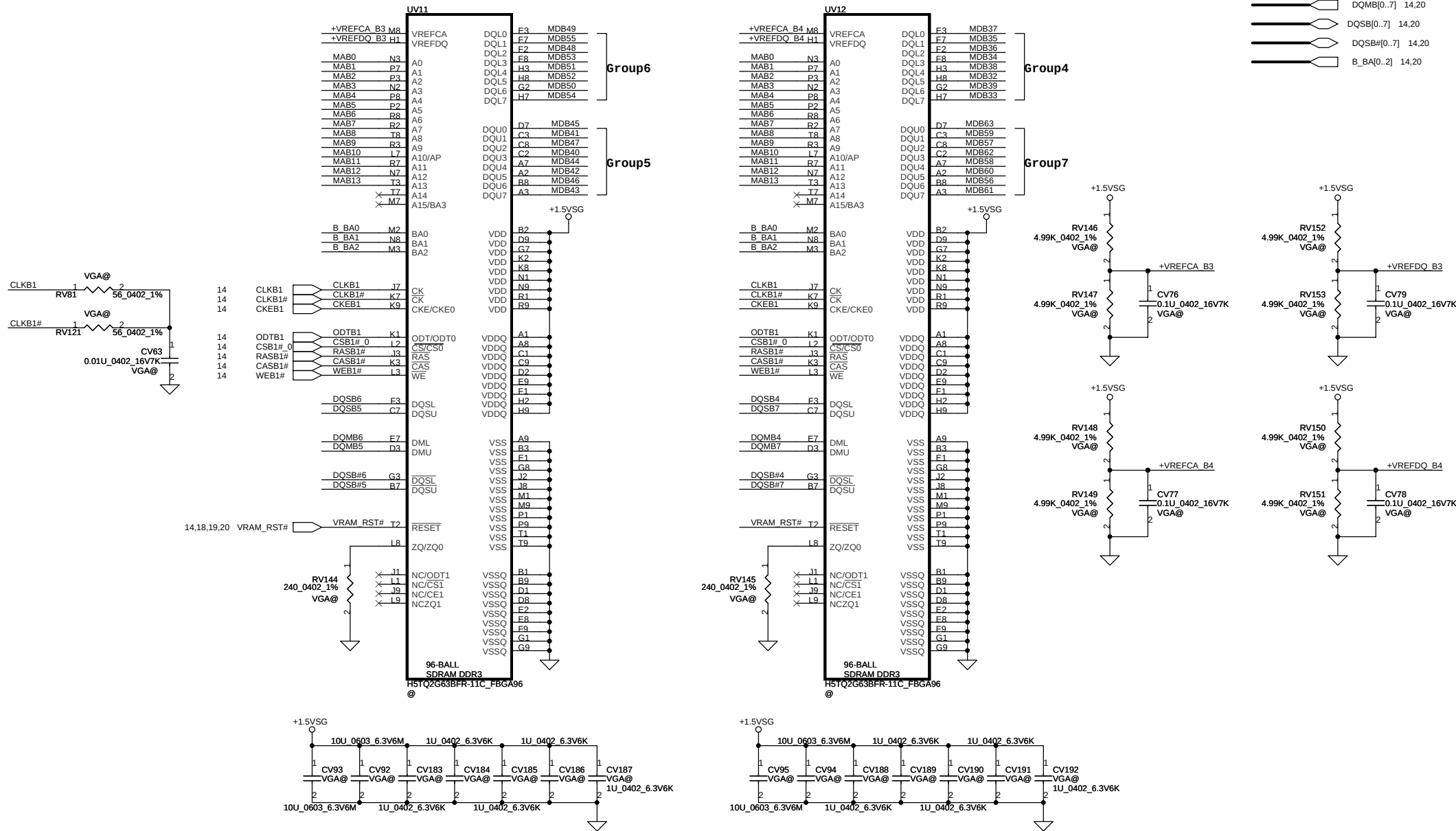
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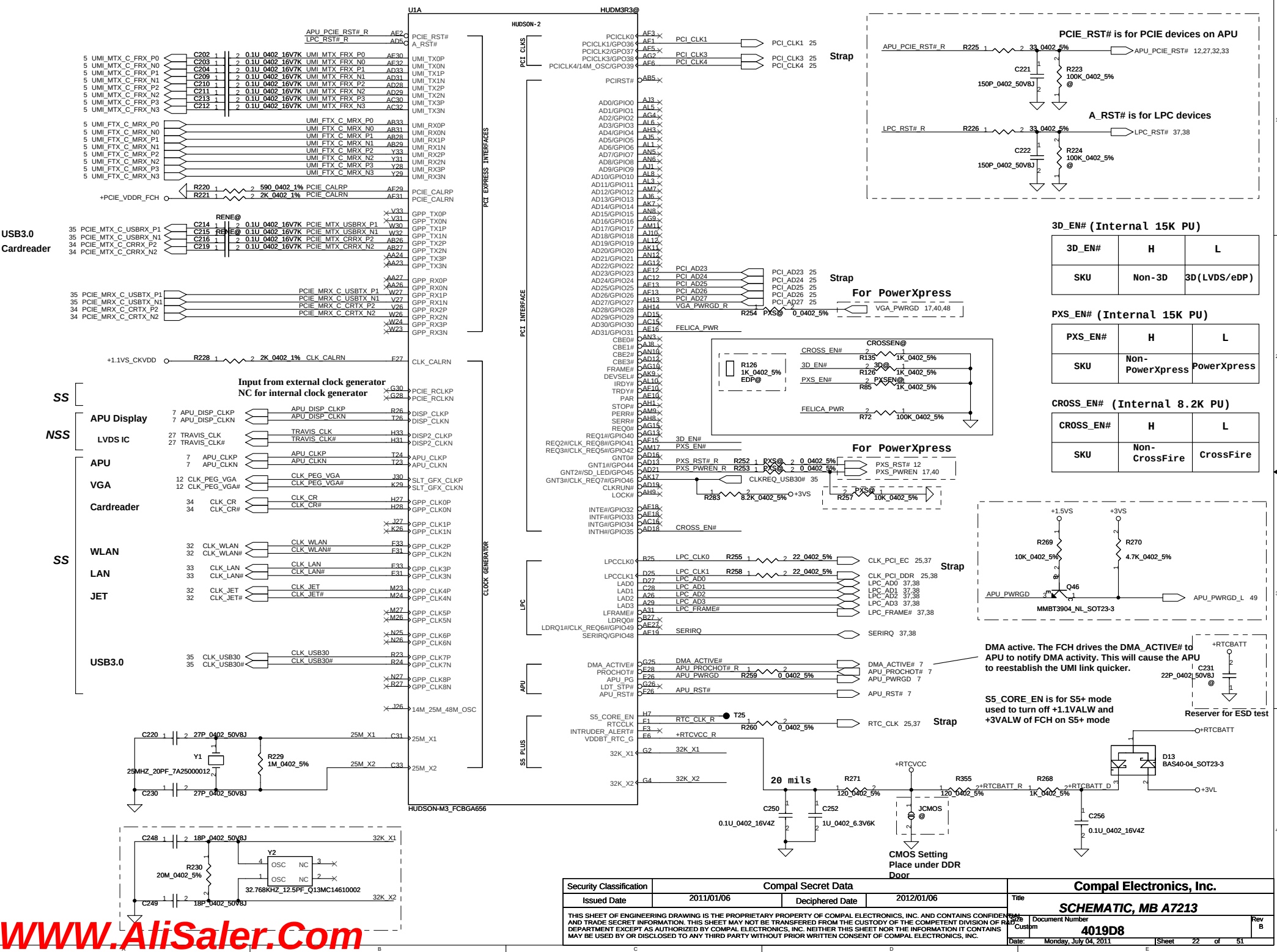


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				Custom	4019D8	B
				Date:	Monday, July 04, 2011	Sheet 20 of 51

Memory Partition C - Upper 32 bits



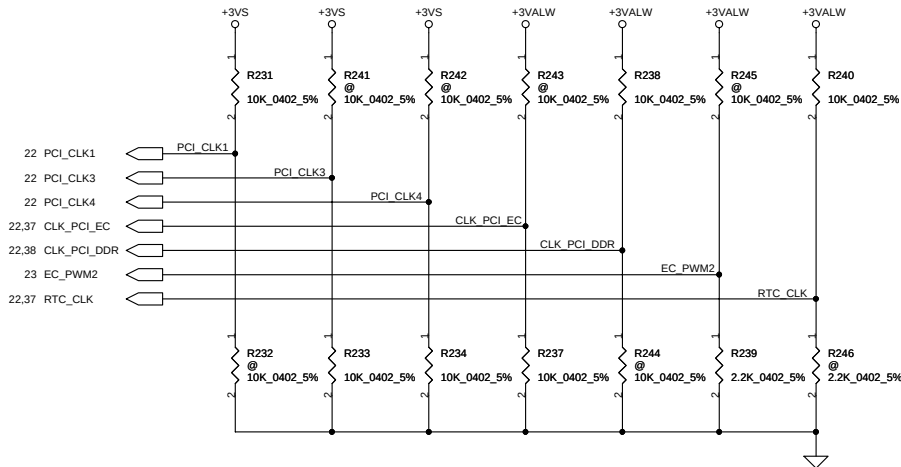
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						Date:		Monday, July 04, 2011		Sheet	





STRAP PINS

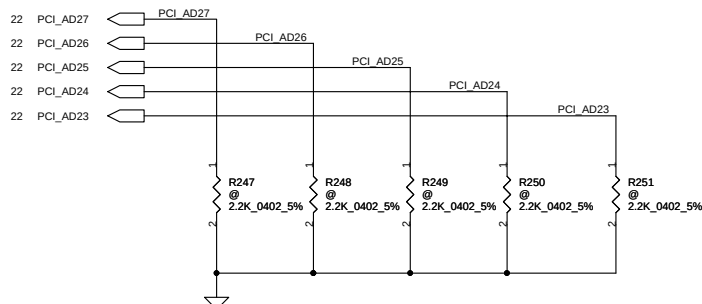
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	ENABLE DEBUG STRAP	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM (INTERNAL 10K PULL-UP)	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	DISABLE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



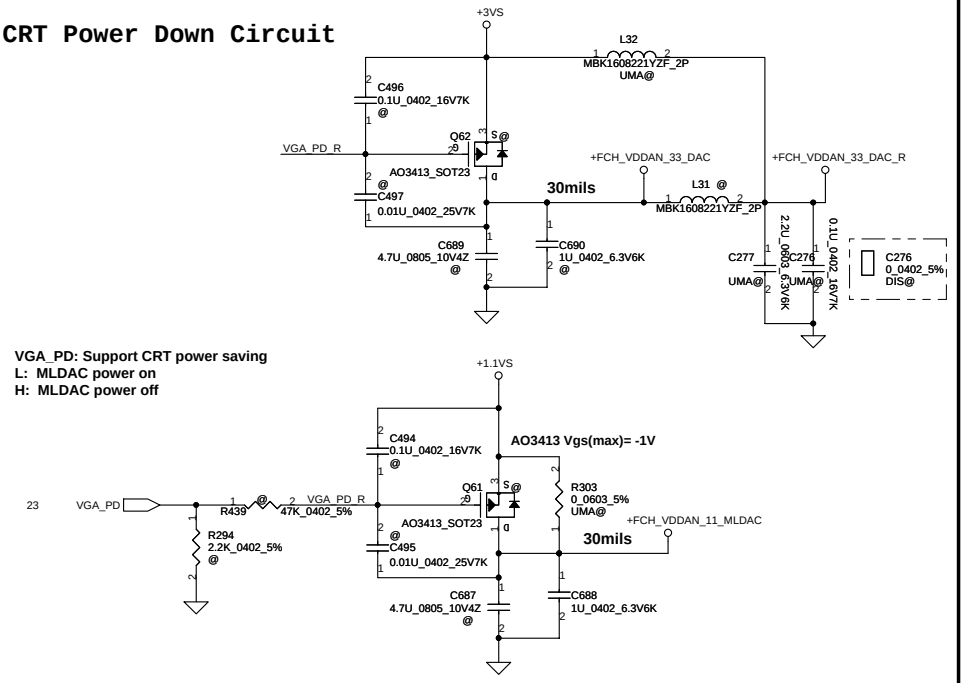
DEBUG STRAPS

FCH HAS 15K INTERNAL PU-UP FOR PCI_AD[27:23]

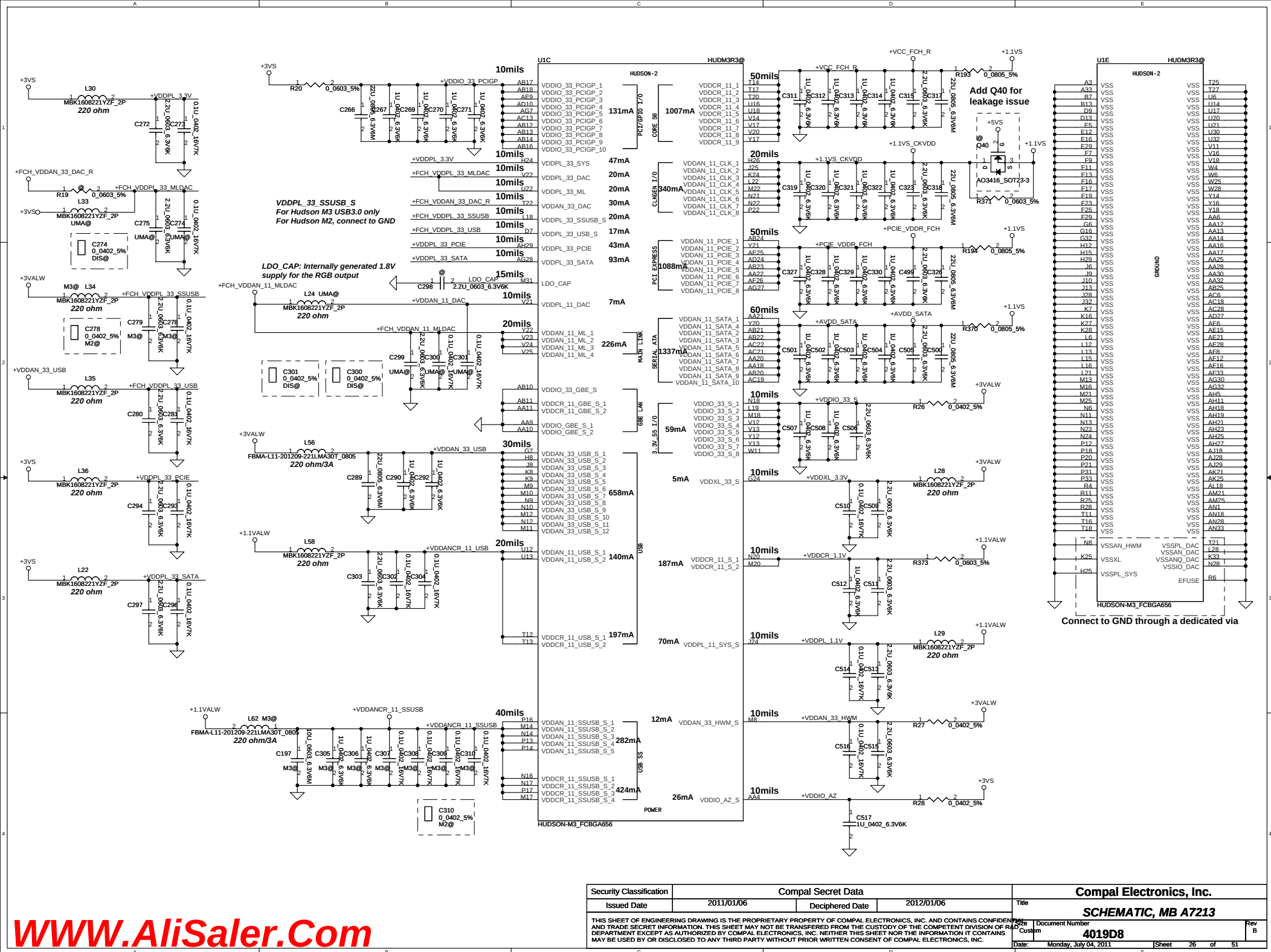
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

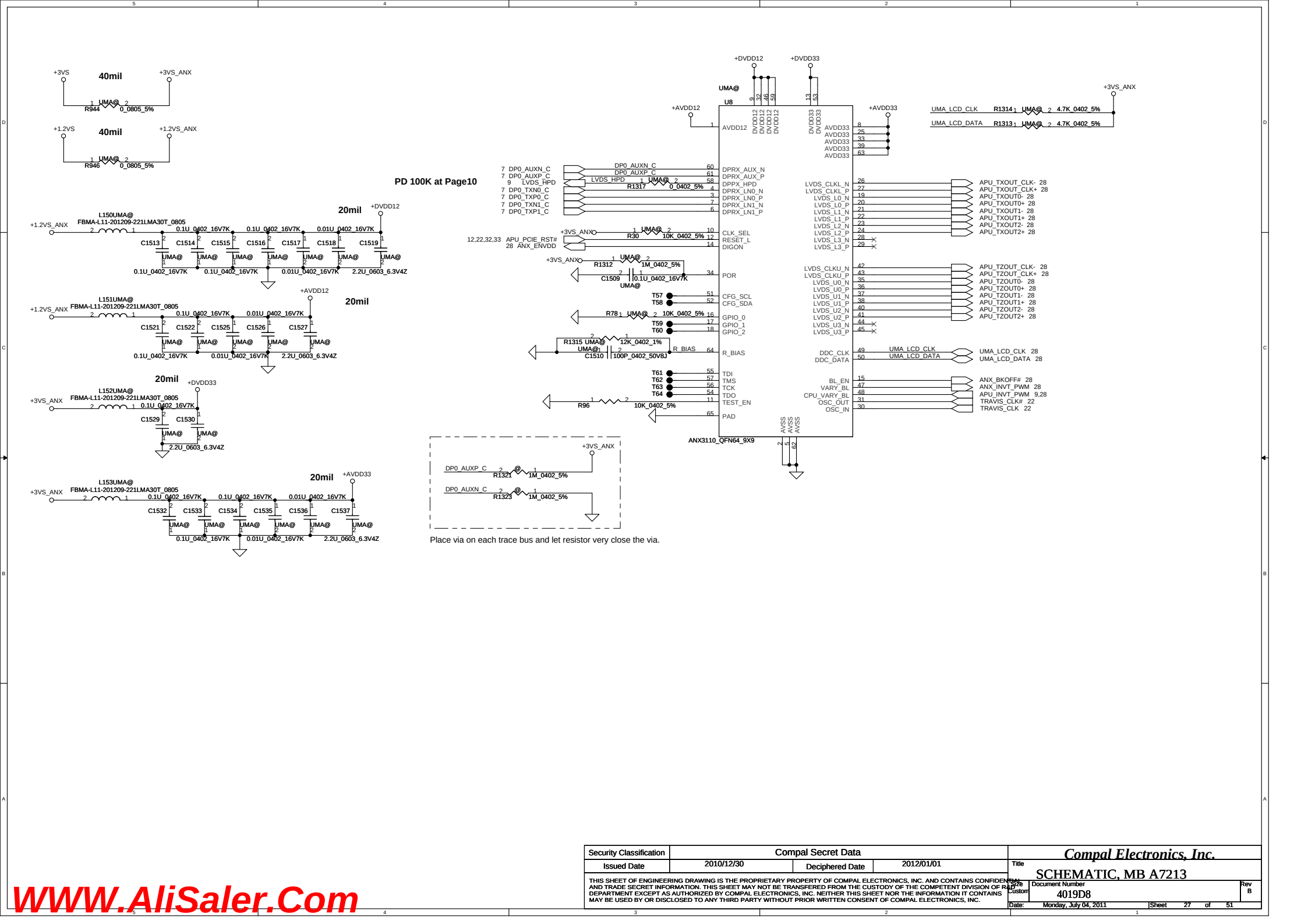


CRT Power Down Circuit



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				Date	Monday, July 04, 2011
				Sheet	25 of 51





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				Document Number	4019D8
				Date	Monday, July 04, 2011
				Sheet	27 of 51

27	APU_TXOUT0+		1 UMA@ 2 RD262 0 0402_5%	LVDS TXOUT0+
27	APU_TXOUT0-		1 UMA@ 2 RD263 0 0402_5%	LVDS TXOUT0-
27	APU_TXOUT1+		1 UMA@ 2 RD265 0 0402_5%	LVDS TXOUT1+
27	APU_TXOUT1-		1 UMA@ 2 RD264 0 0402_5%	LVDS TXOUT1-
27	APU_TXOUT2+		1 UMA@ 2 RD298 0 0402_5%	LVDS TXOUT2+
27	APU_TXOUT2-		1 UMA@ 2 RD277 0 0402_5%	LVDS TXOUT2-
27	APU_TXOUT_CLK+		1 UMA@ 2 RD291 0 0402_5%	LVDS TXCLK+
27	APU_TXOUT_CLK-		1 UMA@ 2 RD296 0 0402_5%	LVDS TXCLK-
27	APU_TZOUT0+		1 UMA@ 2 RD268 0 0402_5%	LVDS TZOUT0+
27	APU_TZOUT0-		1 UMA@ 2 RD267 0 0402_5%	LVDS TZOUT0-
27	APU_TZOUT1+		1 UMA@ 2 RD269 0 0402_5%	LVDS TZOUT1+
27	APU_TZOUT1-		1 UMA@ 2 RD266 0 0402_5%	LVDS TZOUT1-
27	APU_TZOUT2+		1 UMA@ 2 RD302 0 0402_5%	LVDS TZOUT2+
27	APU_TZOUT2-		1 UMA@ 2 RD276 0 0402_5%	LVDS TZOUT2-
27	APU_TZOUT_CLK+		1 UMA@ 2 RD301 0 0402_5%	LVDS TZCLK+
27	APU_TZOUT_CLK-		1 UMA@ 2 RD303 0 0402_5%	LVDS TZCLK-
27	UMA_LCD_CLK		1 UMA@ 2 RD300 0 0402_5%	LVDS EDID CLK
27	UMA_LCD_DATA		1 UMA@ 2 RD299 0 0402_5%	LVDS EDID DATA
9,27	APU_INV_T_PWM		RD332 0 0402_5%	LED PWM
9	APU_ENVDD		1 ② 2 RD350 0 0402_5%	LCD ENVDD
9	APU_ENBKL		1 ② 2 RD357 0 0402_5%	EC ENBKL

EC_ENBKL 37

For DISCRETE

12 VGA_INV_T_PWM   1 Dis0 2 0.0402_5% LED_PWM

12 VGA_ENVDD   1 Dis0 2 0.0402_5% LCD_ENVDD

12 VGA_ENBKL   1 Dis0 2 0.0402_5% EC_ENBKL

Close to LVDS Connector

Remove DISCRETE for 3D LVDS Panel

Remove 3D LVDS Panel

		EDP ₀	
13	VGA_EDP_TX0+	CD880	0.1U 0402 16V7K LVDS TXOUT0+
13	VGA_EDP_TX0-	CD881	0.1U 0402 16V7K LVDS TXOUT0-
13	VGA_EDP_TX1+	CD882	0.1U 0402 16V7K LVDS TXOUT1+
13	VGA_EDP_TX1-	CD883	0.1U 0402 16V7K LVDS TXOUT1-
13	VGA_EDP_TX2+	CD884	0.1U 0402 16V7K LVDS TXOUT2+
13	VGA_EDP_TX2-	CD885	0.1U 0402 16V7K LVDS TXOUT2-
13	VGA_EDP_TX3+	CD886	0.1U 0402 16V7K LVDS TXCLK+
13	VGA_EDP_TX3-	CD887	0.1U 0402 16V7K LVDS TXCLK-

Close to LVDS1 Connector

13 VGA_EDP_AUX+  CD888 1 | | 0.1U 0402 16V7K LVDS EDID_CLK

13 VGA_EDP_AUX-  CD889 1 | | 0.1U 0402 16V7K LVDS EDID_DATA

37

BKOFF#

LED_PWM

LED_PWM_D

BKOFF#_D

RD449

RD30

RB751V40_SC76-2

RB751V40_SC76-2

RD144

RD113

47K_0402_5%

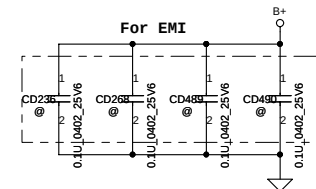
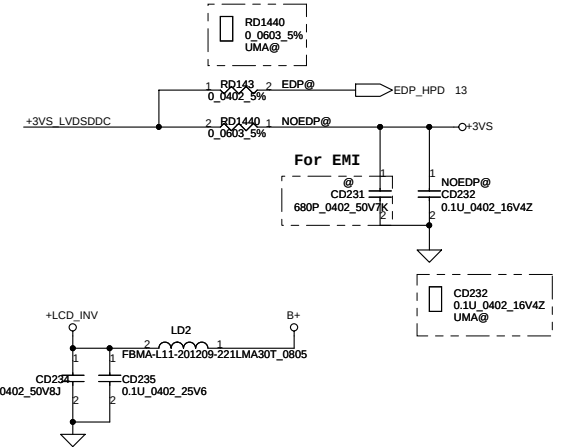
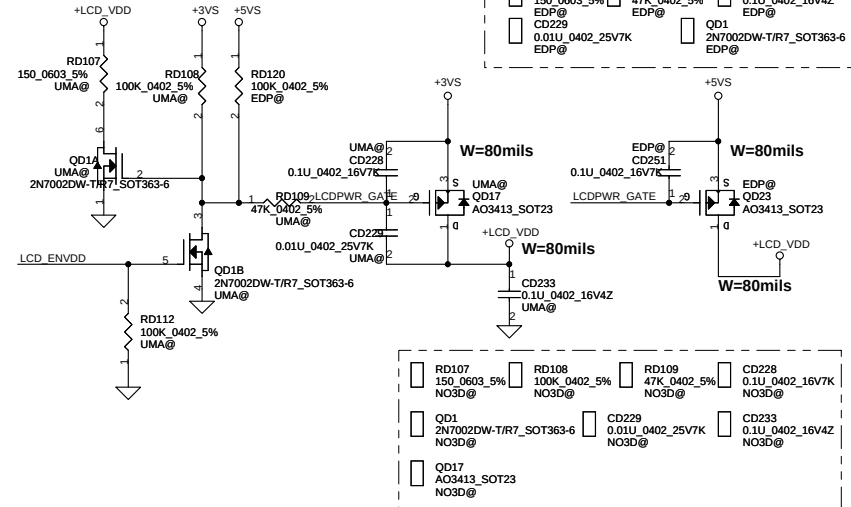
10K_0402_5%

Figure 1: Block diagram of the USB2.0 PHY. The diagram shows a USB2.0 PHY block with four pins: USB20_N5, USB20_P5, USB20_N5_R, and USB20_P5_R. The block contains two transceivers, each with a driver and a receiver. The driver pins are labeled RD78 and RD96, and the receiver pins are labeled D55 and D56. The block is labeled 'WCM-2012-900T_0805'.

37 INVT_PWM 1 RD387 @ 2 LED_PWM
0_0402_5%

[illegible]

27	ANX_INV_T_PWM		1	UMA@	2	LED_PWM
			RD333	0_0402_5%		
27	ANX_ENVDD		1	UMA@	2	LCD_ENVDD
			RD351	0_0402_5%		
27	ANX_BKOFF#		1	UMA@	2	EC_ENBKL
			RD360	0_0402_5%		



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For UMA & PowerXpress

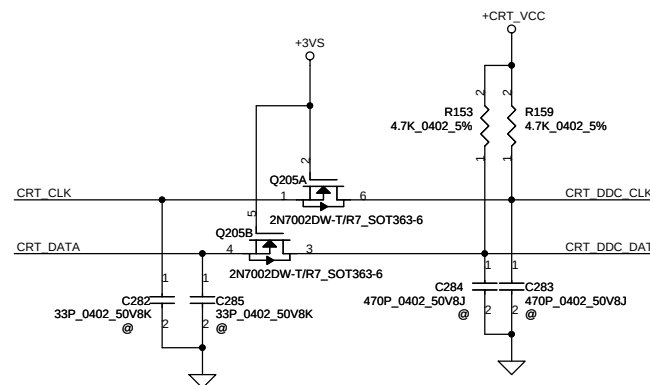
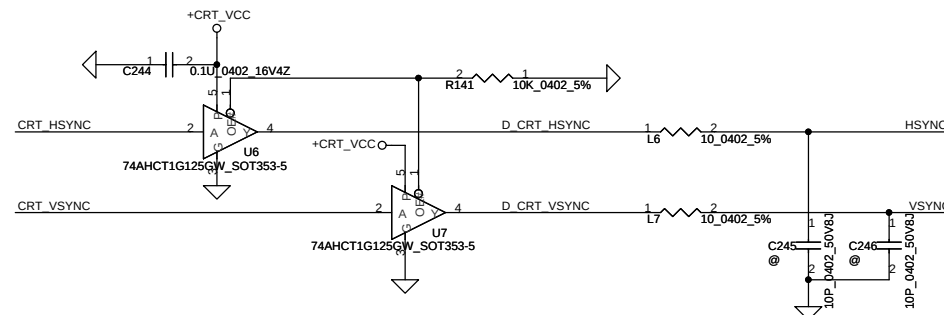
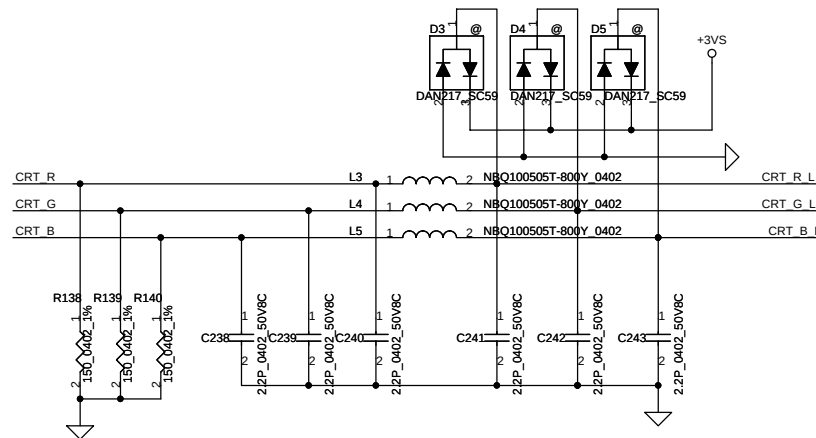
24	UMA_CRT_R	1	UMA	2	CRT_R
		R200	0.0402_5%		
24	UMA_CRT_G	1	UMA	2	CRT_G
		R204	0.0402_5%		
24	UMA_CRT_B	1	UMA	2	CRT_B
		R211	0.0402_5%		
24	UMA_CRT_HSYNC	1	UMA	2	CRT_HSYNC
		R213	0.0402_5%		
24	UMA_CRT_VSYNC	1	UMA	2	CRT_VSYNC
		R235	0.0402_5%		
24	UMA_CRT_CLK	1	UMA	2	CRT_CLK
		R236	0.0402_5%		
24	UMA_CRT_DATA	1	UMA	2	CRT_DATA
		R261	0.0402_5%		

Close to CRT Connector

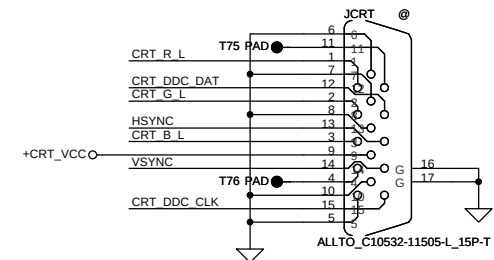
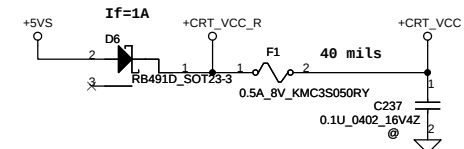
For DISCRETE

13	VGA_CRT_R	1	DIS	2	CRT_R
		R178	0.0402_5%		
13	VGA_CRT_G	1	DIS	2	CRT_G
		R181	0.0402_5%		
13	VGA_CRT_B	1	DIS	2	CRT_B
		R167	0.0402_5%		
13	VGA_CRT_HSYNC	1	DIS	2	CRT_HSYNC
		R177	0.0402_5%		
13	VGA_CRT_VSYNC	1	DIS	2	CRT_VSYNC
		R179	0.0402_5%		
13	VGA_CRT_CLK	1	DIS	2	CRT_CLK
		R209	0.0402_5%		
13	VGA_CRT_DATA	1	DIS	2	CRT_DATA
		R256	0.0402_5%		

Close to CRT Connector

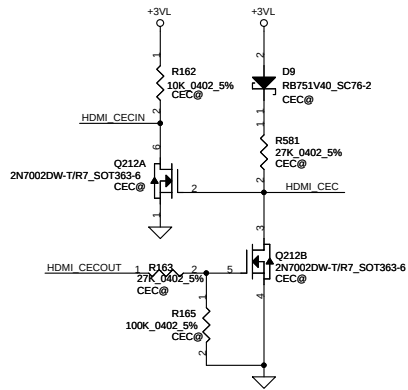


CRT CONNECTOR

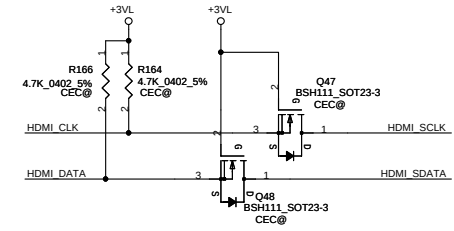
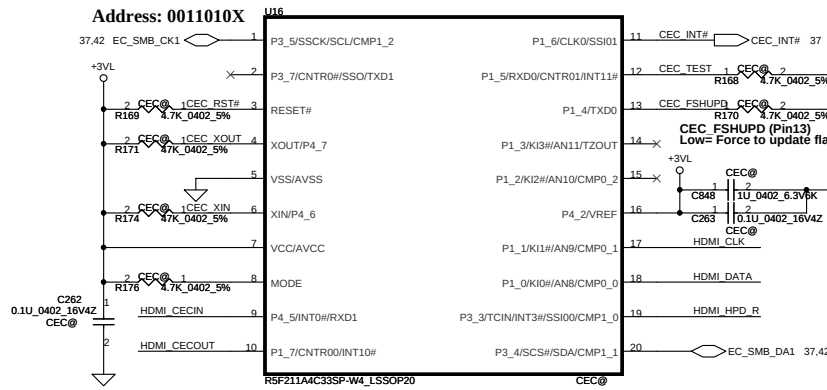


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				Date	Monday, July 04, 2011
				Sheet	29 of 51

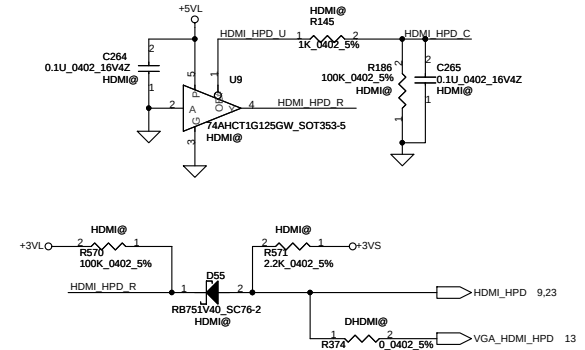
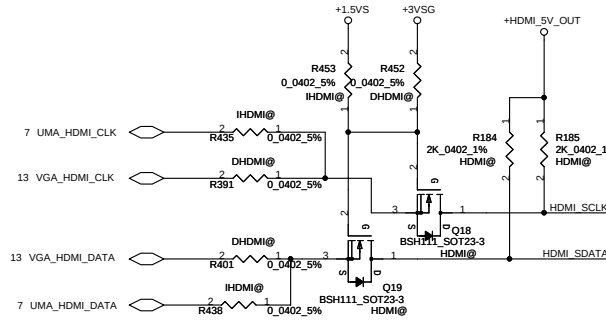
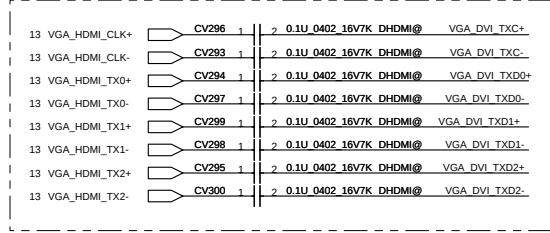
HDMI CEC Controller



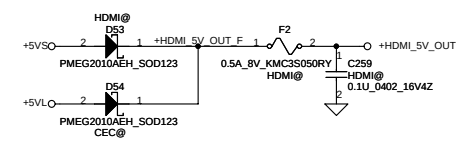
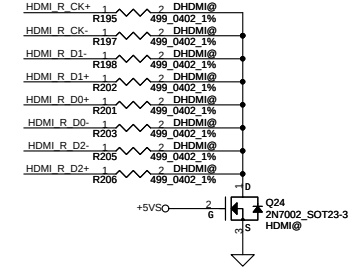
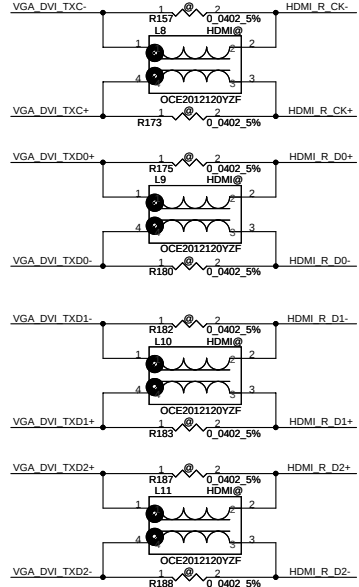
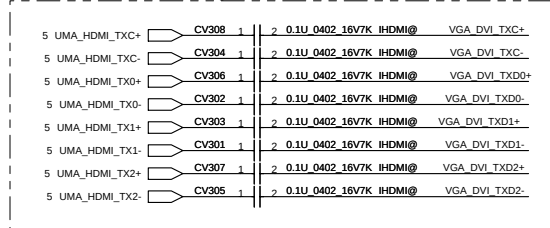
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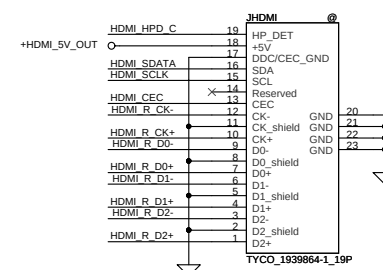
For DISCRETE



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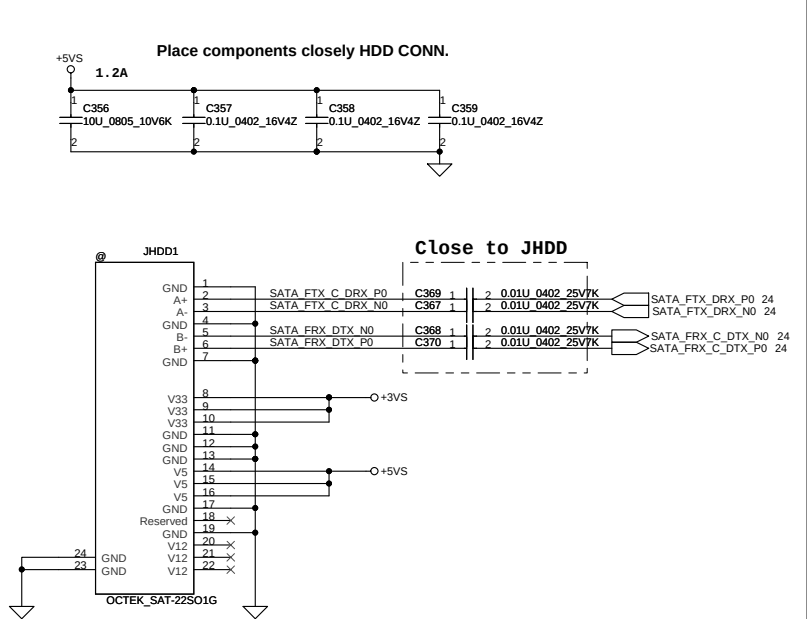


HDMI Connector

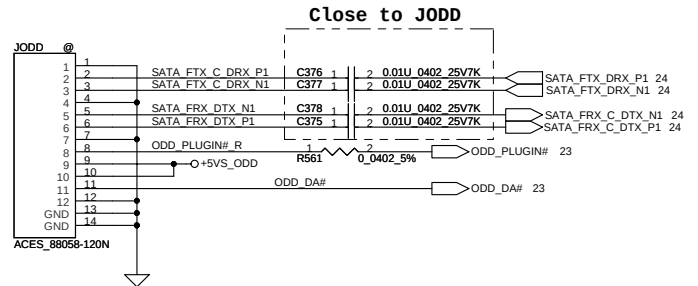


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				Sheet	30 of 51

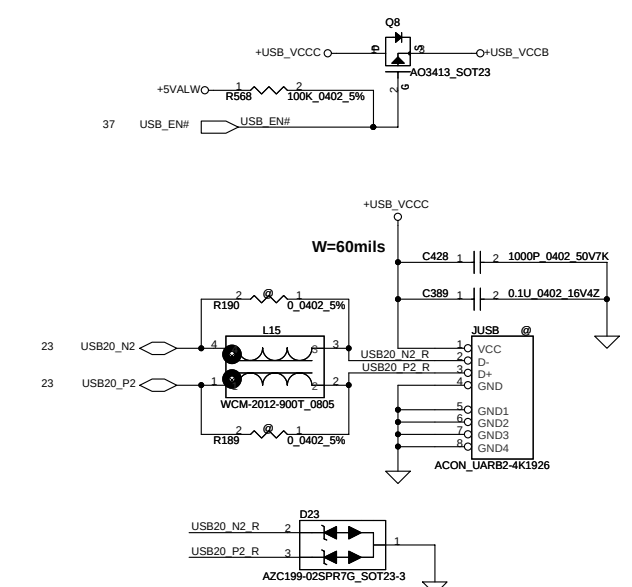
SATA HDD Conn.



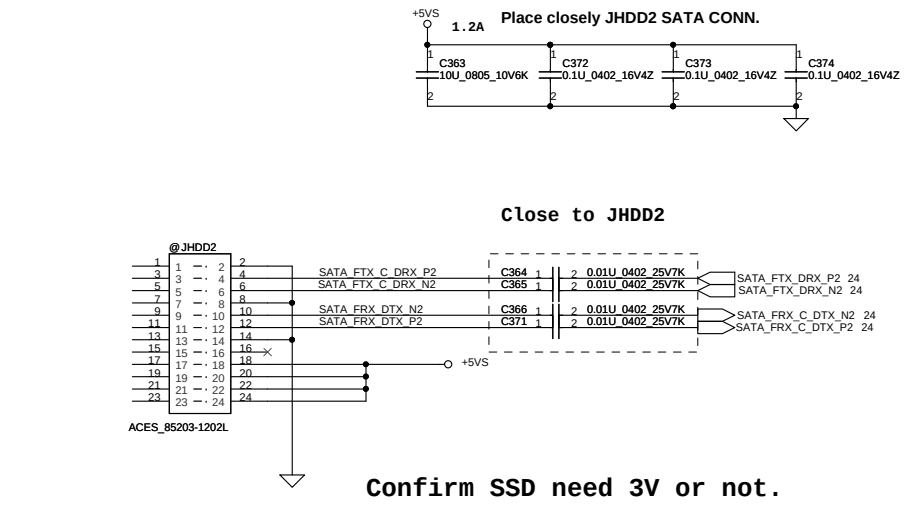
SATA ODD Conn.



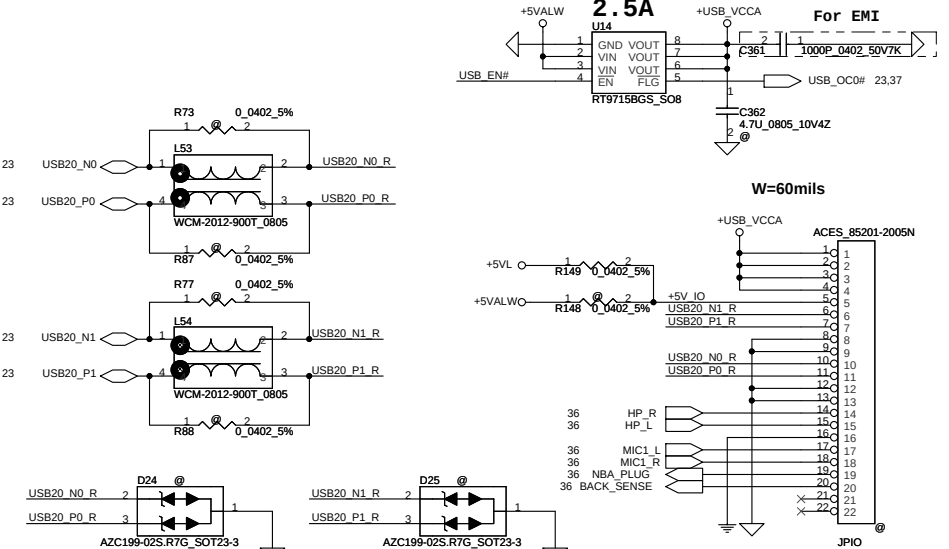
USB Board@ Left Side



SATA 2nd HDD Conn.

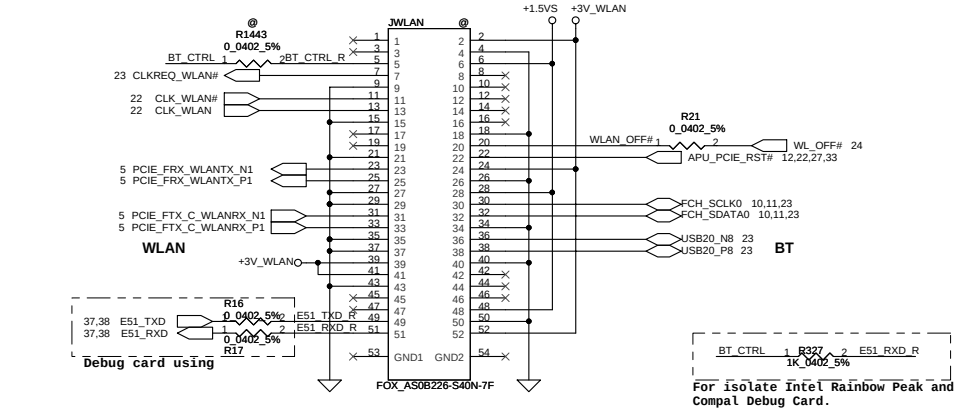
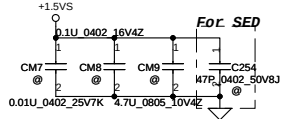
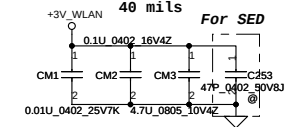
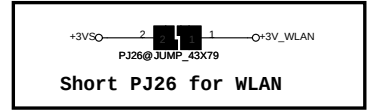


USB Board@ Right Side

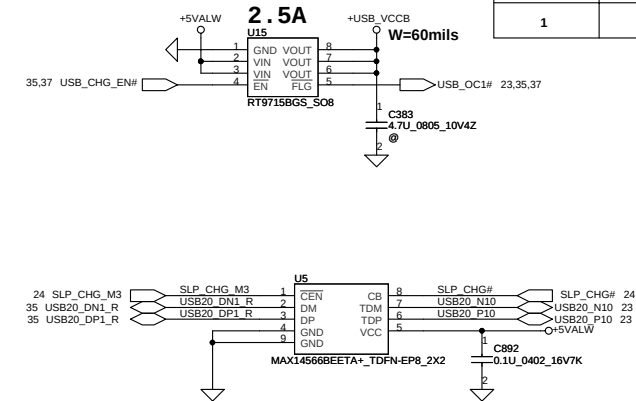


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					4019D8
				Date	Monday, July 04, 2011
				Sheet	31 of 51

Slot 1 Half PCIe Mini Card-WLAN

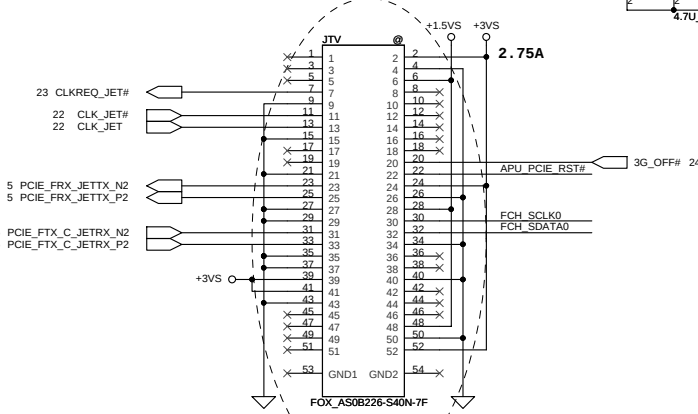


USB Sleep & Charge: Auto-Mode Mode3

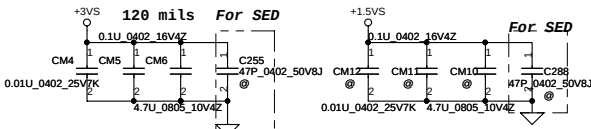


Slot 2 Half PCIe Mini Card- JET

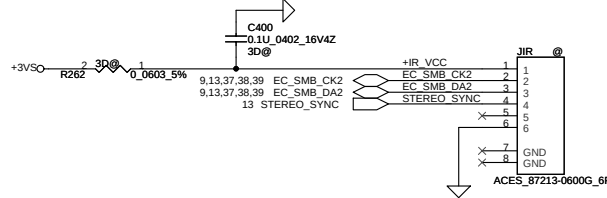
Remove 3G/TV tuner



Need to double check JET pin define

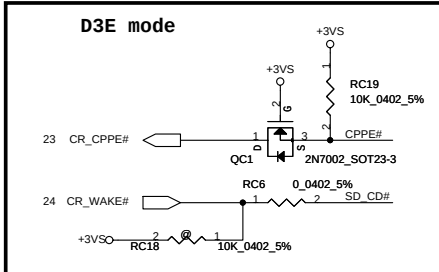
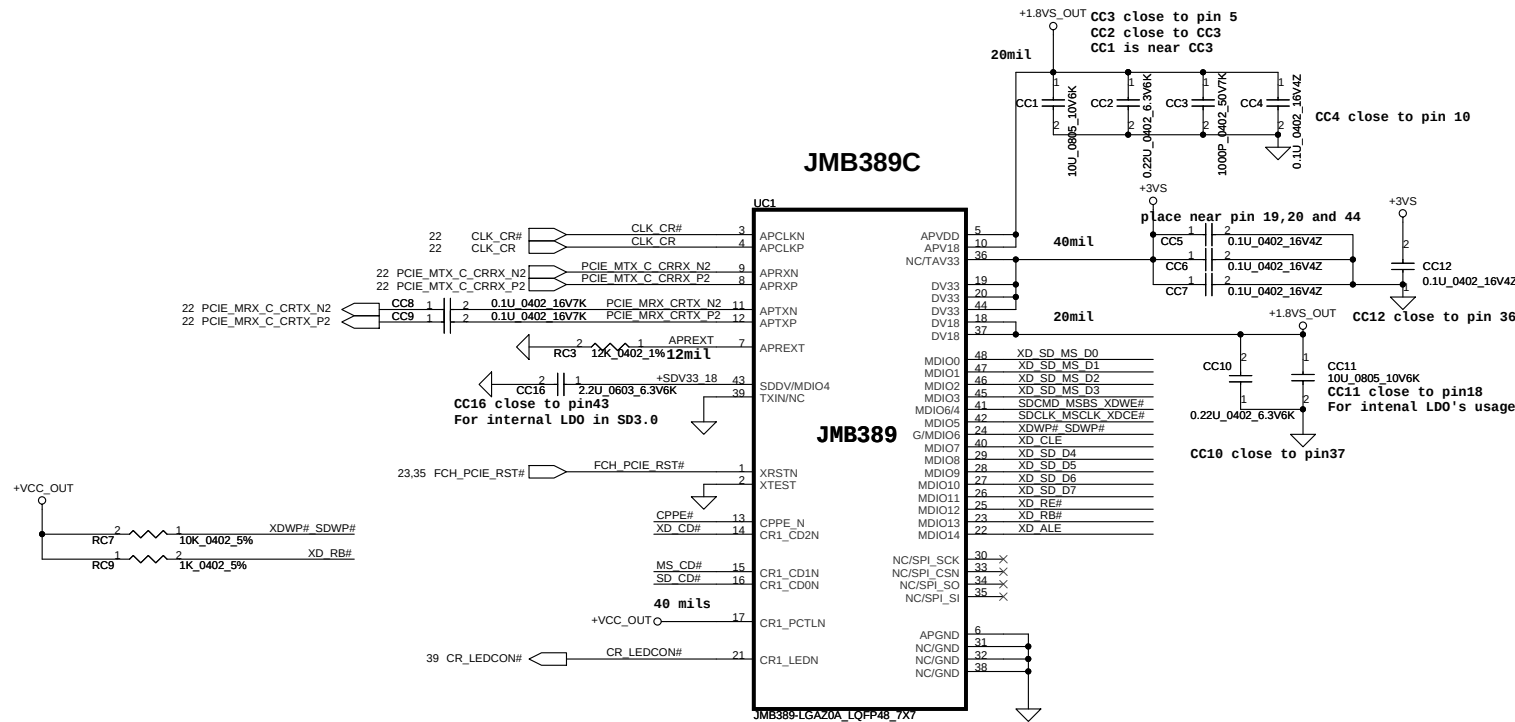


IR Emitter Connector



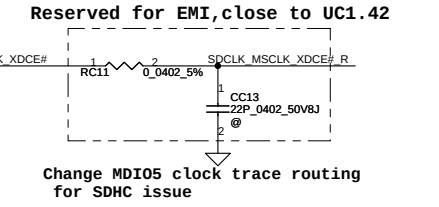
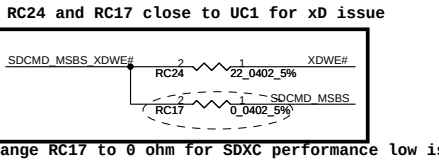
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4019D8				Rev B
Monday, July 04, 2011				Sheet 32 of 51





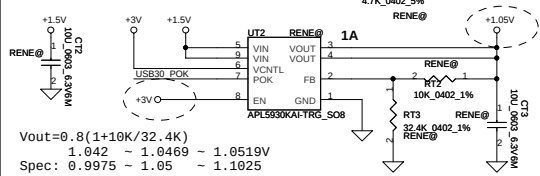
Power On Strapping setting

Pin name	Description	
	High	Low
MDIO7	on-board★	add-in card
MDIO14	CR_LEDON# high active	CR_LEDON# low active★

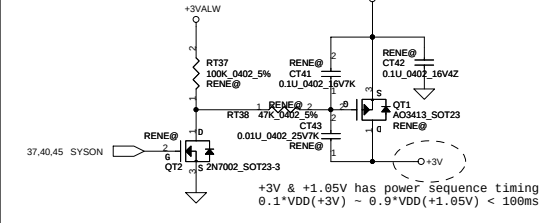


Change MDIO5 clock trace routing for SDHC issue

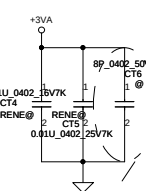
+1.5V to +1.05V Transfer



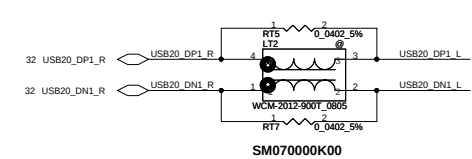
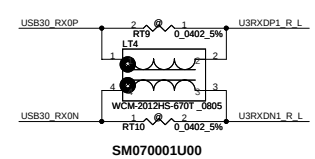
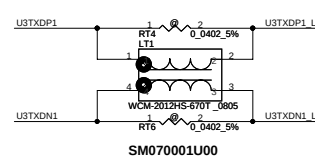
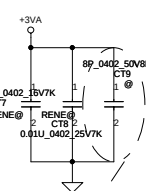
+3VALW to +3V Transfer



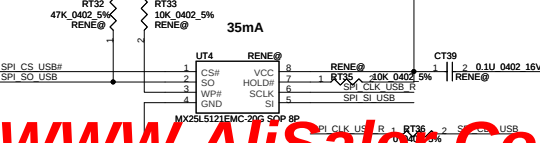
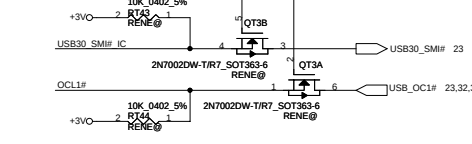
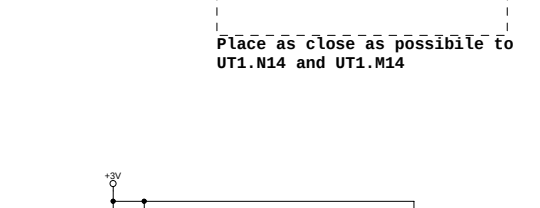
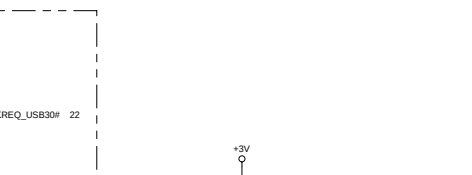
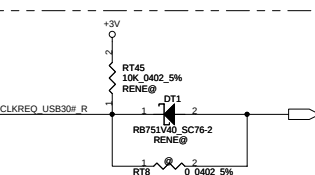
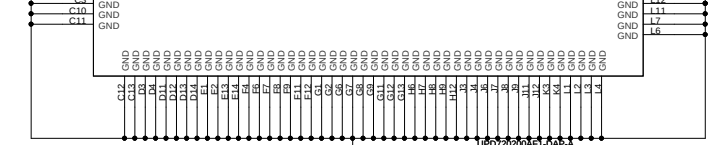
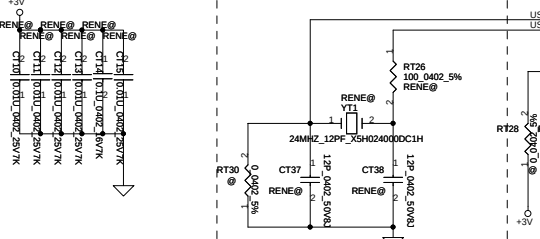
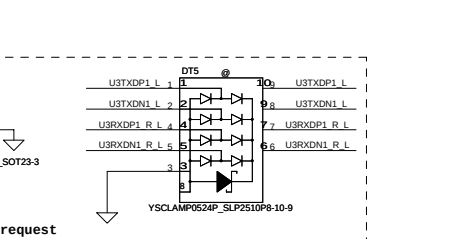
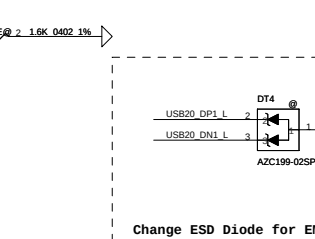
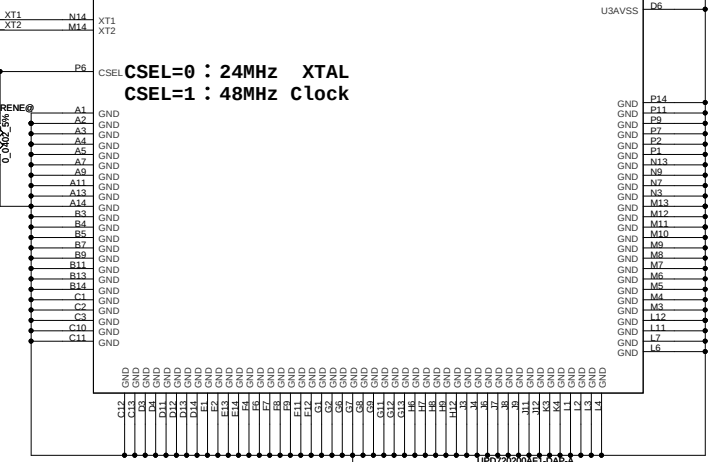
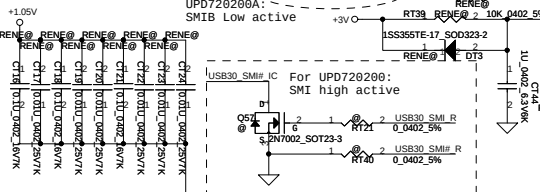
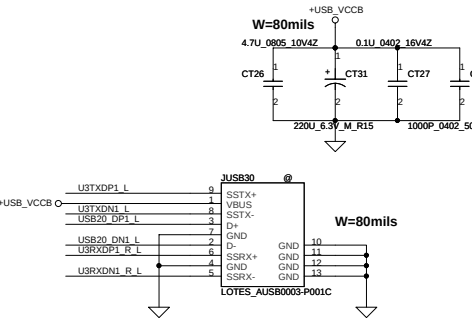
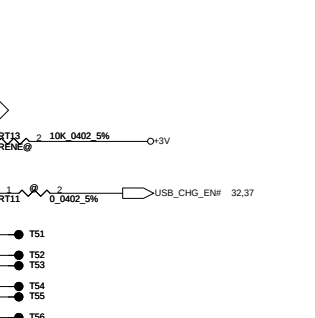
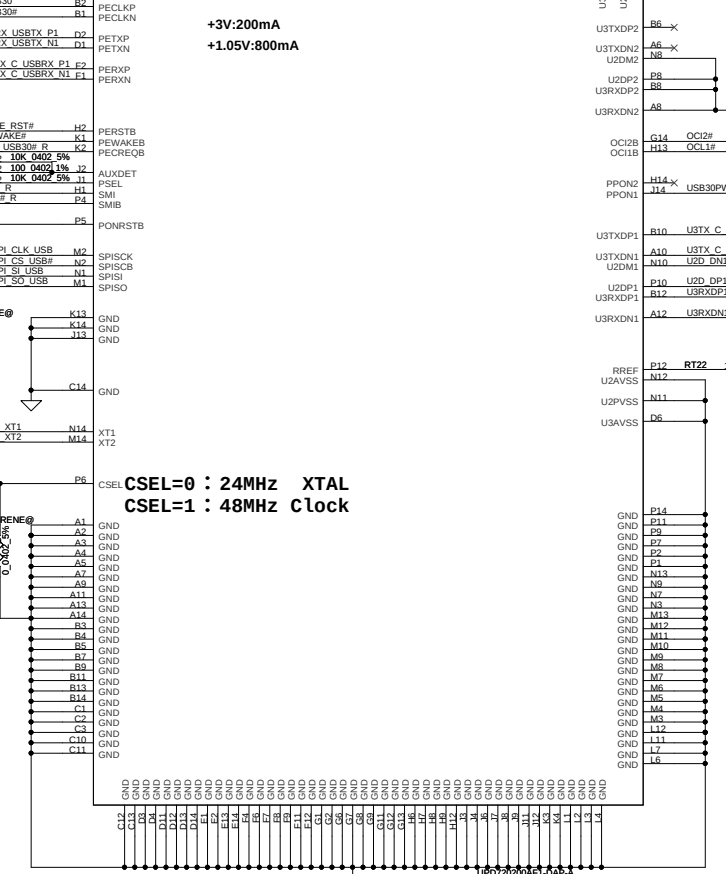
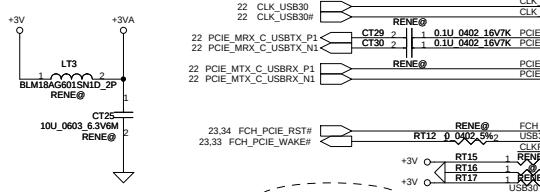
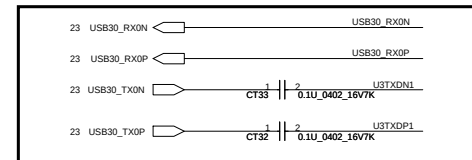
Close to U102.D7



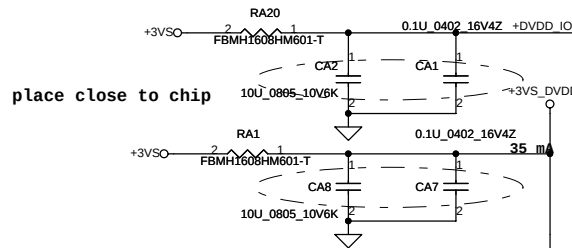
Close to U102.P13



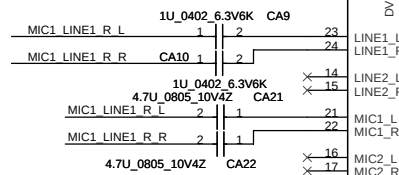
Co-Layout with Hudson M3 internal USB3.0 Place co-layout resistors close to UT1



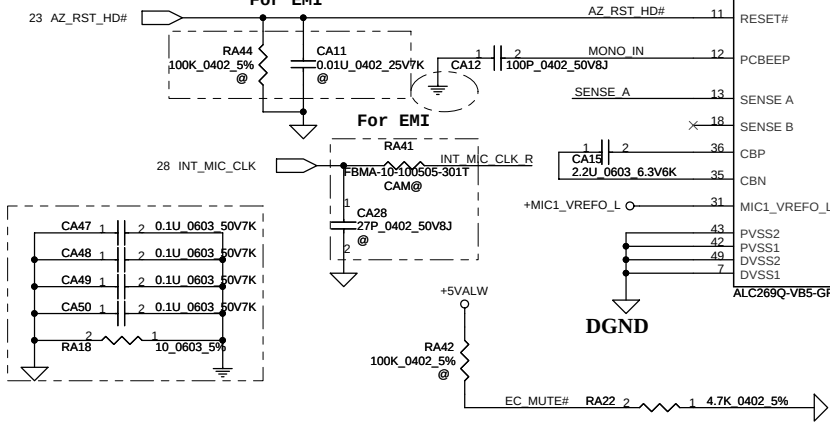
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		2012/01/06	
2011/01/06		2012/01/06		Compal Electronics, Inc.	
2012/01/06		2012/01/06		SCHEMATIC, MB A7213	
2012/01/06		2012/01/06		4019D8	
2012/01/06		2012/01/06		Monday, July 04, 2011	
2012/01/06		2012/01/06		Sheet 35 of 51	



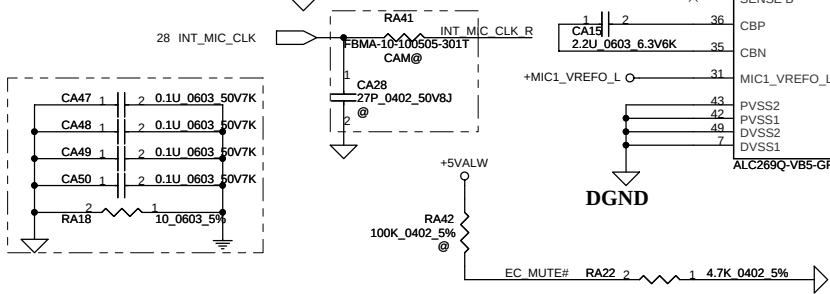
Ext. Mic/LINE IN



For EMI

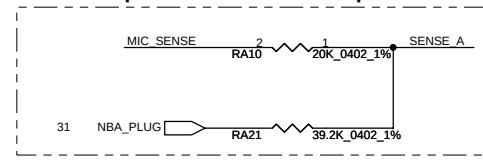


For EMI



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

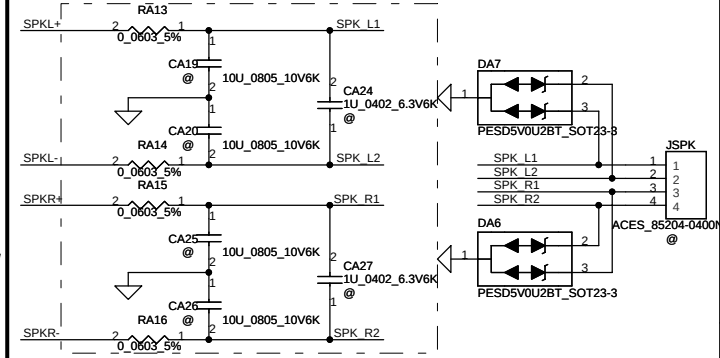
place close to chip



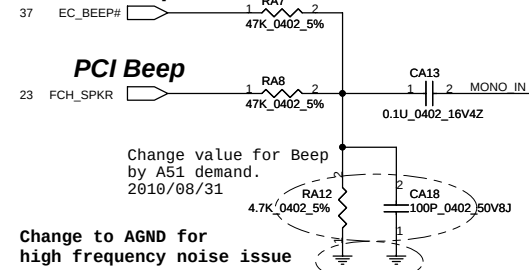
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				Date	Monday, July 04, 2011
				Sheet	36 of 51

Speaker Connector

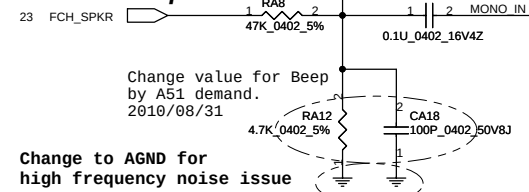
placement near Audio Codec



EC Beep

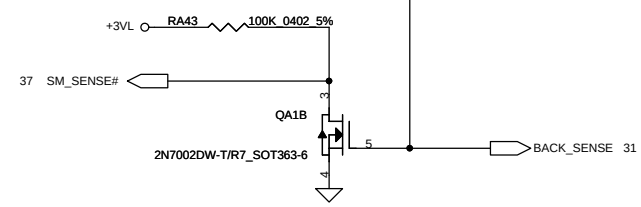
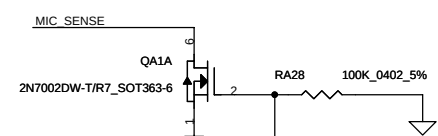
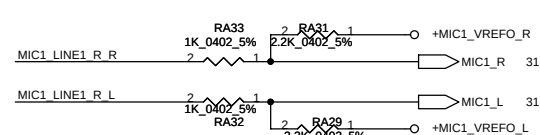


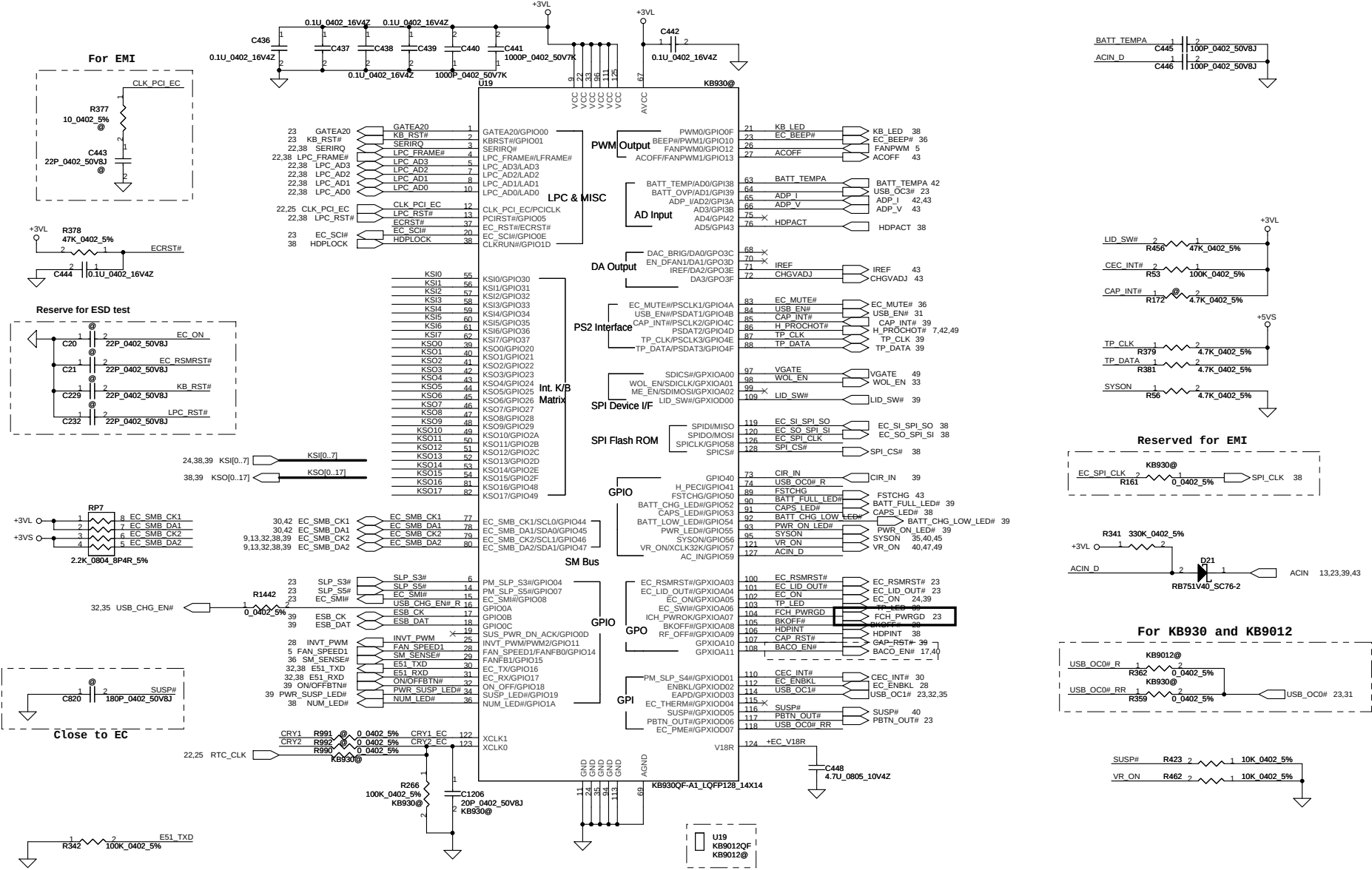
PCI Beep



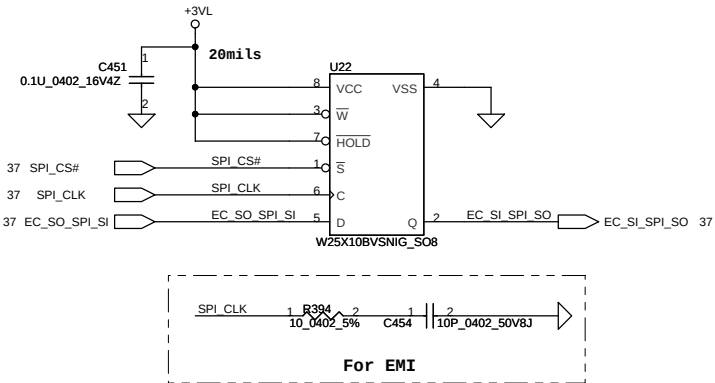
Change value for Beep by A51 demand.
2010/08/31

Ext.MIC/LINE IN JACK



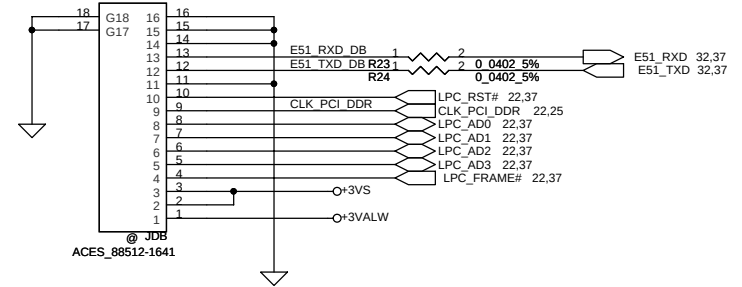
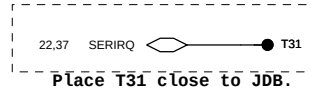


SPI Flash (128KB)



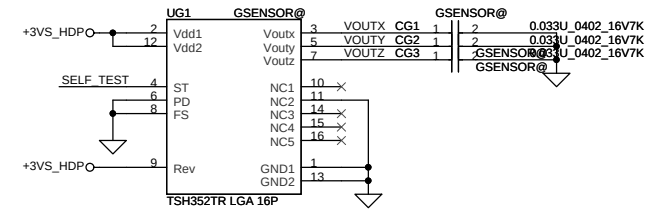
LPC Debug Port

Place JDB under DDR DIMM

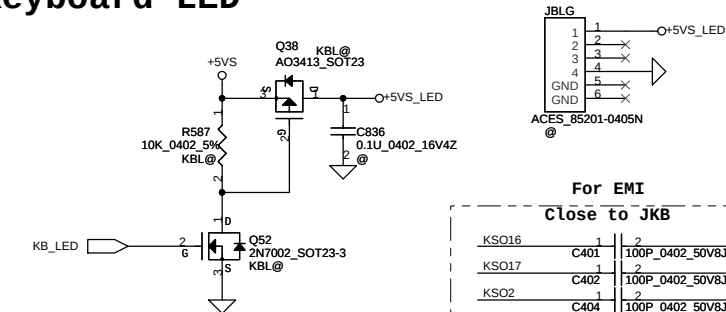


G-Sensor

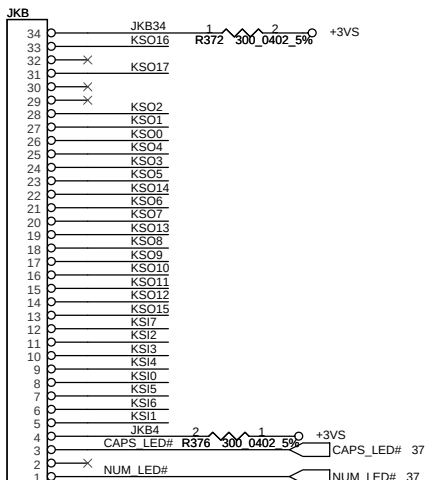
Place UG1 on TOP Layer



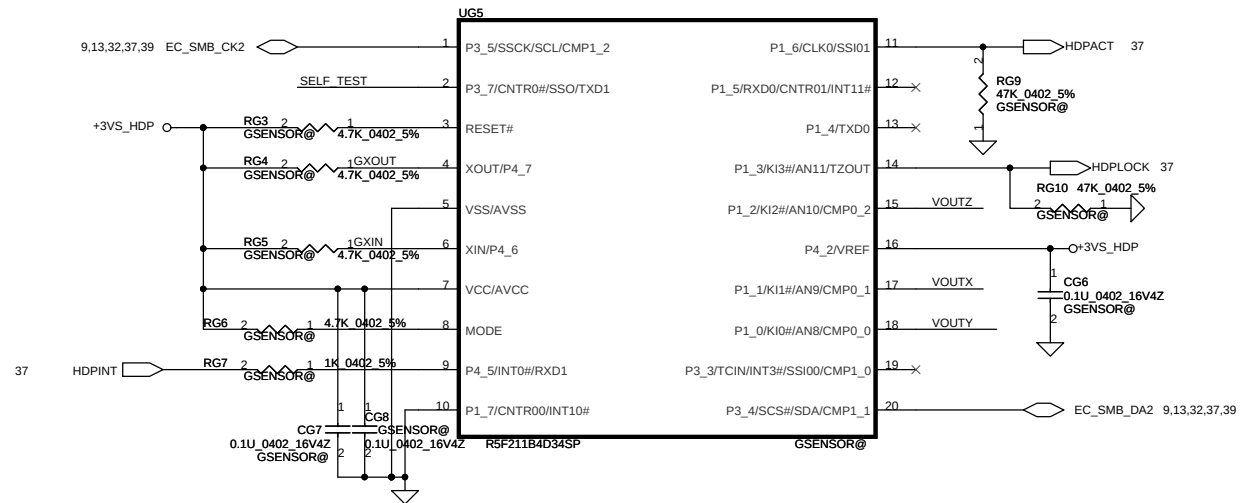
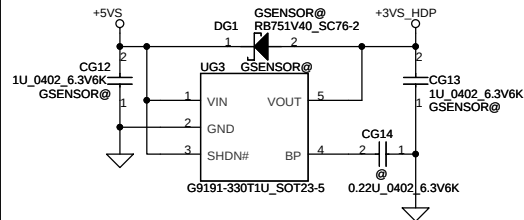
Keyboard LED



KEYBOARD CONN.

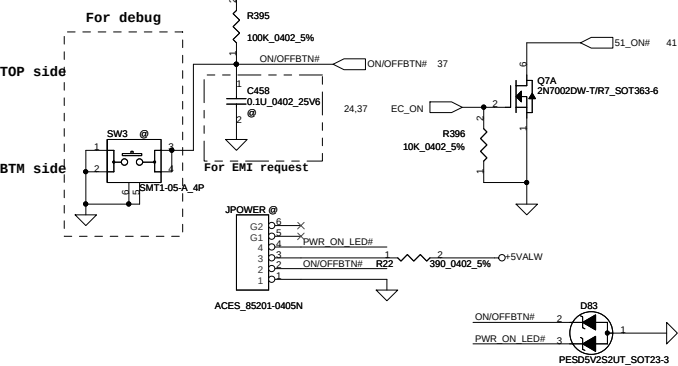


For EMI			
Close to JKB			
KSO16	1	2	
KSO17	1	2	100P_0402_50V8J
	C402	2	100P_0402_50V8J
KSO2	1	2	100P_0402_50V8J
KSO1	1	2	100P_0402_50V8J
	C405	2	100P_0402_50V8J
KSO0	1	2	
	C406	2	100P_0402_50V8J
KSO4	1	2	100P_0402_50V8J
	C407	2	100P_0402_50V8J
KSO3	1	2	100P_0402_50V8J
	C408	2	100P_0402_50V8J
KSO5	1	2	100P_0402_50V8J
	C409	2	100P_0402_50V8J
KSO14	1	2	100P_0402_50V8J
	C410	2	100P_0402_50V8J
KSO6	1	2	100P_0402_50V8J
	C411	2	100P_0402_50V8J
KSO7	1	2	100P_0402_50V8J
	C412	2	100P_0402_50V8J
KSO13	1	2	100P_0402_50V8J
	C413	2	100P_0402_50V8J
KSO8	1	2	100P_0402_50V8J
	C415	2	100P_0402_50V8J
KSO9	1	2	100P_0402_50V8J
	C416	2	100P_0402_50V8J
KSO10	1	2	100P_0402_50V8J
	C417	2	100P_0402_50V8J
KSO11	1	2	100P_0402_50V8J
	C418	2	100P_0402_50V8J
KSO12	1	2	100P_0402_50V8J
	C419	2	100P_0402_50V8J
KSO15	1	2	100P_0402_50V8J
	C420	2	100P_0402_50V8J
KSI7	1	2	100P_0402_50V8J
	C421	2	100P_0402_50V8J
KSI2	1	2	100P_0402_50V8J
	C422	2	100P_0402_50V8J
KSI3	1	2	100P_0402_50V8J
	C423	2	100P_0402_50V8J
KSI4	1	2	100P_0402_50V8J
	C424	2	100P_0402_50V8J
KSI0	1	2	100P_0402_50V8J
	C425	2	100P_0402_50V8J
KSI5	1	2	100P_0402_50V8J
	C427	2	100P_0402_50V8J
KSI6	1	2	100P_0402_50V8J
	C429	2	100P_0402_50V8J
KSI1	1	2	100P_0402_50V8J
	C431	2	100P_0402_50V8J
CAPS_LED#	1	2	100P_0402_50V8J
	C433	2	100P_0402_50V8J
NUM_LED#	1	2	100P_0402_50V8J
	C435	2	100P_0402_50V8J

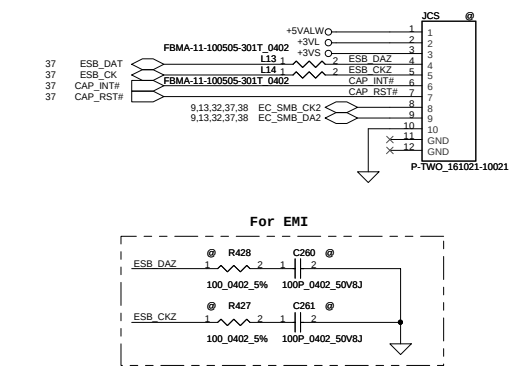


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				4019D8		
				Date: Monday, July 04, 2011	Sheet 38 of 51	

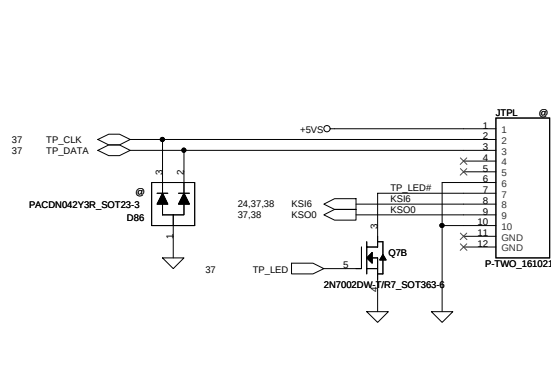
Power Button



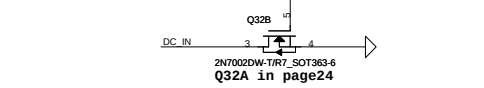
Caps Sensor/Light Sensor Conn.



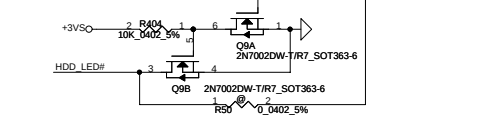
Touchpad & Light Pipe Connector



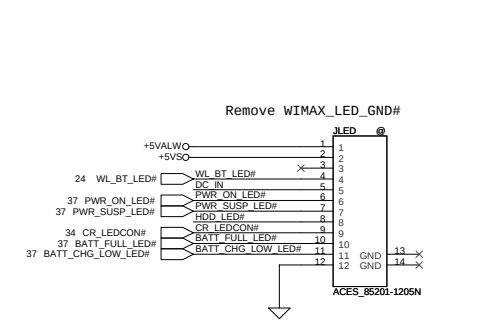
DC-IN LED



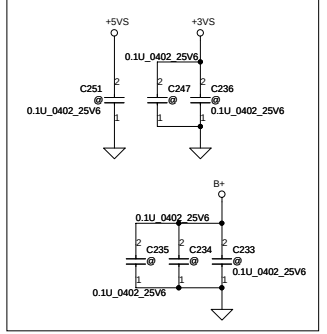
HDD LED



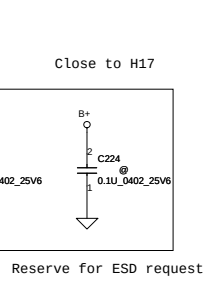
LED/B Connector



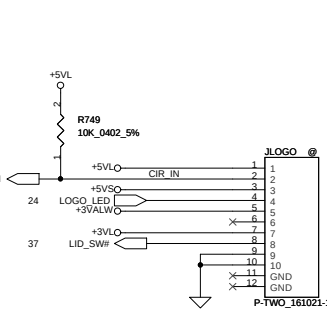
Reserve for ESD request



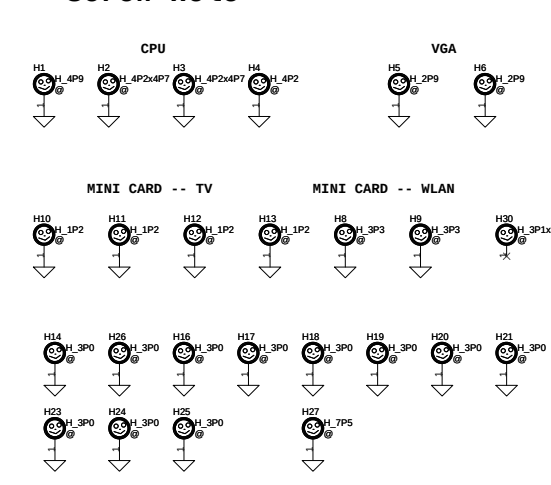
Reserve for EMI request



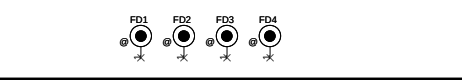
LOGO/B Connector



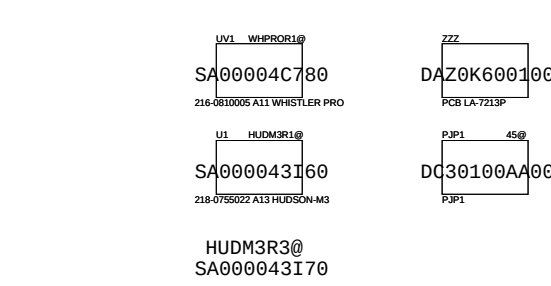
Screw Hole



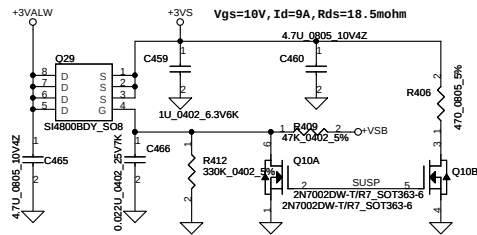
PCB Federal Mark PAD



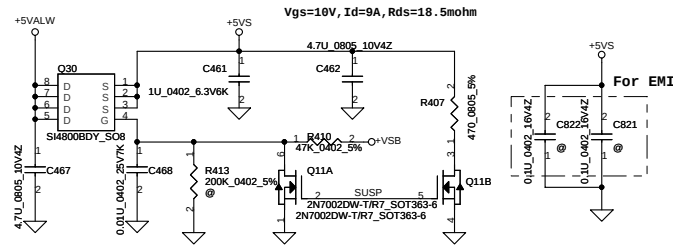
ISPD



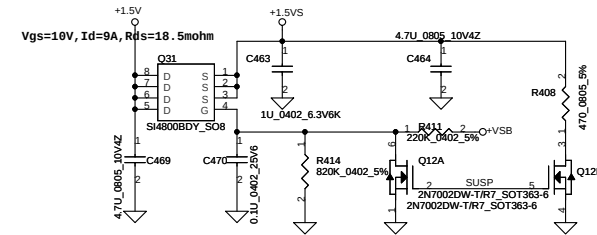
+3VALW TO +3VS



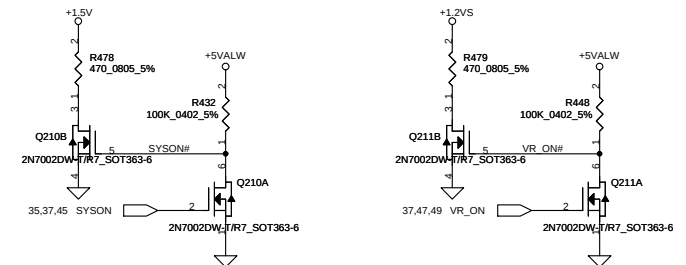
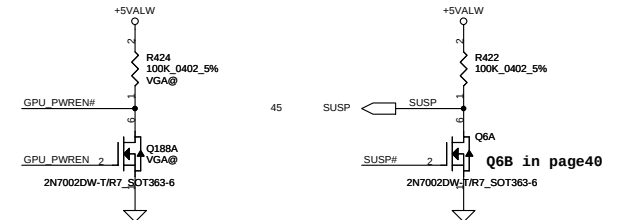
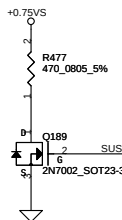
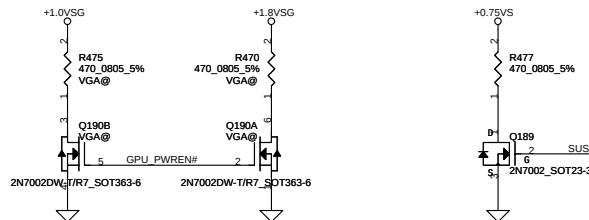
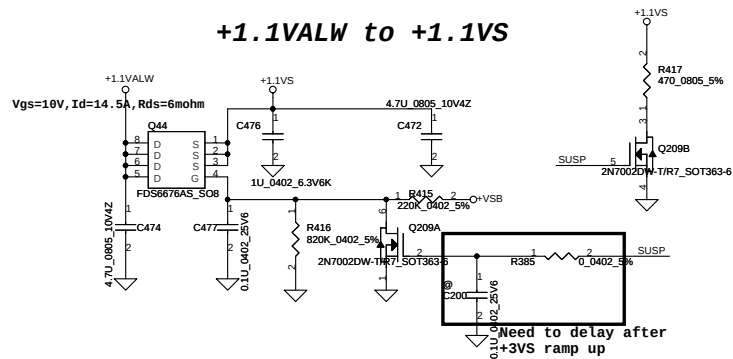
+5VALW TO +5VS



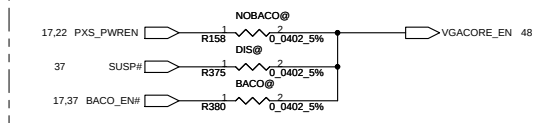
+1.5V to +1.5VS



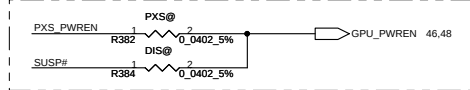
+1.1VALW to +1.1VS



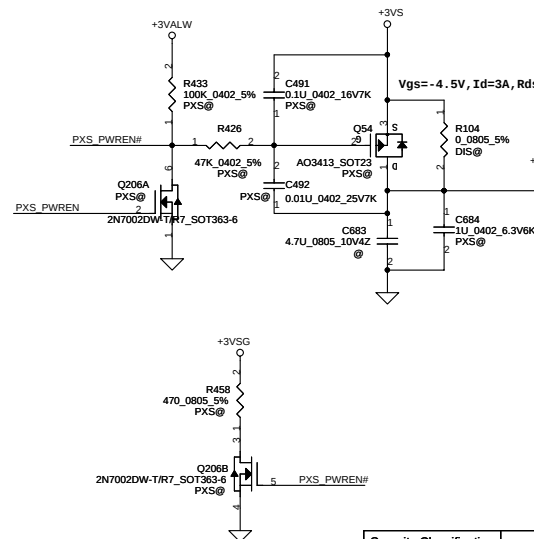
For +VGA_CORE power enable



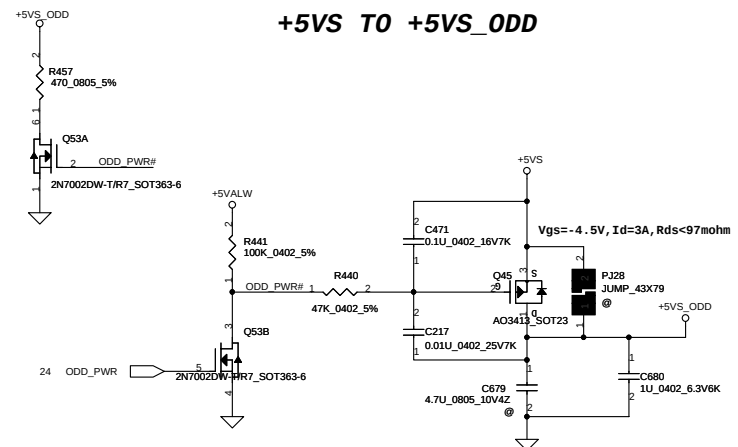
For GPU power enable



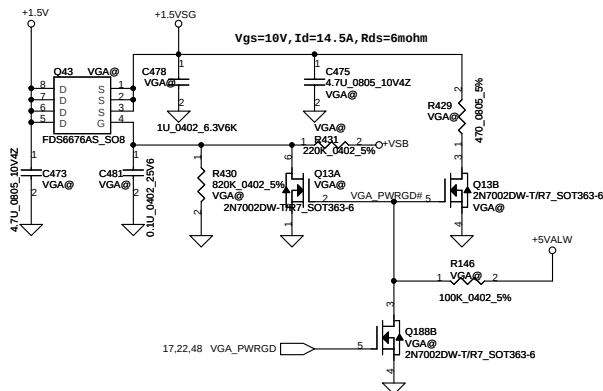
+3VS to +3VSG



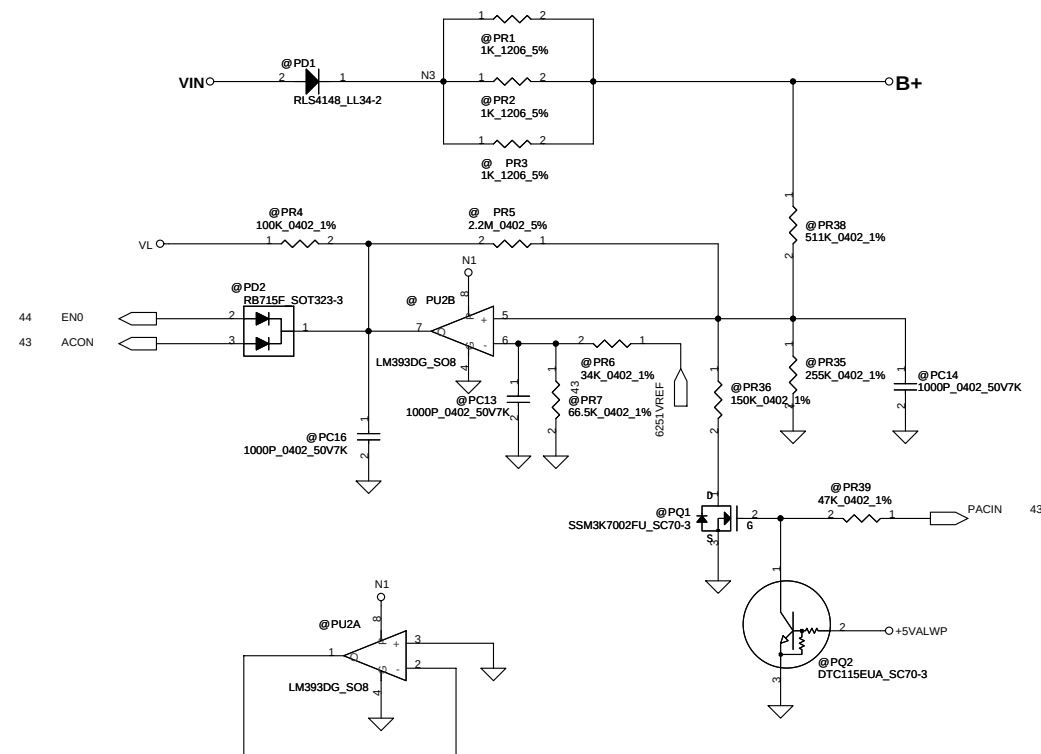
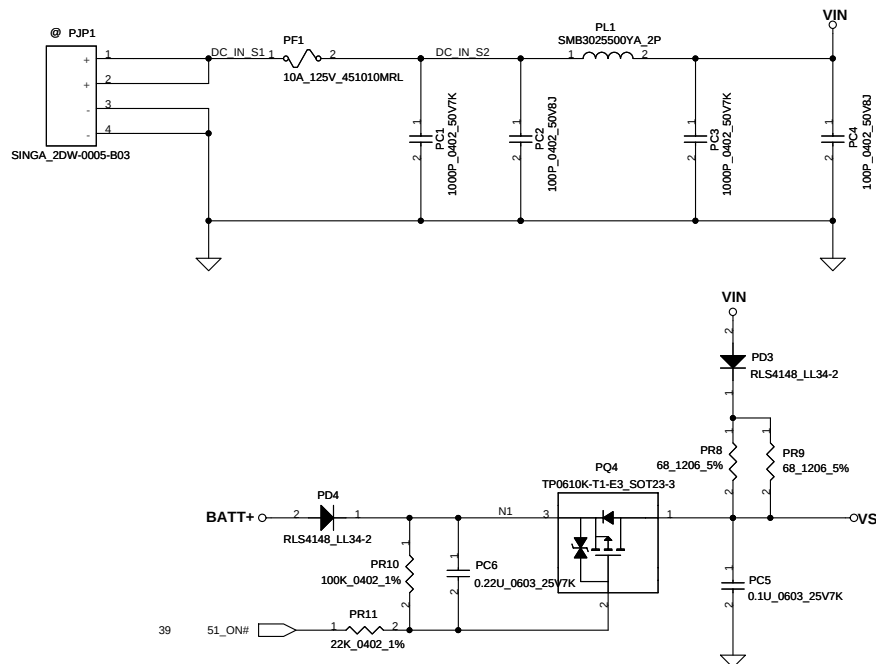
+5VS TO +5VS_ODD



+1.5V to +1.5VSG



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4019D8				Sheet 40 of 51



+3VLP ○ 2 **@ PJ333** 1 ○+3VL
JUMP_43X39
(100mA, 40mils ,Via NO.= 2)

+3VALWP ○ 2 **@ PJ332** 1 ○+3VALW
JUMP_43X118
(5A, 200mils ,Via NO.= 10)
OCP=7.7A

+VGA_COREP ○ 2 **@ PJ702** 1
JUMP_43X118
@ PJ703 1
JUMP_43X118
(32.6A, 1288mils ,Via NO.= 65)
OCP= 36.19A

VL ○ 2 **@ PJ353** 1 ○+5VL
JUMP_43X39

+5VALWP ○ 2 **@ PJ352** 1 ○+5VALW
JUMP_43X118
(5A, 200mils ,Via NO.= 10)
OCP=7.9A

+VSBP ○ 2 **@ PJ72** 1 ○+VSB
JUMP_43X39
(120mA, 40mils ,Via NO.= 1)

+1.1VALWP ○ 2 **@ PJ112** 1 ○+1.1VALW
JUMP_43X118
(5.3A, 212mils ,Via NO.= 11)
OCP=6.81A

+2.5VSP ○ 2 **@ PJ252** 1 ○+2.5VS
JUMP_43X39

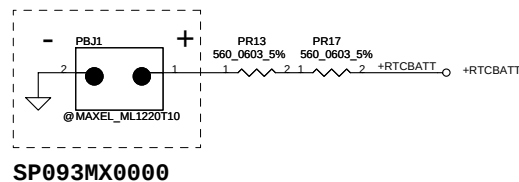
+1.0VSGP ○ 2 **@ PJ102** 1 ○+1.0VSG
JUMP_43X79
(3A, 120mils ,Via NO.= 6)

+1.8VSGP ○ 2 **@ PJ182** 1 ○+1.8VSG
JUMP_43X118
(2.5A, 100mils ,Via NO.= 5)

+0.75VSP ○ 2 **@ PJ76** 1 ○+0.75VS
JUMP_43X79
(0.5A, 40mils ,Via NO.= 1)

+1.2VSP ○ 2 **@ PJ122** 1 ○+1.2VS
JUMP_43X118
(6.5A, 260mils ,Via NO.= 13)
OCP=8.55A

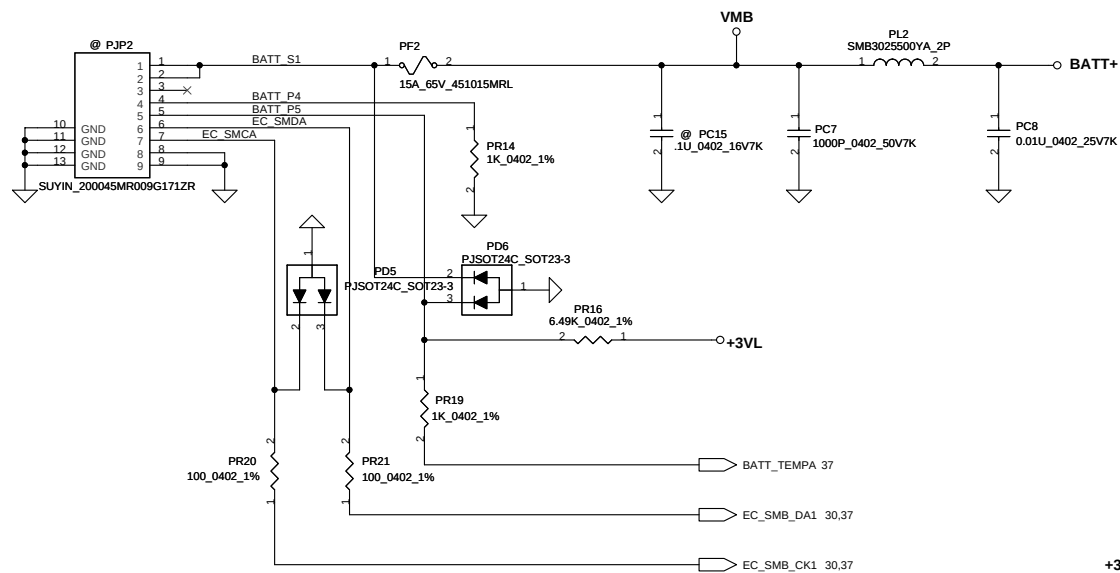
RTC Battery



ACIN

	Precharge detector		
	Min.	typ.	Max
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

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				Date:	Monday, July 04, 2011
				Sheet	41 of 51

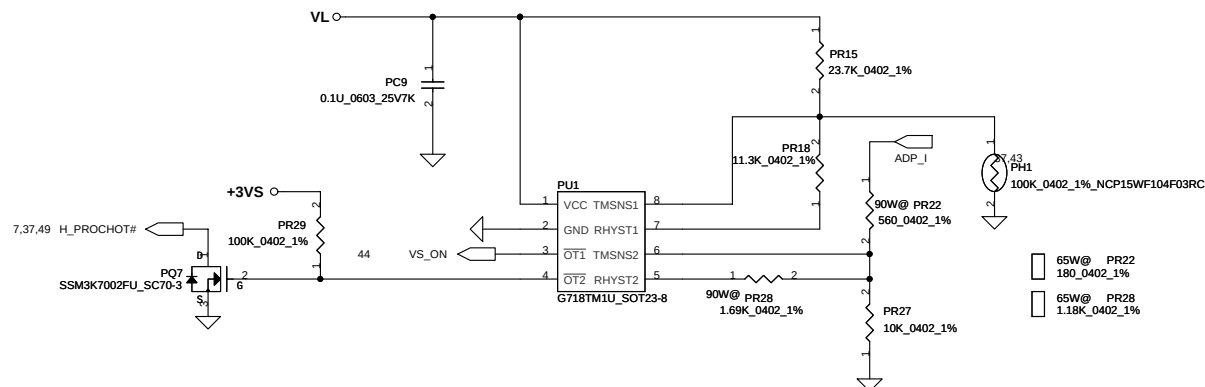


PH1 under CPU bottom side :
CPU thermal protection at 90 degree C
Recovery at 56 degree C

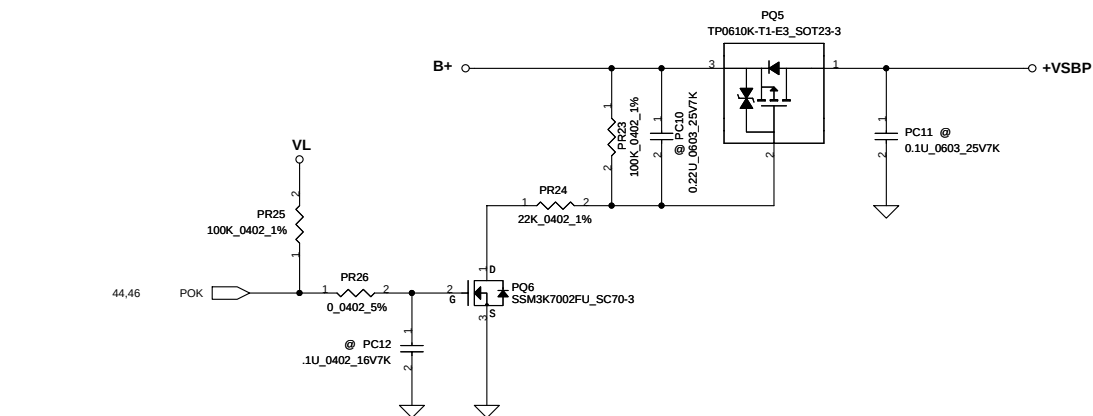
$$R_{set} = 3 * R_{tmh}$$

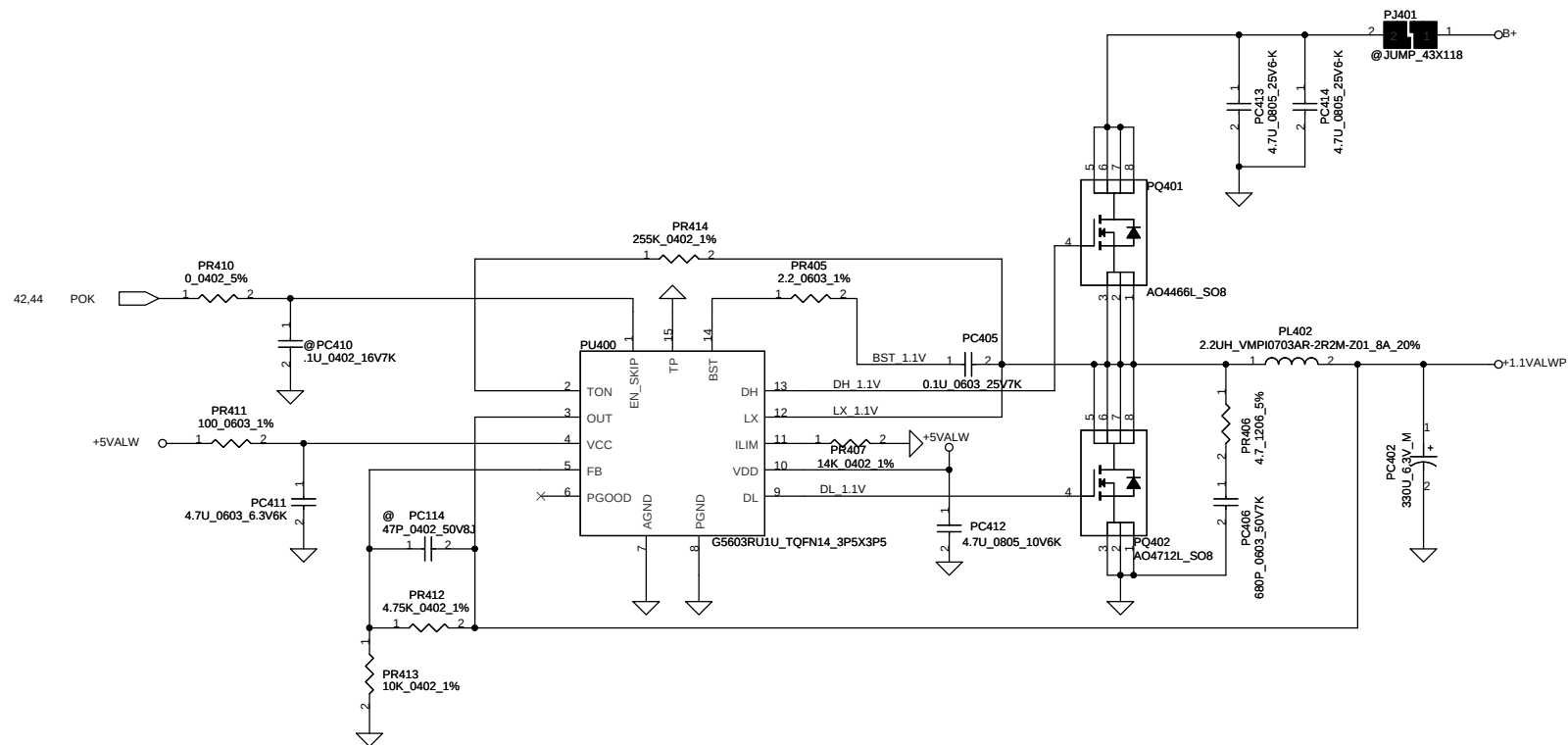
$$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$$

Rtmh at 90C = 7.87K, Rtml at 56C = 26.1K
 $R_{set} = 3 * 7.87K = 23.61K \Rightarrow 23.7K$
 $R_{hyst} = (23.7K * 26.1K) / (3 * 26.1K - 23.7K) = 11.33K \Rightarrow 11.3K$

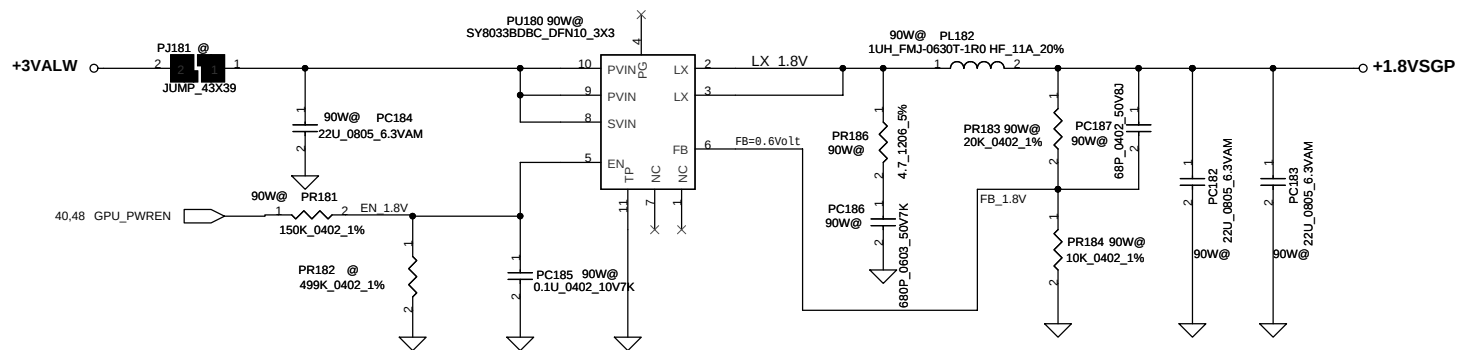


Adaptor protection				
Adaptor	Throttling point	ADP_I	Recovery point	ADP_I
90W	113.5W	1.783V	86.4W	1.357V
65W	71.8W	1.5V	62.44W	1.3V



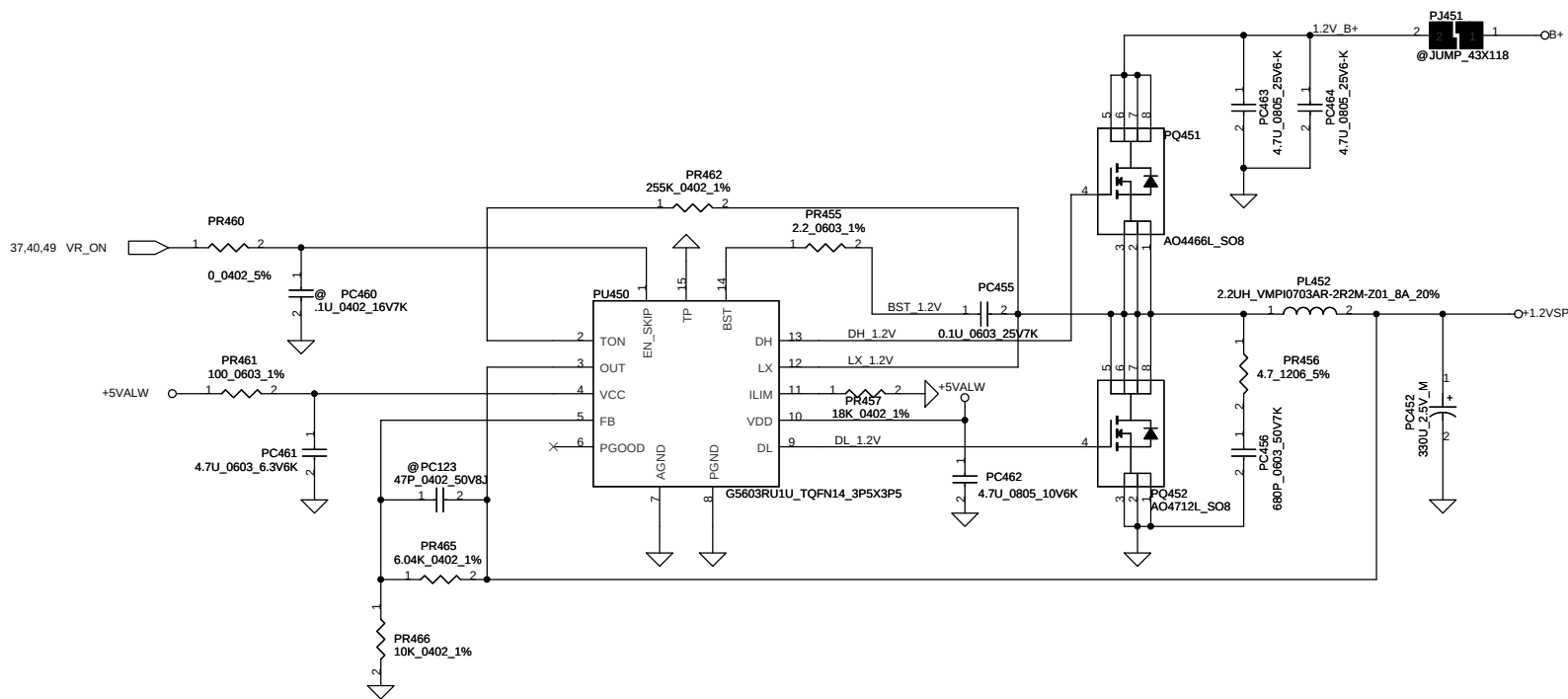


Ipeak=5.3A
Imax=3.71A
Rtrip=14K, OCP=6.64A
F=315KHz
Total Capacitor 330uF,
ESR 15mohm



Ipeak=2.5A
ILIM = 4A
F=1MHz
Total Capacitor 44uF,

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				Date:	Monday, July 04, 2011
				Sheet	46 of 51



Ipeak=6.5A
I_{max}=4.55A
R_{trip}=18K, OCP=8.37A
F=315KHz
Total Capacitor 720uF,
ESR 6mohm
HW side:
C130 390uF 10m

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				Date:	Monday, July 04, 2011
				Sheet	47 of 51

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				Custom	4019D8		
				Date:	Monday, July 04, 2011	Sheet	50 of 51

HW PIR (Product Improve Record)

Q{樗藩惇幹\餹惇幹机販蝴濕藜\驚搗潛EMATIC C{樗惇鶇潛E LIST

REVISION C{樗惇鶇潛E: 0.1 TO 0.2

Item	Date	Page	Solution	Request
1.	3/17	P23	Remove level-shifter for ODD_PLU{鯨確鶇耳	ODD has internal 1K pull-down
2.	3/17	P34	Add level-shifter for CR_CPPE#	For leakage issue
3.	3/17	P23	Change {樗縵置確湜潛PD to {鯨幹\鶇鶇鶇鼻耳\旨彼\程愴琴erve {鯨幹\鶇鶇鶇拂耳\潜EVENT9# has issue	
4.	3/17	P24	Change L0{鯨醺湜餹幹縵\榑睹\潛PI0176 and WL_BT_LED to {鯨藜確醺蝴机机\淳睹程\餹幹縵\疳擘 琴灼\曉琴琴禽愴\疳榑愴程\膜睹欸愴程幹睹旨	
5.	3/24	P10	Add C295,C316,C324,C325	For EMI test
6.	3/28	P39	Reserve C20,C21,C229,C231~C236,C247,C251	For ESD test)
7.	3/29	P38	Change LPC debug port to 16pins connector	To support new debug card
8.	3/30	P07	Add R70,R102,R105	Pull-down for unused {樗藜縵\膜睹程榑

REVISION C{樗惇鶇潛E: 0.2 TO 1.0

Item	Date	Page	Solution	Request
1.	4/15	P31	Reserve D24, D25	
2.	4/27	P22	Change R257 form 100k to 10k for leakage issue.	
3.	4/27	P37	Add BAC0_EN# to EC	To inform EC {鯨藜む\榑灼愴程敞 擘\琴愴旨琴睹程\琴榑 榑禽琴