

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : VCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

VCC_CORE

+1.5V

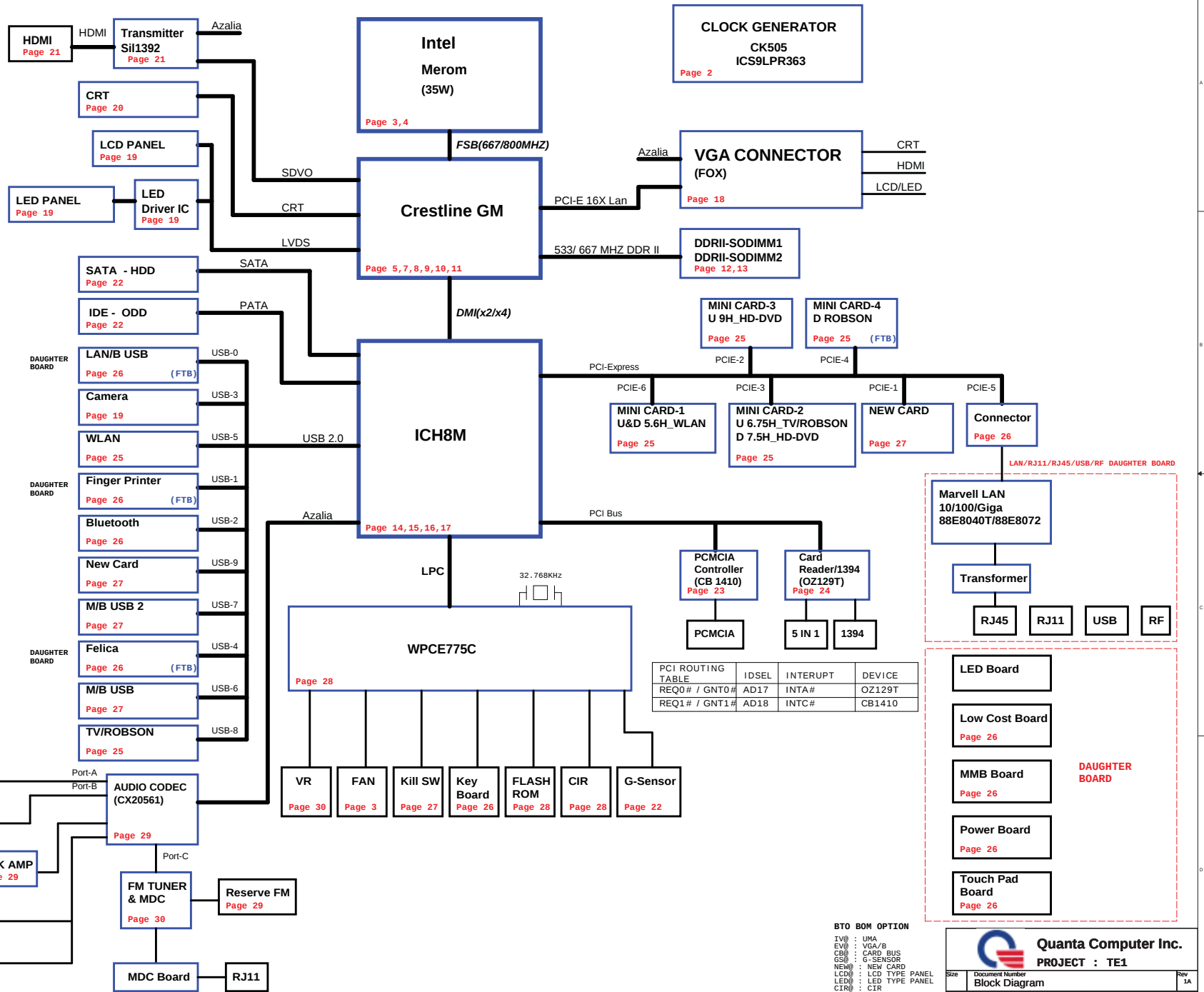
+1.05V

+1.25V

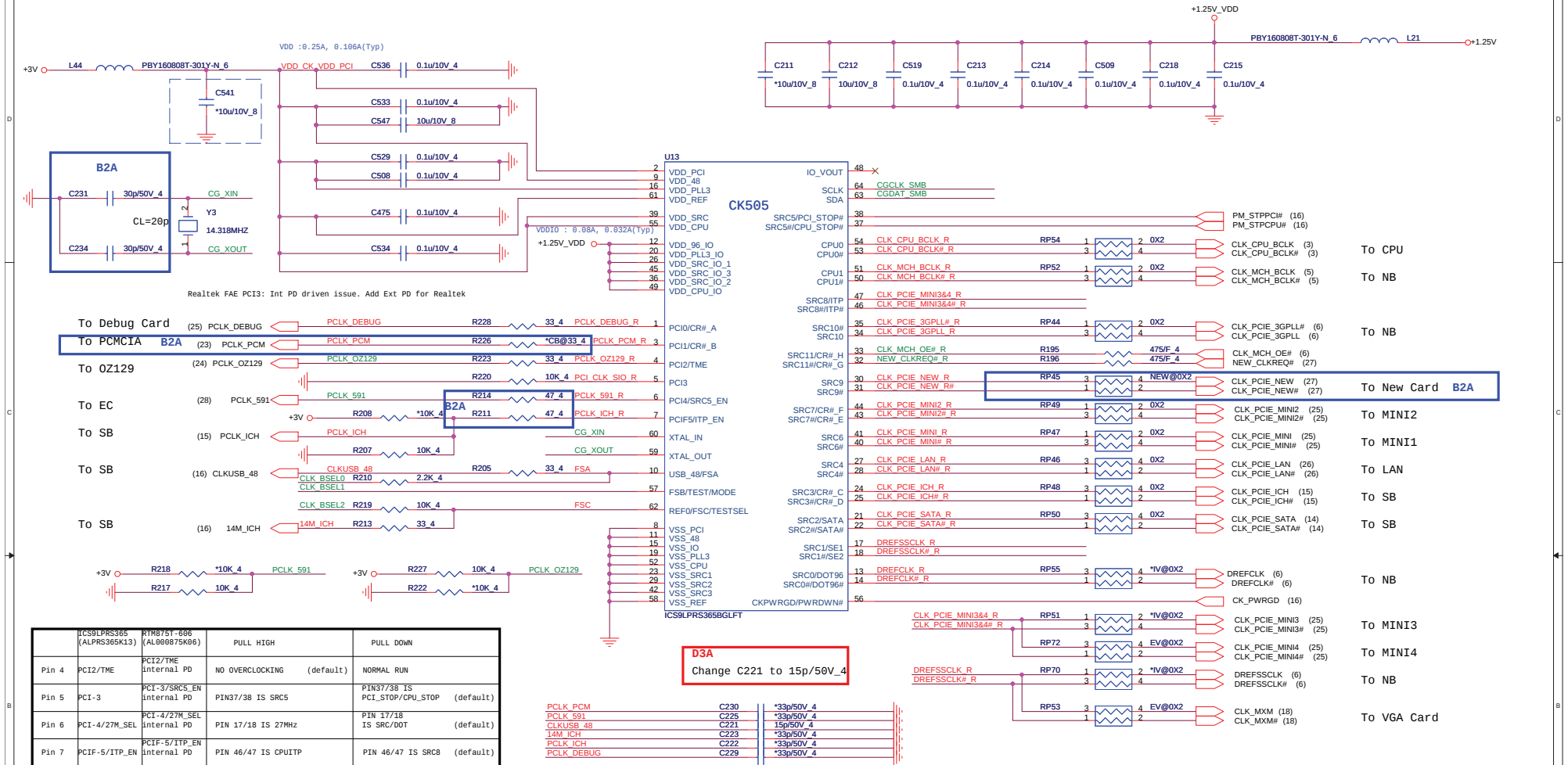
+1.8VSUS
+1.8V

+3VPCU
+3V_S5
+3VSUS
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF

TE1 Block Diagram

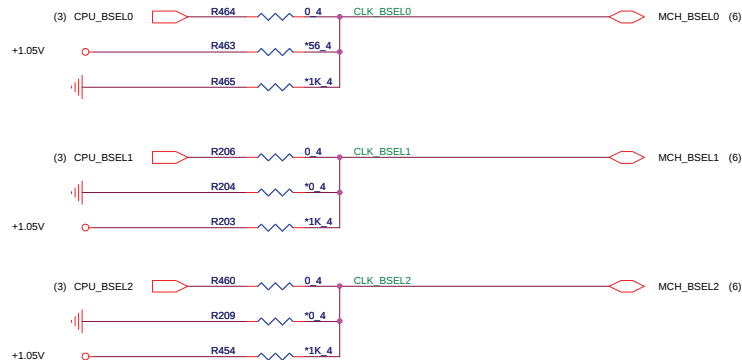


Clock Generator

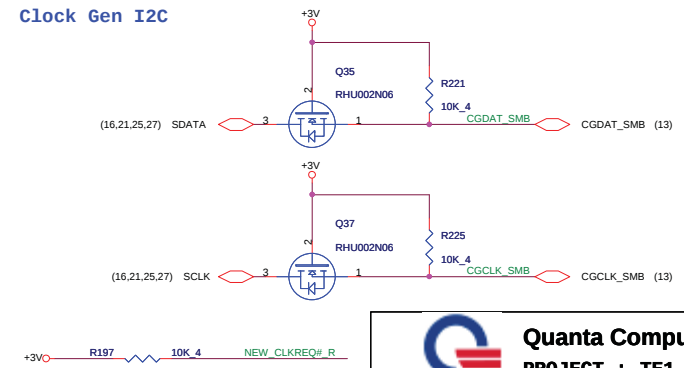


BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

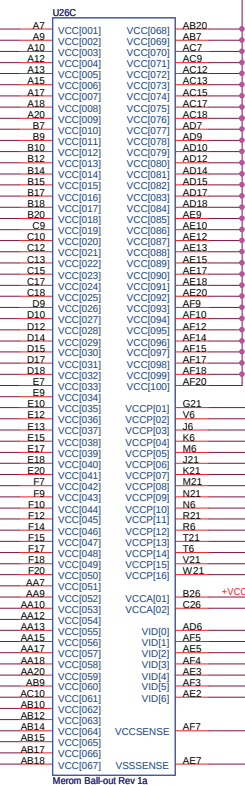
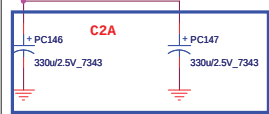
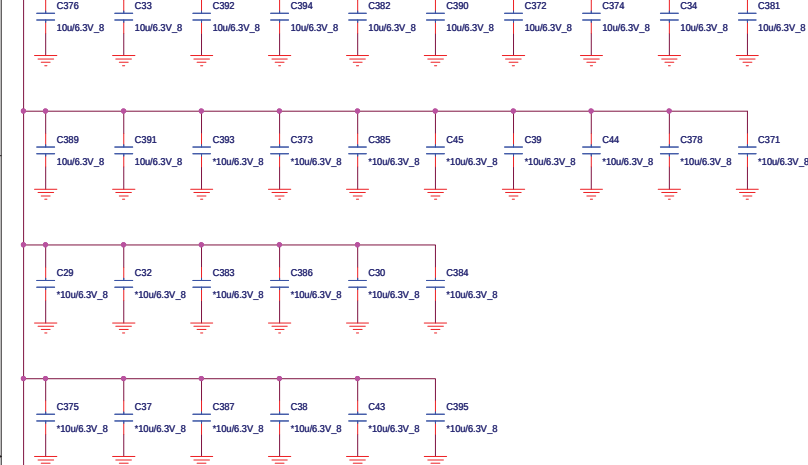


Clock Gen I2C

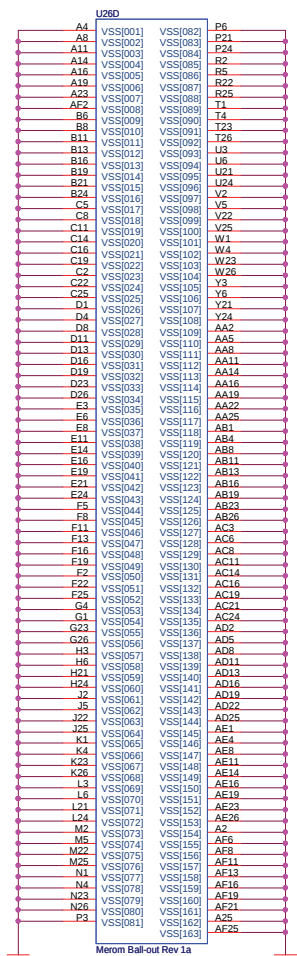
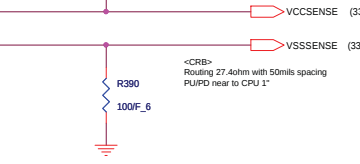
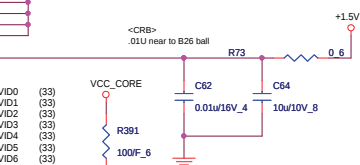
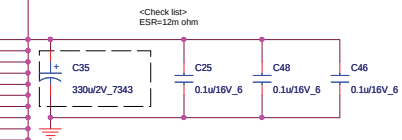


CPU(Power)

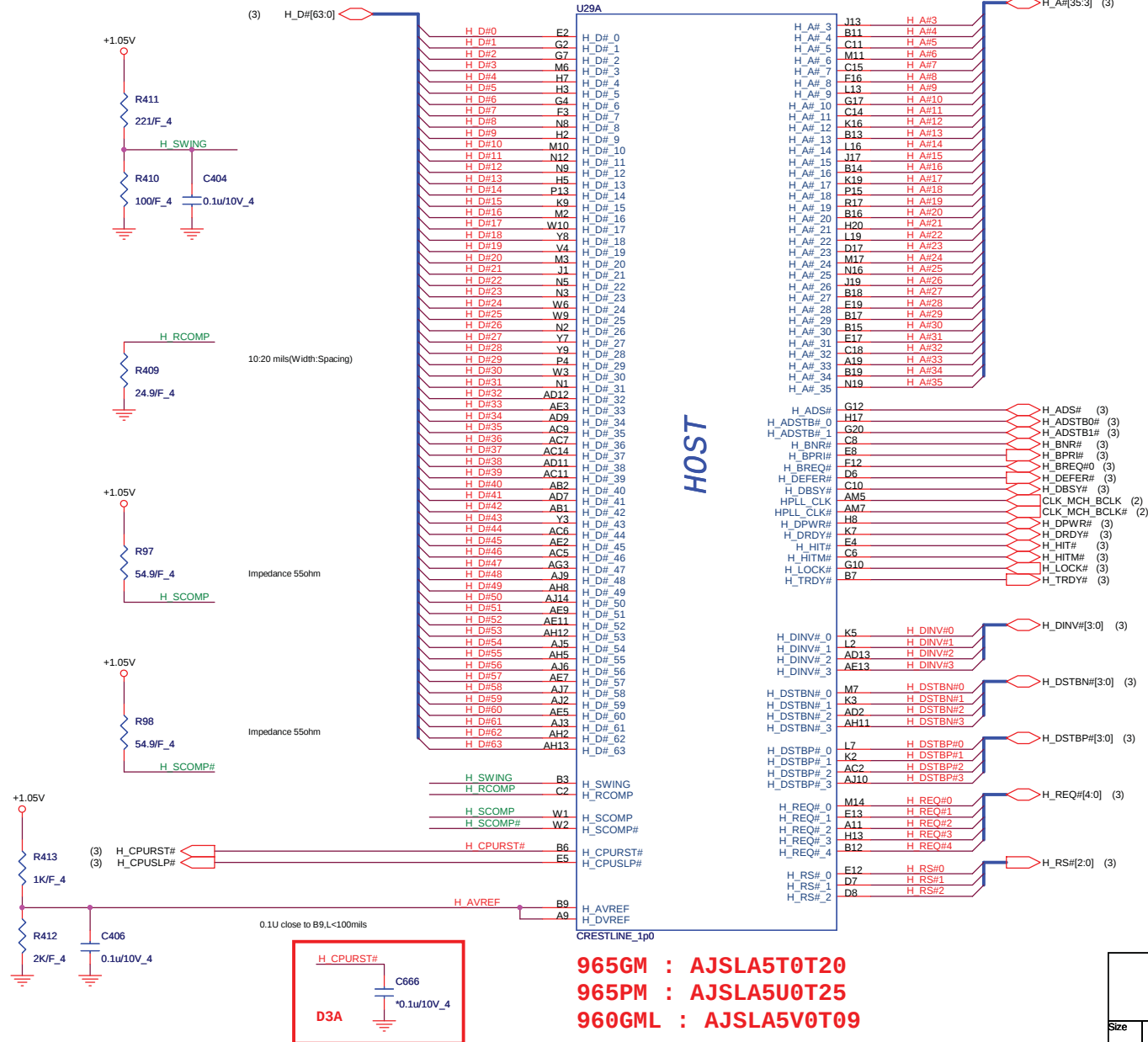
VCC_CORE

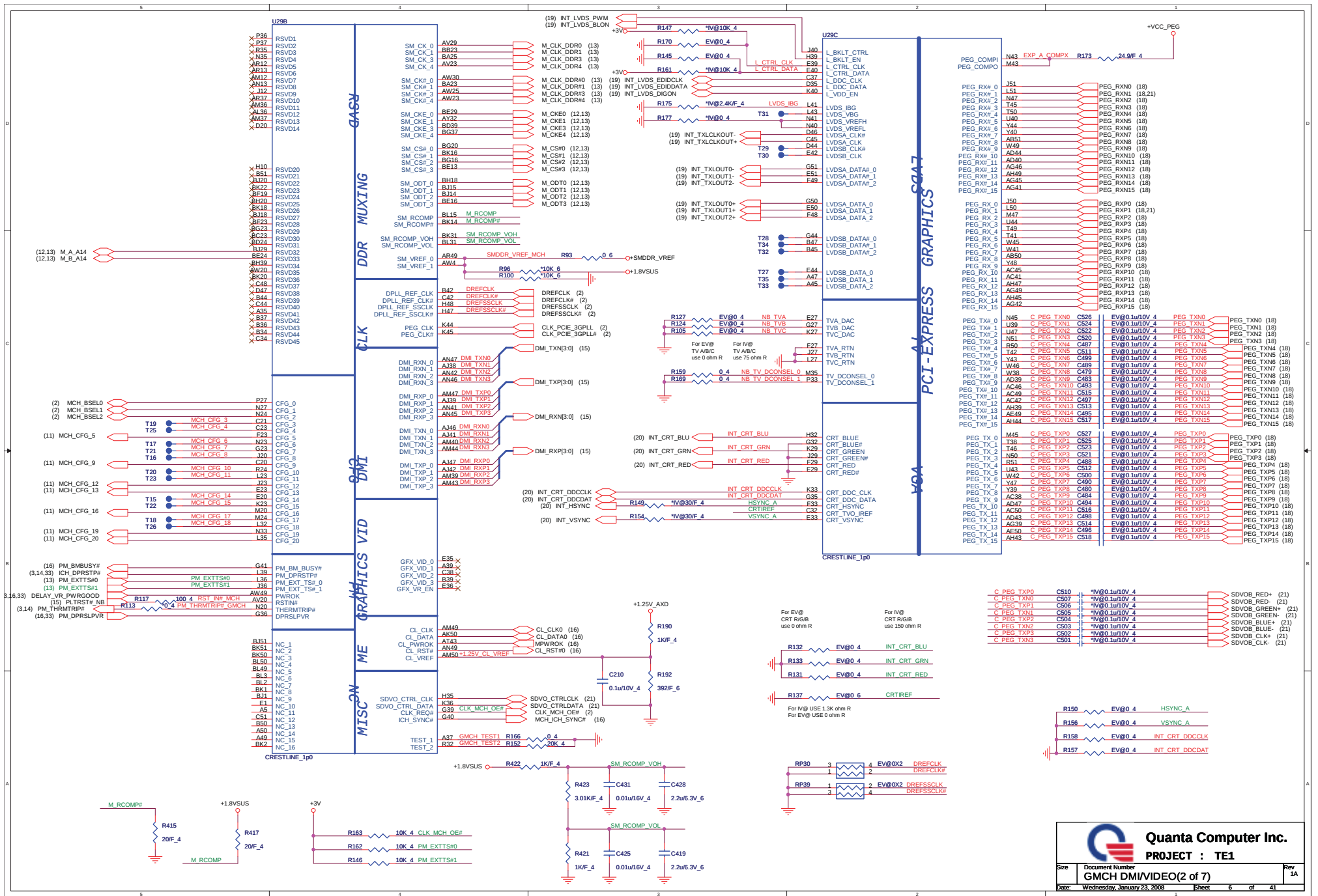


<REV.NO. 0.5/REF.NO.19343>
Ivcc Max 52A
Ivccp Max 6A(VCCP supply before Vcc stable)
Max 2A(VCCP supply after Vcc stable)
Ivcca Max 130mA

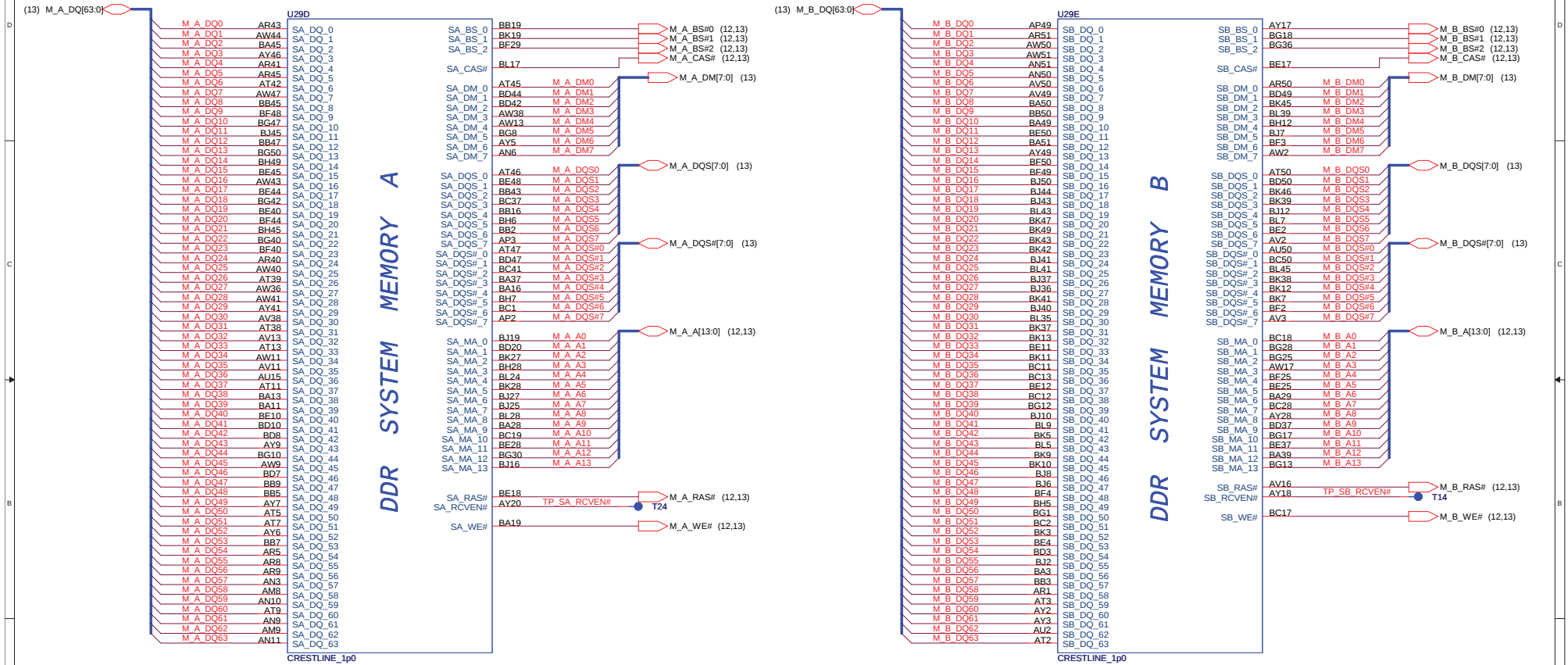


NB (HOST)

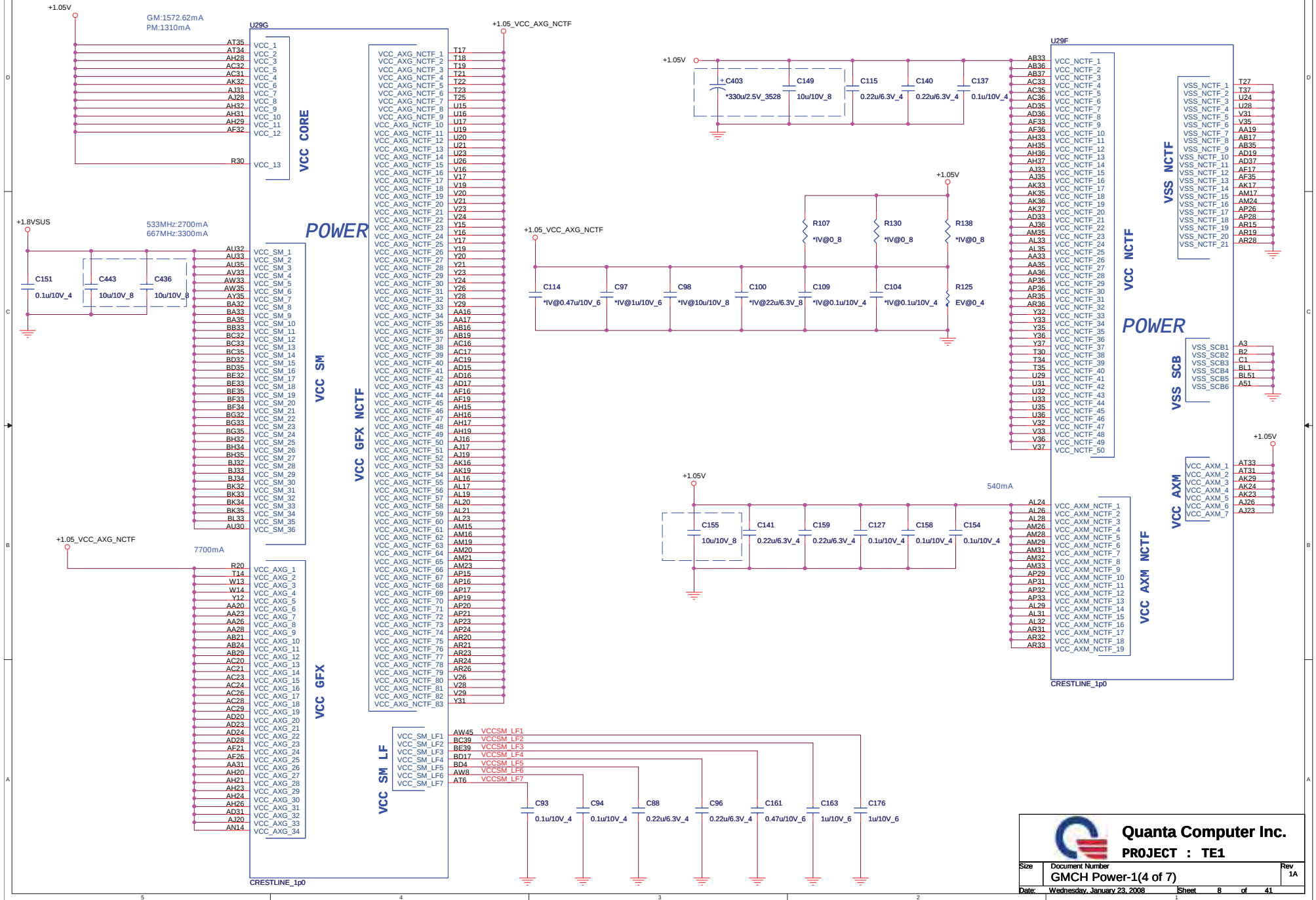




NB(Memory controller)



NB(Power-1)



CRT/TV Disable/Enable guideline

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TVO	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDD_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TVO	3.3V	GND	VSSABG_DAC	GND	GND
VCCA_B_TVO	3.3V	GND	VCC_SYNC	3.3V	GND

U29H

CRT

VCCSYNC

VCCA_CRT_DAC_1

VCCA_CRT_DAC_2

VCCA_DAC_BG

VSSA_DAC_BG

VCCA_DPLL_A

VCCA_DPLLB

VCCA_HPLL

VCCA_MPLL

VCCA_LVDS

VSSA_LVDS

VCCA_PEG_BG

VSSA_PEG_BG

VCCA_PEG_PLL

PLL

A

VCCA_SM_1

VCCA_SM_2

VCCA_SM_3

VCCA_SM_4

VCCA_SM_5

VCCA_SM_7

VCCA_SM_8

VCCA_SM_9

VCCA_SM_10

VCCA_SM_11

VCCA_SM_NCTF_1

VCCA_SM_NCTF_2

SM

VCCA_SM_CK_1

VCCA_SM_CK_2

CK

VCCA_TV_A_DAC_1

VCCA_TV_A_DAC_2

VCCA_TV_B_DAC_1

VCCA_TV_B_DAC_2

VCCA_TV_C_DAC_1

VCCA_TV_C_DAC_2

TV

VCCD_CRT

VCCD_TV_DAC

VCCD_QDAC

VCCD_HPLL

VCCD_PEG_PLL

VCCD_LVDS_1

VCCD_LVDS_2

D

TV/CRT

LVDS

AXD

VCC_AXD_1

VCC_AXD_2

VCC_AXD_3

VCC_AXD_4

VCC_AXD_5

VCC_AXD_6

VCC_AXD_NCTF

AXF

VCC_AXF_1

VCC_AXF_2

VCC_AXF_3

VCC_DMI

SM CK

VCC_SM_CK_1

VCC_SM_CK_2

VCC_SM_CK_3

VCC_SM_CK_4

VCC_TX_LVDS

VCC_HV_1

VCC_HV_2

HV

VCC_PEG_1

VCC_PEG_2

VCC_PEG_3

VCC_PEG_4

VCC_PEG_5

PEG

VCC_RXR_DMI_1

VCC_RXR_DMI_2

DMI

VTTFL1

VTTFL2

VTTFL3

VTTFL

POWER

AT23

AU28

AU24

AT29

AT25

AT30

AR29

B23

B21

A21

BK24

BK23

BJ24

BJ23

A43

C40

B40

AD51

W50

W51

V49

V50

AH50

AH51

A7

F2

AH1

CRESTLINE 1u0

LVDS Disable/Enable guideline

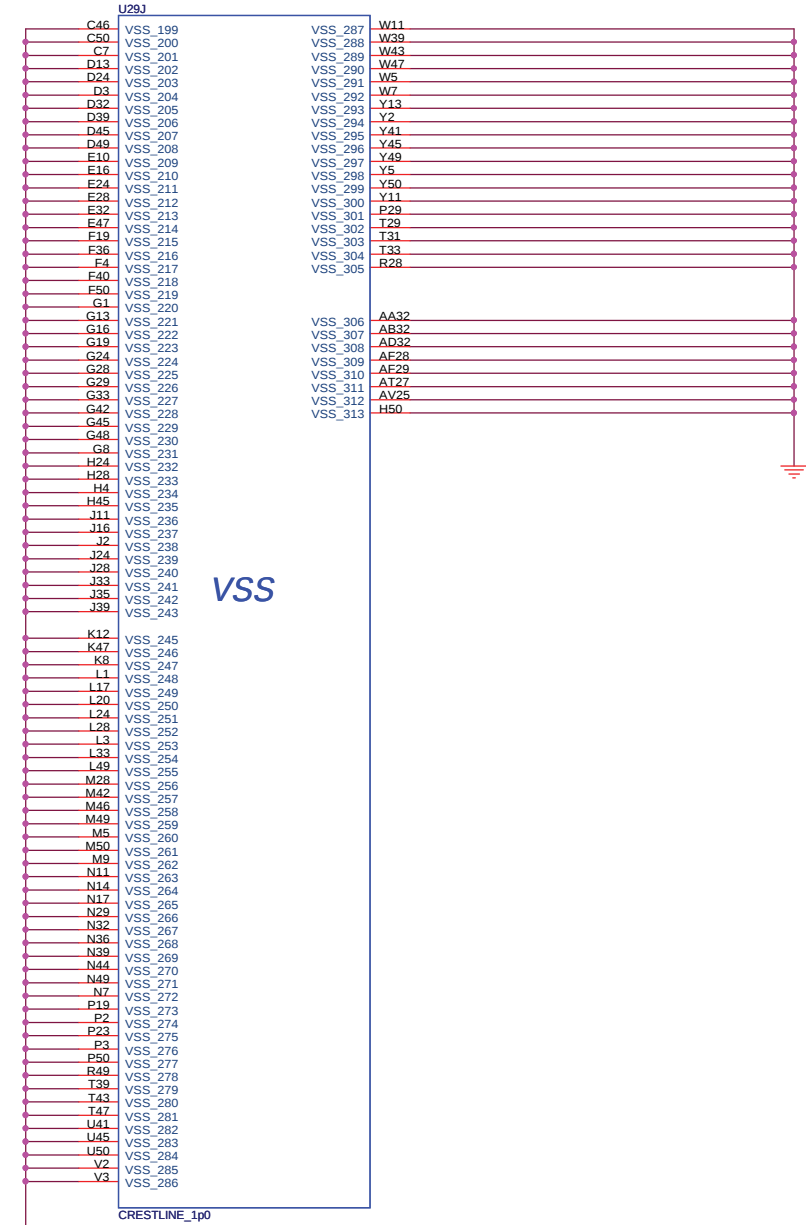
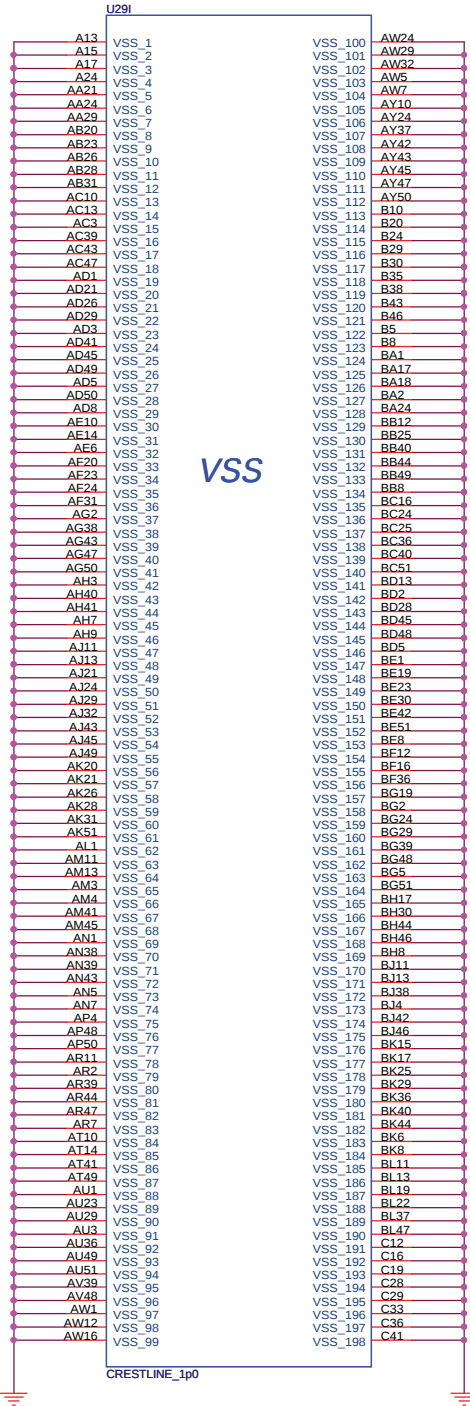
External VGA with EV@part, Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCCTX_LVDS	GND	GND	1.8V

EXTERNAL INTERNAL

The schematic diagram illustrates the LVDS disable/enable circuit. It shows various power rails and their connections to the LVDS driver. Key components include capacitors (C89, C73, C95, C82, C119, C116, C407, C410, C205, C106, C118, C428, C448, C467, C463, C405, C441), resistors (R140, R144, R188, R419, R151), inductors (L14, L37, L38, L32), and a diode (D15). The circuit is divided into sections for different power rails: +1.05V, +1.25V, +1.8VVSUS, +1.8V, +VCC_PEG, +1.05V, +3V_VCCSYNC, and +3V_VCC_HV. A green box highlights the +1.8V section, which includes a diode D15 and a resistor R151. The diagram also shows the connection of the LVDS driver to the external VGA (EV) and internal VGA (IV) parts.

NB(Power-3)



Strap table(base on checklist Ver1.6)

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CF6[17:3] Have internal Pull-up

CF6[18:19] Have internal Pull-down

Any CF6 signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CF6[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CF6[4:3]	Reserved	
CF65	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CF66	Reserved	
CF67	Intel? Management Engine Crypto strap	0 = Intel? Management Engine Crypto Transport Layer.Security (TLS) cipher suite with no confidentiality 1= Intel Management Engine Crypto TLS Cipher Suite with confidentiality (default)
CF68	Reserved	
CF69	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CF6[11:10]	Reserved	
CF6[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CF6[15:14]	Reserved	
CF616	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CF6[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CF619	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CF620	SDVO/PCIE concurrent	0 = Only SDVO or PCIE is operation(Default) 1 = SDVO and PCIE are operating simultaneously via the PEG port

DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIx4(Default)
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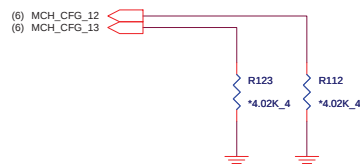
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
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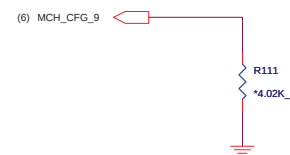
XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
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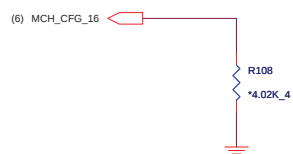


SDVO Present

Strap define at External HDMI control page

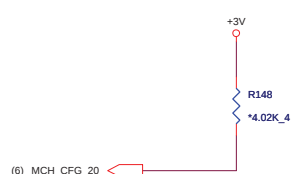
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
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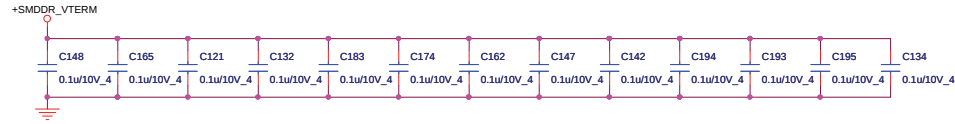


SDVO/PCIE Concurrent operation

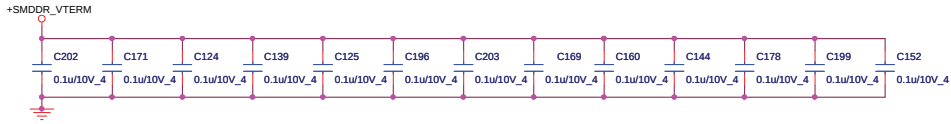
MCH_CFG_20	Low = Only SDVO or PCIE is operational(Default) High = SDVO and PCIE are operating simultaneously via the PEG port
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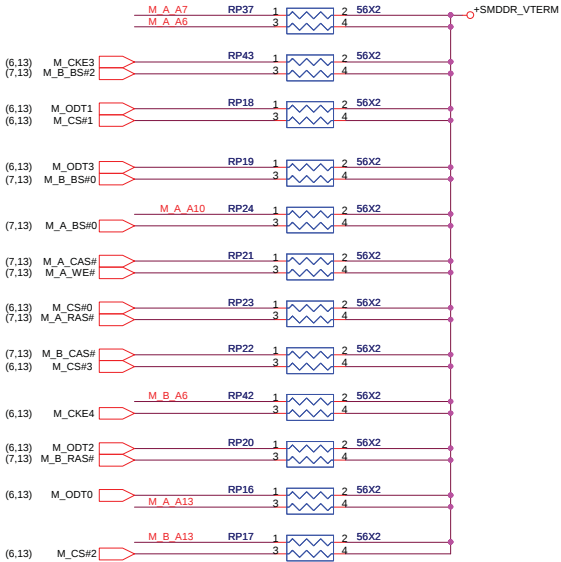
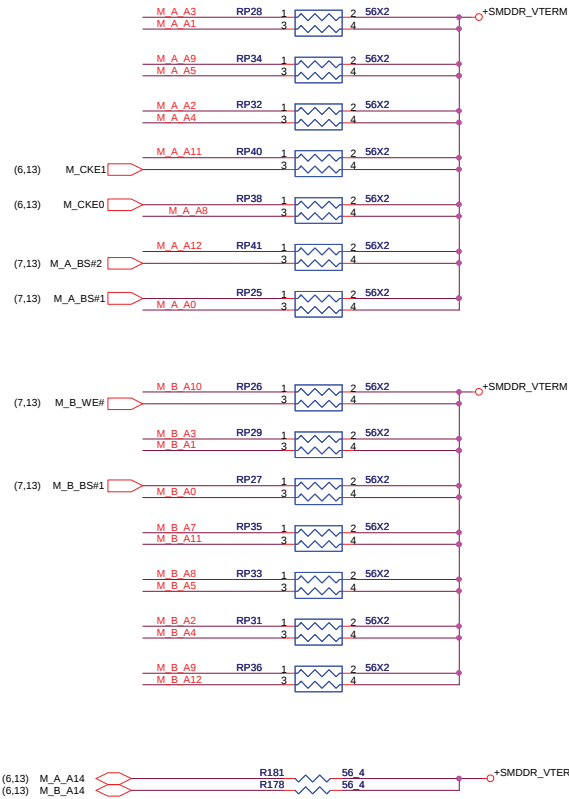
DDR2 A CHANNEL

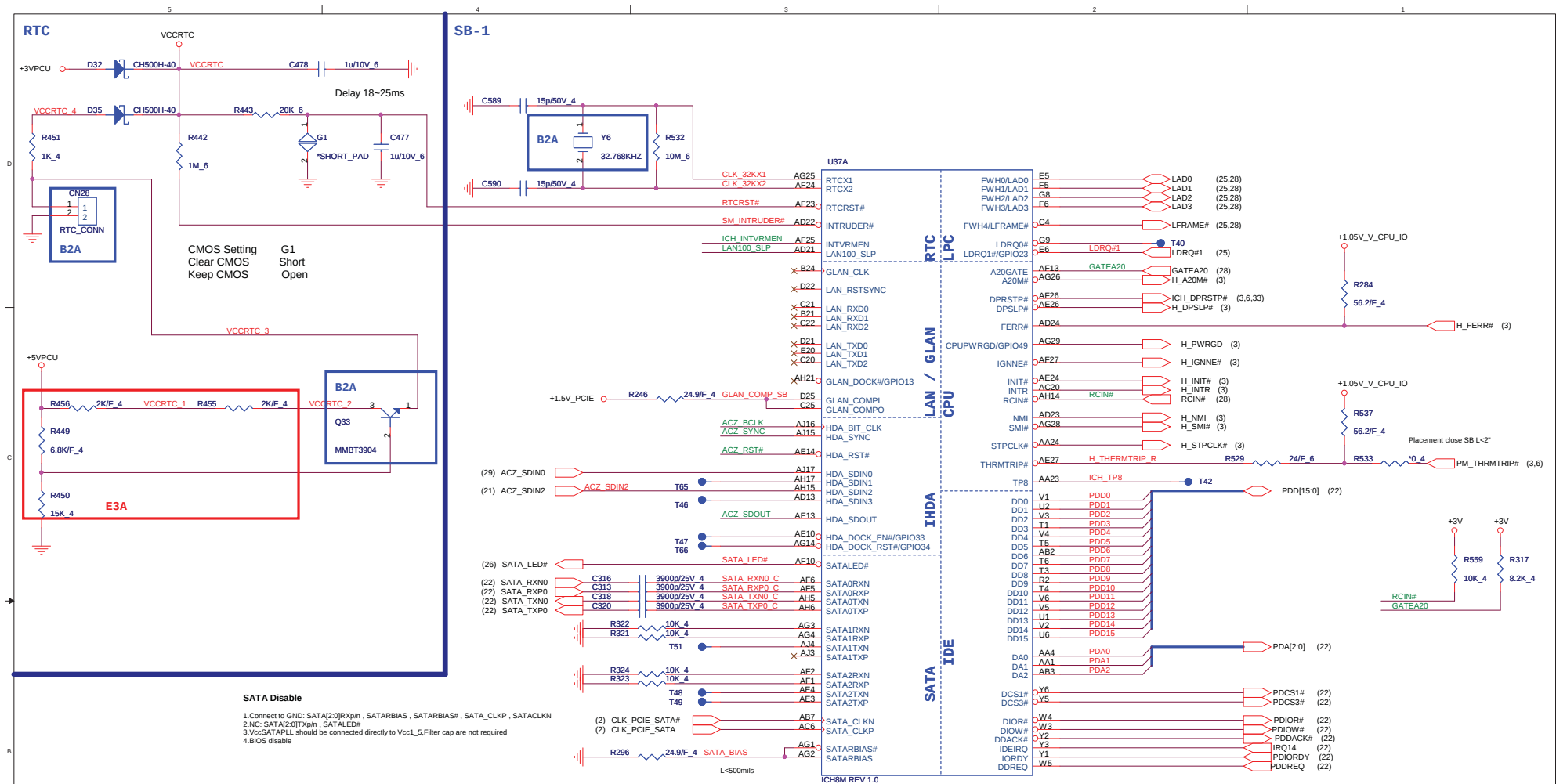


DDR2 B CHANNEL



Place one cap close to every 2 pull-up resistor terminated to SMDDR_VTERM

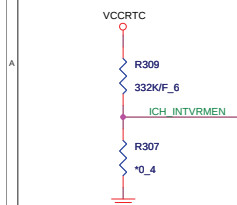




SB Strap

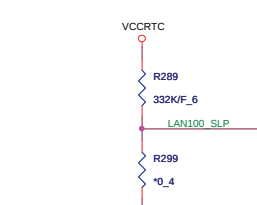
ICH8-M Internal VR Enable strap
(Internal VR for Vccsus1_05, Vccsus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
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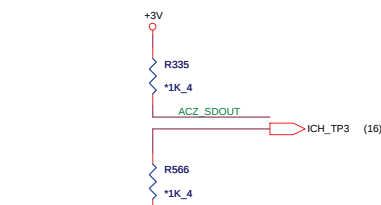
ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
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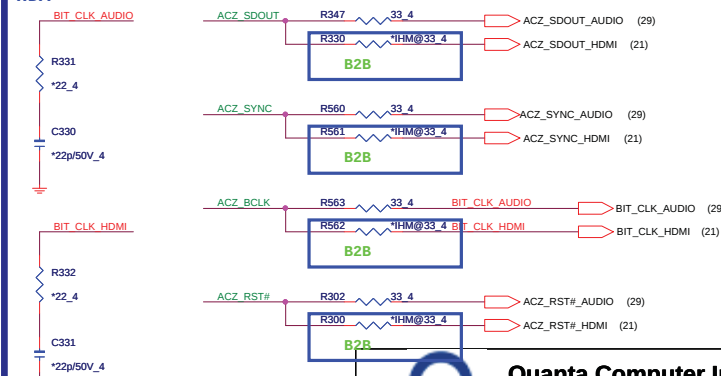


XOR Chain Entrance Strap

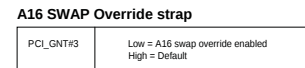
ICH_RSVD	HDA_SDOOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCI port config bit 1



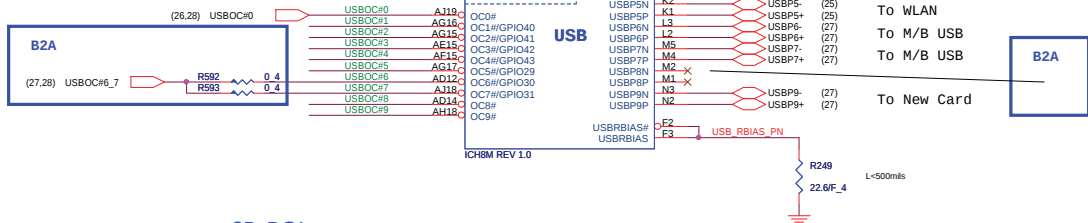
HDA



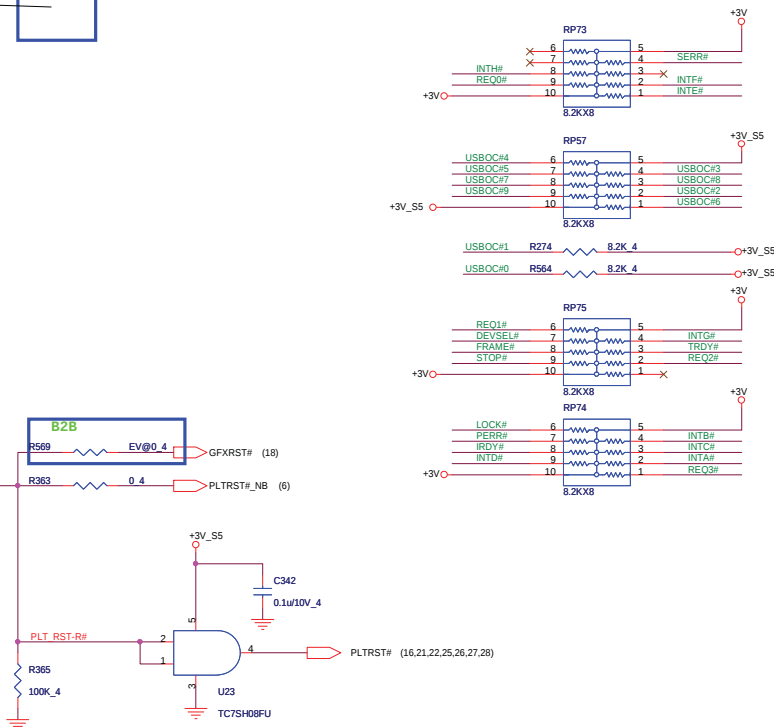
5	4	3	2	1
---	---	---	---	---



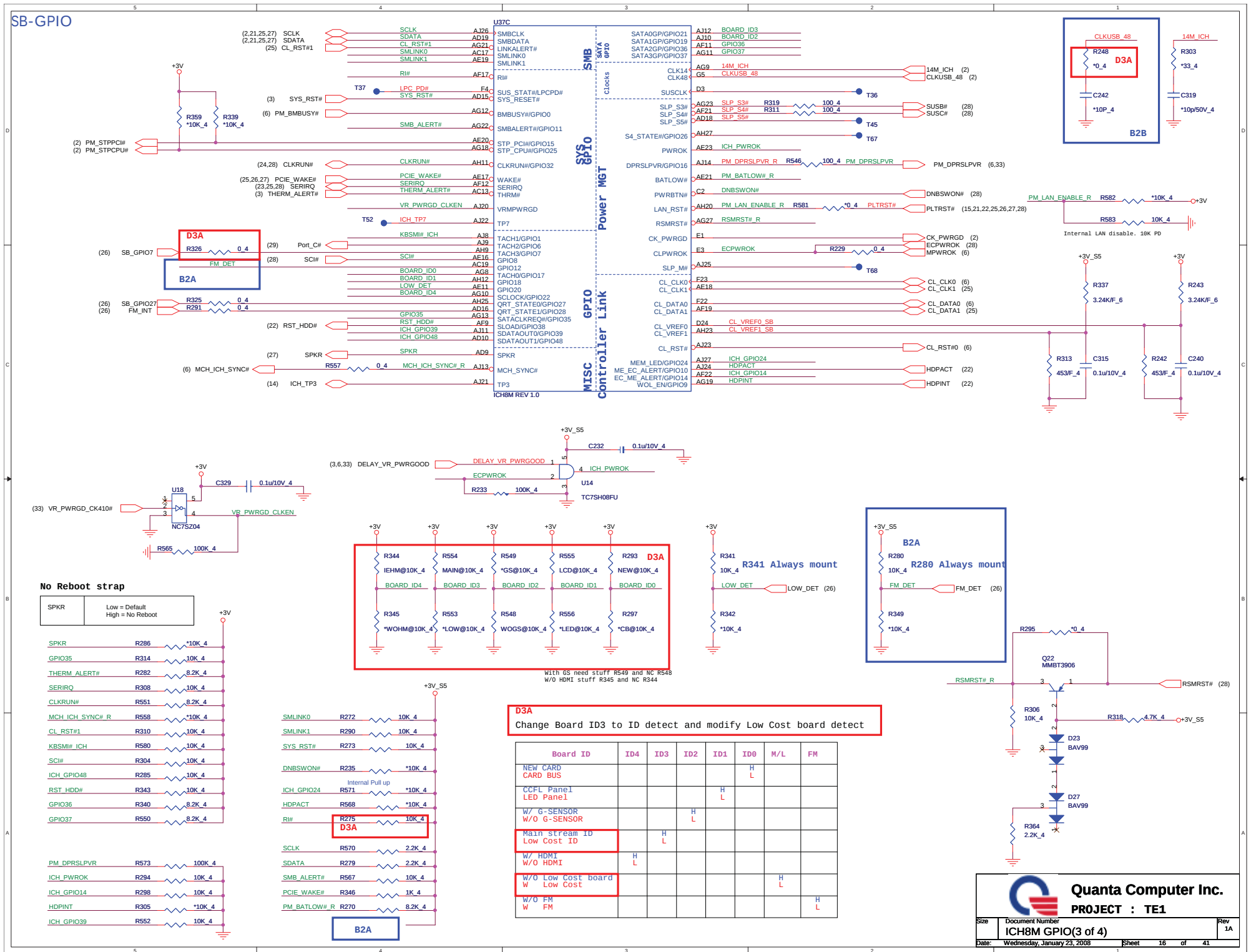
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

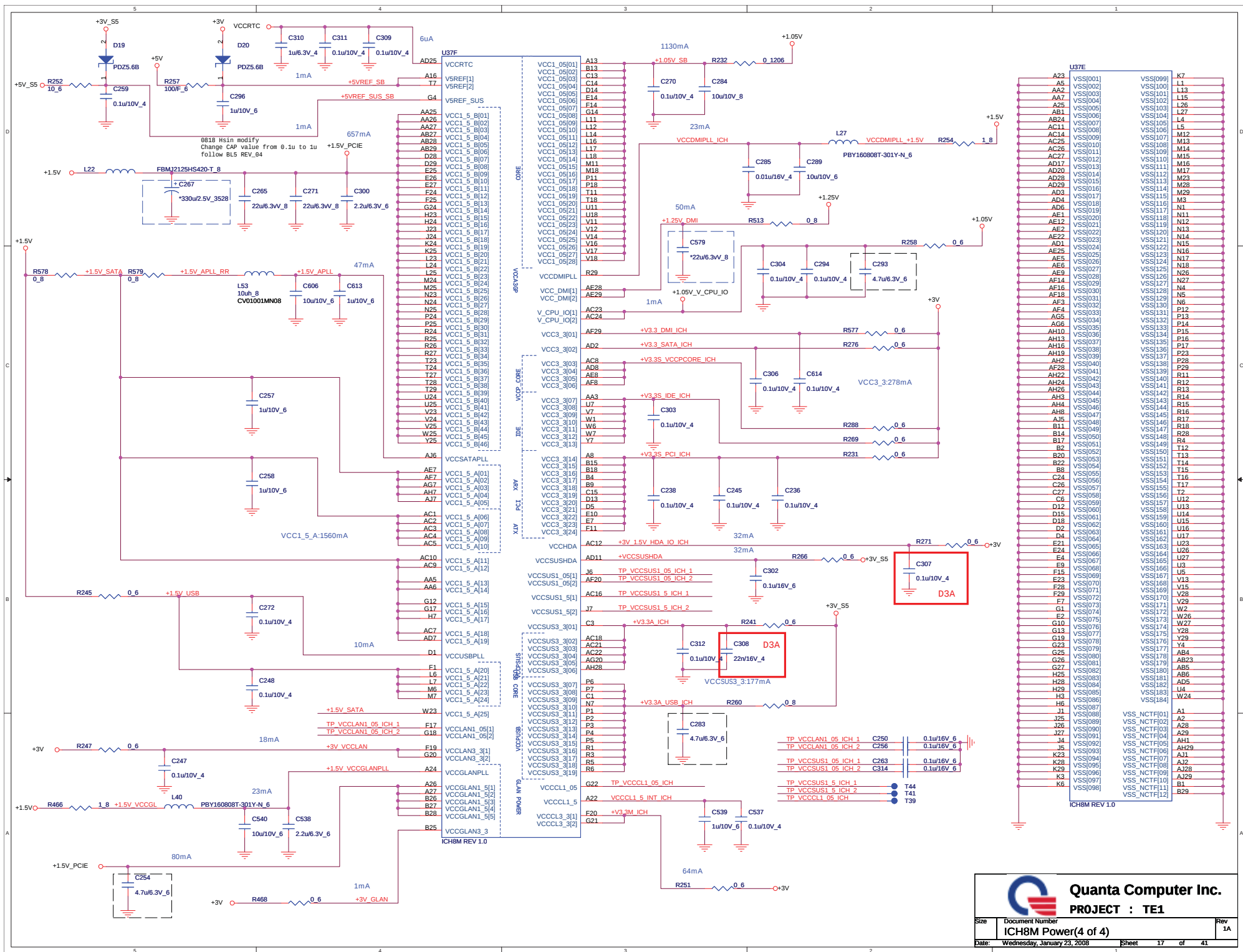
[illegible]

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#	OZ129T
REQ1# / GNT1#	AD20	INTC#	CB1410

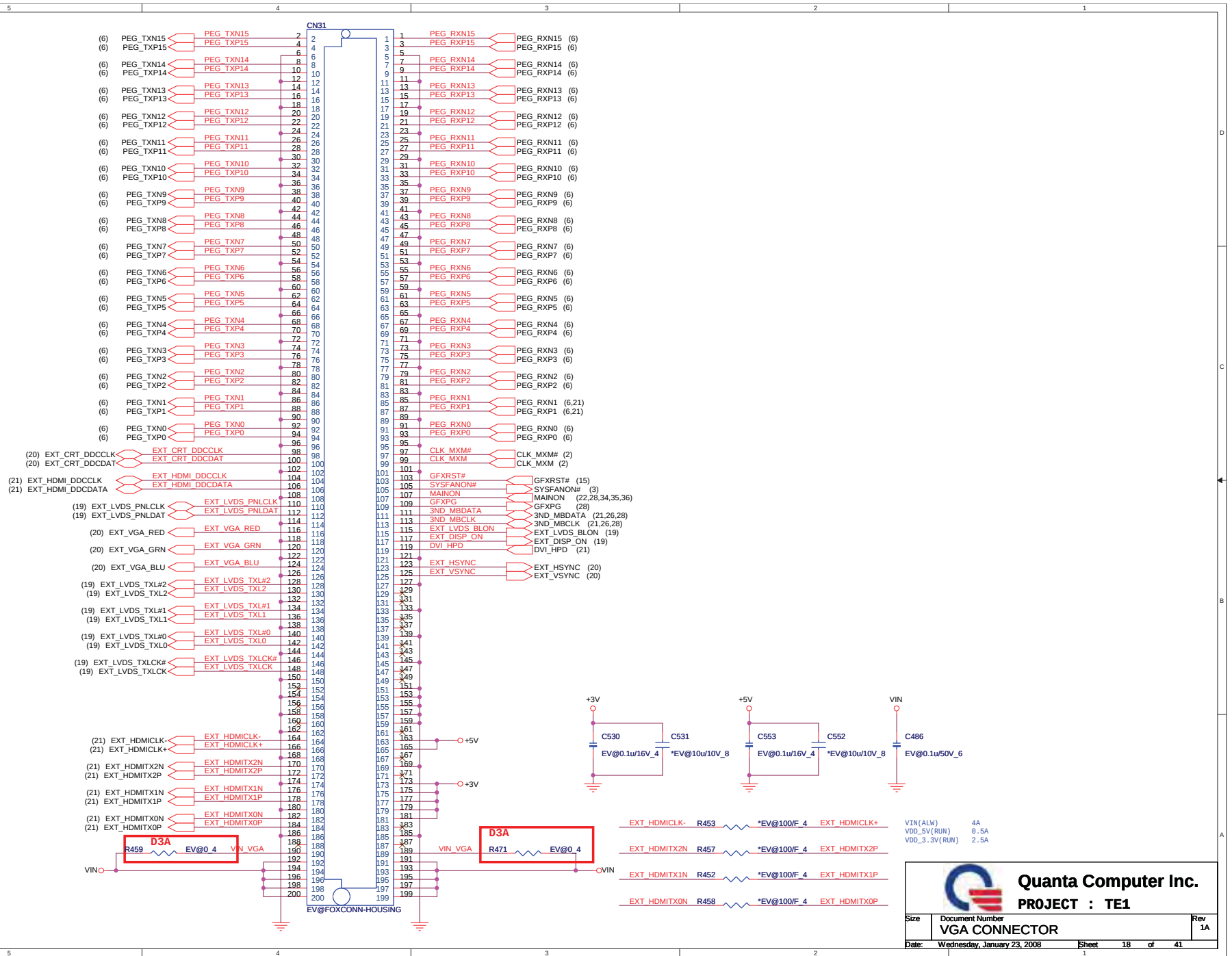


SB-GPIO

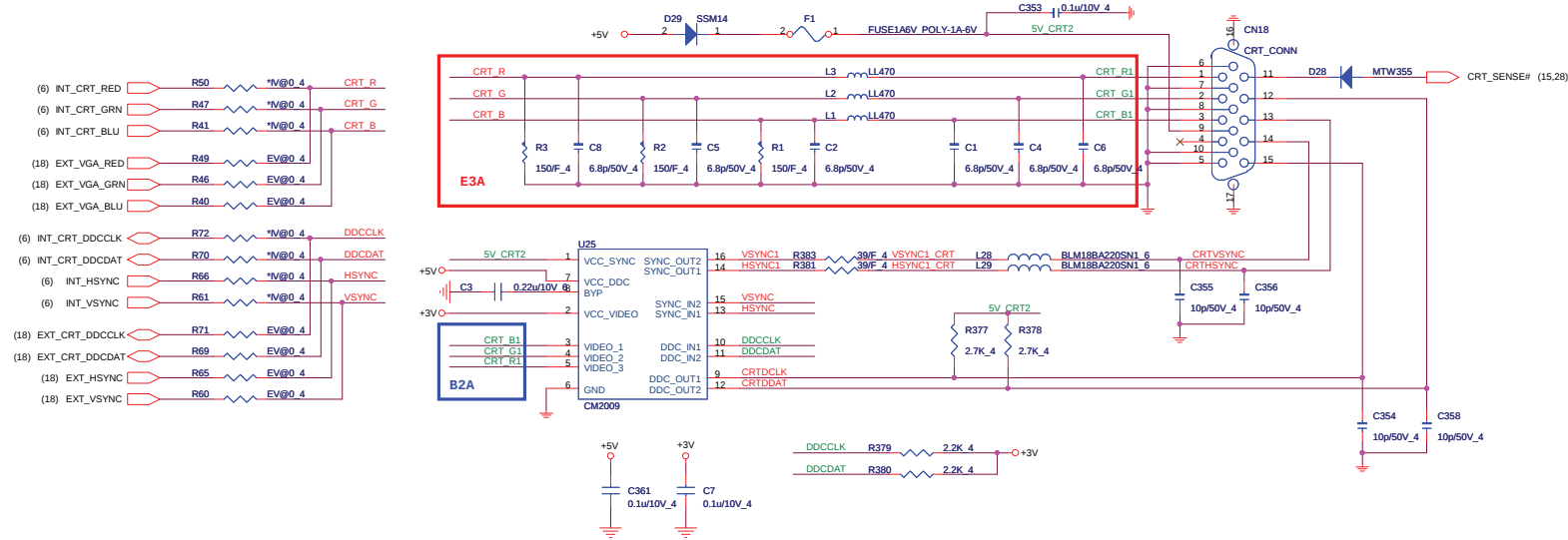




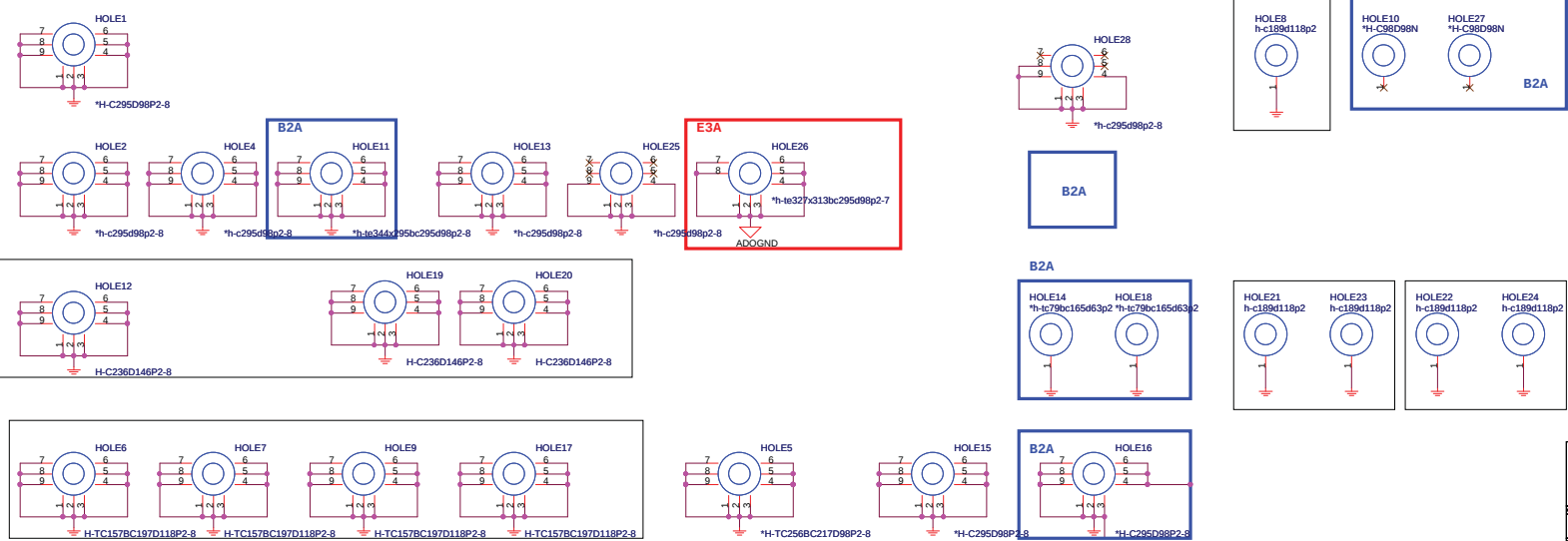
VGA/B conn



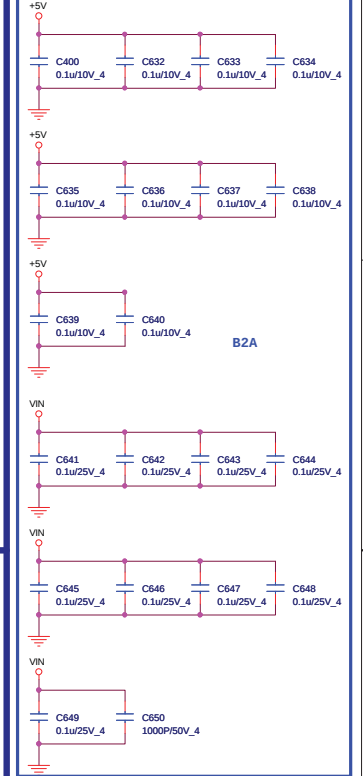
CRT

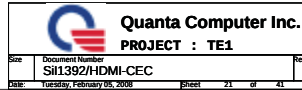


HOLE

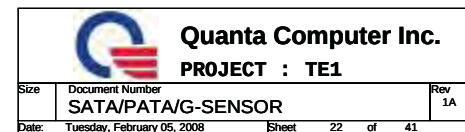


EMI





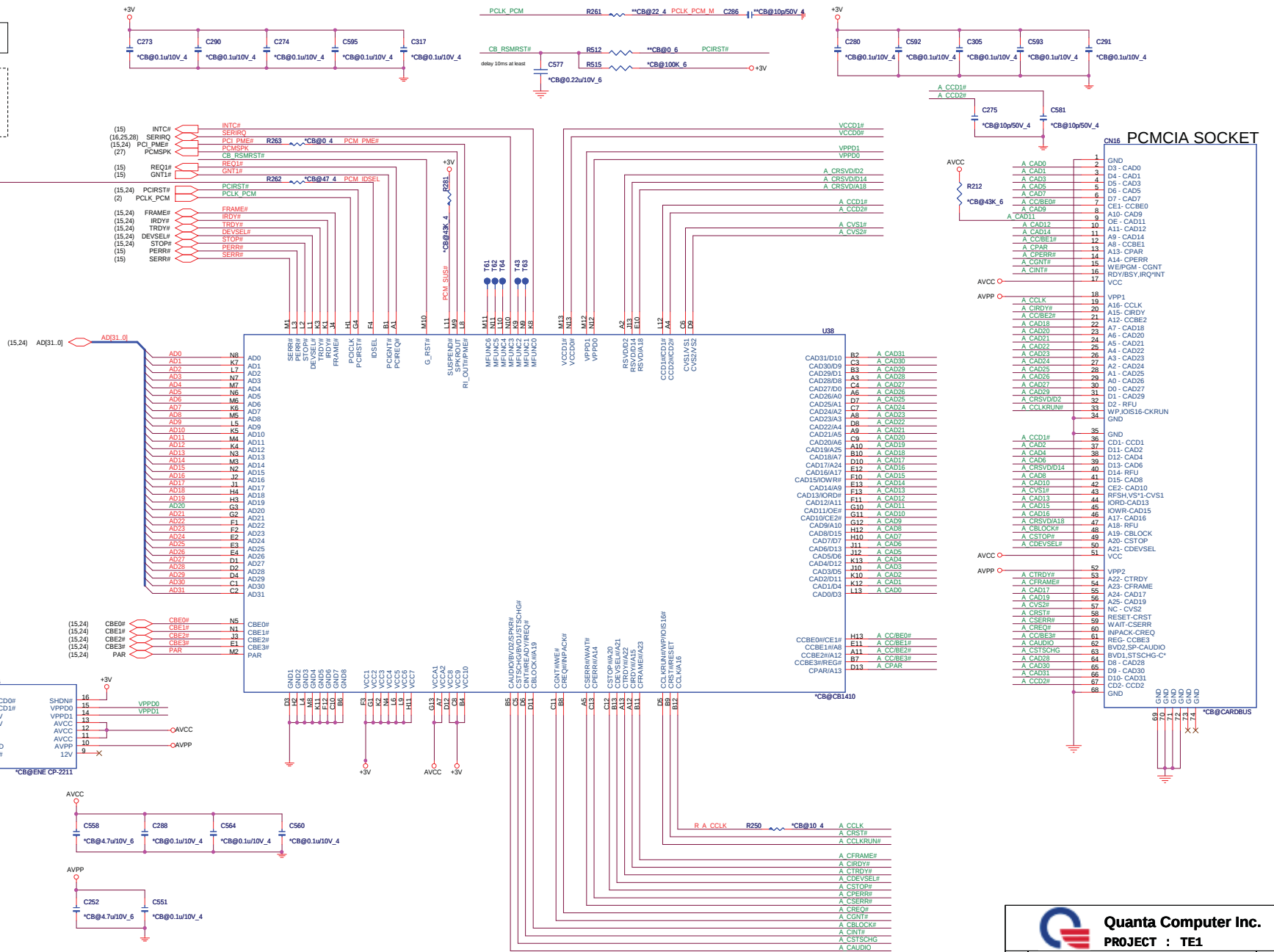
5VHDD (RUN) : 1A



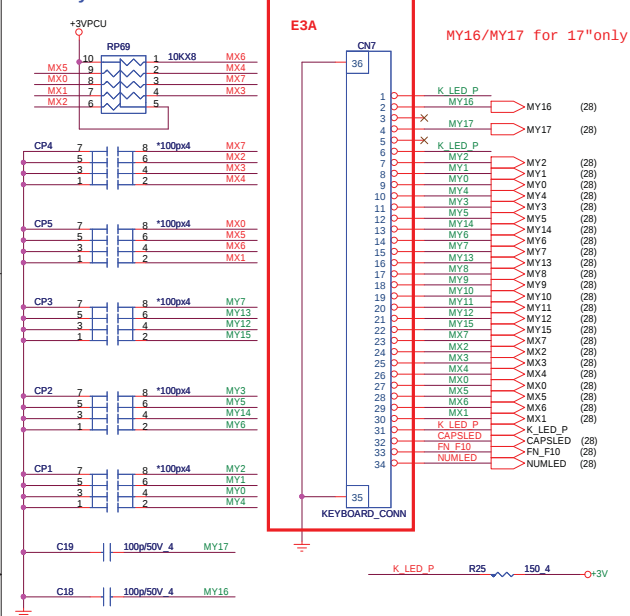
Cardbus

ENE1410 AJ014100T41

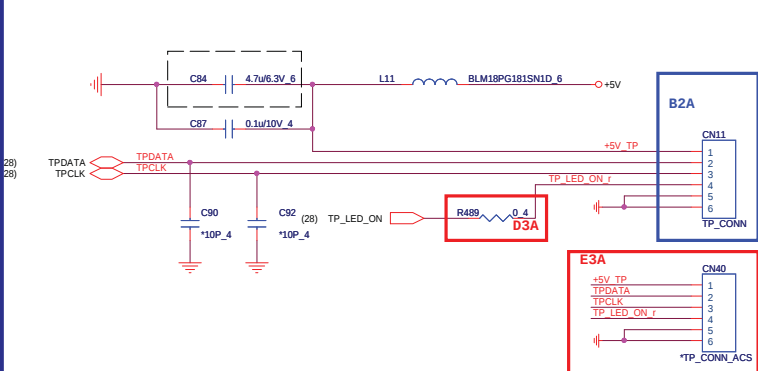
ID Select : AD18
Interrupt Pin : INTC#
Request Indicate : REQ1#
Grant Indicate : GNT1#



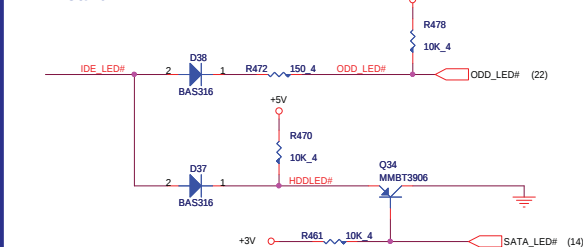
INT KeyBoard



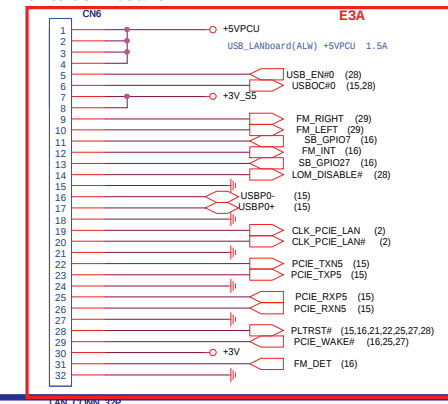
TP Board



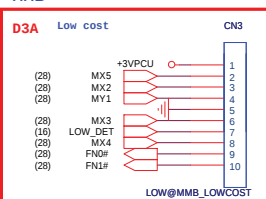
LED Board



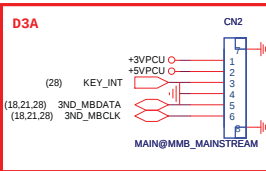
RJ45/USB board



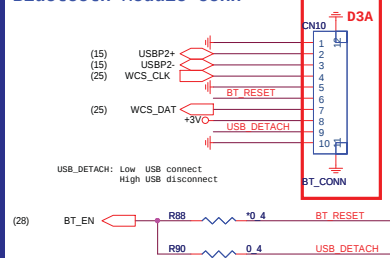
MMB



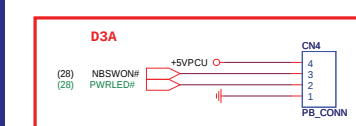
Main stream



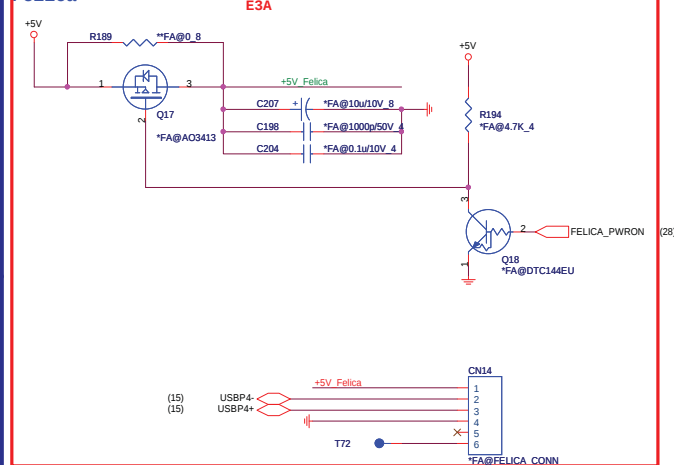
Bluetooth Module Conn



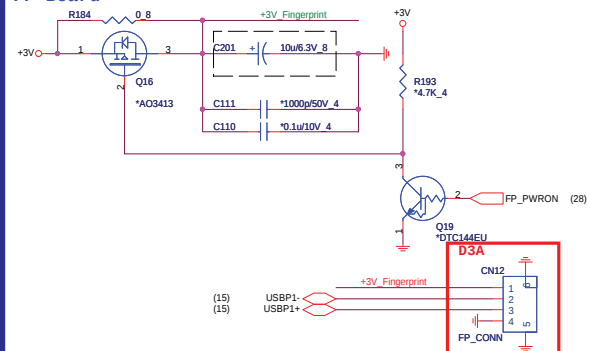
Power board



Felica



FP Board



Quanta Computer Inc.
PROJECT : TE1

Size	Document Number	Rev
	New Card/Keyboard/WTB	1A
Date:	Wednesday, February 13, 2008	Sheet 26 of 41

[illegible][illegible]

The diagram shows a PC-BEEP circuit. It starts with a 3V supply connected to a 10µF capacitor (C334). The signal path includes two 2N217 diodes (D24, D25) and several capacitors (C334, C344, C350, C356, C347, C333). The circuit is controlled by PCMSK and PCMSK_DELAY signals. The output is connected to a speaker (SPKR) through a 10K resistor (R338) and a 10µF capacitor (C333). The circuit is labeled (23) and (29).

Signal	Pin	Level
MBCLK	R395	4.7K 4
MBDATA	R394	4.7K 4
2ND MBCLK	R393	4.7K 4
2ND MBDATA	R392	4.7K 4
FN0#	R53	4.7K 4
FN1#	R52	4.7K 4
3ND MBCLK	R57	4.7K 4
3ND MBDATA	R58	4.7K 4
CRT SENSE#	R398	4.7K 4

I/O Address	
BADDR1-0	Data
0 0	XOR TREE TEST MODE
0 1	CORE DEFINED
1 0	2Eh 2Fh
1 1	164Eh 164Fh

SHMB: Enable shared memory with host BIOS

BADDR0 SHMB0 R56 +10K

BADDR1 BT_EN R385 10K

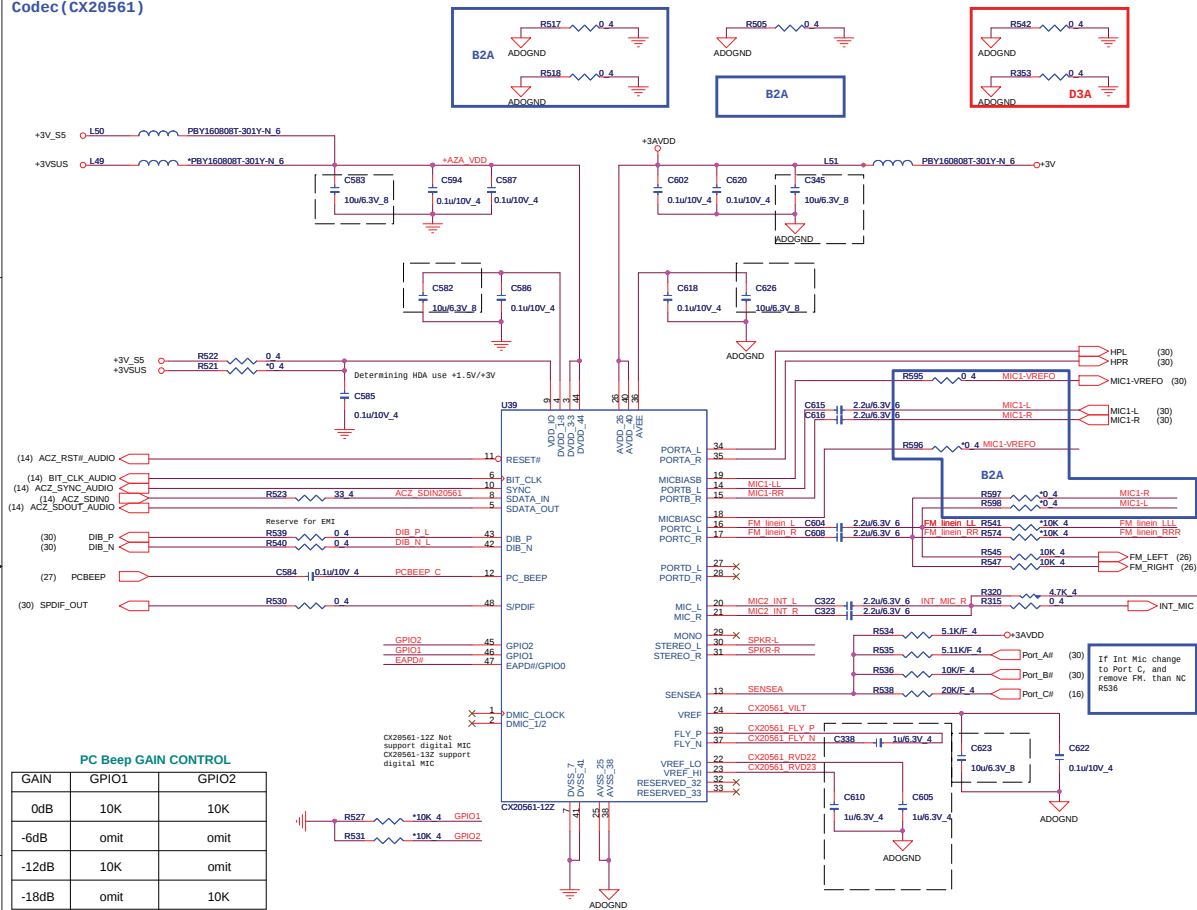
SHBM RF_EN R396 10K

Disabled (*) is using FWH device on LPC.
 Enabled (*) is using SPI flash for both system BIOS and EC firmware

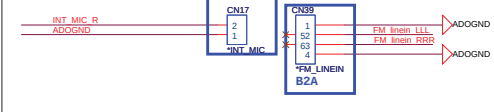
ADDRESS: A0H

MX25L8005M2C-15G	AKE5GFK0Z00
W25X80VSSIG	AKE3GFP0N00
EN25F80-75HCP	AKE3GZP0Q00

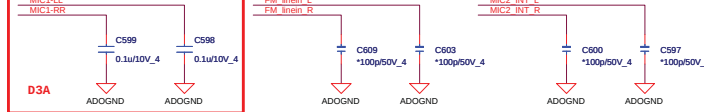
Codec (CX20561)



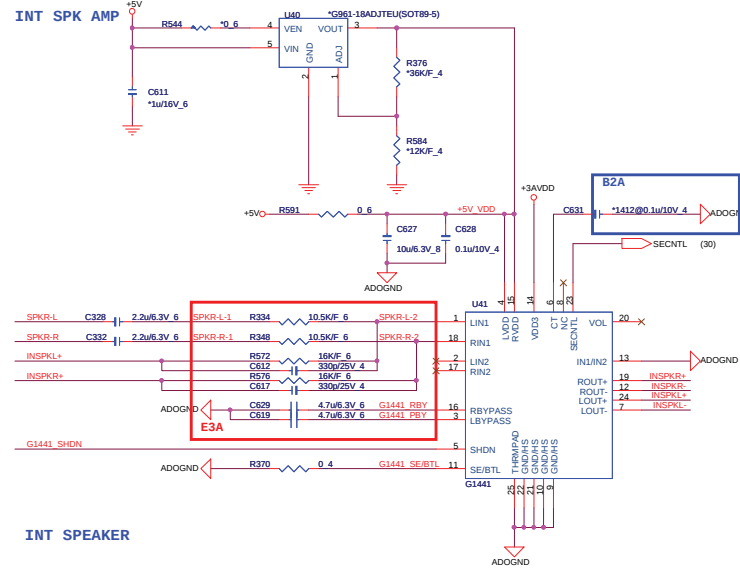
Reserve INTMIC



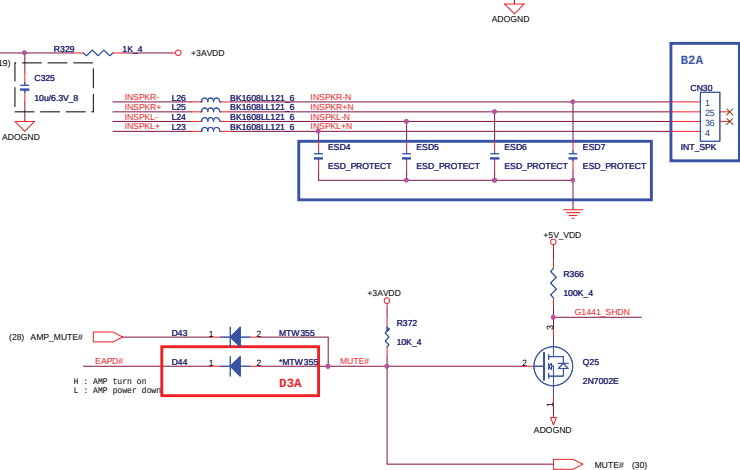
Reserve FM

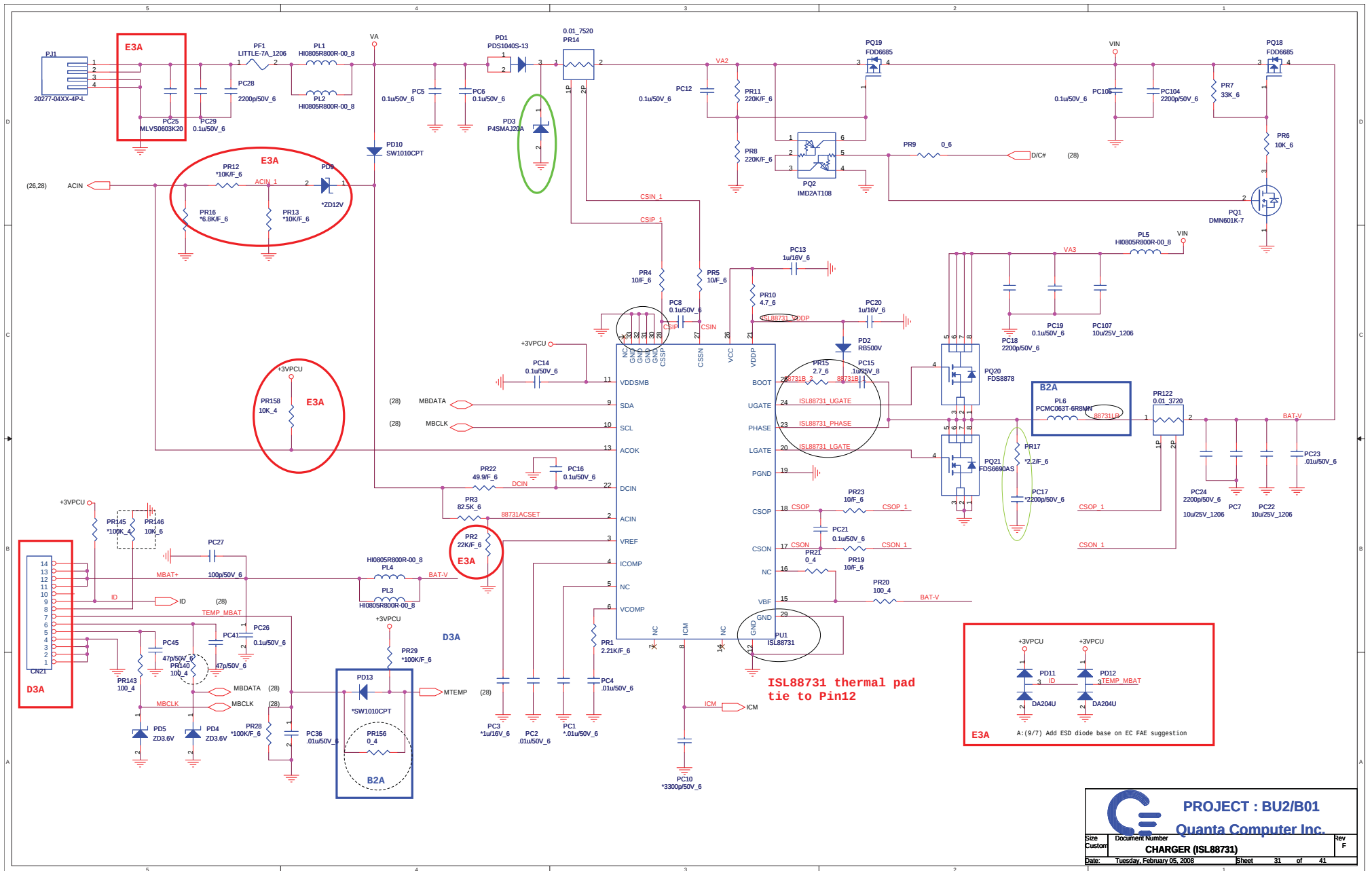


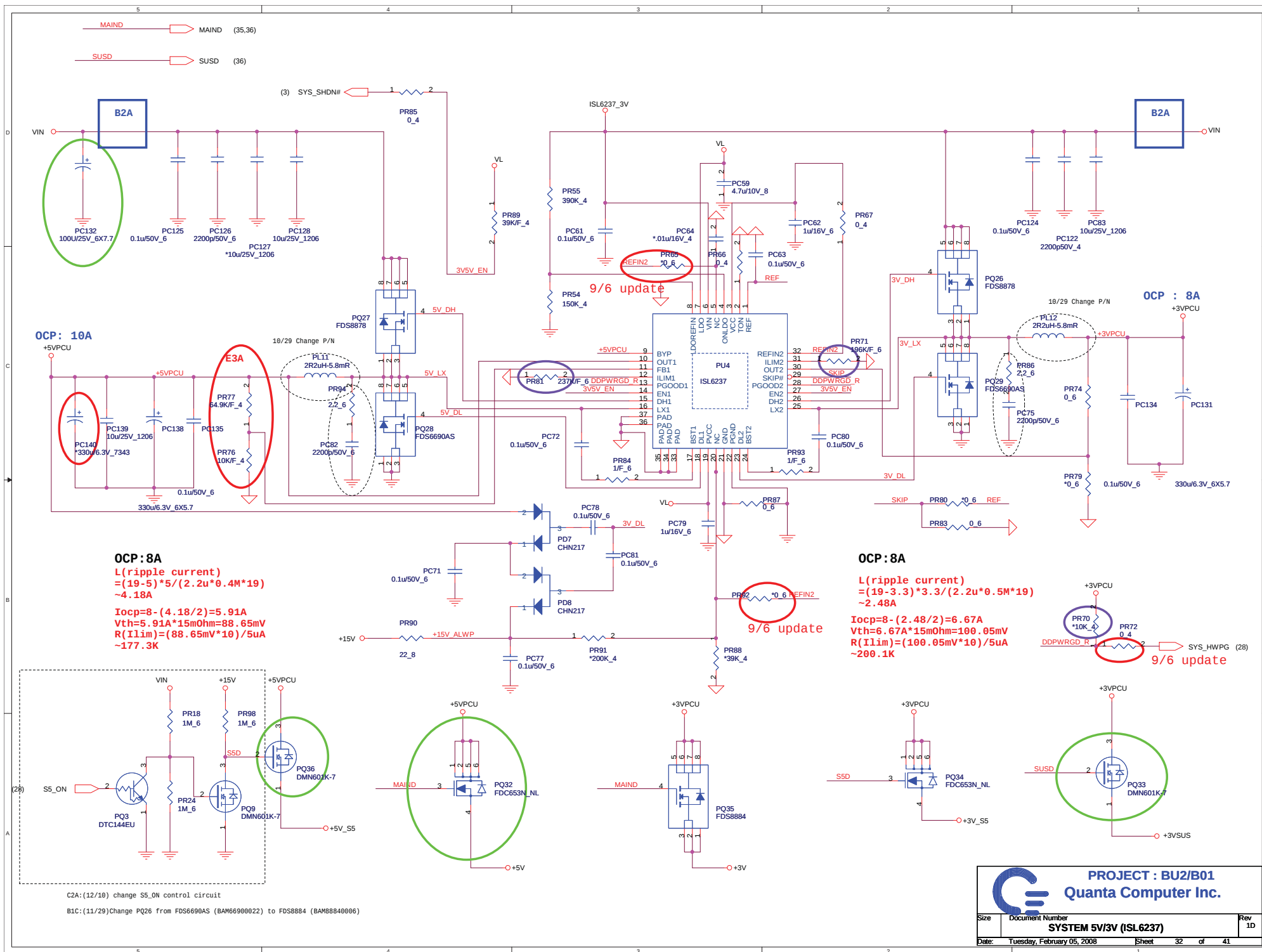
INT SPK AMP

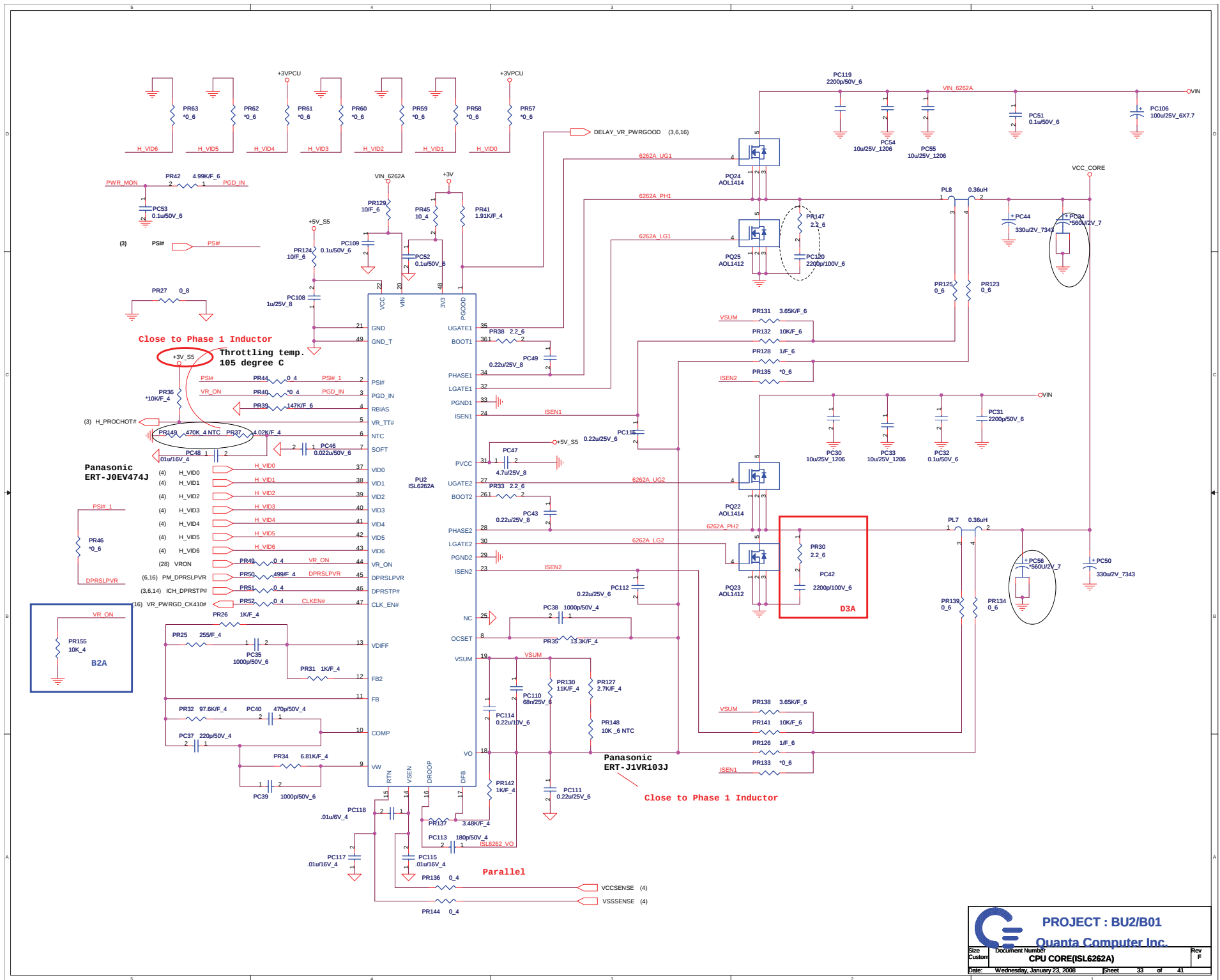


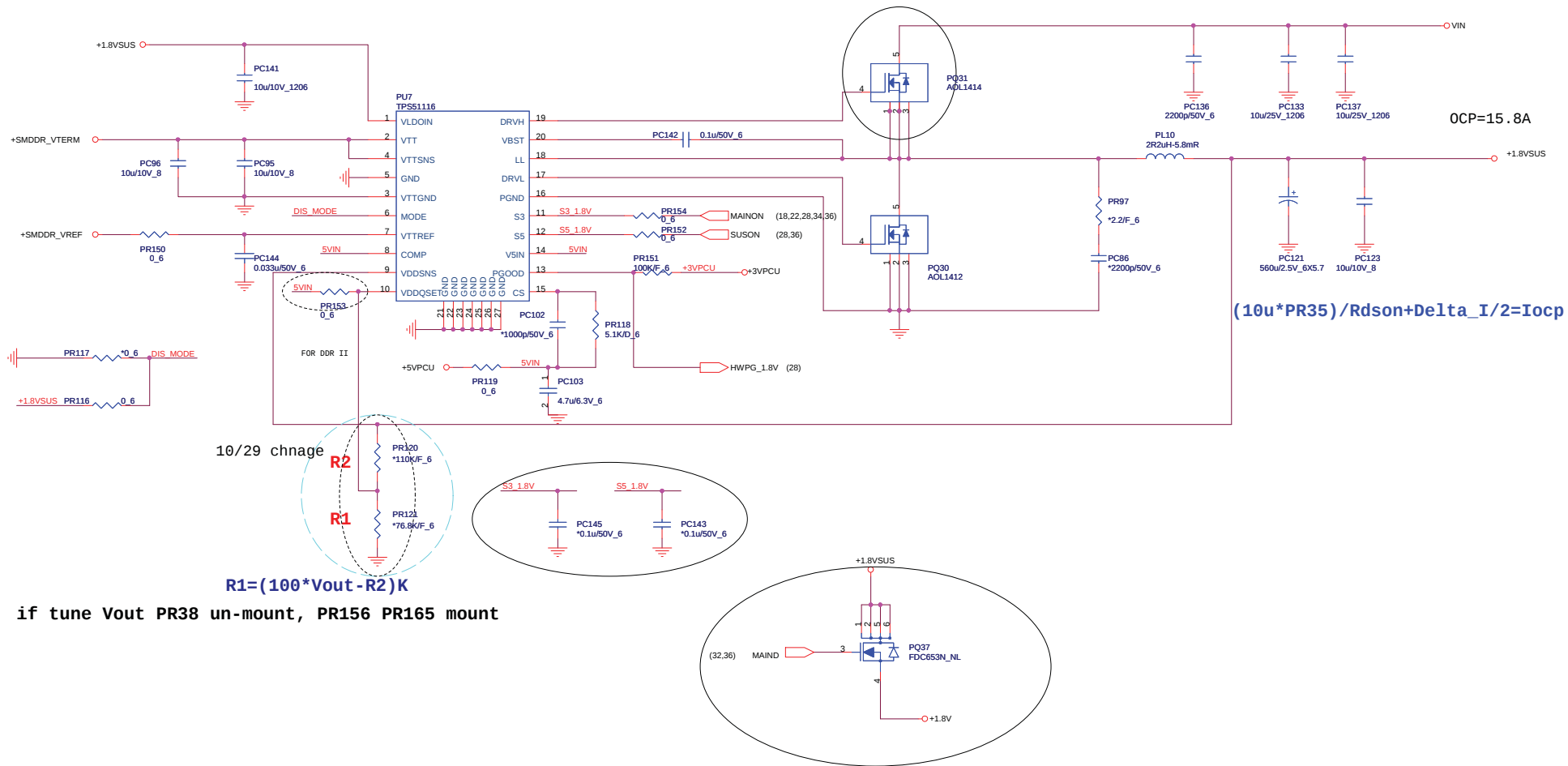
INT SPEAKER

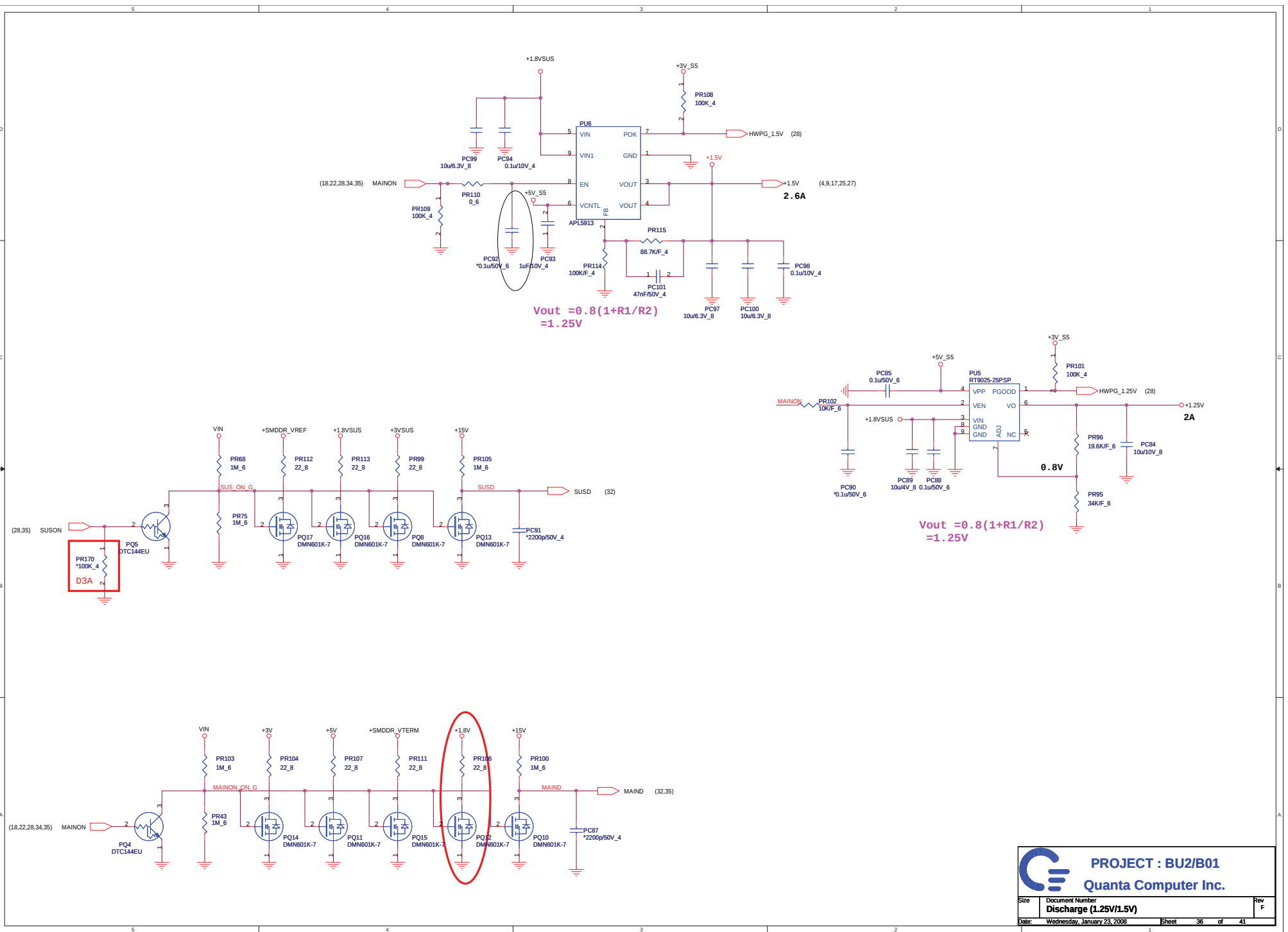












Model	REV	DATE	CHANGE LIST	NOTE
TE1	01	20070824	FIRST RELEASED : 20070824	
	A1A	20070927	FIRST RELEASED : 20070927	
	B2A		Page 22 : U31 for G-sensor SKU must stuff and add GS@ for BOM clear. Page 22 : Change Y4/C476/C485 Value from * to **, because Sensor function default not need that. Page 3/14 : Q6/Q9/Q33 BA039040039 change to BA0390400H0 for before BA039040039 cause RTC charger issue Page 28 : Change SW1 to short PAD for debug only Page 19 : For LED Panel C9/R10 always reserve Page 14/28 : Y1/Y6 shortage issue change from BG332768909 to BG332768224 Page 3 : R81 stuff 10K for OD pin Page 31 : CN21 BOM error, change DFHD07MR000 to DFHD14MS011 Page 17 : C540/C606/C289 CH6102ME904(EOL) change to CH6102M1909 Page 22 : U34 G-sensor P/N change same as BU1 from AL021174C00 to AR0BU1R0000 Page 21 : ESD1/ESD2/ESD3 always reserve for ESD solution. Change value to ** Page 18 : CN31/R471/R459/C530/C531/C553/C552/C486/R453/R457/R452/R458 add EV@ Page 27 : CN15(New card) change PCB Footprint to "ncard-13180151-u-26p1" Page 27 : U17 Value change from NEW@O227C10LN-B1 to NEW@O227C10LN-C1 Let P/N and Value match. Page 21 : UI1 P/N error, so change to "new part number" avoid before use error BOM. UI1 reserve for sil1392. Page 21 : U12 Value add IHM@ to BOM clear. To avoid BOM build error. Page 21 : U9 Value must modify from "CEC@R5F211A4SP to CEC@R5F211A4SP. To clear BOM. Page 25 : CN27/CN34 MINI Card clock connect error. CN27 must connect to CLK_PCIE_MINI3/3#. CN34 must connect to CLK_PCIE_MINI2/2#. Page 24/25 : C261/C246 must stuff before NC for A-test layout issue only. Page 3 : RP45 Value add NEW@ for new card clock BOM clear and better EMI result. Page 2 : R226 Value add *CB@ for PCMCIA clock BOM clear and better EMI result. Page 31 : PL6 Change PCB Footprint to "CHOKE-PCMC0631-3R3MN-BD3A" for SMT issue. Page 19 : U1 add pin27 to GND to meet PCB Footprint. Page 20 : U25 Pin3/Pin5 SWAP for layout smooth Page 30 : Del FM interface. Move to LAN/B and Del C400. Page 26 : LAN/B CONN change to 30pin(BL121-30R-30P-L-TE1, DFFC30FR009), and add FM interface Page 22 : C31 change Footprint from 7343 to 3528 for placement no space for EC Xtal move. Page 26 : CN13 Change Footprint to 88060-12001-12P-L for ME assembly issue. Page 28 : U42(CIR) Change PCB Footprint for SMT suggestion. And change P/N from BEBK0076200 to BEBK0038200 Page 29/30 : HP AMP NC. Reserve only. Page 26 : Del R103, TP(Mainstream/low cost control by TP/B) Page 15/27 : Add R592/R593 for USB port match OC port Page 21 : Add R103/R594/Q46/Q47/R600/R601 for CEC level shift(BOI mail). And adjust net name for ESD protect ESD1 close to connector. Page 29 : Reserve R595-R598 for Audio WHQL issue. (Can not multistream when FM not support. Page 27 : LED1/LED2 change type for ME. And modify LED4 Wimax LED circuit Page 20 : HOLE 16 add GND for ESD Page 21 : Del D13/R115/R116/D14 same as BL55 Page 28 : EC del MMB(10pin)LED0#1/1#2#. And move BT_EN/CRT_SENSE# Page 26 : CN2 modify Footprint to BL123-06R-6P-L-BL5, P/N to DFFC06FR336 Page 26 : CN4 modify Footprint to BL123-04R-4P-L-BL5, P/N to DFFC04FR012. And SWAP pin list for different Footprint Page 26 : CN11/CN14 modify Footprint to BL121-06R-6P-L-BL5, P/N to DFFC06FR003. Page 25 : CN8 modify Footprint to BL123-14R-14P-L-TE1, P/N to DFFC14FR009. Page 22 : CN19 change HDD Footprint to SATA-070820-QU001-22P-R-TE1 Page 2 : C231/C234 for Y3 TxC measurement suggestion change from 33p to 30p Page 24 : C580/C575 for Y3 TxC measurement suggestion change from 10p to 15p Page 20 : Del HOLE3 for ME request Page 26/28 : Add LOM_DISABLE# for LAN power consumption Page 2 : Change R214/R211 from 33ohm to 47ohm for EA fail. Page 29 : CN30 use same parts for BOI project. Change to SCY DF-WF04MS002. Page 20 : HOLE14/HOLE18 modify footprint for new card move 2mm for BOI request. Page 27 : Kill switch(SW2) change part for ME request. P/N is DHLLSS12P07 Page 14 : RTC Circuit R455/R456/R449/R450 follow standar circuit value(Enc Lee) Page 13 : CN24 Change Footprint from DDR-C-292564-200P to DDR-C-292564-200P-TE1 for connector fixed pad not meet Footprint. Page 15/25 : Not support TV. Del USB8 and add T71/T73/T74/T75 Page 24 : C542 stuff 22p for EMI issue. Page 29 : Add R517/R518 0 ohm for EMI issue. Page 20 : +5V/VIN add 0.1u to shape for EMI issue Page 17 : SB CAP cost down C579/C267 Page 9 : NB CAP cost down C119/C458/C69/C155/C403/C149/C443/C436 Page 2 : CLK CAP cost down C541 Page 24 : Card reader cost down, del 0 ohm Page 19 : C16 change BOM/Footprint from CH6101M9905 to CH61001ME96 for cost down Page 27 : C262/C266/C84 change BOM/Footprint from CH5472K9A02 to CH5471M9907 for cost down	

Model	REV	DATE	CHANGE LIST	NOTE
TE1	B2A		Page2429 : C567/C338/C610/C605 change BOM from CH5102K9B06 to CH5101K9B01 for cost down Page?? : C566/C261/C607/C321/C482/C532/C201/C583/C582/C345/C626/C325/C623/C360/C24/C281 change BOM from CH6102K9A01 to CH61001ME96 for cost down Page4 : CPU CAP C35 BOM change for cost down from CH733LM8812 to CH733RM8858 Page9/17 : C293/C254/C283/C102 cost down from CH5472M9901 to CH5471M9907 Page19 : C27 change BOM/Footprint from CH61004M398 to CH61004M291 for cost down Page16 : Add FM_Detect pin to GPIO12 Page3 : Del C50,Add R115/R116 for shut down circuit Page16 : Add FM_Detect pin to GPIO12 Page20 : HOLE11/HOLE28 modify Footprint for ME issue Page29 : Del R528 for no space adjust modem trace Page32 : Del JP1/3P2 Page19 : Reserve R473/R474 200K for LED drive IC Page33 : Add PR155 for VRON stable Page31 : MTEMP add PD13/PR156 Page21 : CN23(HDMI) Connect chnge Footprint and library pin define for correct library from HDMI-C12815-119A5-L-19P-V to HDMI-C12815-119A5-L-19P-V-TE1 Page26 : CN6 apply pin 31 and pin32, modify new footprint : BL121-32R-32P-L-TE1 Page29 : Change C224, C226, C227 and C228 to 'ESD PROTECT (ES04, ESD5, ESD6 and ES07 : DIODE SMD V-PORT-0603-220K-V05)' Page20 : C650 change to 1000P from EMi request Page28 : Apply isolate TP_LED_ON from EC to Mainstream TP Page20 : C641 - C649 apply to CC0402 = CH4104K9B03 Page31-38 : Update power circuit to TE1_965PM_B2A-1030-1030 Page20 : L1-L3 change to CX8LL470000 from EMi suggestion Page20 : Modify Hole26, NC GND net for layout issue Page21 : *HM@1000p/16V_4 change to *HM@1000p/50V_4 Page25 : C468 change Value from 0.01u/25V_4 to 0.01u/16V_4 Page25 : CN27 change to DFHD52MS146 Page19, 29 : INT_MIC change PN to DFHD02MR003 Page29 : CN39 change to DFHD04MR012 Page26 : CN13 change to DFFC12FR006 Page14 : CN28 change to DFWF02MS000 Page29 : R351, R354 change footprint to RC0603 Page26 : modify Low cost MMB pin define, CN3 pin2 change to MX5 Page28 : apply R486, R485 and R477 PU for Battery LED issue follow BL5 Page15 : Del T73, T71 for layout isse (use via to measure) Page20 : del Hole10 and Hole 27 GND pin (layout issue) Page30 : Stuff R357 and R369, reserve C343 U24 R367 Q24 for VR smooth modify Page21 : R144 Value add /F	
	B2B		Page21 : Q7/Q8 Value add CEC@ for BOM option Page21 : F3 Value add IEHM@ for BOM option Page4 : C40/C41 stuff for power measurement issue Page28/31 : PR29 NC / R54 stuff 100K/F for S.Y request Page30 : R516/R543 stuff 1K / R354/R351 stuff 10u/10V_6 Page30 : VR1 change P/N from CK0000RZ004 to CK0000RZ005 Page15 : R569 Value add EV@ for BOM option Page14 : R300/R330/R561/R562 Value add *HM for BOM option Page19 : C13 change to 33n / R14 change to 499/F, and reserve R473 and R474 Page : C289, C540, C606, R351, R354 change to CH6101M9905 for Buyer issue Page16 : Stuff R248 and change 0.4, and Stuff C242 change to 10p_4 for CLKUSB_48 EA1tail issue Page30 : CN20 change PN to DFHS12F5000 with SUY forbidden issue Page28 : Add R385 and NC R56 for Boardcom BT issue	
	C2A		Page04 : C40 change Value to PC146, C41 change to PC147 Page30 : R354 change Value to C651, R351 change to C652 Page31 : Mirror CN21 Pin define Page25 : CN35 change footprint:MIPCI-88958-5204M-52P-H Page28 : C379 and C401 change PN to CH6102K9A19 with BOI issue Page25 : CN35 change to DIP type (footprint:MIPCI-88958-5204M-52P-V), Part Number (DFHS52FR013) Page24 : CN37 change footprint to (4IN1-CMAR-118-43P-L-V), Part Number (DFHD42MS005)	

Model	REV	DATE	CHANGE LIST	NOTE
TE1	D3A		Page19 : modify MR senear with BLON circuit to solve flashing issue when system shut-down Page30 : Change Q24 to U43 to solve VR not smooth Page31,32 : Change Charger circuit to use ACOK to inform EC Page29 : NC D44 to solve switch mute to un-mute, sound will delay about 2seconds Page24 : Apply R351, R354, R367, R487 and R488 for EMI request Page20 : EMI suggest used LL680 + 4.7 pf x6 cap to avoid CRT issue Page19 : Apply U44 circuit for LED panel black light issue Page27 : Change LED1 and LED2 to new part Page3.5 : Apply L54 near CPU side and C666 near NB side for ESD issue Page36 : Reserve SUSON PD resistor Page28 : Apply R489 reserve for TP_LED_ON enable(Low Cost ID) Page03 : NC C71 for Fansing speed issue follow BL55 Page-- : Logo LED, function board conn and Board ID Value apply function option Page21 : HDMI conn change footprint to HDMI-C12815-119A5-L-19P-V-BU2 Page25 : Led board conn change PN and Footprint : DFFC12FR285 Page25 : Function board conn (mainstream and lowcost) change PN Page20 : Hole26 change footprint to h-te327x313oc295d98p2-7 Page22 : SATA conn change Footprint to SATA-070820-QU001-22P-R-TE1 Page-- : DDR socket CN24 change PN to DGMK0000040 WLAN minicard conn change PN to DFHS52FR016 Battery conn change PN to DFHD14MS014 ODD conn change PN to DFHS50FR034 1394 conn change PN to DFHS04FR109 Kill switch change PN to DHLLS512P02 FP board conn change PN to DFHD04MRA75 BT conn change PN to DFHD10MR008 CN3 change PN and Footprint is BL136-10R-10P-L CN2 chaneg PN and Footprint is BL136-06R-6P-R Page-- : R275, C307, C308, R326, R293, R248 change Footprint to -C (circle pad) Page30 : Reserve R490 near VR for ESD portect Page28 : Reserve C33 near CIR for ESD portect Page30 : Reserve C656, C657 for audio noise debug Page21 : NC R136 and C131 to solve HDMI I-diagram fail Page30 : Stuff AMP1412 circuit for audio noise test Page30 : Change L52, L47 to BK1808L1121 and C578 and C601 to 0.1uF to test 3G/GPRS ExpressCard noise in HP. Page29-30 : C599, C598, C569, C568 apply to CH41002KB93, And L45, L46 change to CX8LL121002 for INT MIC recording noise. Page30 : NC R516 and R543 to meet HP Jack signal measure and HP plug- unplug haven't happen bobo-sound too. Page30 : Change C578 and C691 for 0.1u to 0.22u to enhance avoid 3G noise and meet HP Jack signal measure Page25 : Mini card 16GB, MB8-MB11	

Model	REV	DATE	CHANGE LIST	NOTE
TE1	D3A		Inner Document Change C221 to CH01506JBD9, and NC R248, C242 for CLKUSB48 measure pass Add R353 to CS00002JB38 for ESD request Change CN4 PN to DFFC04FR213 Add R459 and R471 to CS00002JB38 for EV request Remove Felica function at EV sku Remove MAIN@ parts at Low Cost ID Q26,Q27,R374 and R375 Add R542 and R490 for ESD request Change R516, R543, C578 and C601 to CH41002KB93	
	E3A	20080116	Page21 : Change HDMI connector footprint to B test (HDMI-C12815-119A5-L-19P-V-TE1) Page26 : Change CN6 to BL134-32RL-TAIG-32P-L Page20 : Hole26 apply AGND pin for ESD Page30 : HP jack pin9,10 apply GND for ESD Page19,31 : Power modify for LED panel Page26 : Apply CN40 for TP connector 2nd source(ACS) Page21 : Change U9 PN to ARBL5MV0000 Page24 : PD XD_WPOH_C with R491(reserve) for XD measure Page26 : Change the footprint of DFFC34FR003 from 88171-3400L-34P-L to 91504-340N-34P-L Page20 : Change L1, L2 and L3 to CX8LL470000, Change C1, C2, C4, C5, C6 and C8 to CH-686T0B07 for EA CRT measure pass Page16 : Change R345 Value to WOHM@10K_4 and Change R548 to WOGS@10K_4 Page26 : Apply FA@ at Felica function Parts Value Page27 : Apply MAIN@ at Q26,Q27,R374 and R375 Page30 : R516 change to C659, R543 change to C658 Page31 : Apply varistor PD11 and PD12 to BCDA204U209 for ESD request Page30 : Apply ESD9, ESD9(BC03220KZ19) and C660 in HP_3P for ESD solution. Page27 : Change R374 and R375 from 390ohm to 150ohm base on ME request for LED light not enough Page27 : Modify New card footprint to NCARD-13180151-U-26P-L-TE1 Page26 : NC CN13 pin3 to follow LED board Page31 : PL6 change PN to CDRH104R-TE1 Page19 : Apply PN in R10 to CS33742FB11 Page14 : Modify RTC circuit to follow BL5S Page30 : Remove 1412 Amp circuit Page29 : Modify speaker gain to 9.7dB, R334 and R348 change to CS31053F909, R572 and R576 change to CS31603F916 Page27 : Change new card power switch to TI (AL002231000) Page24 : NC C542 for customer request, O2 spec can't over 10p	
	E3A-01	20080125	BOM release E3A-01 Page30 : Change C651 and C652 to 0_6 Page24 : Change R488 to 33_4 Page32 : Change PR76 to 10K/F and stuff PR77 to 64.9K/F Page24 : Change VR1 PN to CK0000RZ006 E3B Page14 : remove T50 Page19 : apply R14 Value to LED@ Page25 : remove R312, R301 and R327 Page21 : CN23 apply IEHM@ in Value Page31 : PC25 change to CY060320901 for ESD Page27 : NC C264 and R253 from CS32872FB11 change to CS00002JB38 F3A Page7 : EC Pin 27 connect to DISPON Page22 : Q38 pin2 change to +3V_S5 Page19 : Change CN4 to DFFC04FR012	