

Compal Confidential

ZRMAA/ZEMAA Schematics Document

Haswell ULT with DDR3L

nVIDIA N14P-GV2 (Dual Rank)

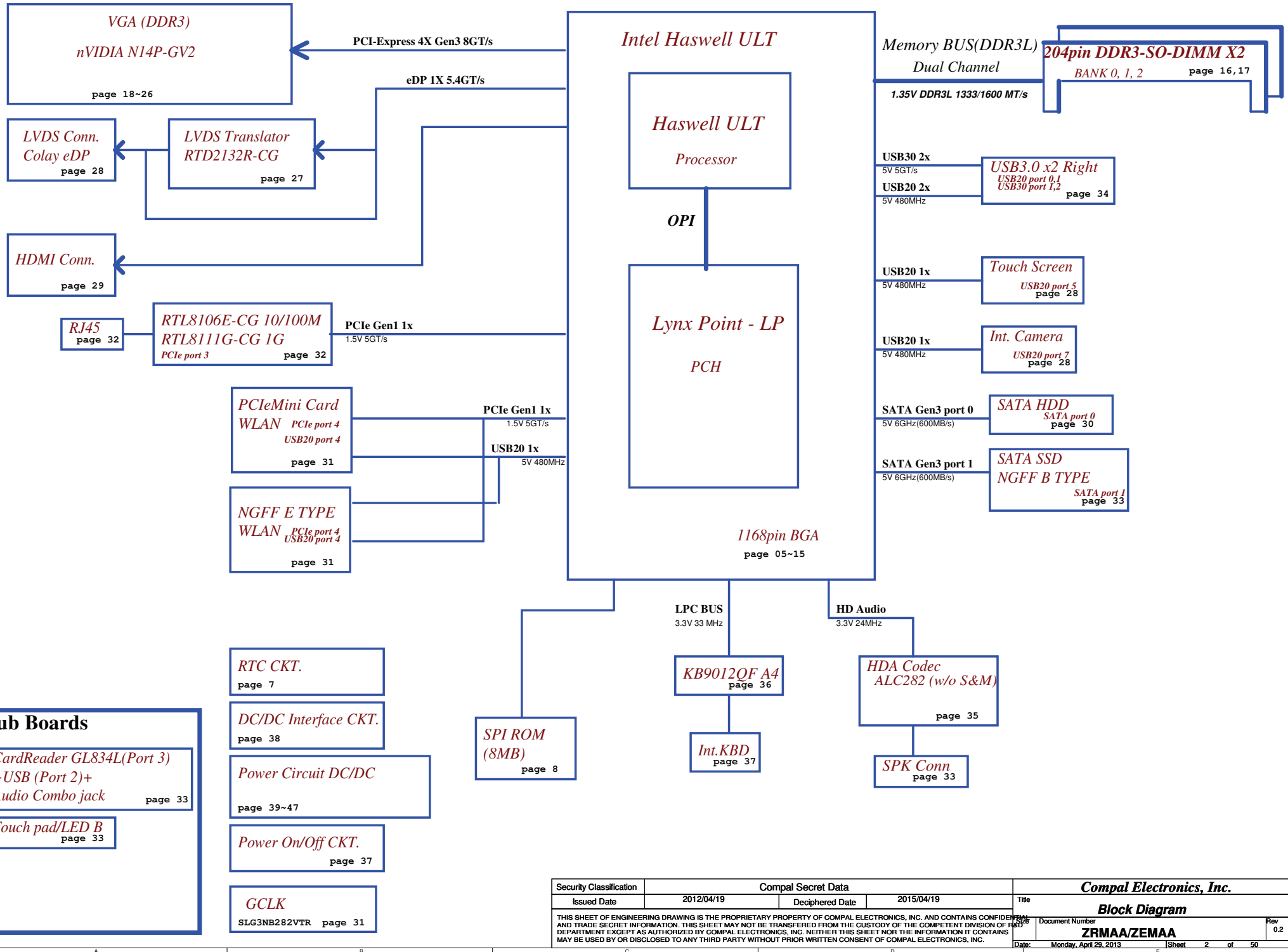
nVIDIA N14M-GL

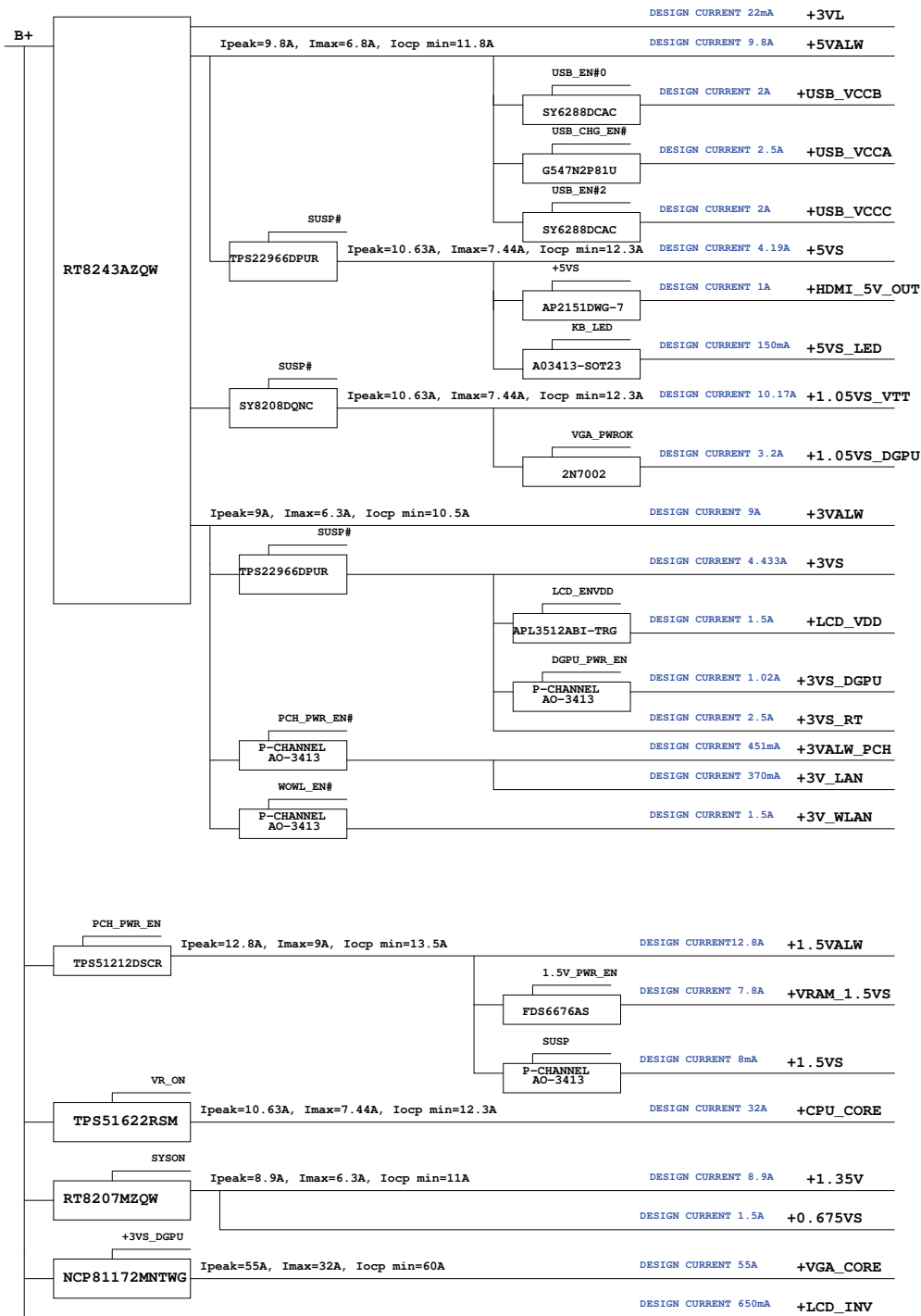
LA-A481P REV 0.2 Schematic

Intel Processor (Haswell)

2013-04-9 Rev 0.2

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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	Cover Page
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Voltage Rails (O MEANS ON X MEANS OFF)

power plane \ State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.5VALW +VSB	+1.35V	+5VS +3VS +1.8VS_CRT +1.5VS +CPU_CORE +VGA_CORE +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU +1.05VS_VTT
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9E H	1001 1010 b

Power	Device	HEX	Address
-------	--------	-----	---------

Platform	SKU	CPU	PCH	VGA
				nVIDIA N13P-GL (N13PGL@)

BTO Option Table

Function	SKU	MIC	LAN			
description						
explain						
BTO						

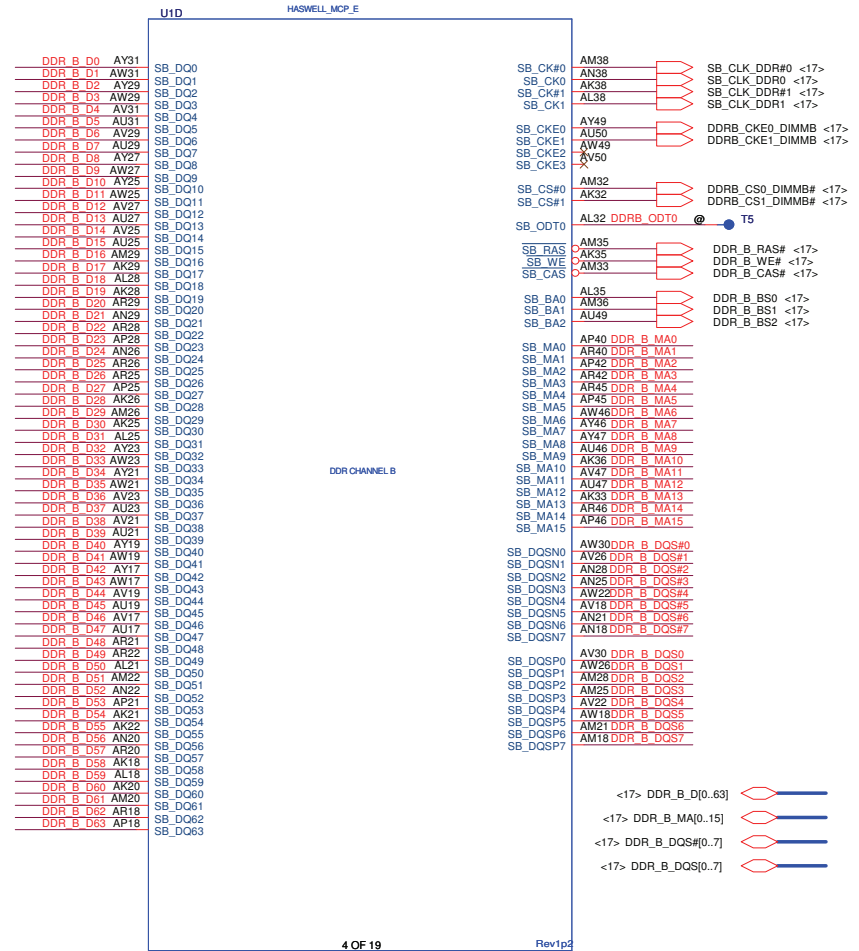
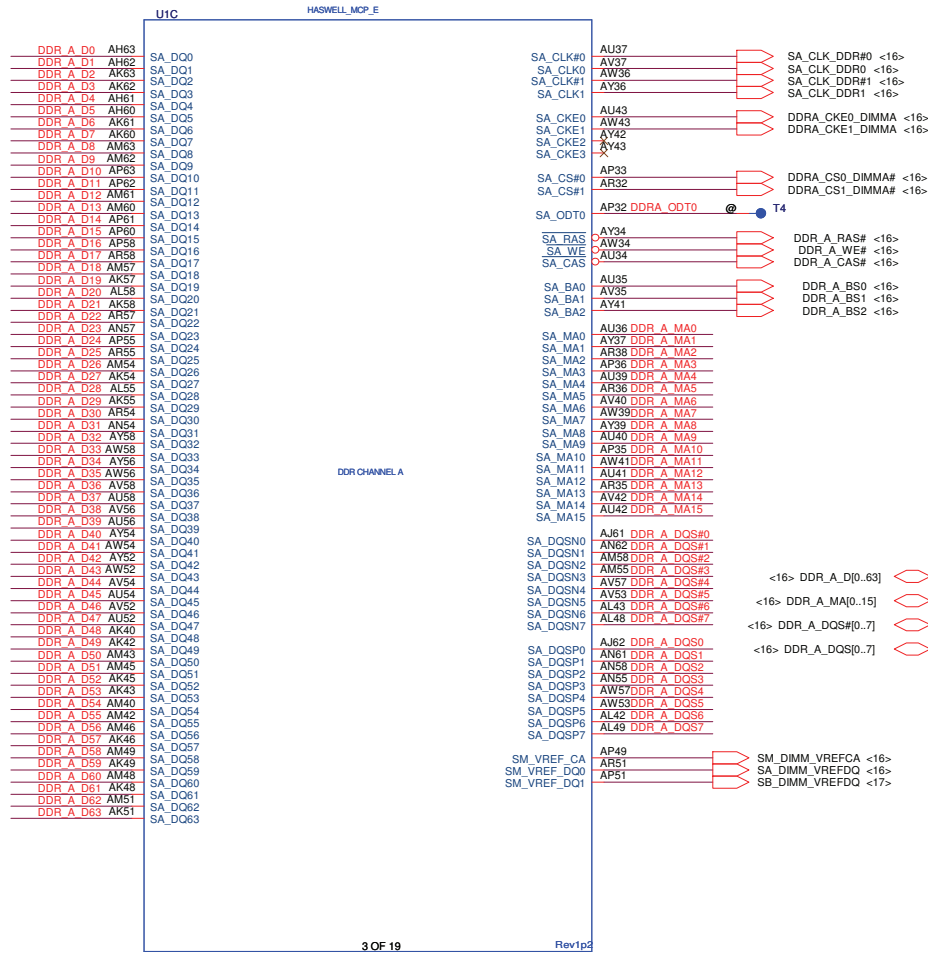
Function						
description						
explain						
BTO						

Function						
description						
explain						
BTO						

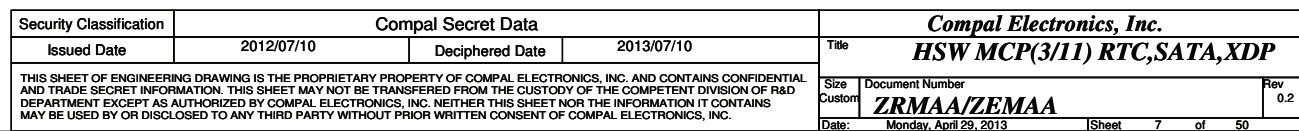
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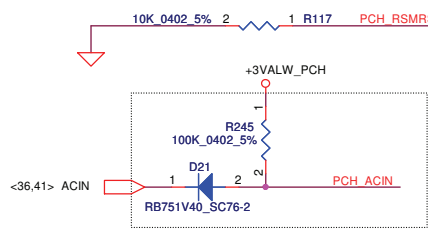
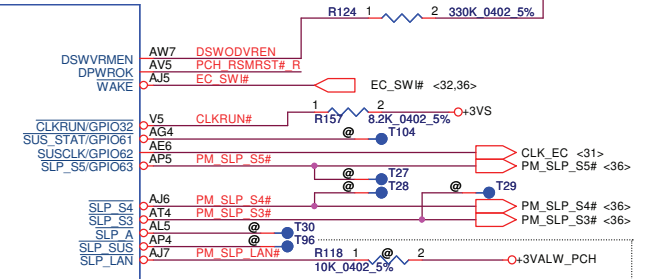
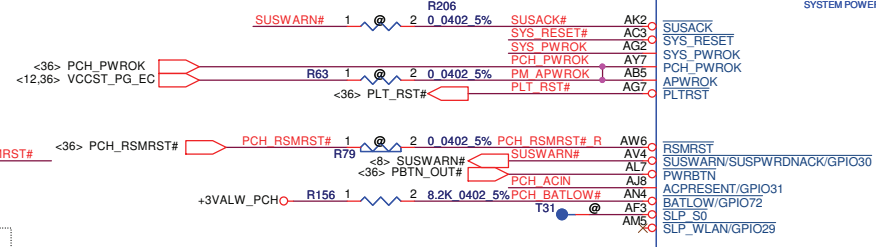
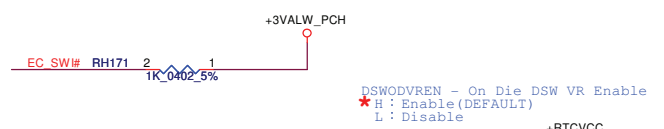
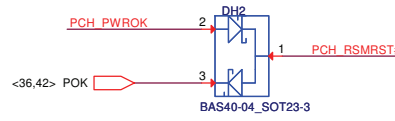
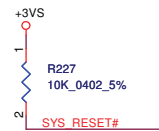
STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title	HSW MCP(2/11) DDRIII
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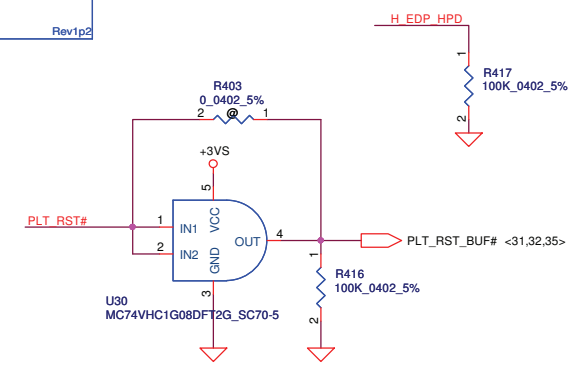
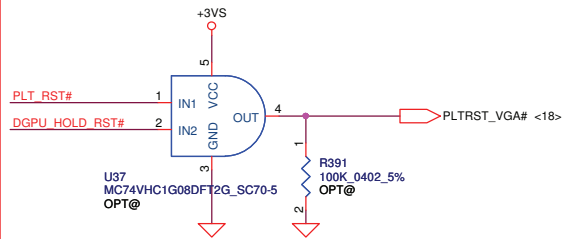
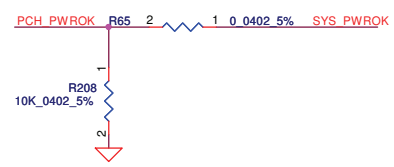
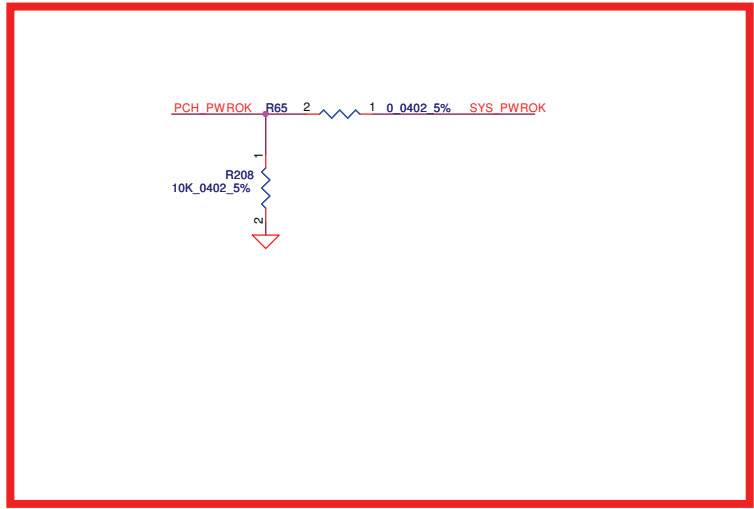
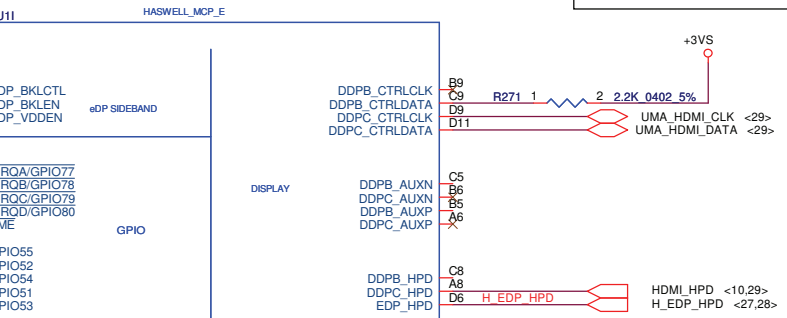
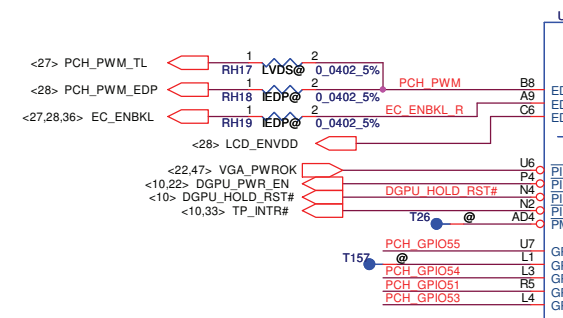




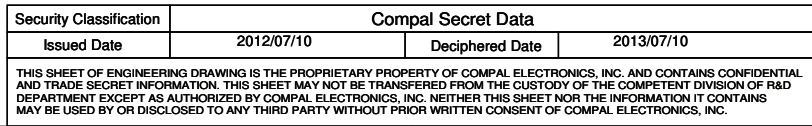
Note for PCH_ACIN: Deep Sx need use EC GPIO for ACPRESENT function

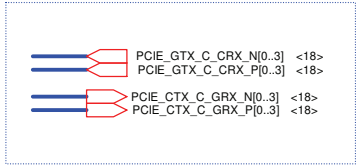
Need to Check

DDPB_CTRLCLK: Port B Detected
DDPC_CTRLCLK: Port C Detected
* 1: Port B or C is detected
0: Port B or C is not detected
(Have internal PD)



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								HSW MCP(5/11) PM,GPIO,DDI	
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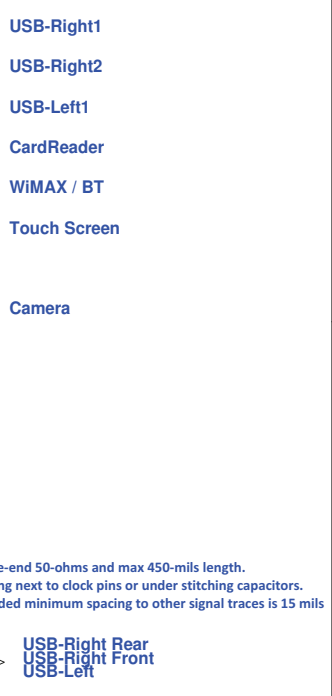
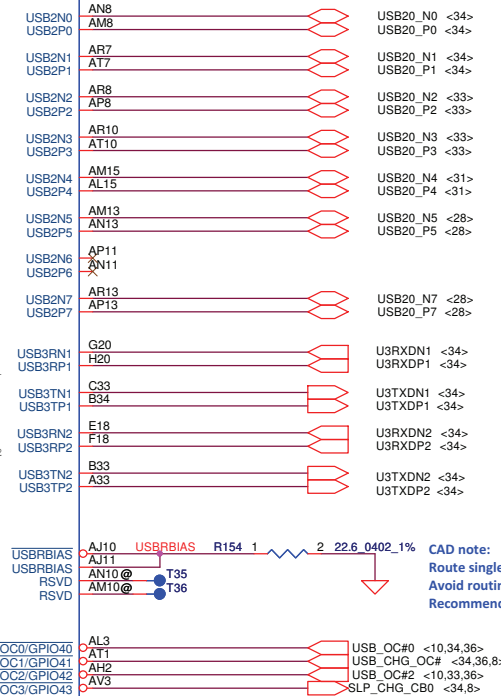
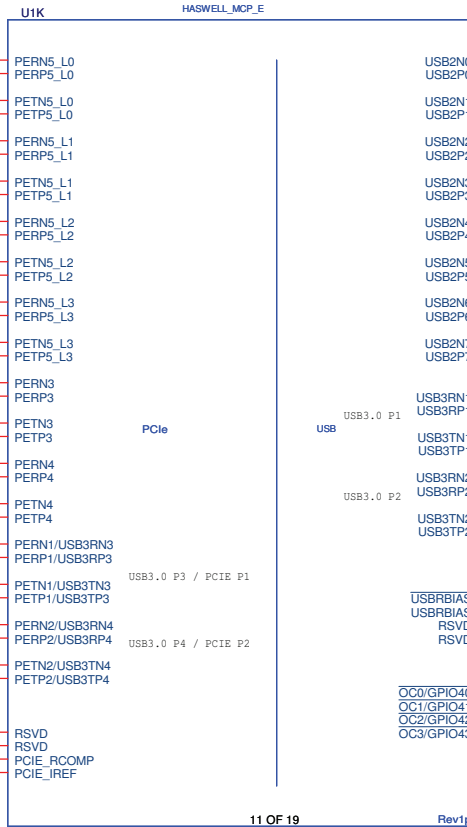
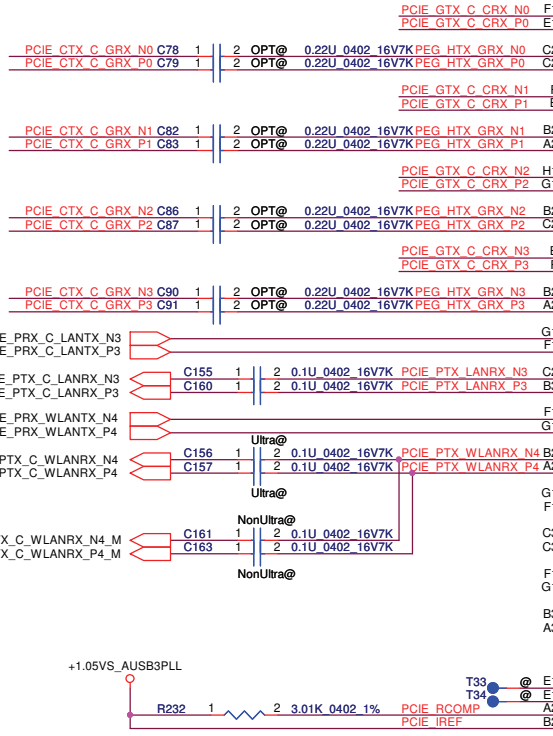




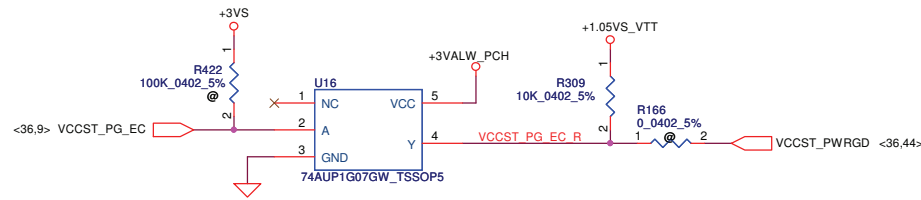
PCIE LAN

WLAN NGFF type

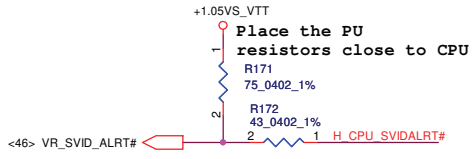
WLAN min PCIE type



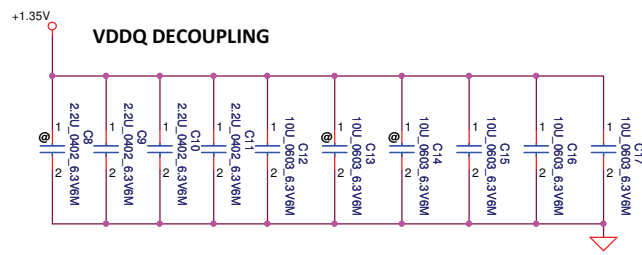
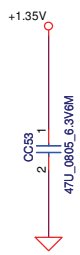
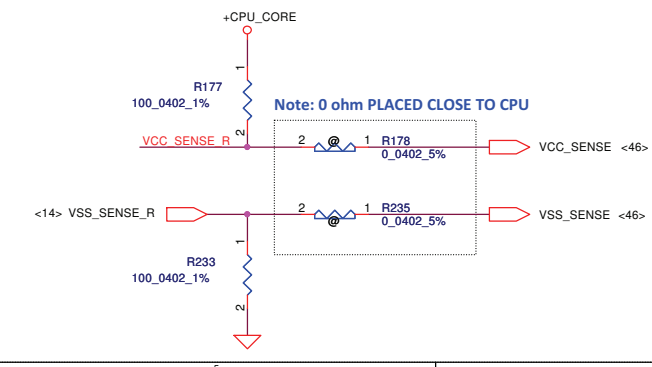
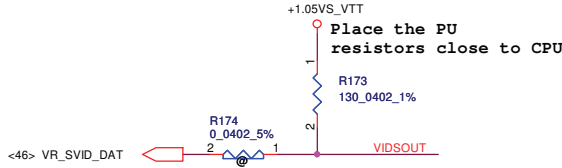
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2013/07/10		Title		HSW MCP(7/11) PCIE,USB	
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SVID ALERT

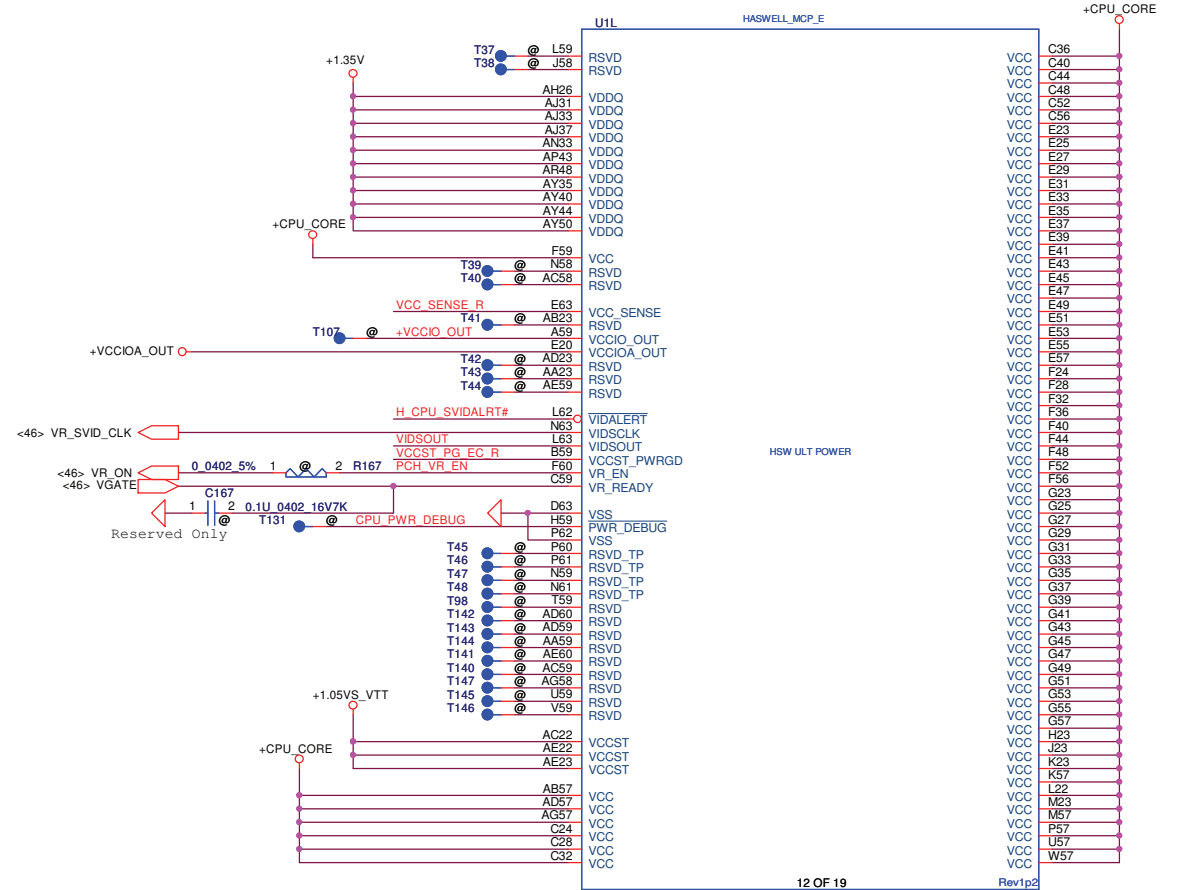


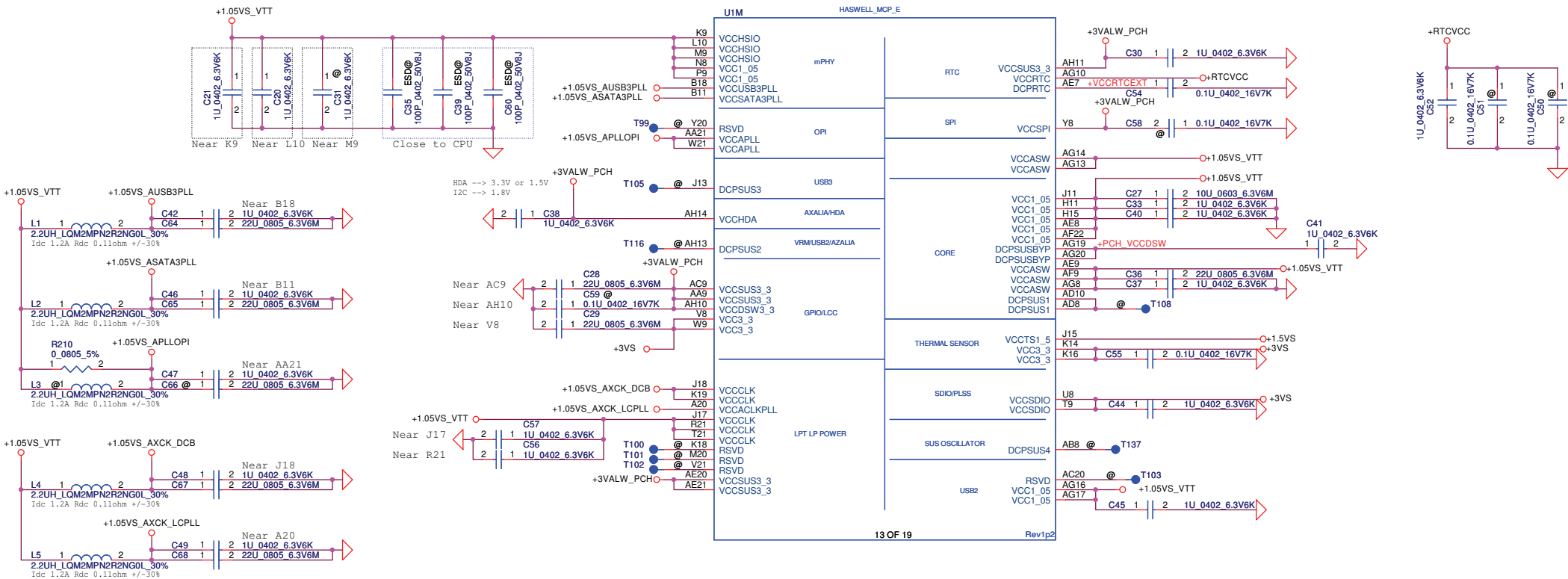
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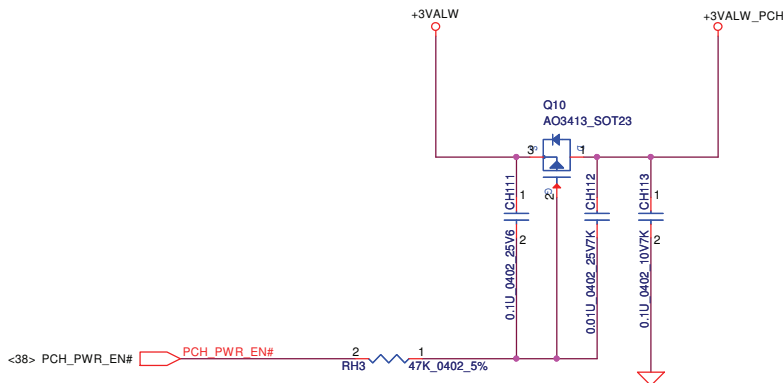
+1.35V : 470UF/2V/7343 *2
 10UF/6.3V/0603 * 6
 2.2UF/6.3V/0402 * 4

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								HWS MCP(8/11) Power					
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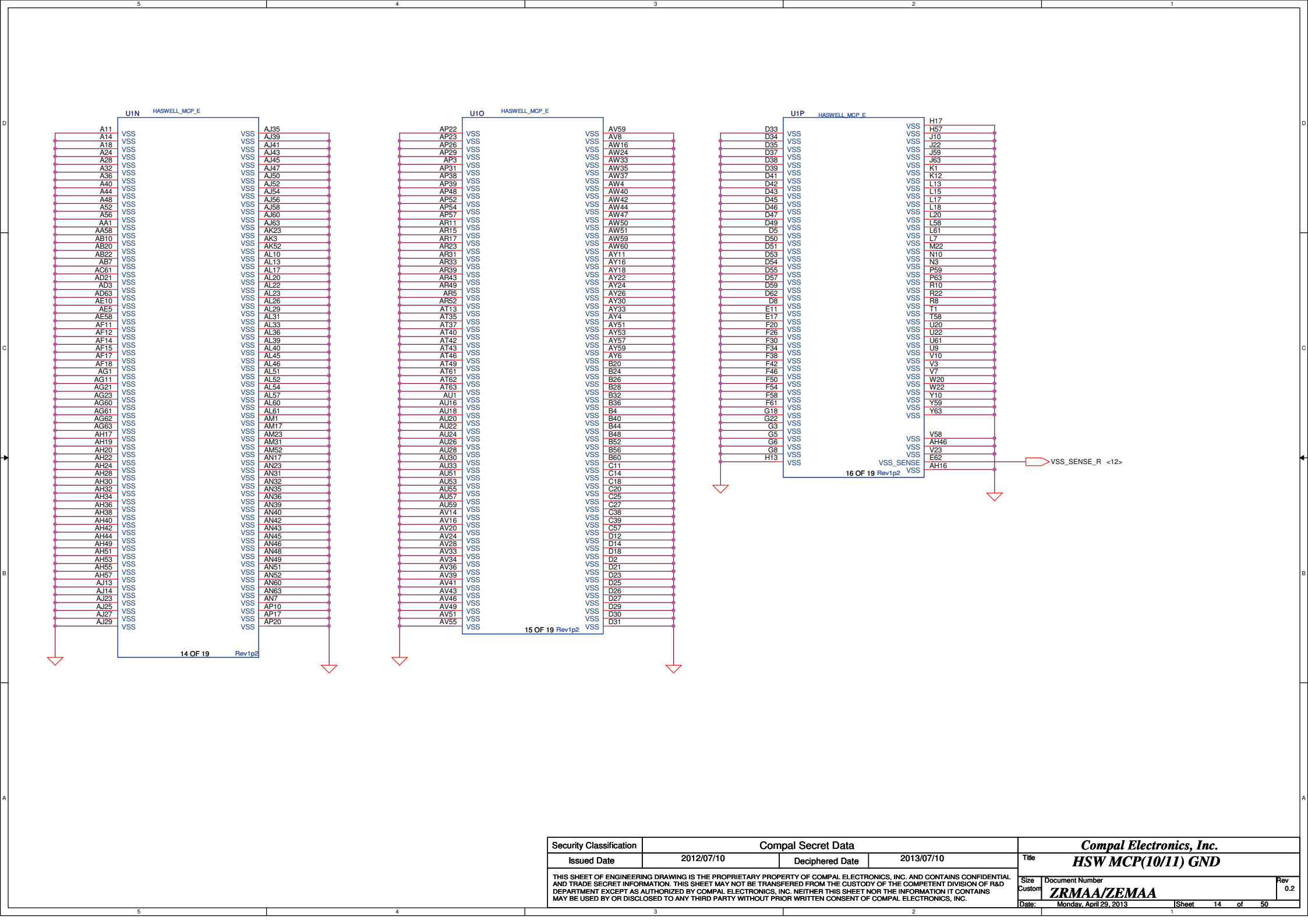


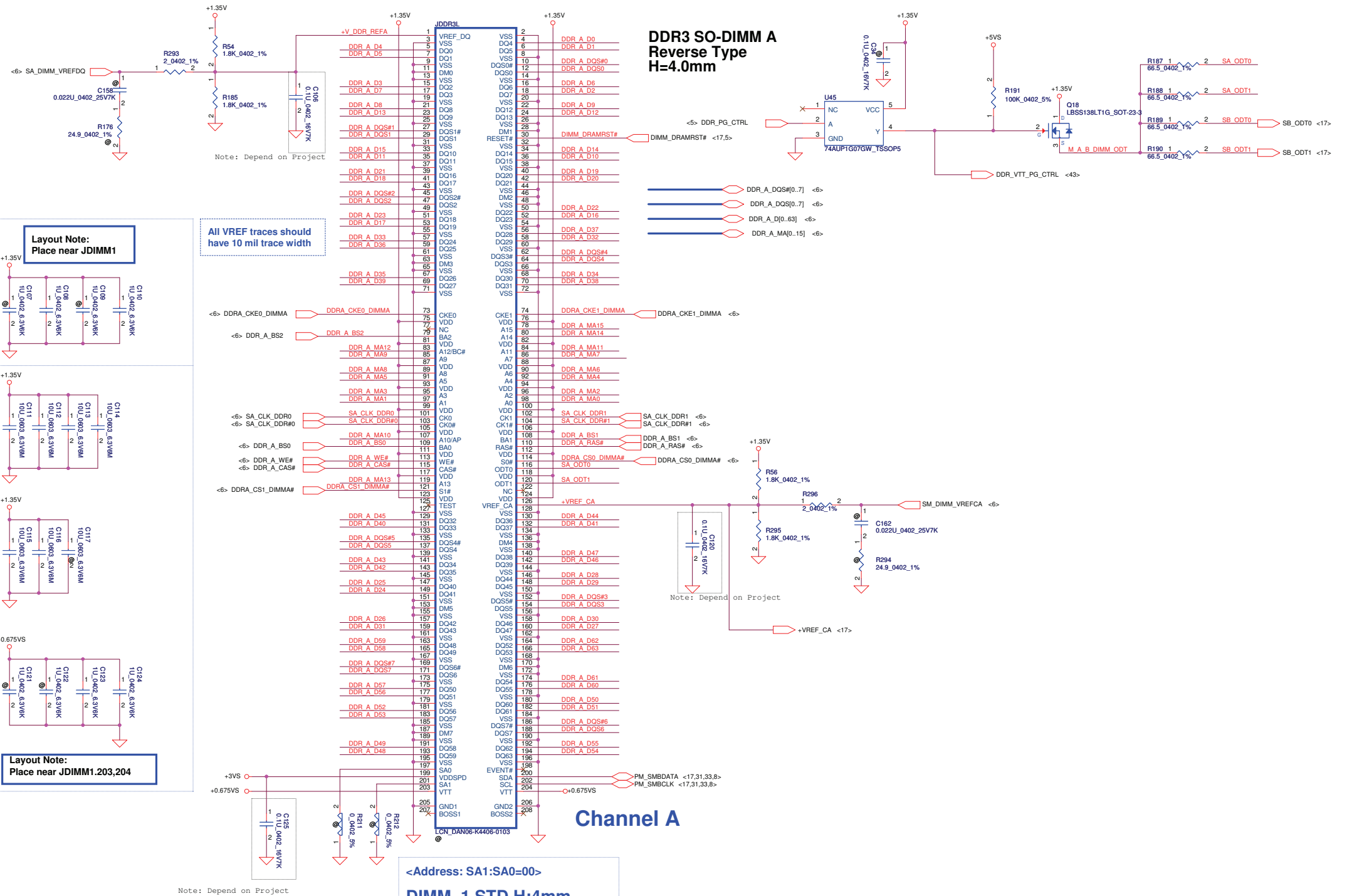
+3VALW to +3VALW_PCH



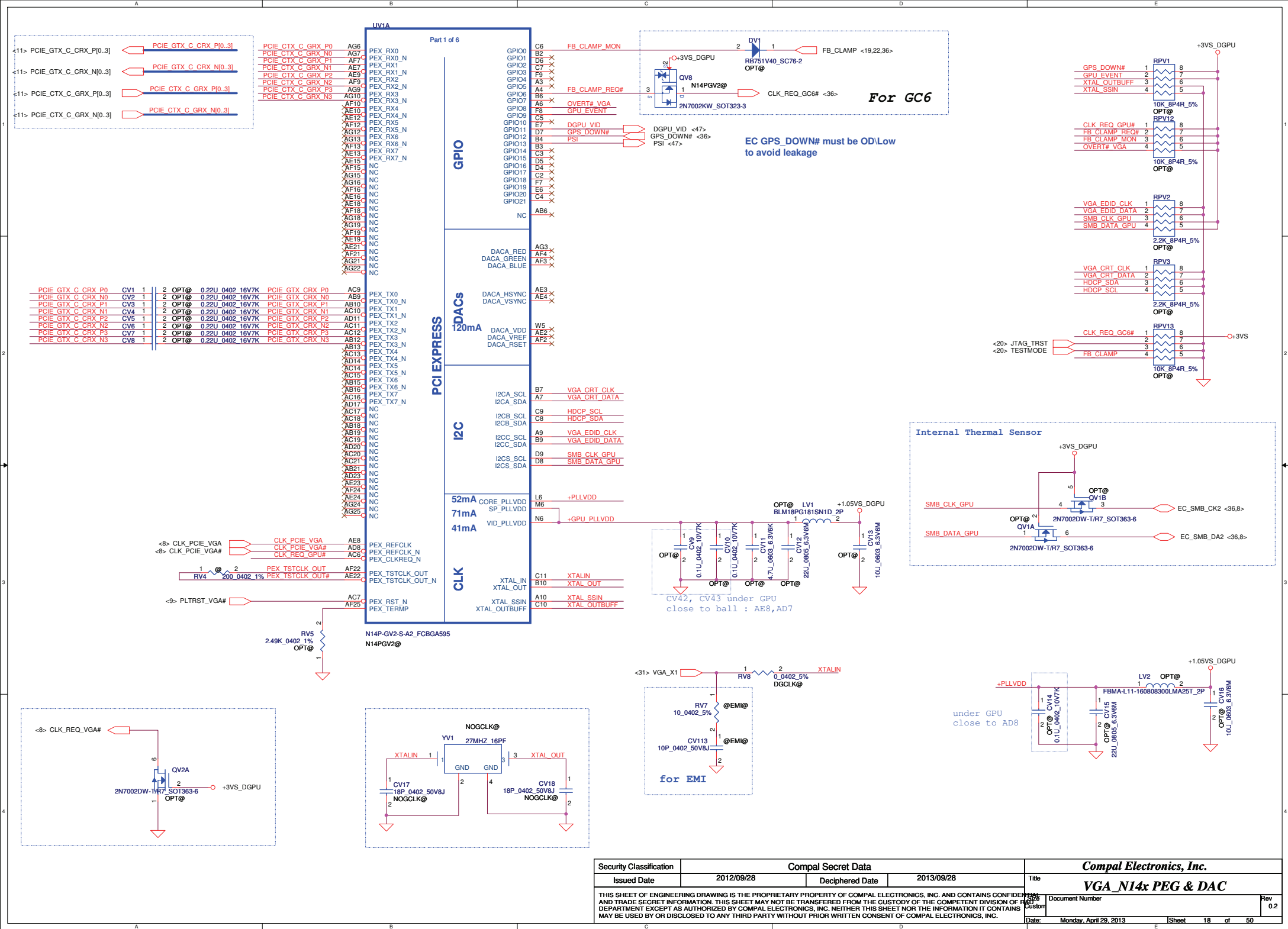
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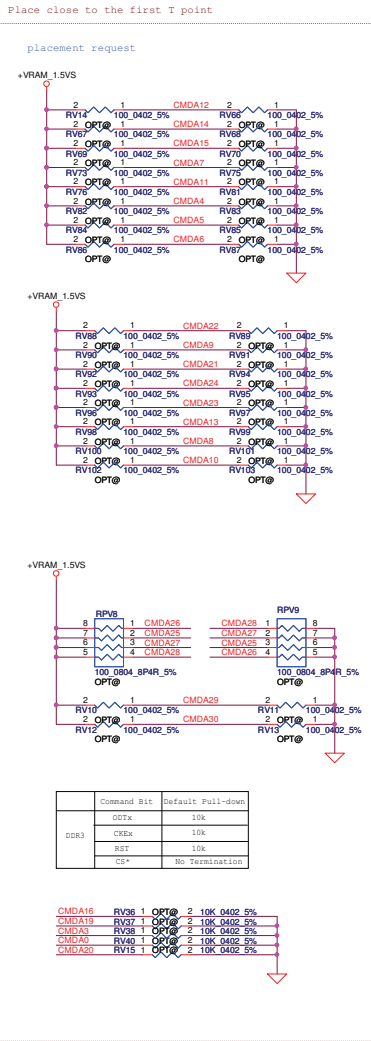
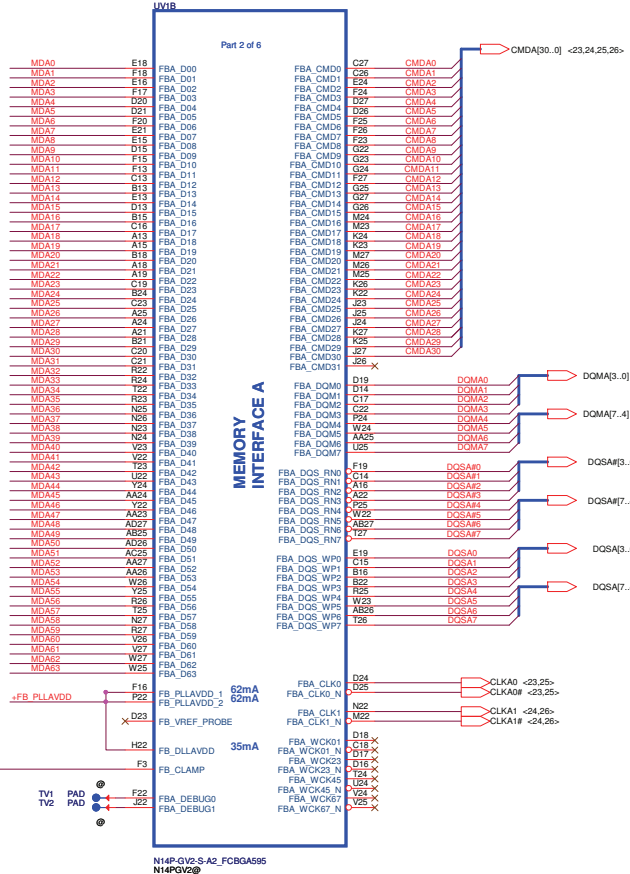
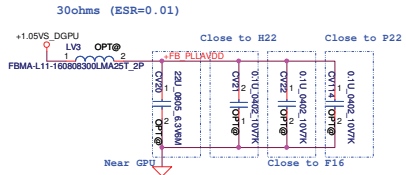




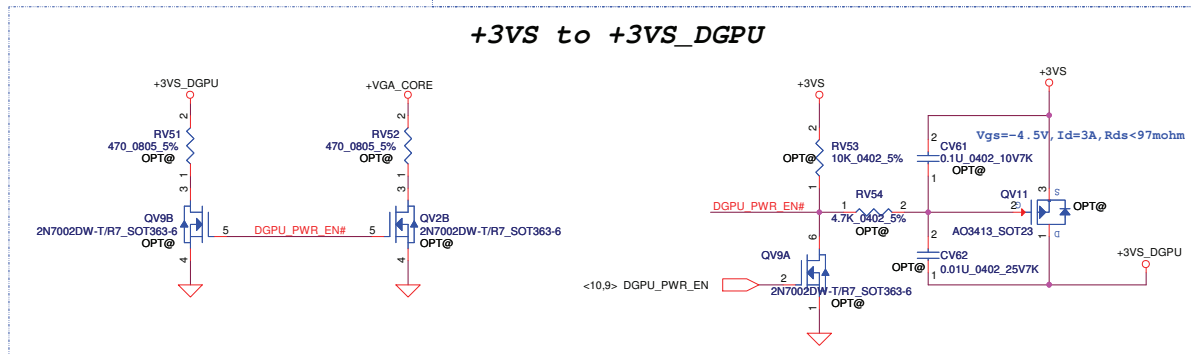
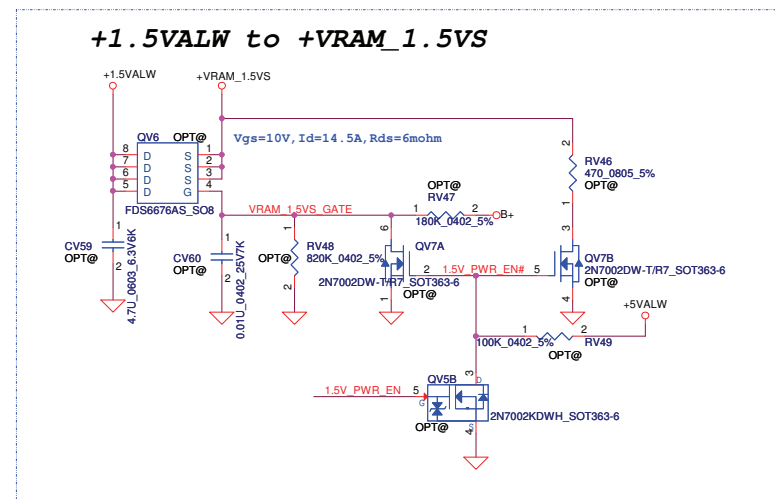
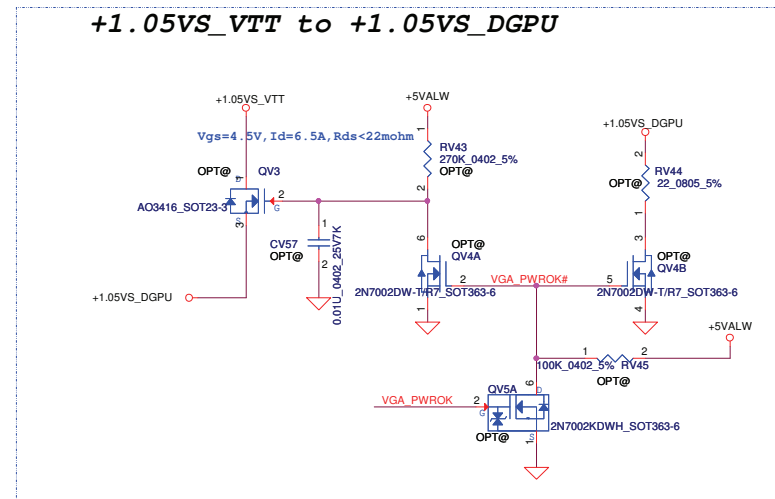
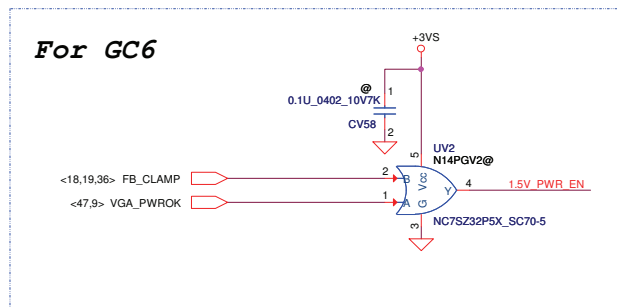
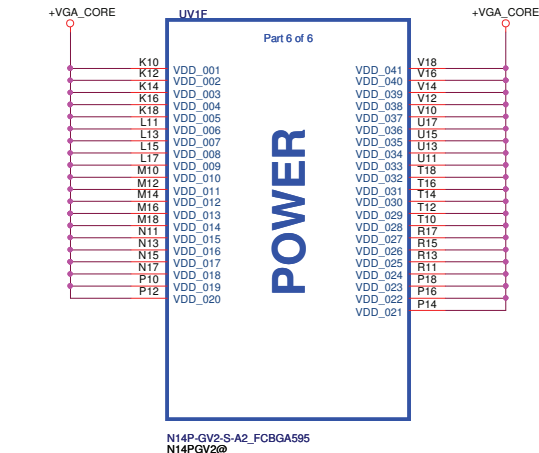
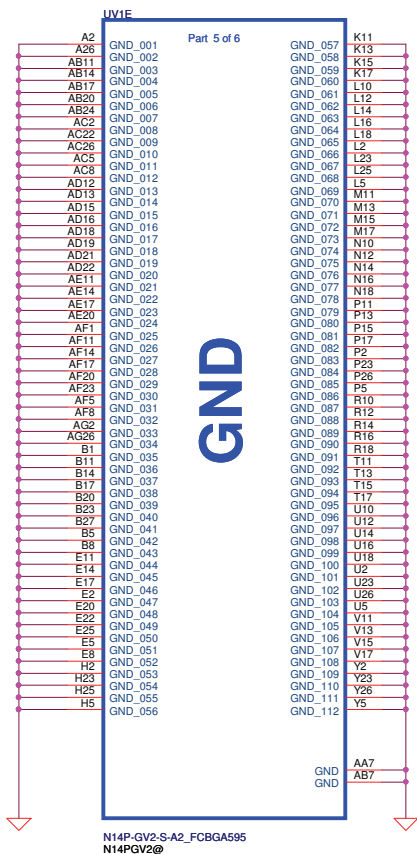
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VRAM Interface

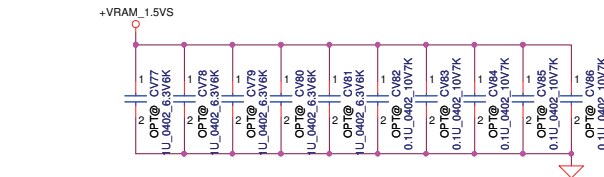
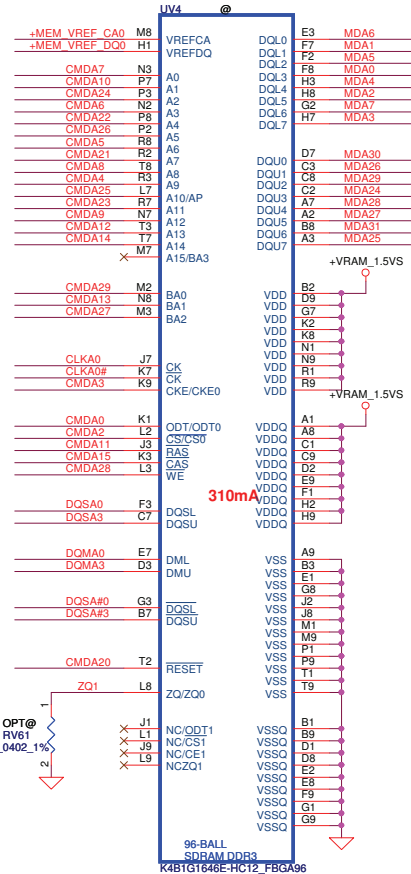
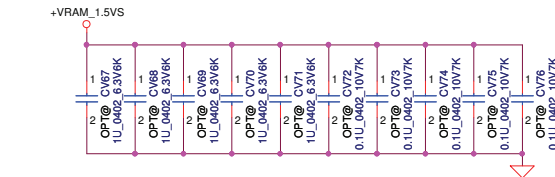
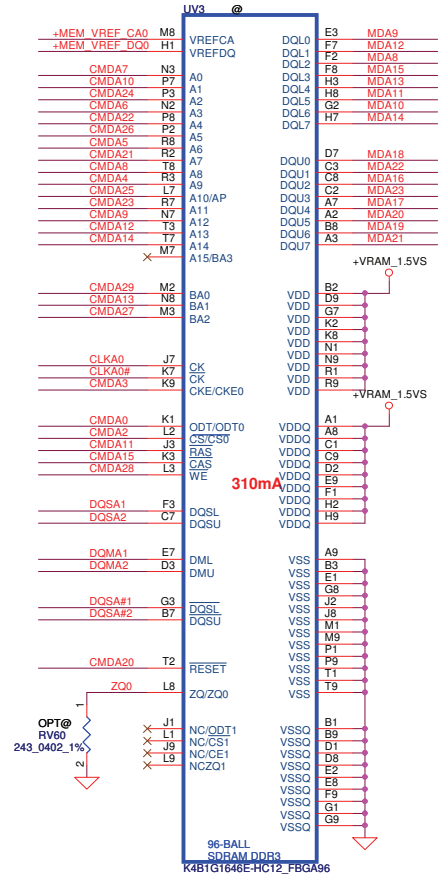
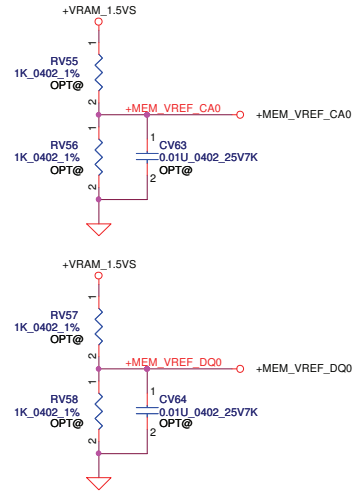
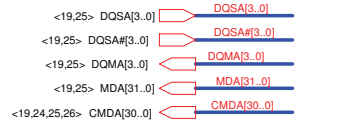


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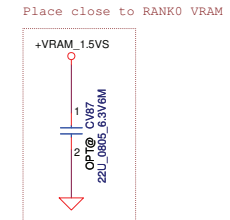
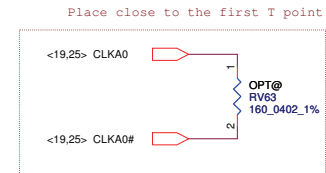


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RANK 0 [31...0] VRAM DDR3 Chips

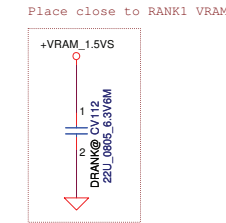
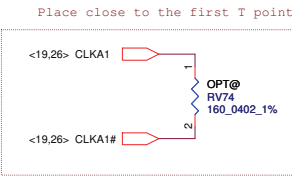
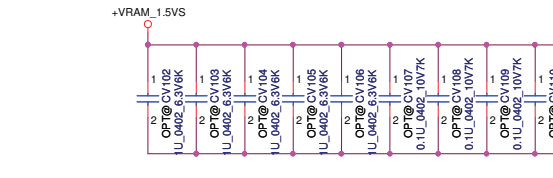
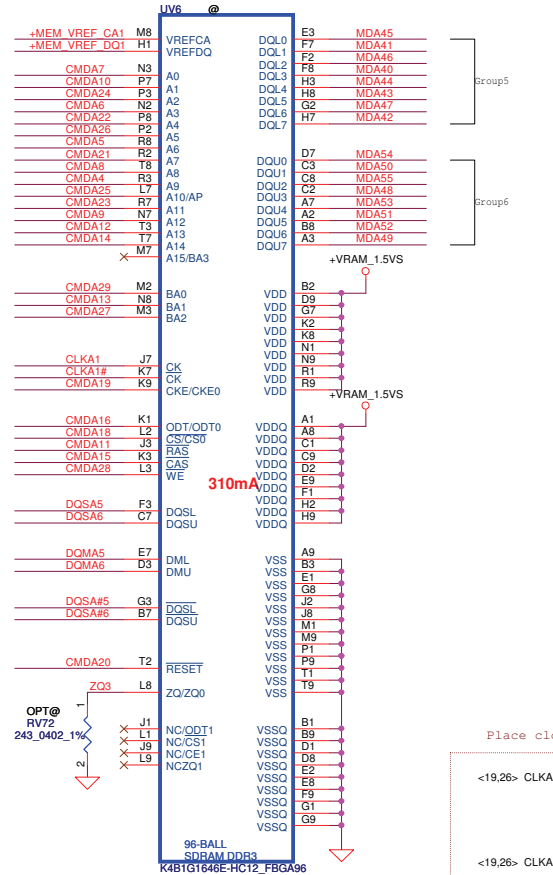
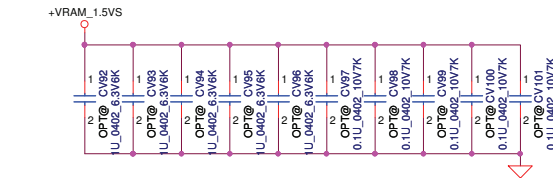
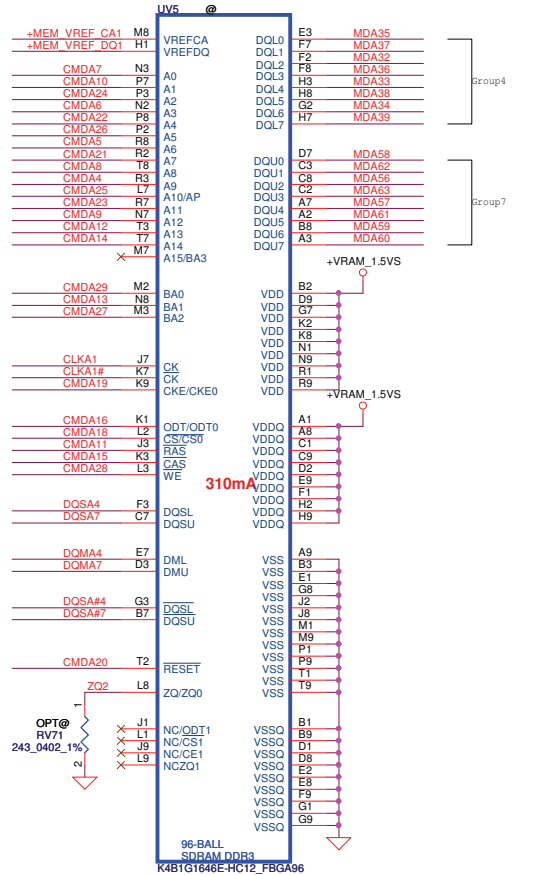
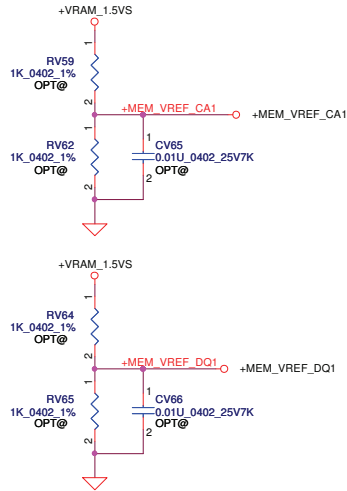


Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2



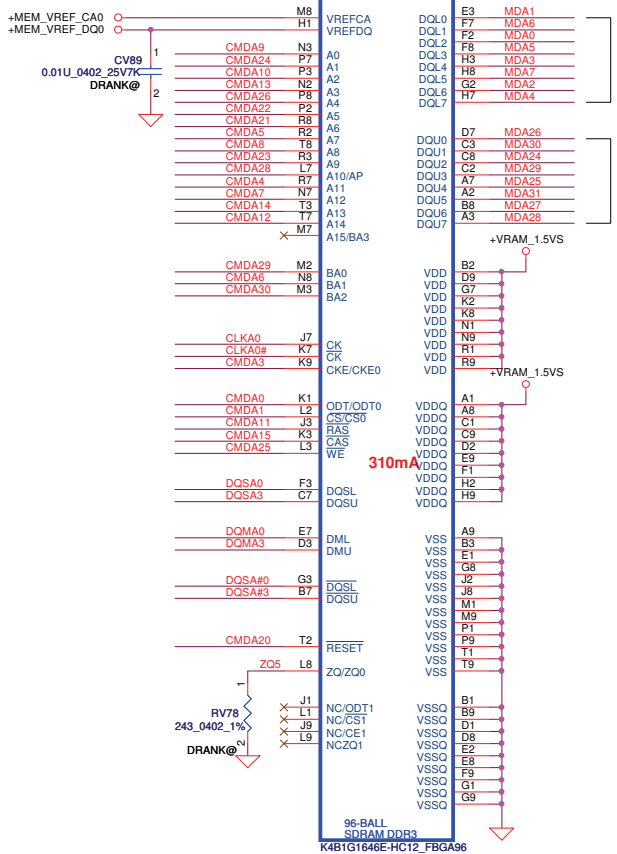
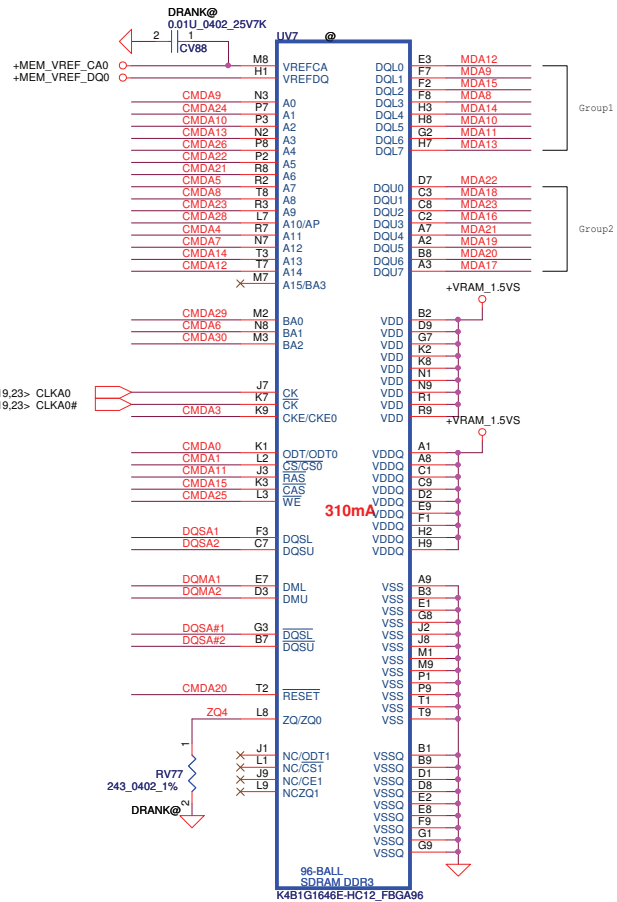
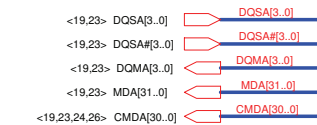
RANK 0 [63...32] VRAM DDR3 Chips

<19,26> DQSA[7..4]  DQSA[7..4]
<19,26> DQSA# [7..4]  DQSA# [7..4]
<19,26> DQMA[7..4]  DQMA[7..4]
<19,26> MDA[63..32]  MDA[63..32]
<19,23,25,26> CMDA[30..0]  CMDA[30..0]



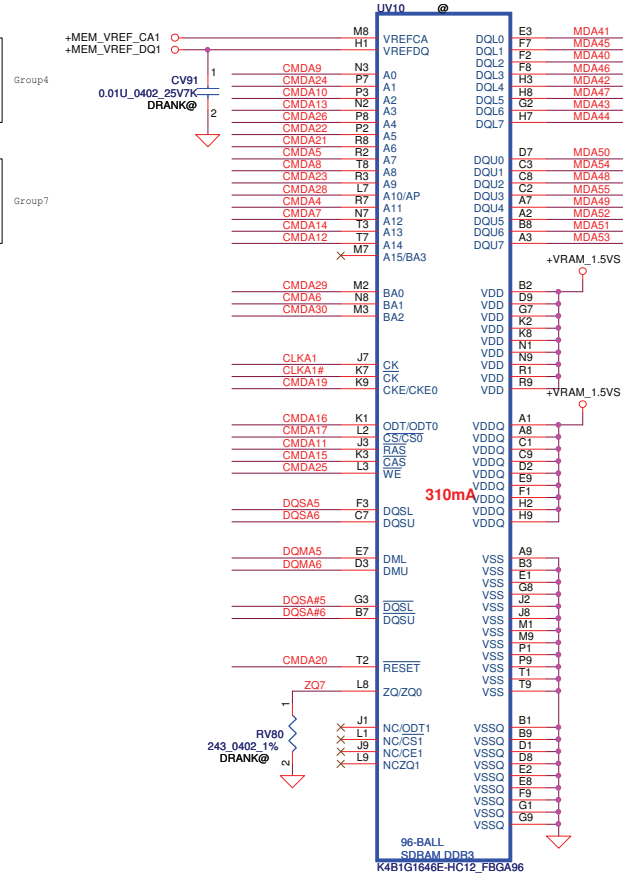
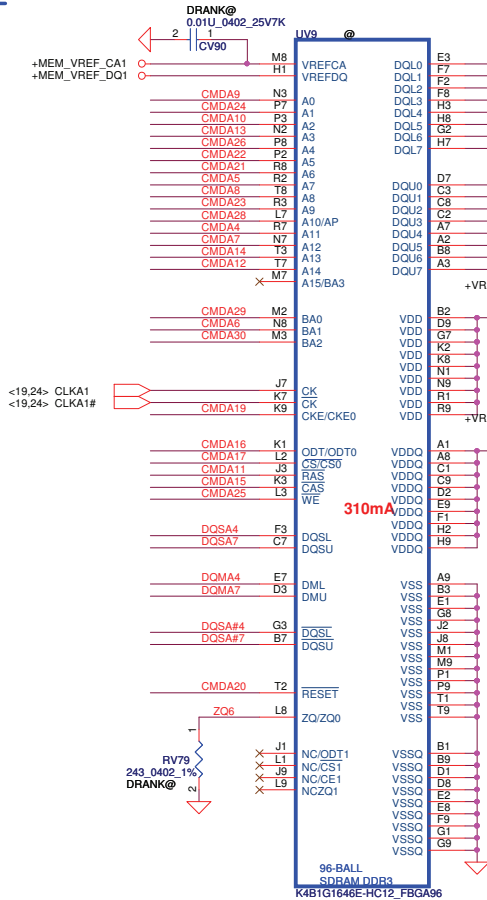
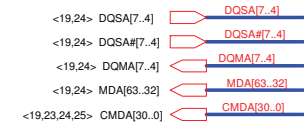
Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17			CS1#	
CMD18		CS0#		
CMD19		CKE	CKE	
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

RANK 1 [31...0]
VRAM DDR3 Chips



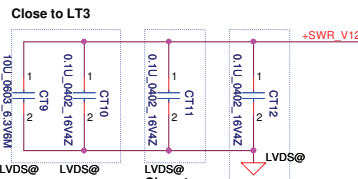
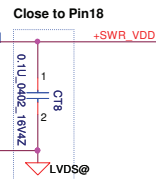
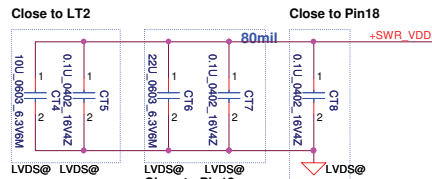
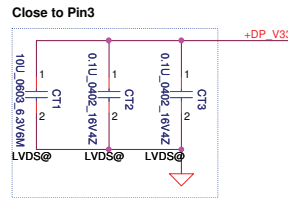
Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17			CS1#	
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

RANK 1 [63...32]



Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

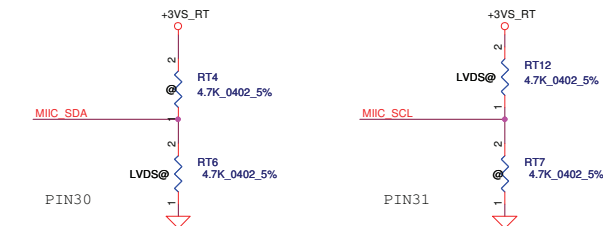
Security Classification		Compal Secret Data		Compal Electronics, Inc. VGA N14x VRAM RANK 1H	
Issued Date	2012/09/28	Deciphered Date	2013/09/28	Title	
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				Custom	
Date: Monday, April 29, 2013		Sheet 26 of 50			



Mode Configure

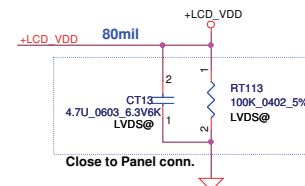
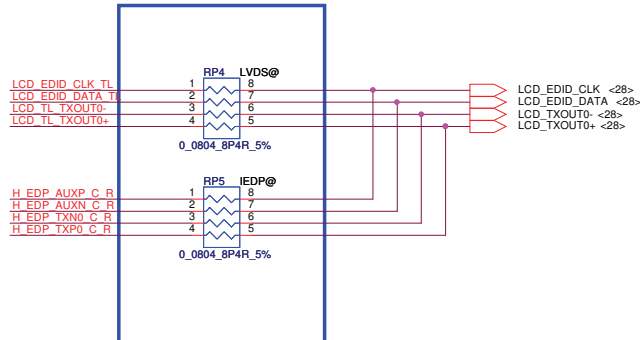
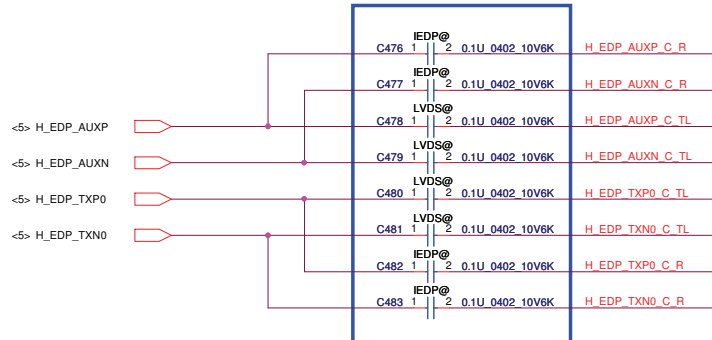
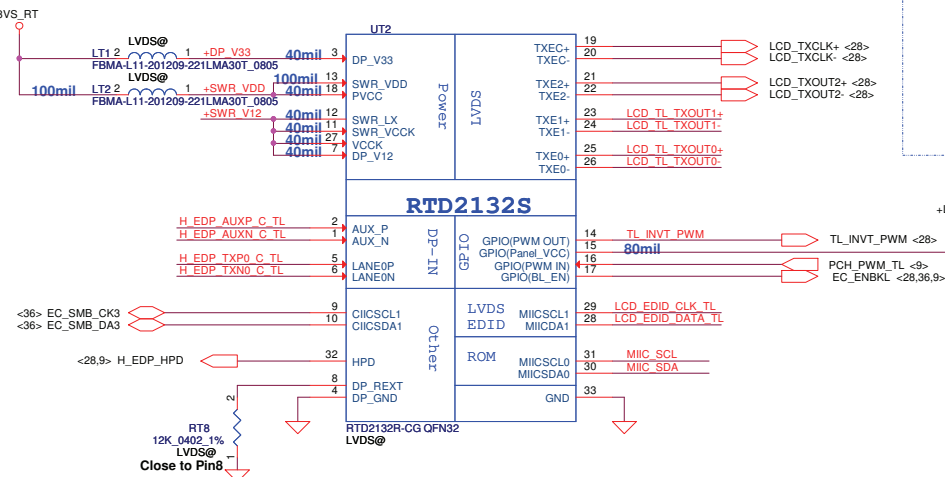
※ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.
EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.
EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.

< ※Default mode >

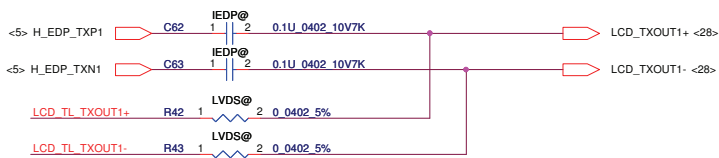


SWR / LDO Mode select

※LDO mode is adopted as default power regulator mode.
Also can implement SWR mode by add inductor.



Place co-layer Resistor back to back on TOP and BOT



	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5~3.3V

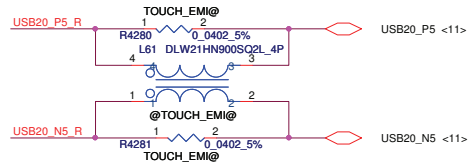
* Version R has internal level shifter, remove level shifter circuit on AMD platform

Different between 2132S and 2132R

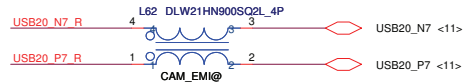
2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

Security Classification	Compal Secret Data	Compal Electronics, Inc.
Issued Date	2011/06/30	Deciphered Date
2013/06/30		
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BTO : TOUCH_EMI@

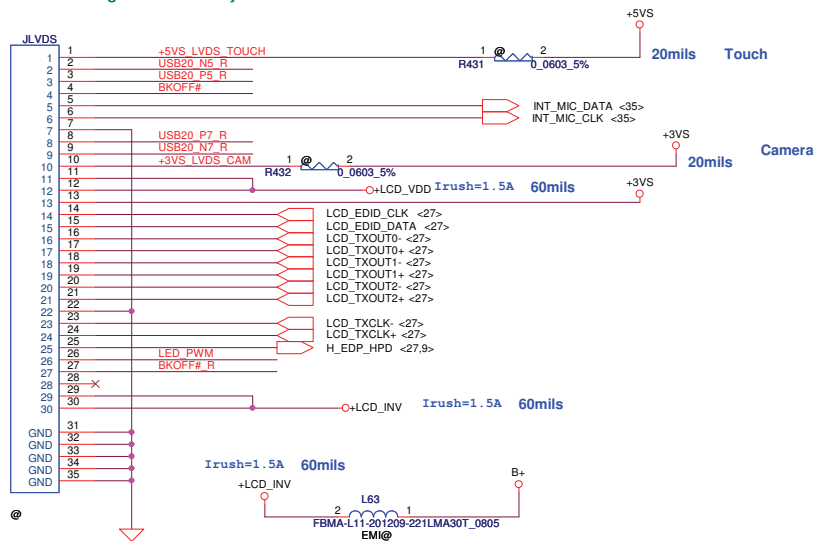


EMI request - Close to JEDP connector

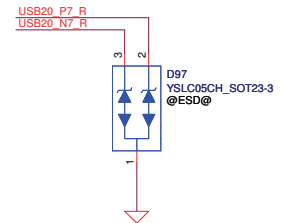
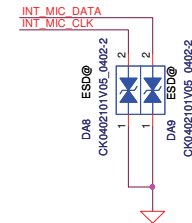
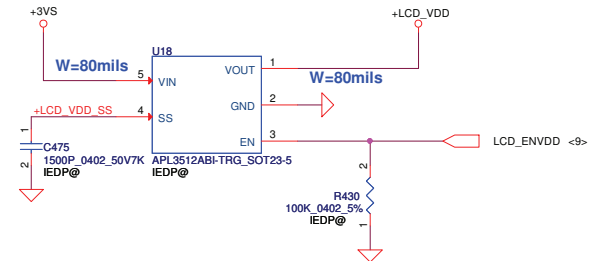


LVDS colay eDP cable

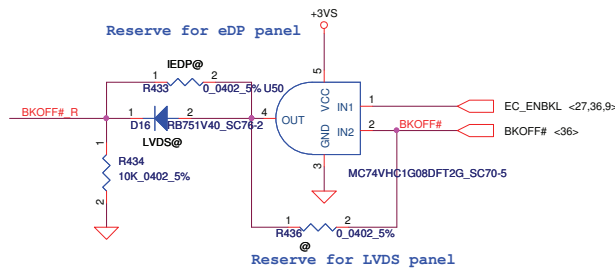
Pin define will be change after ME ready



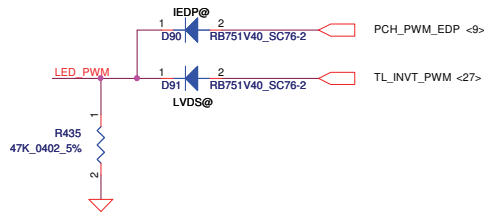
LCD POWER CIRCUIT (For EDP panel only)



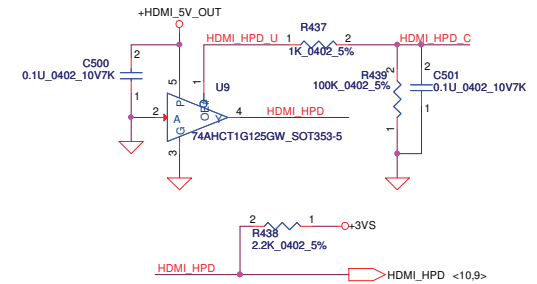
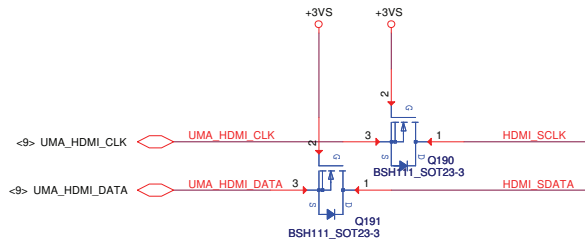
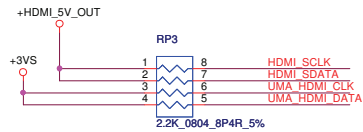
Reserve for eDP panel



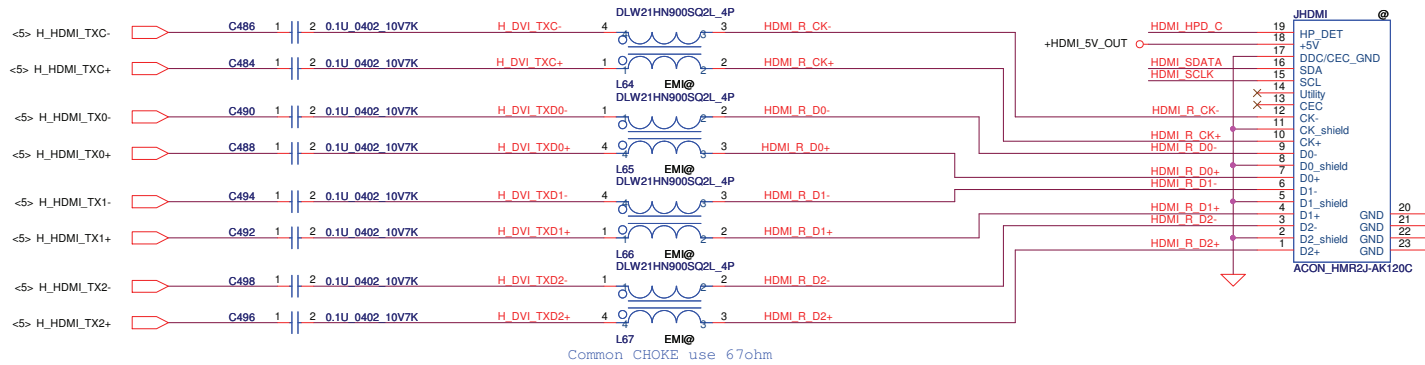
Reserve for LVDS panel



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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title			
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				Revision			
				Document Number			
				Custom			
				ZRMAA/ZEMAA			
				Rev 0.2			
				Date: Monday, April 29, 2013			
				Sheet 28 of 50			



HDMI Connector



HDMI Royalty

ZZZ1 HDM45@

RO0000003HM

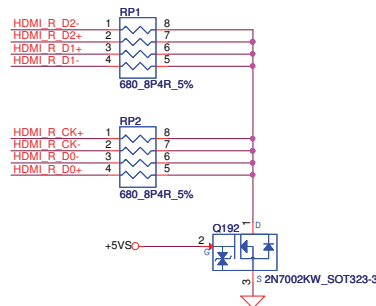
HDMI W/Logo + HDCP

HDMI W/O Logo: RO0000001HM

HDMI W/Logo: RO0000002HM

HDMI W/Logo + HDCP: RO0000003HM

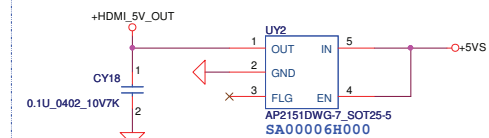
please manually load
this virtual material to 45@ BOM



HDMI POWER CIRCUIT

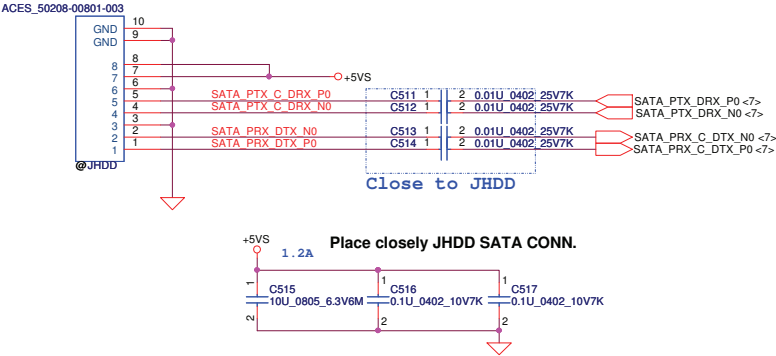
VIN = 5V, IOU = 0.5A, RDS(ON) TYP=95m ; MAX=115m

Current Limit: TYP=0.8A ; MAX=1A

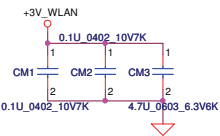


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2012/04/19				Title			
Deciphered Date				2015/04/19				HDMI Conn.			
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Document Number				ZRMMA/ZEMAA				Rev			
29				0.2				Sheet			

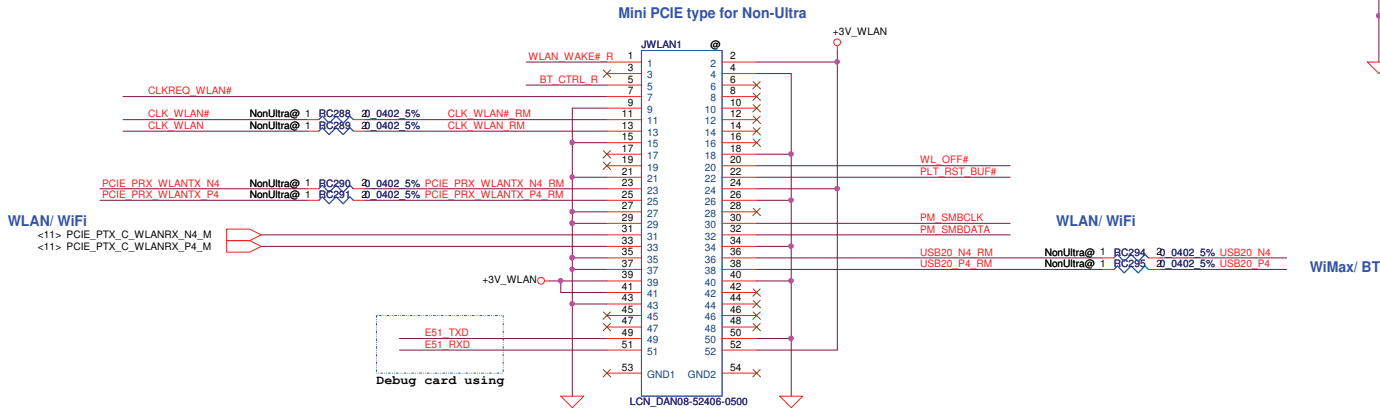
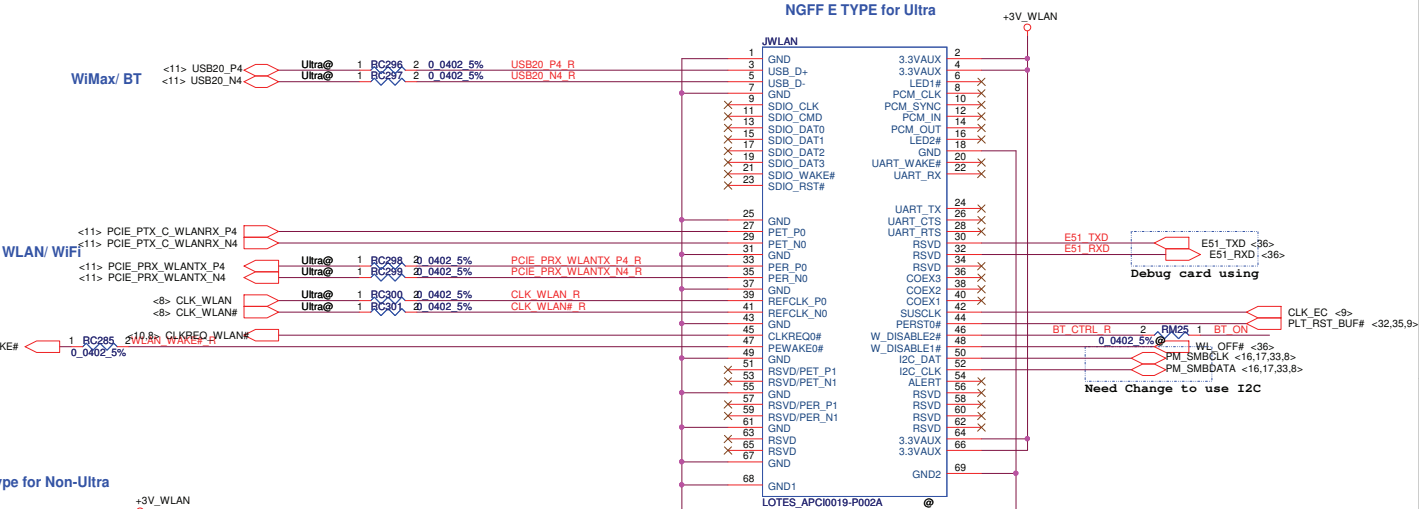
SATA HDD Conn.



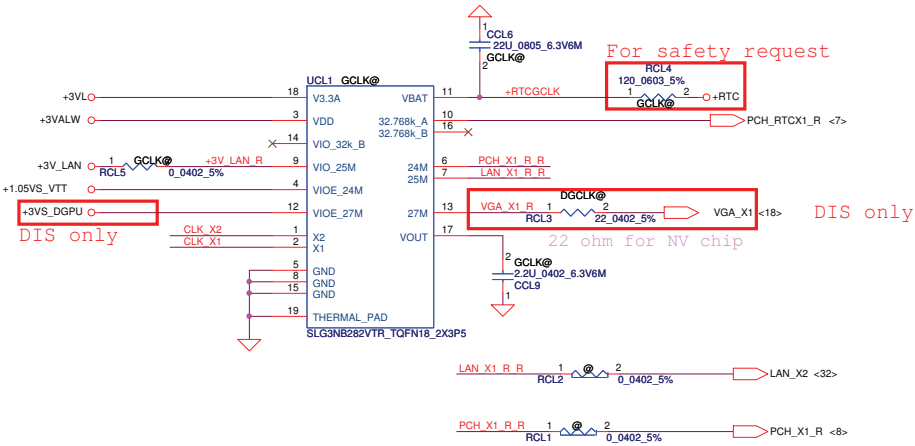
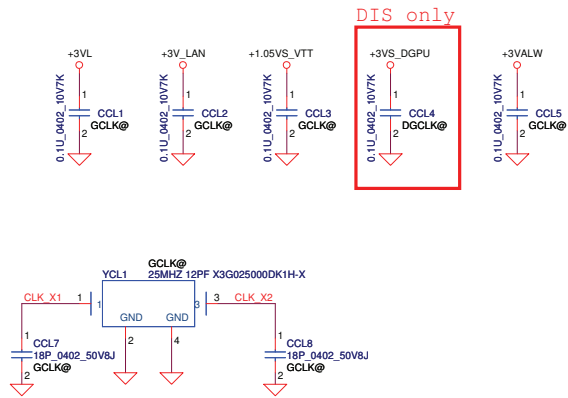
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	HDD/Gsensor
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				Date: Monday, April 29, 2013	Sheet 30 of 50

Slot 1 Half PCIe Mini Card-WLAN

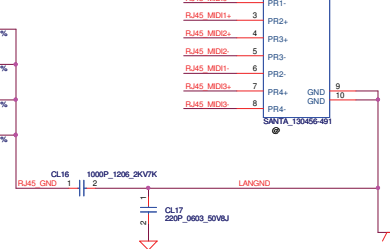
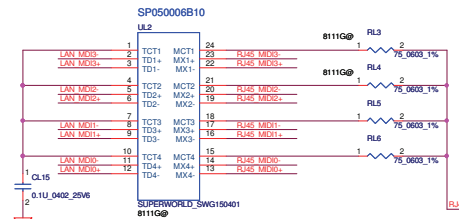
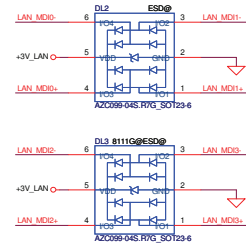
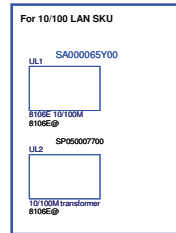
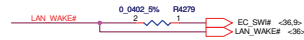
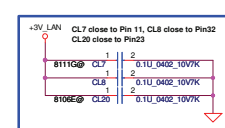
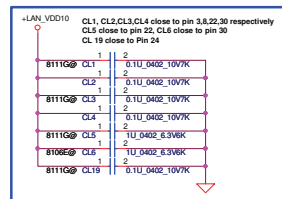
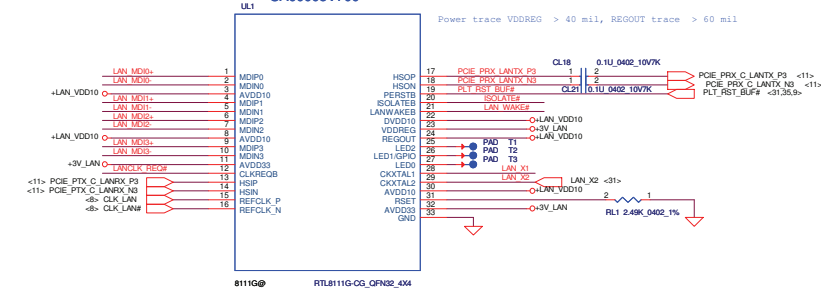
WLAN&BT Combo module circuits		
	BT on module Enable	BT on module Disable
BT_ON	H	L



Green Clock



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				Size	Document Number	ZRM001/ZEMAA			Rev 0.2
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For LAN function

The schematic diagram illustrates the hardware connections for the LAN function. It features two main signal paths:

- LAN_EN Signal Path:** A red line labeled "LAN_EN" originates from a pin labeled "10.B LAN_EN". It passes through a 10kΩ pull-up resistor to a +3V5 supply and is connected to the "ISOLATE#" pin of the PL453. The "ISOLATE#" pin is also connected to a 1kΩ pull-down resistor to ground. The output of the "ISOLATE#" pin is labeled "WOL_EN# <36>".
- LANCLK_REQ Signal Path:** A red line labeled "LANCLK_REQ" originates from a pin labeled "C.B CLKREQ_LAN#". It is connected to the "CLKREQ#" pin of the PL453. The "CLKREQ#" pin is also connected to a 1kΩ pull-down resistor to ground. The output of the "CLKREQ#" pin is labeled "LANCLK_REQ#".

The PL453 component is identified as a 2N7000WV_SOT23-3.

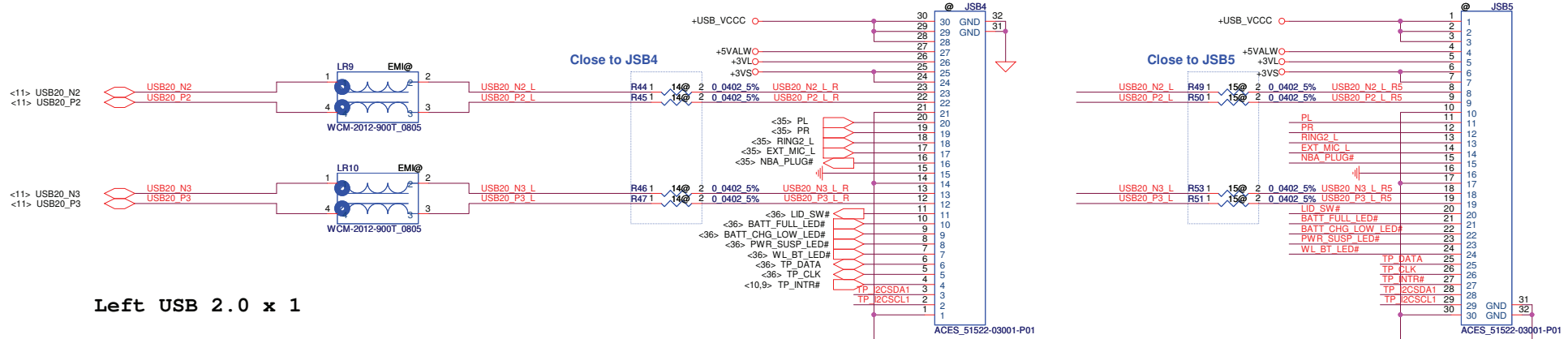
	Sx Enable Wake up	Sx Disable Wake up
WOL_EN#	LOW	HIGH

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

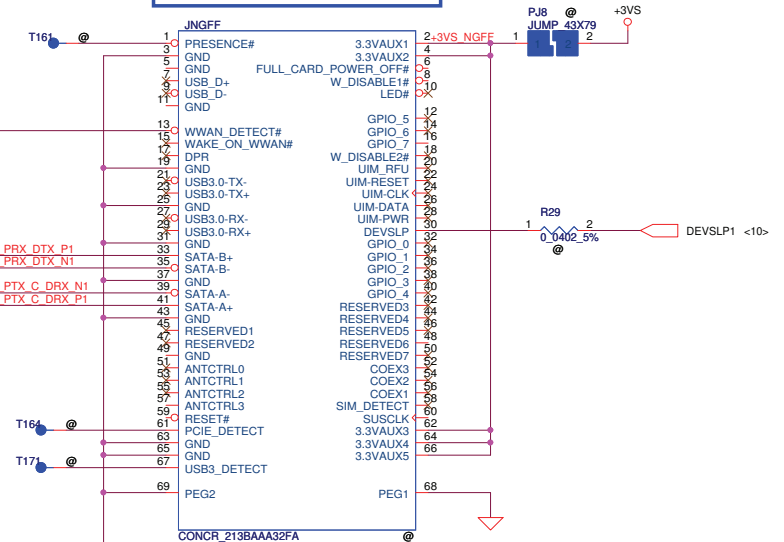
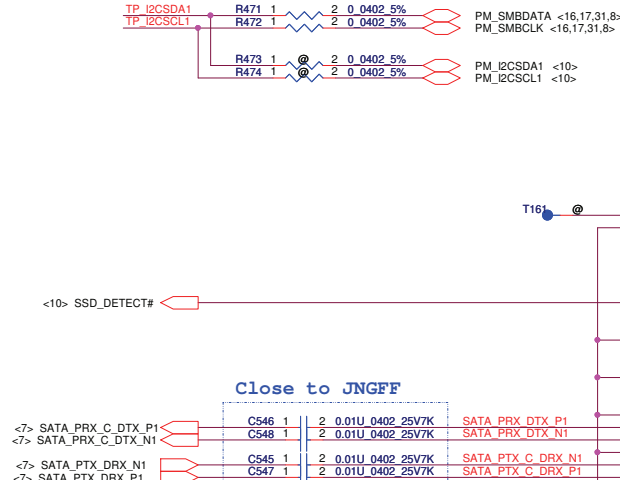
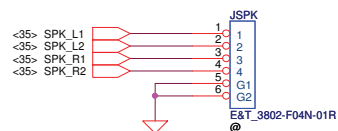
*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

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Small board Conn



SPK Conn.



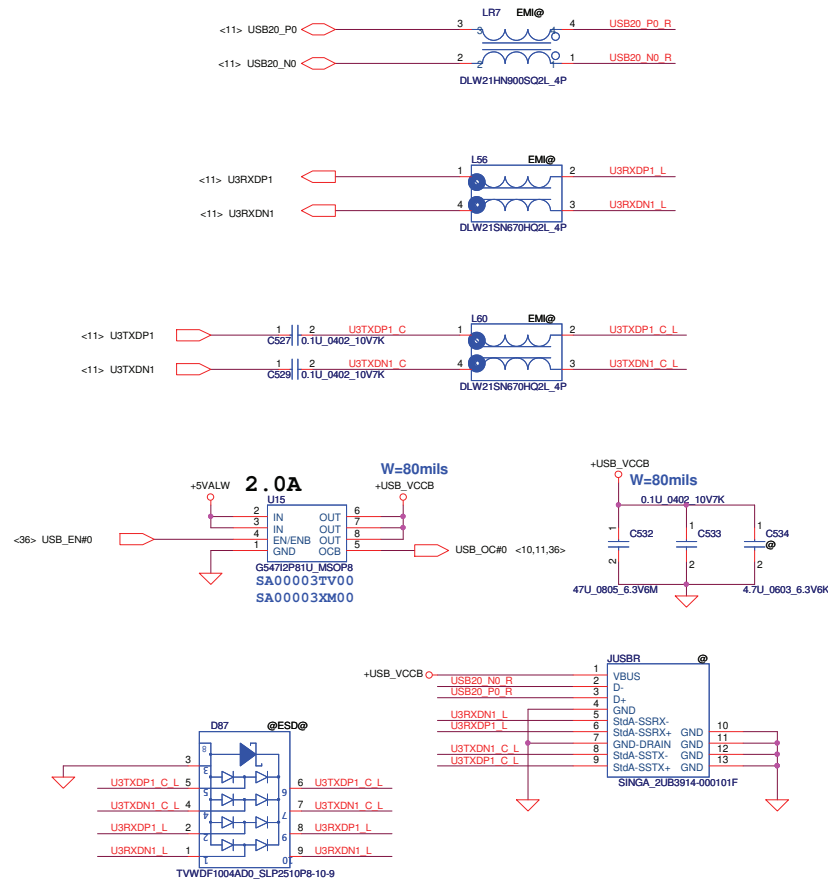
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Size Custom	Document Number	ZRMMA/ZEMAA		Rev 0.2
Date:	Monday, April 29, 2013	Sheet	33	of 50

USB Sleep & Charge

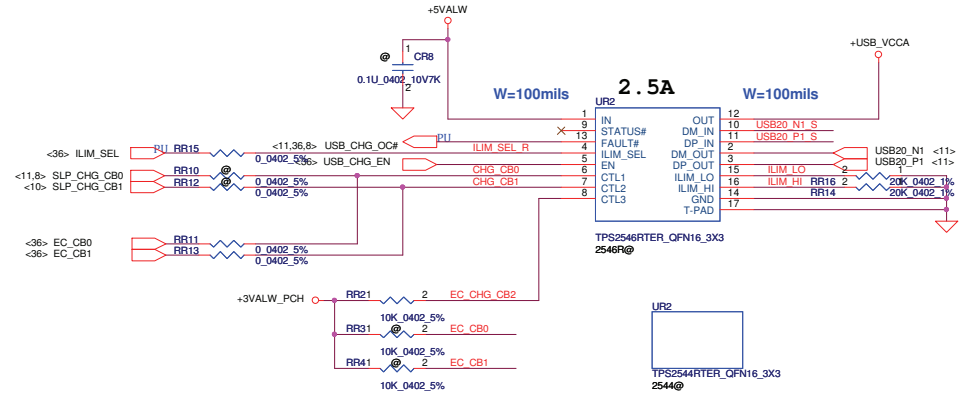
State table for TPS2546RTER

CB0	CB1	CB2	ILIM_SEL	Mode	STATUS
0	1	1	1	Auto	Auto-detection charger mode for Apple devices(2A,1A). Resistor dividers are connected to DP/DM. Including DCP
1	0	1	1	Alternate	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	1	1	0	SDP	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	1	1	CDP	USB pass-through mode with CDP emulation. DP/DM are connected to TDP/TDM

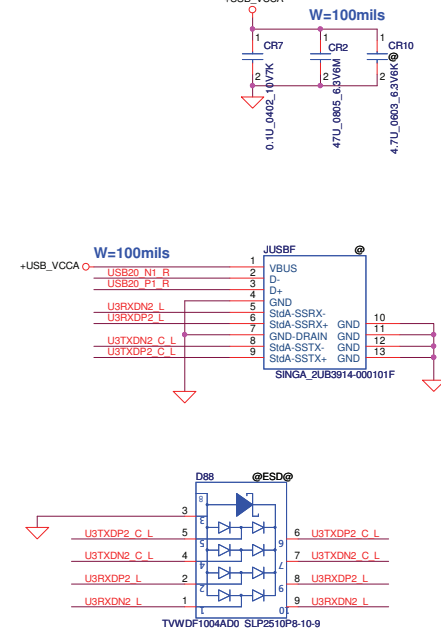
Right rear USB3.0 Conn.

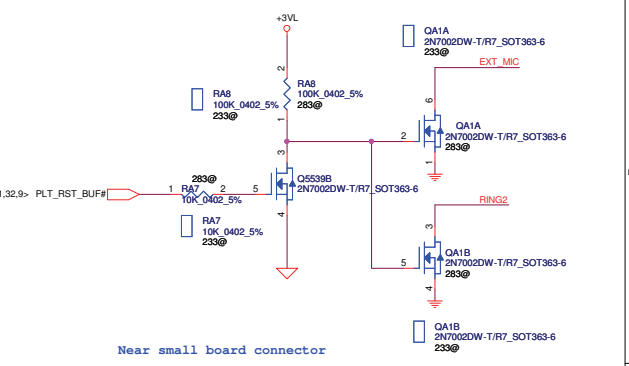
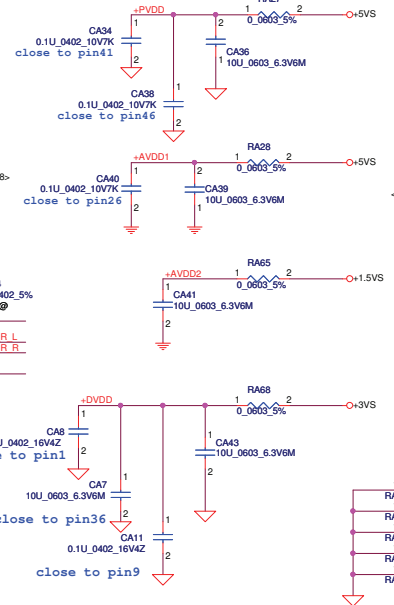
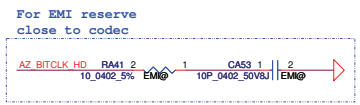
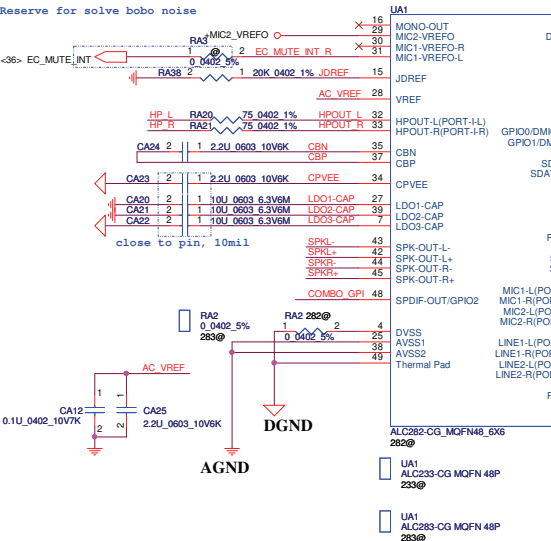


Right side USB 3.0 x 1 W/ Sleep&Charge

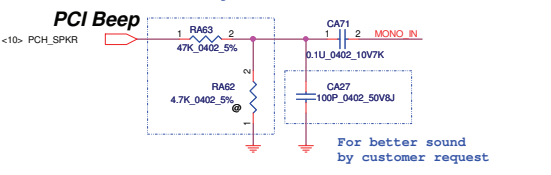


Close to UR2 IN/OUT

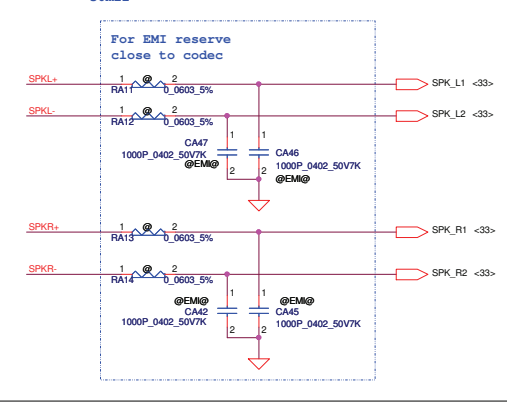




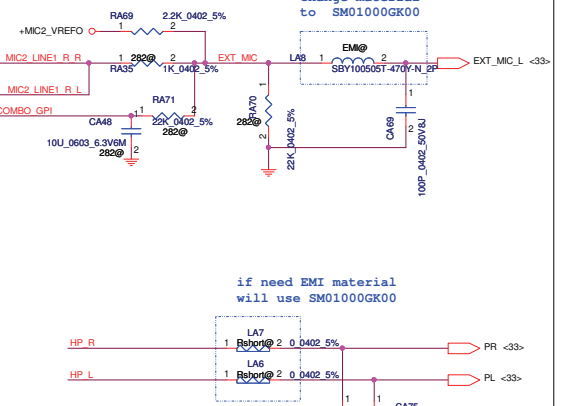
Beep sound IF need cost down and don't care common design
RA63 change to 1K
RA62 change to reserve



SPK



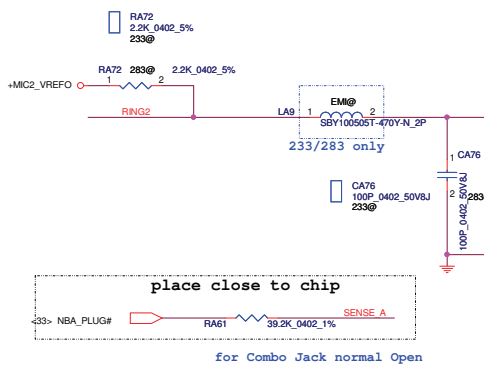
Combo Jack

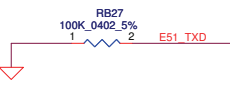
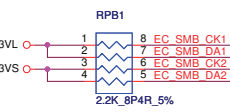
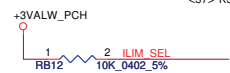
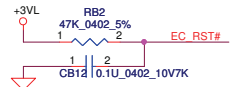
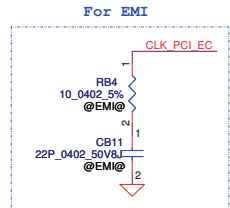


EXT_MIC · EXT_MIC_L · RING2 · RING2_L
need 40mil
RA5 · RA4 · LA8 · CA69 · LA9 · CA76 · RA6
Near small board connector

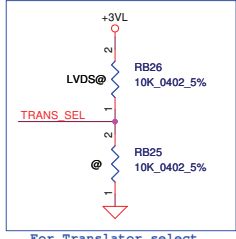
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

Need connector list,
check normal close or open
apple or nokia





Signal pull high is default status (ROM only mode).
If signal pull low, EC will send translator code to chip.(EP mode)

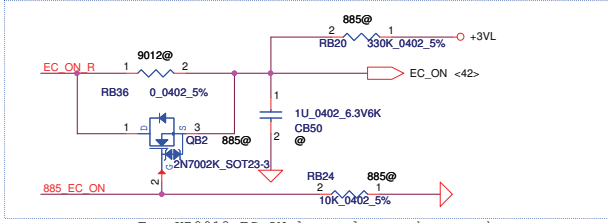


EC DEBUG port



Voltage Comparator Pins FOR 9012 A3

	>1.2V	<1.2V
VCIN0 pin109	HIGH	LOW
VCIN1 pin102	HIGH	LOW
VCOUT0 pin104	HIGH	LOW
VCOUT1 pin103	HIGH	LOW

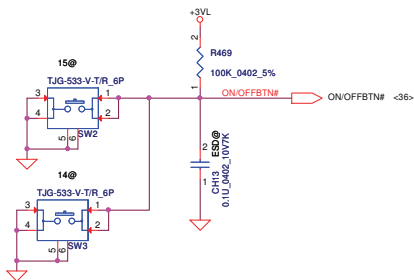


For KB9012 EC_ON low pulse work around

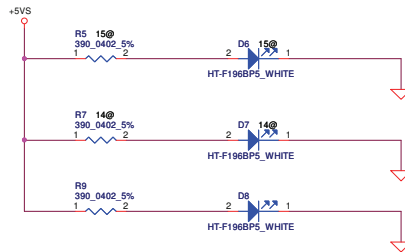
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LPC-EC-KB9012&930		
Rev	0.2	
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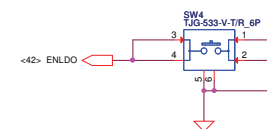
Power Button



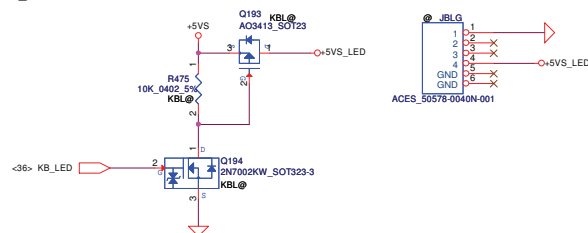
POWER LED



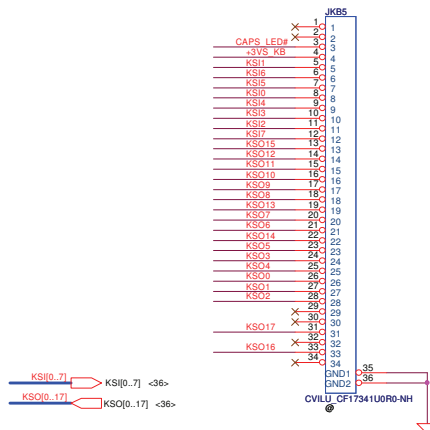
Battery Reset



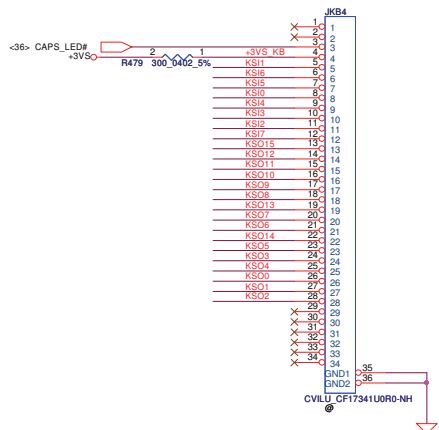
Keyboard LED



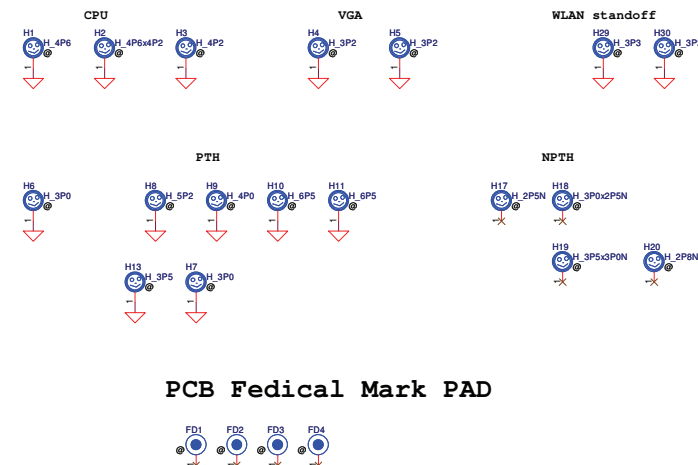
15 " KEYBOARD CONN.



14 " KEYBOARD CONN.



Screw Hole



PCB Federal Mark PAD



ISPD

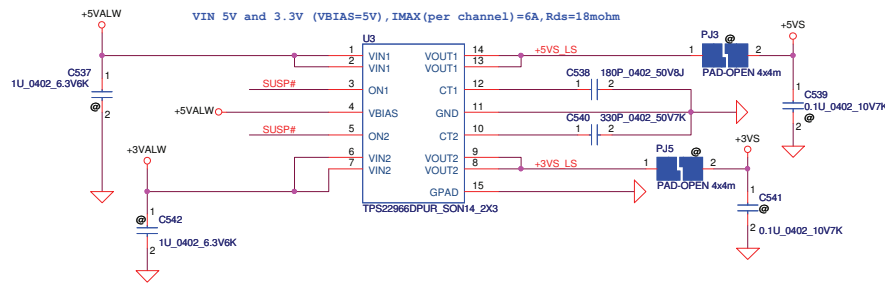


GPU

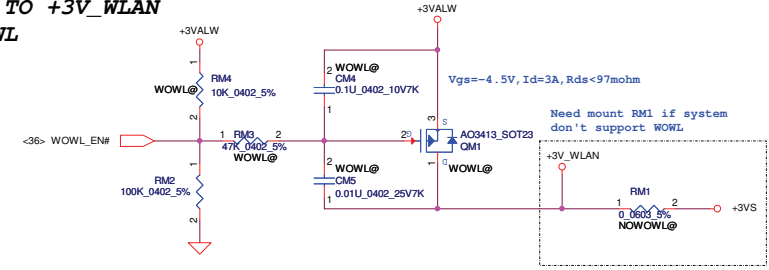


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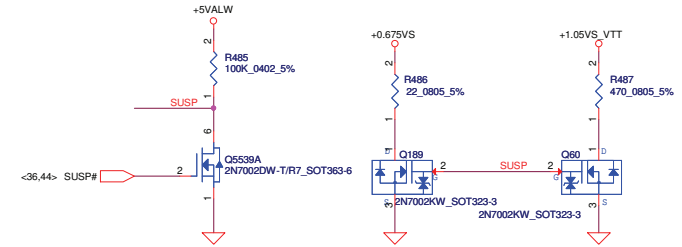
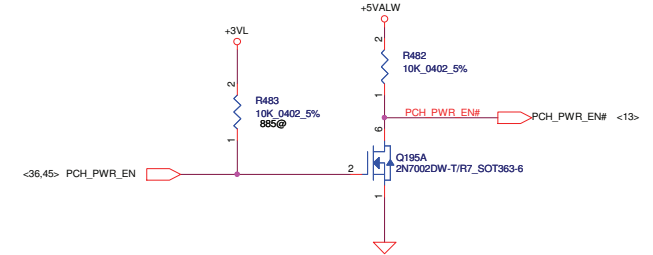
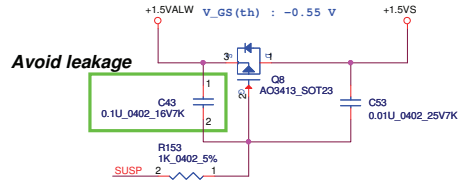
+3VALW TO +3VS **+5VALW TO +5VS** **Load Switch**



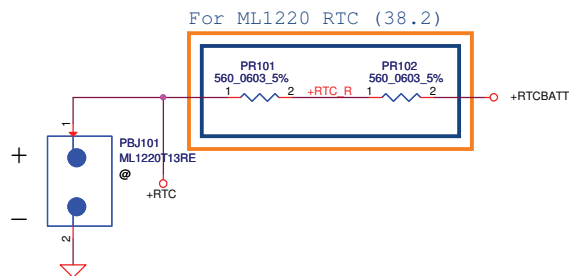
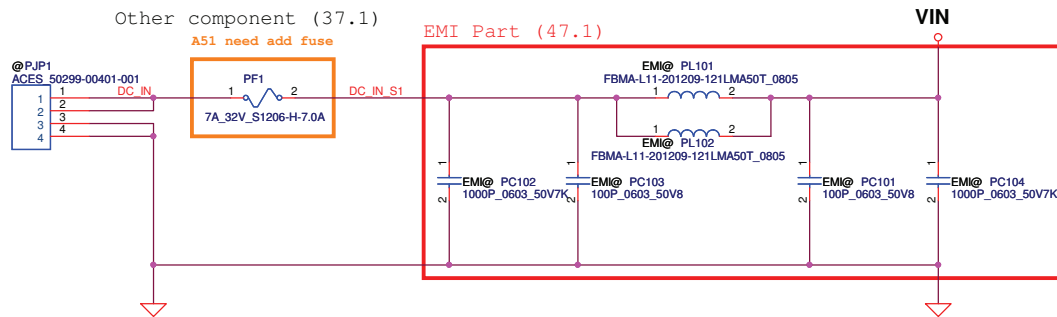
+3VALW TO +3V_WLAN **for WOWL**



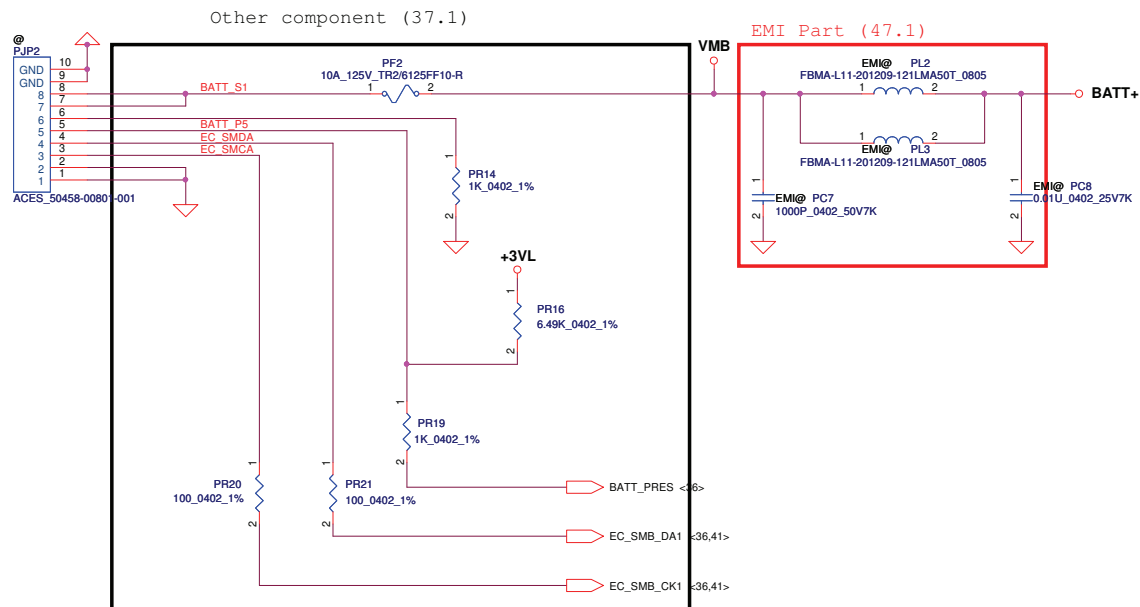
+1.5VALW to +1.5VS



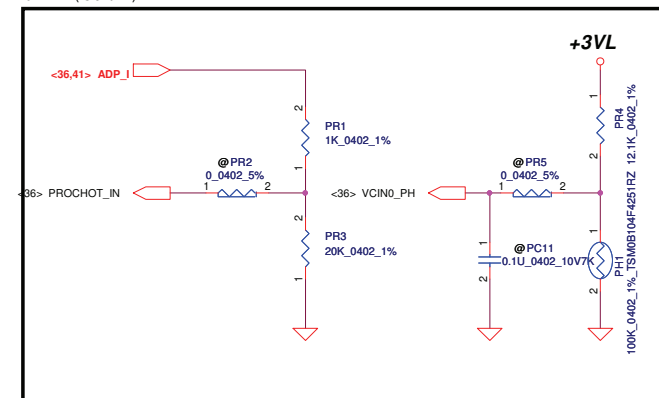
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OTP (39.7)



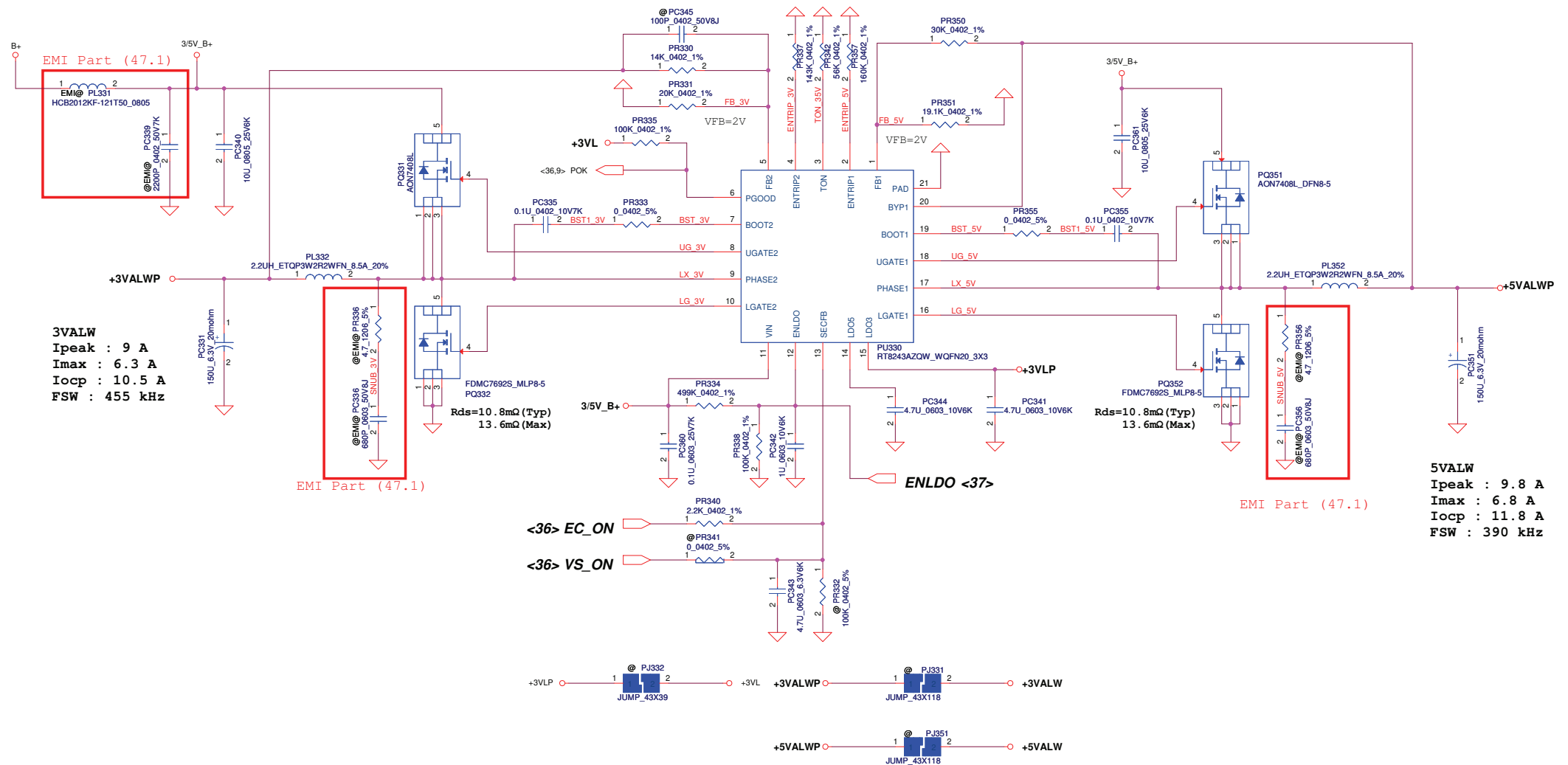
	Initial	Recovery
45W UMA	0.55V	0.43V
75W N14P-GV2	0.90V	0.72V

	Initial	Recovery
CPU OTP	90 C	70 C

Charger controller (40.1), Support component (40.2)

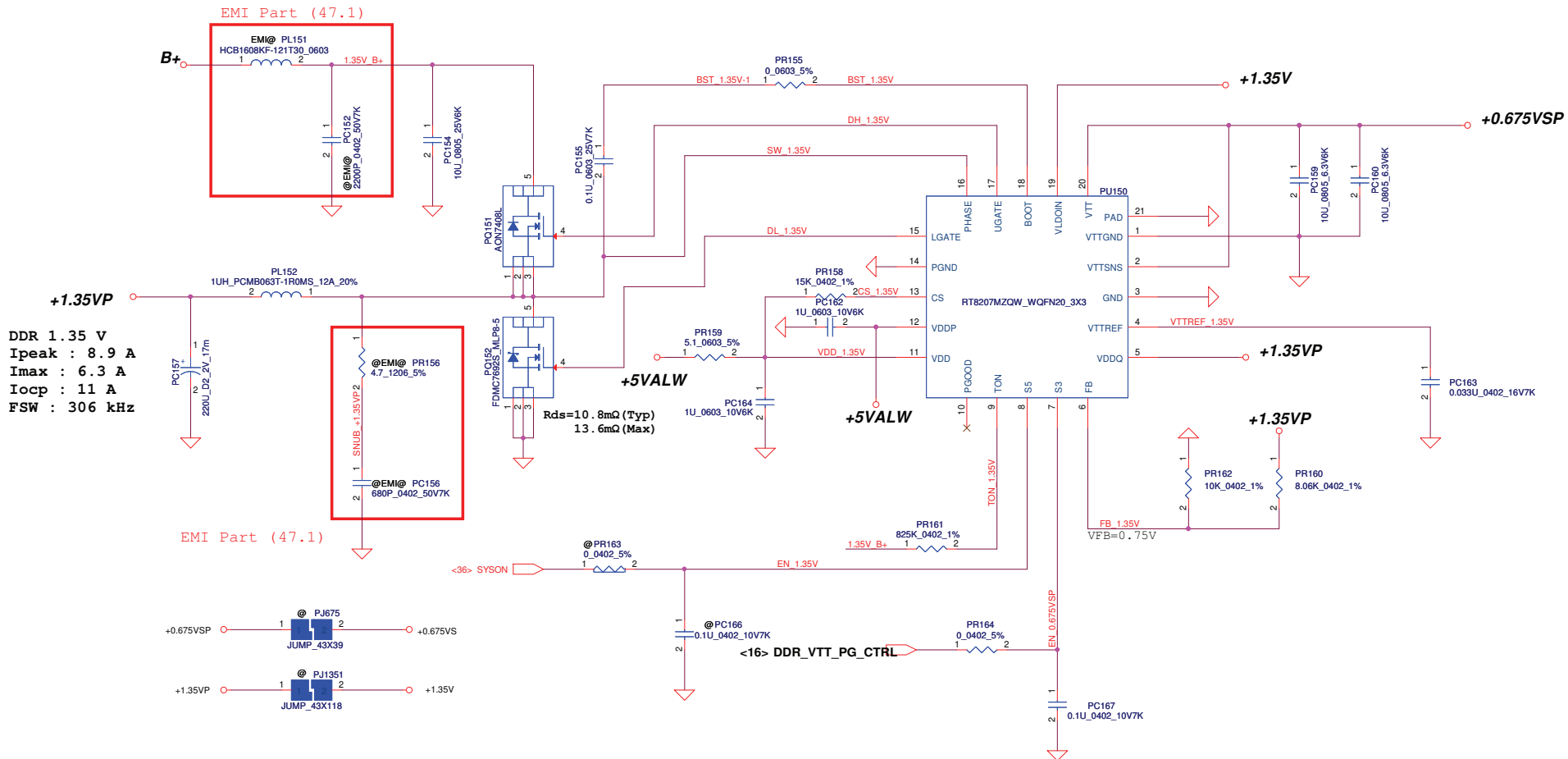


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				Size		Document Number		Rev	
						ZRMAA		0.2	
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				Size		Document Number		Rev	
						ZRMAA		0.2	
Date:		Sheet		42		of 50			

DDR controller (35.3), Support component (35.4)

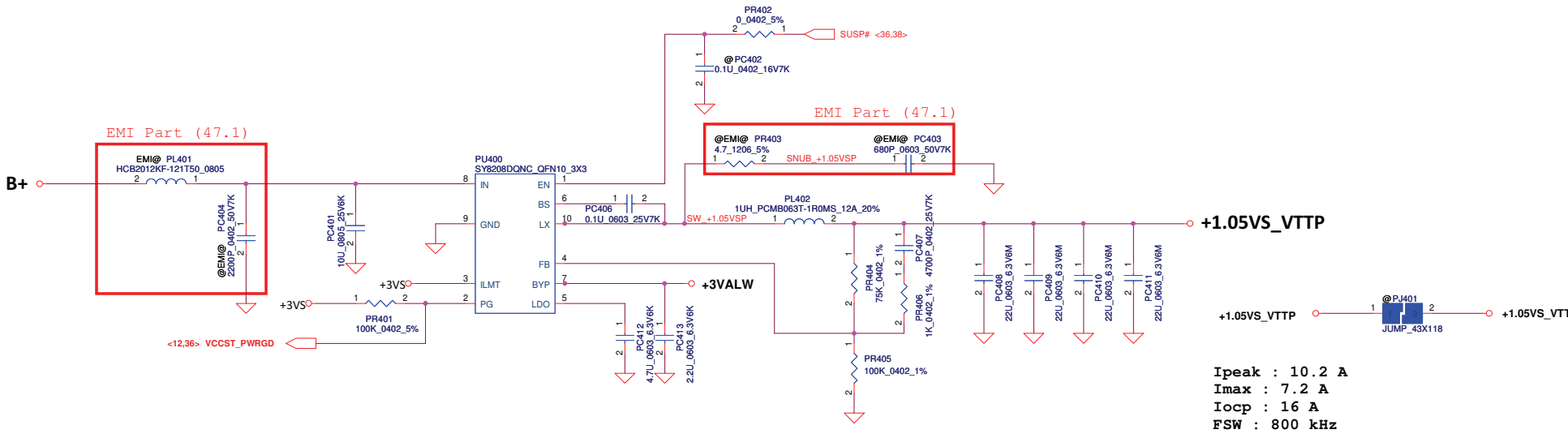


STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

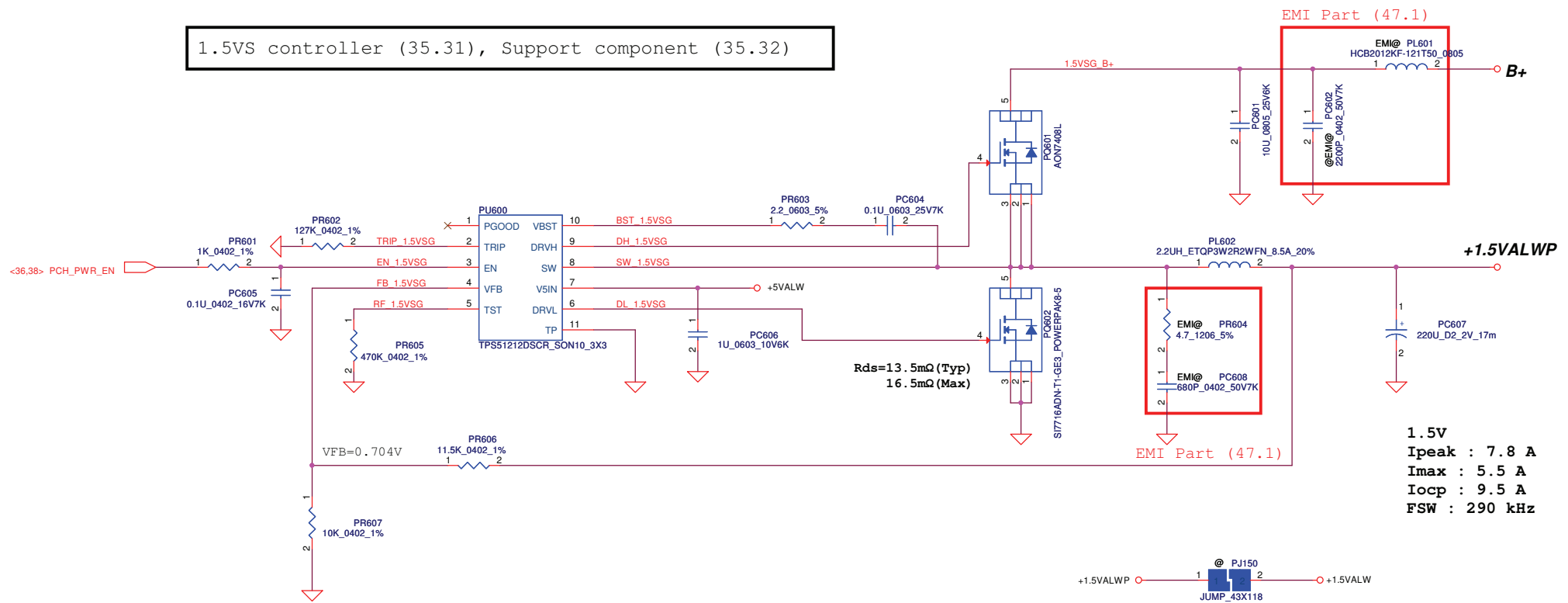
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Issued Date		Deciphered Date		Title 1.35VP/0.675VSP			
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1.05VCCP controller (35.5), Support component (35.6)



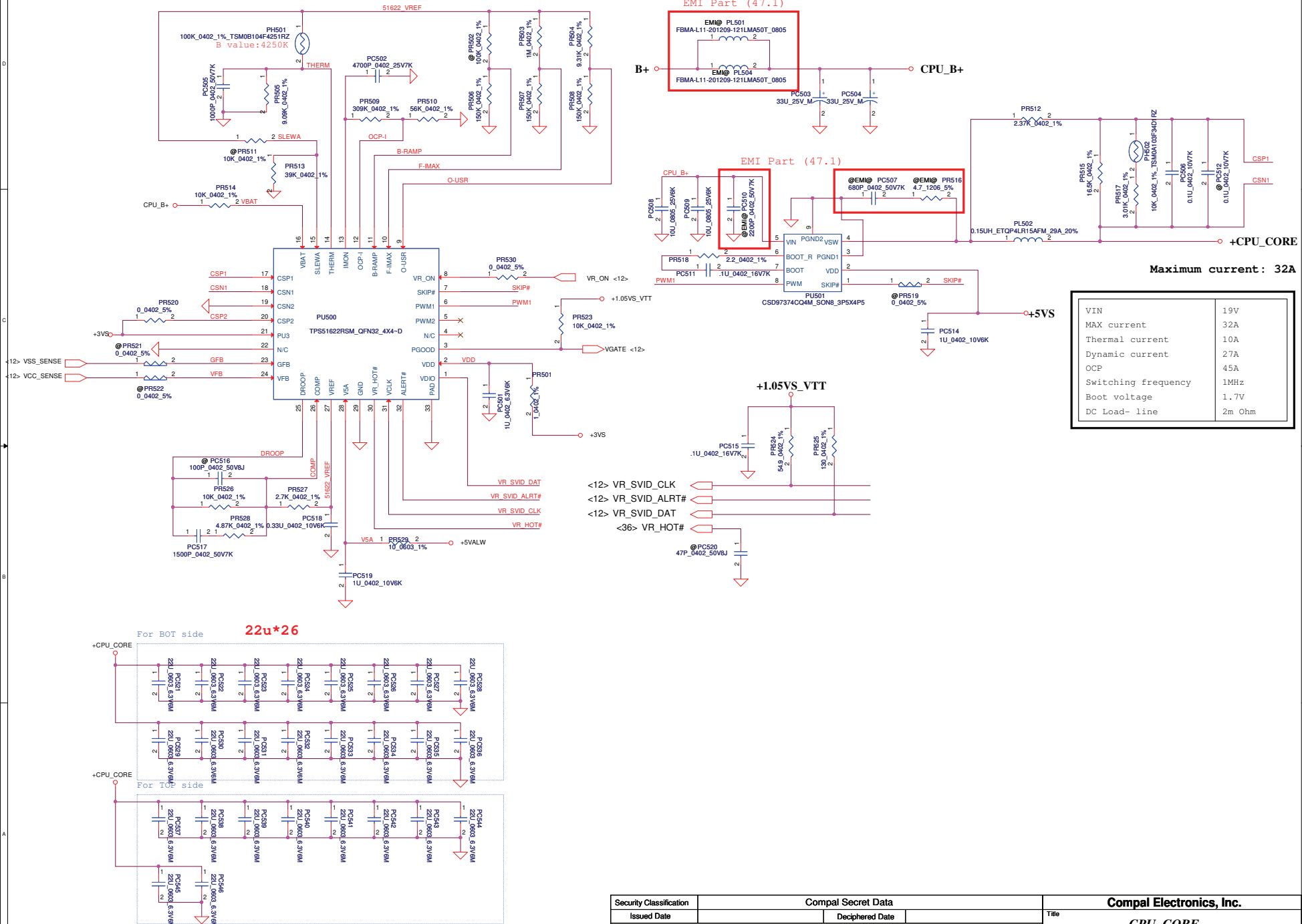
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date		Deciphered Date		Title	+1.05VS VCCP	
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					ZRMAA	0.2
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1.5VS controller (35.31), Support component (35.32)



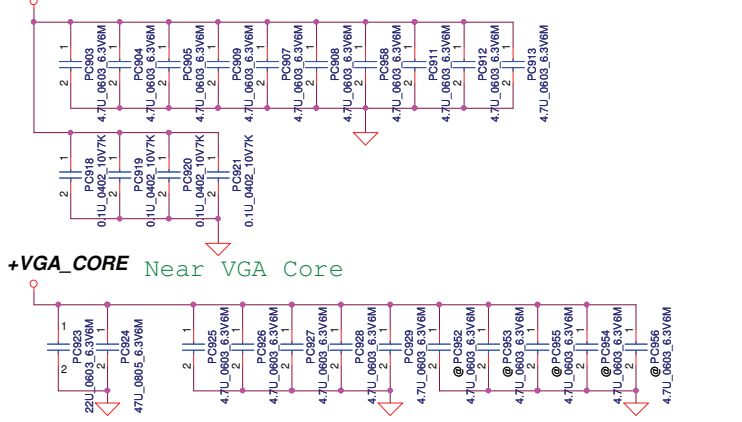
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				+1.5VS	
				ZRMMAA	
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+VCC_CORE controller (36.1), Support component (36.3)
driver(36.2), decoupling cap(36.4)

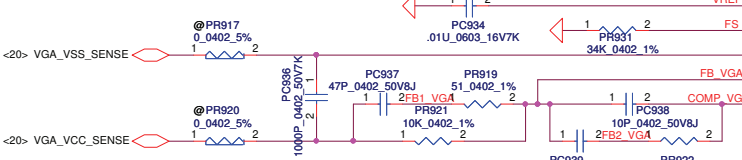
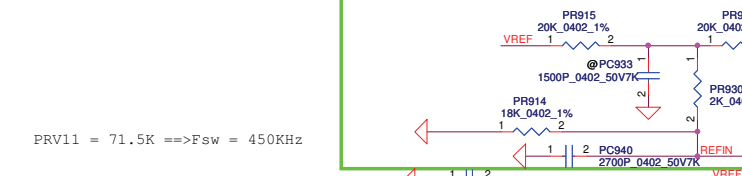


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	CPU CORE
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					ZRMMA
				Date:	Sheet 46 of 50

+VGA_CORE Under VGA Core GB4-128 package

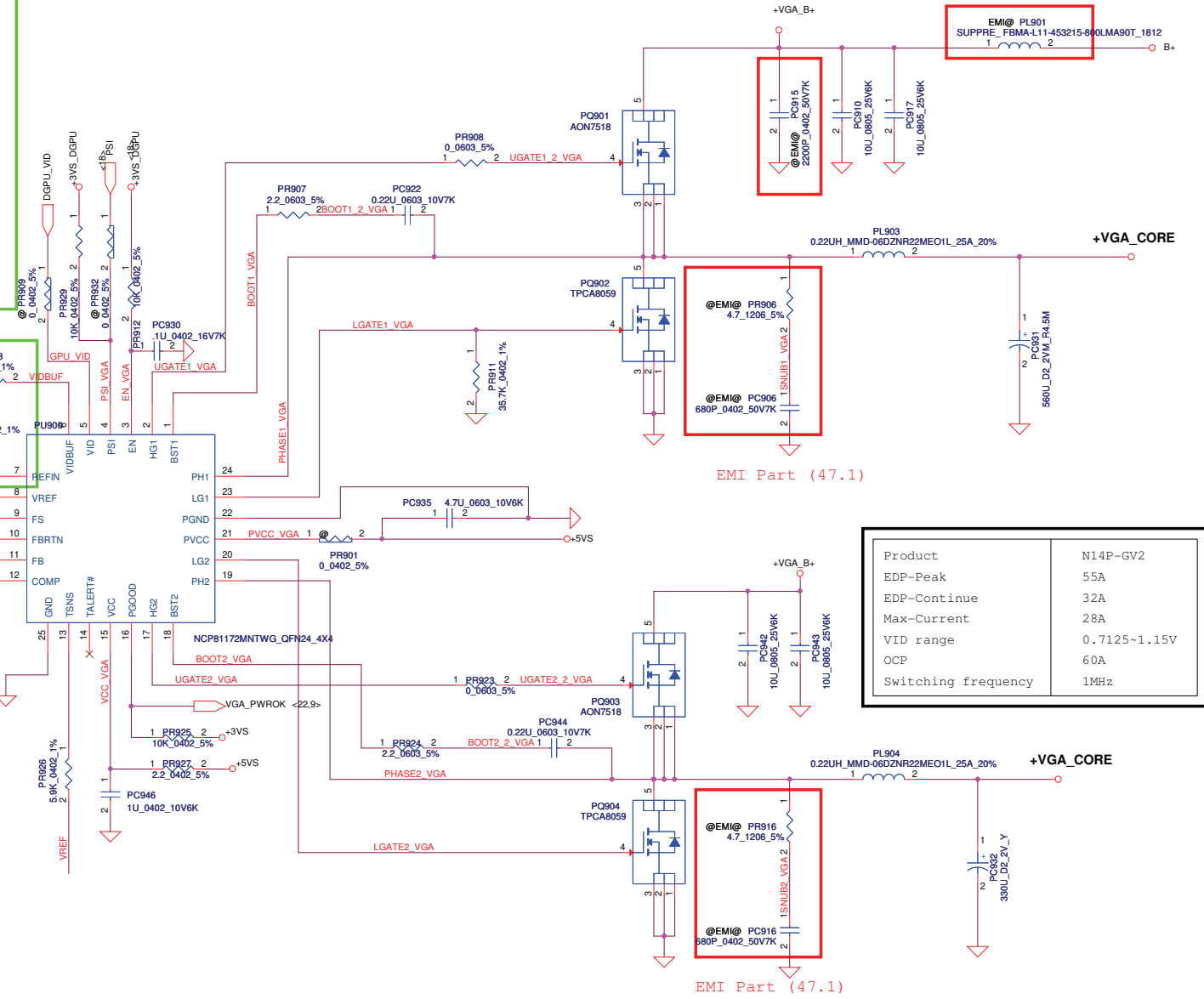


+VGA_CORE Near VGA Core



VGA_CORE controller (43.1), Support component (43.2)

EMI Part (47.1)



Product	N14P-GV2
EDP-Peak	55A
EDP-Continue	32A
Max-Current	28A
VID range	0.7125~1.15V
OCV	60A
Switching frequency	1MHz

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Issued Date	Deciphered Date	Title
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Item	Time (When)	Page (Where)	Location / Discription (How / What)	Request (Who)
1	EVT-2013/04/09	P47-PWR-GPU_CORE	PC930 / Change to Un-pop	HW
2	DVT-2013/04/18	P43-PWR-1.35VP/0.675VSP	PC157 / Change to Polymer CAP (220uF/2V/17m/D2)	Power
3	DVT-2013/04/18	P45-PWR-1.5VALW	PC607 / Change to Polymer CAP (220uF/2V/17m/D2)	Power
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HW PIR (Product Improve Record)

ZRMAA LA-A481P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.0 TO 0.1

GERBER-OUT DATE: 2013/04/01

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	03/04	36	Add EC_SMB_CK3、EC_SMB_DA3、RB135、RB136	Vendor request for LVDS Translator
2	03/04	27	Add EC_SMB_CK3、EC_SMB_DA3	Vendor request for LVDS Translator
3	03/04	31	Change JWLAN connector	For WLAN
4	03/04	31	Change JHDMI connector	For HDMI
5	03/04b	30	Change JHDD pin define	For HDD
6	03/04b	33	Delete DEVSLP0	For HDD
7	03/04b	37	ADD R5、D6、R7、D7	For Power LED
8	03/05A	07	Change FAN connector	For FAN
9	03/05A	16、17	Change DDR net order	For DDR
10	03/05A	33	Change JHP connector	For Small board
11	03/05B	19	Change RV4、RV5、RV6、RV7、RV8、RV9	For Layout placement
12	03/06A	19	Delete RV108、RV109、RV110、RV111、RV104、RV105、RV106、RV107	For Layout placement
13	03/06A	19	ADD RPV8、RPV9	For Layout placement
14	03/06A	06	Update DDR pin for DDR interleave routing	For DDR
15	03/06B	33	Change JHP to JSB4 and Add JSB5	For Small board
16	03/06B	33	ADD R44、R45、R46、R47	For Small board
17	03/06B	33	Change JKB to JKB4、ADD JKB5	For Keyboard
18	03/07A	16、17	Change JDDR3S、JDDR3R	For DDR
19	03/11A	33	Change JNGFF connector	For NGFF SSD
20	03/11A	34	Change JUSBR、JUSBF connector	For NGFF SSD
21	03/11A	37	Modify Hole	For Dummy
22	03/11B	35	ADD RA5、Q5539B for Combo Jack Normal Close	For Audio
23	03/11B	07	Change JSPK	For Speaker
24	03/12A	30	Swap JHDD pin define	For HDD
25	03/12A	29	Swap L64、L65、L66、L67	For HDMI
26	03/12A	37	Change D6、D7 material and Add D8、R19	For 14" 15" LED
27	03/12A	37	Add SW3 for 14"	For Power Button
28	03/12B	37	Add H18、H19 Delete H7、H14、H15	For Hole
29	03/12C	37	Change CCL2 and RCL5 @ to GCLK@	For Green clock
30	03/12C	37	Delete E51_TXD(RB27)、E51_RXD	For WLAN
31	03/12D	31	Change JWLAN to NGFF E type	For WLAN
32	03/13A	37	ADD KSO17、KSO16 for 15" keyboard	For keyboard
33	03/13A	36	Change TRANS_SEL to pin75、CHG_PWR_GATE# to pin89	For keyboard
34	03/13A	36	ADD KSO17、KSO16 for 15" keyboard	For keyboard
35	03/13A	36	Delete BT_ON Pin34	For WLAN
36	03/13A	17、6	Change DDR to no interleave routing	For DDR
37	03/13B	36	Change LAN_WAKE# from UB1.108 to UB1.71	For EC
38	03/13B	36	Change WAKE# to EC_SWI# and connect to UB1.108	For EC
39	03/13B	34	Swap L60、L56、L71、L72	For DDR3
40	03/13B	37	Delete Q196	For WLAN LED
41	03/13B	35	Delete CA54、CA56	For Audio
42	03/13B	35	Swap JSPK	For Audio
43	03/14A	34	Swap LR7、LR8	For USB
44	03/14A	16、17	Swap JDDR3R、JDDR3S	For DDR
45	03/14B	33	Swap R44、R45、R46、R47	For Small board
46	03/14B	36	ADD JDB for EC debug	For Debug
47	03/14B	18	Change XTAL_OUTBUFF、XTAL_SSIN to RPV1.3、RPV1.4	For VGA
50	03/14B	18	Change SMB_CLK_GPU、SMB_DATA_GPU to RPV2.3、RPV2.4	For VGA
51	03/14B	16、17	JDDR3R、JDDR3S to JDDR3H、JDDR3L	For DDR
52	03/14B	31、36	ADD BT_ON	For WLAN
53	03/14B	36	EC_SMB_CK3、EC_SMB_DA3 change use 2.2K	For LVDS SM Bus
54	03/14B	10	Delete R307、R220	For Audio sleep & music
55	03/15A	5、10、37	Change CH7,D98,D99 BOM config from @ESD@ to ESD@	For ESD's request.
56	03/15A	36	Change CB14 BOM config from @ to ESD@ for ESD's request.	For ESD
57	03/15A	35	Delete RA50 for sleep & Music	For Audio
58	03/15A	35	Swap JSB5 and modify JSB4、JSB5 pin define	For Small board
59	03/18A	05	Change CH11 from 180PF to 100PF for ESD's request.	For ESD
60	03/18A	36	Change CB13 from 100PF to 0.1UF for ESD's request.	For ESD

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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	HW-PIR	
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HW PIR (Product Improve Record)

ZRMAA LA-A481P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.0 TO 0.1

GERBER-OUT DATE: 2013/04/01

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
61	03/18A	10	Change CH7, CB14 from 180PF to 0.1UF for ESD's request.	For ESD
62	03/18A	37	Change D98,D99 to CH12, CH13 for ESD's request.	For ESD
63	03/19A	31	Modify JWLAN	For WLAN
64	03/19A	31	Modify JSB4、JSB5 pin define & Add R49、R50、R53、R51	For Small board
65	03/19B	33	Change JNGFF connector	For SSD
66	03/19B	29、28	Swap RP1、RP2、D97、L61、L62	For Layout
67	03/20A	37	R480 +5VS change to +5VALW	For WLAN
68	03/20A	33	Delete LR5(USB20_P2_L、USB20_N2_L), change to small board	For EMI
69	03/20B	33	JNGFF pin1、pin13、pin61、pin67 connect to GND	For SSD
70	03/20B	21	Delete LV4、RV32、RV33、RV34、RV50 (N14MGL@)	For VGA
71	03/20C	28	Swap D97	For Layout
72	03/20D	31	Delete LED_WIMAX#、RM6 (didn't support WIMAX)	For WLAN
73	03/20D	37	Delete Q157、R480 (didn't support WIMAX)	For WLAN
74	03/21A	28	Change U50 BOM config from IEDP@ to always mount.	For LVDS issue
75	03/21A	28	Change R436 BOM config from LVDS@ to @.	For LVDS issue
76	03/21A	28	Change R436 BOM config from LVDS@ to @.	For LVDS issue
77	03/21A	38	Change Q6(SB570020110) to Q5539A(SB00000EO10)	For Layout placement
78	03/21A	36	Add RR8、RR9 then connected to CB0_WAKE# and LAN_WAKE#	For LAN_WAKE#
79	03/21A	36	Add EC_CB1 at pin97	For LAN_WAKE#
80	03/21A	33	Change U13,U15 from SA00004KB00 to SA00003TV00.	For power switch issue on Rosetta
81	03/21A	34	Add RR6、RR7,change RR2、RR3 14641@ to @	For USB Sleep and Charge
82	03/21A	36	Add RR6 then connected to CHG_CB0 and EC_CB0	For USB Sleep and Charge
83	03/21A	34	Add RB11、RB13 on EC_CB0、EC_CB1 then pull-high to +3VALW_PCH	For USB Sleep and Charge
84	03/21A	33	Modify JNGFF Config pin define and add SSD_Detect pin	For SSD
85	03/21A	10	R215 change to 10K pull high 3.3V,PROJECT_ID change to SSD_Detect	For SSD
86	03/25A	35	EC_MUTE_INT change to COMBO_GPI and add CA48(10u)	For Audio Combo jack
87	03/25A	36	Delete EC_MUTE_INT、RB38、RB39	For Audio Combo jack
88	03/25A	33	Add test point	For SSD
89	03/25A	35	Add RA71、change Combo jack GND to AGND、Change NBA_PLUG to NBA_PLUG#	For Audio
90	03/25A	35	Swap Q5539.3(NBA_PLUG) and Q5539.5(NBA_PLUG#)	For Audio
91	03/25A	35	change +MIC_VREFO to UA1.31	For Audio
92	03/25A	37	change ZZZ part number to DA8000Y0000	For Mother board location
93	03/25A	35	Add RA50 Reserve for solve noise issue	For Audio
94	03/25A	36	Add RB38、RB39 fo Reserve solve S3、S4、S5 bo bo issue	For Audio
95	03/25A	31	JWLAN.42(CLK_EC) connect to U1H.AE6 for WLAN NGFF type use	For WLAN
96	03/25A	31	Delete pin64、66 net	For WLAN
97	03/25A	34	Change RB11,RB13 from un-mount to mount.	For Sleep & Charge
98	03/26A	10	ADD R30 for SSD detect	For SSD
99	03/26A	10	ADD RV32 for VRAM Strap pin	For VRAM
100	03/26A	32	Change JRJ45 footprint	For JRJ45
101	03/26A	37	H19 change to H_3P5x3P0N、H20 change to H_2P8N	For ME hole
102	03/26A	36	Delete RB5	For WLAN
103	03/26B	34	ADD RB5 Reserve for Seligo wake function	For USB switch
104	03/27A	34	Swap LR7	For Layout
105	03/27B	38	Change Q195 SB570020110 to SB00000DH00	For layout
106	03/27B	36	Delete RB38(EC_MUTE_INT_R)	For Audio
107	03/27B	38、35、34	Change Q195、Q5539、QR1、Q5540、SB00000EO10 to SB00000DH00	For X1 code
108	03/27B	18、8	Change QV1、QV2、QV4、QV5、QV7、QV9、QH4 SB00000EO10 to SB00000DH00	For X1 code
109	03/27B	29	Change Q190、Q191 SB501110010 to SB00000PF00	For X1 code
110	03/27B	32	Change JRJ45 connector	For LAN
111	03/29A	37	H29、H30 change to H_3P2、ADD H7 H_3P0、H13 change to H_3P5	For ME
113	03/29A	36	Delete RB39	For Audio
114	04/01A	35	ADD RA2、MIC2_R_C_L、MIC2_R_C_R、MIC2_LINE1_R_L、MIC2_LINE1_R_R	For Audio 282 colay with 233
115	04/01A	35	Change +MIC1_VREFO(UA1.31) to +MIC2_VREFO(UA1.29)	For Audio

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HW PIR (Product Improve Record)

ZRMAA LA-A481P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2013/04/28

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	04/02A	29	ZZZ change to ZZZ1	For HDMI
2	04/02A	A11	Delete Footprint *NEW and *-NEW word	For Layout footprint
3	04/02A	35	ADD UA1 233@	For Audio
4	04/02A	21	ADD RV2、CV115、CV116、CV117 and change RV1、CV56、CV32、CV24 to ME@	For ME request
5	04/02A	21	ADD CV118、CV119、CV120、CV121 and change CV28、CV27、CV29、CV40 to ME@	For ME request
6	04/03A	19	ADD LV4 and change LV3 to ME@	For ME request
7	04/03A	35、36	ADD RA3、EC_MUTE_INT connect to EC UB1.122	For Audio bobo noise issue
8	04/03A	35	RA62 change to @	For vendor request
9	04/03A	35	Delete RV2、CV120、CV121 and change to N14PGV2@	For Layout
10	04/03A	35	Change JRJ45 SANTA_130456-311 to SANTA_130456-491	For ME request
11	04/09A	36	Change UB1 Material SA000040B20 (A3) to SA000040B30 (A4)	For EC
12	04/09A	36	Change QB1 Material SB570020020 to SB000000EN00	For PUR cost request
13	04/09A	28	Change U50 Material SA007080100 to SA000000OH00	For Main source common
14	04/09A	35	Delete Q5539、RA5	For Audio combo jack normal open
15	04/09A	33	Change NBA_PLUG to NBA_PLUG#	For Audio combo jack normal open
16	04/15A	22	Change RV54 33K to 4.7K	For +3VS_DGPU sequence faster
17	04/15A	35	Change LA8 KC_FBMA-10-100505-300T_2P to CHILI_SBY100505N-221Y-N_2P	For Layout
18	04/15A	37	Delete H12 and change H9 to H_4P0	For ME request
19	04/16A	31	ADD RC287、RC288、RC289、RC290、RC291、RC292、RC293、RC294、RC295	For mini PCIE WLAN
20	04/16A	31	ADD JWLAN1	For mini PCIE WLAN
21	04/16A	36	Delete UB1.26 FANPWM、ADD UB1.68 DFAN1	For FAN Control Circuit
22	04/16A	07	ADD U4、C26、R25、C24、C25、C32、Change JFAN	For FAN Control Circuit
23	04/16A	07	Delete R32、C4、R33、D1、C5	For FAN Control Circuit
24	04/16B	07	Delete RC292、RC293、ADD C161、C163、RC296、RC297、RC298、RC299、RC300	For mini PCIE WLAN
25	04/16B	07	ADD RC301、RC302、	For mini PCIE WLAN
26	04/16B	07	Change H8 H_5P0 to H_5P2	For ME hole
27	04/16C	07	Delete RC287、RC302	For mini PCIE WLAN
28	04/18A	19	Delete LV4、LV3 config change to OPT@	For mini PCIE WLAN
29	04/18A	35	Change LA8 Footprint to CHILI_SBY100505T-470Y-N_2P	For Audio
30	04/22A	31	JWLAN pin64、66 connctect to +3V_WLAN	For WLAN
31	04/22A	36	UB1.89 CHG_PWR_GATE# change to ILIM_SEL	For USB sleep & charge
32	04/22A	34	Change USB sleep & charge chip to TPS2546RTER (Delete U5、U14、ADD UR4)	For USB sleep & charge
33	04/22A	34	Swap D87、D88	For USB3.0 Layout
34	04/23A	34	Swap L56、L60、L71、L72	For USB3.0 Layout
35	04/23B	35	ADD RA4、RA5 75ohm	For Audio
36	04/23B	34	Swap LR7	For Layout
37	04/23B	07	U4 SA00002XA00 EOL change use SA00003UO00	For FAN
38	04/24A	37	H29 change to H_3P3、H4、H5 change to H_3P2	For ME modify
39	04/24B	31	ADD WLAN net name、C161、C163 change to page 11	For WLAN
40	04/24B	34	UR4.5 USB_CHG_EN# change to USB_CHG_EN	For USB sleep & charge
41	04/24B	36	UB1.18 USB_CHG_EN# change to USB_CHG_EN	For USB sleep & charge
42	04/24B	36	CR10 4.7U_0805 change to 4.7U_0603、ADD RR16 20K_0402_1%	For USB sleep & charge
43	04/24D	34	ADD CR8、ILIM_SEL_R、CHG_CB0、CHG_CB1、EC_CHG_CB2	For USB sleep & charge
44	04/24D	35	Add CA49、CA76、CR8、QA1、RA6、RA7、RA72、RA8、LA9	For co-lay Audio 233/282/283
45	04/24D	35	Delete CA44、Change CA7	For co-lay Audio 233/282/283
46	04/25A	35、36	Delete EC_MUTE_INT、RA3、EC_MUTE_INT_R	For co-lay Audio 233/282/283 Line-in
47	04/25A	35	Add CA54、CA55、RA36、RA37、RA73、RA74	For co-lay Audio 233/282/283 Line-in
48	04/26A	33	Add LR9、LR10	For EMI request
49	04/26B	35	+LINE1_VREFO-R、+LINE1_VREFO-L change to +LINE1_VREFO_R、+LINE1_VREFO_L	For Audio
50	04/26C	33	Swap LR9、LR10	For Layout
51	04/26C	35	Delete +LINE1_VREFO_R、+LINE1_VREFO_L、RA73、RA36、RA37、CA54、CA55	For no support Line-in
52	04/26C	35	Delete RA74	For no support Line-in
53	04/26D	19	Delete LV4	For Layout
54	04/26D	02	Modify Block Diagram	For Schematic
55	04/26E	32	Change UL2 material	For Cost request
56	04/26F	32	Delete R4283、change PCIE_WAKE# to LAN_WAKE#	For LAN
57	04/26F	33	change SSD_Detect to SSD_DETECT#、ADD C4、C5、C6	For SSD
58	04/27G	32	Change UL2 material	For ME request
59	04/28A	35	Change Q5539B AGND to GND、Change title	For Audio
60	04/28A	33	Change title USB-CardReader Genesys GL834L to NGFF SATA/S_B conn/SPK	For Title
61	04/28B	08	RH66 0ohm change to 33ohm	For SPI EA report
62	04/29A	34	RR3、RR4 change config to @、Change UR4 to UR2、Delete CR9	For USB sleep & charge

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HW PIR (Product Improve Record)

ZRMAA LA-A481P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2013/04/28

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
63	04/29B	10	Change R272 0603 to 0402	For EC

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	HW-PIR
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