BL1

CPU CORE Page:25 — VCC_CORE

+3VPCU / +3V_S5/+3VSUS / +3V
+5VSUS/+5V / +12V Page:26 — +3VPCU, +3V_S5, +3VSUS, +3V, +5VSUS, +5V, +12V

+1.8VSUS/+1.8V / +1.2V / +0.9VSUS Page:27 — +1.8VSUS, +1.8V, +1.2V, SMDDR_VTERM

+1.8V_S5 / +1.05V Page:26,29 — +1.8V_S5, VTT

BATTERY CHARGER Page:28

Power State Table

Power Name	Control Signal	Power State	Power Source
VCC_CORE	VRON	S0	VIN
+3VPCU	N/A	ALWAYS	VIN
+3V_S5	S5_ON	S0-S5	+3VPCU
+3VSUS	SUSON	S0-S3	+3VPCU
+3V	MAINON	S0	+3VPCU
+12V	MAINON	S0	
+1.2V	MAINON	S0	
+1.05V	MAINON	S0	+1.8VSUS
+0.9V	MAINON	S0	+1.8VSUS
+1.8V_S5	S5_ON	S0-S5	+3VPCU
+1.8VSUS	SUSON	S0-S3	VIN
+1.8V	MAINON	S0	+1.8VSUS

CLOCK GEN
RTM865-300
+3V Page:4

CELERON-M/PENTIUM-M
INTEL Mobile_479 CPU
Page:2, 3

HOST BUS 400MHZ

NB
RC410MB/RC410MD
ATI
Page: 5, 6 , 7, 8

RGB → **CRT** Page: 10
LVDS → **LVDS** Page: 10

DDR-II SODIMM1 Page: 9
DDR-II SODIMM2 Page: 9
DDR-II

2X PCIE

SB
ATi SB450
Page: 11, 12, 13, 14

SATA HDD Page: 18 — SATA
IDE-ODD Page: 18 — ATA 66/100
HD AUDIO

PCI BUS 33MHZ
USB 2.0
LPC 33MHZ

ENE PCMCIA CB1410
AD17
REQ3# / GNT3#
INTE#
Page: 16
→ **TYPE II SLOT** Page: 16

MINI-PCI Wireless LAN
AD20
REQ1# / GNT1#
INTG# , INTH#
Page: 17

REALTEK RTL8100CL
AD18
REQ0# / GNT0#
INTF#
Page: 15
→ **BOTHHAND TRANSFORMER NS0013** Page: 15
→ **RJ45** Page: 15

AUDIO CODEC
REALTEK ALC861
Page: 19

GMT G1432+G1410 Page: 20
MODEM AGERE DELPHI-MOM Page: 21,22

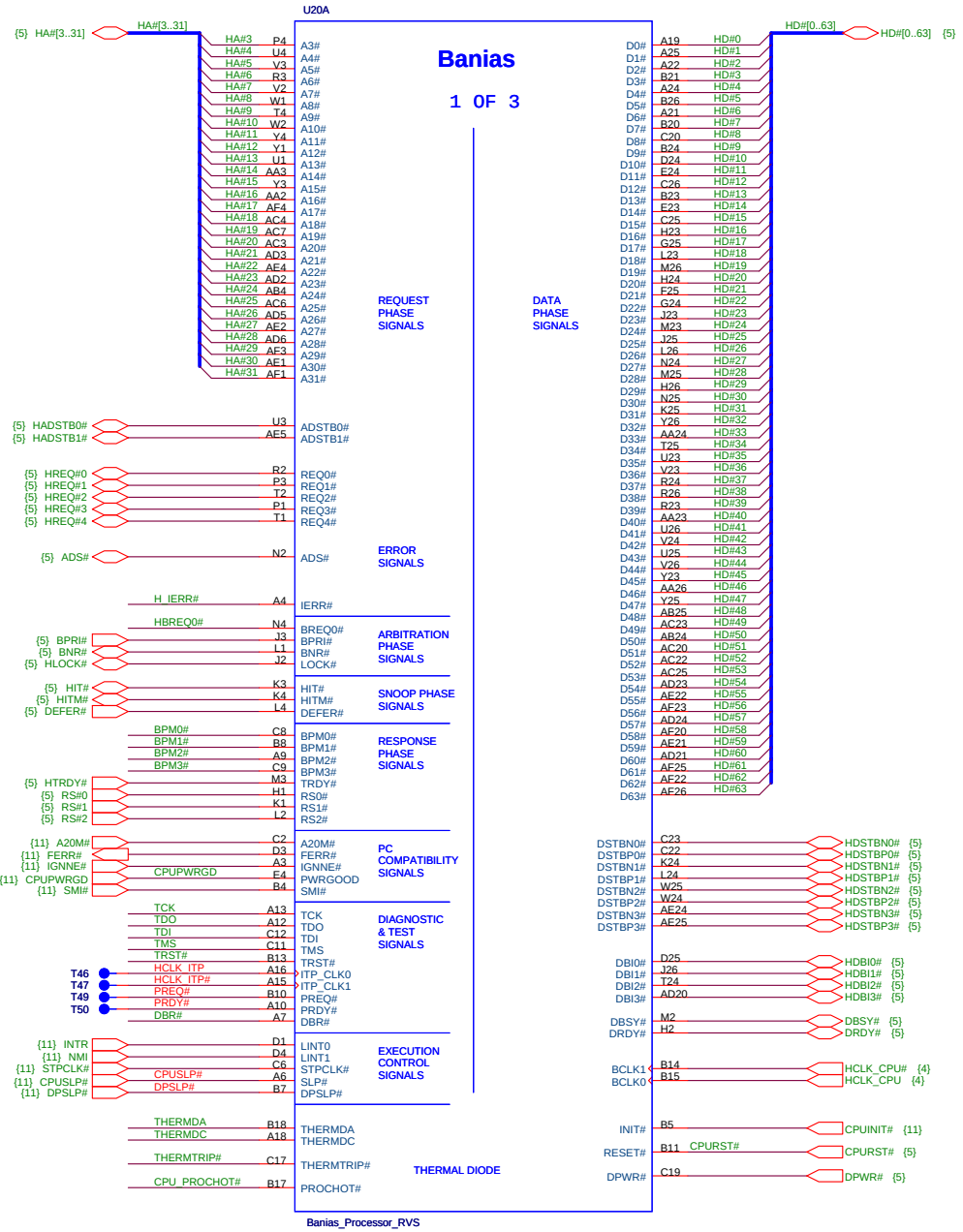
KBC NS PC97541V Page: 23

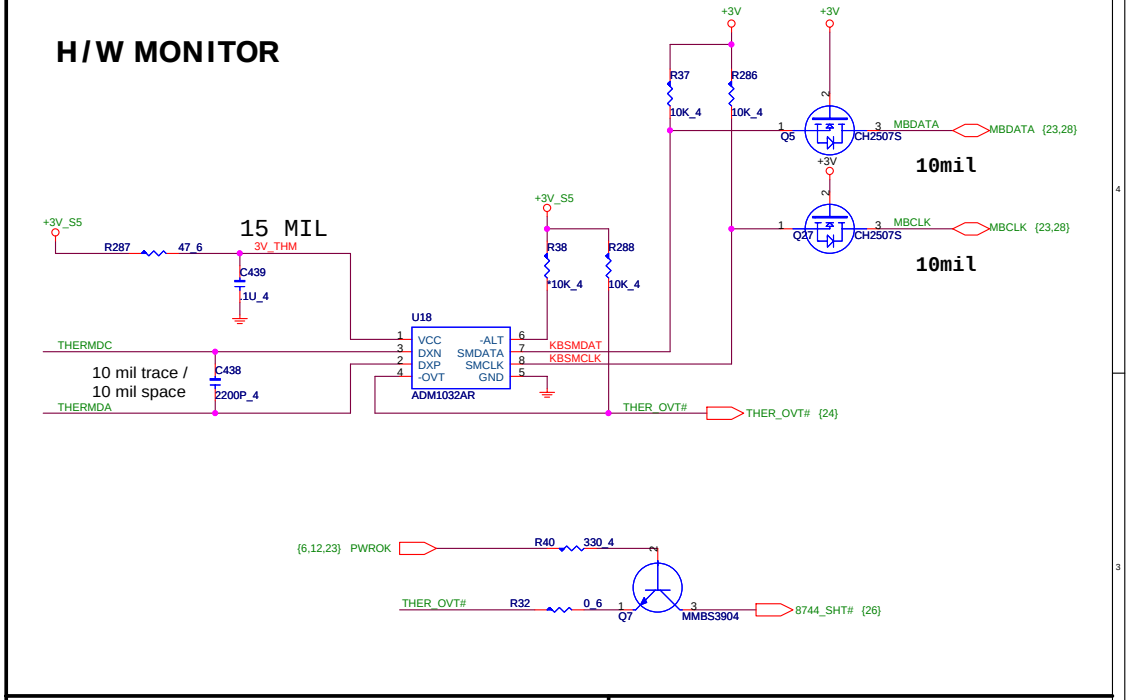
MIC IN Page: 20
SPEAKER Page: 20
LINE OUT Page: 20
RJ11
Touchpad Page: 24
Keyboard Page: 24
FLASH Page: 24
FAN Page: 24

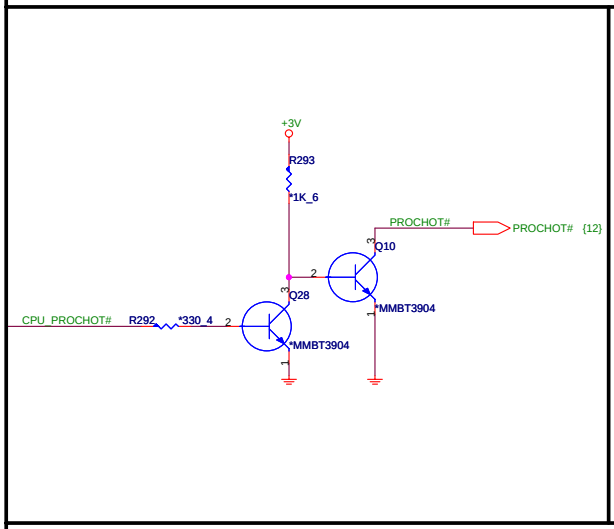
SYSTEM USB PORT *2
USB2,3
Page: 17

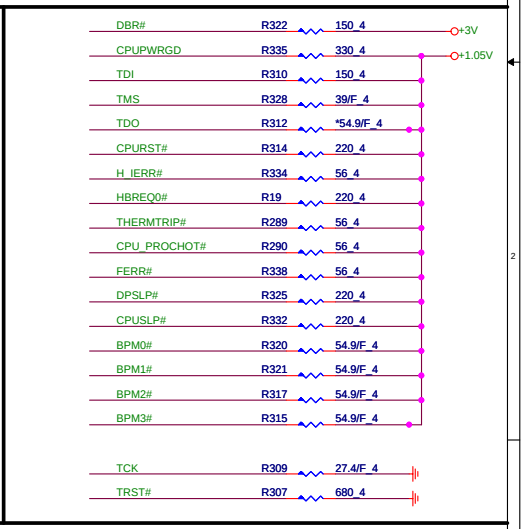
PROJECT : BL1
Quanta Computer Inc.

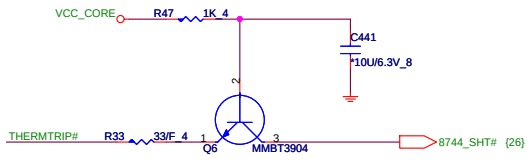
Size	Document Number	Rev
	BLOCK DIAGRAM	1A
Date: Saturday, January 07, 2006	Sheet 1 of 29	











CPU

POWER CHECK

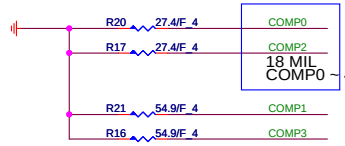
VCC_CORE {3,25}
+3V {4,6,7,8,9,10,11,12,13,14,16,17,18,19,20,23,24,25,26,27}
+1.05V {3,4,5,6,8,11,13,26,29}

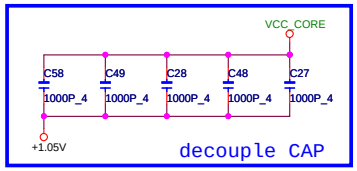
PROJECT : BL1

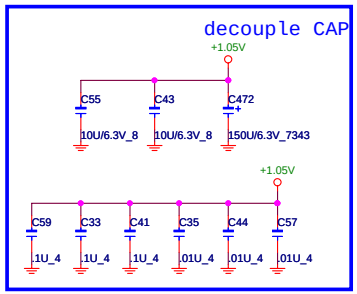
Quanta Computer Inc.

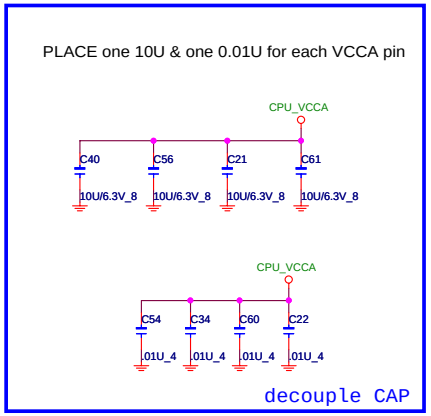
Size	Document Number	Rev
	CPU (HOST BUS)-1	1A

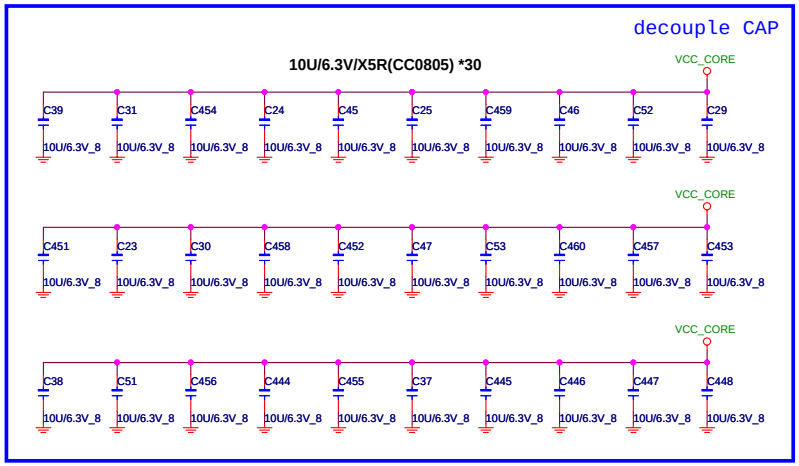
Date: Saturday, January 07, 2006 Sheet 2 of 29



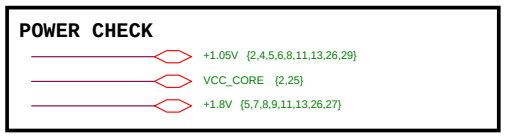


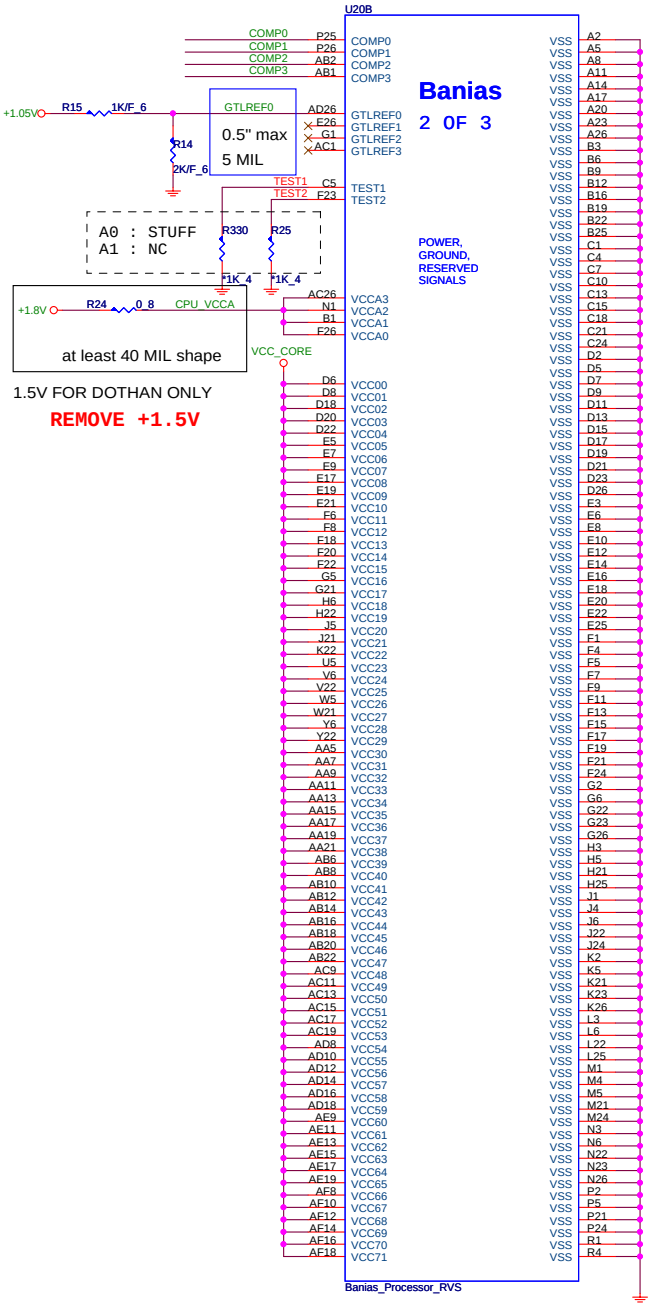


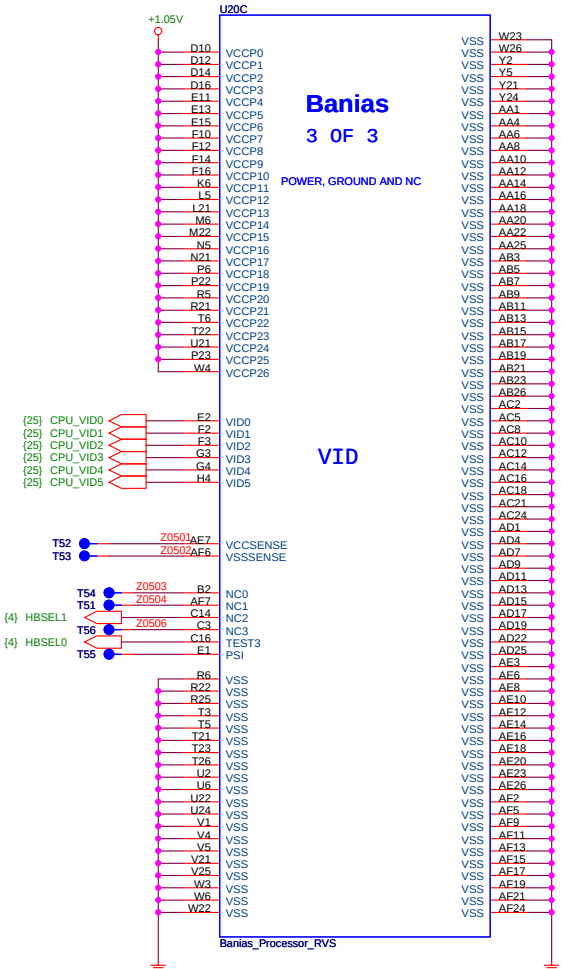




CPU





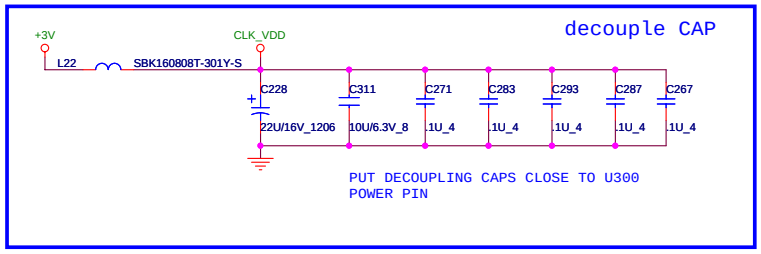


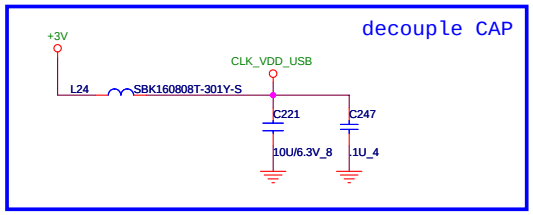
PROJECT : BL1

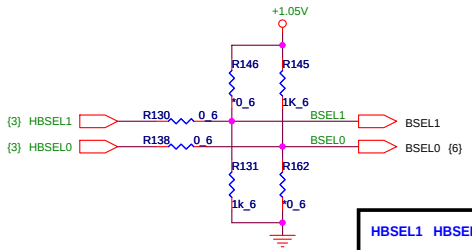
Quanta Computer Inc.

Size	Document Number	Rev
	CPU (POWER)-2	1A

Date: Saturday, January 07, 2006 Sheet 3 of 29







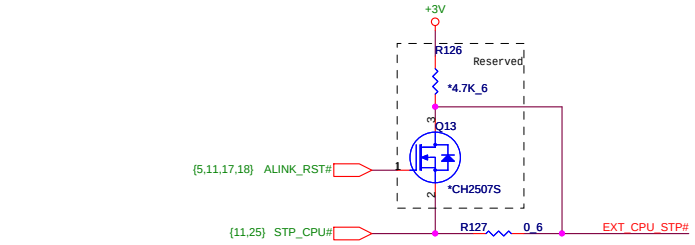
HBSEL1	HBSEL0	
0	0	133 MHz
0	1	100 MHz

CLK

POWER CHECK

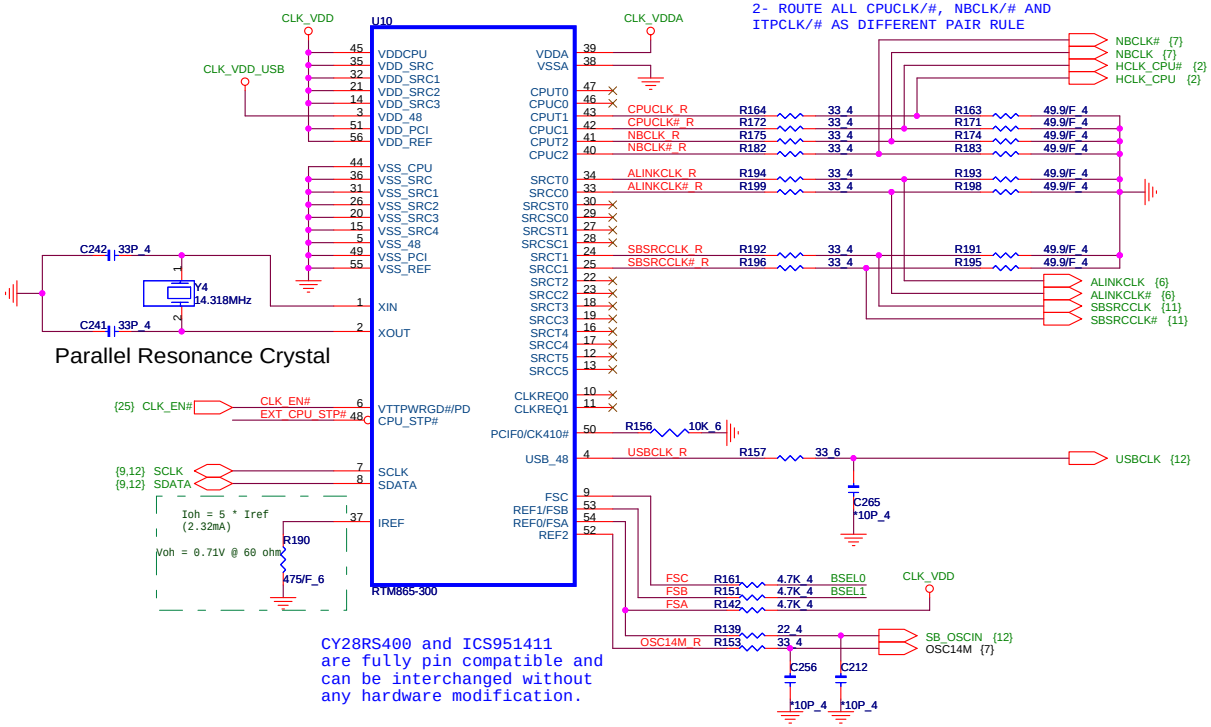
+3V {2,6,7,8,9,10,11,12,13,14,16,17,18,19,20,23,24,25,26,27}

+1.05V {2,3,5,6,8,11,13,26,29}



1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS CLK GEN AS POSSIBLE

2- ROUTE ALL CPUCLK/#, NBCLK/# AND ITPCLK/# AS DIFFERENT PAIR RULE



CY28RS400 and ICS951411 are fully pin compatible and can be interchanged without any hardware modification.

CK410 FREQUENCY SELECT TABLE(MHZ)

FSC	FSB	FSA	CPU
BSEL0	BSEL1		MHz
0	0	0	266.66
0	0	1	133.33
0	1	0	200.00
0	1	1	166.66
1	0	0	333.33
1	0	1	100.00
1	1	0	400.00
1	1	1	Rsvd

PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	EXTERNAL CLKGEN	1A

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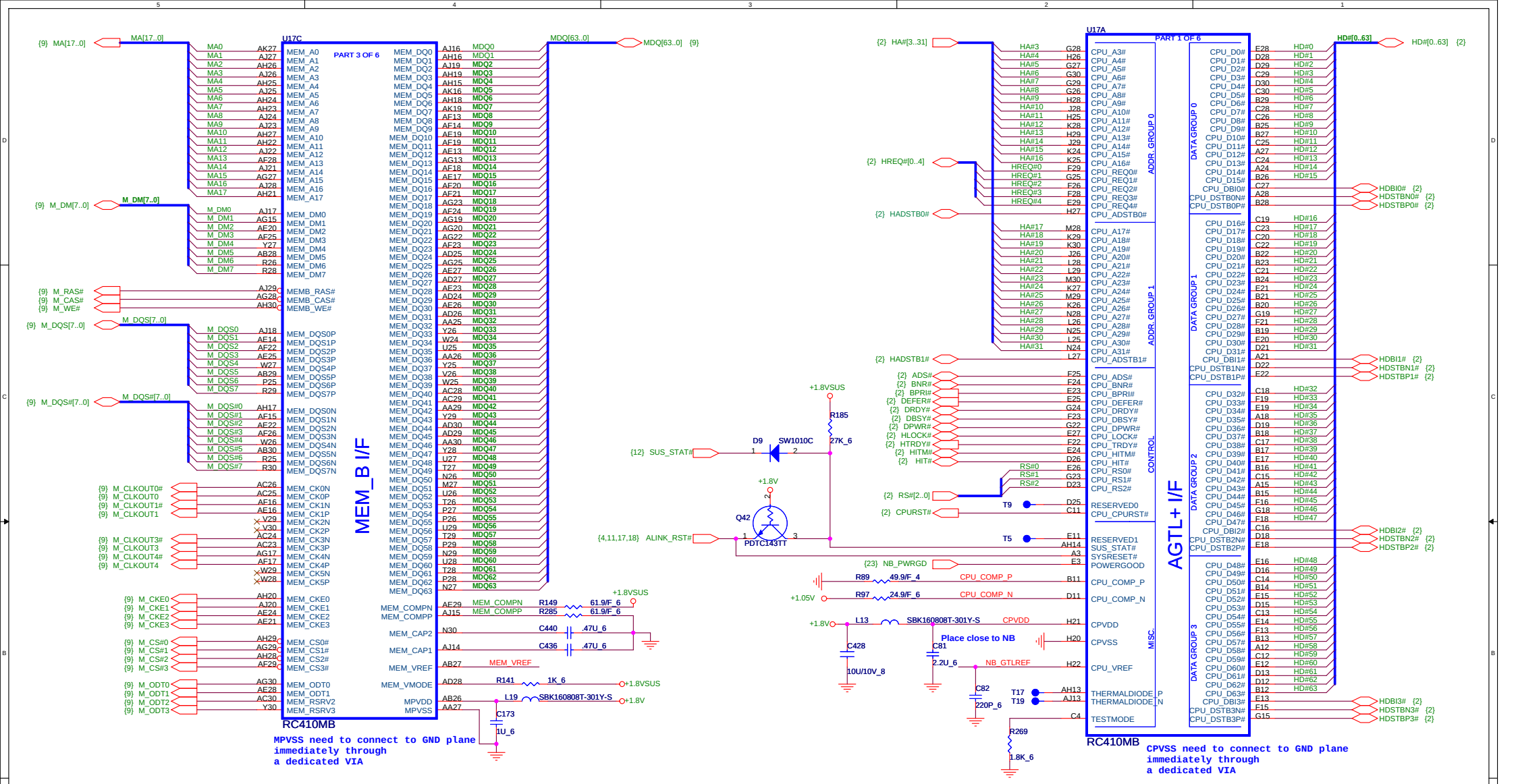

CLG

POWER CHECK

- +1.05V {2,3,4,6,8,11,13,26,29}
- +1.8VSUS {8,9,13,26,27,29}
- +1.8V {3,7,8,9,11,13,26,27}

PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	RC410MB-AGTL+ I/F	1A

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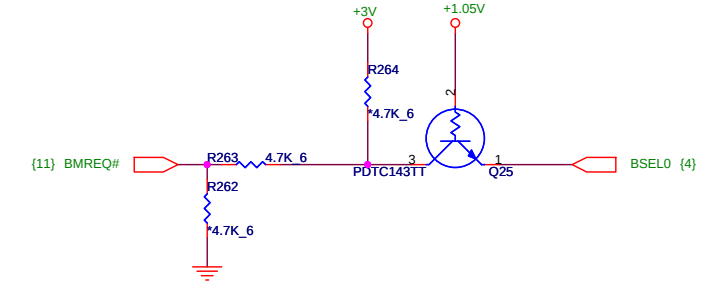
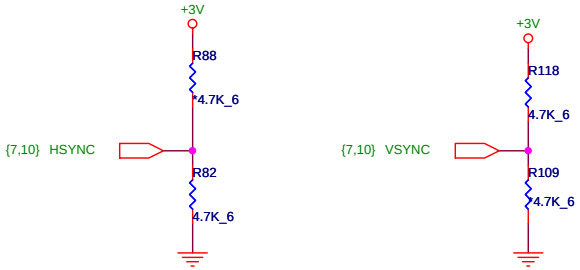
NB strapping



BSEL1	BSEL0	
0	0	133 MHz
0	1	100 MHz

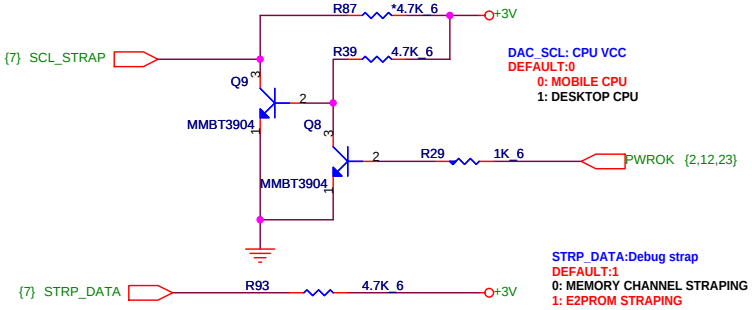


BMREQ#&HSYNC&VSYNC: FSB CLK SPEED

DEFAULT: 101

101: 100 MHZ RC420MB

001: 133 MHZ RC420MD



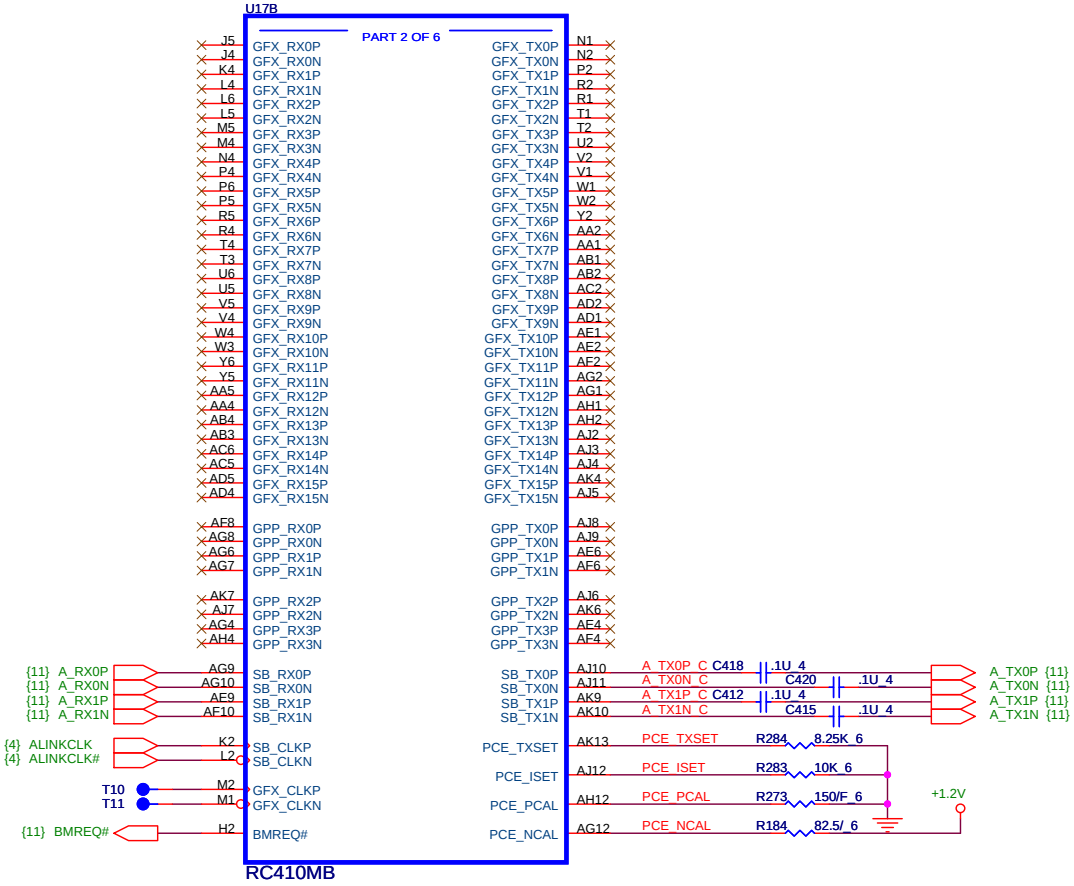
DAC_SCL: CPU VCC
DEFAULT:0
0: MOBILE CPU
1: DESKTOP CPU

STRP_DATA:Debug strap
DEFAULT:1
0: MEMORY CHANNEL STRAPING
1: E2PROM STRAPING

CLG

POWER CHECK

- +1.2V {8,26,27}
- +3V {2,4,7,8,9,10,11,12,13,14,16,17,18,19,20,23,24,25,26,27}
- +1.05V {2,3,4,5,8,11,13,26,29}



PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	RC410MB-PCIE LINK I/F	1A

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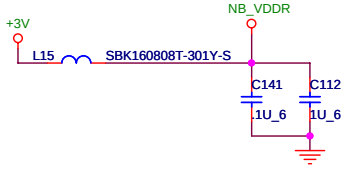
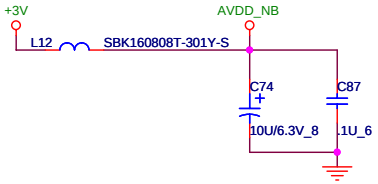
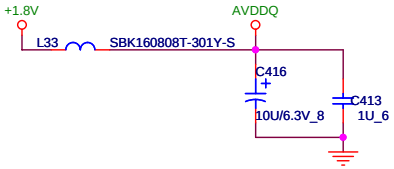
decouple CAP

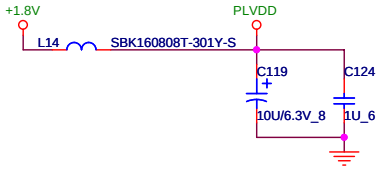
FOR VDDR3 ,S0 max:100mA



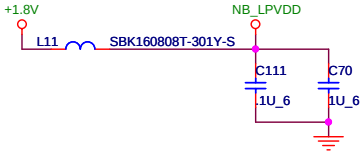
FOR AVDD ,S0 max:250mA

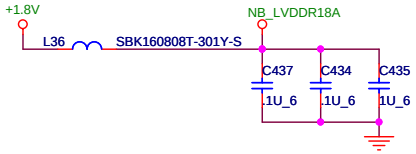


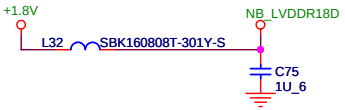




PUT AVDD_NB, AVDDQ,NB_VDDR,
PLVDD,NB_LPVDD,NB_LVDDR18D,NB_LVDDR18A DECOUPLING
CAPS ON THE BOTTOM SIDE, CLOSE TO BALLS







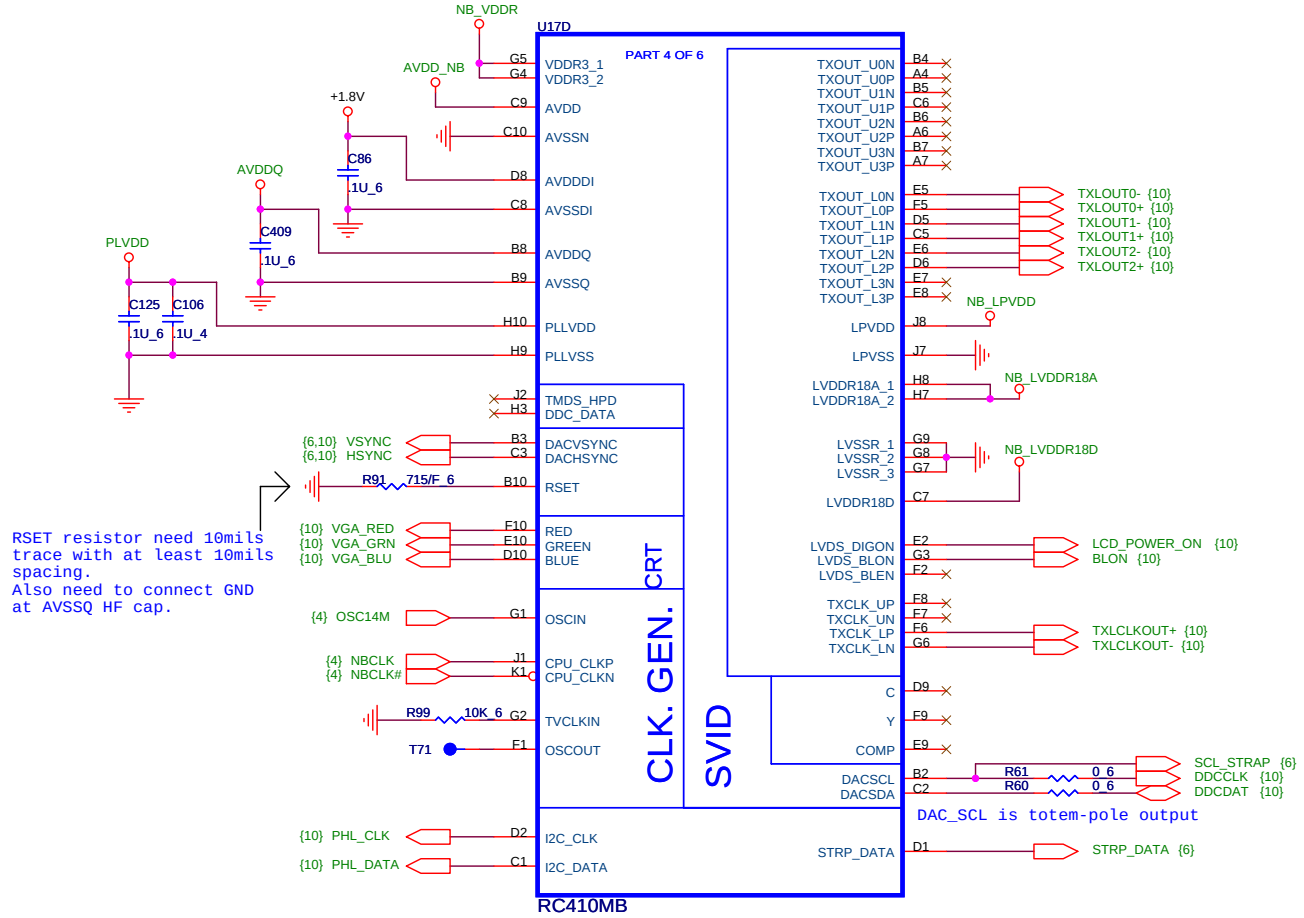
FOR CPVDD,MPVDD,AVDDQ,PLLVDD,AVDDDI,LPVDD,LVDDR18A,LVDDR18D
,S0 total max:300mA

CLG

POWER CHECK

+3V {2,4,6,8,9,10,11,12,13,14,16,17,18,19,20,23,24,25,26,27}

+1.8V {3,5,8,9,11,13,26,27}



RSET resistor need 10mils
trace with at least 10mils
spacing.
Also need to connect GND
at AVSSQ HF cap.

PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	RC410MB-VIDEO & CLKGEN	1A
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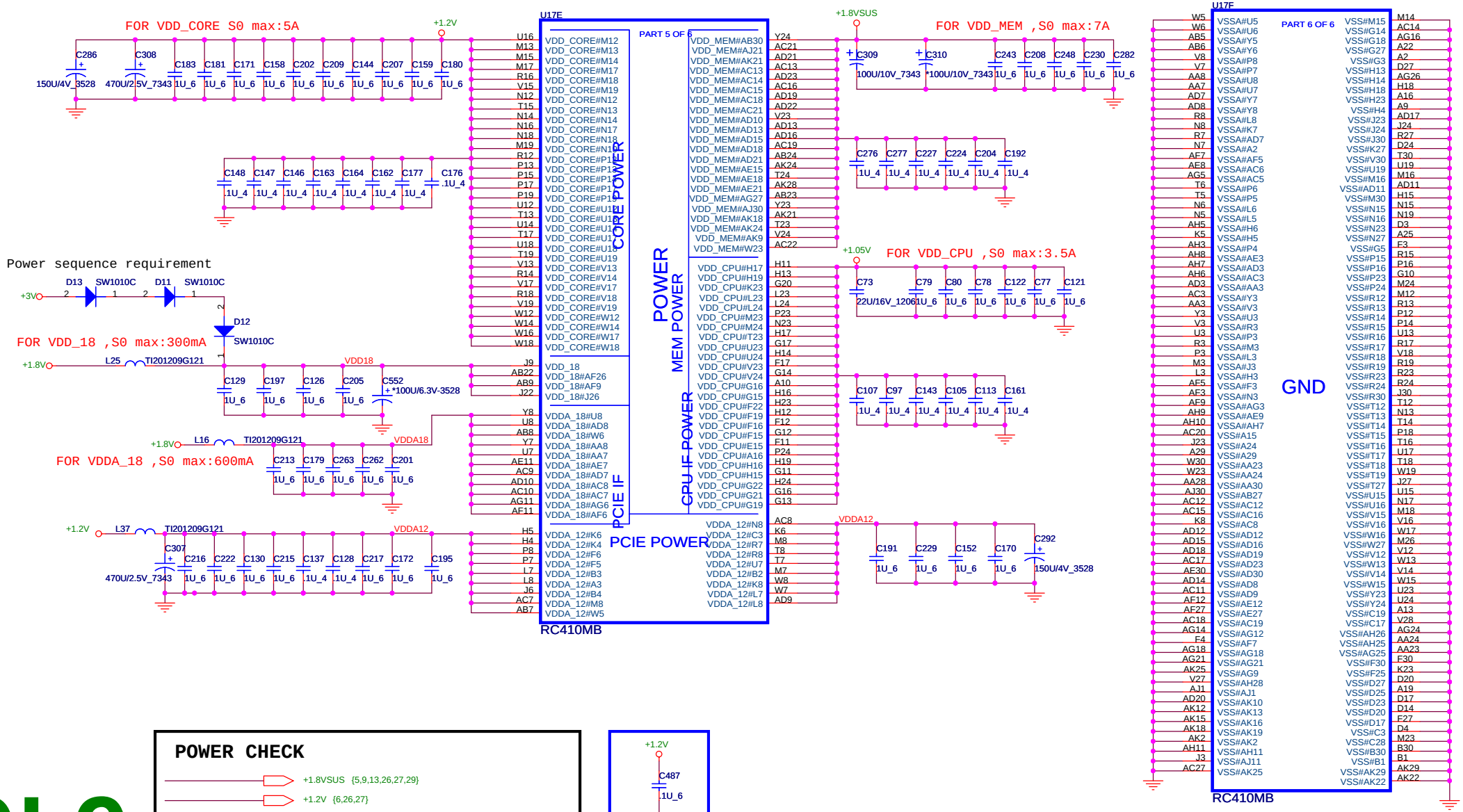
FOR VDD_CORE S0 max:5A
+1.2V
U17E
PART 5 OF 6
CORE POWER
MEM POWER
CPU IF POWER
PCIE IF
PCIE POWER
RC410MB
Power sequence requirement
+3V
D13
SW1010C
D11
SW1010C
D12
SW1010C
FOR VDD_18 ,S0 max:300mA
+1.8V
L25
TI201209G121
VDD18
FOR VDDA_18 ,S0 max:600mA
L16
TI201209G121
VDDA18
+1.2V
L37
TI201209G121
VDDA12
FOR VDD_MEM ,S0 max:7A
+1.8VSUS
FOR VDD_CPU ,S0 max:3.5A
+1.05V
VDDA12
U17F
PART 6 OF 6
GND
RC410MB
POWER CHECK
+1.8VSUS {5,9,13,26,27,29}
+1.2V {6,26,27}
+1.05V {2,3,4,5,6,11,13,26,29}
+1.8V {3,5,7,9,11,13,26,27}
+3V {2,4,6,7,9,10,11,12,13,14,16,17,18,19,20,23,24,25,26,27}
+1.2V
C487
1U_6
FOR EMI
CLG
PROJECT : BL1
Quanta Computer Inc.
Size
Document Number
RC410MB-POWER
Rev
1A
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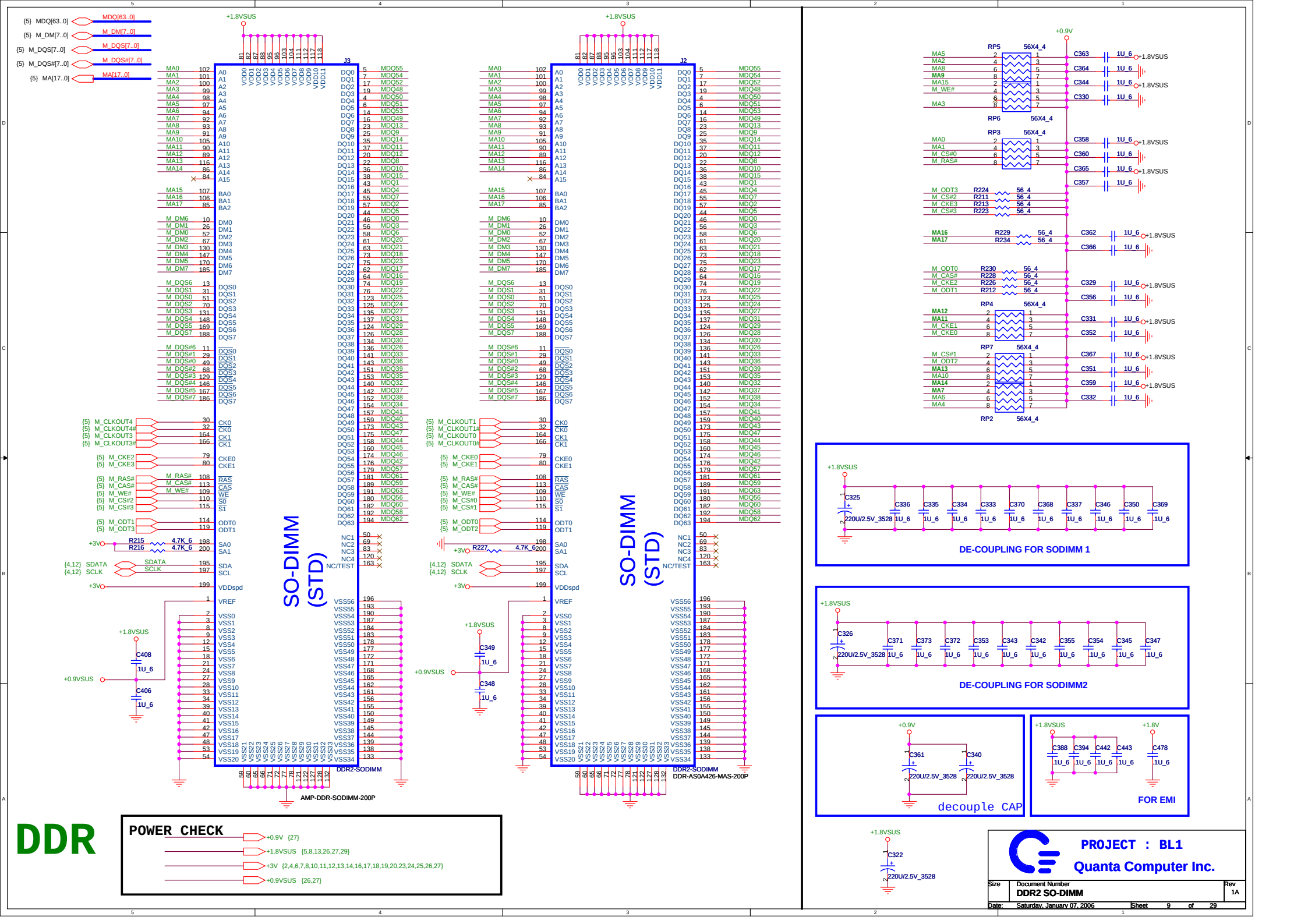
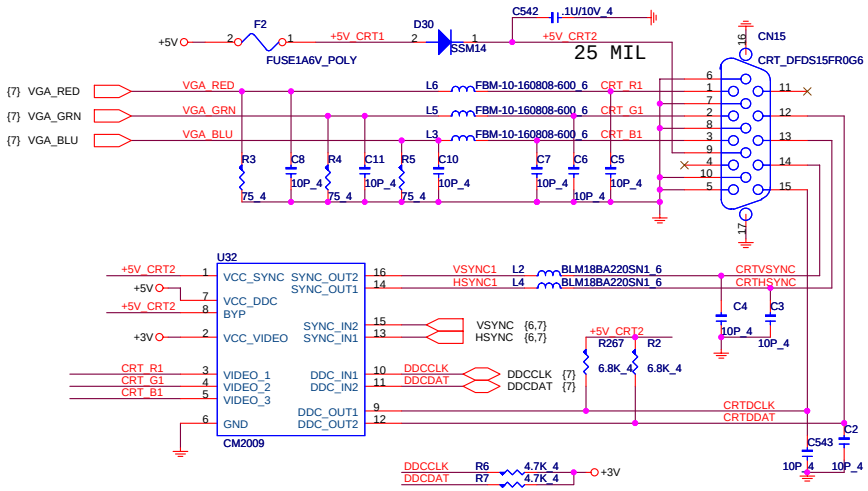
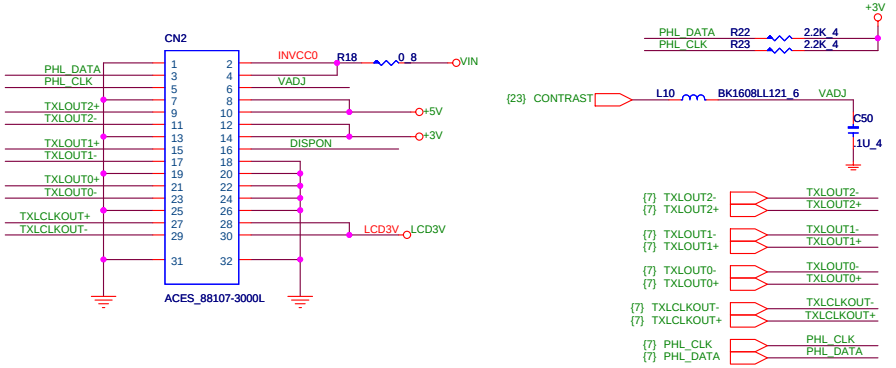
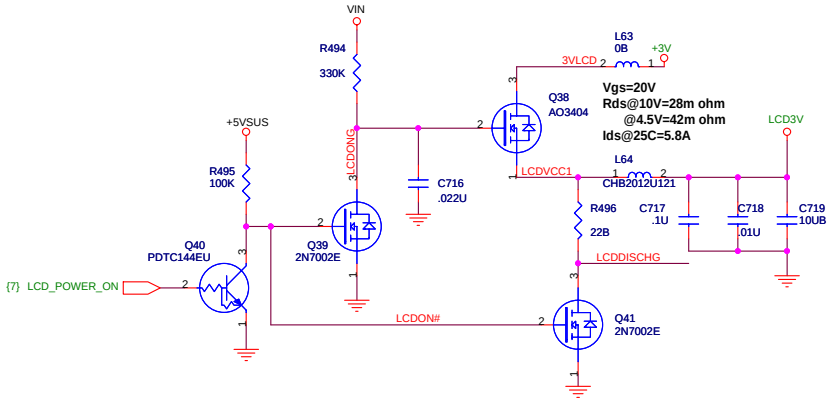

DDR
POWER CHECK
+0.9V {27}
+1.8VSUS {5,8,13,26,27,29}
+3V {2,4,6,7,8,10,11,12,13,14,16,17,18,19,20,23,24,25,26,27}
+0.9VSUS {26,27}
SO-DIMM (STD)
DDR2-SODIMM
AMP-DDR-SODIMM-200P
DDR2-SODIMM
DDR-AS0A426-MAS-200P
DE-COUPLING FOR SODIMM 1
DE-COUPLING FOR SODIMM2
decouple CAP
FOR EMI
PROJECT : BL1
Quanta Computer Inc.
DDR2 SO-DIMM
Saturday, January 07, 2006
Sheet 9 of 29

CRT PORT

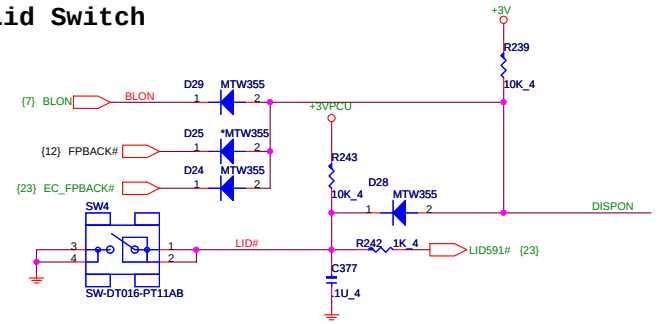


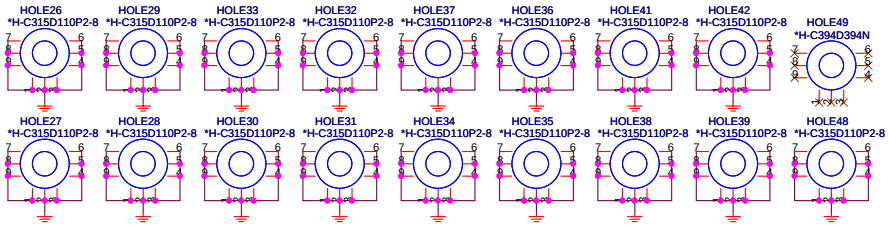
LCD Connector





Lid Switch





MDC(OPTION)

HOLE51
MTG_HOLE

NB SINK

HOLE50
*H-C236D161P2-8

KEYBOARD

HOLE47
*H-C236D161P2-8

CPU

HOLE43 *H-C295D201P2-8
HOLE44 *H-C295D201P2-8
HOLE45 *H-C295D201P2-8
HOLE46 *H-C295D201P2-8

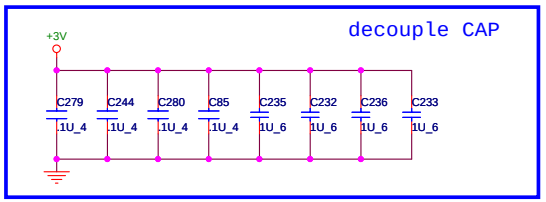
VGA

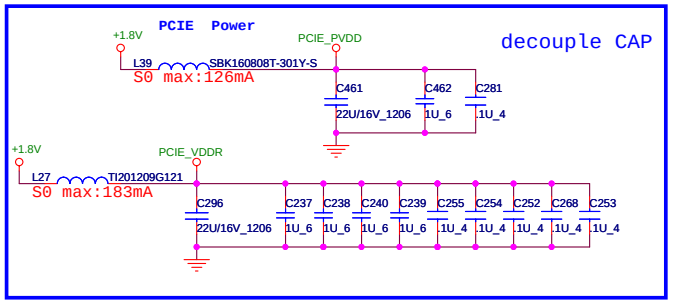
POWER CHECK

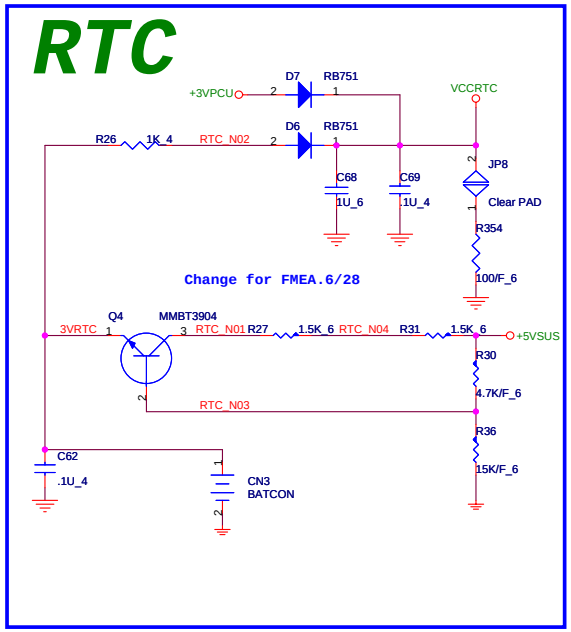
- +5V {13,15,16,17,18,19,20,24,25,26}
- +3V {2,4,6,7,8,9,11,12,13,14,16,17,18,19,20,23,24,25,26,27}
- +3VPCU {11,23,24,26,28}
- VIN {25,26,27,28}

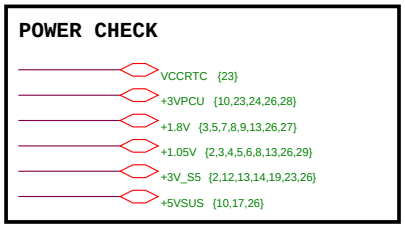
PROJECT : BL1
Quanta Computer Inc.

Size	Document Number	Rev
	VGA Ports, LID, & HOLES	1A
Date: Saturday, January 07, 2006	Sheet 10 of 29	

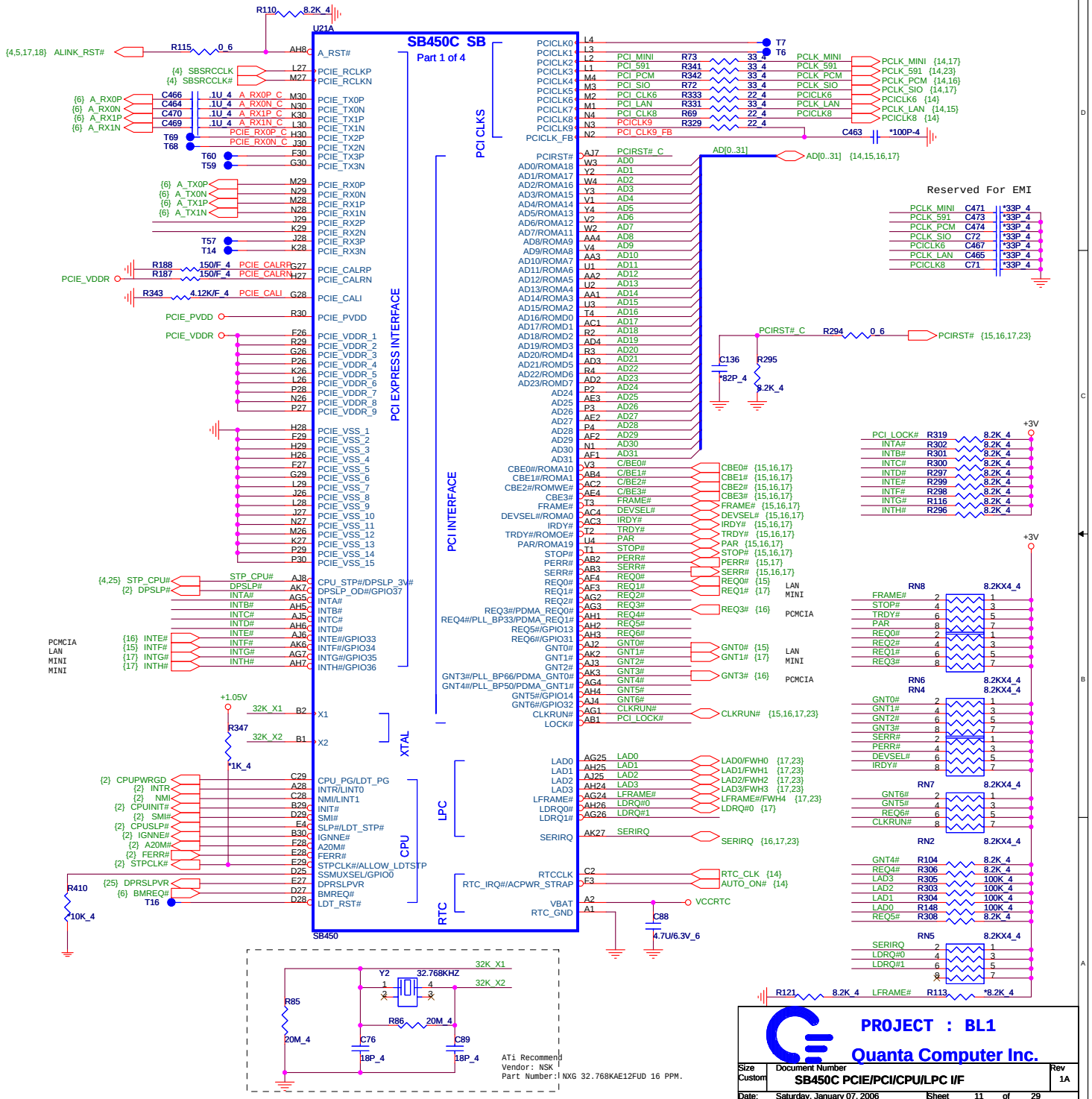








CLG

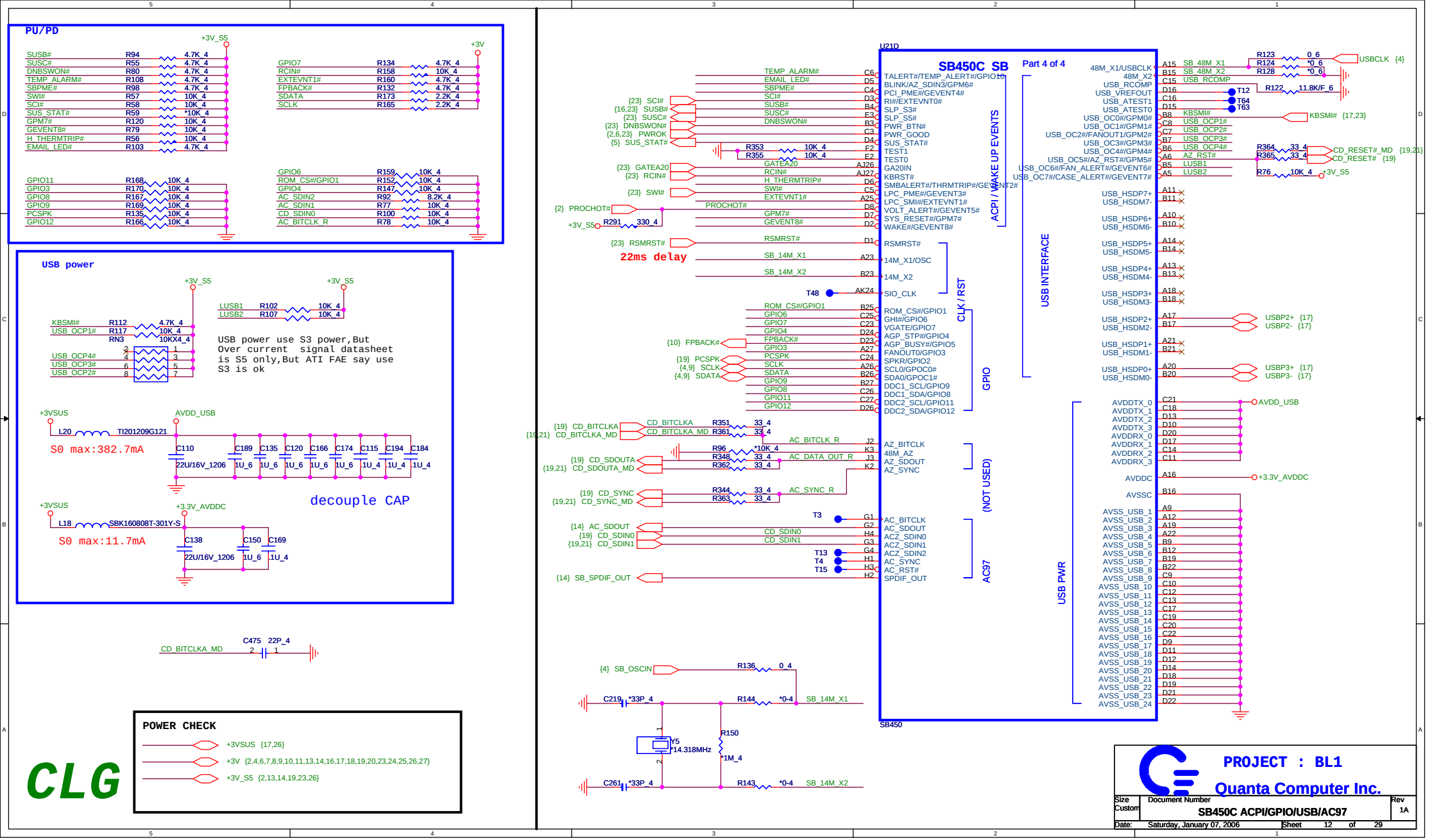


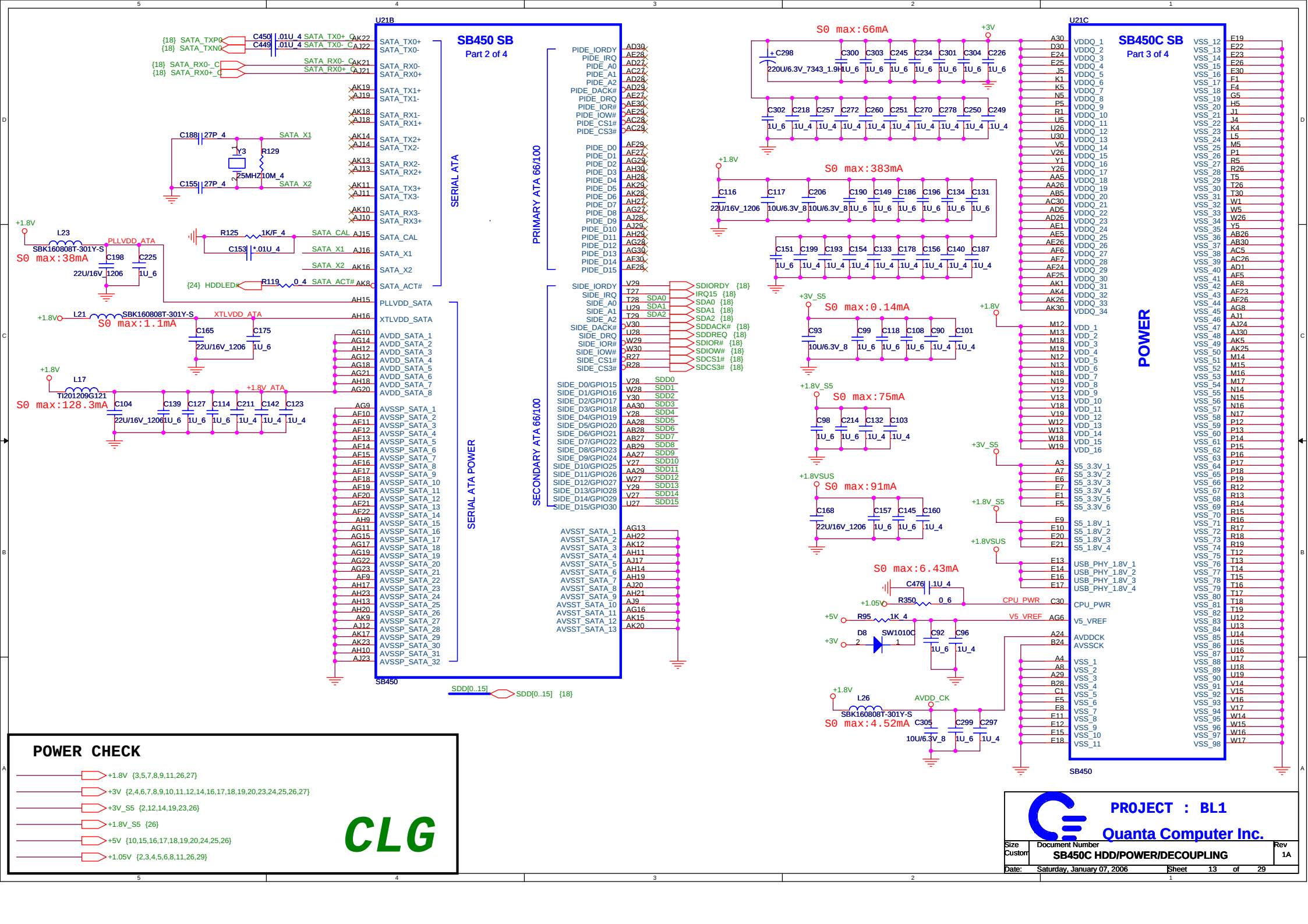
PROJECT : BL1

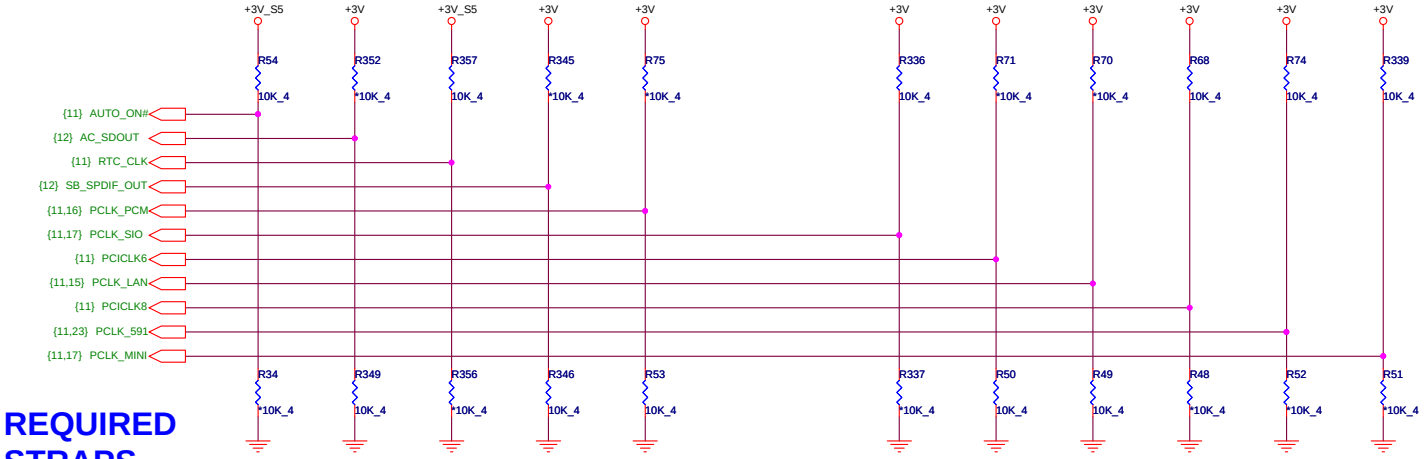
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB450C PCIE/PCI/CPU/LPC I/F	1A

Date: Saturday, January 07, 2006 Sheet 11 of 29


PU/PD
USB power
USB power use S3 power,But
Over current signal datasheet
is S5 only,But ATI FAE say use
S3 is ok
S0 max:382.7mA
S0 max:11.7mA
decouple CAP
POWER CHECK
+3VSUS {17,26}
+3V {2,4,6,7,8,9,10,11,13,14,16,17,18,19,20,23,24,25,26,27}
+3V_S5 {2,13,14,19,23,26}
CLG
SB450C SB
Part 4 of 4
ACPI / WAKE UP EVENTS
CLK / RST
GPIO
AC97
(NOT USED)
USB INTERFACE
USB PWR
22ms delay
SB450
PROJECT : BL1
Quanta Computer Inc.
SB450C ACPI/GPIO/USB/AC97
Saturday, January 07, 2006

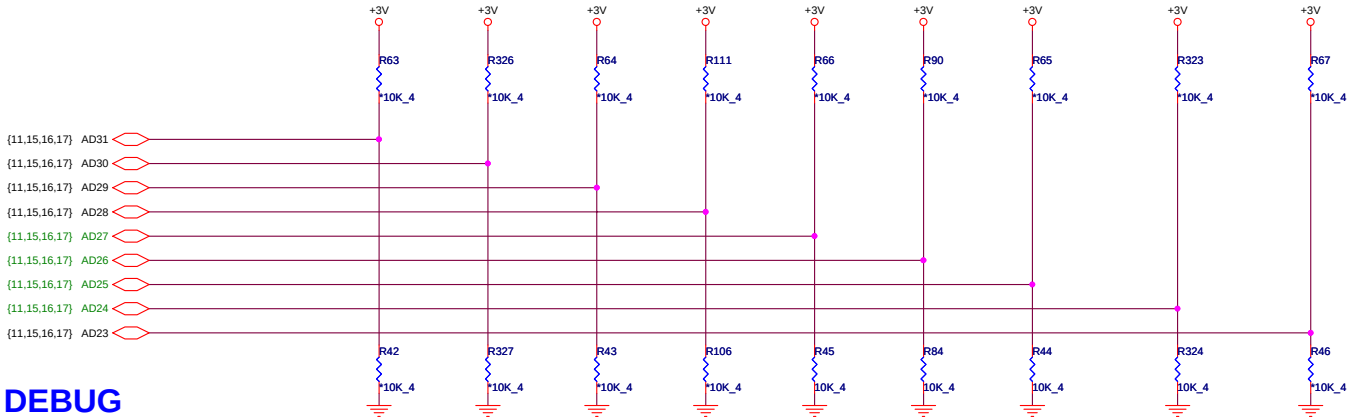

SB450 SB
Part 2 of 4
SERIAL ATA
PRIMARY ATA 66/100
SECONDARY ATA 66/100
SERIAL ATA POWER
SB450
SB450C SB
Part 3 of 4
POWER
SB450
S0 max:38mA
S0 max:1.1mA
S0 max:128.3mA
S0 max:66mA
S0 max:383mA
S0 max:0.14mA
S0 max:75mA
S0 max:91mA
S0 max:6.43mA
S0 max:4.52mA
POWER CHECK
+1.8V {3,5,7,8,9,11,26,27}
+3V {2,4,6,7,8,9,10,11,12,14,16,17,18,19,20,23,24,25,26,27}
+3V_S5 {2,12,14,19,23,26}
+1.8V_S5 {26}
+5V {10,15,16,17,18,19,20,24,25,26}
+1.05V {2,3,4,5,6,8,11,26,29}
CLG
PROJECT : BL1
Quanta Computer Inc.
Size Custom
Document Number SB450C HDD/POWER/DECOUPLING
Rev 1A
Date: Saturday, January 07, 2006
Sheet 13 of 29



REQUIRED STRAPS

	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7	PCI_CLK8	PCI_CLK3	PCI_CLK2
	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCI_CLK6	PCLK_LAN	PCI_CLK8	PCLK_591	PCLK_MINI*
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz use Internal PLL	14MHz OSC MODE DEFAULT	CPU I/F = K8	H,H = PCI(X BUS) ROM H,L = LPC ROM I (LPC addresses are translated to the top of the 4G address space)		USB PHY PWRDOWN DISABLE DEFAULT	48MHz Crystal Pad DEFAULT
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	48MHz use External Clock DEFAULT	14MHz XTAL MODE	CPU I/F = P4 DEFAULT	L,H = LPC ROM II DEFAULT (addresses mapped to below 1M) L,L = FWH ROM		USB PHY PWRDOWN ENABLE	48MHz OSC/Clock Buffer

*This strap is only required if the strap on PCICLK4 is configured for External Clock.



DEBUG STRAPS

	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

POWER CHECK

+3V_S5 {2,12,13,19,23,26}

+3V {2,4,6,7,8,9,10,11,12,13,16,17,18,19,20,23,24,25,26,27}

CLG

PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB450C STRAPS	1A
Date: Saturday, January 07, 2006	Sheet 14 of 29	

ID Select : AD18
Interrupt Pin : INTF#
Request Indicate : REQ0#
Grant Indicate : GNT0#

U16

RTL8110SBL/8100CL

RTL8110SBL

VDD33---+3.3V DIGITAL
AVDDH------+3.3V ANALOG
AVDDL------+2.5V ANALOG
DVDD-----+1.2V DIGITAL
DVDD_A----+1.2V ANALOG

RTL8100CL

VDD33---+3.3V DIGITAL
AVDDL-----+3.3V ANALOG
DVDD-----+2.5V DIGITAL
AVDDH------+2.5V ANALOG

Near Lan chipset

Transform to Daughter Board

U15 93C46-3GR

POWER CHECK

LANVCC {26}

+5V {10,13,16,17,18,19,20,24,25,26}

LAN

decouple CAP

U31 NS681687

CN18 RJ45-C100F8-100B-8P-L

PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	LAN RTL8110SBL/8100CL	1A

Date: Saturday, January 07, 2006 Sheet 15 of 29

ID Select : AD17
Interrupt Pin : INTE#
Request Indicate : REQ3#
Grant Indicate : GNT3#

U33
CB1410

U34
CP2211

Near TPS2211A

Near Slot

CN27
PCMCIA SOCKET
SANTA-1306-68P

+3V Plane

Near Chipset

delay 10ms at least

*DTC144EU

PROJECT : BL1
Quanta Computer Inc.

Size	Document Number	Rev
	PCMCIA(CB1410)	1A
Date: Saturday, January 07, 2006	Sheet 16 of 29	

ID Select : AD20
Interrupt Pin : INTG# , INTH#
Request Indicate : REQ1#
Grant Indicate : GNT1#

MINI-PCI

CN12
FOX_MINIPCI_H7.95

D26 MTW355

RP8 *0X4_4

R251 R252 *0-4 RLRESET#

R247 150_4 AD20

R248 R250 *0-4

R253 *0-4

R245 R254 *22_4

C379 C385 *10P_4

R249 *4.7K_4

R246 4.7K_4

C383 C382 C381 C380 C378 C384 1U_4

decouple CAP

USB

U22
G545B2RD1U

U23
G545B2RD1U

R340 R358 *6.34K/F_6

CN17
USB_DFHD04MR671

L51
RFCM1632100M3

C468 C486 100U/6.3V-3528

CN4
SPK

POWER CHECK

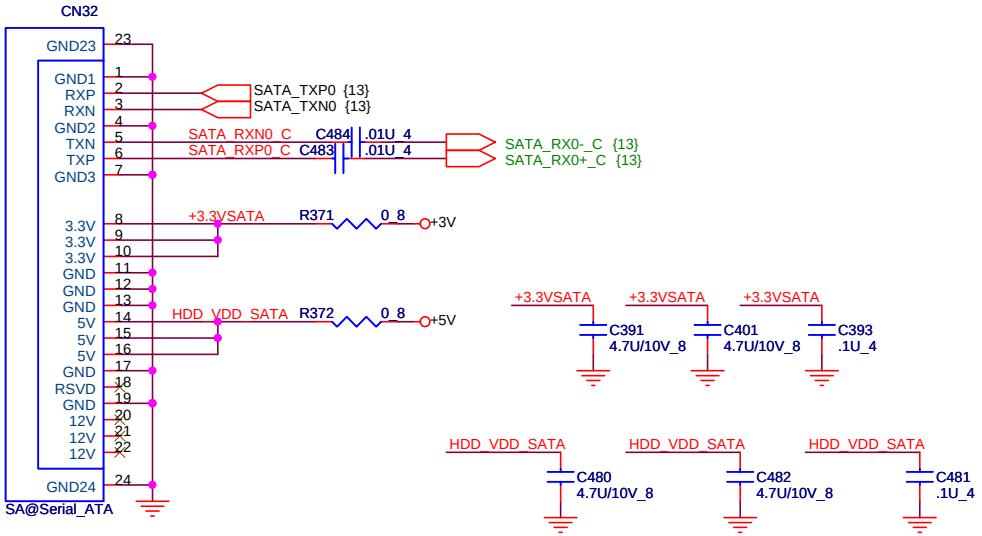
+3V {2,4,6,7,8,9,10,11,12,13,14,16,18,19,20,23,24,25,26,27}
+5VSUS {10,11,26}
+3VSUS {12,26}
+5V {10,13,15,16,18,19,20,24,25,26}

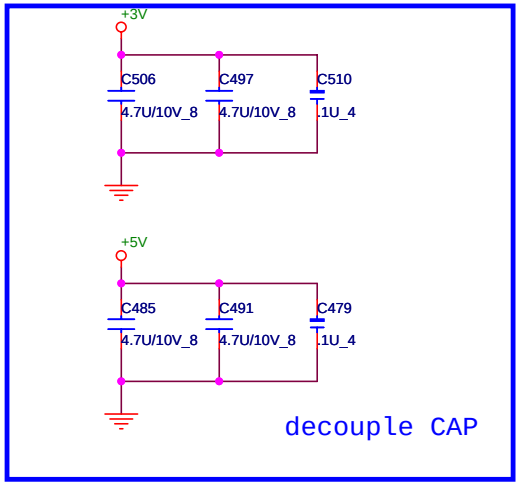
MPC

PROJECT : BL1
Quanta Computer Inc.

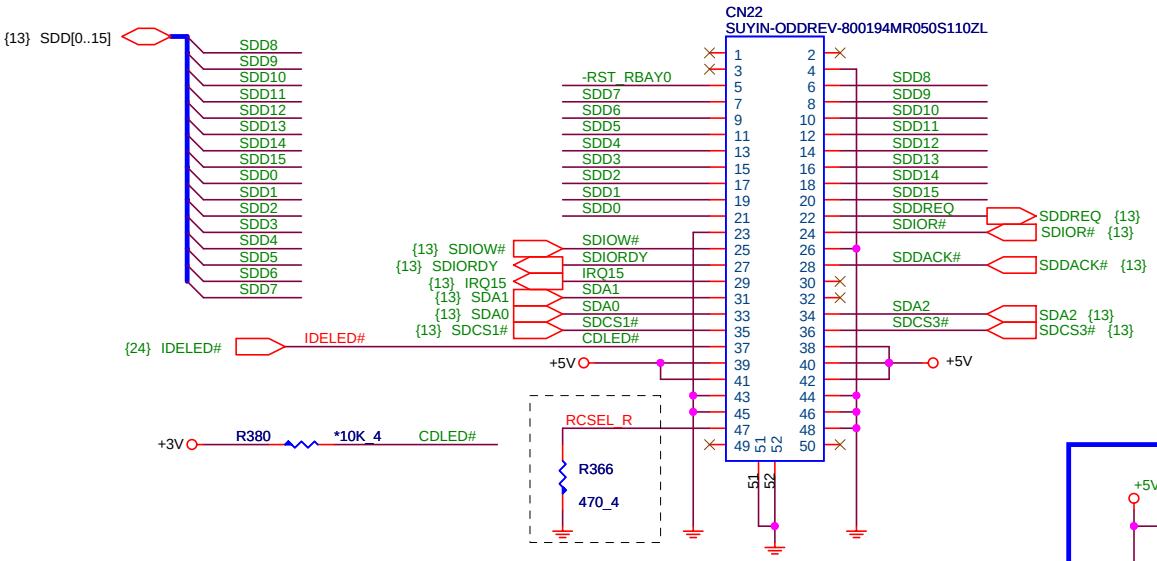
Size	Document Number	Rev
	MINI PCI,USB	1A
Date: Saturday, January 07, 2006	Sheet 17 of 29	

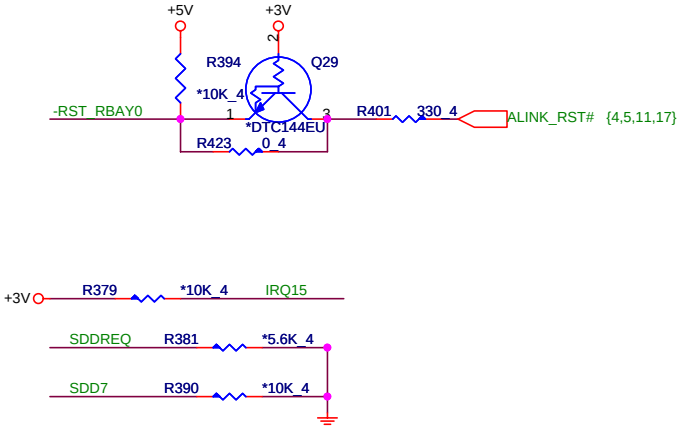
SATA HDD CONN

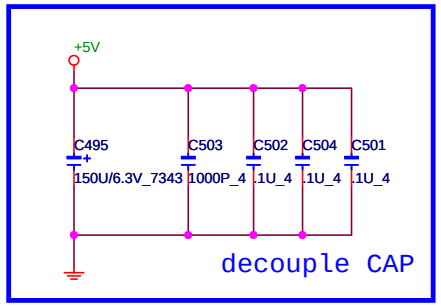




ODD CONN







POWER CHECK

+5V {10,13,15,16,17,19,20,24,25,26}

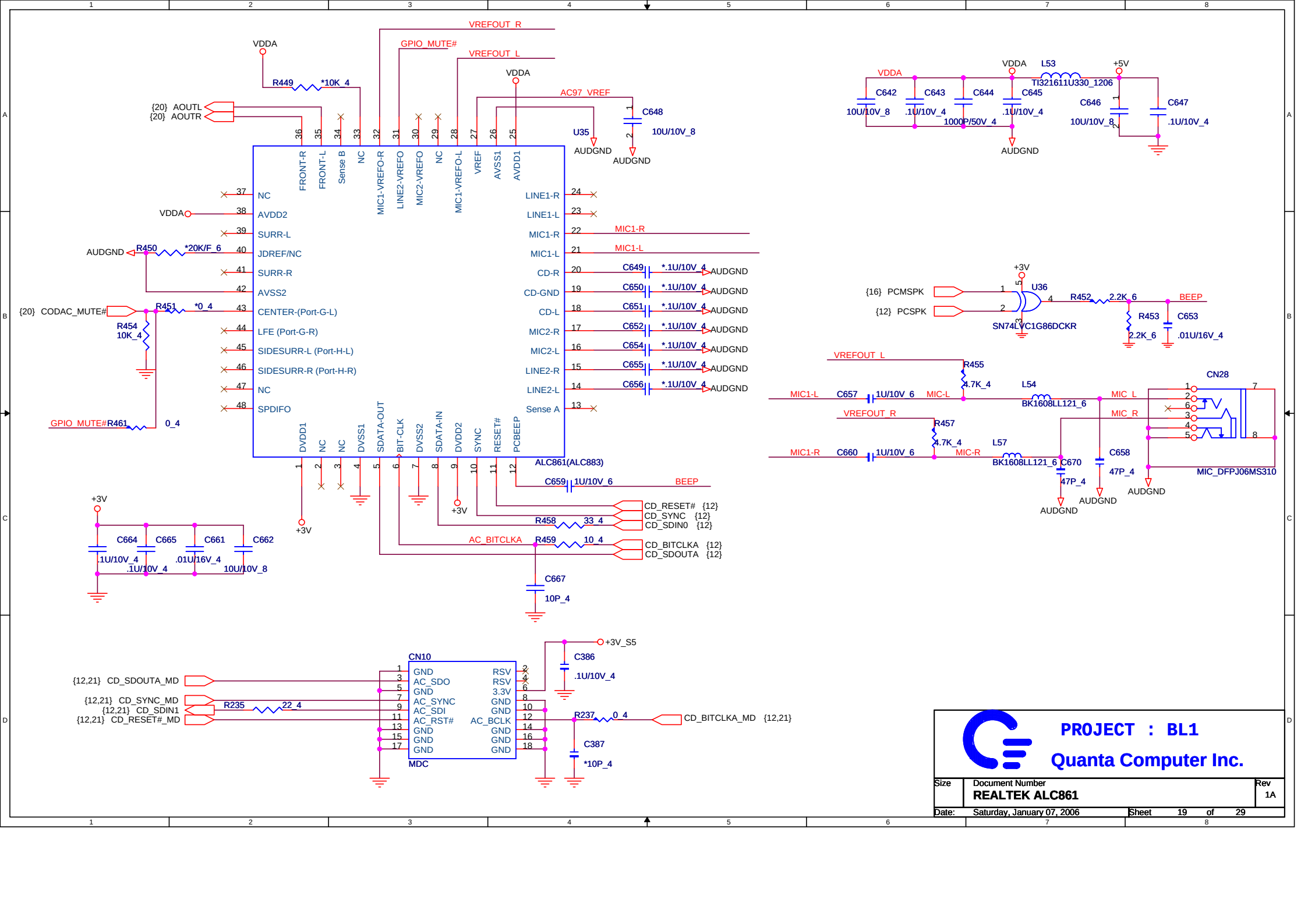
+3V {2,4,6,7,8,9,10,11,12,13,14,16,17,19,20,23,24,25,26,27}

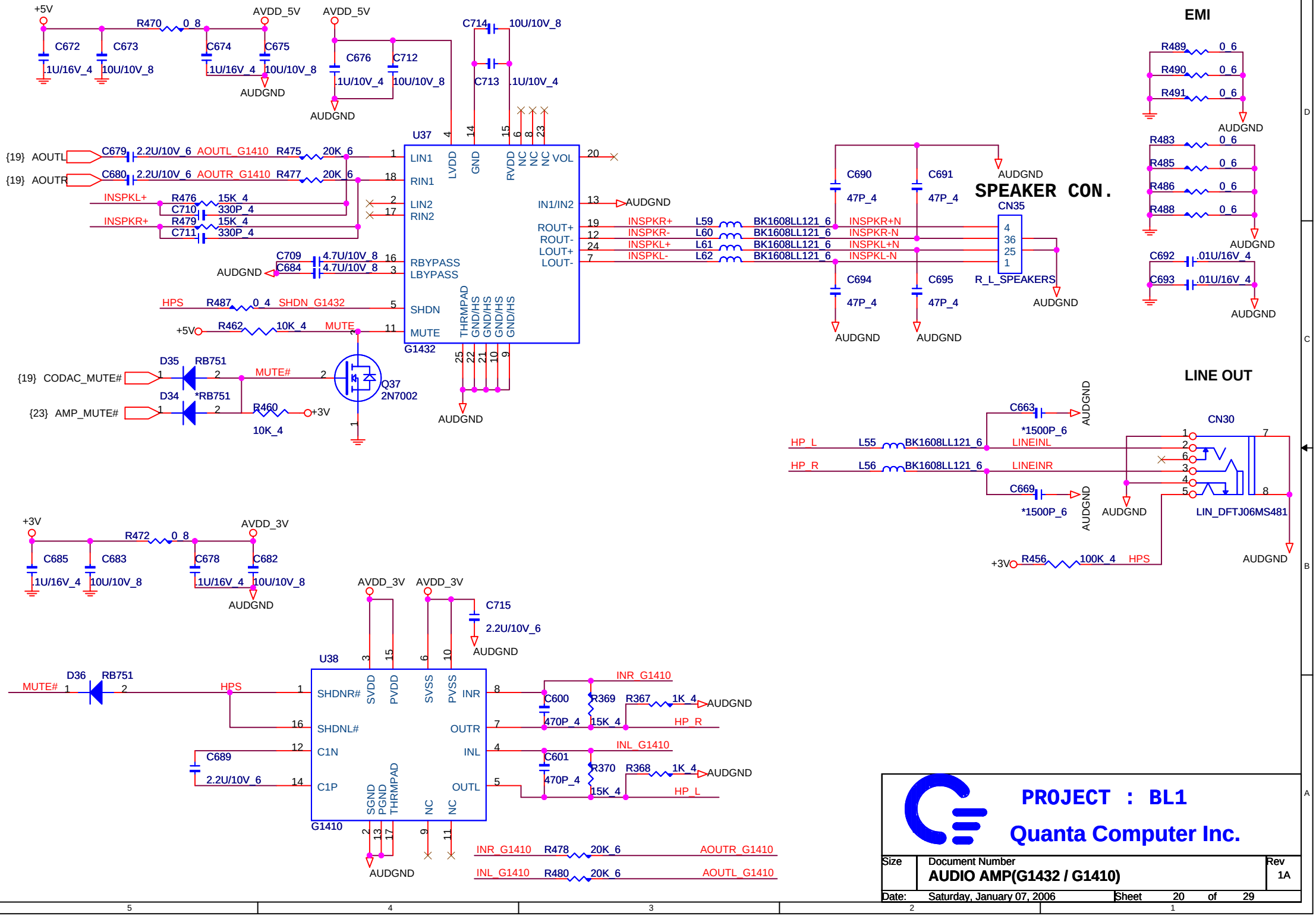
IDE

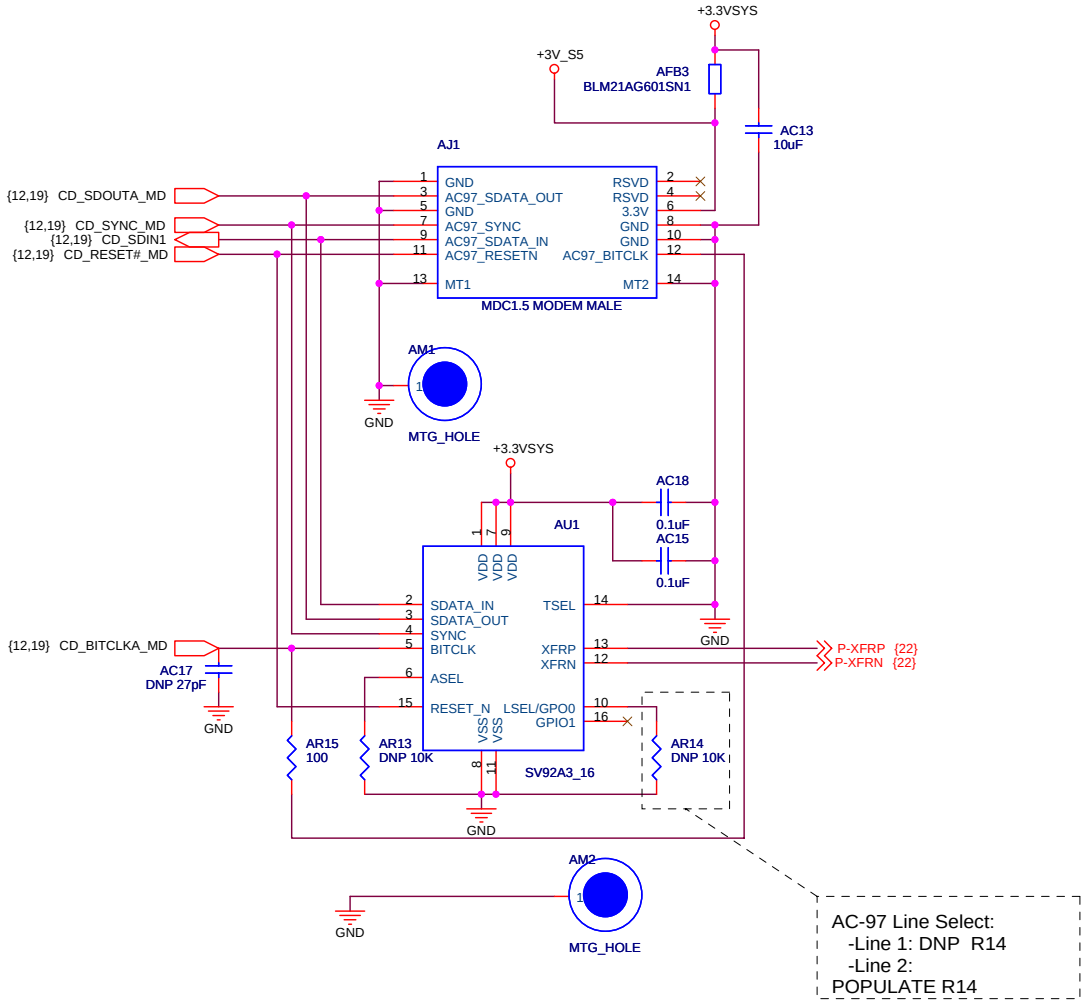
PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	HDD & CDROM	1A
Date: Saturday, January 07, 2006	Sheet 18 of 29	


VDDA
VREFOUT_R
GPIO_MUTE#
VREFOUT_L
AC97_VREF
R449 *10K_4
{20} AOUTL
{20} AOUTR
C648 10U/10V_8
U35
AUDGND
FRONT-R
FRONT-L
Sense B
NC
MIC1-VREFO-R
LINE2-VREFO
MIC2-VREFO
NC
MIC1-VREFO-L
VREF
AVSS1
AVDD1
NC
AVDD2
SURR-L
JDREF/NC
SURR-R
AVSS2
CENTER-(Port-G-L)
LFE (Port-G-R)
SIDESURR-L (Port-H-L)
SIDESURR-R (Port-H-R)
NC
SPDIFO
LINE1-R
LINE1-L
MIC1-R
MIC1-L
CD-R
CD-GND
CD-L
MIC2-R
MIC2-L
LINE2-R
LINE2-L
Sense A
MIC1-R
MIC1-L
R450 *20K/F_6
R451 *0_4
R454 10K_4
{20} CODAC_MUTE#
GPIO_MUTE# R461 0_4
C649 *.1U/10V_4
C650 *.1U/10V_4
C651 *.1U/10V_4
C652 *.1U/10V_4
C654 *.1U/10V_4
C655 *.1U/10V_4
C656 *.1U/10V_4
DVDD1
NC
NC
DVSS1
SDATA-OUT
BIT-CLK
DVSS2
SDATA-IN
DVDD2
SYNC
RESET#
PCBEEP
ALC861(ALC883)
C659 1U/10V_6
BEEP
CD_RESET# {12}
CD_SYNC {12}
CD_SDIN0 {12}
R458 33_4
AC_BITCLKA
R459 10_4
CD_BITCLKA {12}
CD_SDOUTA {12}
C667 10P_4
+3V
C664 .1U/10V_4
C665 .1U/10V_4
C661 .01U/16V_4
C662 10U/10V_8
VDDA
L53 TI321611U330_1206
+5V
C642 10U/10V_8
C643 .1U/10V_4
C644 1000P/50V_4
C645 .1U/10V_4
C646 10U/10V_8
C647 .1U/10V_4
AUDGND
+3V
U36
SN74LVC1G86DCKR
{16} PCMSPK
{12} PCSPK
R452 2.2K_6
R453 2.2K_6
C653 .01U/16V_4
BEEP
VREFOUT_L
VREFOUT_R
R455 4.7K_4
R457 4.7K_4
MIC1-L
MIC1-R
C657 1U/10V_6
C660 1U/10V_6
MIC-L
MIC-R
L54 BK1608LL121_6
L57 BK1608LL121_6
MIC_L
MIC_R
C670 47P_4
C658 47P_4
CN28
MIC_DFPJ06MS310
AUDGND
CN10
GND
AC_SDO
GND
AC_SYNC
AC_SDI
AC_RST#
GND
GND
GND
RSV
RSV
3.3V
GND
GND
AC_BCLK
GND
GND
GND
MDC
{12,21} CD_SDOUTA_MD
{12,21} CD_SYNC_MD
{12,21} CD_SDIN1
{12,21} CD_RESET#_MD
R235 22_4
+3V_S5
C386 .1U/10V_4
R237 0_4
CD_BITCLKA_MD {12,21}
C387 *10P_4
PROJECT : BL1
Quanta Computer Inc.
Size
Document Number
REALTEK ALC861
Rev
1A
Date: Saturday, January 07, 2006
Sheet 19 of 29


+5V
R470 0_8
AVDD_5V
C672
C673
C674
C675
1U/16V_4
10U/10V_8
AUDGND
C676
C712
C714 10U/10V_8
C713 1U/10V_4
U37
LIN1
RIN1
LIN2
RIN2
LVDD
GND
RVDD
NC
VOL
IN1/IN2
ROUT+
ROUT-
LOUT+
LOUT-
RBYPASS
LBYPASS
SHDN
MUTE
THRMPAD
G1432
{19} AOUTL
{19} AOUTR
C679 2.2U/10V_6 AOUTL_G1410 R475 20K_6
C680 2.2U/10V_6 AOUTR_G1410 R477 20K_6
INSPKL+
INSPKR+
R476 15K_4
C710 330P_4
R479 15K_4
C711 330P_4
C709 4.7U/10V_8
C684 4.7U/10V_8
HPS
R487 0_4 SHDN_G1432
+5V
R462 10K_4 MUTE
{19} CODAC_MUTE#
{23} AMP_MUTE#
D35 RB751
D34 *RB751
MUTE#
Q37
2N7002
R460 10K_4
+3V
INSPKR+ L59 BK1608LL121_6 INSPKR+N
INSPKR- L60 BK1608LL121_6 INSPKR-N
INSPKL+ L61 BK1608LL121_6 INSPKL+N
INSPKL- L62 BK1608LL121_6 INSPKL-N
C690 47P_4
C691 47P_4
C694 47P_4
C695 47P_4
SPEAKER CON.
CN35
R_L_SPEAKERS
EMI
R489 0_6
R490 0_6
R491 0_6
R483 0_6
R485 0_6
R486 0_6
R488 0_6
C692 .01U/16V_4
C693 .01U/16V_4
LINE OUT
C663 *1500P_6
C669 *1500P_6
HP_L
HP_R
L55 BK1608LL121_6
L56 BK1608LL121_6
LINEINL
LINEINR
CN30
LIN_DFTJ06MS481
R456 100K_4 HPS
+3V
R472 0_8
AVDD_3V
C685
C683
C678
C682
C715 2.2U/10V_6
U38
SHDNR#
SHDNL#
C1N
C1P
SVDD
PVDD
SVSS
PVSS
INR
OUTR
INL
OUTL
SGND
PGND
THRMPAD
NC
G1410
D36 RB751
C689 2.2U/10V_6
C600 470P_4
C601 470P_4
R369 15K_4
R370 15K_4
R367 1K_4
R368 1K_4
INR_G1410
INL_G1410
HP_R
HP_L
R478 20K_6 AOUTR_G1410
R480 20K_6 AOUTL_G1410
PROJECT : BL1
Quanta Computer Inc.
Size
Document Number
AUDIO AMP(G1432 / G1410)
Rev
1A
Date: Saturday, January 07, 2006
Sheet 20 of 29



Pb

Agere Systems Proprietary
DRAFT COPY - FOR REVIEW ONLY
SUBJECT TO CHANGE

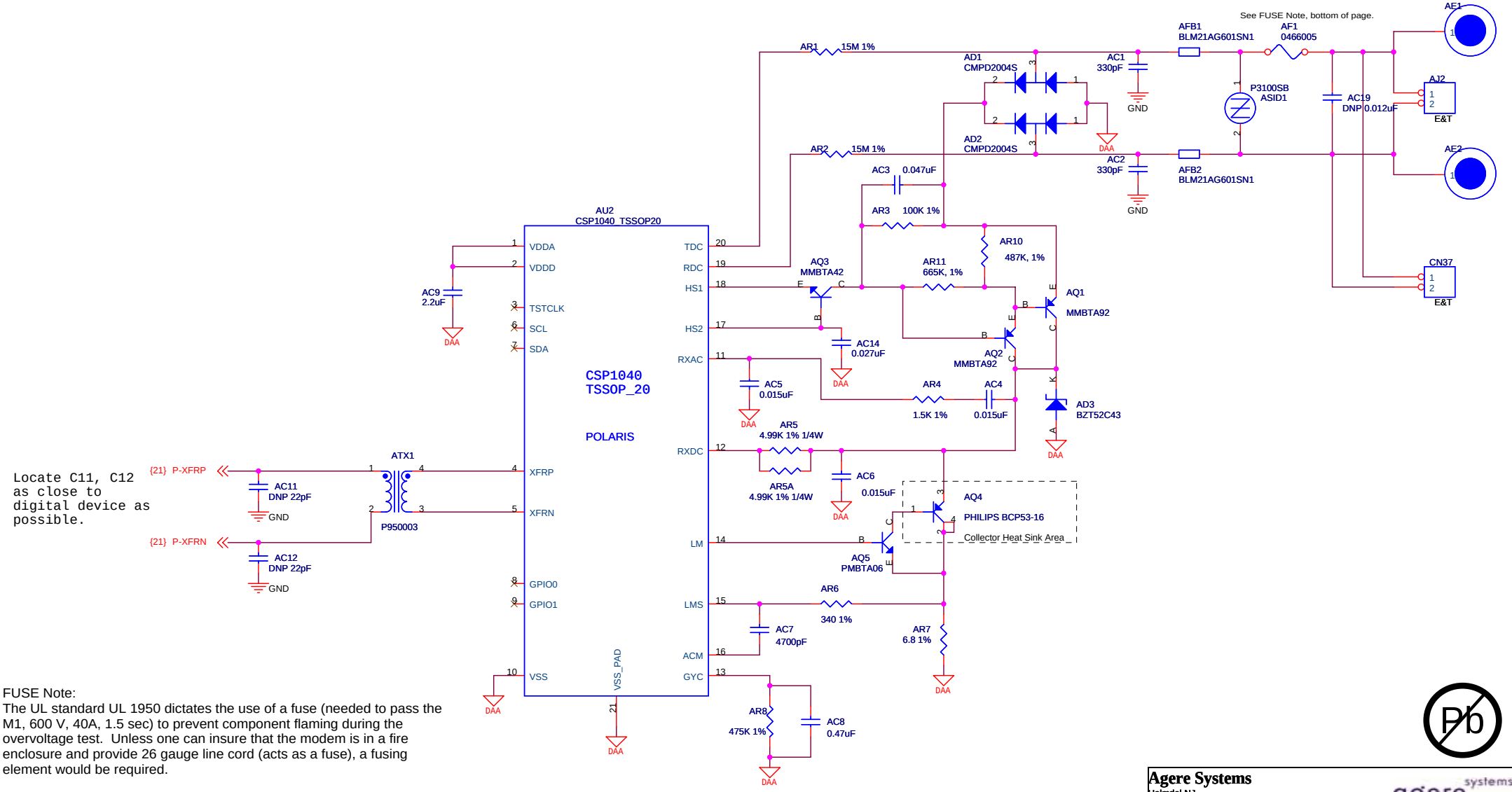
Agere Systems
Holmdel NJ

Design Engineer: C. Russo

Title
DELPHI SV92A3 MDC 1.5 Reference Design

Size	Document Number	Rev
B	**DIGITAL INTERFACE**	AM3

Date: Saturday, January 07, 2006 Sheet 21 of 29



FUSE Note:
The UL standard UL 1950 dictates the use of a fuse (needed to pass the M1, 600 V, 40A, 1.5 sec) to prevent component flaming during the overvoltage test. Unless one can insure that the modem is in a fire enclosure and provide 26 gauge line cord (acts as a fuse), a fusing element would be required.

Alternatively, if a TNV-1 flame resistant material is used, either as a wrap or cover over the DAA portion of the modem, this could satisfy both overvoltage protection and the separation requirement also contained in UL 1950. This latter requirement provides isolation such that unearthed parts of the DAA cannot be touched by a test finger or test probe.

Pb

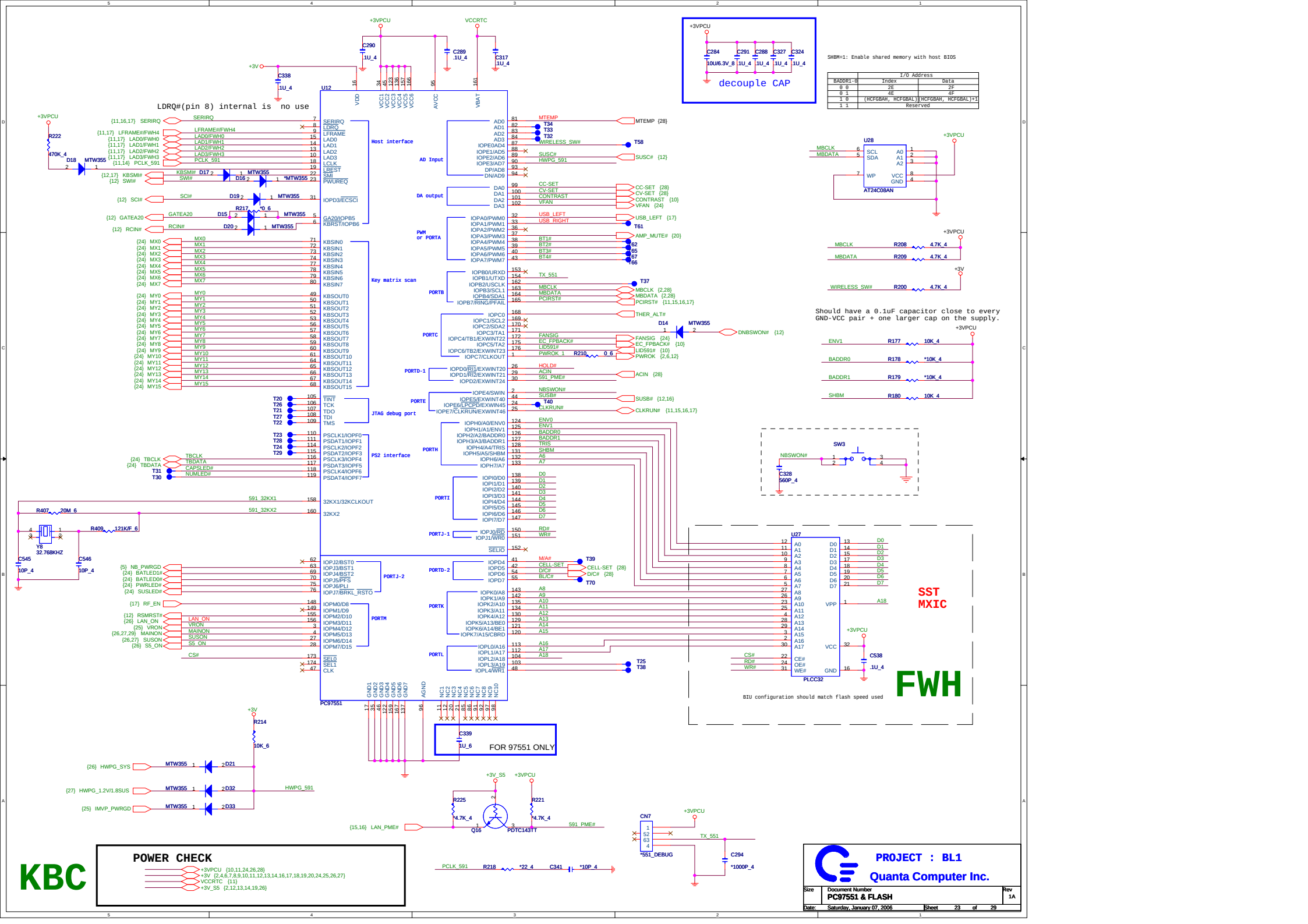
Agere Systems
Holmdel NJ
agere systems

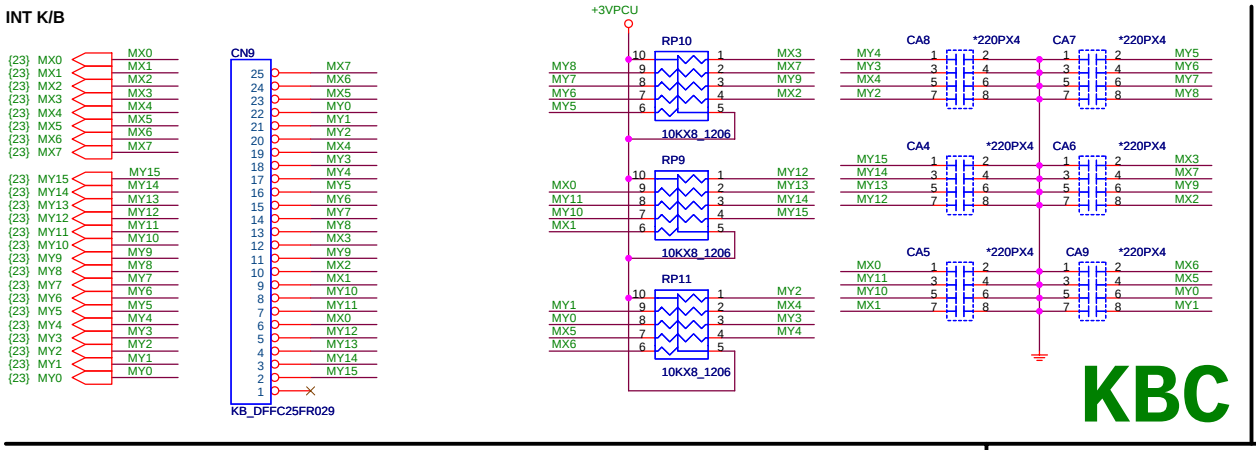
Design Engineer: R. Trevino

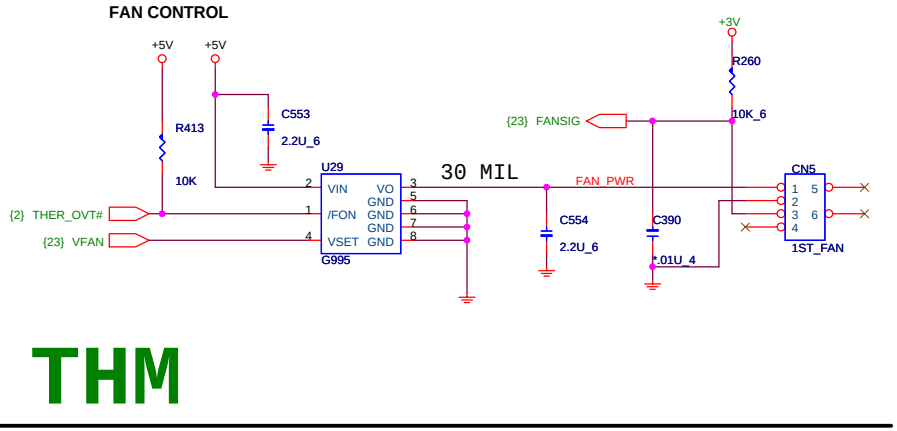
Title
DELPHI SV92A3 MDC 1.5 Reference Design

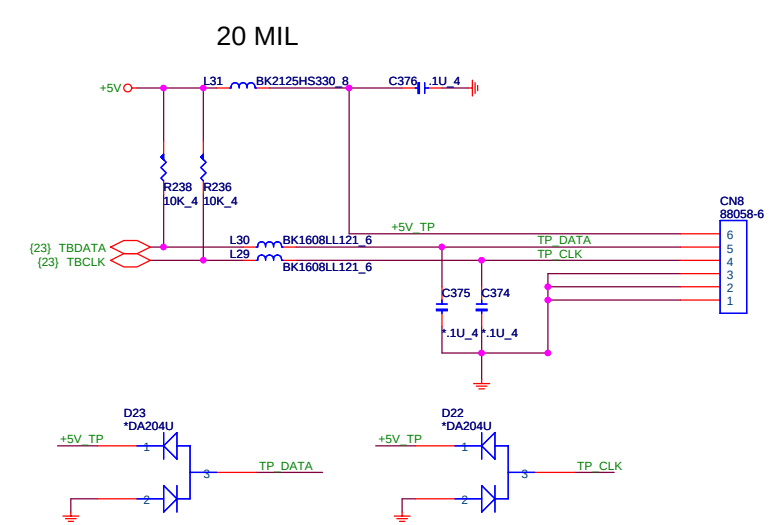
Size	Document Number	Rev
B	**CSP1040 DAA**	AM3

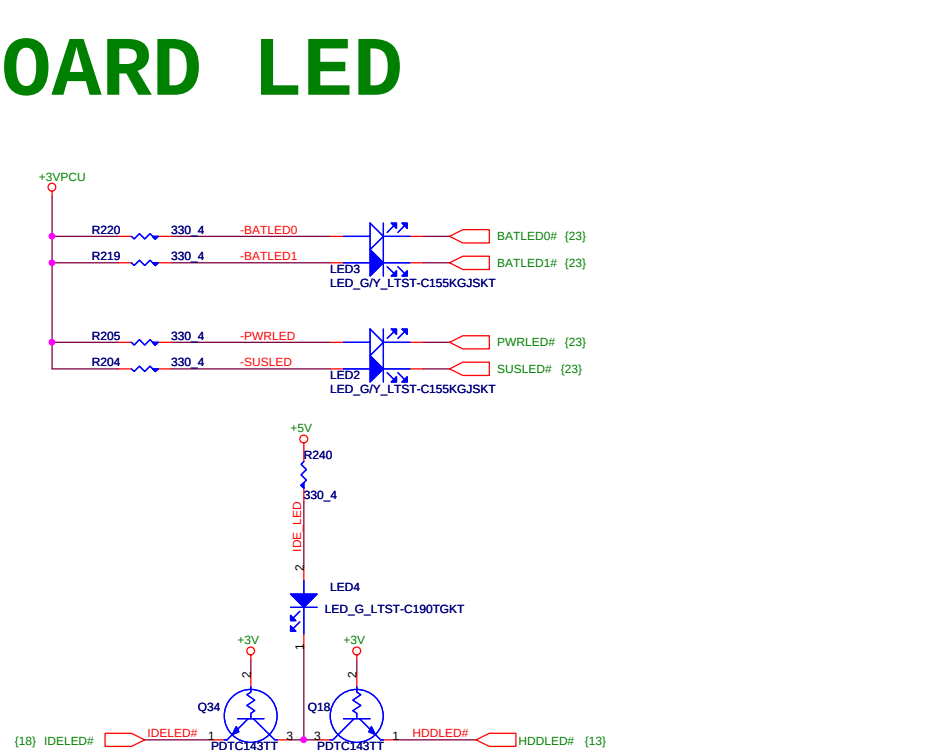
Date: Saturday, January 07, 2006 Sheet 22 of 29

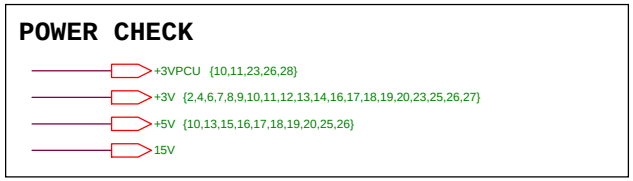

LDRQ#(pin 8) internal is no use
U12
PC97551
Host interface
Key matrix scan
JTAG debug port
PS2 interface
PWM or PORTA
PORTB
PORTC
PORTD-1
PORTE
PORTH
PORTI
PORTJ-1
PORTJ-2
PORTD-2
PORTK
PORTL
PORTM
AD Input
DA output
SELIO
32KX1/32KCLKOUT
32KX2
SERIRQ
LFRAME
LAD0
LAD1
LAD2
LAD3
LCLK
LRESET
SMI
PWUREQ
IOPD3/ECSCI
GA20/IOPB5
KBRST/IOPB6
TINT
TCK
TDO
TDI
TMS
PSCLK1/IOPF0
PSDAT1/IOPF1
PSCLK2/IOPF2
PSDAT2/IOPF3
PSCLK3/IOPF4
PSDAT3/IOPF5
PSCLK4/IOPF6
PSDAT4/IOPF7
MTEMP
WIRELESS_SW#
SUSC#
HWPG_591
CC-SET
CV-SET
CONTRAST
VFAN
USB_LEFT
USB_RIGHT
AMP_MUTE#
BT1#
BT2#
BT3#
BT4#
TX_551
MBCLK
MBDATA
PCIRST#
THER_ALT#
DNBSWON#
FANSIG
EC_FPBACK#
LID591#
PWROK
HOLD#
ACIN
591_PME#
NBSWON#
SUSB#
CLKRUN#
ENV0
ENV1
BADDR0
BADDR1
TRIS
SHBM
M/A#
CELL-SET
D/C#
BLC#
RD#
WR#
SELO
SEL1
CLK
CS#
LAN_ON
VRON
MAINON
SUSON
S5_ON
RF_EN
NB_PWRGD
BATLED1#
BATLED0#
PWRLED#
SUSLED#
RSMRST#
LAN_PME#
HWPG_SYS
HWPG_1.2V/1.8SUS
IMVP_PWRGD
PCLK_591
SERIRQ
LFRAME#/FWH4
LAD0/FWH0
LAD1/FWH1
LAD2/FWH2
LAD3/FWH3
PCLK_591
KBSMI#
SWI#
SCI#
GATEA20
RCIN#
MX0
MX1
MX2
MX3
MX4
MX5
MX6
MX7
MY0
MY1
MY2
MY3
MY4
MY5
MY6
MY7
MY8
MY9
MY10
MY11
MY12
MY13
MY14
MY15
TBCLK
TBDATA
CAPSLED#
NUMLED#
591_32KX1
591_32KX2
+3VPCU
+3V
VCCRTC
+3V_S5
FOR 97551 ONLY
decouple CAP
SHBM=1: Enable shared memory with host BIOS
I/O Address
BADDR1-0
Index
Data
(HCFGBAH, HCFGBAL)
(HCFGBAH, HCFGBAL)+1
Reserved
U28
AT24C08AN
SCL
SDA
WP
Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.
SW3
U27
PLCC32
SST
MXIC
FWH
BIU configuration should match flash speed used
CN7
*551_DEBUG
POWER CHECK
+3VPCU {10,11,24,26,28}
+3V {2,4,6,7,8,9,10,11,12,13,14,16,17,18,19,20,24,25,26,27}
VCCRTC {11}
+3V_S5 {2,12,13,14,19,26}
KBC
PROJECT : BL1
Quanta Computer Inc.
PC97551 & FLASH
Rev 1A
Saturday, January 07, 2006
Sheet 23 of 29











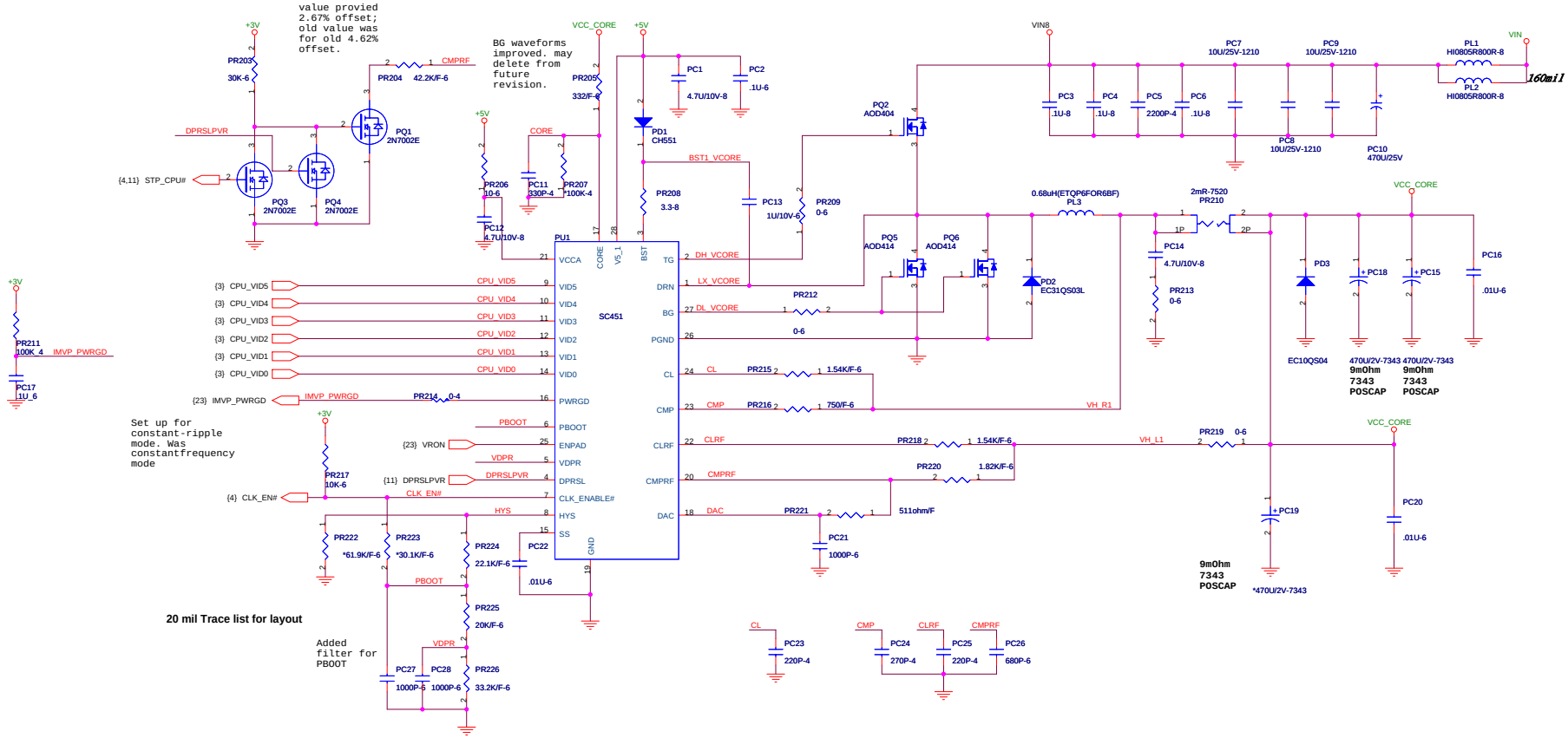
TPD

PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	T/P,FAN,SWITCH,LED,K/B	1A

Date: Saturday, January 07, 2006 Sheet 24 of 29



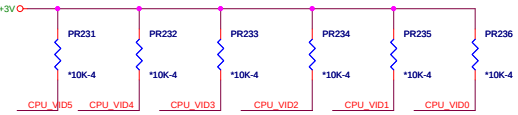
V I D						Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940

100 mil Trace list for layout

DH_VCORE
LX_VCORE
DL_VCORE
DH_VCORE2
LX_VCORE2
DL_VCORE2

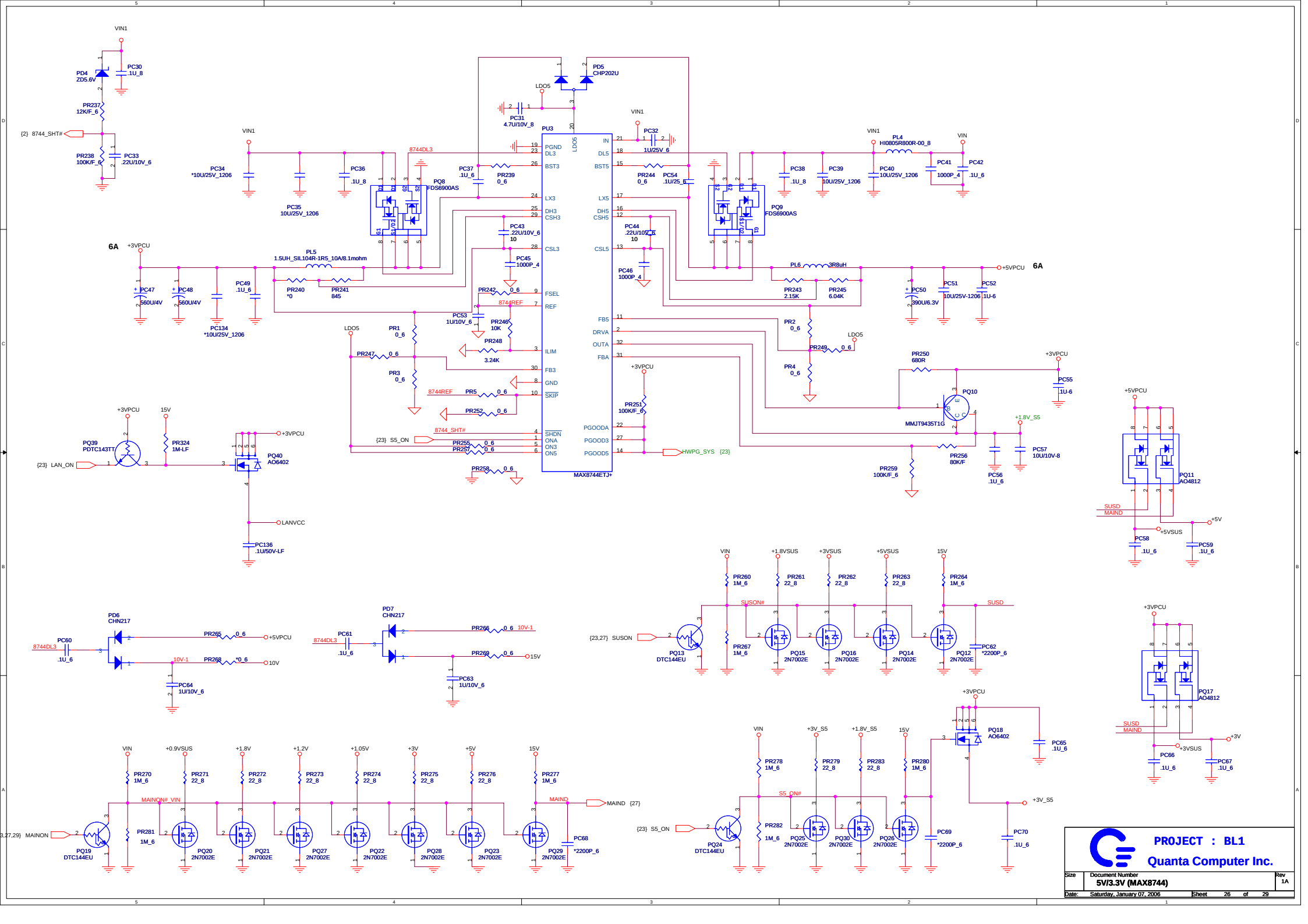
10 mil Trace list for layout

SC1476
pin 4 pin
5 pin 7
pin 25
pin 30



PROJECT : BL1
Quanta Computer Inc.

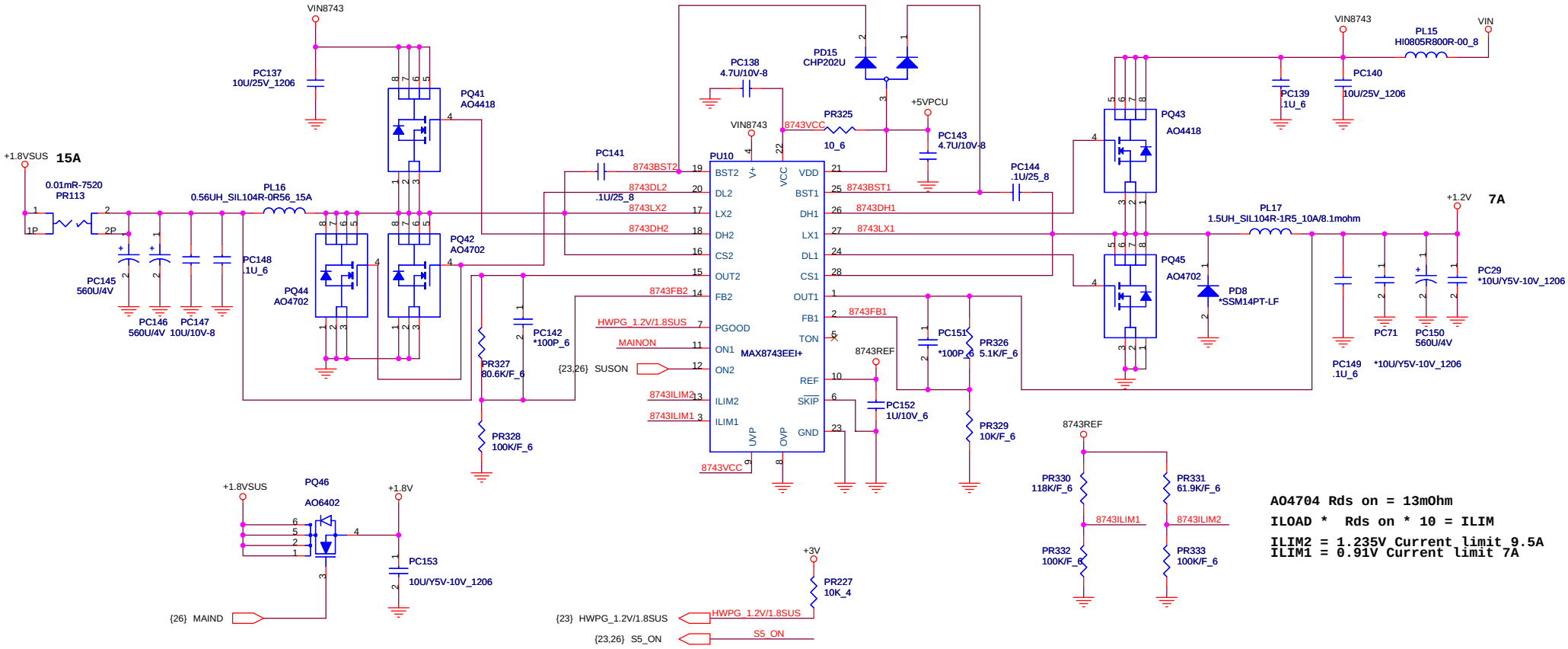
Size	Document Number	Rev
	SC451(VCORE)	1A
Date: Saturday, January 07, 2006	Sheet 25 of 29	



PROJECT : BL1

Quanta Computer Inc.

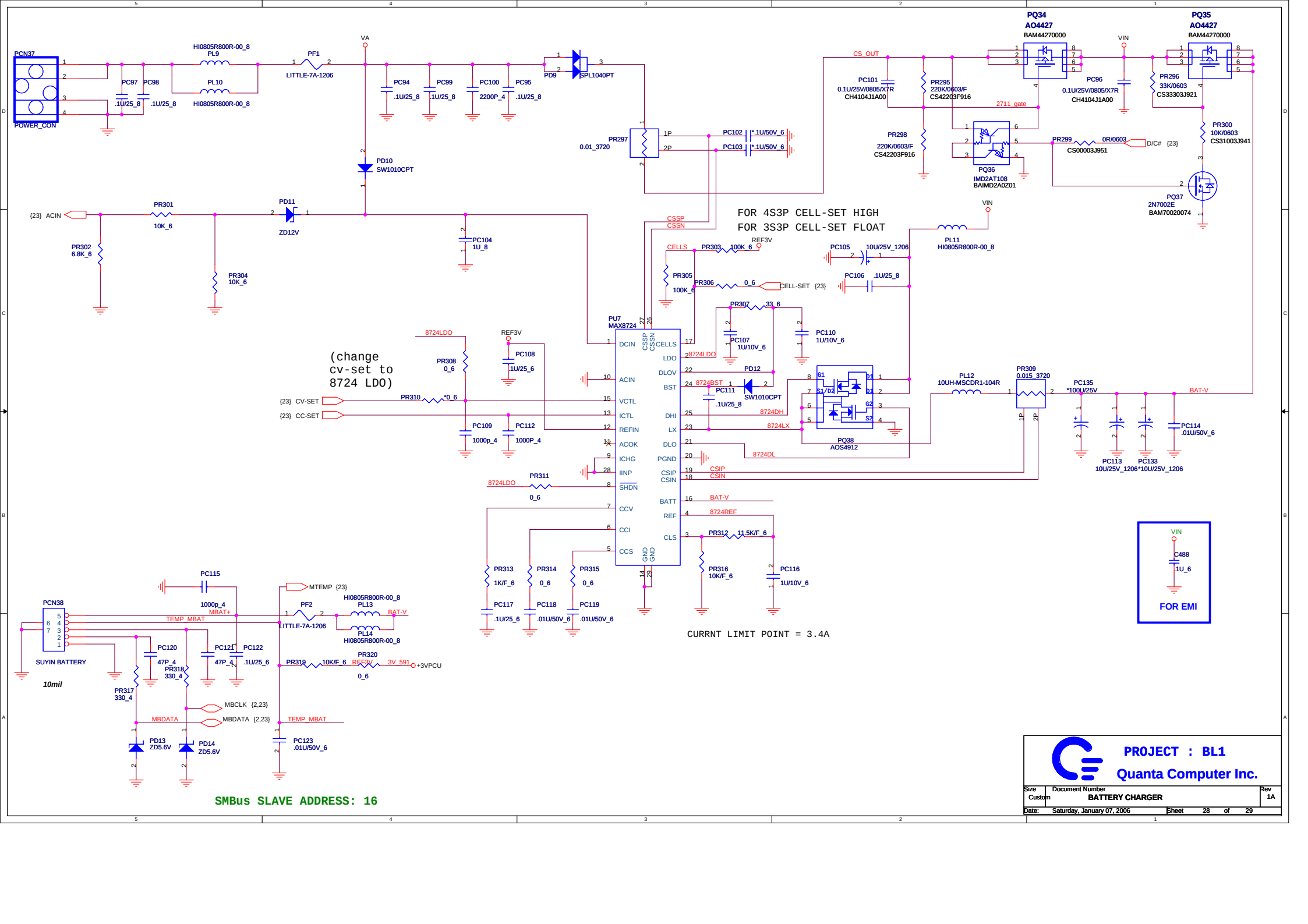
Size	Document Number	Rev
	5V/3.3V (MAX8744)	1A
Date: Saturday, January 07, 2006	Sheet 26 of 29	

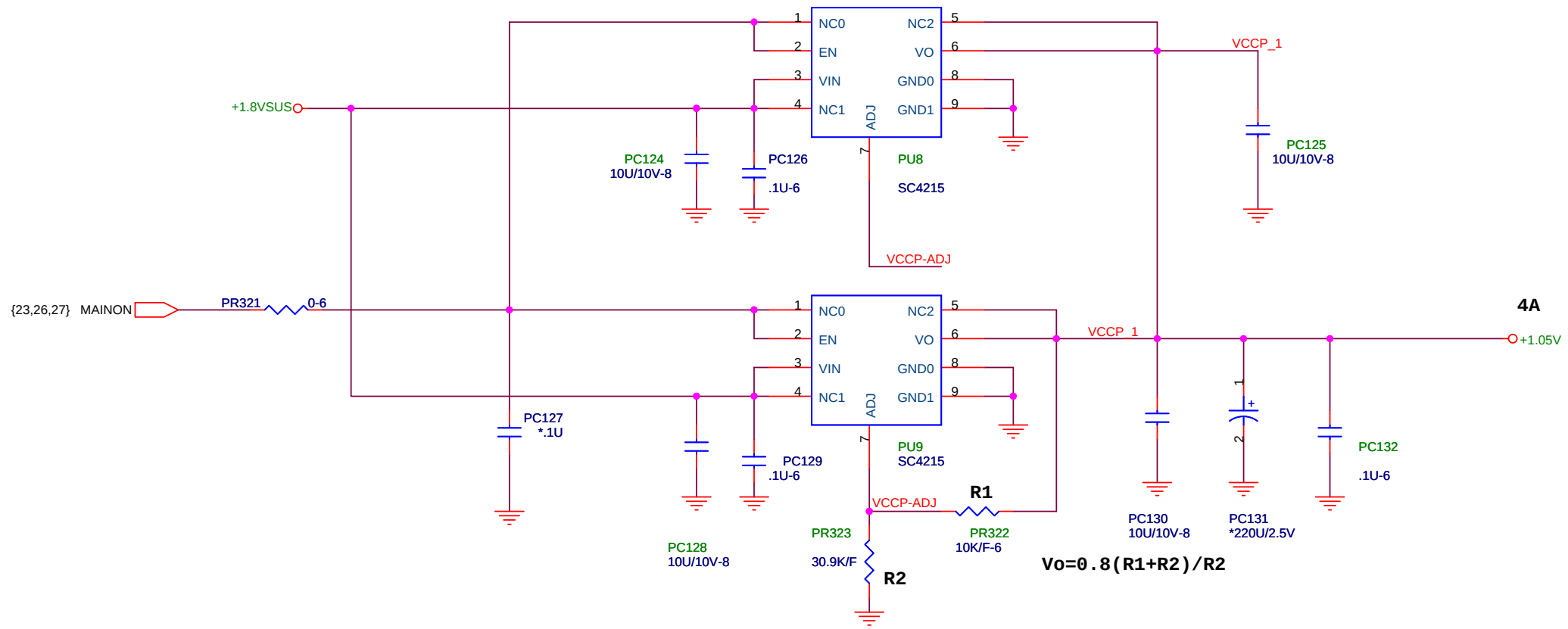


PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	+1.8/1.2V / VTT	1A
Date: Saturday, January 07, 2006	Sheet 27 of 29	


PCN37
POWER_CON
PC97 .1U/25_8
PC98 .1U/25_8
HI0805R800R-00_8
PL9
PL10
HI0805R800R-00_8
PF1
LITTLE-7A-1206
VA
PC94 .1U/25_8
PC99 .1U/25_8
PC100 2200P_4
PC95 .1U/25_8
PD9
SPL1040PT
PD10
SW1010CPT
PR297
0.01_3720
PC102 *.1U/50V_6
PC103 *.1U/50V_6
PQ34
AO4427
BAM44270000
PQ35
AO4427
BAM44270000
CS_OUT
PC101
0.1U/25V/0805/X7R
CH4104J1A00
PR295
220K/0603/F
CS42203F916
2711_gate
PC96
0.1U/25V/0805/X7R
CH4104J1A00
VIN
PR296
33K/0603
CS33303J921
PR298
220K/0603/F
CS42203F916
PQ36
IMD2AT108
BAIMD2A0Z01
PR299
0R/0603
CS00003J951
D/C# {23}
PR300
10K/0603
CS31003J941
PQ37
2N7002E
BAM70020074
{23} ACIN
PR301
10K_6
PD11
ZD12V
PR302
6.8K_6
PR304
10K_6
PC104
1U_8
CSSP
CSSN
FOR 4S3P CELL-SET HIGH
FOR 3S3P CELL-SET FLOAT
CELLS
PR303 100K_6
REF3V
PR305
100K_6
PR306 0_6
CELL-SET {23}
PC105 10U/25V_1206
PC106 .1U/25_8
PL11
HI0805R800R-00_8
PR307 33_6
PC107
1U/10V_6
PC110
1U/10V_6
PU7
MAX8724
DCIN
ACIN
VCTL
ICTL
REFIN
ACOK
ICHG
IINP
SHDN
CCV
CCI
CCS
CSSP
CSSN
CELLS
LDO
DLOV
BST
DHI
LX
DLO
PGND
CSIP
CSIN
BATT
REF
CLS
GND
8724LDO
PD12
SW1010CPT
8724BST
PC111
.1U/25_8
8724DH
8724LX
8724DL
PQ38
AOS4912
PL12
10UH-MSCDR1-104R
PR309
0.015_3720
PC135
*100U/25V
BAT-V
PC114
.01U/50V_6
PC113
10U/25V_1206
PC133
*10U/25V_1206
8724LDO
REF3V
PC108
.1U/25_6
PR308
0_6
PR310
*0_6
{23} CV-SET
{23} CC-SET
PC109
1000p_4
PC112
1000P_4
(change
cv-set to
8724 LDO)
PR311
0_6
PR313
1K/F_6
PR314
0_6
PR315
0_6
PC117
.1U/25_6
PC118
.01U/50V_6
PC119
.01U/50V_6
8724REF
PR312 11.5K/F_6
PR316
10K/F_6
PC116
1U/10V_6
CURRNT LIMIT POINT = 3.4A
VIN
C488
1U_6
FOR EMI
PC115
1000p_4
MBAT+
TEMP_MBAT
PCN38
SUYIN BATTERY
10mil
PC120
47P_4
PC121
47P_4
PC122
.1U/25_6
PR318
330_4
PR317
330_4
MTEMP {23}
PF2
LITTLE-7A-1206
HI0805R800R-00_8
PL13
PL14
HI0805R800R-00_8
BAT-V
PR319 10K/F_6
REF3V
PR320
0_6
3V_591
+3VPCU
MBCLK {2,23}
MBDATA {2,23}
MBDATA
TEMP_MBAT
PD13
ZD5.6V
PD14
ZD5.6V
PC123
.01U/50V_6
SMBus SLAVE ADDRESS: 16
PROJECT : BL1
Quanta Computer Inc.
Size
Custom
Document Number
BATTERY CHARGER
Rev
1A
Date: Saturday, January 07, 2006
Sheet 28 of 29



PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	+1.05V	1A
Date: Saturday, January 07, 2006	Sheet 29 of 29	