

**CPU CORE**  
SENTECH  
SC451  
Page: 25

**+3VPCU**  
**+3V\_S5/+3VSUS**  
**+3V**  
**+5VSUS/+5V**  
**10V/15V**  
**+1.8V\_S5**  
MAXIM  
MAX8744ETJ+  
Page: 26

**+1.8VSUS/+1.8V**  
**+1.2V**  
MAXIM  
MAX8743EEI  
Page: 27

**+1.05V**  
SENTECH  
SC4215\*2  
Page: 29

**+0.9VSUS**  
**+0.9V**  
GMT  
G2996  
Page: 26, 29

**BATTERY CHARGER**  
MAXIM  
MAX8724  
Page: 28

**Power State Table**

| Power Name | Control Signal | Power State | Power Source |
|------------|----------------|-------------|--------------|
| VCC_CORE   | VR0N           | S0          | VIN          |
| +3VPCU     | N/A            | ALWAYS      | VIN          |
| +3V_S5     | S5_ON          | S0-S5       | +3VPCU       |
| +3VSUS     | SUS0N          | S0-S3       | +3VPCU       |
| +3V        | MAIN0N         | S0          | +3VPCU       |
| +5VPCU     | N/A            | ALWAYS      | VIN          |
| +5V_S5     | S5_ON          | S0-S5       | +5VPCU       |
| +5VSUS     | SUS0N          | S0-S3       | +5VPCU       |
| +5V        | MAIN0N         | S0          | +5VPCU       |
| 15V/10V    | N/A            | S0          | +5VPCU       |
| +1.2V      | MAIN0N         | S0          | VIN          |
| +1.05V     | MAIN0N         | S0          | +1.8VSUS     |
| +0.9V      | MAIN0N         | S0          | +1.8VSUS     |
| +1.8V_S5   | S5_ON          | S0-S5       | +3VPCU       |
| +1.8VSUS   | SUS0N          | S0-S3       | VIN          |
| +1.8V      | MAIN0N         | S0          | +1.8VSUS     |
| +1.5V      | MAIN0N         | S0          | +3V          |

**CLOCK GEN**  
RTM865-300  
**+3V**  
Page: 4

**Yonah Celeron-M**  
INTEL Mobile\_479 CPU  
SOCKET\_M  
Page: 2, 3

**DDR-II SODIMM1**  
Page: 9

**DDR-II SODIMM2**  
Page: 9

**NB**  
**RC410MD**  
**ATI**  
Page: 5, 6, 7, 8

**SATA HDD**  
Page: 18

**IDE-ODD**  
Page: 18

**SB**  
**ATi SB450**  
Page: 11, 12, 13, 14

**AUDIO CODEC**  
REALTEK  
ALC861  
Page: 19

**GMT**  
G1432+G1410  
Page: 20

**MODEM**  
AGERE  
DELPHI-MOM  
Page: 21, 22

**KBC**  
NS  
PC97551  
Page: 23

**Winbond**  
PC87383  
(Option)  
Page: 30

**RS-232**  
(option)  
Page: 30

**MIC IN**  
Page: 20

**SPEAKER**  
Page: 20

**LINE OUT**  
Page: 20

**RJ11**

**Touchpad**  
Page: 24

**Keyboard**  
Page: 24

**FLASH**  
Page: 24

**FAN**  
Page: 24

**ENE PCMCIA**  
**CB1410 (option)**  
AD17  
REQ3# / GNT3#  
INTE#  
Page: 16

**TYPE II**  
**SLOT**  
Page: 16

**MINI-PCI**  
**Wireless LAN**  
AD20  
REQ1# / GNT1#  
INTG# , INT#  
Page: 17

**REALTEK**  
**RTL8100CL**  
AD18  
REQ0# / GNT0#  
INTF#  
Page: 15

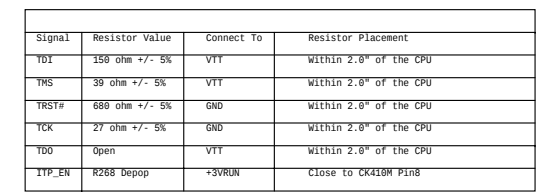
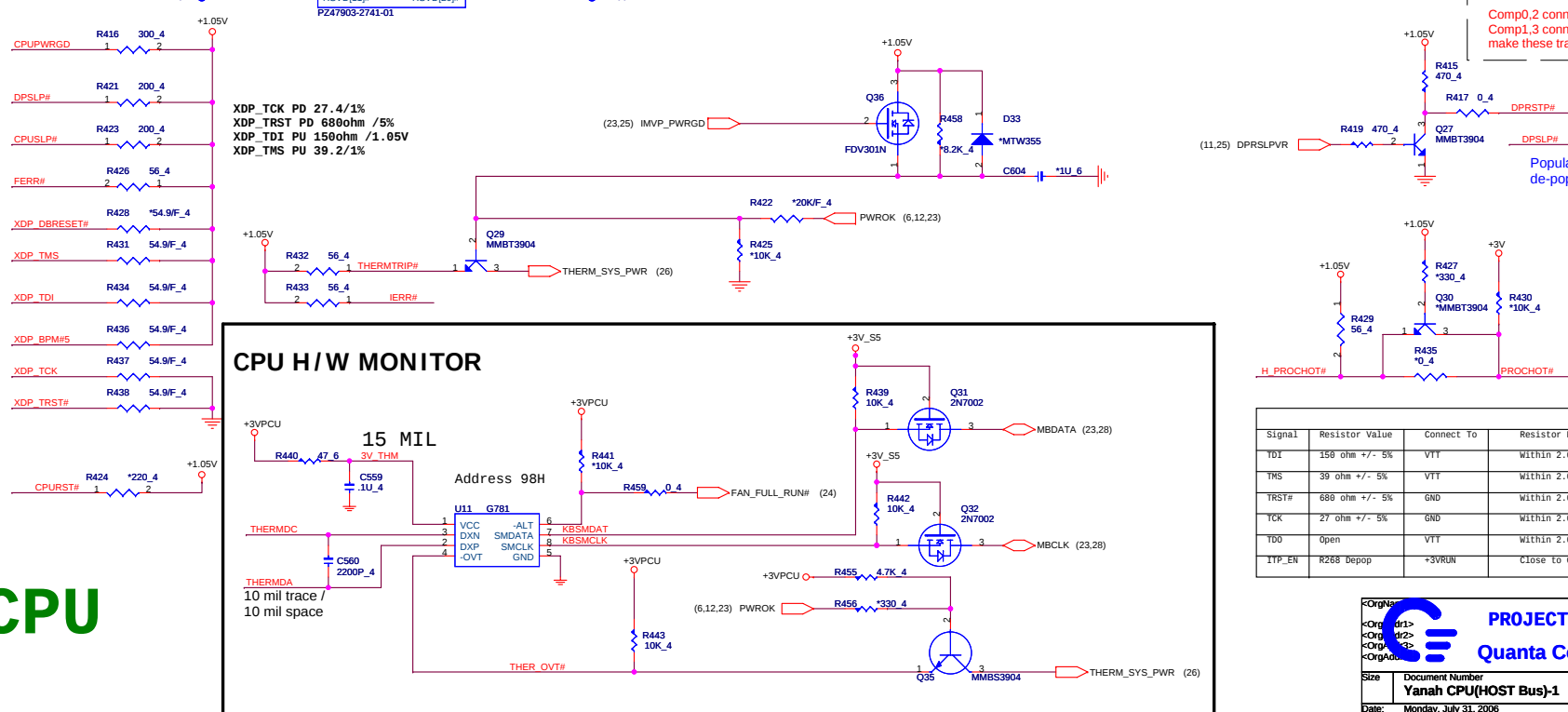
**BOTH HAND**  
**TRANSFORMER**  
NS0013  
Page: 15

**RJ45**  
Page: 15

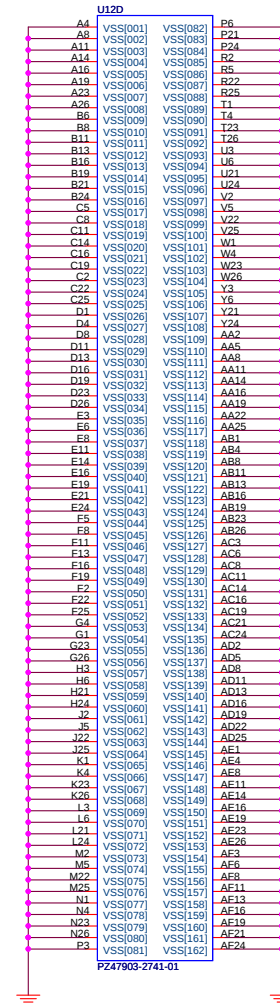
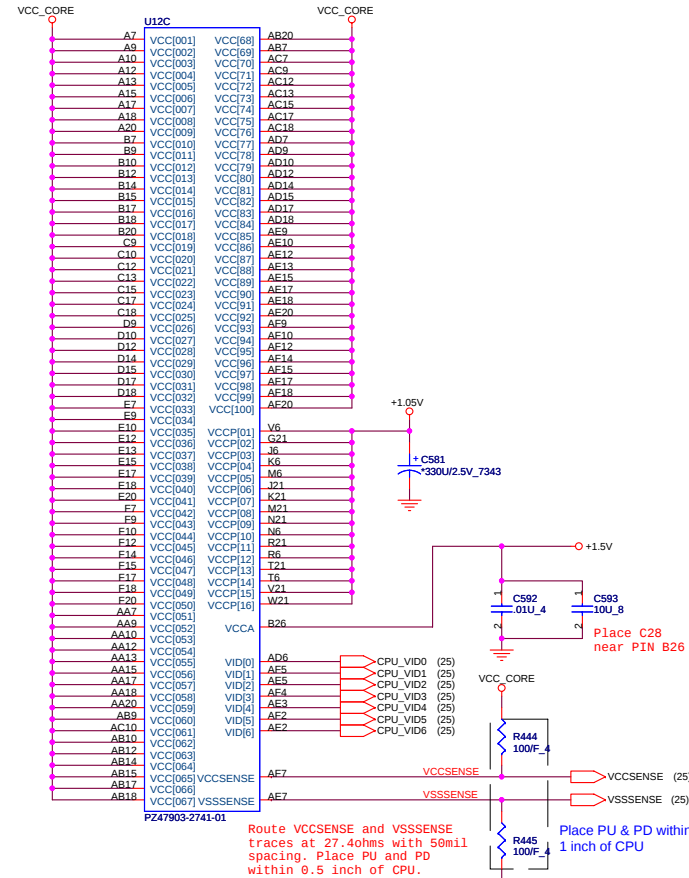
**SYSTEM**  
**USB PORT \*2**  
USB2,3  
Page: 17

**PROJECT : BL3**  
**Quanta Computer Inc.**

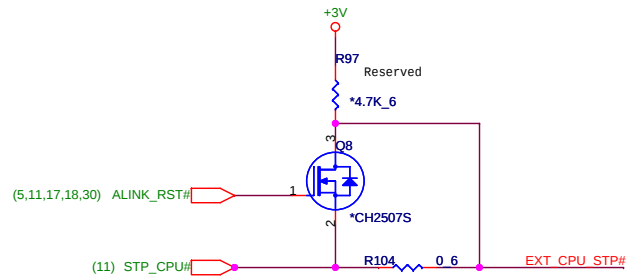
|       |                       |               |
|-------|-----------------------|---------------|
| Size  | Document Number       | Rev           |
|       | <b>BLOCK DIAGRAM</b>  | 3B            |
| Date: | Monday, July 31, 2006 | Sheet 1 of 31 |



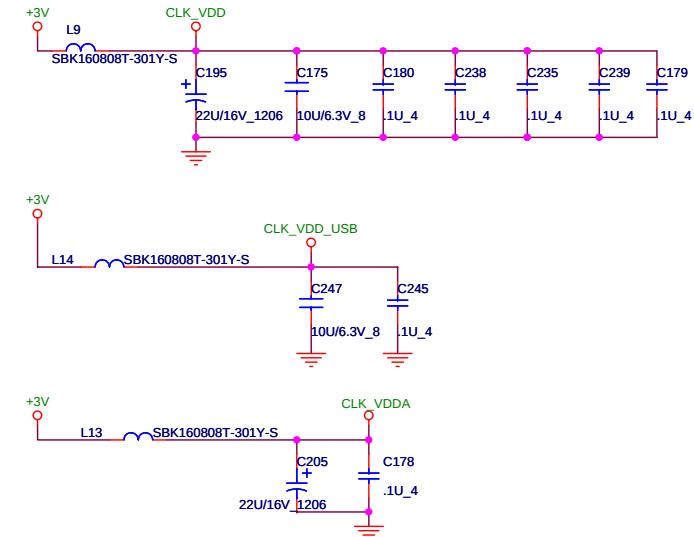
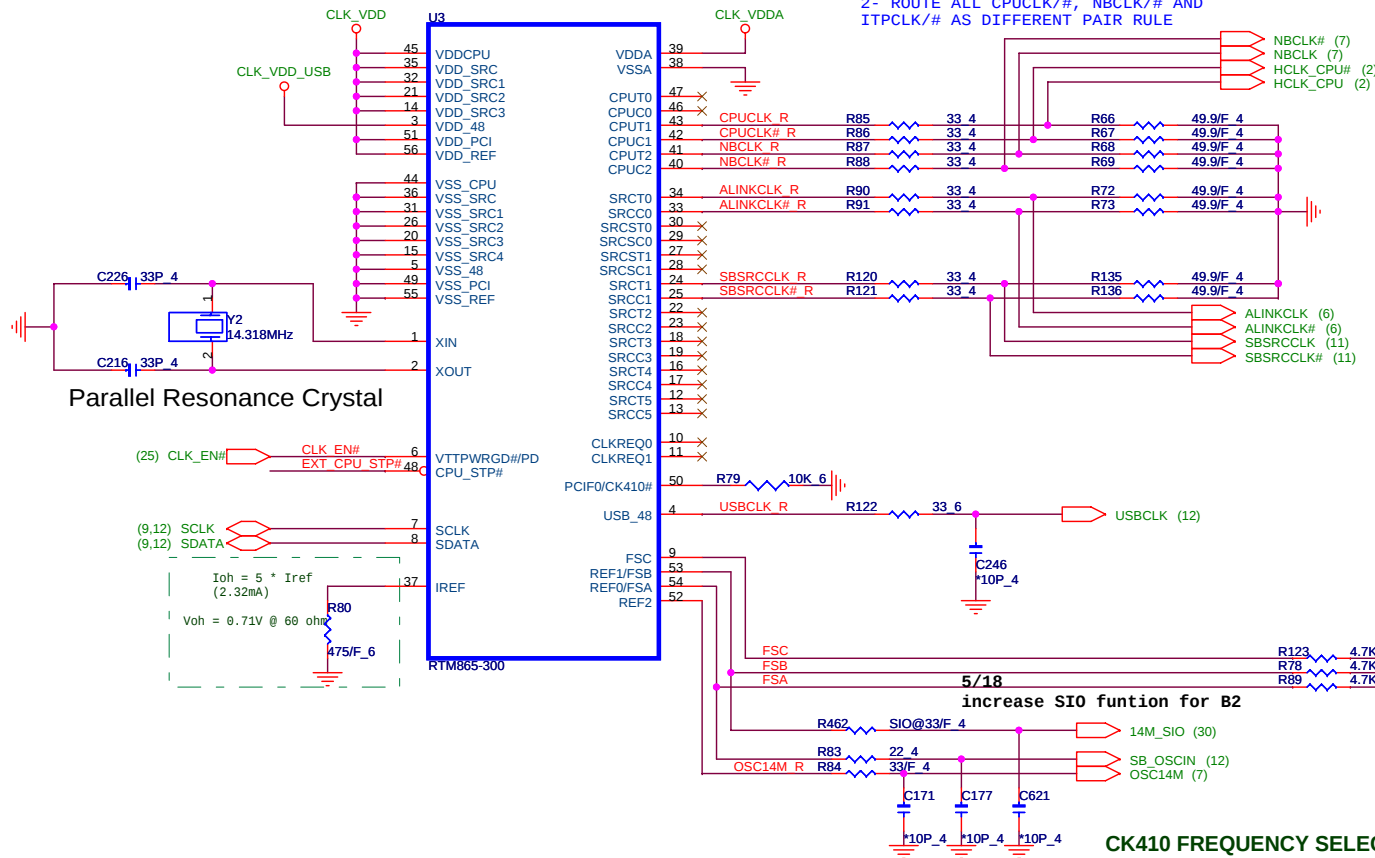
22uF 0805 X6S->105 degree C  
8 inside cavity north side secondary layer, 8 inside cavity south side secondary layer, 6 inside cavity north side primary layer, 6 inside cavity south side primary layer.



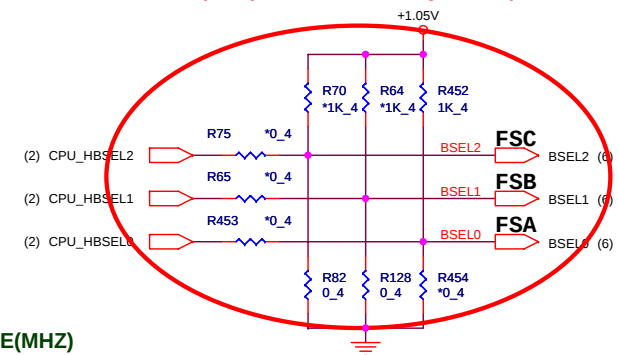
CPU



- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS CLK GEN AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBCLK/# AND ITPCLK/# AS DIFFERENT PAIR RULE



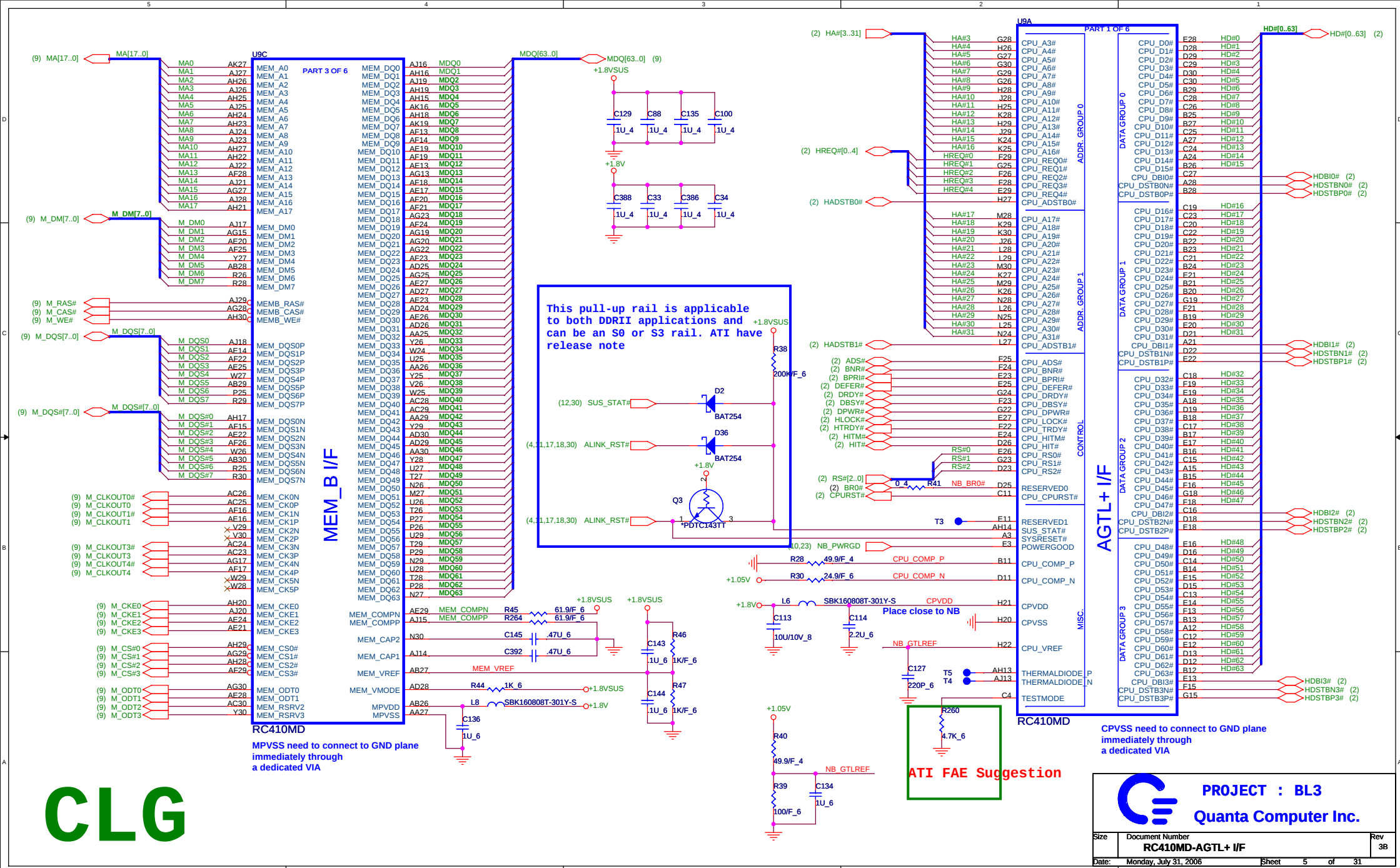
fixed CPU frequency 133MHz for 0 degree temperature issue



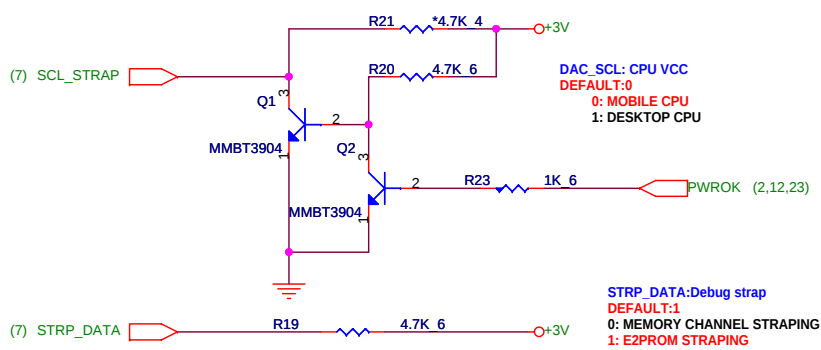
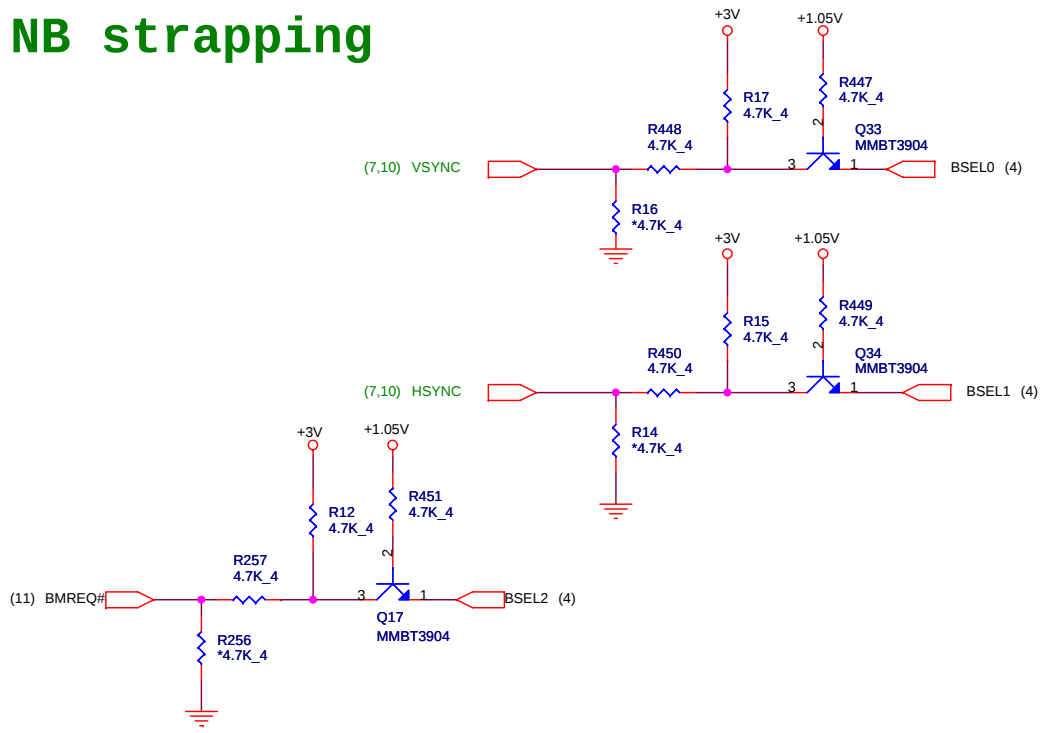
CK410 FREQUENCY SELECT TABLE(MHZ)

| FSC   | FSB   | FSA   | CPU  | SRC | PCI | REF   |
|-------|-------|-------|------|-----|-----|-------|
| BSEL2 | BSEL1 | BSEL0 |      |     |     |       |
| 1     | 0     | 1     | 100  | 100 | 33  | 14.31 |
| 0     | 0     | 1     | 133  | 100 | 33  | 14.31 |
| 0     | 1     | 1     | 166  | 100 | 33  | 14.31 |
| 0     | 1     | 0     | 200  | 100 | 33  | 14.31 |
| 0     | 0     | 0     | 266  | 100 | 33  | 14.31 |
| 1     | 0     | 0     | 333  | 100 | 33  | 14.31 |
| 1     | 1     | 0     | 400  | 100 | 33  | 14.31 |
| 1     | 1     | 1     | Resv | 100 | 33  | 14.31 |

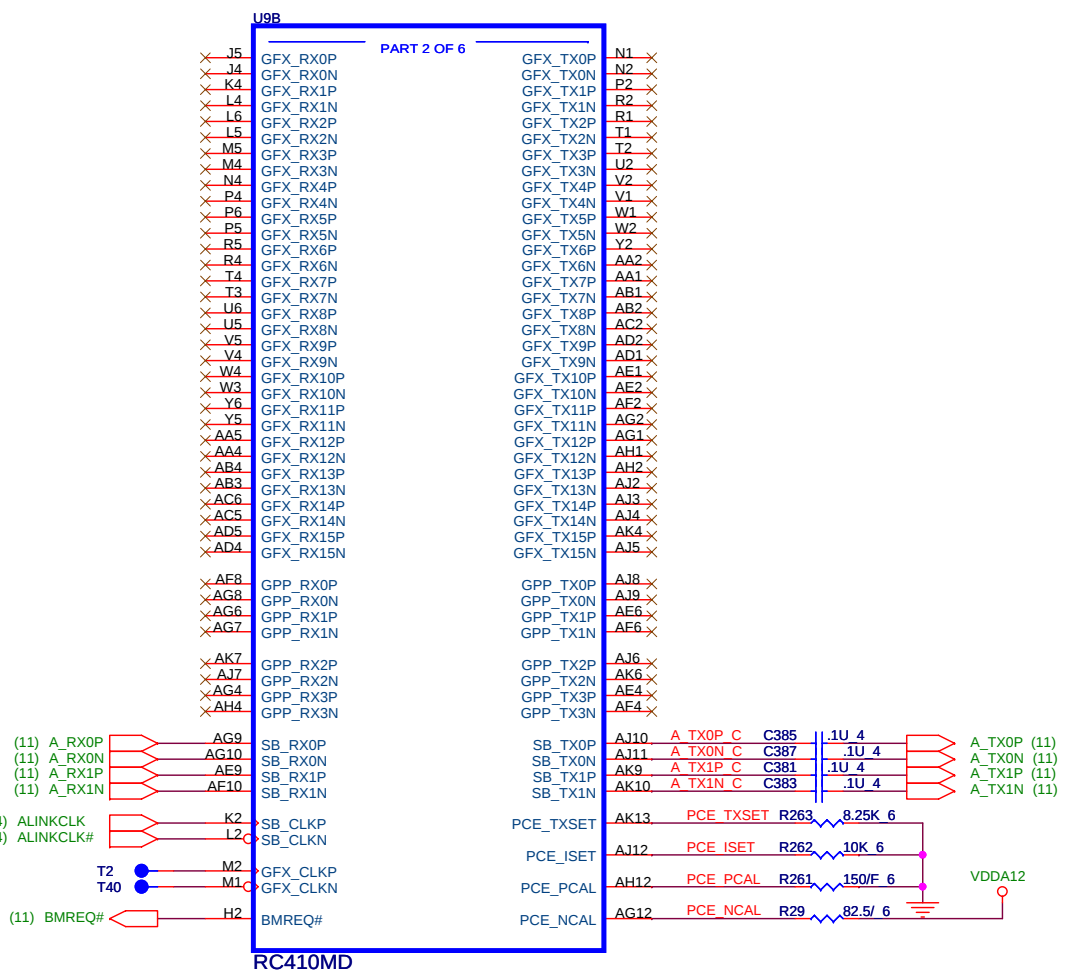
CLK



# NB strapping



# CLG





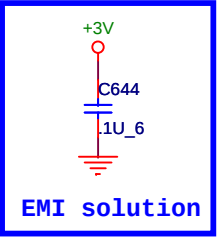
**PROJECT : BL3**

**Quanta Computer Inc.**

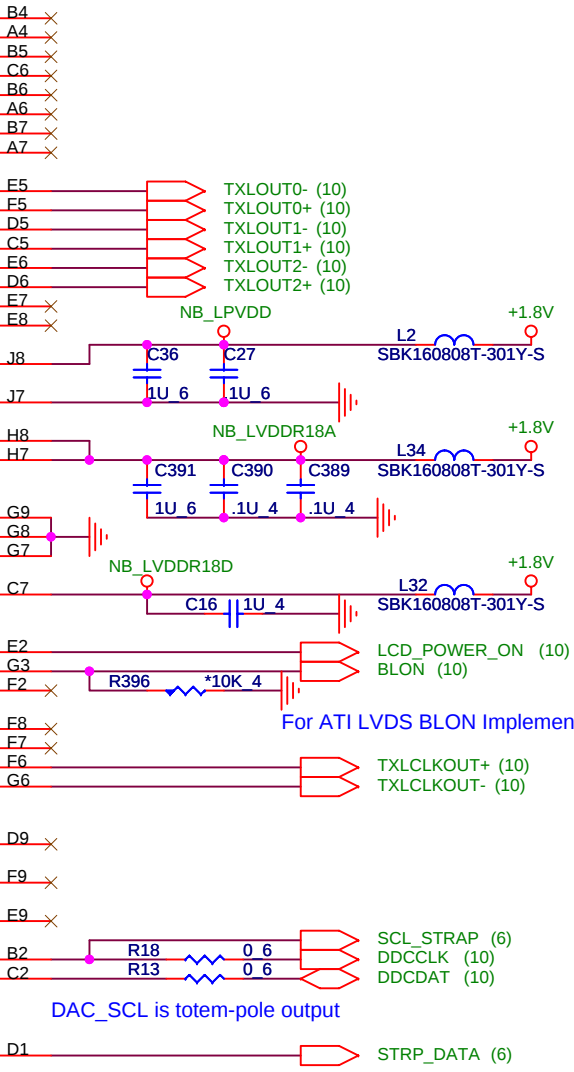
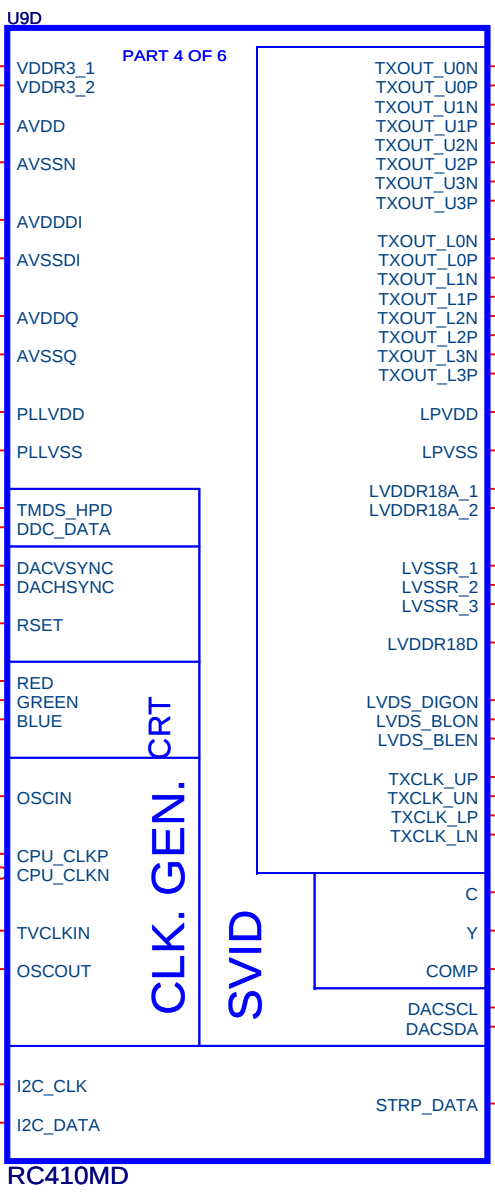
|       |                              |               |
|-------|------------------------------|---------------|
| Size  | Document Number              | Rev           |
|       | <b>RC410MD-PCIE LINK I/F</b> | 3B            |
| Date: | Friday, August 11, 2006      | Sheet 6 of 31 |

Change L5 from bead to inductance  
for CRT flicker issue

RSET resistor need 10mils  
trace with at least 10mils  
spacing.  
Also need to connect GND  
at AVSSQ HF cap.



CLG





**PROJECT : BL3**

**Quanta Computer Inc.**

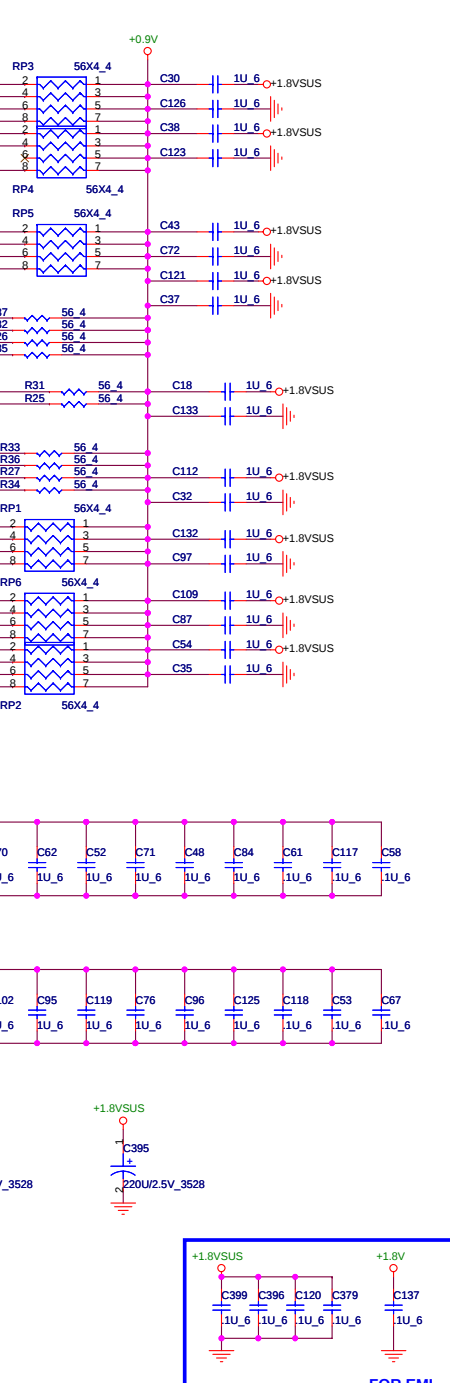
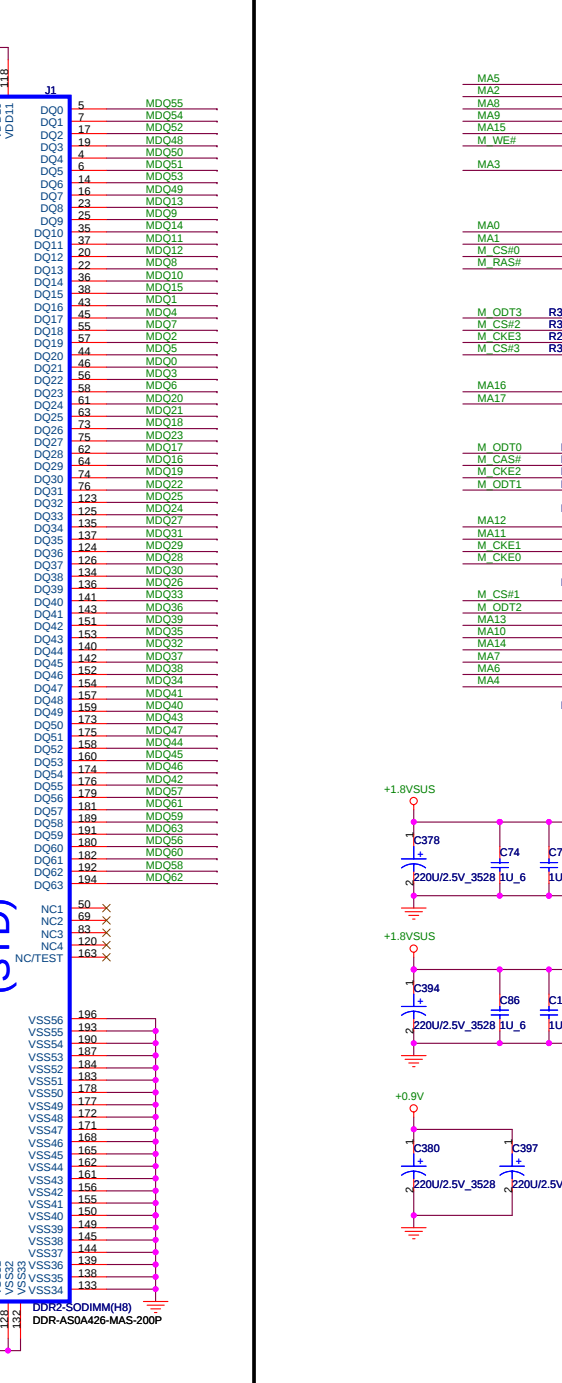
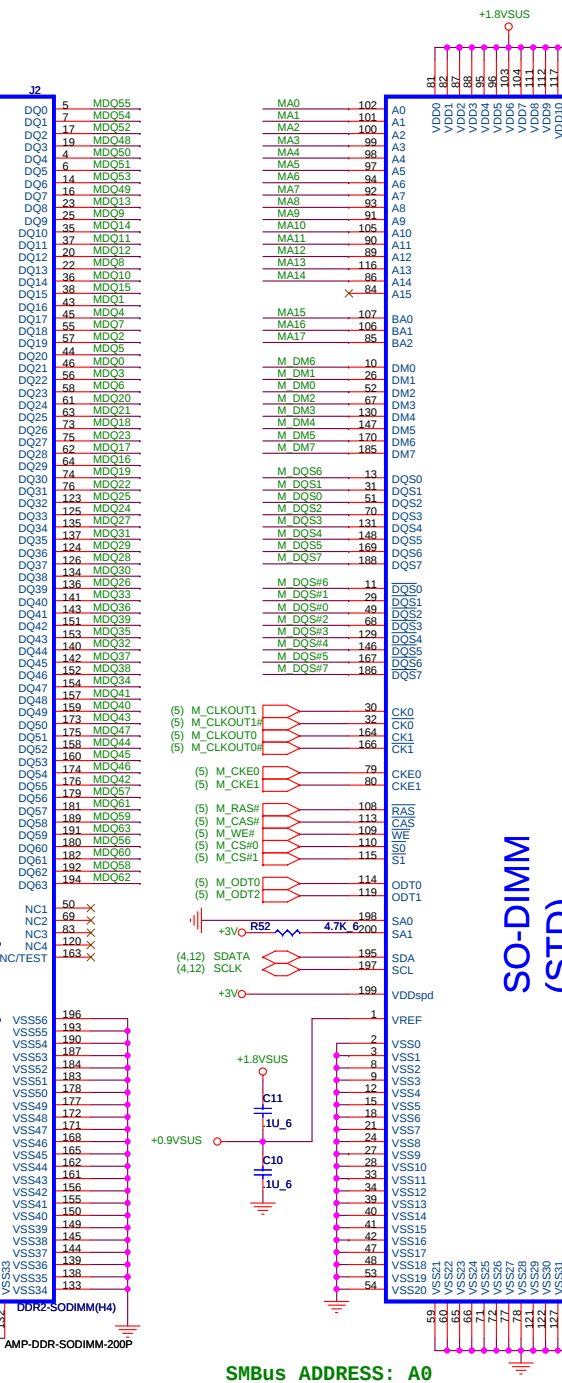
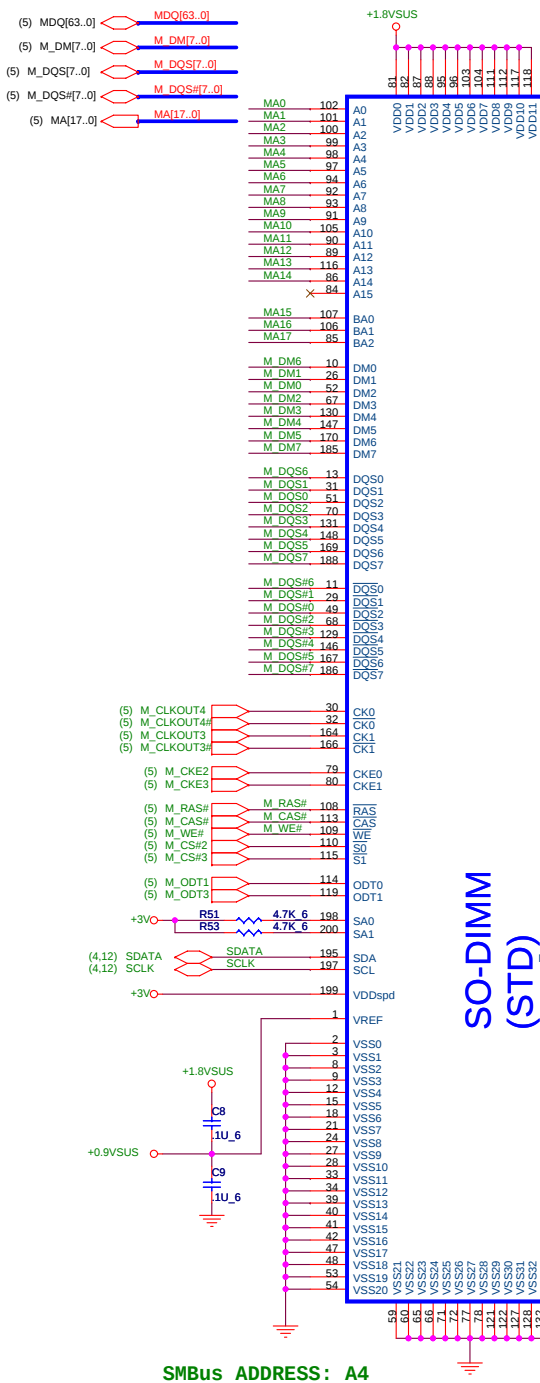
|       |                                   |               |
|-------|-----------------------------------|---------------|
| Size  | Document Number                   | Rev           |
|       | <b>RC410MD-VIDEO &amp; CLKGEN</b> | <b>3B</b>     |
| Date: | Friday, August 11, 2006           | Sheet 7 of 31 |



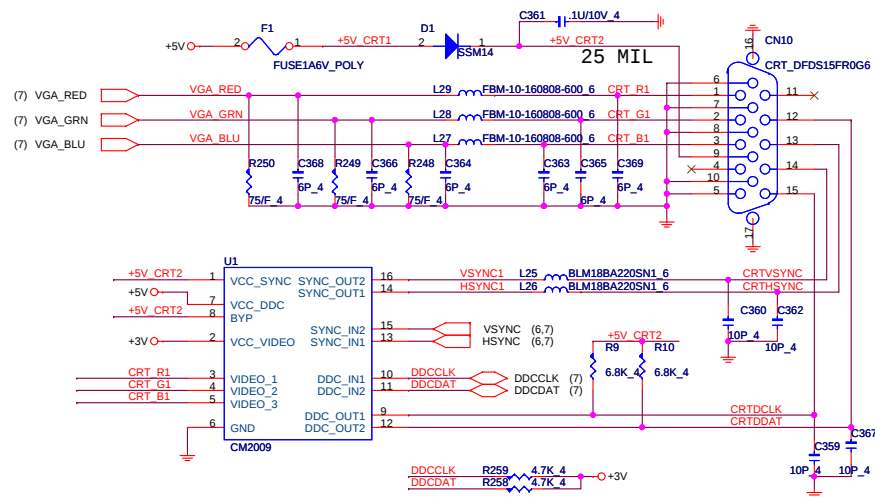
**PROJECT : BL3**  
**Quanta Computer Inc.**

|       |                                         |                  |
|-------|-----------------------------------------|------------------|
| Size  | Document Number<br><b>RC410MD-POWER</b> | Rev<br><b>3B</b> |
| Date: | Friday, August 11, 2006                 | Sheet 8 of 31    |

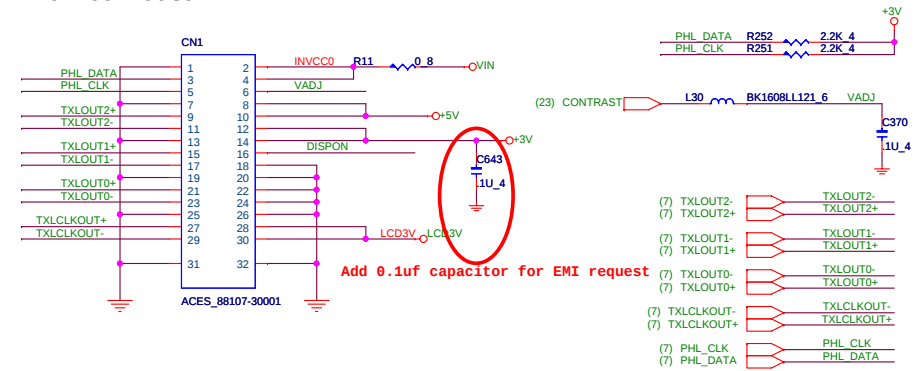
DDR



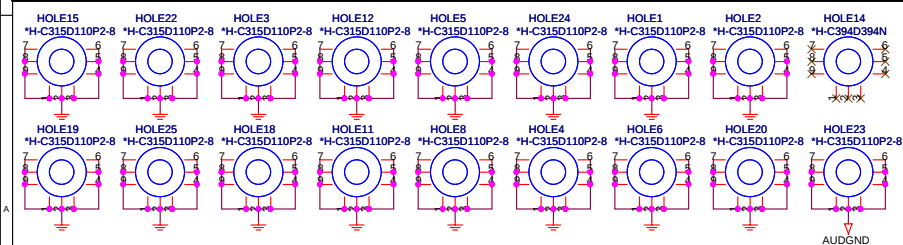
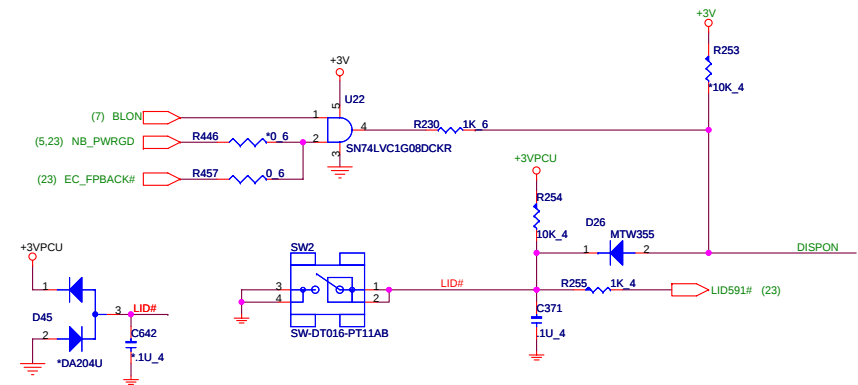
## CRT PORT



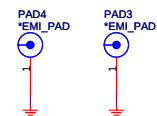
## LCD Connector



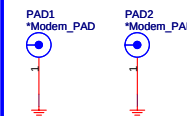
## Lid Switch



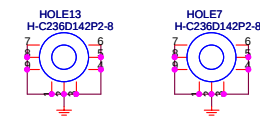
### EMI PAD



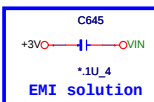
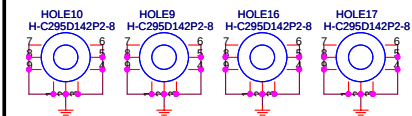
### Modem



### NB SINK



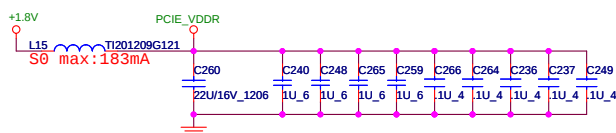
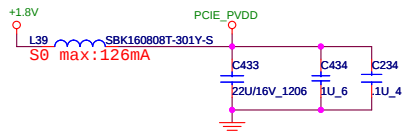
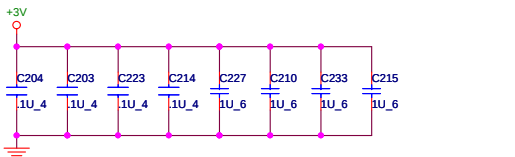
### CPU SINK



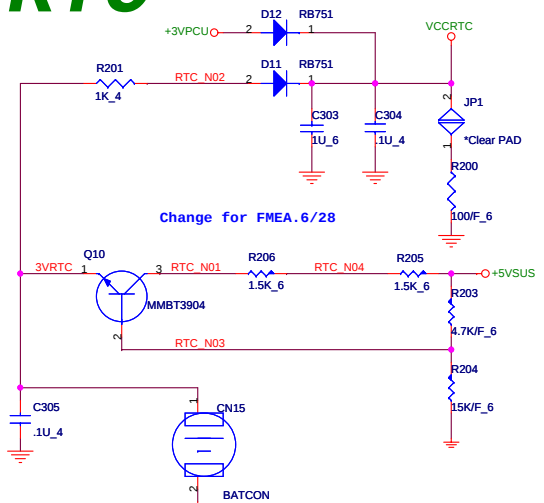
PROJECT : BL3  
Quanta Computer Inc.

| Size  | Document Number         | Rev            |
|-------|-------------------------|----------------|
|       | VGA Ports, LID, & HOLES | 3B             |
| Date: | Friday, August 11, 2006 | Sheet 10 of 31 |

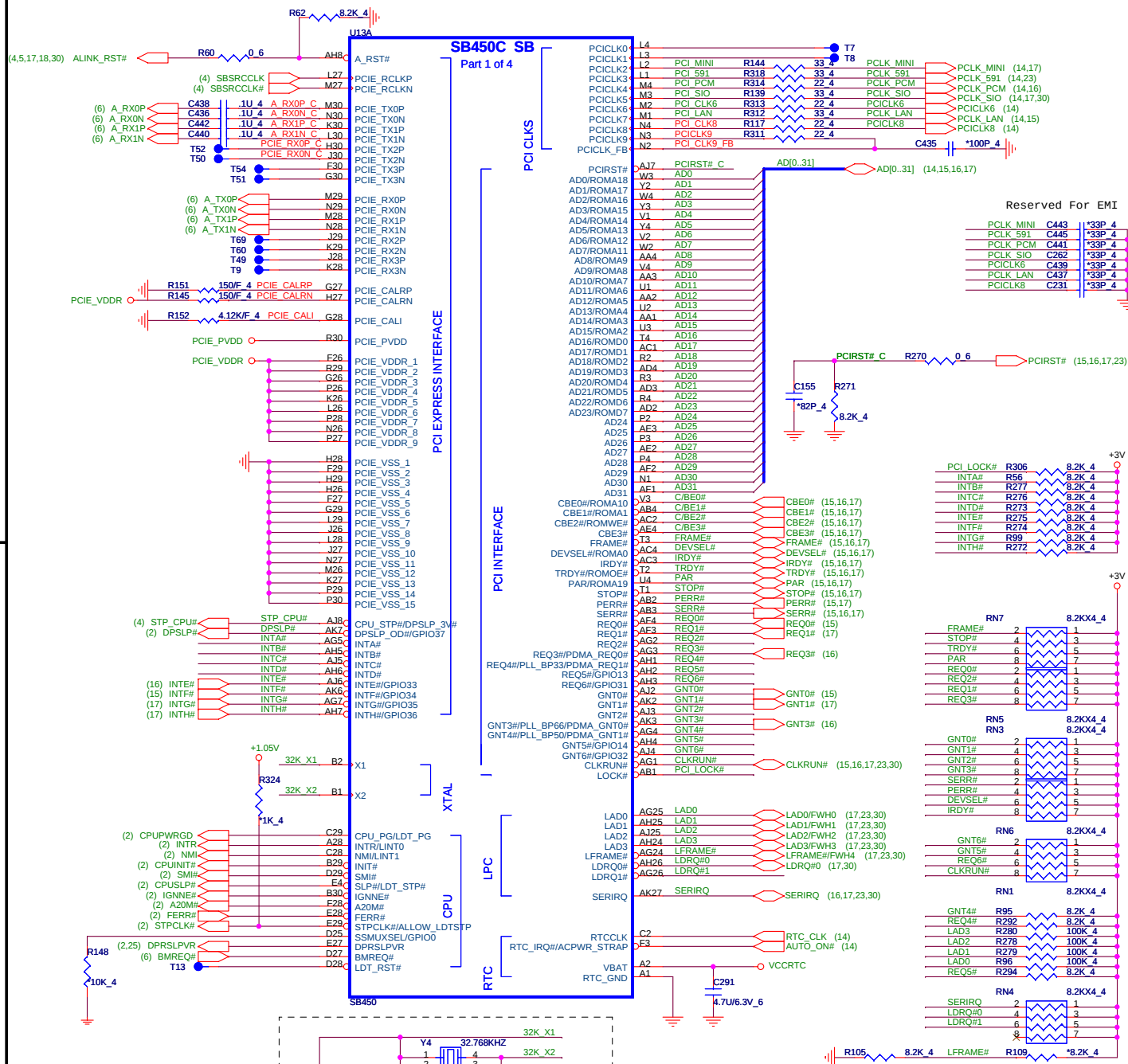
VGA



# RTC



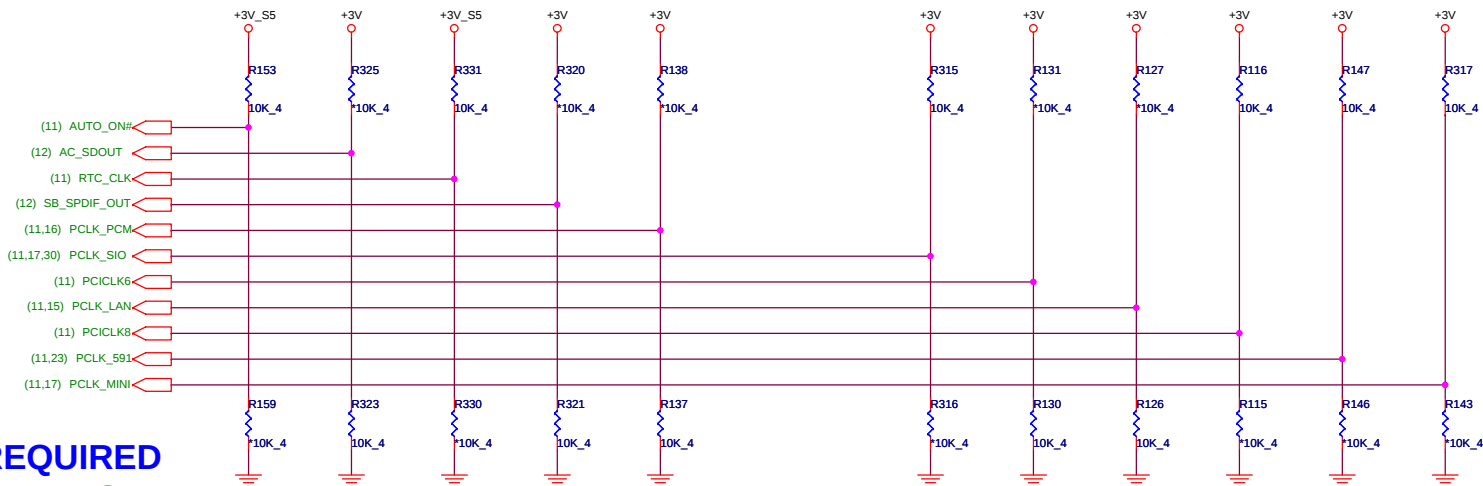
# CLG







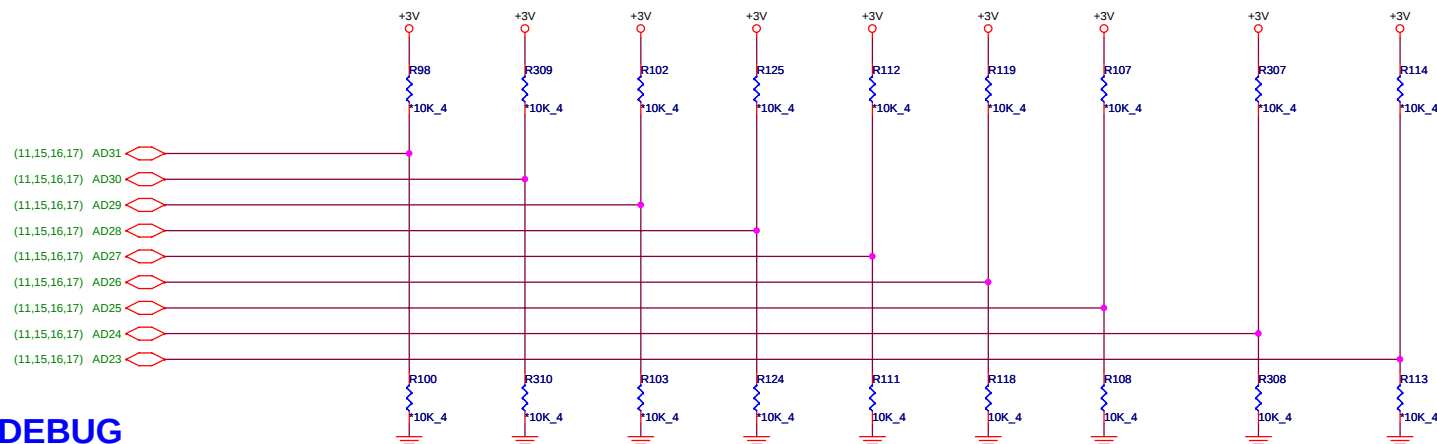
## REQUIRED STRAPS



|           |                          |                                |                                         |                      | PCI_CLK4                            | PCI_CLK5                  | PCI_CLK6                | PCI_CLK7                                                                                                  | PCI_CLK8                                                            | PCI_CLK3                           | PCI_CLK2                     |
|-----------|--------------------------|--------------------------------|-----------------------------------------|----------------------|-------------------------------------|---------------------------|-------------------------|-----------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|------------------------------------|------------------------------|
|           | ACPWRON                  | AC_SDOUT                       | RTC_CLK                                 | SPDIF_OUT            | PCLK_PCM                            | PCLK_SIO                  | PCI_CLK6                | PCLK_LAN                                                                                                  | PCI_CLK8                                                            | PCLK_591                           | PCLK_MINI*                   |
| PULL HIGH | MANUAL PWR ON<br>DEFAULT | USE DEBUG STRAPS               | INTERNAL RTC<br>DEFAULT                 | SIO 24MHz            | 48MHz use Internal PLL              | 14MHz OSC MODE<br>DEFAULT | CPU I/F = K8            | H,H = PCI(X BUS) ROM<br>H,L = LPC ROM I (LPC addresses are translated to the top of the 4G address space) | L,H = LPC ROM II<br>(addresses mapped to below 1M)<br>L,L = FWH ROM | USB PHY PWRDOWN DISABLE<br>DEFAULT | 48MHz Crystal Pad<br>DEFAULT |
| PULL LOW  | AUTO PWR ON              | IGNORE DEBUG STRAPS<br>DEFAULT | EXTERNAL RTC (NOT SUPPORTED W/ IT8712 ) | SIO 48MHz<br>DEFAULT | 48MHz use External Clock<br>DEFAULT | 14MHz XTAL MODE           | CPU I/F = P4<br>DEFAULT |                                                                                                           |                                                                     | USB PHY PWRDOWN ENABLE             | 48MHz OSC/Clock Buffer       |

\*This strap is only required if the strap on PCICLK4 is configured for External Clock.

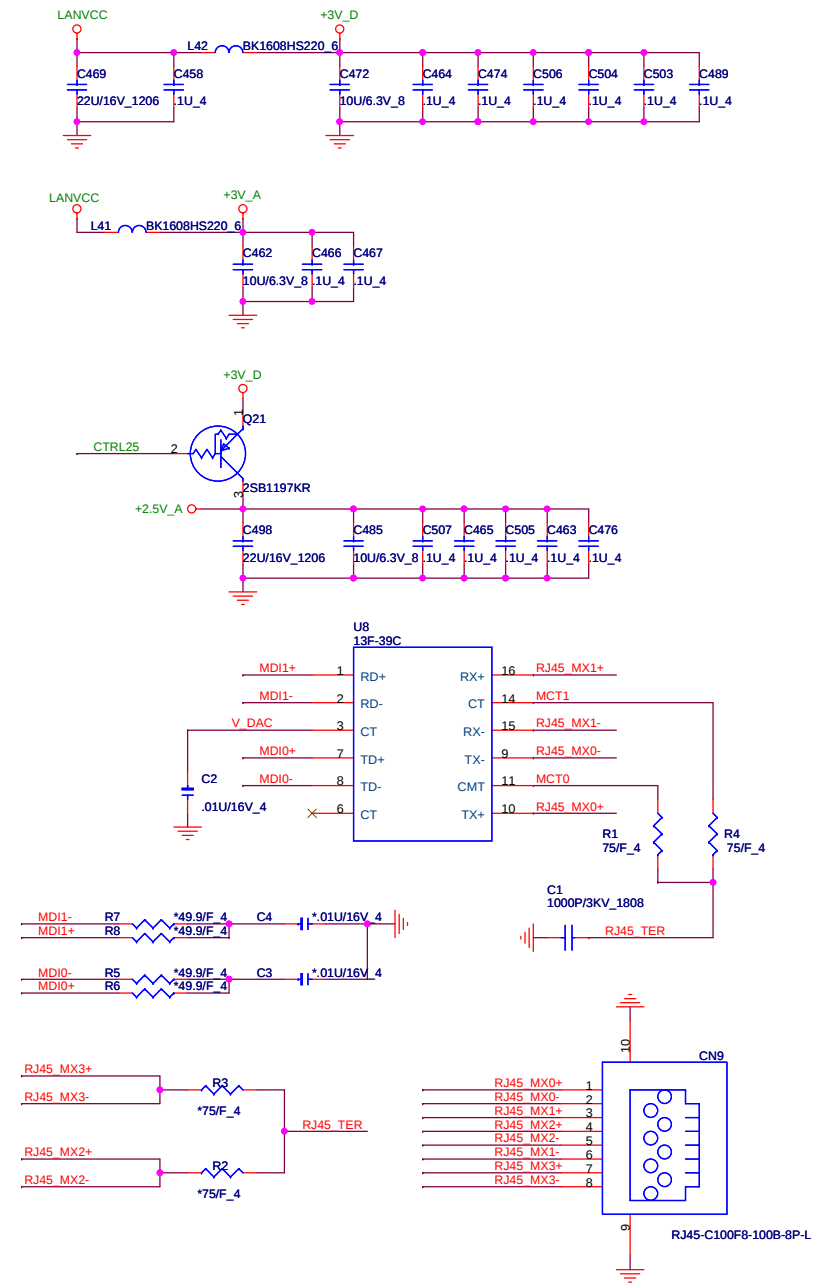
## DEBUG STRAPS



|           | PDACK#                    | PCI_AD31 | PCI_AD30 | PCI_AD29 | PCI_AD28 | PCI_AD27               | PCI_AD26                 | PCI_AD25               | PCI_AD24                           | PCI_AD23 |
|-----------|---------------------------|----------|----------|----------|----------|------------------------|--------------------------|------------------------|------------------------------------|----------|
| PULL HIGH | USE LONG RESET<br>DEFAULT | Reserved | Reserved | Reserved | Reserved | BYPASS PCI PLL         | BYPASS ACPI BCLK         | BYPASS IDE PLL         | USE EEPROM PCIE STRAPS             | Reserved |
| PULL LOW  | USE SHORT RESET           |          |          |          |          | USE PCI PLL<br>DEFAULT | USE ACPI BCLK<br>DEFAULT | USE IDE PLL<br>DEFAULT | USE DEFAULT PCIE STRAPS<br>DEFAULT |          |

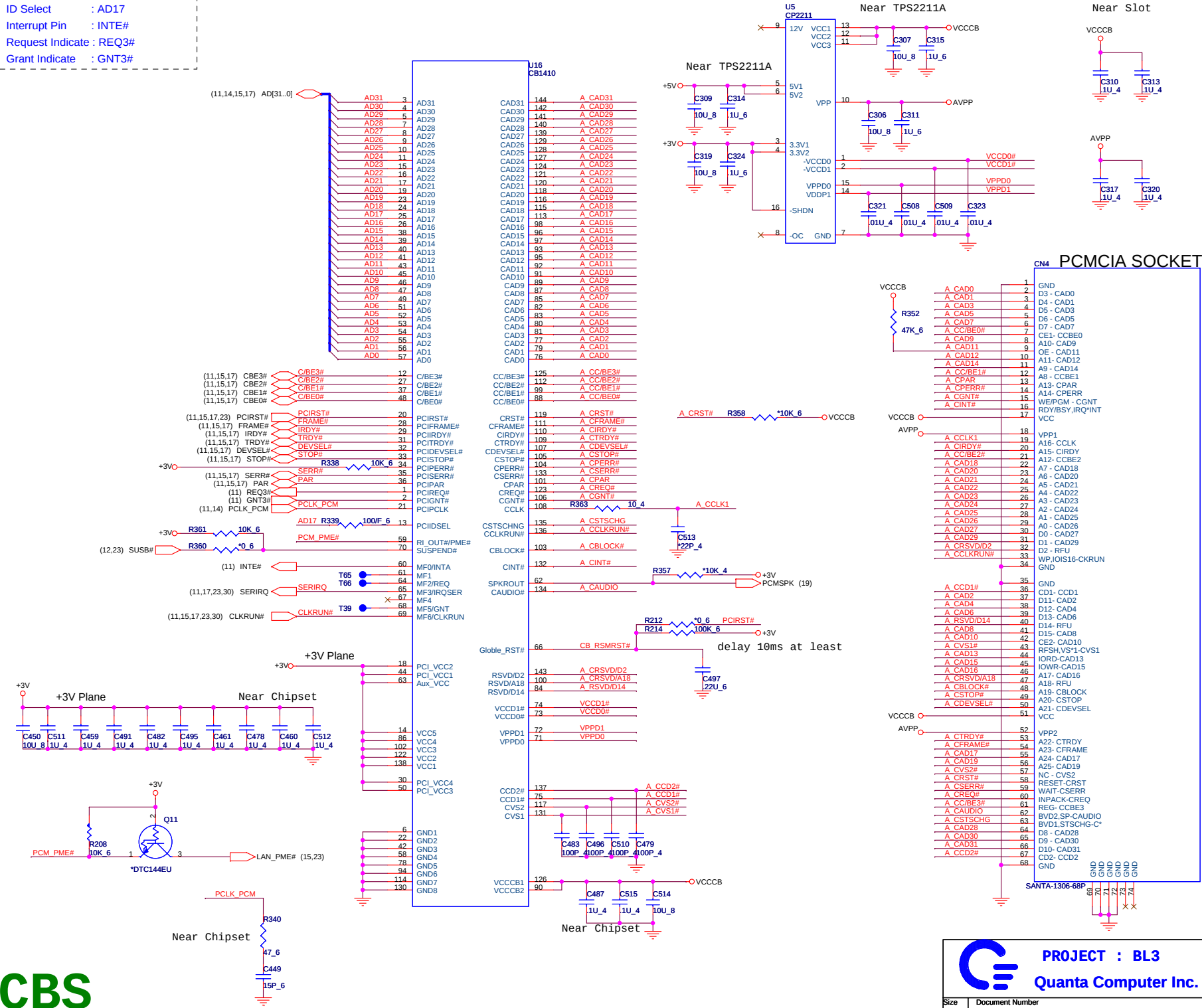
CLG

# LAN



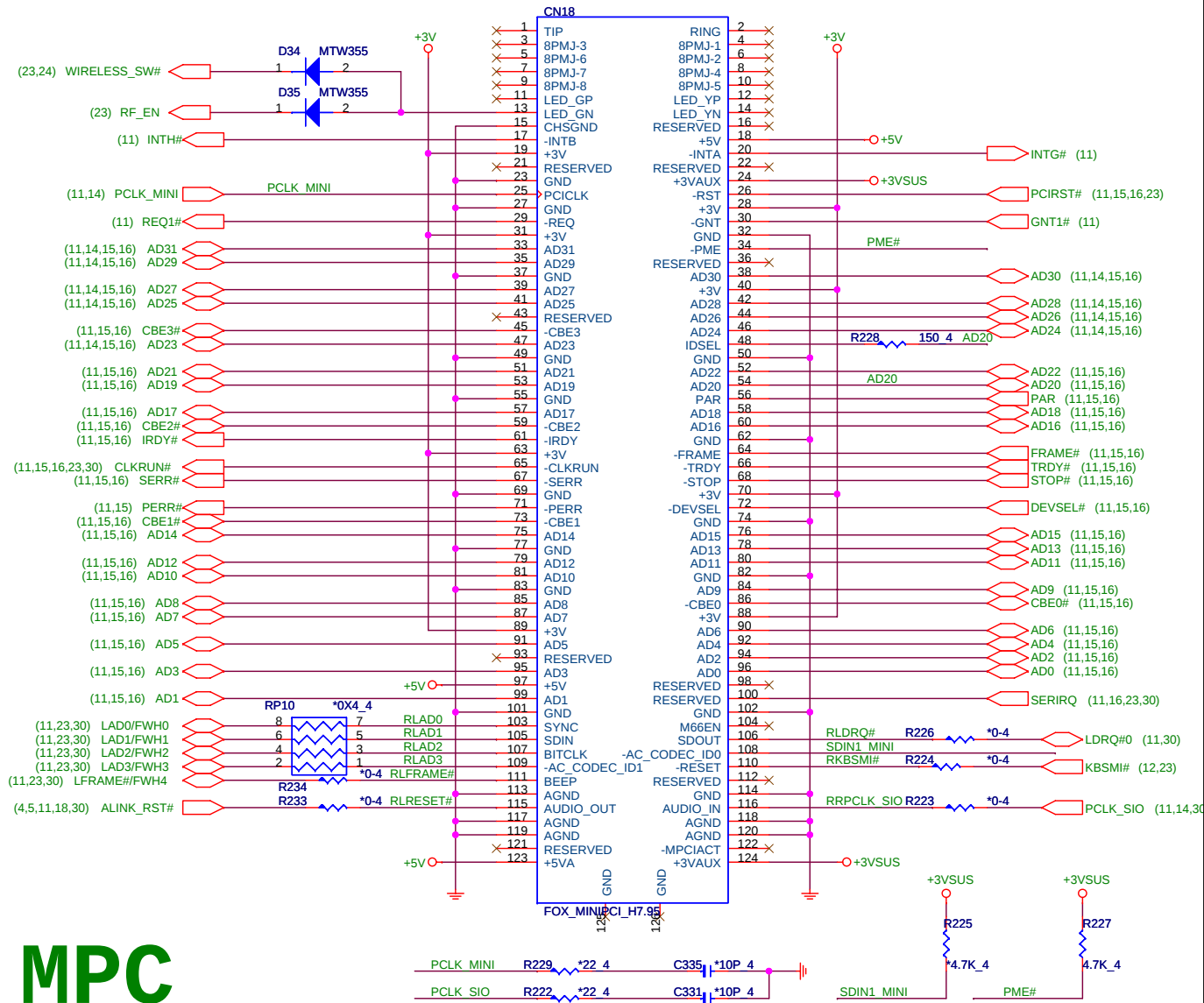
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|-------|-------------------------------------------------|----------------|
| Size  | Document Number<br><b>LAN RTL8110SBL/8100CL</b> | Rev<br>3B      |
| Date: | Friday, August 11, 2006                         | Sheet 15 of 31 |

ID Select : AD17  
Interrupt Pin : INTE#  
Request Indicate : REQ3#  
Grant Indicate : GNT3#



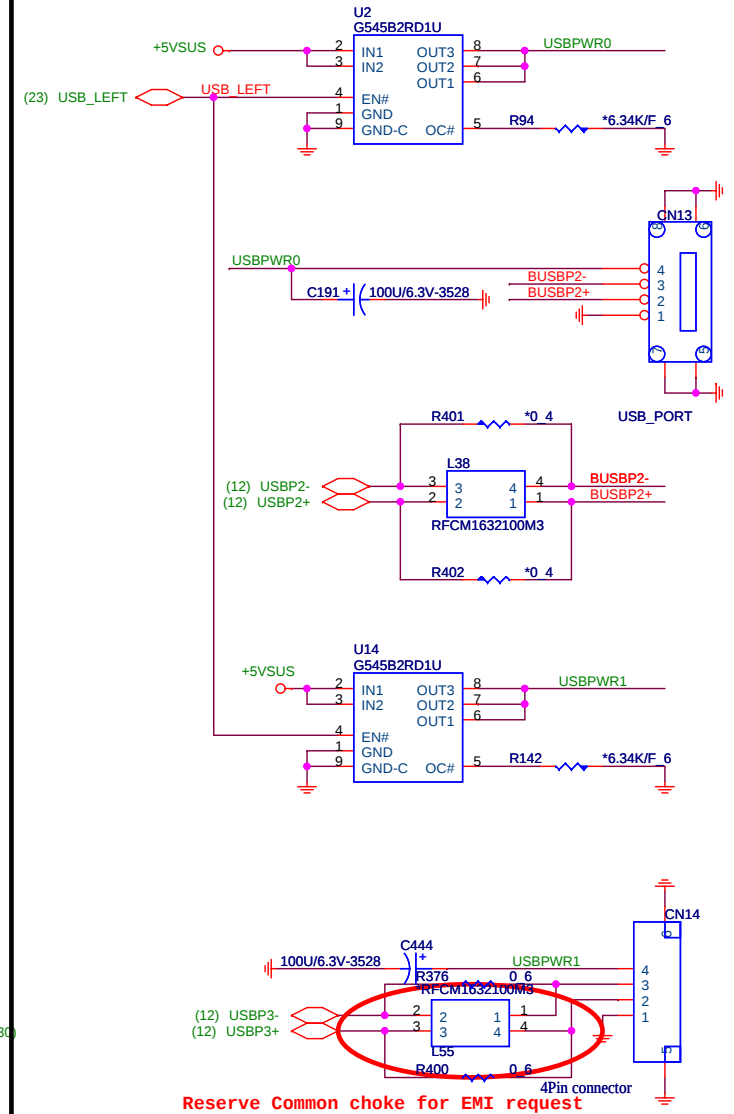
ID Select : AD20  
Interrupt Pin : INTG# , INT#  
Request Indicate : REQ1#  
Grant Indicate : GNT1#

### MINI-PCI



# MPC

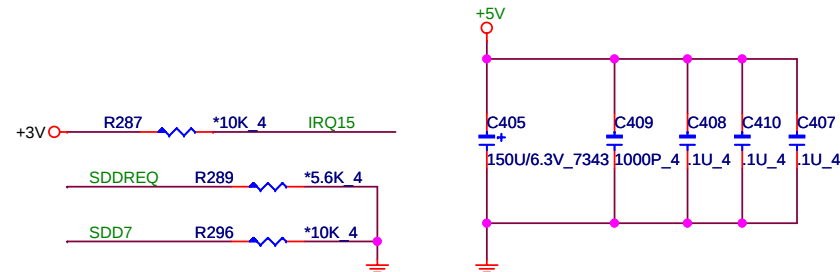
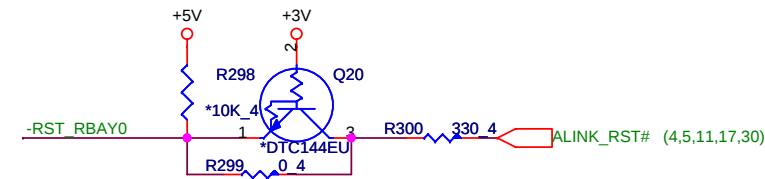
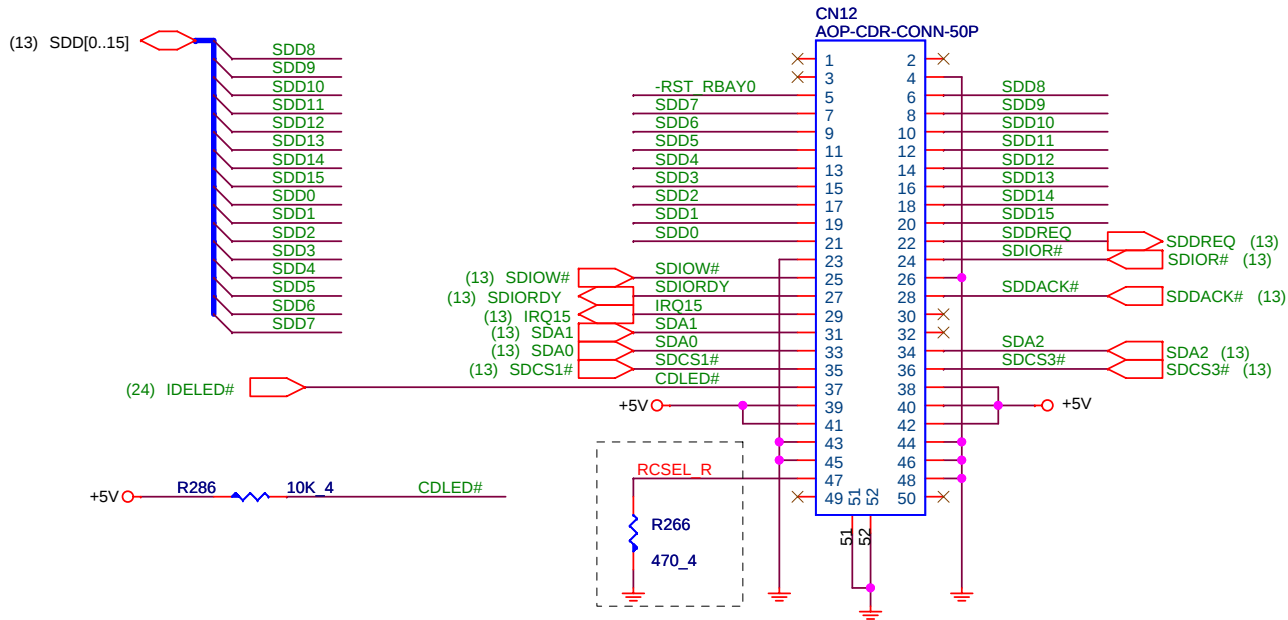
# USB



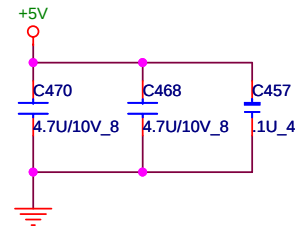
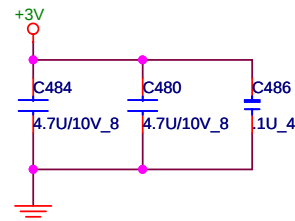
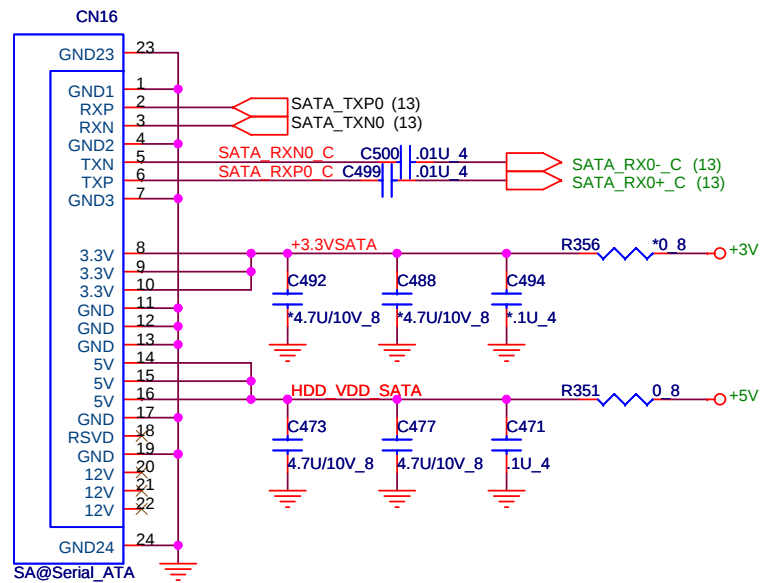
Reserve Common choke for EMI request

|            |                         |                      |          |
|------------|-------------------------|----------------------|----------|
| <OrgName>  |                         | PROJECT : BL3        |          |
| <OrgAddr>  |                         | Quanta Computer Inc. |          |
| <OrgAddr2> |                         |                      |          |
| <OrgAddr3> |                         |                      |          |
| Size       | Document Number         | Rev                  |          |
|            | MINI PCI,USB            | 3B                   |          |
| Date:      | Friday, August 11, 2006 | Sheet                | 17 of 31 |

## ODD CONN



## SATA HDD CONN



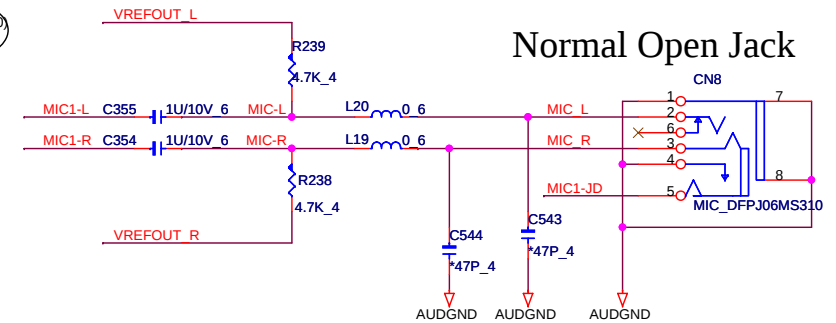
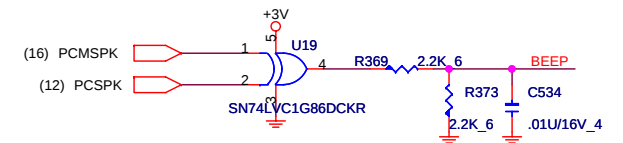
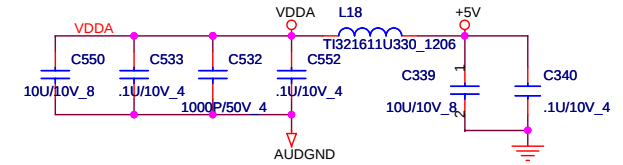
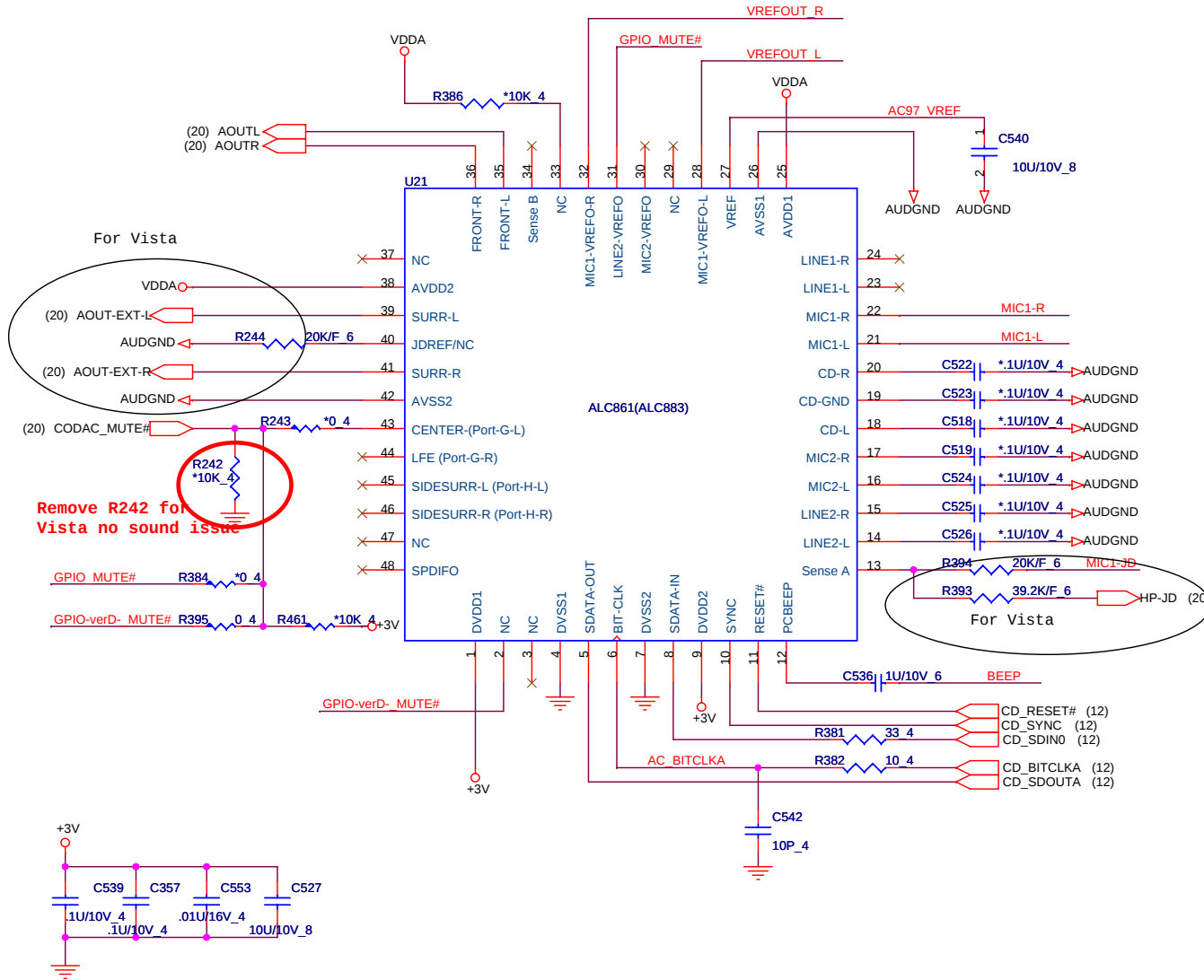
IDE



**PROJECT : BL3**  
**Quanta Computer Inc.**

|       |                          |                |
|-------|--------------------------|----------------|
| Size  | Document Number          | Rev            |
|       | <b>HDD &amp; CDROM</b>   | 3B             |
| Date: | Tuesday, August 08, 2006 | Sheet 18 of 31 |

ADO

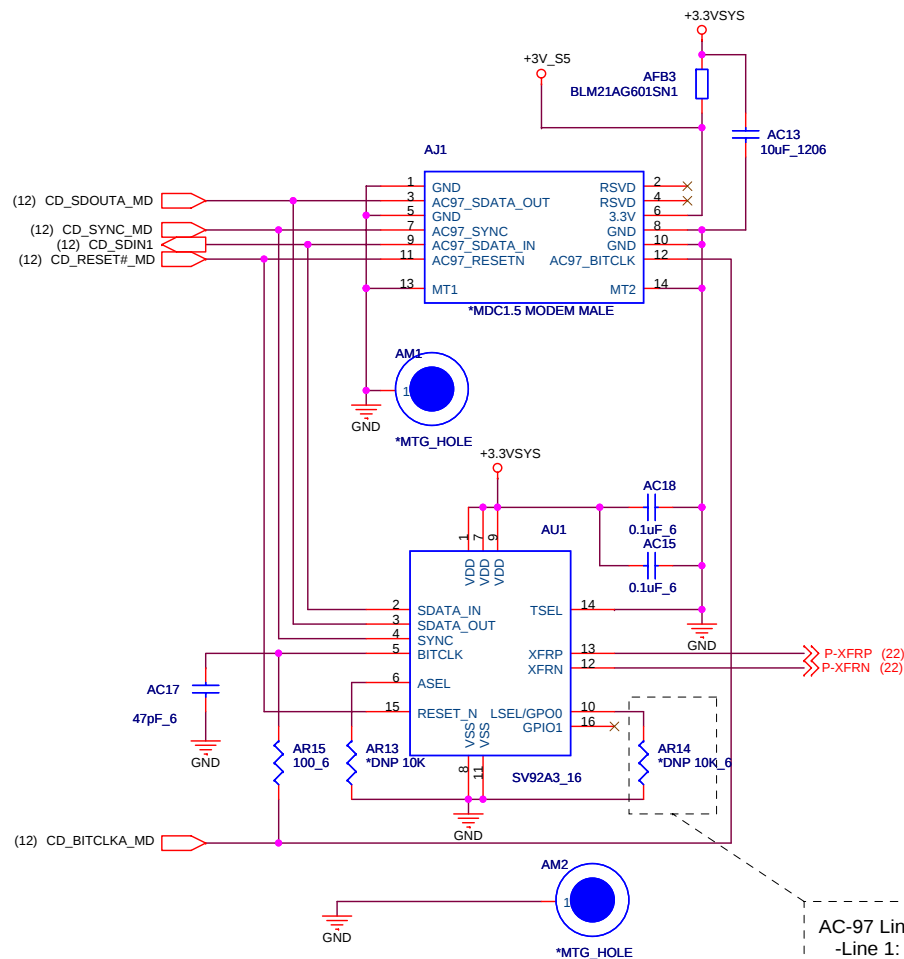


PROJECT : BL3  
Quanta Computer Inc.

|       |                         |                |
|-------|-------------------------|----------------|
| Size  | Document Number         | Rev            |
|       | REALTEK ALC861          | 3B             |
| Date: | Friday, August 11, 2006 | Sheet 19 of 31 |



# MDM

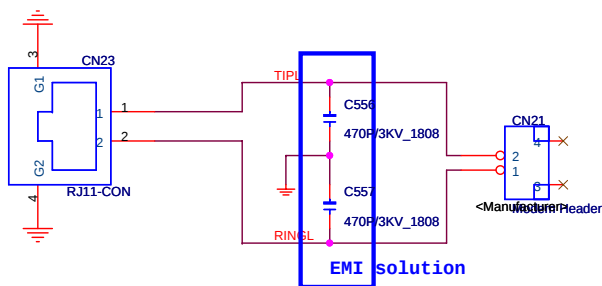


AC-97 Line Select:  
 -Line 1: DNP R14  
 -Line 2:  
 POPULATE R14

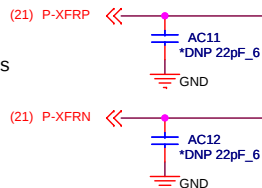


Agere Systems Proprietary  
 DRAFT COPY - FOR REVIEW ONLY  
 SUBJECT TO CHANGE

|                                               |                 |        |
|-----------------------------------------------|-----------------|--------|
| <b>Agere Systems</b><br>Holmdel NJ            |                 |        |
| <b>Design Engineer: C. Russo</b>              |                 |        |
| <b>DELPHI SV92A3 MDC 1.5 Reference Design</b> |                 |        |
| Size B                                        | Document Number | Rev 3B |
| Date: Monday, July 31, 2006                   | Sheet 21 of 31  |        |



Locate C11, C12 as close to digital device as possible.

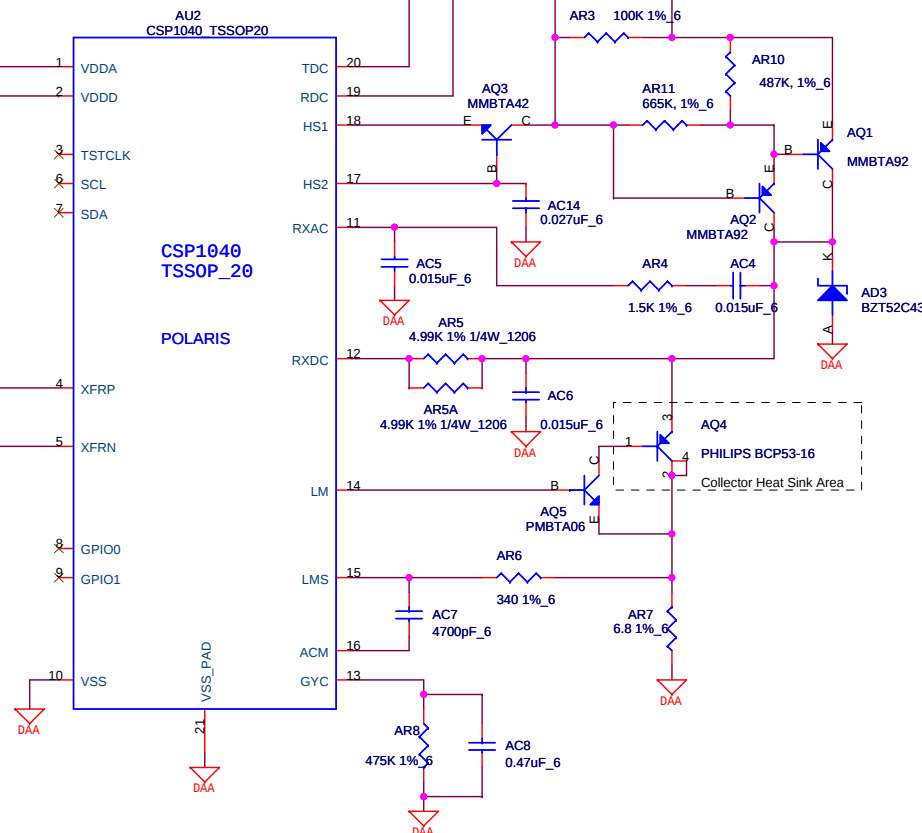


# MDM

## FUSE Note:

The UL standard UL 1950 dictates the use of a fuse (needed to pass the M1, 600 V, 40A, 1.5 sec) to prevent component flaming during the overvoltage test. Unless one can insure that the modem is in a fire enclosure and provide 26 gauge line cord (acts as a fuse), a fusing element would be required.

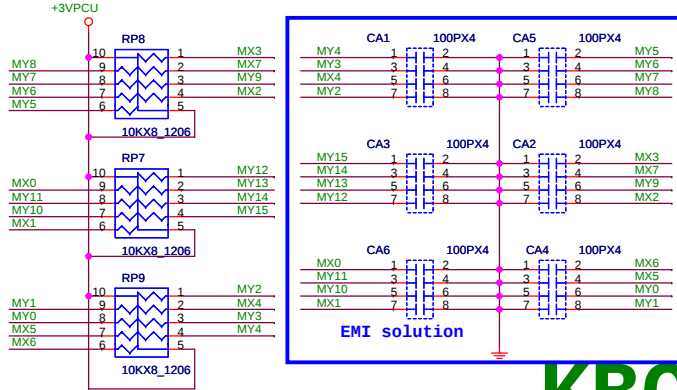
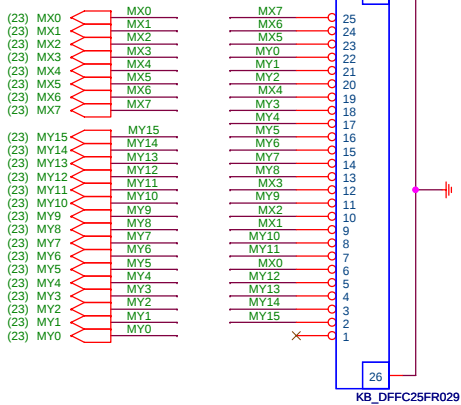
Alternatively, if a TNV-1 flame resistant material is used, either as a wrap or cover over the DAA portion of the modem, this could satisfy both overvoltage protection and the separation requirement also contained in UL 1950. This latter requirement provides isolation such that unearthed parts of the DAA cannot be touched by a test finger or test probe.



|                                               |                                       |        |
|-----------------------------------------------|---------------------------------------|--------|
| <b>Agere Systems</b><br>Holmdel NJ            |                                       |        |
| <b>Design Engineer: R. Trevino</b>            |                                       |        |
| <b>DELPHI SV92A3 MDC 1.5 Reference Design</b> |                                       |        |
| Size B                                        | Document Number<br><b>CSP1040 DAA</b> | Rev 3B |
| Date: Tuesday, August 08, 2006                | Sheet 22 of 31                        |        |

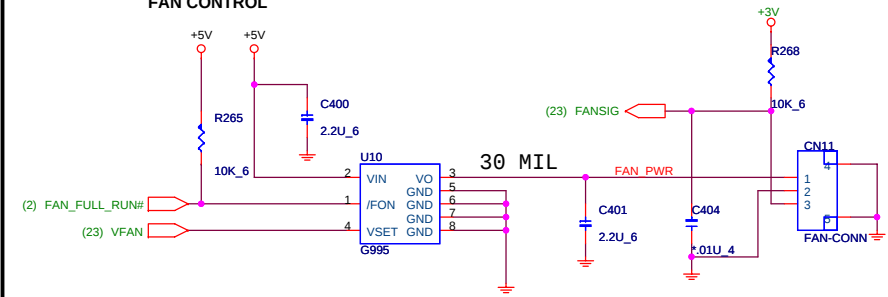
Agere Systems Proprietary  
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SUBJECT TO CHANGE



**INT K/B**

**KBC**

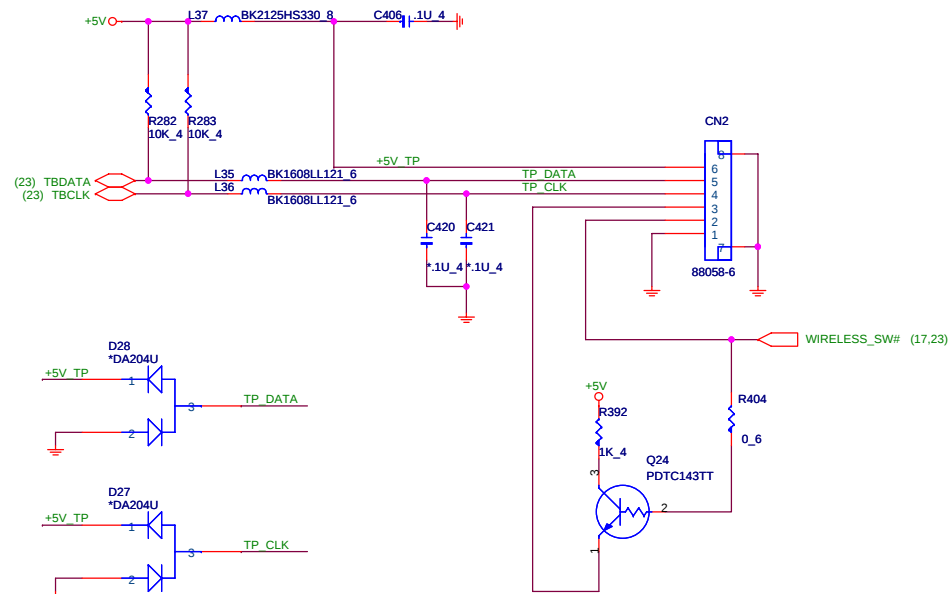
## FAN CONTROL



# THM

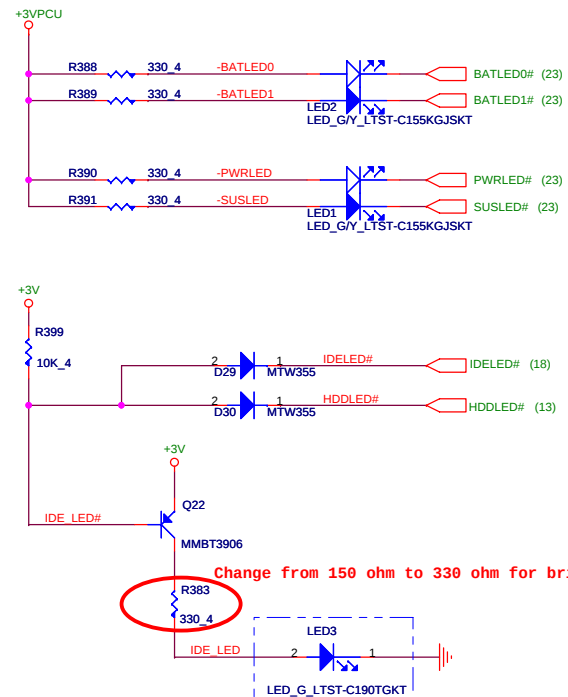
**TOUCH PAD**

20 MIL

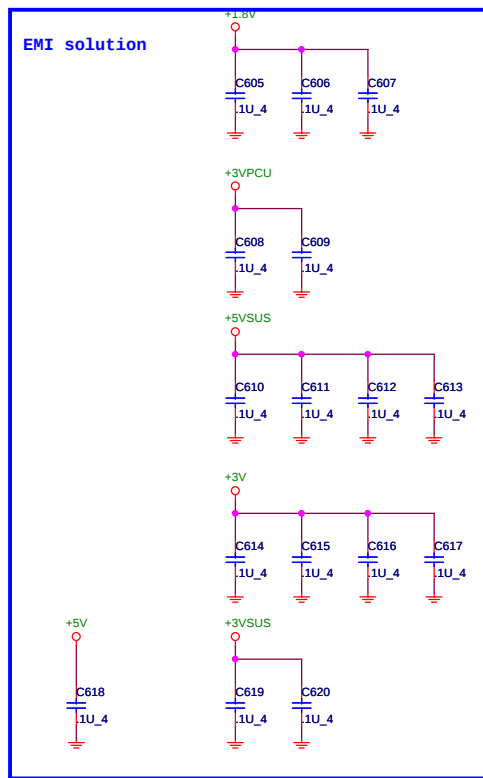


# TPD

# ON BOARD LED

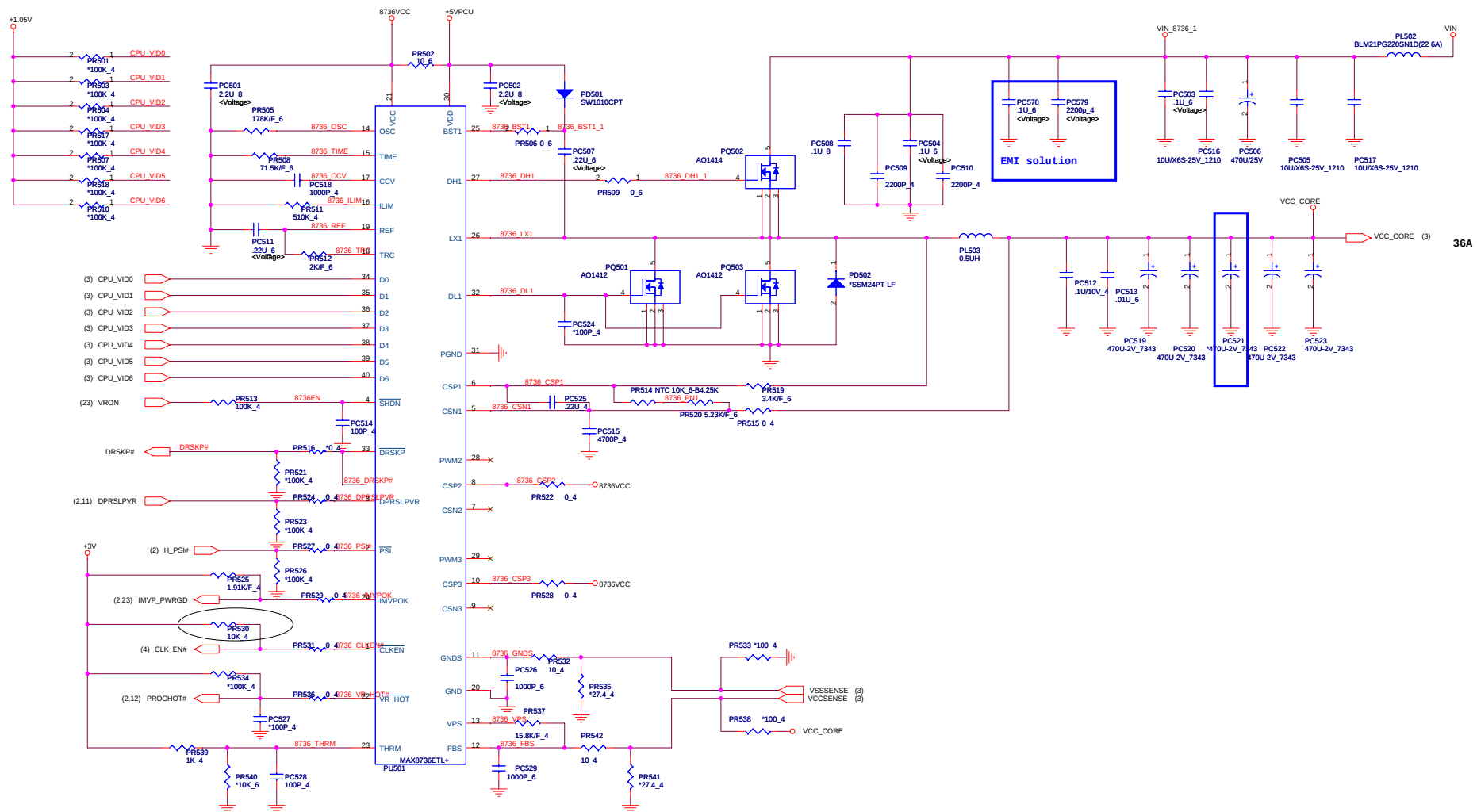


## EMI solution

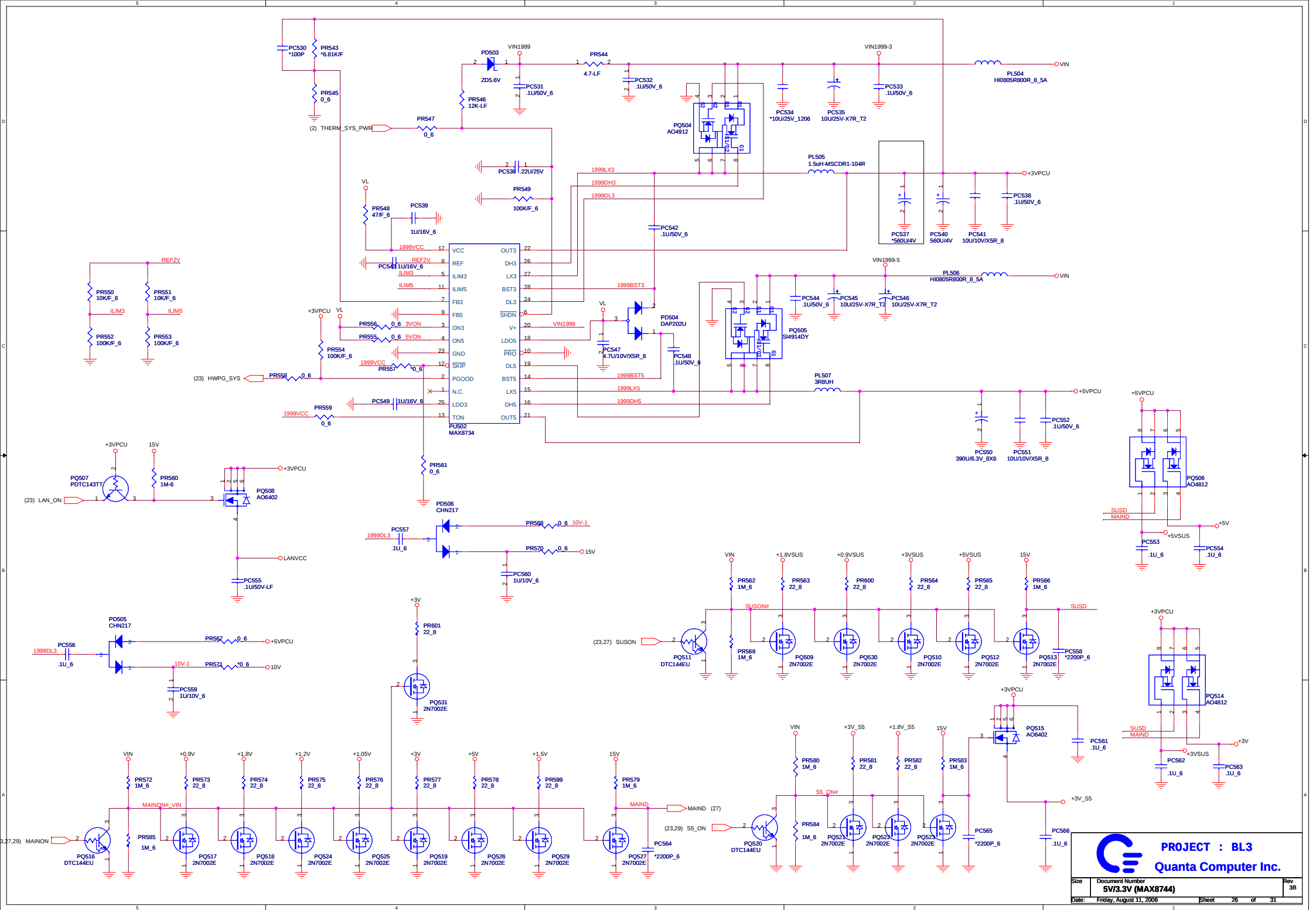


**PROJECT : BL3**  
**Quanta Computer Inc.**

|       |                                                  |                  |
|-------|--------------------------------------------------|------------------|
| Size  | Document Number<br><b>T/P,FAN,SWITCH,LED,K/B</b> | Rev<br><b>3B</b> |
| Date: | Friday, August 11, 2006                          | Sheet 24 of 31   |

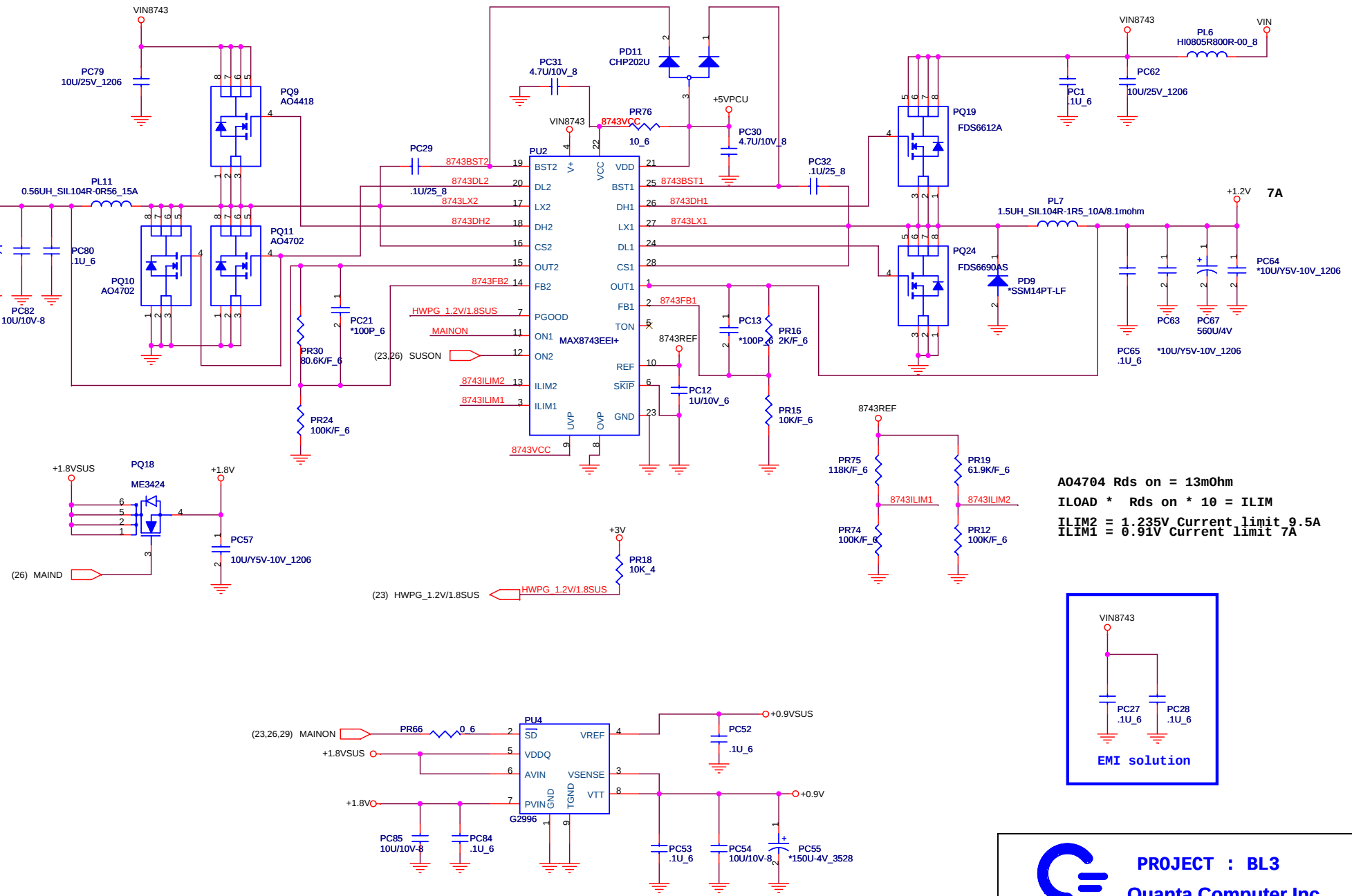


# CPU CORE

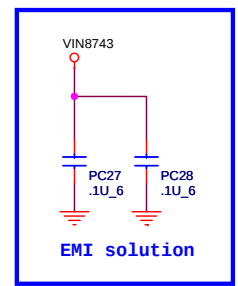


PROJECT : BL3  
Quanta Computer Inc.

# DCD



A04704 Rds on = 13mOhm  
 ILOAD \* Rds on \* 10 = ILIM  
 ILIM2 = 1.235V Current limit 9.5A  
 ILIM1 = 0.91V Current limit 7A



**PROJECT : BL3**  
**Quanta Computer Inc.**

|       |                          |                |
|-------|--------------------------|----------------|
| Size  | Document Number          | Rev            |
|       | <b>+1.8/1.2V / VTT</b>   | 3B             |
| Date: | Tuesday, August 08, 2006 | Sheet 27 of 31 |

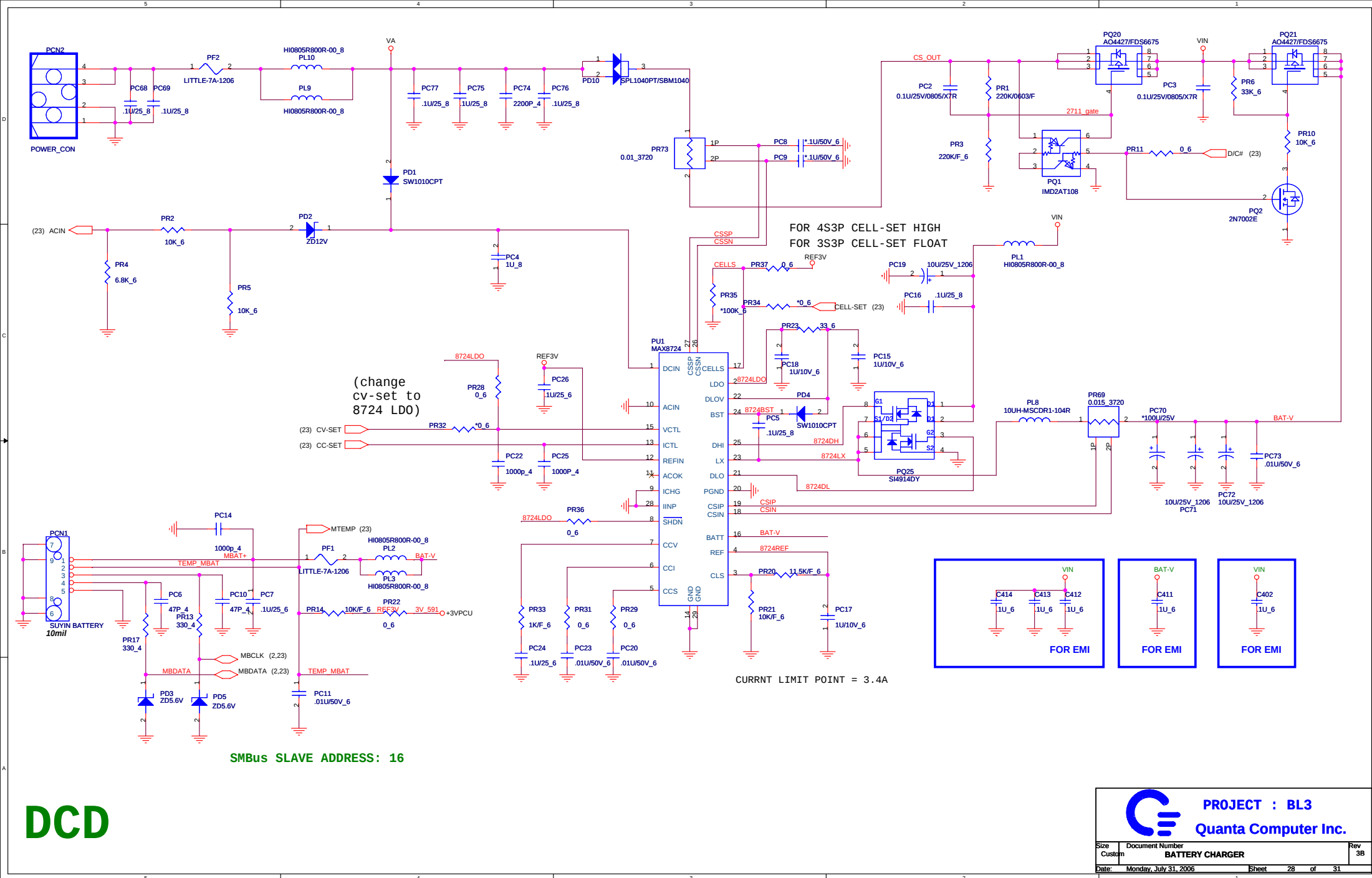
DCD

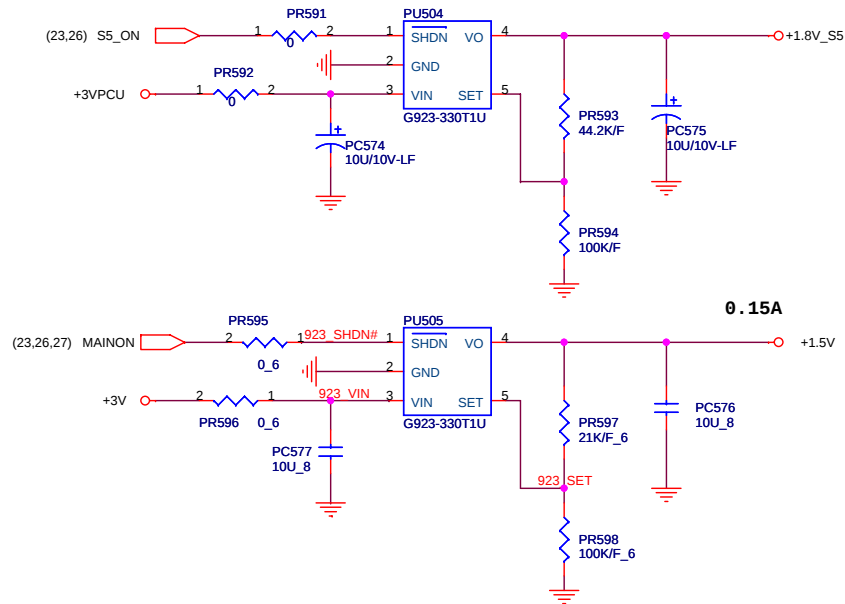
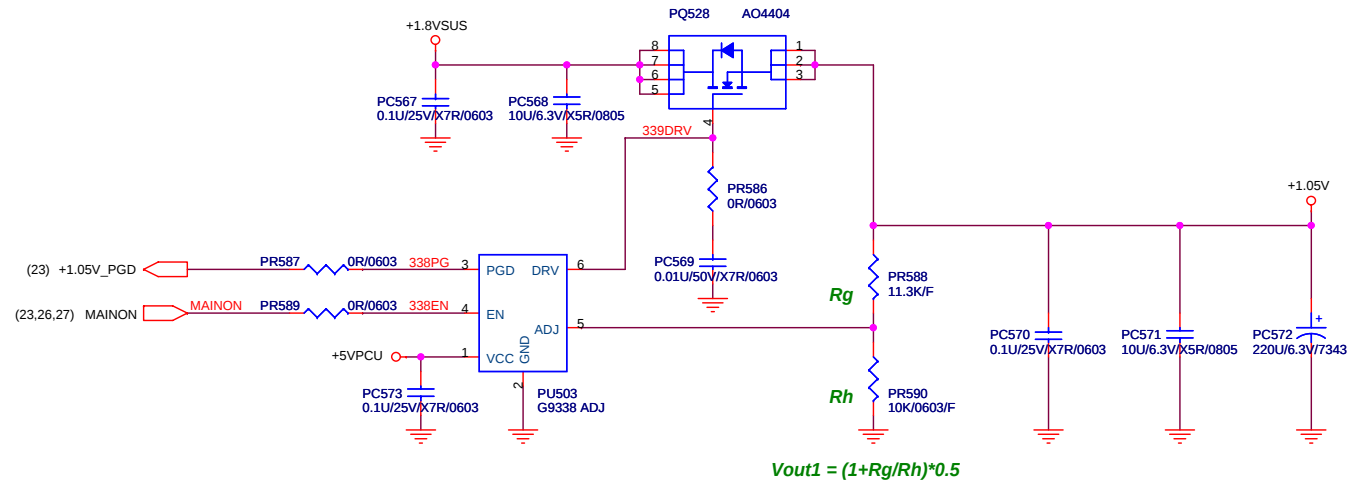
SMBus SLAVE ADDRESS: 16

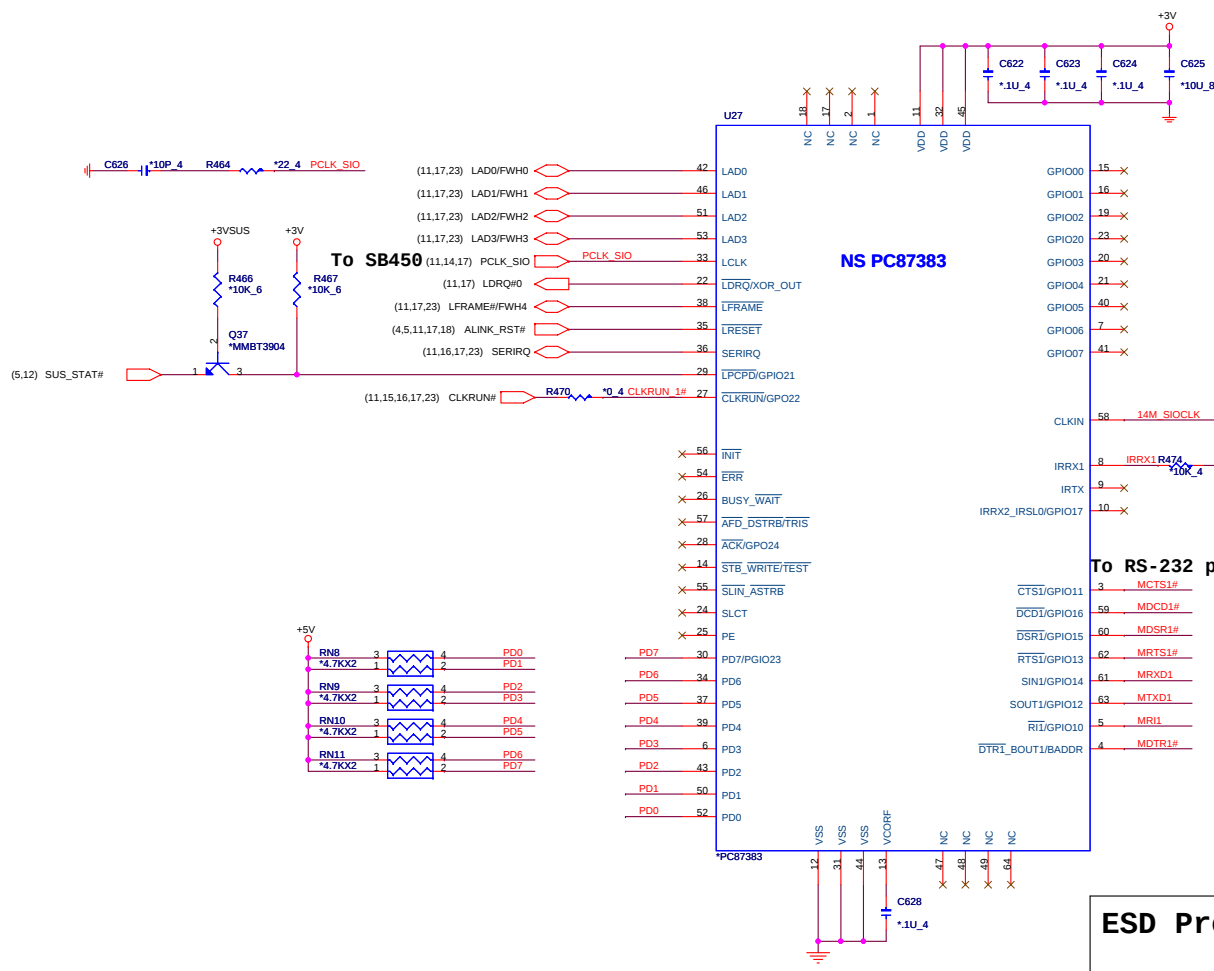


PROJECT : BL3  
Quanta Computer Inc.

|        |                       |                |
|--------|-----------------------|----------------|
| Size   | Document Number       | Rev            |
| Custom | BATTERY CHARGER       | 3B             |
| Date:  | Monday, July 31, 2006 | Sheet 28 of 31 |







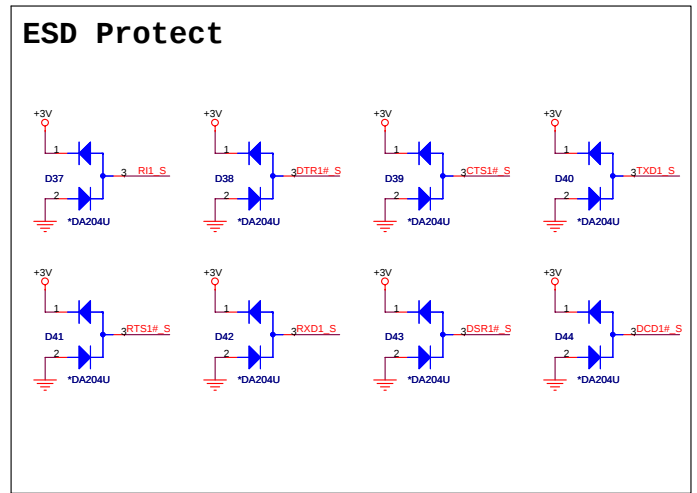
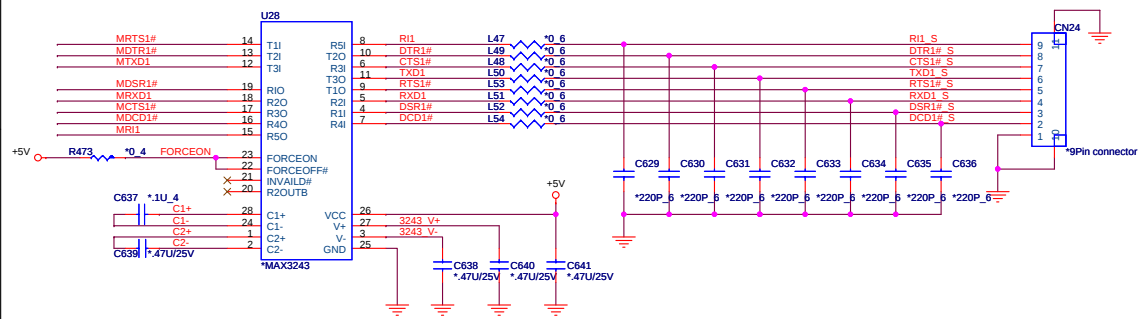
To SB450

NS PC87383

To Clock gen.

To RS-232 port

**STRAP PINS**  
 NC==>the index-data pair at 164Eh to 164Fh  
 PD==>the index-data pair at 2Eh to 2Fh



**SIO**