TE1M Block Diagram

VER : E3D

BOM P/N	Description
31TE1MB0010	TE1M MB(PM45/RB/MS)WO CPU
31TE1MB0120	TE1M MB(PM45/MAIN/RB/HDMI/CIR)WO CPU
31TE1MB0130	TE1M MB(GM45/EXP/NO CIR/MS)WO CPU
31TE1MB0140	TE1M MB(GM45/GS/EXP/MS)WO CPU
31TE1MB0170	TE1M MB(GM45/GS/EXP/LC)WO CPU
31TE1MB01N0	TE1M MB(GM45/HDMI/EXP/MS)WO CPU
31TE1MB01M0	TE1M MB(GM45/HDMI/GS/CIR/MS)WO CPU
31TE1MB01P0	TE1M MB ASY(GL40/PC/GS/FE/HD/KI,MS)WOCPU
31TE1MB01Q0	TE1M MB ASY(GM45/PC/GS/FE/HD/KI,MS)WOCPU
31TE1MB01S0	TE1M MB(PM45/HDMI/NO CIR/MS)WO CPU

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND1
- LAYER 3 : IN1
- LAYER 4 : VCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND2
- LAYER 8 : BOT

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA

PENRYN 478P uFCPGA — FSB P3,4

FSB(667/800/1066MHZ)

CANTIGA NB P5,7,8,9,10,11 — FSB, PCI-E, DMI, DDR SYSTEM MEMORY, Graphics Interfaces

DMI(x2/x4)

Intel I/O Controller Hub 9 (ICH9M) NB — RTC P12, 13, 14, 15

DDRII-SODIMM1 / DDRII-SODIMM2 P16,17 — Dual Channel DDR II 667/800 MHZ

Azalia — VGA Con. (FOX) P18 — EXT_CRT, EXT_LVDS, EXT_HDMI

PCI-E x16 / PCIE — PI3VDP411LST HDMI level shift P21 — INT_HDMI

INT_CRT, INT_LVDS

I2C — R5F211A4SP CEC P21 — CEC_I2C

SWITCH CIRCUIT — USB-3

CRT Con. P20

LCD/CCD Con. P19

LED/CCD Con. P19

HDMI Con. P21

SATA - HDD P22

SATA - ODD P22

SATA 0, SATA 1, SATA 4

PI2EQX3201B Re-driver P27

USB/ESATA P27 — USB-7

Finger Printer (FTB) P26 — USB-1

Bluetooth Con. P26 — USB-2

Felica Con. (FTB) P26 — USB-4

USB Port P27 — USB-6

USB 2.0 (Port0~9)

BATTERY P12

W25X16VSS1G SPI FLASH P13 — SPI

MDC Con. P30 — Azalia

PCI-Express

PCIE-1 — USB-9 — NEW CARD Con. P27

PCIE-2 — MINI CARD-3 U 9H_HD-DVD P25

PCIE-3 — USB-8 — MINI CARD-2 U 5.6H_TV/ROBSON D 7.5H_HD-DVD P25

PCIE-4 — MINI CARD-4 (FTB) D ROBSON P25

PCIE-5 — USB-0 — Port-C (FM) — LAN/ USB/ FM Con. P26

PCIE-6 — USB-5 — MINI CARD-1 U&D 5.6H_WLAN P25

PCI Bus

CB1410 PCMCIA Controller P23 — PCMCIA SOCKET P23

OZ129T Cardreader/1394 Controller P24 — Cardreader Con. 5 IN 1 P24 — 1394 Con. P24

LPC

CX20561-12Z AUDIO CODEC P29

INT_ MIC P19

INT_ MIC P29

Port-C (FM) — Port-B — Port-A

MIC JACK P30 — HP AMP P30 — SPK AMP P29

FM P29 — HP/SPDIF P30 — SPK Con. P29

WPC8763LDG EC P28

VR P30 — Kill SW P27 — CIR P28 — LIS3L02AQ3 G-Sensor P22 — MMB Board Con. P26 — Touch Pad Board Con. P26 — Power Board Con. P26

FAN P3 — K/B Con. P26 — W25X16VSS1G SPI FLASH P28 — EC2648 HALL SENSOR P19 — Low Cost Board Con. P26 — LED Board Con. P26

ICS9LPR365 CK505 CLOCK GENERATOR P2

POWER SYSTEM
ISL88731 P31
ISL6237 P32
ISL6266A P33
RT8202 P34
TPS51116 P35
APL5913 P36
G909 P36
LED POWER DRIVER
ISL97636 P19

VCC_CORE

+1.5V

+1.05V

+1.8VSUS
+1.8V

+1.5V_S5
+3VPCU
+3V_S5
+3VSUS
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF

Quanta Computer Inc.
PROJECT : TE1M

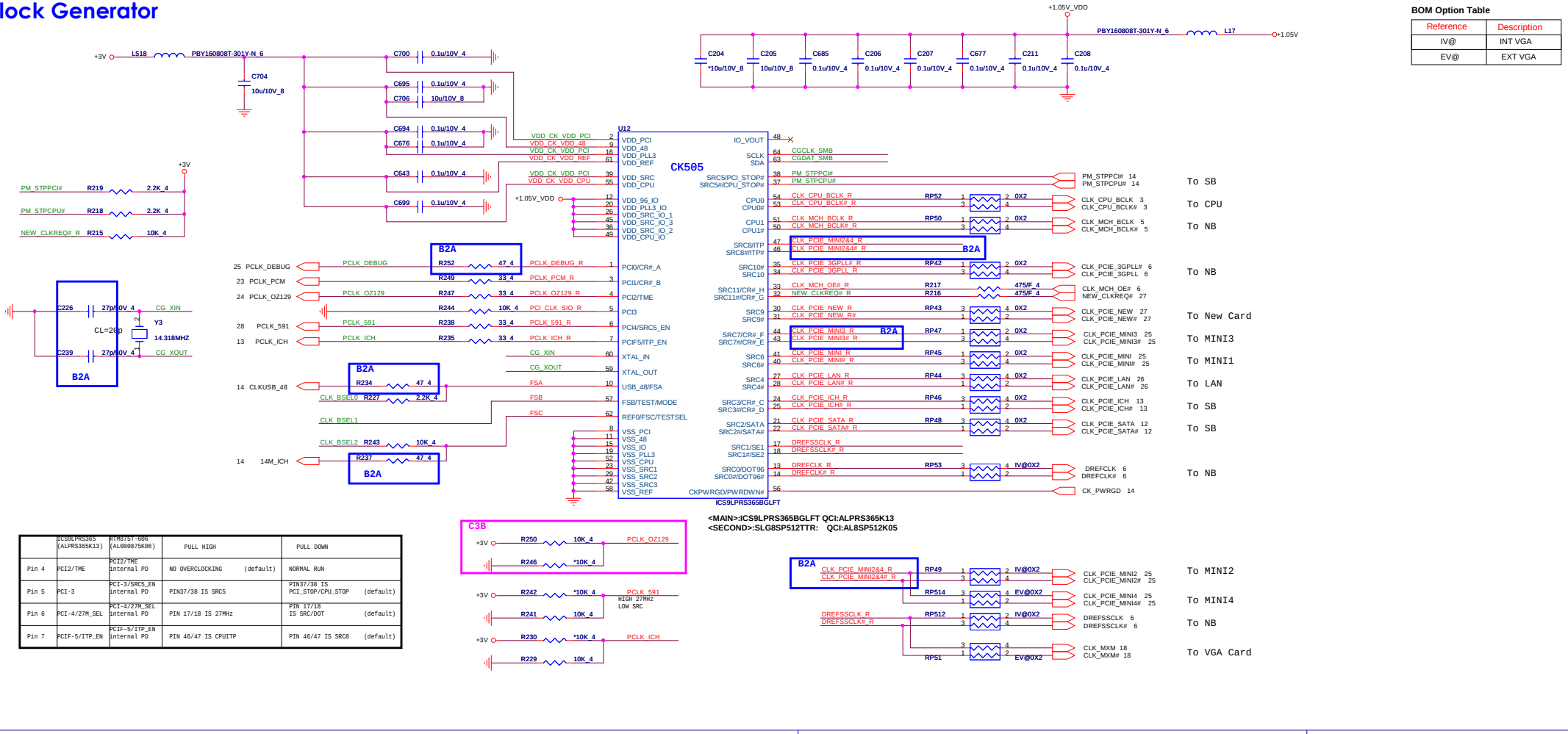
Size	Document Number	Rev
	Block Diagram	E3D

Date: Monday, May 26, 2008 Sheet 1 of 40

Clock Generator

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA

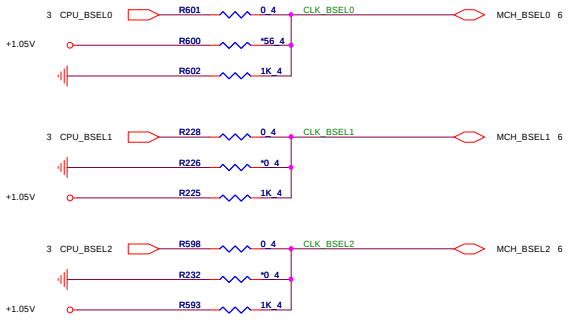


	ICS9LPRS365 (ALPRS365K13)	XTM0757-000 (AL000075K06)	PULL HIGH	PULL DOWN
Pin 4	PCI2/TME	PCI2/TME internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 5	PCI-3	PCI-3/SRC5_EN internal PD	PIN37/38 IS SRC5	PIN37/38 IS PCI_STOP/CPU_STOP (default)
Pin 6	PCI-4/27M_SEL	PCI-4/27M_SEL internal PD	PIN 17/18 IS 27MHz	PIN 17/18 IS SRC/DOT (default)
Pin 7	PCIF-5/ITP_EN	PCIF-5/ITP_EN internal PD	PIN 46/47 IS CPUITP	PIN 46/47 IS SRC8 (default)

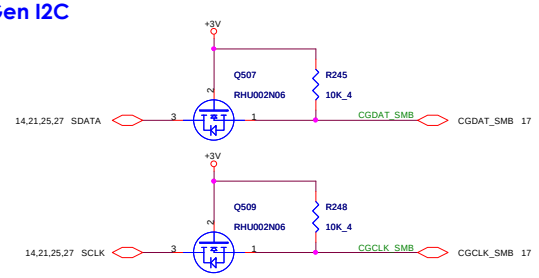
FREQ. SEL TABLE

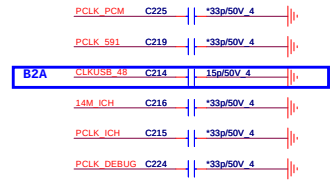
BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



Clock Gen I2C





Quanta Computer Inc.
PROJECT : TE1M

Size	Document Number	Rev
	Clock Gen	E3D

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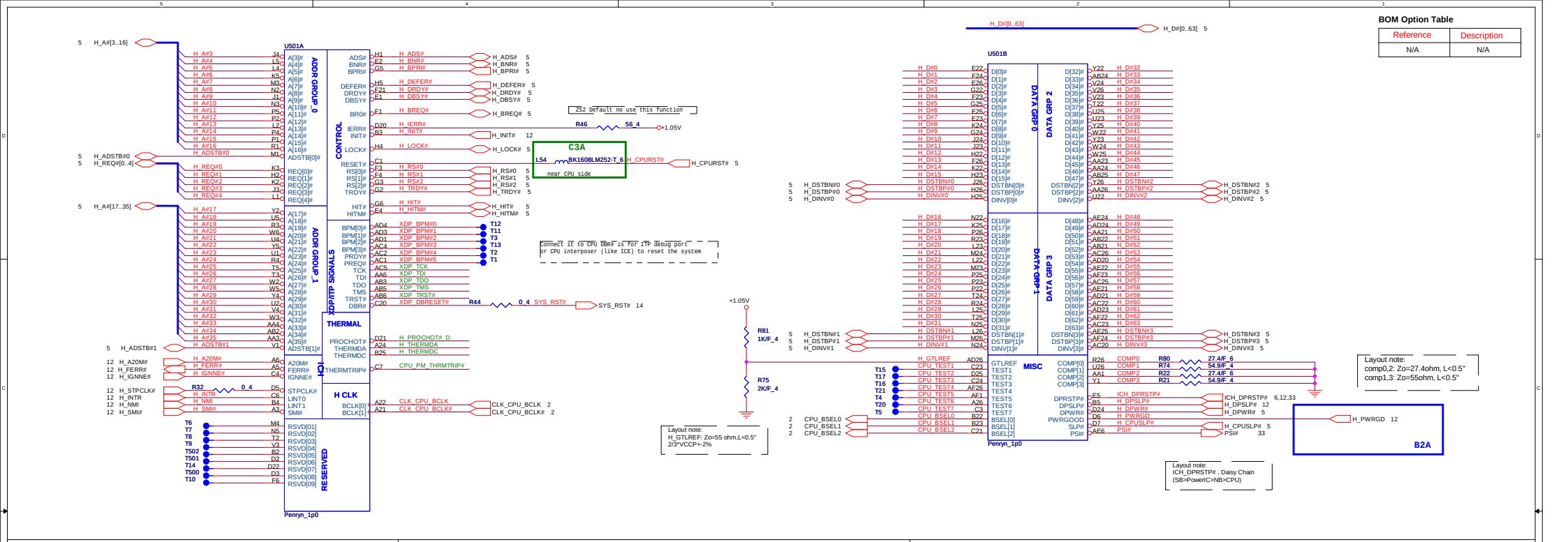
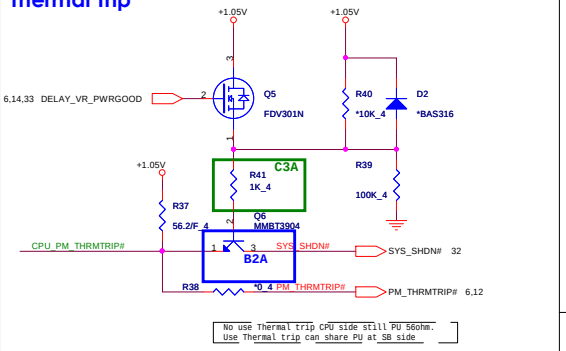
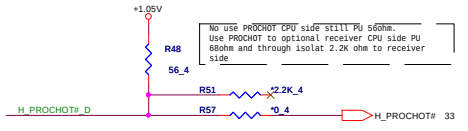


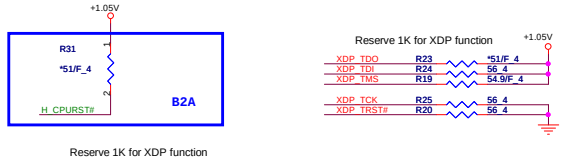
Thermal Trip



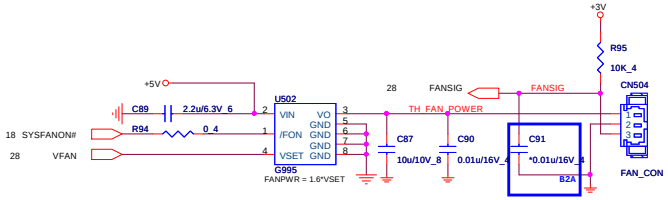
Processor hot



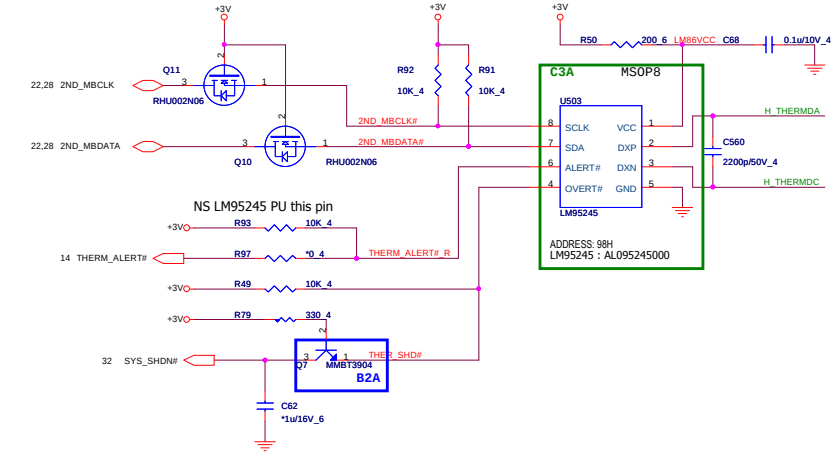
XDP



CPU FAN CTRL



CPU Thermal monitor

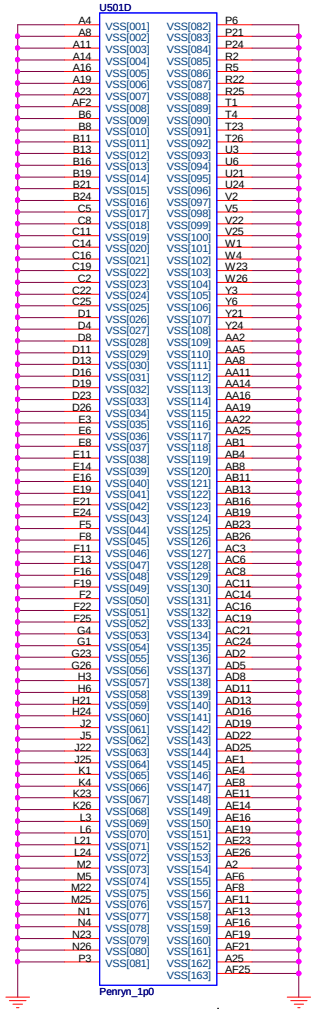


Quanta Computer Inc.		
PROJECT : TE1M		
Size	Document Number: CPU(1/2)- Host Bus	Rev: E3D
Date: Monday, May 26, 2008	Sheet 3 of 40	

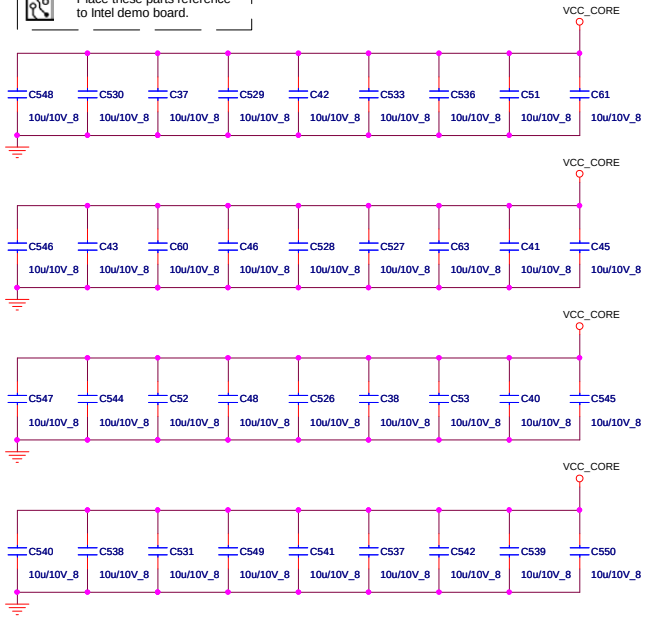
BOM Option Table

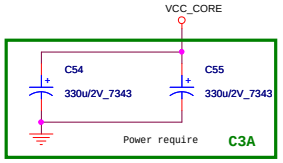
Reference	Description
N/A	N/A

Need NC 20PCS 10u before A1 BOM released(A0 all stuff)

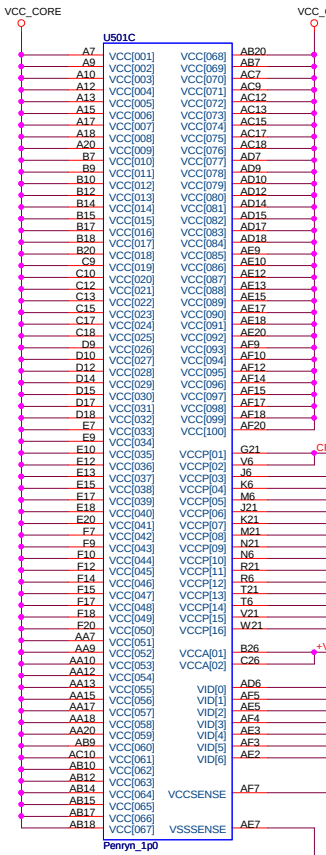


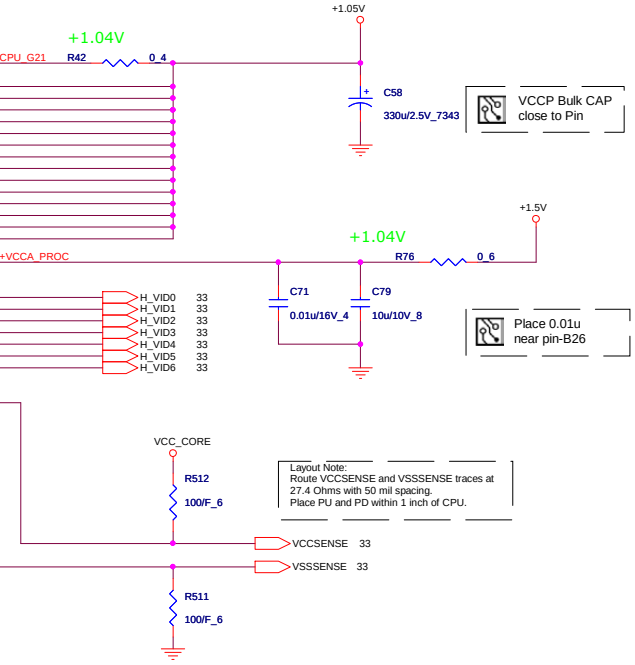
Place these parts reference to Intel demo board.



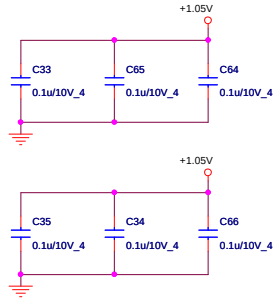


VCC_CORE Bulk CAPs place to BOT of CPU centeral





Layout Note:
Inside CPU center cavity in 2 rows



VCCP Bulk CAP close to Pin

Place 0.01u near pin-B26

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.

Penryn CPU Power Status and max current table

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC_CORE	O	X	X	VID	47A	Standard Voltage CPU
VCC_CORE	O	X	X	VID	50A	SV Design Target
VCC_CORE	O	X	X	VID	TBD	Extreme Edition CPU
VCC_CORE	O	X	X	VID	67A	EE Design Target
VCCA	O	X	X	+1.5V	130mA	
VCCP	O	X	X	+1.05V	4.5A	Before VCC Stable
VCCP	O	X	X	+1.05V	2.5A	After VCC Stable

(See Penryn EMTS Rev:1.0 Table7,8 for voltage and current)

(See Penryn EMTS Rev:1.0 Table-3 for VID table)

Quanta Computer Inc.
PROJECT : TE1M

Size	Document Number	Rev
	CPU(2/2)- Power	E3D

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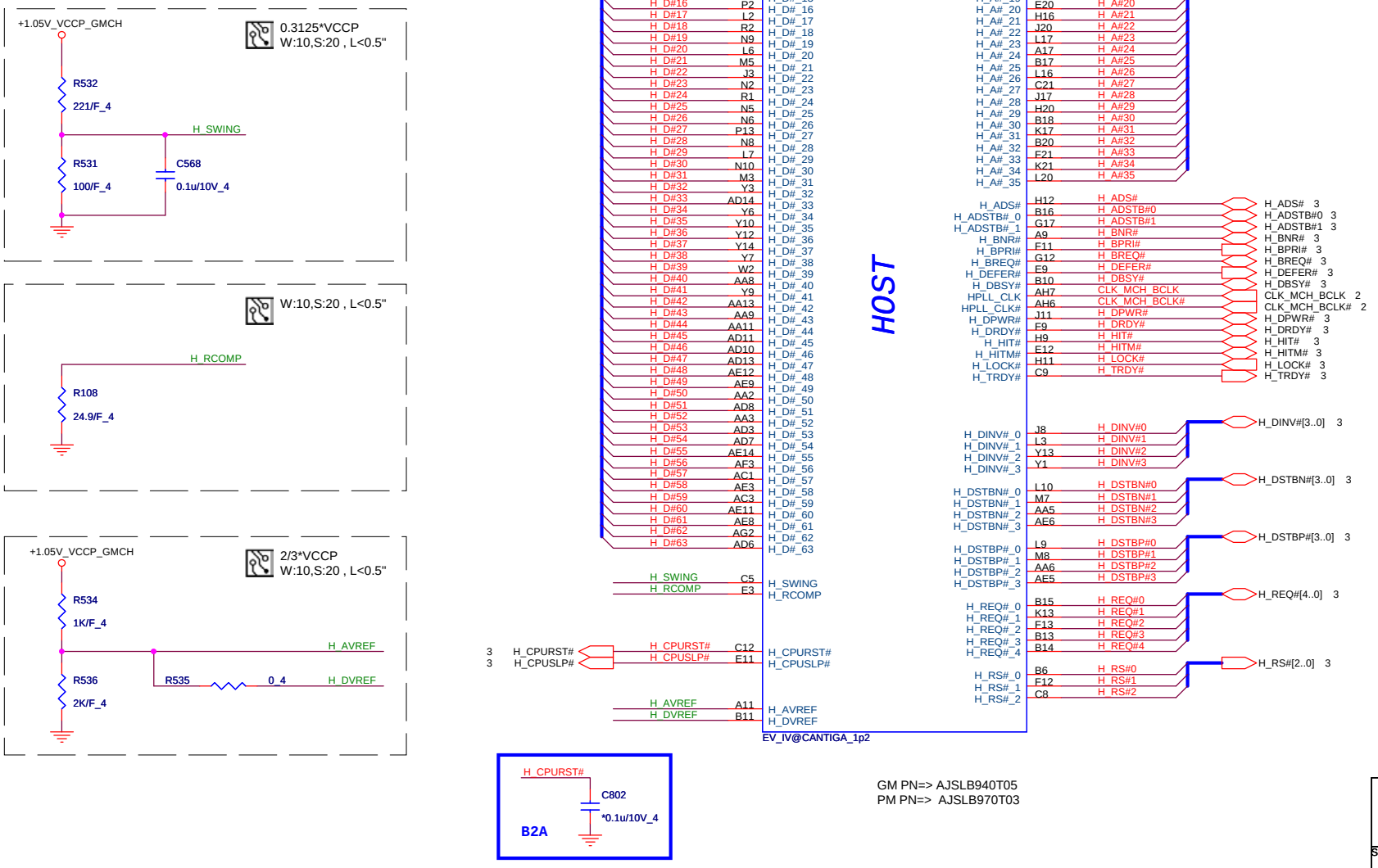
BOM Option Table

Reference	Description
EV_IV@	EV&IV diff. BOM



GM PN=> AJSLB940T05
PM PN=> AJSLB970T03

Quanta Computer Inc.

PROJECT : TE1M

Size	Document Number	Rev
	NB (1/7)- HOST	E3D
Date: Monday, May 26, 2008	Sheet 5 of 40	

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA
IHM@	INT HDMI
EV_IV@	EV&IV diff. BOM

GM PN=> AJSLB940T05
PM PN=> AJSLB970T03

U504B

RSVD / DDR CLK / CONTROL/COMPENSATION

MCH_RSVD1 M36 RSVD1
MCH_RSVD2 N36 RSVD2
MCH_RSVD3 R33 RSVD3
MCH_RSVD4 T33 RSVD4
MCH_RSVD5 AH9 RSVD5
MCH_RSVD6 AH10 RSVD6
MCH_RSVD7 AH12 RSVD7
MCH_RSVD8 AH13 RSVD8
MCH_RSVD9 K12 RSVD9
MCH_RSVD14 T24 RSVD14
MCH_RSVD15 B31 RSVD15
MCH_RSVD17 M1 RSVD17
MCH_RSVD20 AY21 RSVD20
MCH_RSVD21 B2 RSVD21
MCH_RSVD22 BG23 RSVD22
MCH_RSVD23 BF23 RSVD23
MCH_RSVD24 BH18 RSVD24
MCH_RSVD25 BF18 RSVD25

SA_CK_0 AP24 M_CLK_DDR0 → M_CLK_DDR0 17
SA_CK_1 AT21 M_CLK_DDR1 → M_CLK_DDR1 17
SB_CK_0 AV24 M_CLK_DDR3 → M_CLK_DDR3 17
SB_CK_1 AV20 M_CLK_DDR4 → M_CLK_DDR4 17
SA_CK#_0 AP24 M_CLK_DDR#0 → M_CLK_DDR#0 17
SA_CK#_1 AR21 M_CLK_DDR#1 → M_CLK_DDR#1 17
SB_CK#_0 AU24 M_CLK_DDR#3 → M_CLK_DDR#3 17
SB_CK#_1 AV20 M_CLK_DDR#4 → M_CLK_DDR#4 17
SA_CKE_0 BC28 M_CKE0 → M_CKE0 16,17
SA_CKE_1 AY28 M_CKE1 → M_CKE1 16,17
SB_CKE_0 AY36 M_CKE3 → M_CKE3 16,17
SB_CKE_1 BB36 M_CKE4 → M_CKE4 16,17
SA_CS#_0 BA17 M_CS#0 → M_CS#0 16,17
SA_CS#_1 AY16 M_CS#1 → M_CS#1 16,17
SB_CS#_0 AV16 M_CS#2 → M_CS#2 16,17
SB_CS#_1 AR13 M_CS#3 → M_CS#3 16,17
SA_ODT_0 BD17 M_ODT0 → M_ODT0 16,17
SA_ODT_1 AY17 M_ODT1 → M_ODT1 16,17
SB_ODT_0 BF15 M_ODT2 → M_ODT2 16,17
SB_ODT_1 AY13 M_ODT3 → M_ODT3 16,17
SM_RCOMP BG22 M_RCOMP
SM_RCOMP# BH21 M_RCOMP#
SM_RCOMP_VOH BF28 SM_RCOMP_VOH
SM_RCOMP_VOL BH28 SM_RCOMP_VOL
SM_VREF AV42 SM_VREF
SM_PWROK AR36 SM_PWROK
SM_REXT BF17 SM_REXT
SM_DRAMRST# BC36 MCH_SM_DRAMRST# → T77
SM_DRAMRST# only for DDR3 (DDR2 NC)

DPLL_REF_CLK B38 DREFCLK → DREFCLK 2
DPLL_REF_CLK# A38 DREFCLK# → DREFCLK# 2
DPLL_REF_SSCLK E41 DREFSSCLK → DREFSSCLK 2
DPLL_REF_SSCLK# F41 DREFSSCLK# → DREFSSCLK# 2

JTAG / CLK

PEG_CLK F43 CLK_PCIE_3GPLL → CLK_PCIE_3GPLL 2
PEG_CLK# E43 CLK_PCIE_3GPLL# → CLK_PCIE_3GPLL# 2
JTAG_TCK AL34 ME_JTAG_TCK
JTAG_TDI AK34 ME_JTAG_TDI
JTAG_TDO AN35 ME_JTAG_TDO
JTAG_TMS AM35 ME_JTAG_TMS

DMI

DMI_RXN_0 AE41 DMI_TXN0
DMI_RXN_1 AE37 DMI_TXN1
DMI_RXN_2 AE47 DMI_TXN2
DMI_RXN_3 AH39 DMI_TXN3 → DMI_TXN[3:0] 13
DMI_RXP_0 AE40 DMI_TXP0
DMI_RXP_1 AE38 DMI_TXP1
DMI_RXP_2 AE48 DMI_TXP2
DMI_RXP_3 AH40 DMI_TXP3 → DMI_TXP[3:0] 13
DMI_TXN_0 AE35 DMI_RXN0
DMI_TXN_1 AE43 DMI_RXN1
DMI_TXN_2 AE46 DMI_RXN2
DMI_TXN_3 AH42 DMI_RXN3 → DMI_RXN[3:0] 13
DMI_TXP_0 AD35 DMI_RXP0
DMI_TXP_1 AE44 DMI_RXP1
DMI_TXP_2 AF46 DMI_RXP2
DMI_TXP_3 AH43 DMI_RXP3 → DMI_RXP[3:0] 13

CFG

2 MCH_BSEL0 → MCH_BSEL0 T25 → CFG_0
2 MCH_BSEL1 → MCH_BSEL1 R25 → CFG_1
2 MCH_BSEL2 → MCH_BSEL2 P25 → CFG_2
MCH_CFG_3 P20 CFG_3
T46 MCH_CFG_4 P24 CFG_4
T58
11 MCH_CFG_5 → MCH_CFG_5 C25 → CFG_5
11 MCH_CFG_6 → MCH_CFG_6 N24 → CFG_6
11 MCH_CFG_7 → MCH_CFG_7 M24 → CFG_7
T48 MCH_CFG_8 F21 CFG_8
11 MCH_CFG_9 → MCH_CFG_9 C23 → CFG_9
11 MCH_CFG_10 → MCH_CFG_10 C24 → CFG_10
T45 MCH_CFG_11 N21 CFG_11
11 MCH_CFG_12 → MCH_CFG_12 P21 → CFG_12
11 MCH_CFG_13 → MCH_CFG_13 T21 → CFG_13
T47 MCH_CFG_14 R20 CFG_14
T44 MCH_CFG_15 M20 CFG_15
11 MCH_CFG_16 → MCH_CFG_16 L21 → CFG_16
MCH_CFG_17 H21 CFG_17
T49 MCH_CFG_18 P29 CFG_18
T59
11 MCH_CFG_19 → MCH_CFG_19 R28 → CFG_19
11 MCH_CFG_20 → MCH_CFG_20 T28 → CFG_20

GRAPHICS VID

GFX_VID_0 B33
GFX_VID_1 B32
GFX_VID_2 G33
GFX_VID_3 F33
GFX_VID_4 E33
GFX_VR_EN C34

PM

14 PM_SYNC# R126 0_4 PM_SYNC# R R29 → PM_SYNC#
3,12,33 ICH_DPRSTP# R533 0_4 ICH_DPRSTP# R B7 → PM_DPRSTP#
17 PM_EXTTS#0 R183 0_4 PM_EXTTS#0 1_EC R N33 → PM_EXT_TS#_0
17 PM_EXTTS#1 R178 0_4 TSRDIMM0_1 R F32 → PM_EXT_TS#_1
R207 0_4 AT40 → PWROK
3,14,33 DELAY_VR_PWRGOOD R114 100_4 RST_IN# MCH AT11 → RSTIN#
13 PLT_RST#_NB R120 *0_4 THRMTRIP# R T20 → THERMTRIP#
3,12 PM_THRMTRIP# R138 0_4 DPRSLPVR R R32 → DPRSLPVR
14,33 PM_DPRSLPVR

NB Thermal trip pin
No use Thermal trip NB side can NC.(NB has ODT)

PM_DPRSTP#
The Daisy chain topology should be routed from ICH9M to MVP , then to (G)MCH and CPU, in that order.

MISC / NC

TP_MCH_NC1 BG48 NC_1
TP_MCH_NC2 BF48 NC_2
TP_MCH_NC3 BD48 NC_3
TP_MCH_NC4 BC48 NC_4
TP_MCH_NC5 BH47 NC_5
TP_MCH_NC6 BG47 NC_6
TP_MCH_NC7 BE47 NC_7
TP_MCH_NC8 BH46 NC_8
TP_MCH_NC9 BF46 NC_9
TP_MCH_NC10 BC45 NC_10
TP_MCH_NC11 BH44 NC_11
TP_MCH_NC12 BH43 NC_12
TP_MCH_NC13 BH6 NC_13
TP_MCH_NC14 BH5 NC_14
TP_MCH_NC15 BG4 NC_15
TP_MCH_NC16 BH3 NC_16
TP_MCH_NC17 BF3 NC_17
TP_MCH_NC18 BH2 NC_18
TP_MCH_NC19 BG2 NC_19
TP_MCH_NC20 BE2 NC_20
TP_MCH_NC21 BG1 NC_21
TP_MCH_NC22 BF1 NC_22
TP_MCH_NC23 BD1 NC_23
TP_MCH_NC24 BC1 NC_24
TP_MCH_NC25 F1 NC_25

CL_CLK AH37 CL_CLK0 → CL_CLK0 14
CL_DATA AH36 CL_DATA0 → CL_DATA0 14
CL_PWROK AN36 MPWROK → MPWROK 14
CL_RST# AJ35 CL_RST# → CL_RST# 14
CL_VREF AH34 MCH_CLVREF_R

DDPC_CTRLCLK N28 DDPC_CTRLCLK → T57
DDPC_CTRLDATA M28 DDPC_CTRLDATA → DDPC_CTRLDATA 11
SDVO_CTRLCLK G36 SDVO_CTRLCLK → SDVO_CTRLCLK 21
SDVO_CTRLDATA E36 SDVO_CTRLDATA → SDVO_CTRLDATA 11,21
CLKREQ# K36 CLK_MCH_OE# → CLK_MCH_OE# 2
ICH_SYNC# H36 MCH_ICH_SYNC# → MCH_ICH_SYNC# 14
DDPC_CTRL for HDMI port C
SDVO_CTRL for HDMI port B

TSATN# B12 TSATN#

HDA

HDA_BCLK B28 HDA_BIT_CLK_HDMI → HDA_BIT_CLK_HDMI 12
HDA_RST# B30 HDA_RST# HDMI → HDA_RST# HDMI 12
HDA_SDI B29 HDA_SDIN_HDMI → HDA_SDIN_HDMI 12
HDA_SDO C29 HDA_SDOUT_HDMI → HDA_SDOUT_HDMI 12
HDA_SYNC A28 HDA_SYNC_HDMI → HDA_SYNC_HDMI 12

EV_IV@CANTIGA_1p2

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

U504C

LVDS I/F

19 INT_LVDS_PWM → INT_LVDS_PWM L32 → L_BKLT_CTRL
19 INT_LVDS_BLON → INT_LVDS_BLON G32 → L_BKLT_EN
L_CTRL_CLK M32 → L_CTRL_CLK
L_CTRL_DATA M33 → L_CTRL_DATA
19 INT_LVDS_EDIDCLK → INT_LVDS_EDIDCLK K33 → L_DDC_CLK
11,19 INT_LVDS_EDIDDATA → INT_LVDS_EDIDDATA J33 → L_DDC_DATA
19 INT_LVDS_DIGON → INT_LVDS_DIGON M29 → L_VDD_EN
LVDS_IBG C44 → LVDS_IBG
T85 LVDS_VBG B43 → LVDS_VBG
LVDS_VREFH E37 → LVDS_VREFH
LVDS_VREFL E38 → LVDS_VREFL
19 INT_TXLCLKOUT- → INT_TXLCLKOUT- C41 → LVDSA_CLK#
19 INT_TXLCLKOUT+ → INT_TXLCLKOUT+ C40 → LVDSA_CLK
T65 INT_TXUCLKOUT- B37 → LVDSB_CLK#
T71 INT_TXUCLKOUT+ A37 → LVDSB_CLK
19 INT_TXLOUT0- → INT_TXLOUT0- H47 → LVDSA_DATA#_0
19 INT_TXLOUT1- → INT_TXLOUT1- E46 → LVDSA_DATA#_1
19 INT_TXLOUT2- → INT_TXLOUT2- G40 → LVDSA_DATA#_2
T74 INT_TXLOUT3- A40 → LVDSA_DATA#_3
19 INT_TXLOUT0+ → INT_TXLOUT0+ H48 → LVDSA_DATA_0
19 INT_TXLOUT1+ → INT_TXLOUT1+ D45 → LVDSA_DATA_1
19 INT_TXLOUT2+ → INT_TXLOUT2+ F40 → LVDSA_DATA_2
T78 INT_TXLOUT3+ B40 → LVDSA_DATA_3
T84 INT_TXUOUT0- A41 → LVDSB_DATA#_0
T83 INT_TXUOUT1- H38 → LVDSB_DATA#_1
T75 INT_TXUOUT2- G37 → LVDSB_DATA#_2
T86 INT_TXUOUT3- J37 → LVDSB_DATA#_3
T79 INT_TXUOUT0+ B42 → LVDSB_DATA_0
T82 INT_TXUOUT1+ G38 → LVDSB_DATA_1
T72 INT_TXUOUT2+ F37 → LVDSB_DATA_2
T81 INT_TXUOUT3+ K37 → LVDSB_DATA_3

TV I/F (Disable)

INT_TV_COMP F25 → TVA_DAC
INT_TV_Y/G H25 → TVB_DAC
INT_TV_C/R K25 → TVC_DAC
INT_TV_RNT H24 → TV_RTN
TV_DCONSEL_0 C31 → TV_DCONSEL_0
TV_DCONSEL_1 E32 → TV_DCONSEL_1

CRT I/F

20 INT_CRT_BLU → INT_CRT_BLU E28 → CRT_BLUE
20 INT_CRT_GRN → INT_CRT_GRN G28 → CRT_GREEN
20 INT_CRT_RED → INT_CRT_RED J28 → CRT_RED
CRT_IRTN G29 → CRT_IRTN
20 INT_CRT_DDCCLK → INT_CRT_DDCCLK H32 → CRT_DDC_CLK
20 INT_CRT_DDCDAT → INT_CRT_DDCDAT J32 → CRT_DDC_DATA
20 INT_HSYNC → INT_HSYNC R163 IV@30.1/F_4 HSYNC_G J29 → CRT_HSYNC
CRTIREF F29 → CRT_TVO_IREF
20 INT_VSYNC → INT_VSYNC R165 IV@30.1/F_4 VSYNC_G L29 → CRT_VSYNC
HSYNC/VSYNC serial R place close to NB
For IV @ Connect to 30.1ohm
For EV@ NC

PCI-EXPRESS GRAPHICS / LVDS / VGA

L<0.5" , if PCIE not support still connect to +VCC_PEG
+1.05V_VCC_PEG
PEG_COMPI T37 EXP_A_COMPX R204 49.9/F_4
PEG_COMPO T36

PEG_RX#_0 H44 PEG_RXN0
PEG_RX#_1 J46 PEG_RXN1
PEG_RX#_2 L44 PEG_RXN2
PEG_RX#_3 L40 PEG_RXN3
PEG_RX#_4 N41 PEG_RXN4
PEG_RX#_5 P48 PEG_RXN5
PEG_RX#_6 N44 PEG_RXN6
PEG_RX#_7 T43 PEG_RXN7
PEG_RX#_8 U43 PEG_RXN8
PEG_RX#_9 Y43 PEG_RXN9
PEG_RX#_10 Y48 PEG_RXN10
PEG_RX#_11 Y36 PEG_RXN11
PEG_RX#_12 AA43 PEG_RXN12
PEG_RX#_13 AD37 PEG_RXN13
PEG_RX#_14 AC47 PEG_RXN14
PEG_RX#_15 AD39 PEG_RXN15
PEG_RXN[15:0] 18

PEG_RX_0 H43 PEG_RXP0
PEG_RX_1 J44 PEG_RXP1
PEG_RX_2 L43 PEG_RXP2
PEG_RX_3 L41 PEG_RXP3
PEG_RX_4 N40 PEG_RXP4
PEG_RX_5 P47 PEG_RXP5
PEG_RX_6 N43 PEG_RXP6
PEG_RX_7 T42 PEG_RXP7
PEG_RX_8 U42 PEG_RXP8
PEG_RX_9 Y42 PEG_RXP9
PEG_RX_10 W47 PEG_RXP10
PEG_RX_11 Y37 PEG_RXP11
PEG_RX_12 AA42 PEG_RXP12
PEG_RX_13 AA36 PEG_RXP13
PEG_RX_14 AC48 PEG_RXP14
PEG_RX_15 AD40 PEG_RXP15
PEG_RXP[15:0] 18

PEG_TX#_0 J41 C_PEG_TXN0 C690 EV@0.1u/10V_4 PEG_TXN0
PEG_TX#_1 M46 C_PEG_TXN1 C692 EV@0.1u/10V_4 PEG_TXN1
PEG_TX#_2 M47 C_PEG_TXN2 C688 EV@0.1u/10V_4 PEG_TXN2
PEG_TX#_3 M40 C_PEG_TXN3 C686 EV@0.1u/10V_4 PEG_TXN3
PEG_TX#_4 M42 C_PEG_TXN4 C654 EV@0.1u/10V_4 PEG_TXN4
PEG_TX#_5 R48 C_PEG_TXN5 C681 EV@0.1u/10V_4 PEG_TXN5
PEG_TX#_6 N38 C_PEG_TXN6 C663 EV@0.1u/10V_4 PEG_TXN6
PEG_TX#_7 T40 C_PEG_TXN7 C656 EV@0.1u/10V_4 PEG_TXN7
PEG_TX#_8 U37 C_PEG_TXN8 C644 EV@0.1u/10V_4 PEG_TXN8
PEG_TX#_9 U40 C_PEG_TXN9 C646 EV@0.1u/10V_4 PEG_TXN9
PEG_TX#_10 Y40 C_PEG_TXN10 C673 EV@0.1u/10V_4 PEG_TXN10
PEG_TX#_11 AA46 C_PEG_TXN11 C649 EV@0.1u/10V_4 PEG_TXN11
PEG_TX#_12 AA37 C_PEG_TXN12 C678 EV@0.1u/10V_4 PEG_TXN12
PEG_TX#_13 AA40 C_PEG_TXN13 C651 EV@0.1u/10V_4 PEG_TXN13
PEG_TX#_14 AD43 C_PEG_TXN14 C661 EV@0.1u/10V_4 PEG_TXN14
PEG_TX#_15 AC46 C_PEG_TXN15 C683 EV@0.1u/10V_4 PEG_TXN15
PEG_TXN[15:0] 18

PEG_TX_0 J42 C_PEG_TXP0 C691 EV@0.1u/10V_4 PEG_TXP0
PEG_TX_1 L46 C_PEG_TXP1 C693 EV@0.1u/10V_4 PEG_TXP1
PEG_TX_2 M48 C_PEG_TXP2 C689 EV@0.1u/10V_4 PEG_TXP2
PEG_TX_3 M39 C_PEG_TXP3 C687 EV@0.1u/10V_4 PEG_TXP3
PEG_TX_4 M43 C_PEG_TXP4 C655 EV@0.1u/10V_4 PEG_TXP4
PEG_TX_5 R47 C_PEG_TXP5 C682 EV@0.1u/10V_4 PEG_TXP5
PEG_TX_6 N37 C_PEG_TXP6 C664 EV@0.1u/10V_4 PEG_TXP6
PEG_TX_7 T39 C_PEG_TXP7 C657 EV@0.1u/10V_4 PEG_TXP7
PEG_TX_8 U38 C_PEG_TXP8 C645 EV@0.1u/10V_4 PEG_TXP8
PEG_TX_9 U39 C_PEG_TXP9 C642 EV@0.1u/10V_4 PEG_TXP9
PEG_TX_10 Y39 C_PEG_TXP10 C674 EV@0.1u/10V_4 PEG_TXP10
PEG_TX_11 Y46 C_PEG_TXP11 C650 EV@0.1u/10V_4 PEG_TXP11
PEG_TX_12 AA36 C_PEG_TXP12 C679 EV@0.1u/10V_4 PEG_TXP12
PEG_TX_13 AA39 C_PEG_TXP13 C652 EV@0.1u/10V_4 PEG_TXP13
PEG_TX_14 AD42 C_PEG_TXP14 C662 EV@0.1u/10V_4 PEG_TXP14
PEG_TX_15 AD46 C_PEG_TXP15 C684 EV@0.1u/10V_4 PEG_TXP15
PEG_TXP[15:0] 18

EV_IV@CANTIGA_1p2

UMA iHDMI I/F

RAMP2
PEG_RXP3 R200 IV@0_4 Port-B_HPD# → Port-B_HPD# 21

C_PEG_TXP0 C680 IHM@0.1u/10V_4 TMDSB_DATA2 → TMDSB_DATA2 21
C_PEG_TXN0 C672 IHM@0.1u/10V_4 TMDSB_DATA2# → TMDSB_DATA2# 21
C_PEG_TXP1 C671 IHM@0.1u/10V_4 TMDSB_DATA1 → TMDSB_DATA1 21
C_PEG_TXN1 C670 IHM@0.1u/10V_4 TMDSB_DATA1# → TMDSB_DATA1# 21
C_PEG_TXP2 C669 IHM@0.1u/10V_4 TMDSB_DATA0 → TMDSB_DATA0 21
C_PEG_TXN2 C668 IHM@0.1u/10V_4 TMDSB_DATA0# → TMDSB_DATA0# 21
C_PEG_TXP3 C667 IHM@0.1u/10V_4 TMDSB_CLK → TMDSB_CLK 21
C_PEG_TXN3 C666 IHM@0.1u/10V_4 TMDSB_CLK# → TMDSB_CLK# 21

Check list note : CL_REF=0.35V

+1.05V
R180 1K/F_4
MCH_CLVREF_R
C164 0.1u/10V_4
R181 511/F_6

SM_VREF.Default use voltage divider for poor layout cause +SMDDR_VREF not meet spec.And Intel circuit PU/PD is 1K,But Check list PU/PD is 10K.

R206 *0_6 +SMDDR_VREF
SM_VREF R191 10K/F_4 +1.8VSUS_GMCH
R205 10K/F_4

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56- pull-up resistor to VCCP.

+1.05V
TSATN# 56_4 R537
+3V
CLK_MCH_OE# 10K_4 R172
PM_EXTTS#0 10K_4 R184
PM_EXTTS#1 10K_4 R179
SM_REXT R132 499/F_4

IV&EV Dis/Enable LVDS setting(See DG 1.0 P190 Table 103)

R190 IV@0_4 LVDS_VREFH / LVDS_VREFL — For IV @ 0ohm / For EV@ NC
R563 IV@2.37K/F_4 LVDS_IBG — For IV @ 2.37K/F / For EV@ NC
+3VO R154 IV@10K_4 L_CTRL_CLK
R155 IV@10K_4 L_CTRL_DATA — For IV @ 10K / For EV@ NC

IV&EV Dis/Enable CRT setting(See DG 1.0 P190 Table 103)

R176 *EV@0_4 INT_CRT_DDCCLK
R177 *EV@0_4 INT_CRT_DDCDAT — For IV @ NC / For EV@ 0ohm to GND or NC
R162 EV@0_4 HSYNC_G
R164 EV@0_4 VSYNC_G — For IV @ NC / For EV@ 0ohm to GND
R159 EV_IV@150/F_4 INT_CRT_BLU
R160 EV_IV@150/F_4 INT_CRT_GRN
R161 EV_IV@150/F_4 INT_CRT_RED — For IV @ Connect to 150ohm/F / For EV@ Connect to 0ohm GND
R157 EV_IV@1K/F_4 CRTIREF — For IV @ Connect to 1.02K/F / For EV@ Connect to 0ohm GND

Layout Note :See DG1.0 P180

Dis TV/En CRT(See DG1.0 P208 Table 118)

R142 EV_IV@75_4 INT_TV_COMP
R143 EV_IV@75_4 INT_TV_Y/G
R144 EV_IV@75_4 INT_TV_C/R — For IV @ 75ohm to GND / For EV@ 0ohm to GND
R158 0_4 TV_DCONSEL_0
R175 0_4 TV_DCONSEL_1 — For IV @ 0ohm to GND / For EV@ 0ohm to GND

IV&EV Dis/Enable PLL setting(See DG 1.0 P190 Table 103)

DREFCLK R561 EV@0_4
DREFCLK# R562 EV@0_4
DREFSSCLK R197 EV@0_4
DREFSSCLK# R198 EV@0_4 — For IV @ NC / For EV@ 0ohm to GND

+1.8VSUS_GMCH
R547 80.6/F_4
M_RCOMP
R548 *20/F_4
+1.8VSUS_GMCH
R545 *20/F_4
M_RCOMP#
R546 80.6/F_4

+1.8VSUS_GMCH R553 1K/F_4
R551 3.01K/F_4
C585 0.01u/16V_4
SM_RCOMP_VOH
C589 2.2u/6.3V_6
R550 1K/F_4
C583 0.01u/16V_4
SM_RCOMP_VOL
C584 2.2u/6.3V_6

SM_PWROK only for DDR3.(DDR2 PD only)

HWPG_1.8V 28,35
R194 *12K/F_4
SM_PWROK
R186 10K/F_6

Quanta Computer Inc.
PROJECT : TE1M

Size	Document Number	Rev
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BOM Option Table

Reference	Description
EV_IV@	EV&IV diff. BOM

GM PN=> AJSLB940T05
PM PN=> AJSLB970T03

17 M_A_DQ[63:0]

U504D

M_A_DQ0	AJ38	SA_DQ_0	
M_A_DQ1	AJ41	SA_DQ_1	
M_A_DQ2	AN38	SA_DQ_2	
M_A_DQ3	AM38	SA_DQ_3	
M_A_DQ4	AJ36	SA_DQ_4	
M_A_DQ5	AJ40	SA_DQ_5	
M_A_DQ6	AM44	SA_DQ_6	
M_A_DQ7	AM42	SA_DQ_7	
M_A_DQ8	AN43	SA_DQ_8	
M_A_DQ9	AN44	SA_DQ_9	
M_A_DQ10	AU40	SA_DQ_10	
M_A_DQ11	AT38	SA_DQ_11	
M_A_DQ12	AN41	SA_DQ_12	
M_A_DQ13	AN39	SA_DQ_13	
M_A_DQ14	AU44	SA_DQ_14	
M_A_DQ15	AU42	SA_DQ_15	
M_A_DQ16	AV39	SA_DQ_16	
M_A_DQ17	AY44	SA_DQ_17	
M_A_DQ18	BA40	SA_DQ_18	
M_A_DQ19	BD43	SA_DQ_19	
M_A_DQ20	AV41	SA_DQ_20	
M_A_DQ21	AY43	SA_DQ_21	
M_A_DQ22	BB41	SA_DQ_22	
M_A_DQ23	BC40	SA_DQ_23	
M_A_DQ24	AY37	SA_DQ_24	
M_A_DQ25	BD38	SA_DQ_25	
M_A_DQ26	AV37	SA_DQ_26	
M_A_DQ27	AT36	SA_DQ_27	
M_A_DQ28	AY38	SA_DQ_28	
M_A_DQ29	BB38	SA_DQ_29	
M_A_DQ30	AV36	SA_DQ_30	
M_A_DQ31	AW36	SA_DQ_31	
M_A_DQ32	BD13	SA_DQ_32	
M_A_DQ33	AU11	SA_DQ_33	
M_A_DQ34	BC11	SA_DQ_34	
M_A_DQ35	BA12	SA_DQ_35	
M_A_DQ36	AU13	SA_DQ_36	
M_A_DQ37	AV13	SA_DQ_37	
M_A_DQ38	BD12	SA_DQ_38	
M_A_DQ39	BC12	SA_DQ_39	
M_A_DQ40	BB9	SA_DQ_40	
M_A_DQ41	BA9	SA_DQ_41	
M_A_DQ42	AU10	SA_DQ_42	
M_A_DQ43	AV9	SA_DQ_43	
M_A_DQ44	BA11	SA_DQ_44	
M_A_DQ45	BD9	SA_DQ_45	
M_A_DQ46	AY8	SA_DQ_46	
M_A_DQ47	BA6	SA_DQ_47	
M_A_DQ48	AV5	SA_DQ_48	
M_A_DQ49	AV7	SA_DQ_49	
M_A_DQ50	AT9	SA_DQ_50	
M_A_DQ51	AN8	SA_DQ_51	
M_A_DQ52	AU5	SA_DQ_52	
M_A_DQ53	AU6	SA_DQ_53	
M_A_DQ54	AT5	SA_DQ_54	
M_A_DQ55	AN10	SA_DQ_55	
M_A_DQ56	AM11	SA_DQ_56	
M_A_DQ57	AM5	SA_DQ_57	
M_A_DQ58	AJ9	SA_DQ_58	
M_A_DQ59	AJ8	SA_DQ_59	
M_A_DQ60	AN12	SA_DQ_60	
M_A_DQ61	AM13	SA_DQ_61	
M_A_DQ62	AJ11	SA_DQ_62	
M_A_DQ63	AJ12	SA_DQ_63	

DDR SYSTEM MEMORY A

SA_BS_0	BD21	M_A_BS#0	M_A_BS#0 16,17
SA_BS_1	BG18	M_A_BS#1	M_A_BS#1 16,17
SA_BS_2	AT25	M_A_BS#2	M_A_BS#2 16,17
SA_RAS#	BB20	M_A_RAS#	M_A_RAS# 16,17
SA_CAS#	BD20	M_A_CAS#	M_A_CAS# 16,17
SA_WE#	AY20	M_A_WE#	M_A_WE# 16,17
SA_DM_0	AM37	M_A_DM0	M_A_DM[7:0] 17
SA_DM_1	AT41	M_A_DM1	
SA_DM_2	AY41	M_A_DM2	
SA_DM_3	AU39	M_A_DM3	
SA_DM_4	BB12	M_A_DM4	
SA_DM_5	AY6	M_A_DM5	
SA_DM_6	AT7	M_A_DM6	
SA_DM_7	AJ5	M_A_DM7	
SA_DQS_0	AJ44	M_A_DQS0	M_A_DQS[7:0] 17
SA_DQS_1	AT44	M_A_DQS1	
SA_DQS_2	BA43	M_A_DQS2	
SA_DQS_3	BC37	M_A_DQS3	
SA_DQS_4	AW12	M_A_DQS4	
SA_DQS_5	BC8	M_A_DQS5	
SA_DQS_6	AU8	M_A_DQS6	
SA_DQS_7	AM7	M_A_DQS7	
SA_DQS#_0	AJ43	M_A_DQS#0	M_A_DQS#[7:0] 17
SA_DQS#_1	AT43	M_A_DQS#1	
SA_DQS#_2	BA44	M_A_DQS#2	
SA_DQS#_3	BD37	M_A_DQS#3	
SA_DQS#_4	AY12	M_A_DQS#4	
SA_DQS#_5	BD8	M_A_DQS#5	
SA_DQS#_6	AU9	M_A_DQS#6	
SA_DQS#_7	AM8	M_A_DQS#7	
SA_MA_0	BA21	M_A_A0	M_A_A[14:0] 16,17
SA_MA_1	BC24	M_A_A1	
SA_MA_2	BG24	M_A_A2	
SA_MA_3	BH24	M_A_A3	
SA_MA_4	BG25	M_A_A4	
SA_MA_5	BA24	M_A_A5	
SA_MA_6	BD24	M_A_A6	
SA_MA_7	BG27	M_A_A7	
SA_MA_8	BF25	M_A_A8	
SA_MA_9	AW24	M_A_A9	
SA_MA_10	BC21	M_A_A10	
SA_MA_11	BG26	M_A_A11	
SA_MA_12	BH26	M_A_A12	
SA_MA_13	BH17	M_A_A13	
SA_MA_14	AY25	M_A_A14	

EV_IV@CANTIGA_1p2

17 M_B_DQ[63:0]

U504E

M_B_DQ0	AK47	SB_DQ_0	
M_B_DQ1	AH46	SB_DQ_1	
M_B_DQ2	AP47	SB_DQ_2	
M_B_DQ3	AP46	SB_DQ_3	
M_B_DQ4	AJ46	SB_DQ_4	
M_B_DQ5	AJ48	SB_DQ_5	
M_B_DQ6	AM48	SB_DQ_6	
M_B_DQ7	AP48	SB_DQ_7	
M_B_DQ8	AU47	SB_DQ_8	
M_B_DQ9	AU46	SB_DQ_9	
M_B_DQ10	BA48	SB_DQ_10	
M_B_DQ11	AY48	SB_DQ_11	
M_B_DQ12	AT47	SB_DQ_12	
M_B_DQ13	AR47	SB_DQ_13	
M_B_DQ14	BA47	SB_DQ_14	
M_B_DQ15	BC47	SB_DQ_15	
M_B_DQ16	BC46	SB_DQ_16	
M_B_DQ17	BC44	SB_DQ_17	
M_B_DQ18	BG43	SB_DQ_18	
M_B_DQ19	BF43	SB_DQ_19	
M_B_DQ20	BE45	SB_DQ_20	
M_B_DQ21	BC41	SB_DQ_21	
M_B_DQ22	BF40	SB_DQ_22	
M_B_DQ23	BE41	SB_DQ_23	
M_B_DQ24	BG38	SB_DQ_24	
M_B_DQ25	BF38	SB_DQ_25	
M_B_DQ26	BH35	SB_DQ_26	
M_B_DQ27	BG35	SB_DQ_27	
M_B_DQ28	BH40	SB_DQ_28	
M_B_DQ29	BG39	SB_DQ_29	
M_B_DQ30	BG34	SB_DQ_30	
M_B_DQ31	BH34	SB_DQ_31	
M_B_DQ32	BH14	SB_DQ_32	
M_B_DQ33	BG12	SB_DQ_33	
M_B_DQ34	BH11	SB_DQ_34	
M_B_DQ35	BC8	SB_DQ_35	
M_B_DQ36	BH12	SB_DQ_36	
M_B_DQ37	BF11	SB_DQ_37	
M_B_DQ38	BF8	SB_DQ_38	
M_B_DQ39	BG7	SB_DQ_39	
M_B_DQ40	BC5	SB_DQ_40	
M_B_DQ41	BC6	SB_DQ_41	
M_B_DQ42	AY3	SB_DQ_42	
M_B_DQ43	AY1	SB_DQ_43	
M_B_DQ44	BF6	SB_DQ_44	
M_B_DQ45	BF5	SB_DQ_45	
M_B_DQ46	BA1	SB_DQ_46	
M_B_DQ47	BD3	SB_DQ_47	
M_B_DQ48	AV2	SB_DQ_48	
M_B_DQ49	AU3	SB_DQ_49	
M_B_DQ50	AR3	SB_DQ_50	
M_B_DQ51	AN2	SB_DQ_51	
M_B_DQ52	AY2	SB_DQ_52	
M_B_DQ53	AV1	SB_DQ_53	
M_B_DQ54	AP3	SB_DQ_54	
M_B_DQ55	AR1	SB_DQ_55	
M_B_DQ56	AL1	SB_DQ_56	
M_B_DQ57	AL2	SB_DQ_57	
M_B_DQ58	AJ1	SB_DQ_58	
M_B_DQ59	AH1	SB_DQ_59	
M_B_DQ60	AM2	SB_DQ_60	
M_B_DQ61	AM3	SB_DQ_61	
M_B_DQ62	AH3	SB_DQ_62	
M_B_DQ63	AJ3	SB_DQ_63	

DDR SYSTEM MEMORY B

SB_BS_0	BC16	M_B_BS#0	M_B_BS#0 16,17
SB_BS_1	BB17	M_B_BS#1	M_B_BS#1 16,17
SB_BS_2	BB33	M_B_BS#2	M_B_BS#2 16,17
SB_RAS#	AU17	M_B_RAS#	M_B_RAS# 16,17
SB_CAS#	BG16	M_B_CAS#	M_B_CAS# 16,17
SB_WE#	BF14	M_B_WE#	M_B_WE# 16,17
SB_DM_0	AM47	M_B_DM0	M_B_DM[7:0] 17
SB_DM_1	AY47	M_B_DM1	
SB_DM_2	BD40	M_B_DM2	
SB_DM_3	BF35	M_B_DM3	
SB_DM_4	BG11	M_B_DM4	
SB_DM_5	BA3	M_B_DM5	
SB_DM_6	AP1	M_B_DM6	
SB_DM_7	AK2	M_B_DM7	
SB_DQS_0	AL47	M_B_DQS0	M_B_DQS[7:0] 17
SB_DQS_1	AV48	M_B_DQS1	
SB_DQS_2	BG41	M_B_DQS2	
SB_DQS_3	BG37	M_B_DQS3	
SB_DQS_4	BH9	M_B_DQS4	
SB_DQS_5	BB2	M_B_DQS5	
SB_DQS_6	AU1	M_B_DQS6	
SB_DQS_7	AN6	M_B_DQS7	
SB_DQS#_0	AL46	M_B_DQS#0	M_B_DQS#[7:0] 17
SB_DQS#_1	AV47	M_B_DQS#1	
SB_DQS#_2	BH41	M_B_DQS#2	
SB_DQS#_3	BH37	M_B_DQS#3	
SB_DQS#_4	BG9	M_B_DQS#4	
SB_DQS#_5	BC2	M_B_DQS#5	
SB_DQS#_6	AT2	M_B_DQS#6	
SB_DQS#_7	AN5	M_B_DQS#7	
SB_MA_0	AV17	M_B_A0	M_B_A[14:0] 16,17
SB_MA_1	BA25	M_B_A1	
SB_MA_2	BC25	M_B_A2	
SB_MA_3	AU25	M_B_A3	
SB_MA_4	AW25	M_B_A4	
SB_MA_5	BB28	M_B_A5	
SB_MA_6	AU28	M_B_A6	
SB_MA_7	AW28	M_B_A7	
SB_MA_8	AT33	M_B_A8	
SB_MA_9	BD33	M_B_A9	
SB_MA_10	BB16	M_B_A10	
SB_MA_11	AW33	M_B_A11	
SB_MA_12	AY33	M_B_A12	
SB_MA_13	BH15	M_B_A13	
SB_MA_14	AU33	M_B_A14	

EV_IV@CANTIGA_1p2

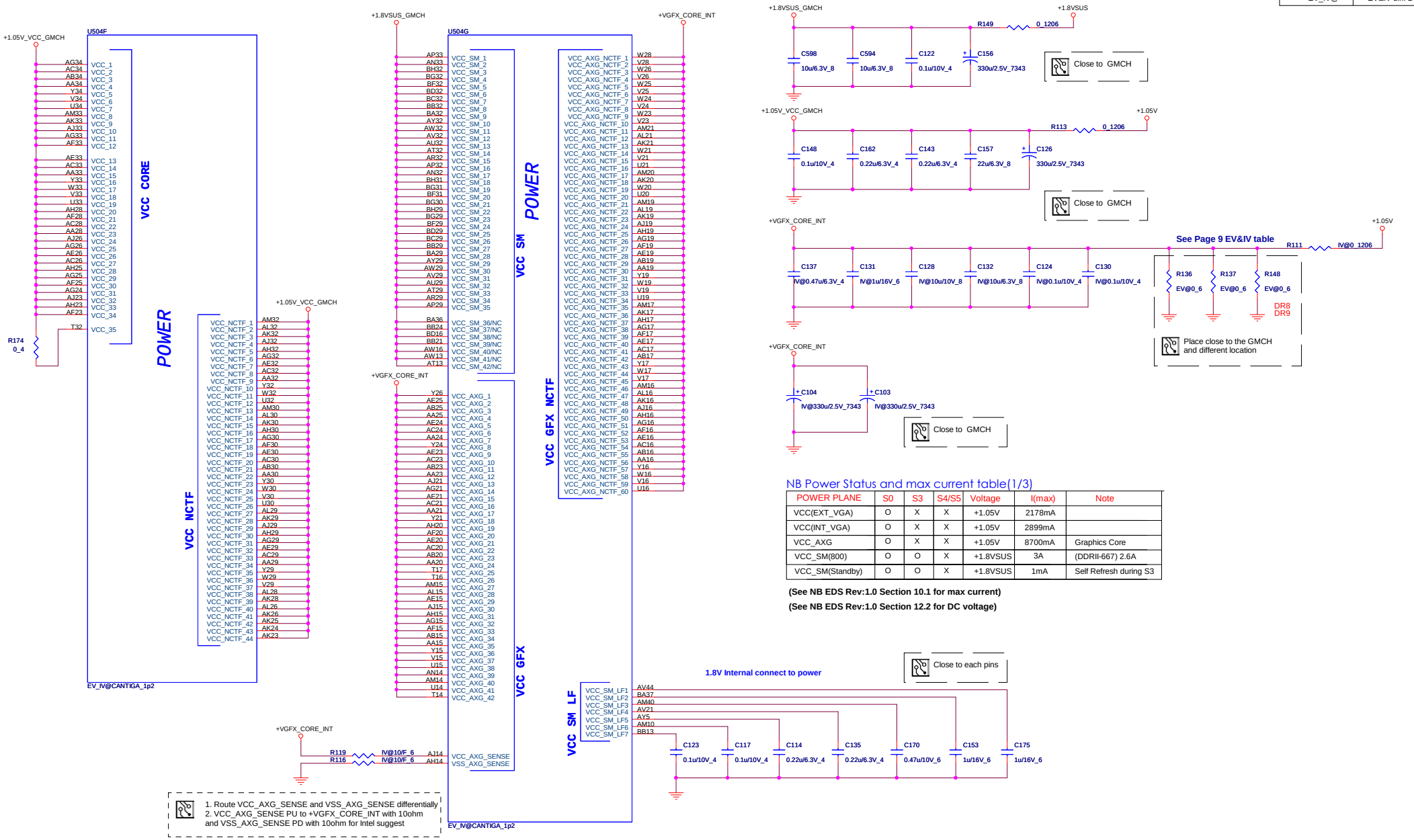
Quanta Computer Inc.
PROJECT : TE1M

Size	Document Number	Rev
	NB (3/7)- DDRII	E3D
Date: Monday, May 26, 2008	Sheet 7 of 40	

GM PN=> AJSLB940T05
PM PN=> AJSLB970T03

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA
EV_IV@	EV&IV diff. BOM



1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

NB Power Status and max current table(1/3)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC(EXT_VGA)	O	X	X	+1.05V	2178mA	
VCC(INT_VGA)	O	X	X	+1.05V	2899mA	
VCC_AXG	O	X	X	+1.05V	8700mA	Graphics Core
VCC_SM(800)	O	O	X	+1.8VSUS	3A	(DDRII-667) 2.6A
VCC_SM(Standby)	O	O	X	+1.8VSUS	1mA	Self Refresh during S3

(See NB EDS Rev:1.0 Section 10.1 for max current)

(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

Quanta Computer Inc.
PROJECT : TE1M

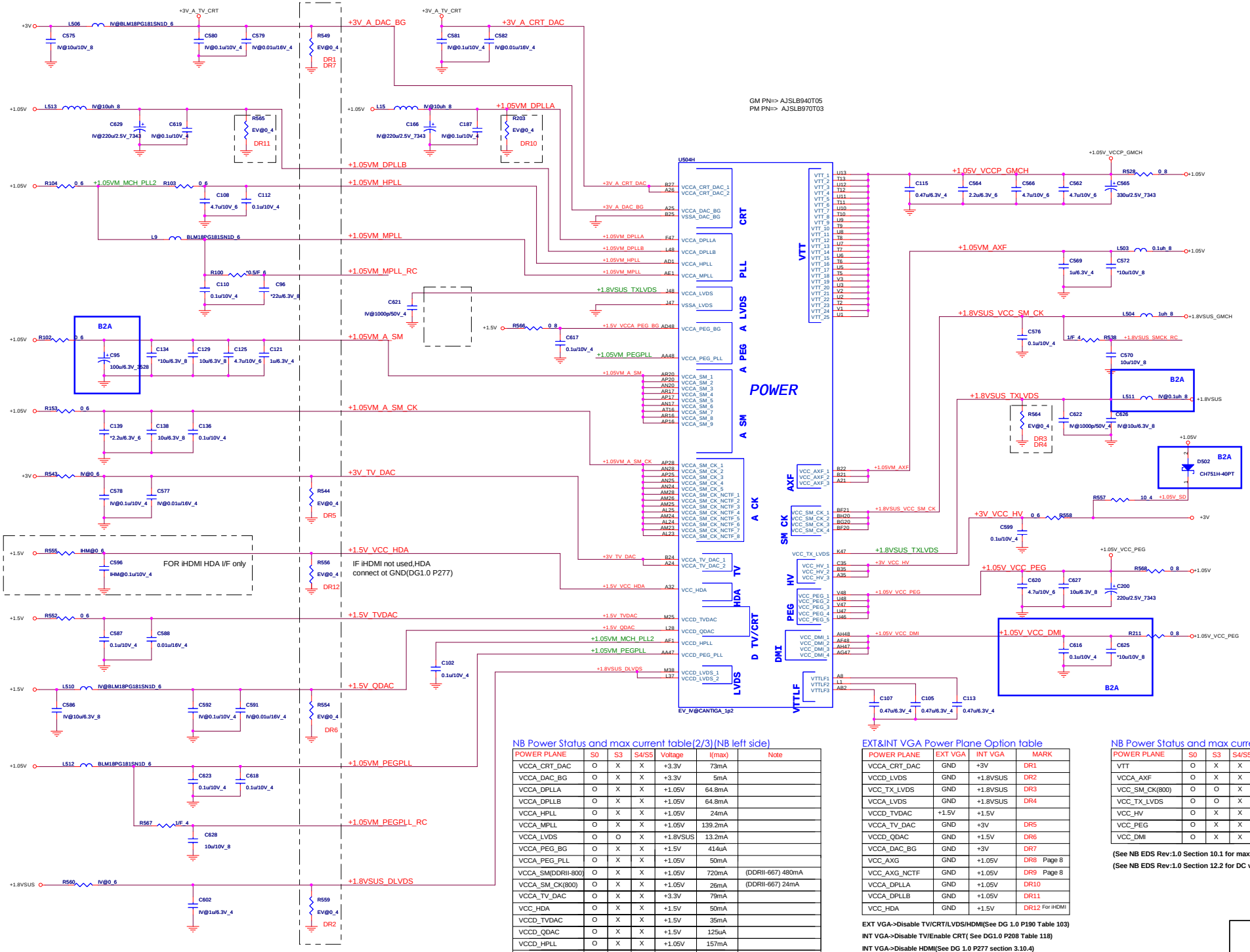
Size	Document Number	Rev
	NB (4/7)- VCC, NCTF	E3D

Date: Monday, May 26, 2008 Sheet 8 of 40

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA
IHM@	INT HDMI
EV_IV@	EV&IV diff. BOM

GM PN=> AJSLB940T05
PM PN=> AJSLB970T03



NB Power Status and max current table(2/3)(NB left side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCCA_CRT_DAC	O	X	X	+3.3V	73mA	
VCCA_DAC_BG	O	X	X	+3.3V	5mA	
VCCA_DPLLA	O	X	X	+1.05V	64.8mA	
VCCA_DPLLB	O	X	X	+1.05V	64.8mA	
VCCA_HPLL	O	X	X	+1.05V	24mA	
VCCA_MPLL	O	X	X	+1.05V	139.2mA	
VCCA_LVDS	O	O	X	+1.8VSUS	13.2mA	
VCCA_PEG_BG	O	X	X	+1.5V	414uA	
VCCA_PEG_PLL	O	X	X	+1.05V	50mA	
VCCA_SM(DDRII-800)	O	X	X	+1.05V	720mA	(DDRII-667) 480mA
VCCA_SM_CK(800)	O	X	X	+1.05V	26mA	(DDRII-667) 24mA
VCCA_TV_DAC	O	X	X	+3.3V	79mA	
VCC_HDA	O	X	X	+1.5V	50mA	
VCCD_TVDAC	O	X	X	+1.5V	35mA	
VCCD_QDAC	O	X	X	+1.5V	125uA	
VCCD_HPLL	O	X	X	+1.05V	157mA	
VCCD_PEG_PLL	O	X	X	+1.05V	50mA	
VCCD_LVDS	O	O	X	+1.8VSUS	60mA	

EXT&INT VGA Power Plane Option table

POWER PLANE	EXT VGA	INT VGA	MARK
VCCA_CRT_DAC	GND	+3V	DR1
VCCD_LVDS	GND	+1.8VSUS	DR2
VCC_TX_LVDS	GND	+1.8VSUS	DR3
VCCA_LVDS	GND	+1.8VSUS	DR4
VCCD_TVDAC	+1.5V	+1.5V	
VCCA_TV_DAC	GND	+3V	DR5
VCCD_QDAC	GND	+1.5V	DR6
VCCA_DAC_BG	GND	+3V	DR7
VCC_AXG	GND	+1.05V	DR8 Page 8
VCC_AXG_NCTF	GND	+1.05V	DR9 Page 8
VCCA_DPLLA	GND	+1.05V	DR10
VCCA_DPLLB	GND	+1.05V	DR11
VCC_HDA	GND	+1.5V	DR12 For iHDMI

EXT VGA->Disable TV/CRT/LVDS/HDMI(See DG 1.0 P190 Table 103)
INT VGA->Disable TV/Enable CRT(See DG1.0 P208 Table 118)
INT VGA->Disable HDMI(See DG 1.0 P277 section 3.10.4)

NB Power Status and max current table(3/3)(NB Right side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VTT	O	X	X	+1.05V	852mA	FSB at 1067MHz
VCCA_AXF	O	X	X	+1.05V	322mA	
VCC_SM_CK(800)	O	O	X	+1.8VSUS	124mA	(DDRII-667) 120mA
VCC_TX_LVDS	O	O	X	+1.8VSUS	119mA	
VCC_HV	O	X	X	+3V	106mA	
VCC_PEG	O	X	X	+1.05V	1782mA	
VCC_DMI	O	X	X	+1.05V	456mA	

(See NB EDS Rev:1.0 Section 10.1 for max current)
(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

Quanta Computer Inc.
PROJECT : TE1M

Size	Document Number	Rev
	NB (5/7)- POWER	E3D
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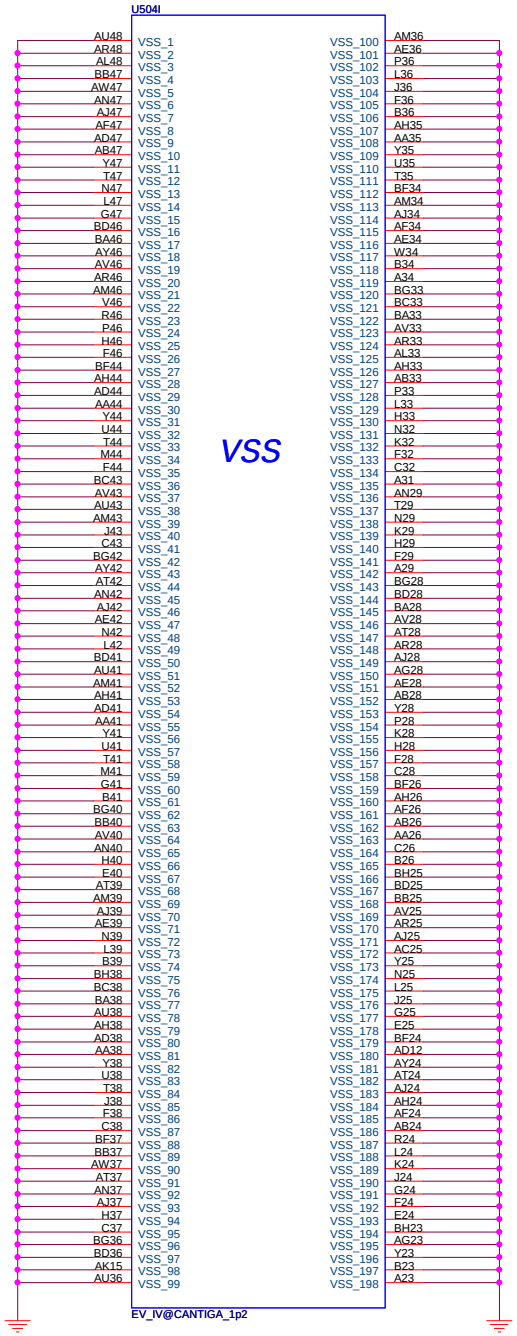
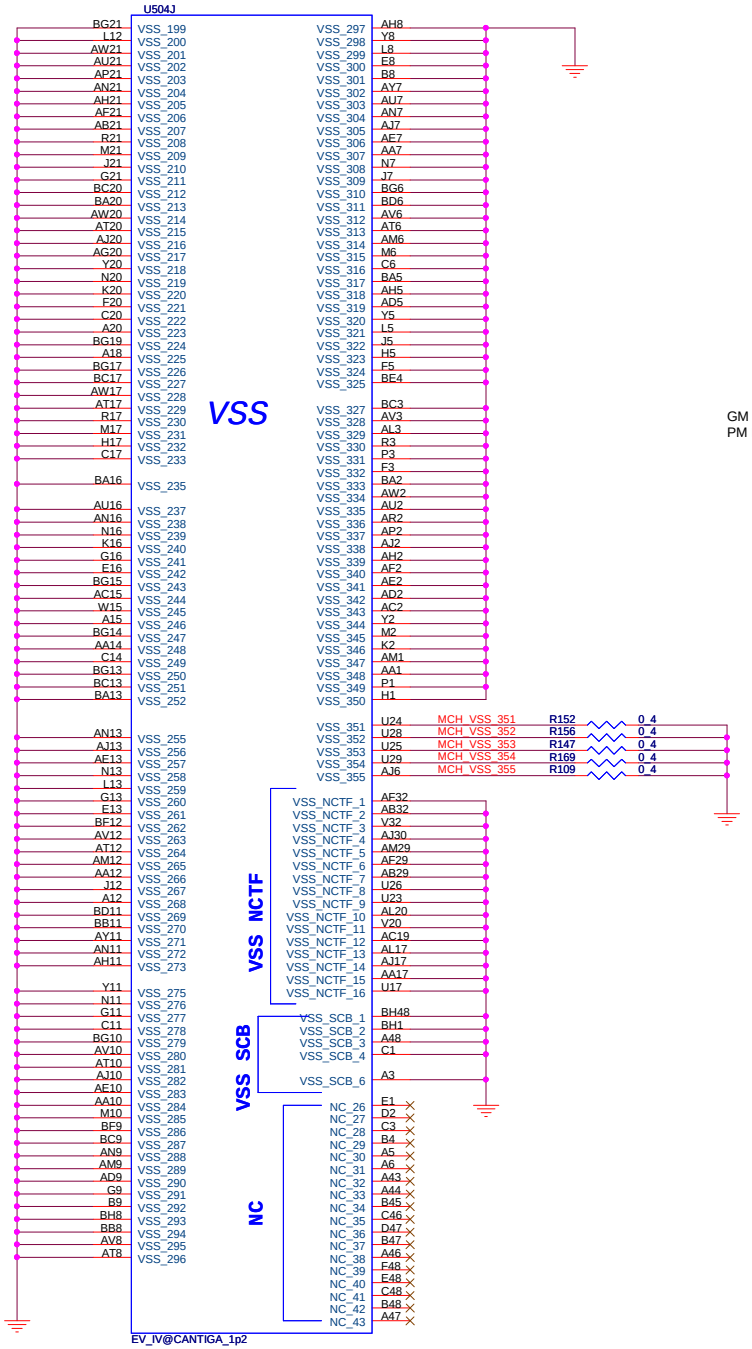
BOM Option Table

Reference	Description
EV_IV@	EV&IV diff. BOM





GM PN=> AJSLB940T05
PM PN=> AJSLB970T03

U24	MCH_VSS_351	R152	0_4
U28	MCH_VSS_352	R156	0_4
U25	MCH_VSS_353	R147	0_4
U29	MCH_VSS_354	R169	0_4
AJ6	MCH_VSS_355	R109	0_4

Quanta Computer Inc.
PROJECT : TE1M

Size	Document Number	Rev
	NB (6/7)- VSS	E3D
Date: Monday, May 26, 2008	Sheet 10 of 40	

North Bridge Strap Pin Configuration Table

(See DG 1.0 P295 Table 184)
(See NB EDS 1.0 P187 Table 74)

BOM Option Table

Reference	Description
iTPM@	Internal TPM

Pin Name	Strap description	Configuration	PU<4.02K> PD <2.21K>	Note
CFG[2:0]	FSB Frequency Select	[000]= FSB 1066MHz [010] = FSB 800MHz [011] = FSB 667MHz	See Page 2 FSB selection table	
CFG[4:3]	Reserved			
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)	6 MCH_CFG_5 R141 *4.02K/F_4	
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)	6 MCH_CFG_6 R146 *iTPM@10K/F_4	
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)	6 MCH_CFG_7 R145 *4.02K/F_4	
CFG8	Reserved			
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)	6 MCH_CFG_9 R540 *4.02K/F_4	
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)	6 MCH_CFG_10 R542 *4.02K/F_4	
CFG11	Reserved			
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)	6 MCH_CFG_12 R130 *4.02K/F_4	
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)	6 MCH_CFG_13 R131 *4.02K/F_4	
CFG[15:14]	Reserved			
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)	6 MCH_CFG_16 R129 *4.02K/F_4	
CFG[18:17]	Reserved			
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed	6 MCH_CFG_19 R124 *4.02K/F_4 +3V	
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port	6 MCH_CFG_20 R125 *4.02K/F_4 +3V	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI/DP Device Present(Default) 1 = SDVO/HDMI/DP Device present	6,21 SDVO_CTRLDATA R170 *2.2K/F_4 +3V	Reference PAGE21 R185
L_DDC_DATA	Local Flat Panel(LFP) Present	0 = LFP Disable(Default) 1 = LFP Card Present;PCIE disable	6,19 INT_LVDS_EDIDDATA R168 *2.2K/F_4 +3V	
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present	6 DDPC_CTRLDATA R123 *2.2K/F_4 +3V	

Enable iTPM Table

PAGE	Net Name	PU & PD	NOTE
11	MCH_CFG_6	PD 10K to GND	NB Strap pin
13	SPI_MOSI	PU 20K to +3V_S5	SB Strap pin
14	CLGPIO5	PU 10K to +3V_S5	SB Strap pin

Quanta Computer Inc.
PROJECT : TE1M

Size	Document Number	Rev
	NB (7/7)- STRAP PIN	E3D

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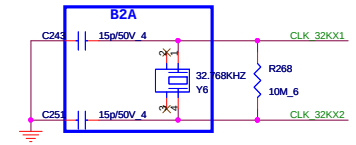
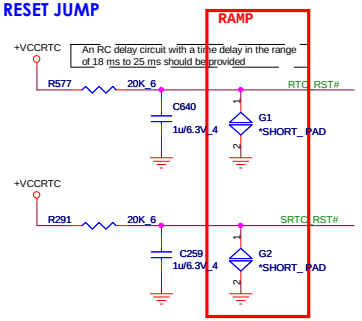
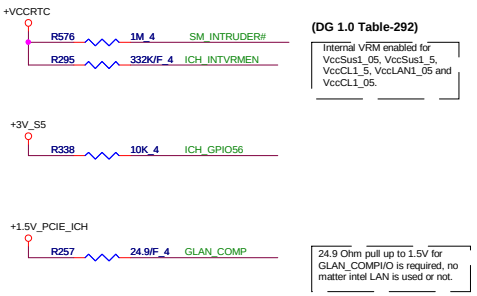
RTC CRYSTAL



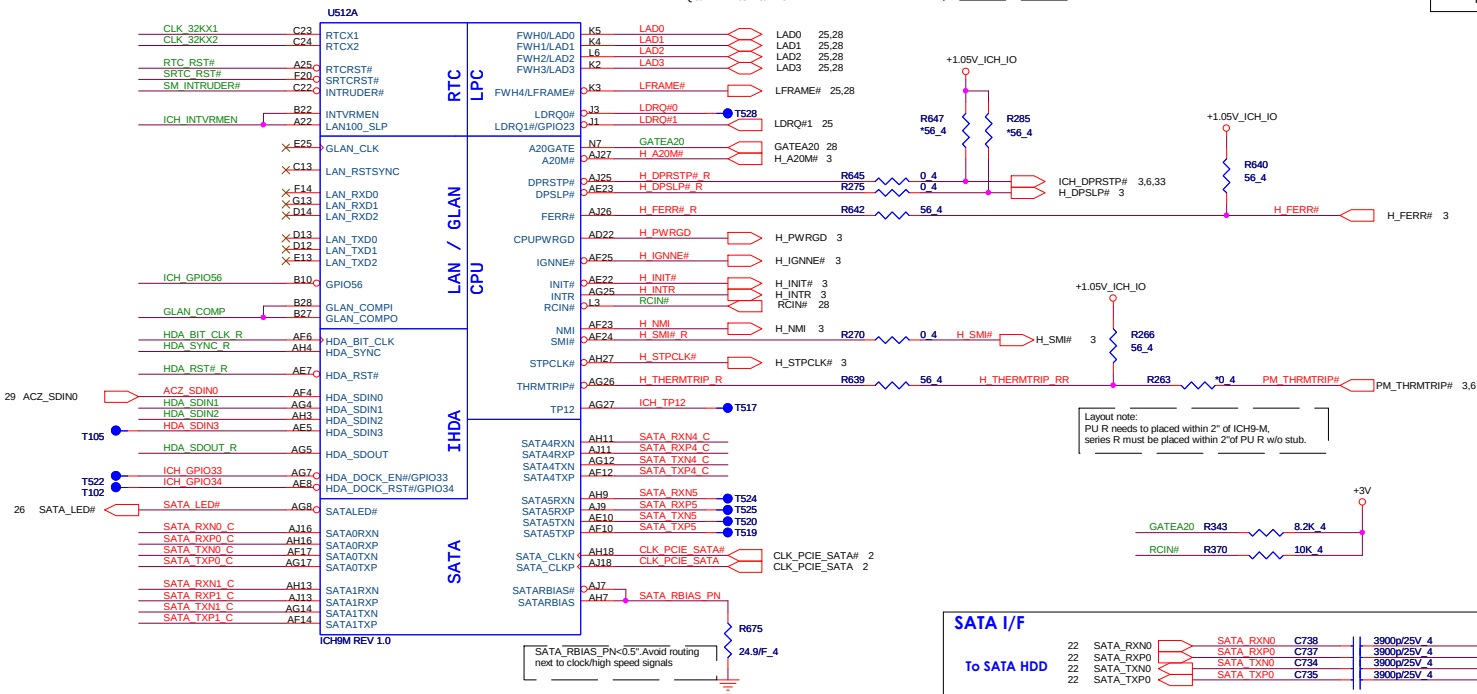
RESET JUMP





LDRQ0/1# : Internal PU

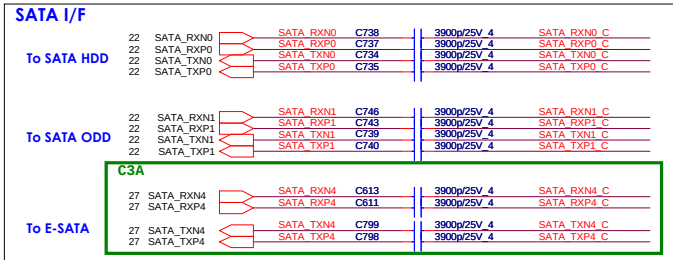
Layout note:
DPRSTP# , Daisy Chain
(SB>Power>NB>CPU)



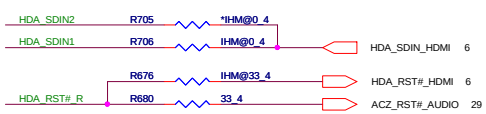
BOM Option Table

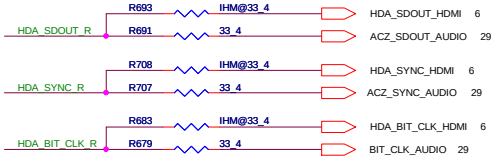
Reference	Description
IHM@	INT HDMI

SATA I/F



HD Audio I/F(CODEC& iHDMI)

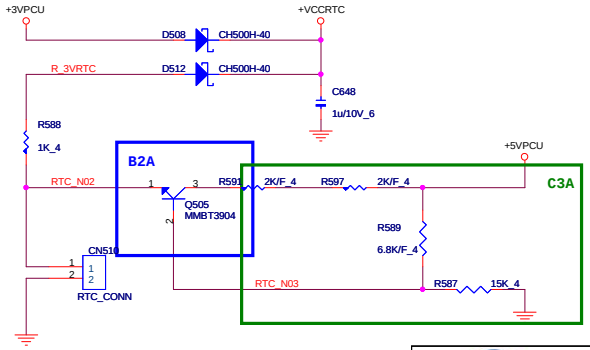




South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT / Description 0 / 0 / RSVD 0 / 1 / Enter XOR Chain 1 / 0 / Normal opration(Default) 1 / 1 / Set PCIE port config bit 1	14 ICH_TP3 — ICH_TP3 R280 *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_SDOUT_R R697 *1K_4 +3V_HDA_IO_ICH PU +1.5V

RTC BATTERY

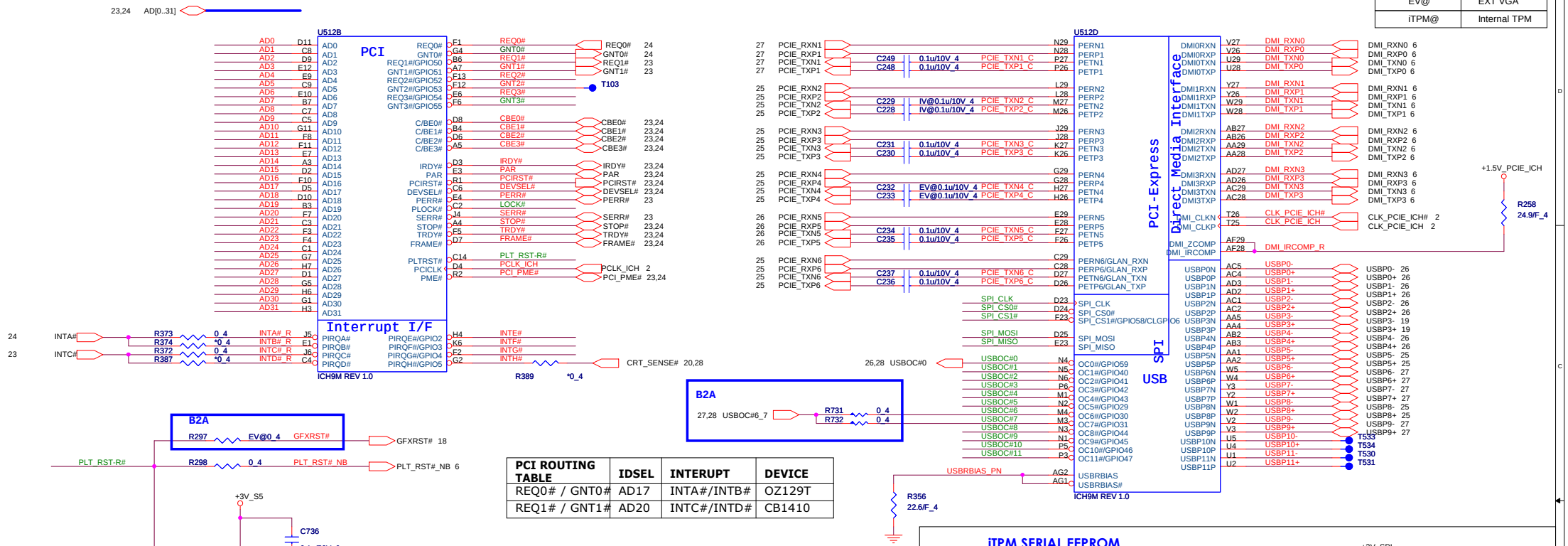


Quanta Computer Inc.		
PROJECT : TE1M		
Size	Document Number: SB (1/4)- HOST	Rev: E3D
Date: Monday, May 26, 2008	Sheet 12 of 40	

PCI/PCI-E/USB/DMI/SPI

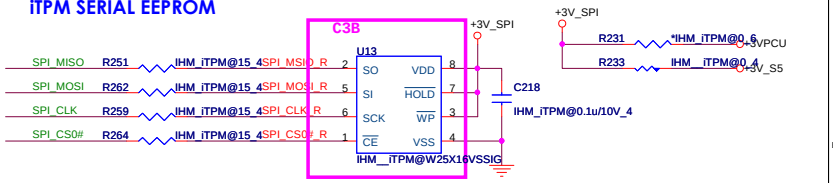
BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA
iTPM@	Internal TPM



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#/INTB#	OZ129T
REQ1# / GNT1#	AD20	INTC#/INTD#	CB1410

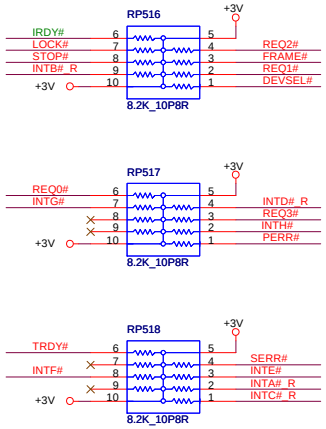
iTPM SERIAL EEPROM



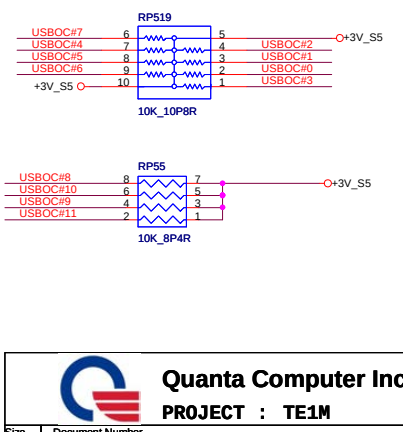
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R376 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI R607 *iTPM@20K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI(Default) 1 / 0 / PCI 1 / 1 / LPC	GNT0# R375 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# R267 *1K_4

PCI PULL-UP



USBOC# PULL-UP



Quanta Computer Inc.

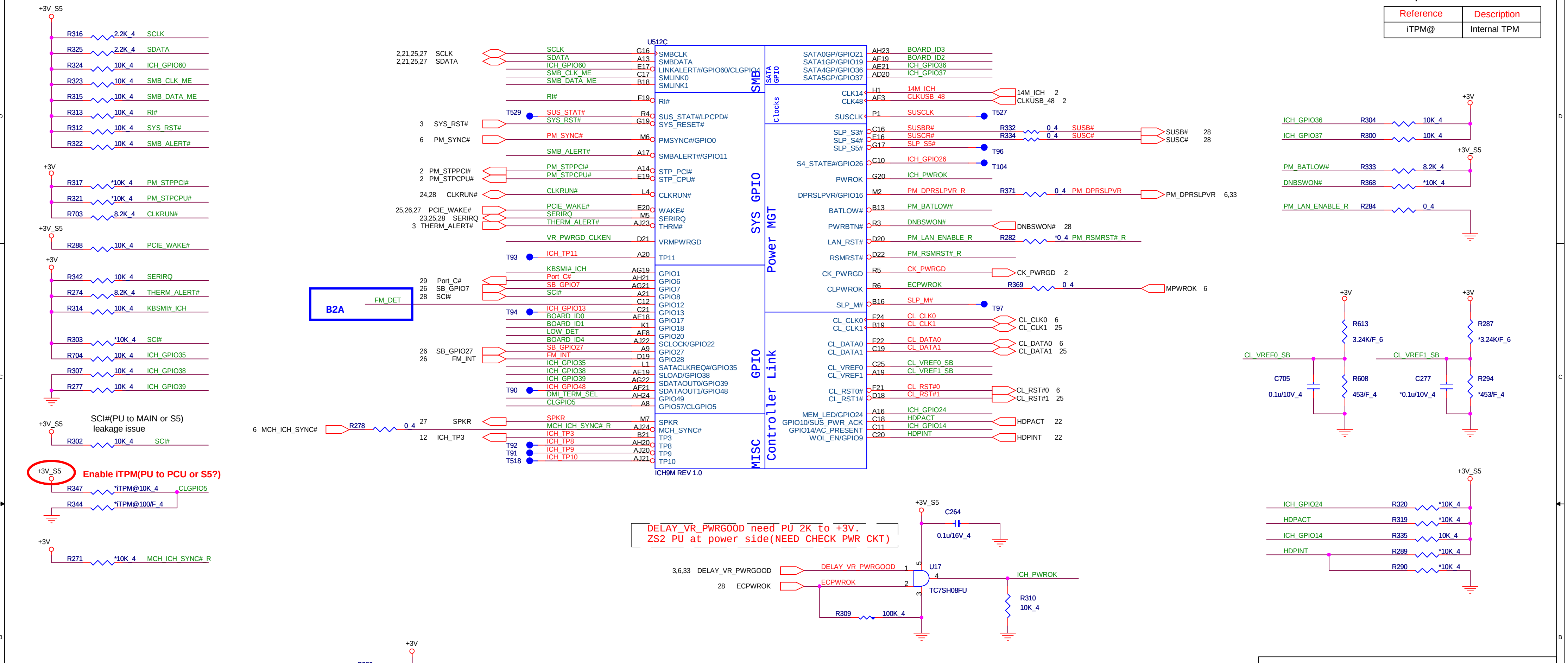
PROJECT : TE1M

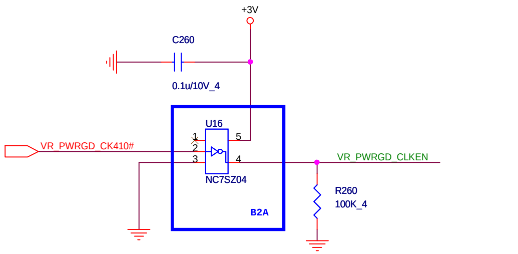
Size	Document Number	Rev
	SB (2/4)- PCIE/PCI/USB	E3D

Date: Monday, May 26, 2008 Sheet 13 of 40

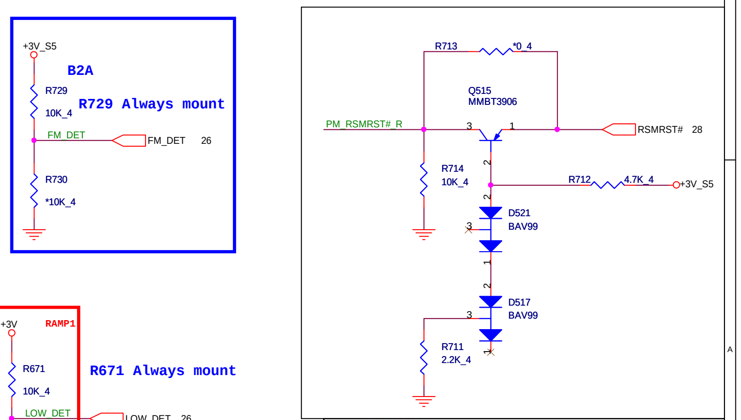
BOM Option Table

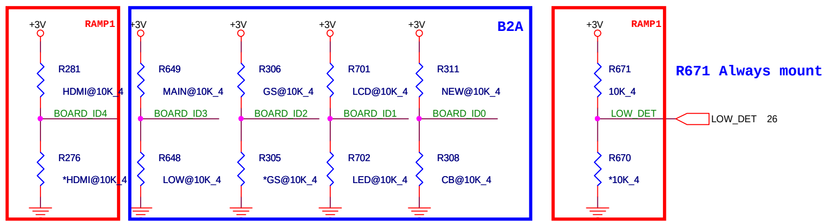
Reference	Description
iTPM@	Internal TPM





Board ID	ID4	ID3	ID2	ID1	ID0	M/L	FM
NEW CARD CARD BUS					H L		
CCFL Panel LED Panel				H L			
W/ G-SENSOR W/O G-SENSOR			H L				
Main stream ID Low Cost ID		H L					
W/ HDMI W/O HDMI	H L						
W/O Low Cost board W Low Cost						H L	
W/O FM W FM							H L





South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	SPKR R341 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R269 *1K_4

Quanta Computer Inc.

PROJECT : TE1M

Size	Document Number	Rev
	SB (3/4)- GPIO	E3D

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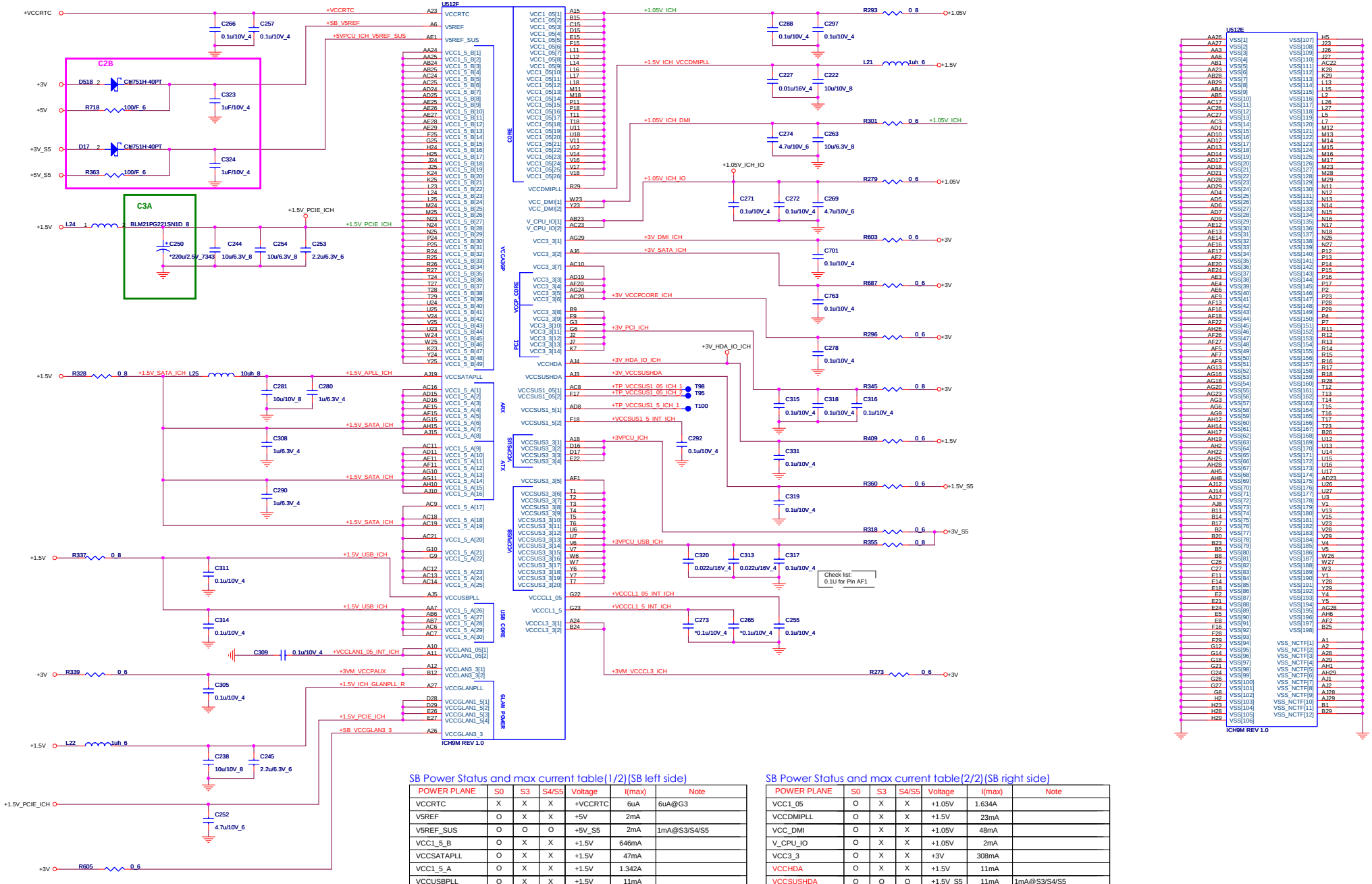
BOM Option Table

Reference	Description
N/A	N/A



SB Power Status and max current table(1/2)(SB left side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCCRTC	X	X	X	+VCCRTC	6uA	6uA@G3
V5REF	O	X	X	+5V	2mA	
V5REF_SUS	O	O	O	+5V_S5	2mA	1mA@S3/S4/S5
VCC1_5_B	O	X	X	+1.5V	646mA	
VCCSATAPLL	O	X	X	+1.5V	47mA	
VCC1_5_A	O	X	X	+1.5V	1.342A	
VCCUSBPLL	O	X	X	+1.5V	11mA	
VCCLAN1_05	O	X	X	+1.05V	X	Powered by Vcc1_05 in S0
VCCLAN3_3	O	X	X	+3V	19mA	Tied to +3V,not +3VSUS
VCCGLANPLL	O	X	X	+1.5V	23mA	
VCCGLAN1_5	O	X	X	+1.5V	80mA	
VCCGLAN3_3	O	X	X	+3V	1mA	

SB Power Status and max current table(2/2)(SB right side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC1_05	O	X	X	+1.05V	1.634A	
VCCDMIPLL	O	X	X	+1.5V	23mA	
VCC_DMI	O	X	X	+1.05V	48mA	
V_CPU_IO	O	X	X	+1.05V	2mA	
VCC3_3	O	X	X	+3V	308mA	
VCCHDA	O	X	X	+1.5V	11mA	
VCCSUSHDA	O	O	O	+1.5V_S5	11mA	1mA@S3/S4/S5
VCCSUS1_05	O	O	O	+1.05V	X	Powered by Vcc1_05 in S0
VCCSUS1_5	O	O	O	+1.5V	X	Powered by Vcc1_5_A in S0
VCCSUS3_3	O	O	O	+3VSUS	212mA	52mA@S3/S4/S5
VCCCL1_05	O	X	X	+1.05V	X	Powered by Vcc1_05 in S0
VCCCL1_5	O	X	X	+1.5V	X	Powered by Vcc1_5_A in S0
VCCCL3_3	O	X	X	+3V	19mA	Tied to +3V,not +3VSUS

Note:VCCSUS1_05 , VCCSUS1_5 are powered by VccSus3_3 in S3/S4/S5

Quanta Computer Inc.
PROJECT : TE1M

Size	Document Number	Rev
	SB (4/4)- POWER	E3D

Date: Monday, May 26, 2008 Sheet 15 of 40

DDR2 Dual channel A/B PULL UP

BOM Option Table

Reference	Description
N/A	N/A

M_A_A[14..0] → M_A_A[14..0] 7,17

M_B_A[14..0] → M_B_A[14..0] 7,17

DDRII A CHANNEL

+SMDDR_VTERM

C160 C171 C140 C144 C184 C176 C168 C159 C155 C190 C189 C191 C145

0.1u/10V_4

DDRII B CHANNEL

+SMDDR_VTERM

C196 C174 C141 C154 C142 C192 C198 C173 C167 C158 C178 C194 C163

0.1u/10V_4

Place one cap close to every 2 pull-up resistor terminated to SMDDR_VTERM

RP28: M_A_A3, M_A_A1 — 56X2 — +SMDDR_VTERM

RP33: M_A_A9, M_A_A5 — 56X2

RP31: M_A_A2, M_A_A4 — 56X2

RP38: M_A_A11 — 56X2 — 6,17 M_CKE1

RP37: M_A_A8 — 56X2 — 6,17 M_CKE0

RP39: M_A_A12 — 56X2 — 7,17 M_A_BS#2

RP25: M_A_A0 — 56X2 — 7,17 M_A_BS#1

RP26: M_B_A10 — 56X2 — 7,17 M_B_WE# — +SMDDR_VTERM

RP29: M_B_A3, M_B_A1 — 56X2

RP27: M_B_A0 — 56X2 — 7,17 M_B_BS#1

RP34: M_B_A7, M_B_A11 — 56X2

RP32: M_B_A8, M_B_A5 — 56X2

RP30: M_B_A2, M_B_A4 — 56X2

RP35: M_B_A9, M_B_A12 — 56X2

M_A_A14 — R202 — 56_4 — +SMDDR_VTERM

RP36: M_A_A7, M_A_A6 — 56X2 — +SMDDR_VTERM

RP41: 56X2 — 6,17 M_CKE3, 7,17 M_B_BS#2

RP18: 56X2 — 6,17 M_ODT1, 6,17 M_CS#1

RP19: 56X2 — 6,17 M_ODT3, 7,17 M_B_BS#0

RP24: M_A_A10 — 56X2 — 7,17 M_A_BS#0

RP21: 56X2 — 7,17 M_A_CAS#, 7,17 M_A_WE#

RP23: 56X2 — 6,17 M_CS#0, 7,17 M_A_RAS#

RP22: 56X2 — 7,17 M_B_CAS#, 6,17 M_CS#3

RP40: M_B_A6 — 56X2 — 6,17 M_CKE4

RP20: 56X2 — 6,17 M_ODT2, 7,17 M_B_RAS#

RP16: M_A_A13 — 56X2 — 6,17 M_ODT0

RP17: M_B_A13 — 56X2 — 6,17 M_CS#2

M_B_A14 — R201 — 56_4 — +SMDDR_VTERM

Quanta Computer Inc.

PROJECT : TE1M

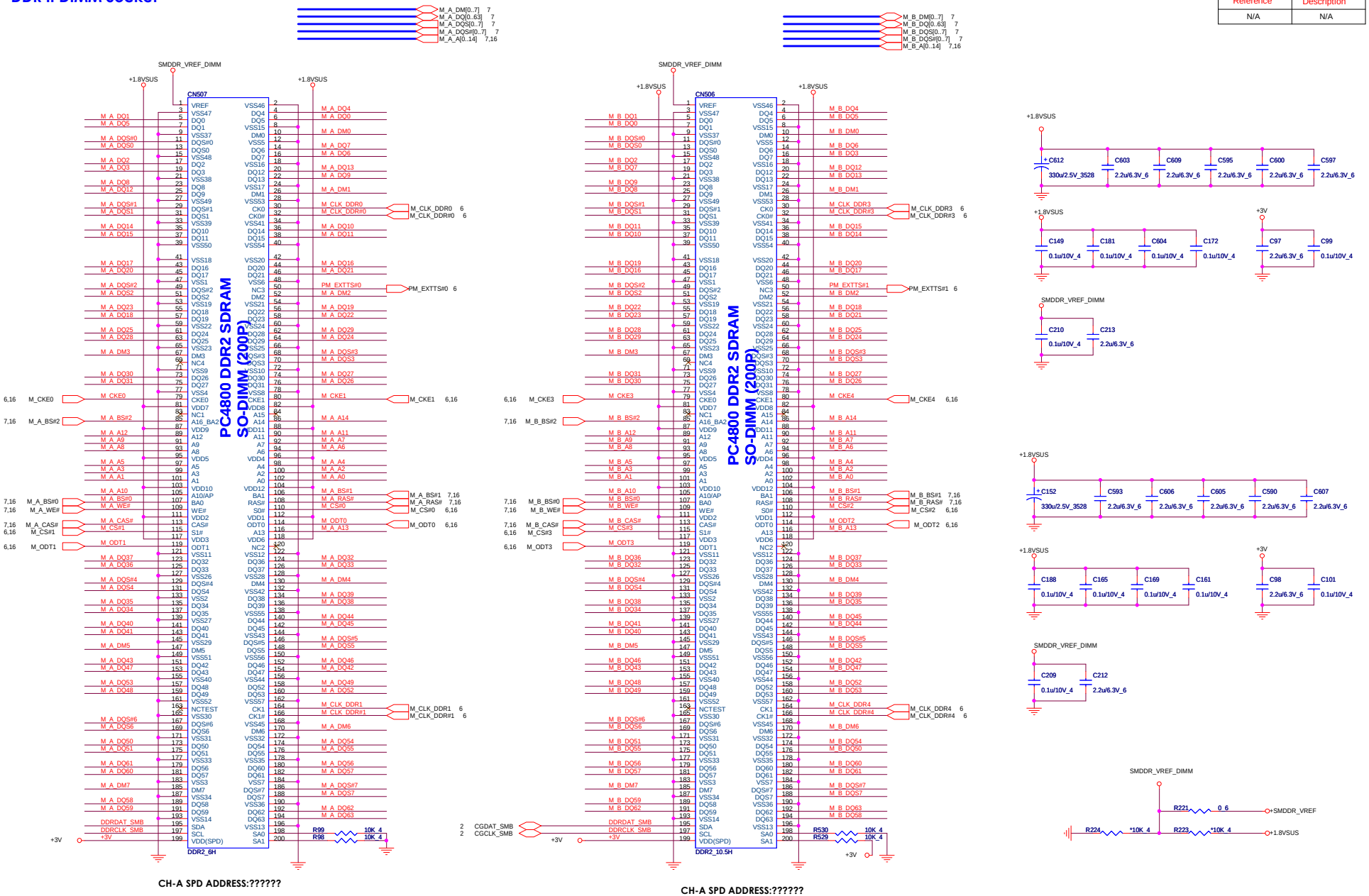
Size	Document Number	Rev
	DDR RES. ARRAY	E3D

Date: Monday, May 26, 2008 Sheet 16 of 40

DDR II DIMM Socket

BOM Option Table

Reference	Description
N/A	N/A



Quanta Computer Inc.

PROJECT : TE1M

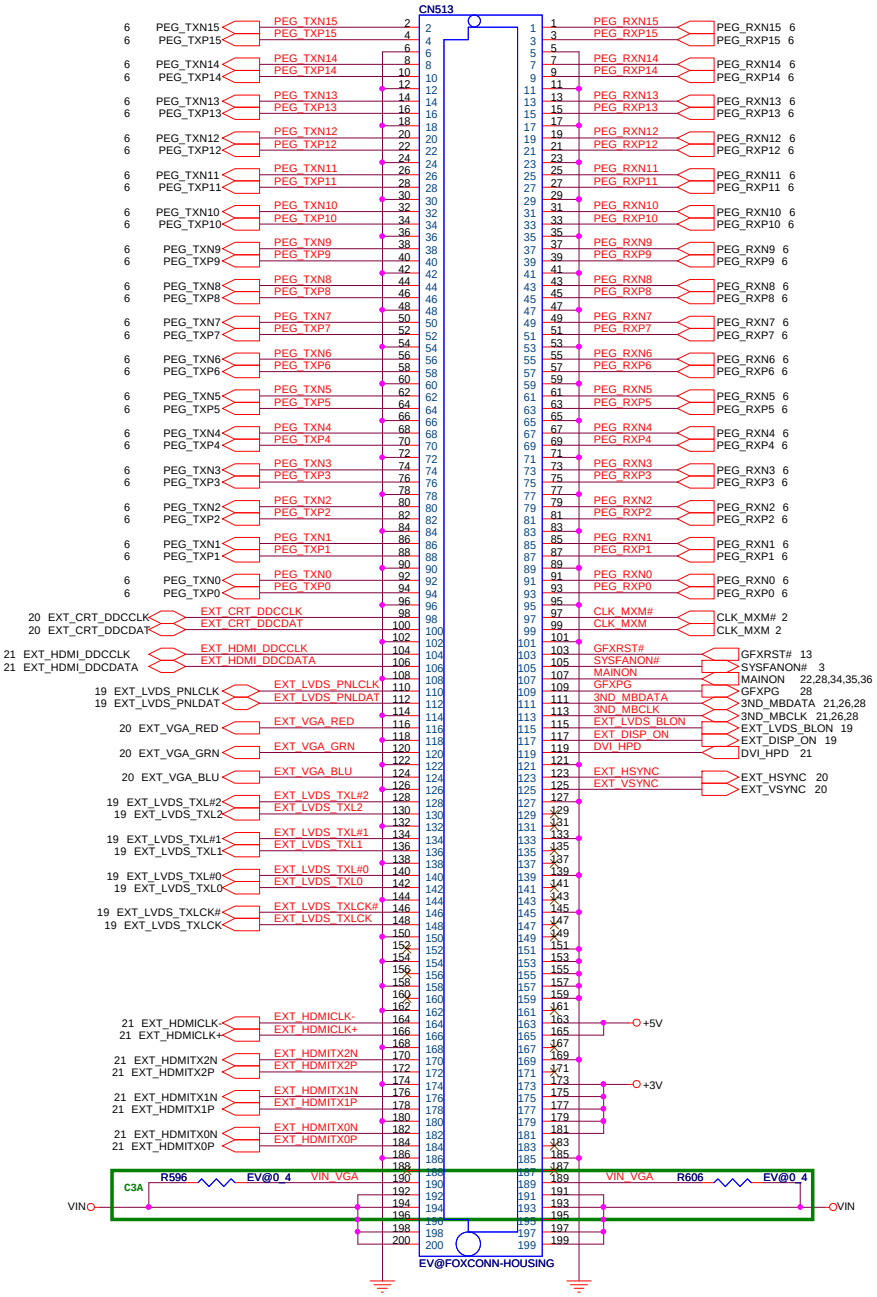
Size	Document Number	Rev
	DDR SO-DIMM	E3D

Date: Monday, May 26, 2008 Sheet 17 of 40

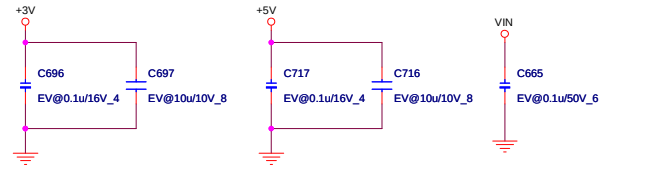
VGA BOARD CONNECOTR

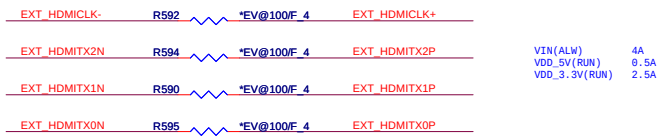
BOM Option Table

Reference	Description
EV@	EXT VGA



EMI De-coupling CAP





VIN(ALW)	4A
VDD_5V(RUN)	0.5A
VDD_3.3V(RUN)	2.5A

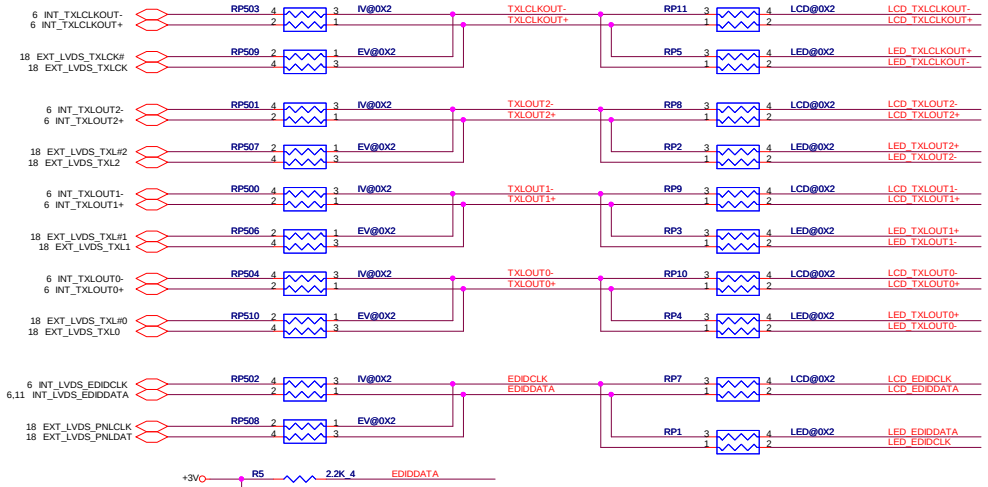
Quanta Computer Inc.

PROJECT : TE1M

Size	Document Number	Rev
	VGA CONNECTOR	E3D

Date: Friday, June 13, 2008 Sheet 18 of 40

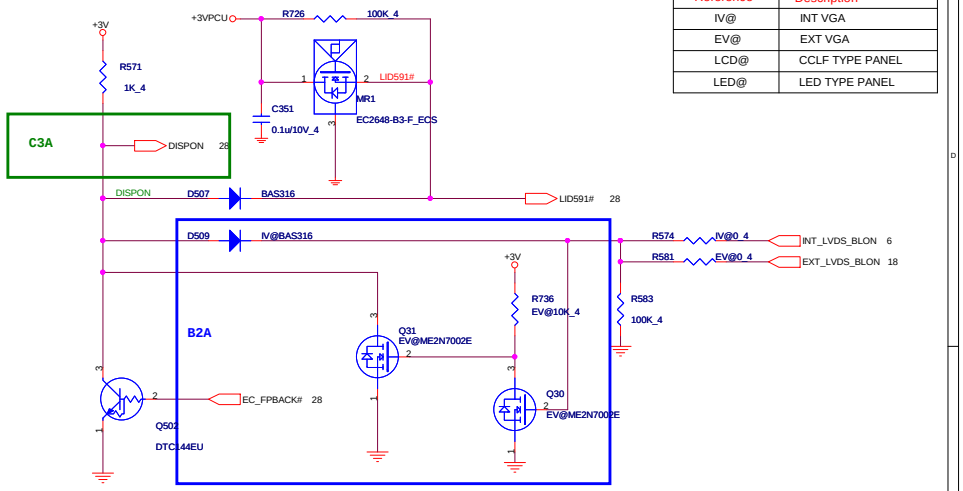
LVDS SIGNALS



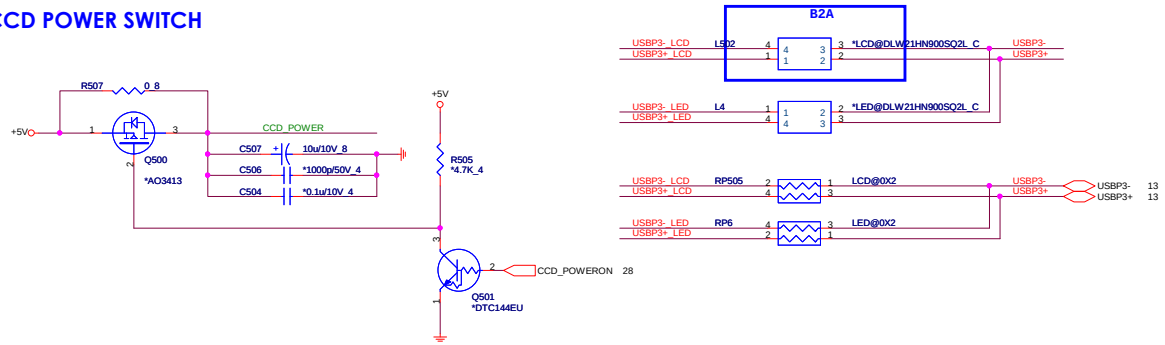
HALL SENSOR&BACK LIGHT SWITCH

BOM Option Table

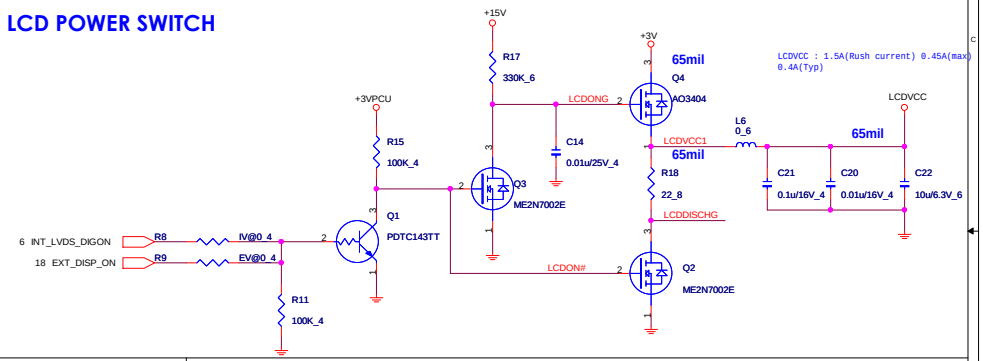
Reference	Description
IV@	INT VGA
EV@	EXT VGA
LCD@	CCLF TYPE PANEL
LED@	LED TYPE PANEL



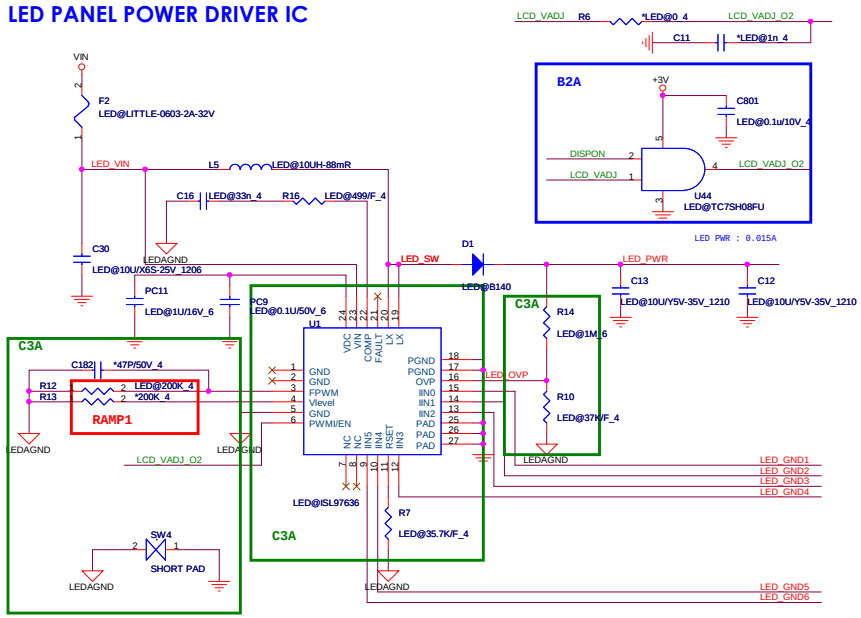
CCD POWER SWITCH



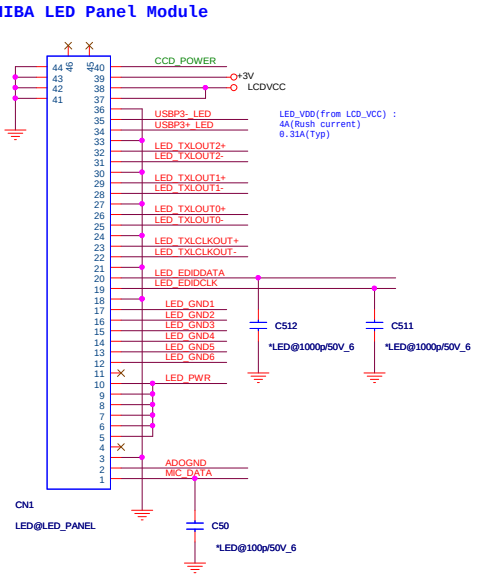
LCD POWER SWITCH



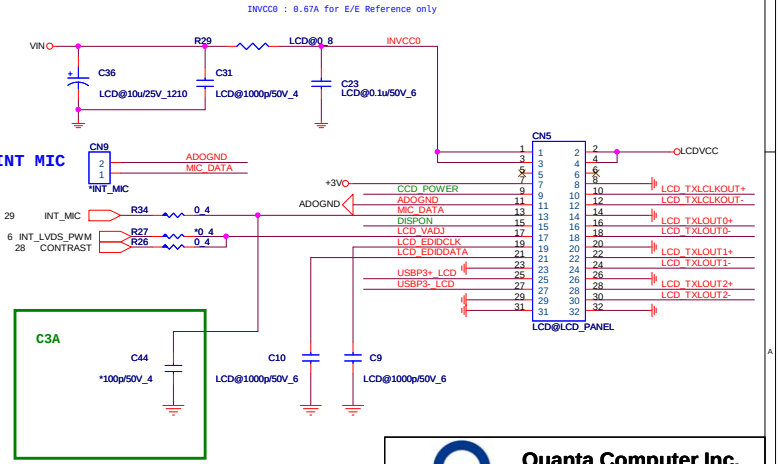
LED PANEL POWER DRIVER IC



TOSHIBA LED Panel Module



LCD Panel Module



Quanta Computer Inc.

PROJECT : TE1M

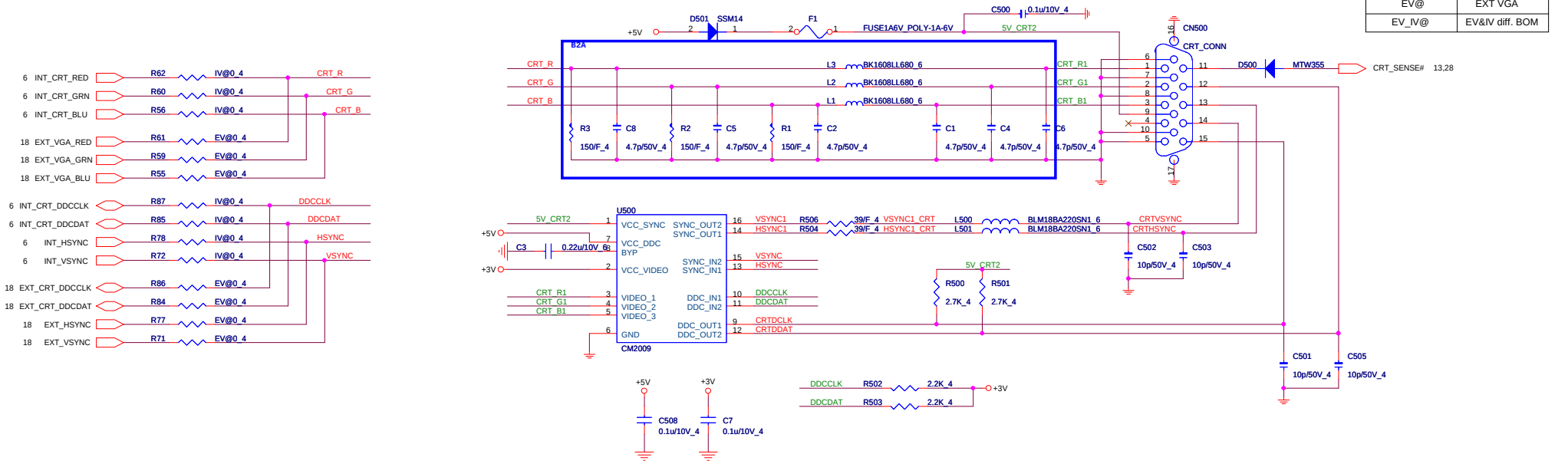
Size	Document Number	Rev
	LCD/LED Panel/CCD	E3D

Date: Friday, June 13, 2008 Sheet 19 of 40

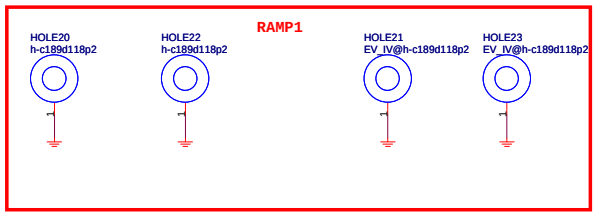
CRT CONN & DDC LEVEL SHIFT IC

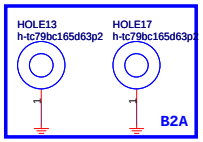
BOM Option Table

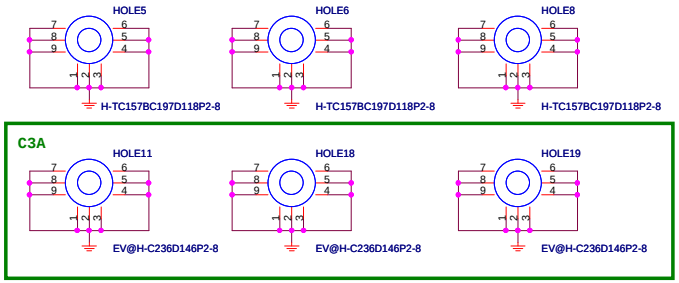
Reference	Description
IV@	INT VGA
EV@	EXT VGA
EV_IV@	EV&IV diff. BOM

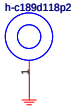


HOLE & NUTS

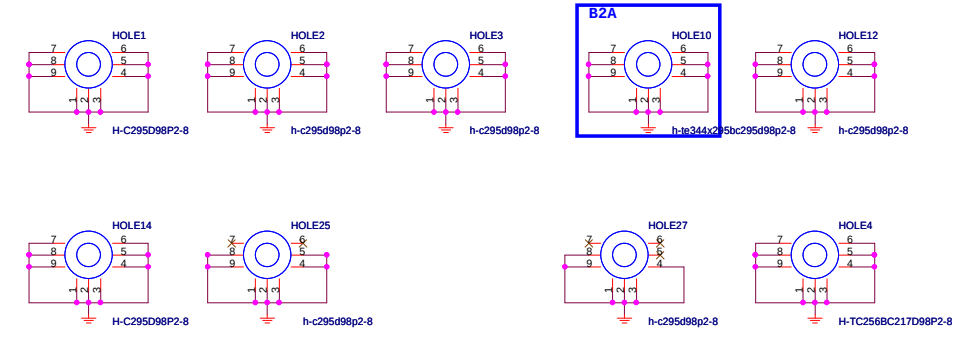








NUTS NEED RATING TOP or BOT (NUT don't use *)



Quanta Computer Inc.

PROJECT : TE1M

Size	Document Number	Rev
	CRT/HOLE	E3D

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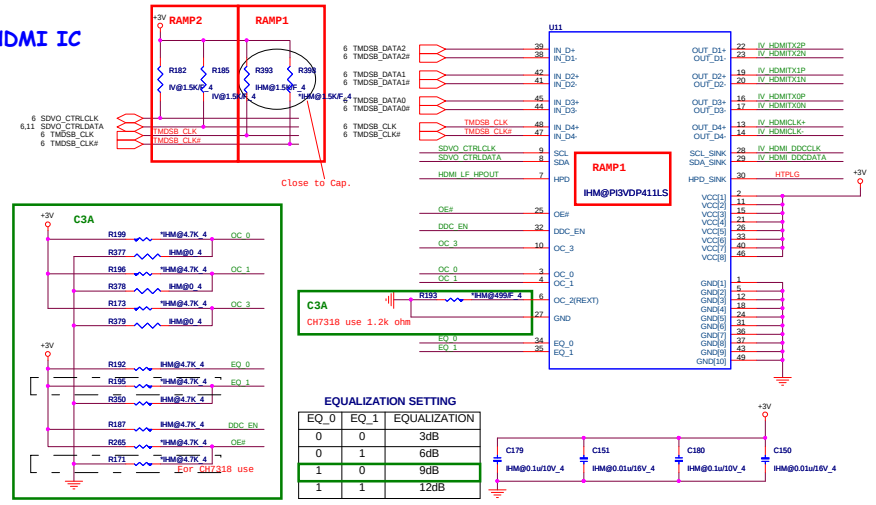
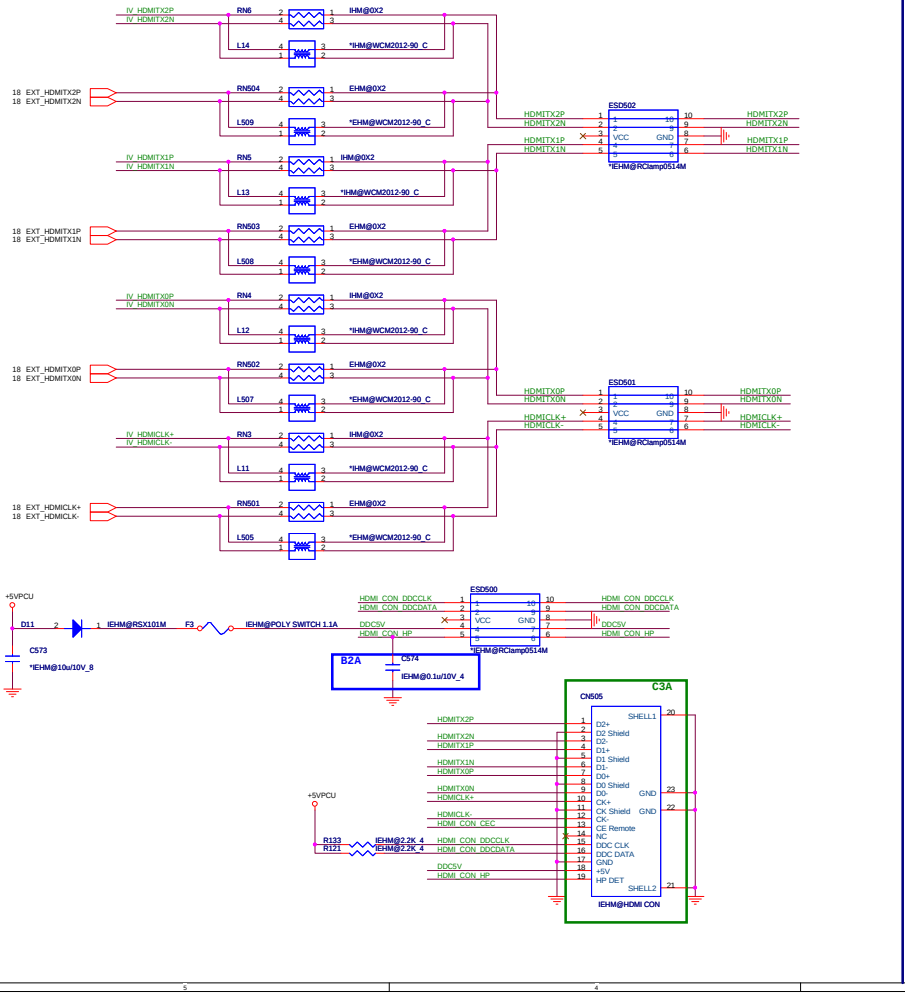
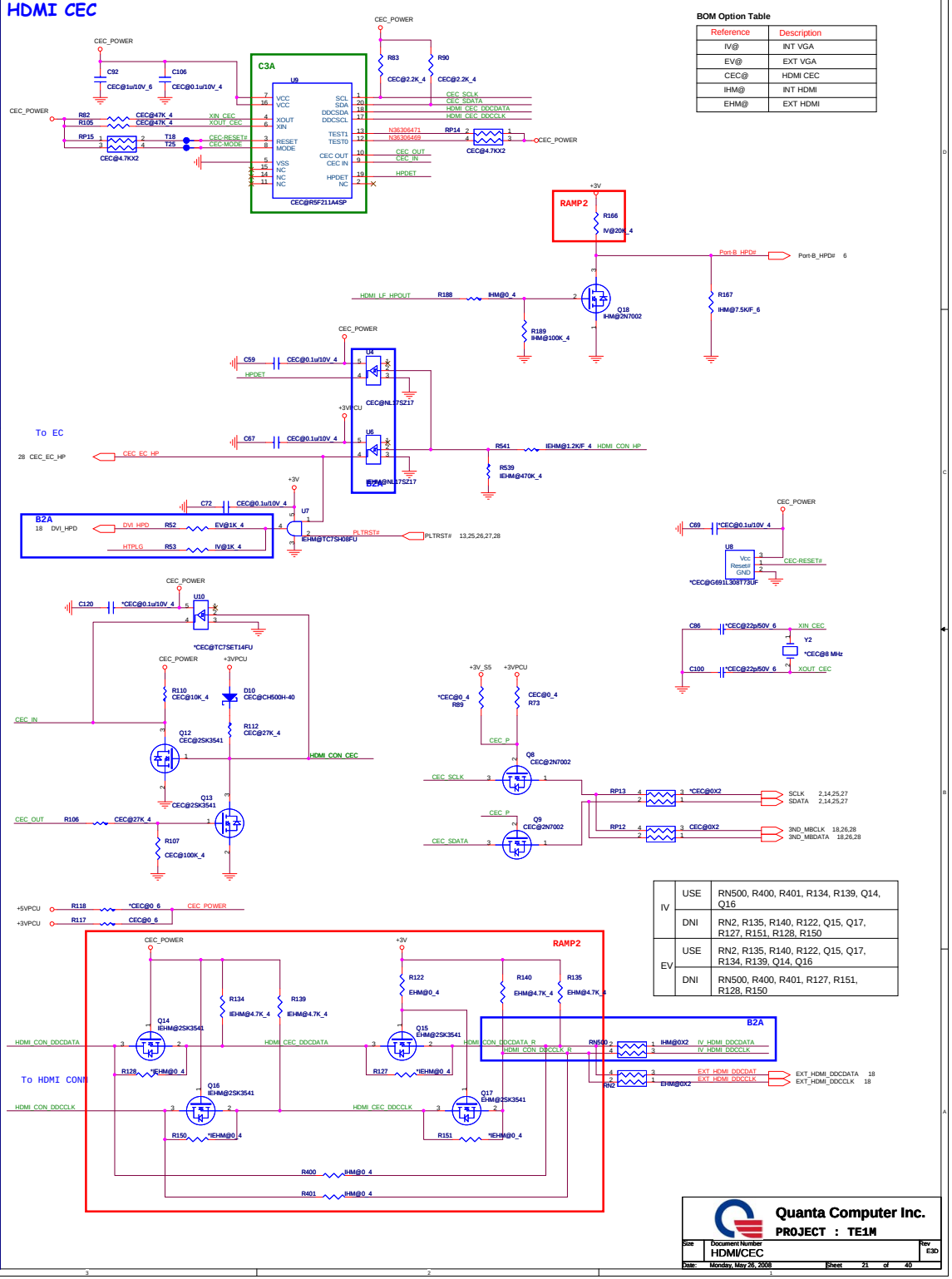
HDMI IC





HDMI CEC



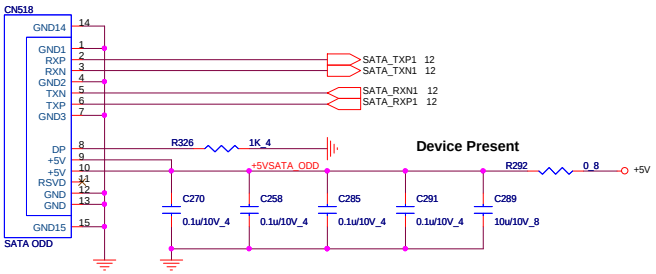
BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA
CEC@	HDMI CEC
IIHM@	INT HDMI
EHM@	EXT HDMI

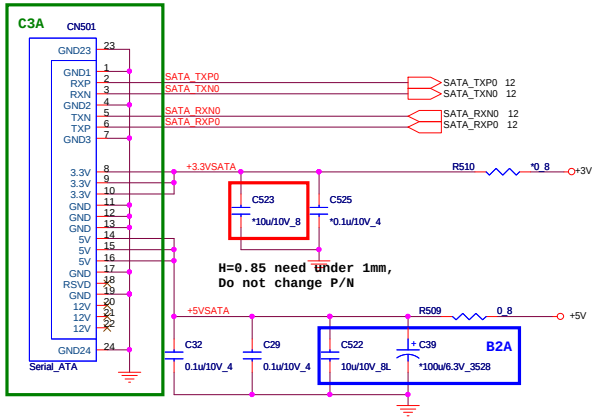
IV	USE	RN500, R400, R401, R134, R139, Q14, Q16
	DNI	RN2, R135, R140, R122, Q15, Q17, R127, R151, R128, R150
EV	USE	RN2, R135, R140, R122, Q15, Q17, R134, R139, Q14, Q16
	DNI	RN500, R400, R401, R127, R151, R128, R150

Quanta Computer Inc.
PROJECT : TE1M
Size | Document Number: HDMI/CEC | Rev: E3D
Date: Monday, May 26, 2008 | Sheet 21 of 40

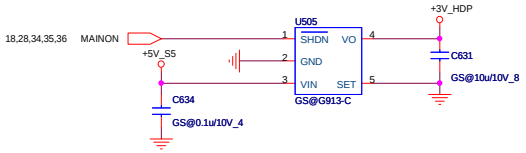
SATA ODD



SATA HDD



G SENSOR

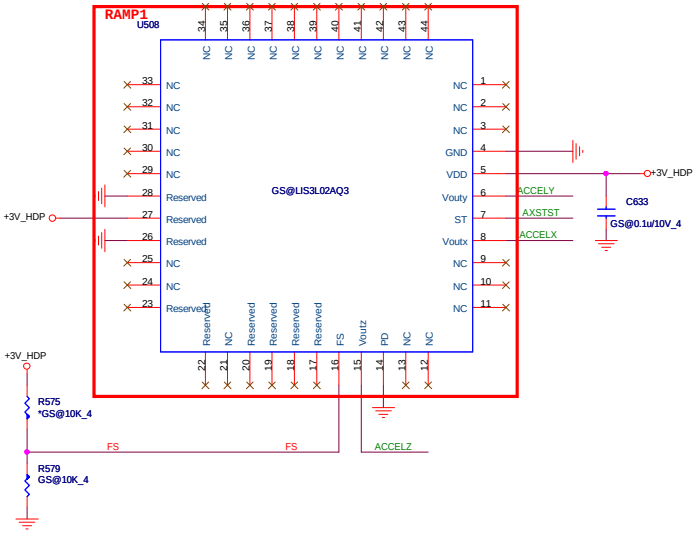


FS (Full Scale) selection

FS	0	1
	2g Full-Scale	6g Full-Scale

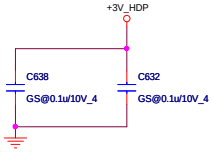
PD (Power Down) selection

PD	0	1
	Normal Mode	Power-down mode



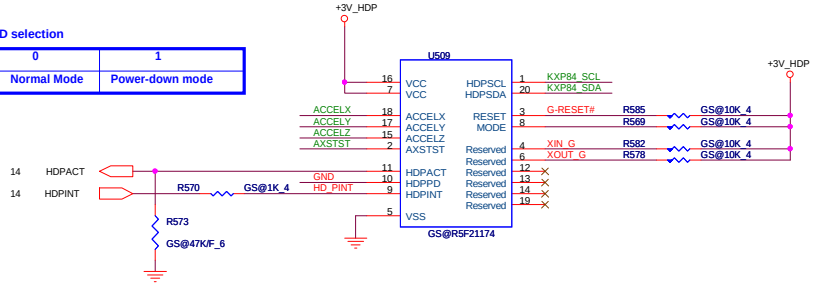
BOM Option Table

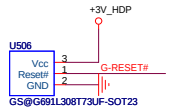
Reference	Description
GS@	G-SENSOR SEL

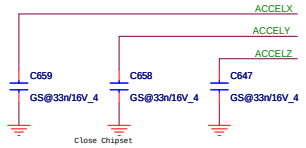


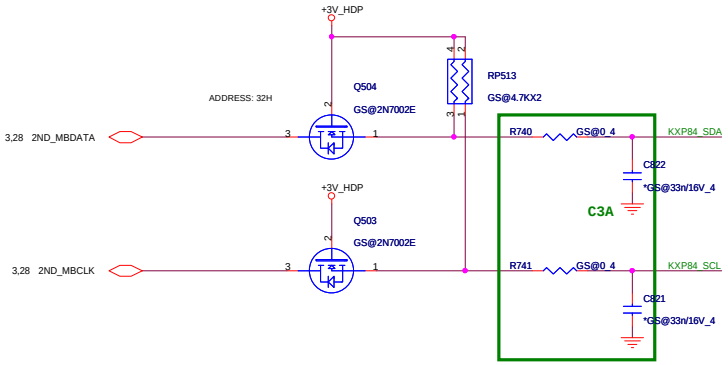
HDPPD selection

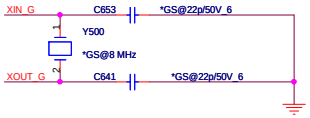
HDPPD	0	1
	Normal Mode	Power-down mode











Quanta Computer Inc.

PROJECT : TE1M

Size	Document Number	Rev
	HDD/ODD/G-SENSOR	E3D

Date: Monday, May 26, 2008 Sheet 22 of 40

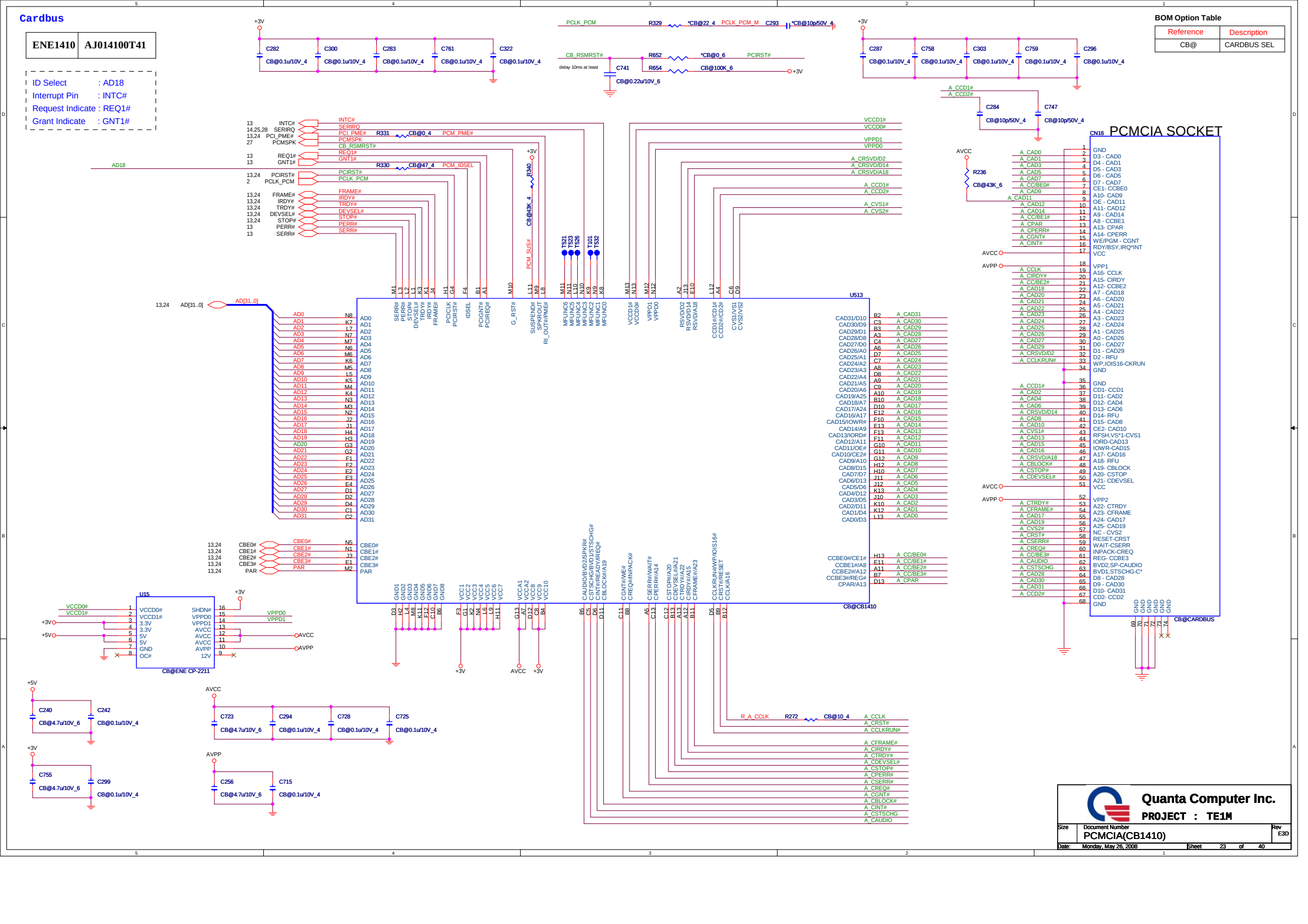
Cardbus

ENE1410	AJ014100T41

ID Select : AD18
Interrupt Pin : INTC#
Request Indicate : REQ1#
Grant Indicate : GNT1#

BOM Option Table

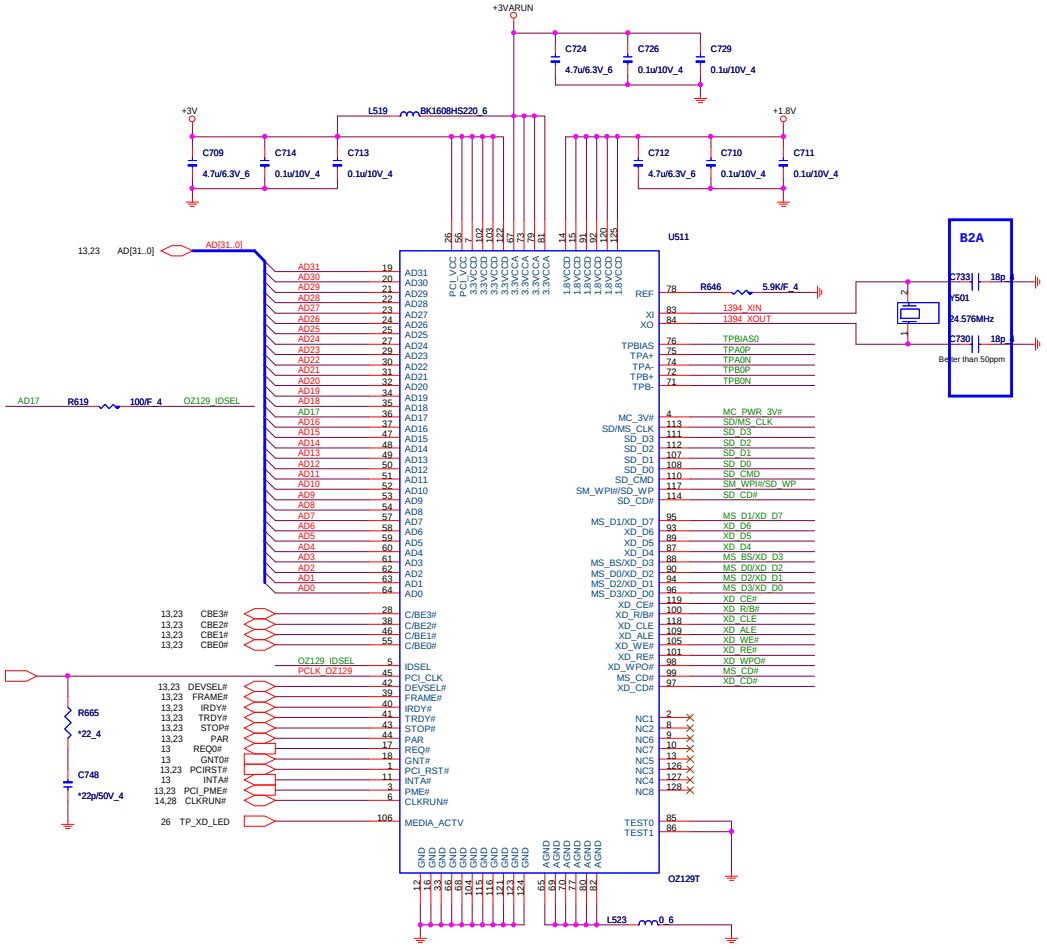
Reference	Description
CB@	CARDBUS SEL



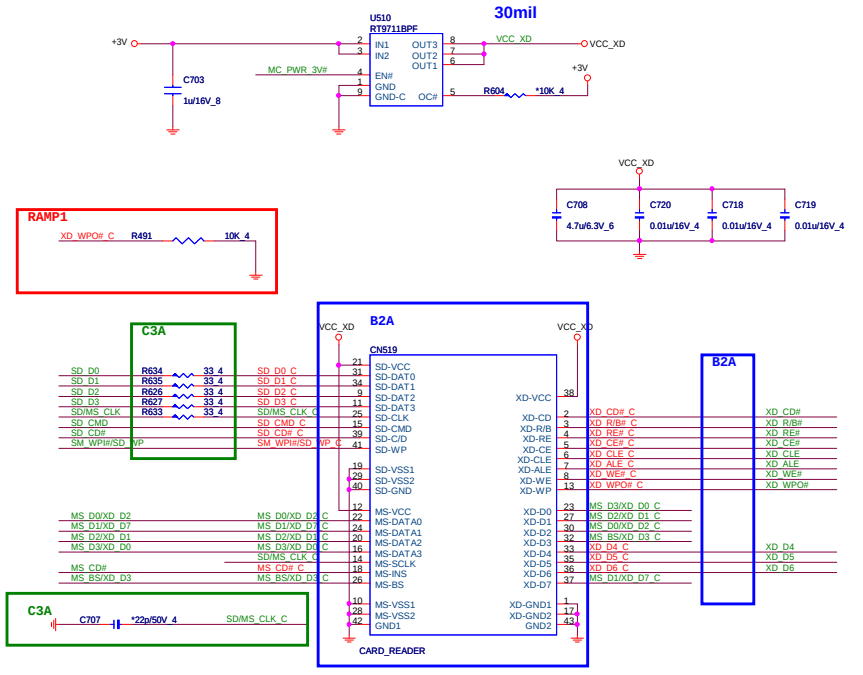
Quanta Computer Inc.		
PROJECT : TE1M		
Size	Document Number: PCMCIA(CB1410)	Rev: E3D
Date: Monday, May 26, 2008	Sheet 23 of 40	

OZ129 for Cardreader+1394

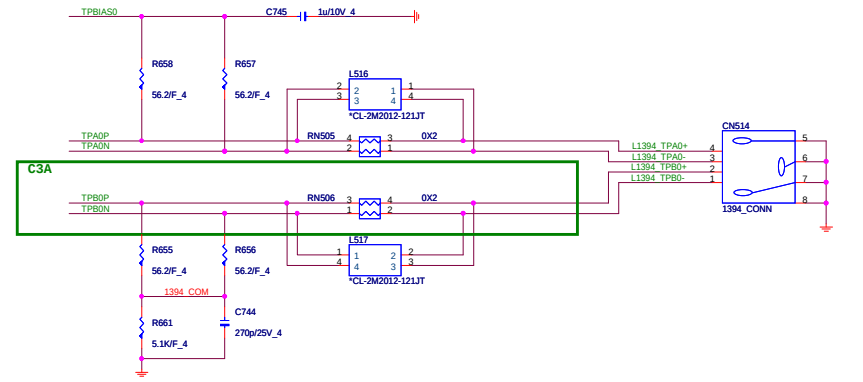
ID Select	: AD17
Interrupt Pin	: INTA#
Request Indicate	: REQ0#
Grant Indicate	: GNT0#



5 IN 1 Card reader



1394



Quanta Computer Inc.

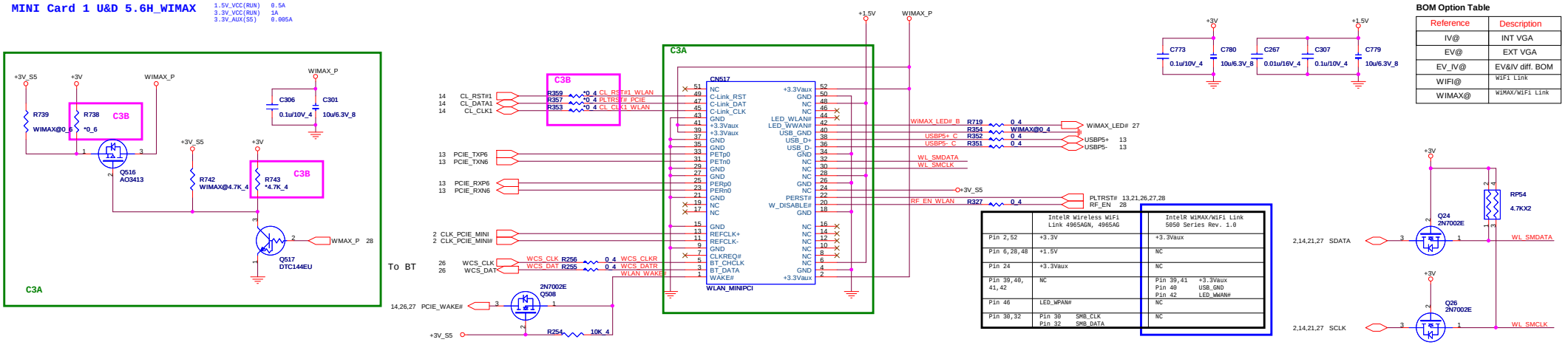
PROJECT : TE1M

Size	Document Number	Rev
	OZ129T(5in1/1394)	E3D

Date: Monday, May 26, 2008 Sheet 24 of 40

MINI Card 1 U&D 5.6H_WIMAX

1.5V_VCC(RUN) 0.5A
3.3V_VCC(RUN) 1A
3.3V_AUX(S5) 0.005A



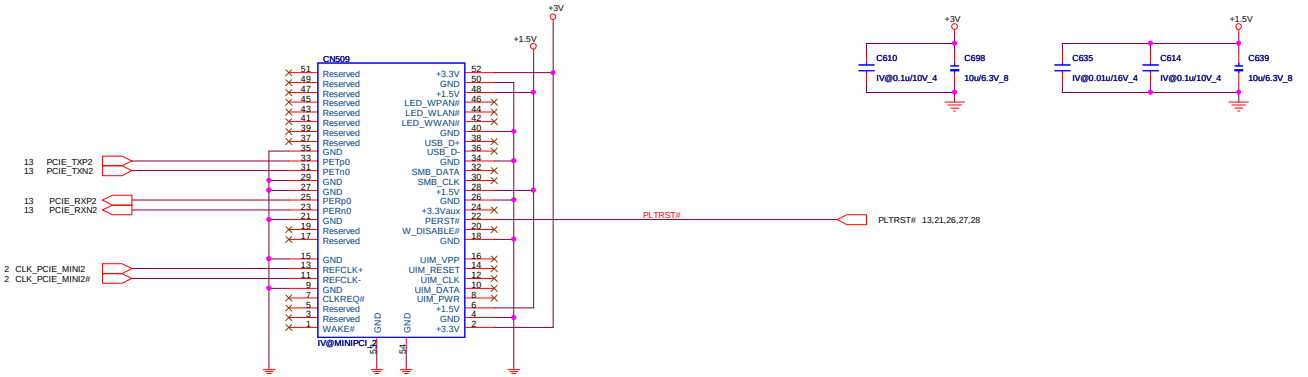
IntelR Wireless WiFi Link 4965AGN, 4965AG	IntelR WiMAX/WiFi Link 5050 Series Rev. 1.0
Pin 2,52 +3.3V	+3.3Vaux
Pin 6,28,48 +1.5V	NC
Pin 24 +3.3Vaux	NC
Pin 39,40, 41,42 NC	Pin 39,41 +3.3Vaux Pin 40 USB_GND Pin 42 LED_WWAN#
Pin 46 LED_WPAN#	NC
Pin 30,32 Pin 30 SMB_CLK Pin 32 SMB_DATA	NC

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA
EV_IV@	EV&IV diff. BOM
WIFI@	WiFi Link
WIMAX@	WiMAX/WiFi Link

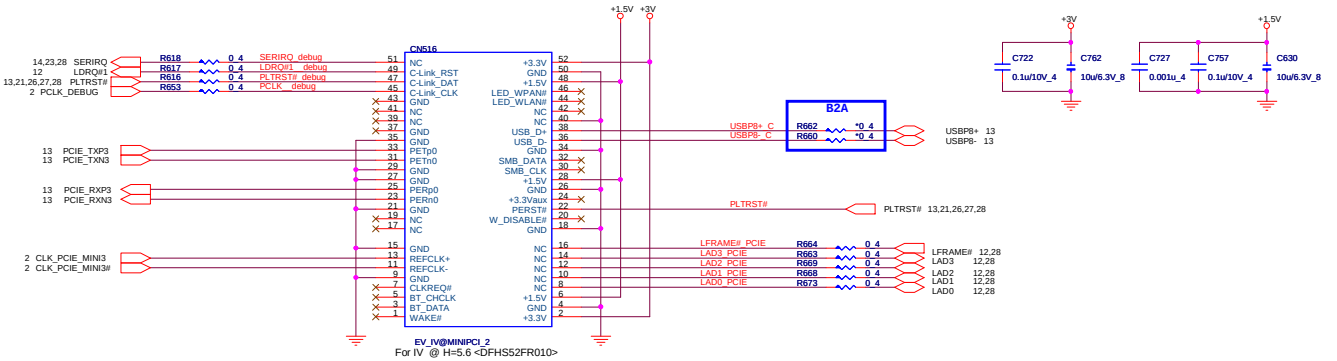
MINI Card 3 U 9H_HD-DVD

1.5V_VCC(RUN) 0.5A
3.3V_VCC(RUN) 1A



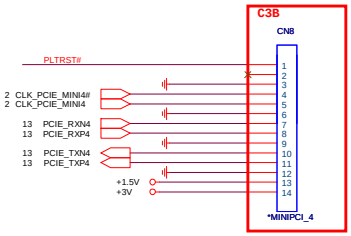
MINI Card 2
U 5.6H_TV/ROBOSON
D 7.5H_HD-DVD

1.5V_VCC(RUN) 0.5A
3.3V_VCC(RUN) 1A



For IV @ H=5.6 <DFHS52FR010>
For EV@ H=7.5 <DFHS52FR011>

MINI Card 4-D/Robson



Remark1:TV+Robson or HD-DVD+Robson or TV+HD-DVD for UMA SKU

Remark2:TV is just for UMA(13")

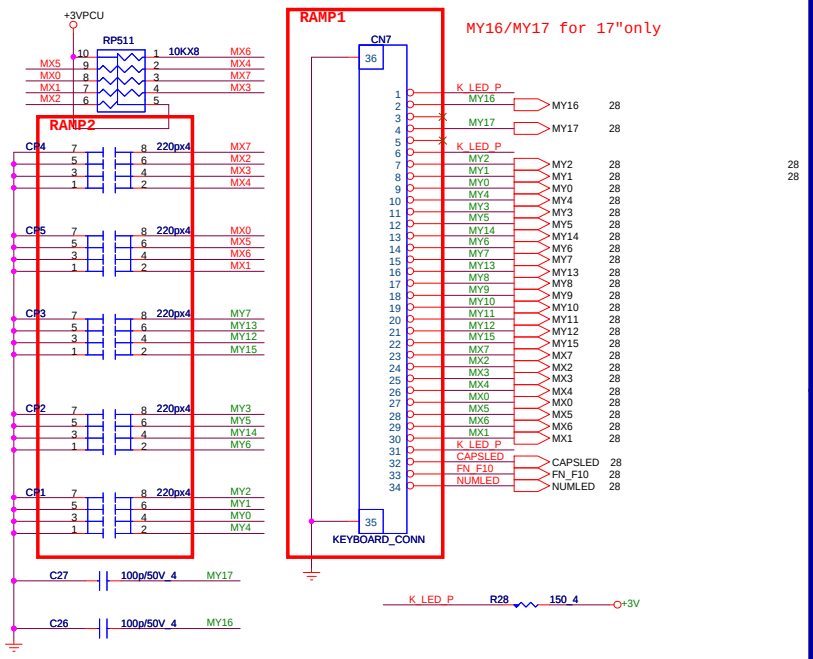
	UMA	Discrete
1	WLAN	WLAN
2	TV or Robson	HD-DVD
3	HD-DVD or Robson	N.C
4	N.C	Robson

Quanta Computer Inc.
PROJECT : TE1M

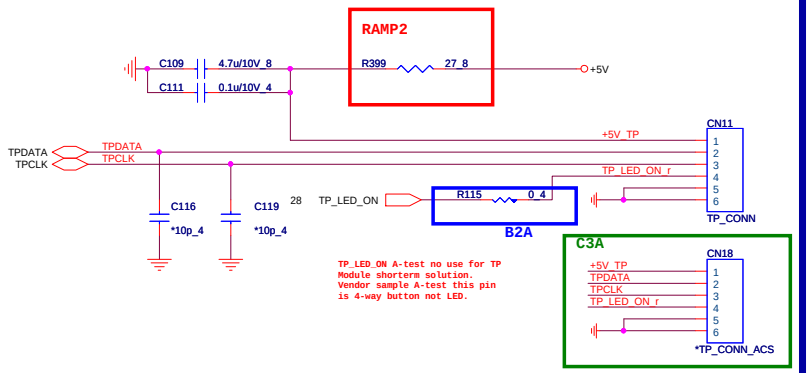
Size	Document Number	Rev
	MINI CARD	E3D

Date: Monday, May 26, 2008 Sheet 25 of 40

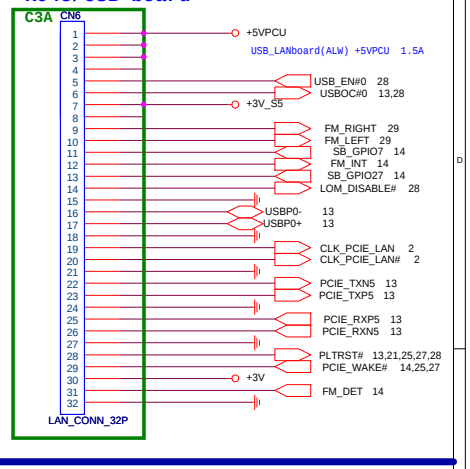
INT KeyBoard



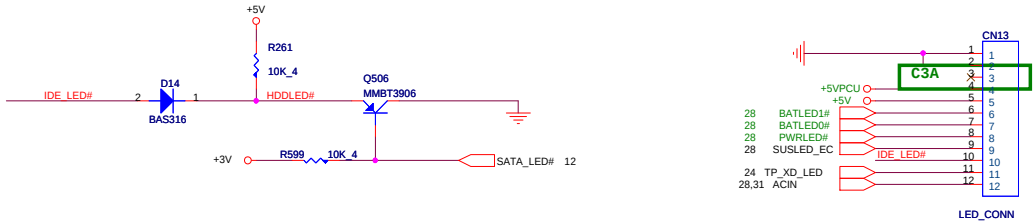
TP Board



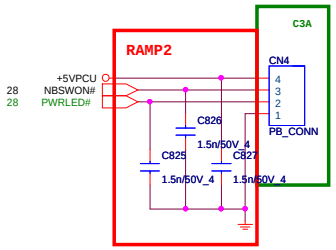
RJ45/USB board



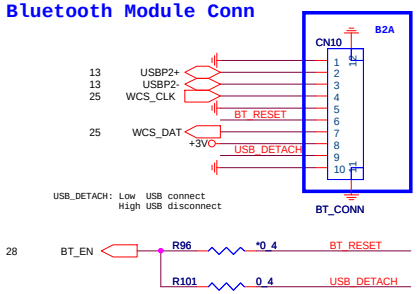
LED Board



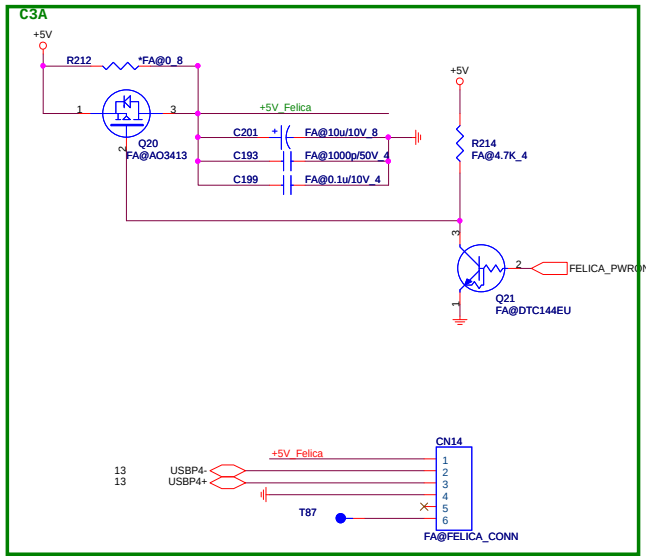
Power board



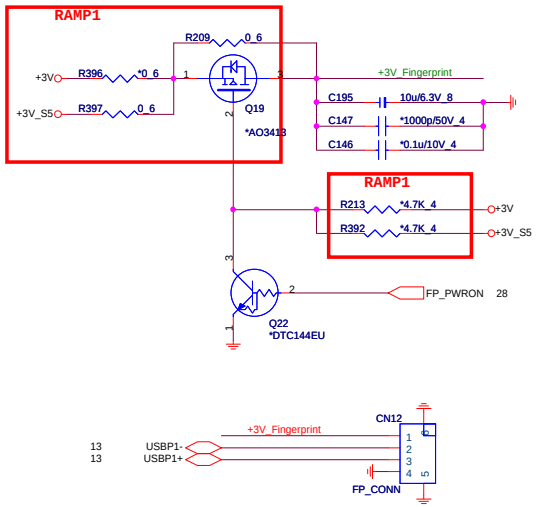
Bluetooth Module Conn



Felica



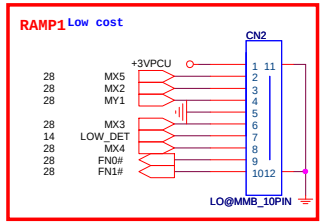
FP Board

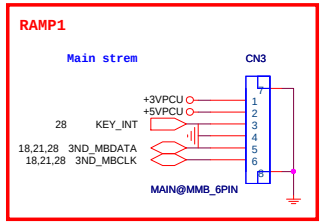


MMB

BOM Option Table

Reference	Description
LO@	LOW COST
MAIN@	MAINSTREM





Quanta Computer Inc.

PROJECT : TE1M

Size	Document Number	Rev
	New Card/Keyboard/WTB	E3D

Date: Friday, June 13, 2008 Sheet 26 of 40

New card (BTO)

BOM Option Table

Reference	Description
CB@	CARDBUS SEL

USB

E-SATA

W-LAN&BT LED

BOM Option Table

Reference	Description
LO@	LOW COST
MAIN@	MAINSTREM

Mainstream --> Orange
Low Cost --> Orange

WiMAX LED

Kill SW

Satellite LED

White Right angle type

Mainstream --> White
Low Cost --> N/A

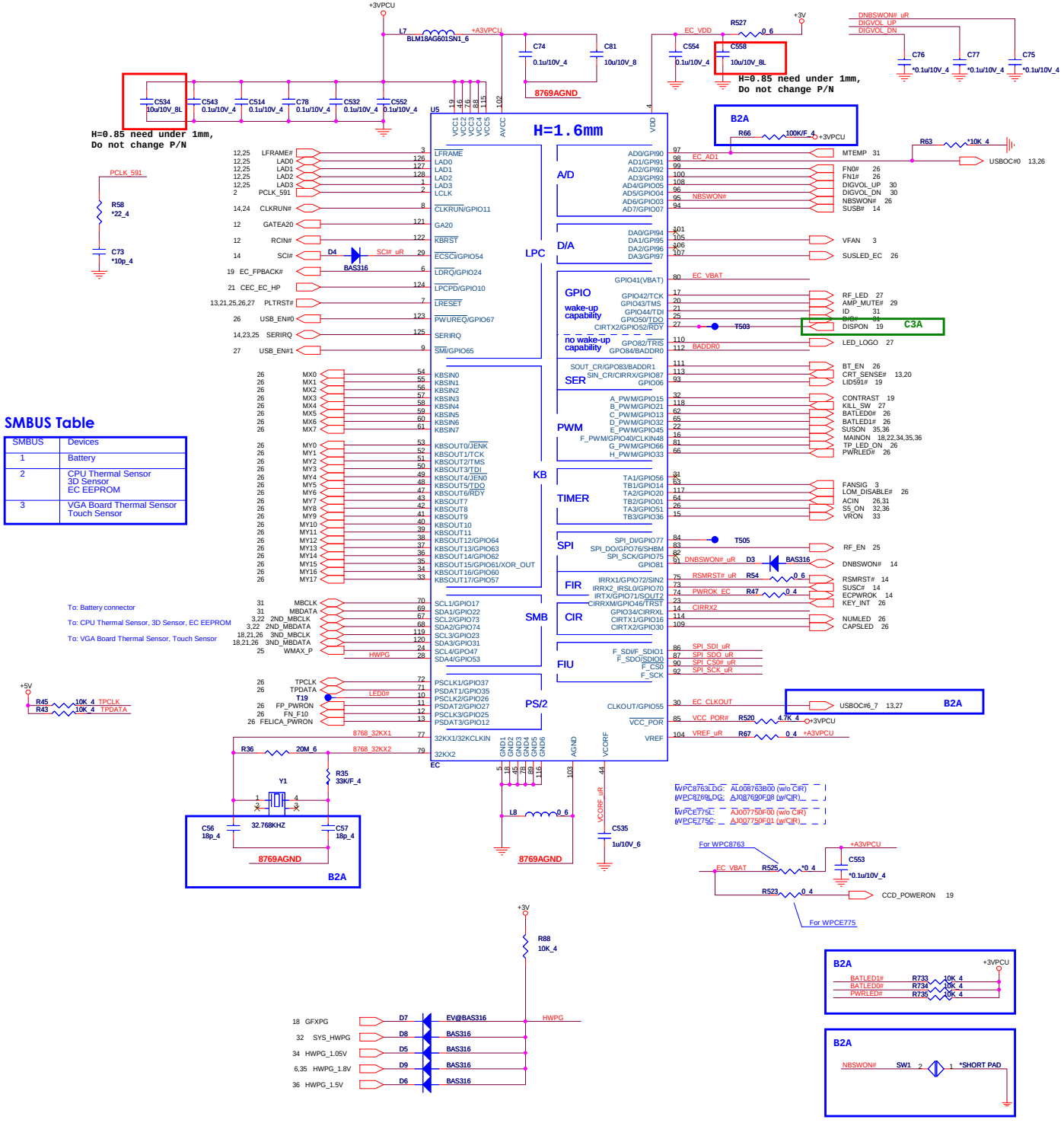
PC-Beep

Option SB to ESATA directly

Quanta Computer Inc.
PROJECT : TE1M

Size	Document Number	Rev
	TP/SW/LED	E3D
Date: Monday, May 26, 2008	Sheet 27 of 40	

EC

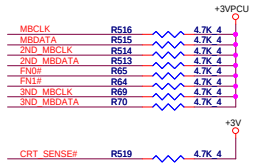


SMBUS Table

SMBUS	Devices
1	Battery
2	CPU Thermal Sensor 3D Sensor EC EEPROM
3	VGA Board Thermal Sensor Touch Sensor

To: Battery connector
To: CPU Thermal Sensor, 3D Sensor, EC EEPROM
To: VGA Board Thermal Sensor, Touch Sensor

SM BUS PU



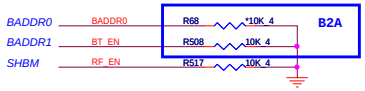
BOM Option Table

Reference	Description
EV@	EXT VGA
CIR@	CIR FUNC.
WOFP@	Debug switch

I/O Base Address

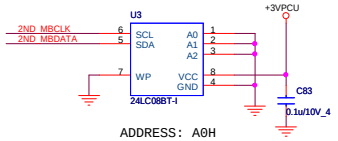
	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

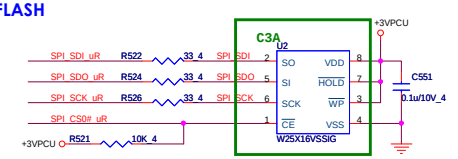


Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

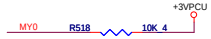
ID



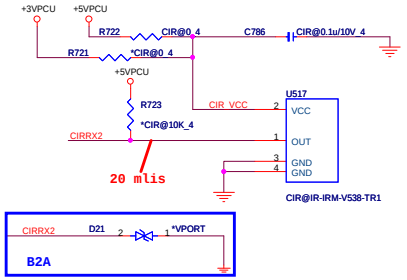
SPI FLASH



INTERNAL KEYBOARD STRIP SET

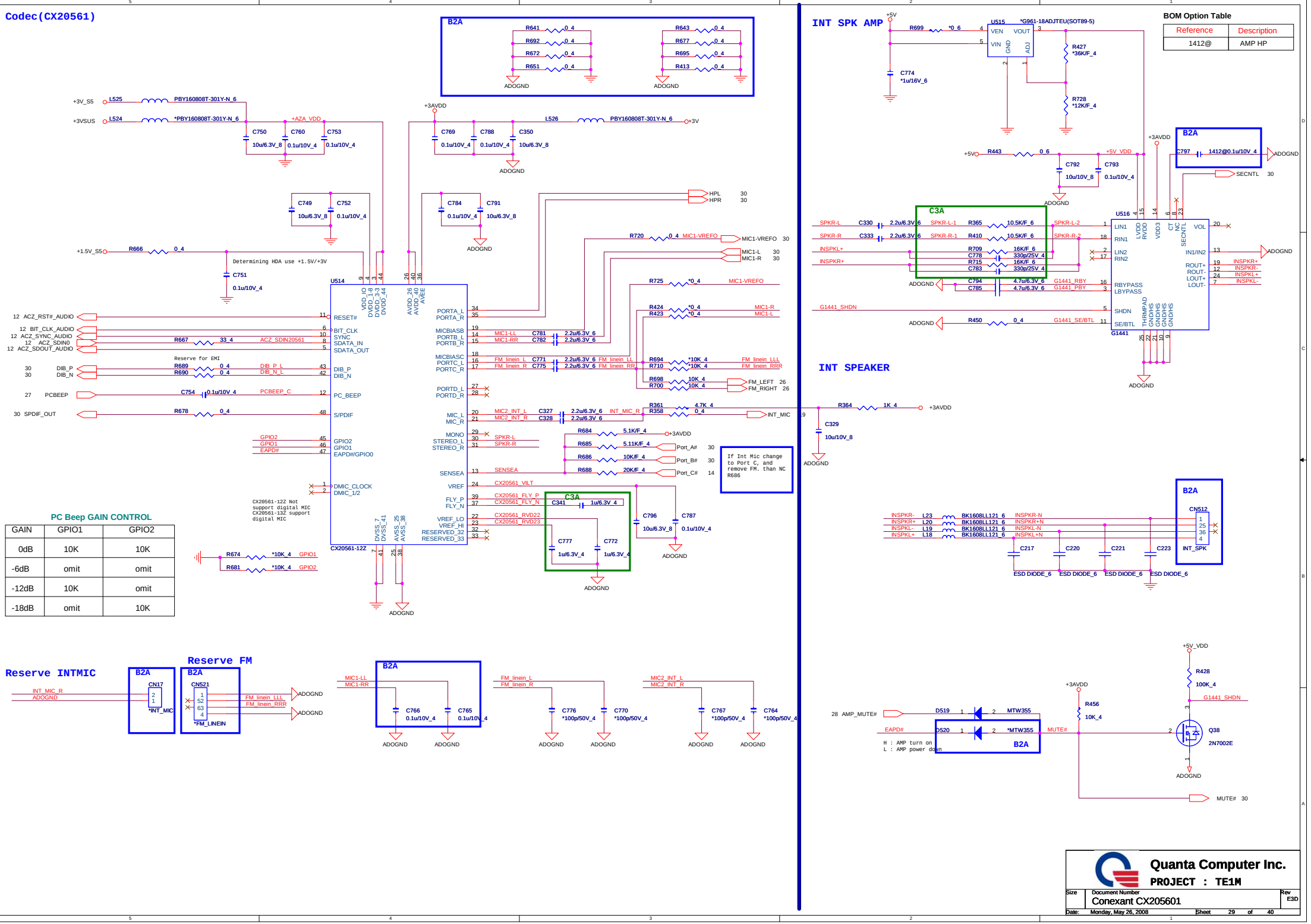


CIR



Quanta Computer Inc.
PROJECT : TE1M
Size: Document Number: EC-PC8763 Rev: E3D
Date: Saturday, June 14, 2008 Sheet 28 of 40

Codec(CX20561)



PC Beep GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

Reserve INTMIC

Reserve FM

INT SPK AMP

INT SPEAKER

BOM Option Table

Reference	Description
1412@	AMP HP

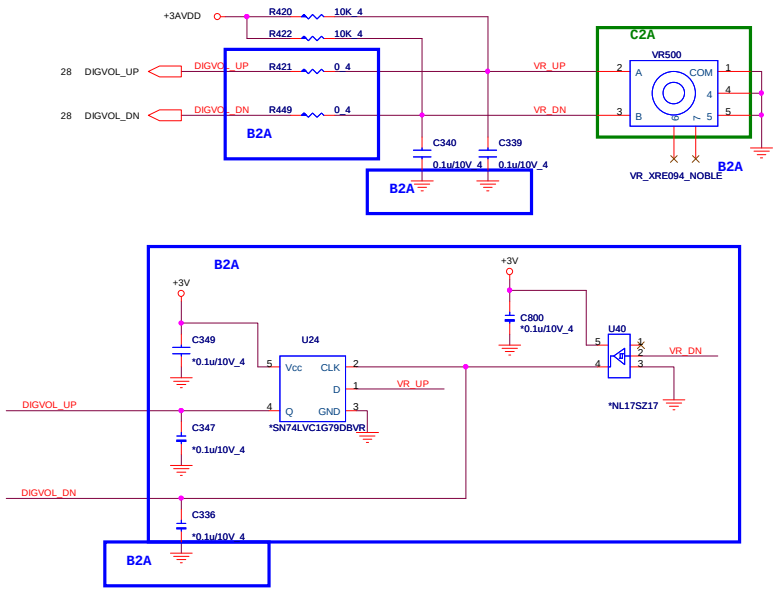
Quanta Computer Inc.

PROJECT : TE1M

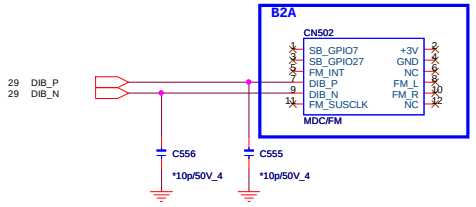
Size	Document Number	Rev
	Conexant CX205601	E3D

Date: Monday, May 26, 2008 Sheet 29 of 40

VR



FM Tuner MDC

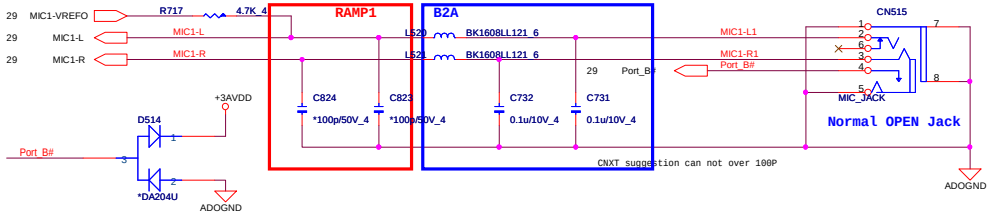


BOM Option Table

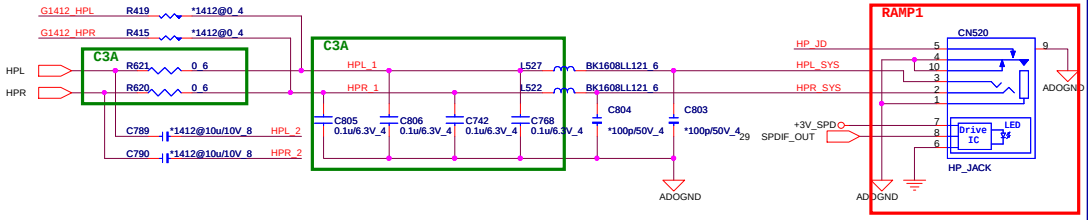
Reference	Description
1412@	AMP HP
CDCHP@	CODEC HP

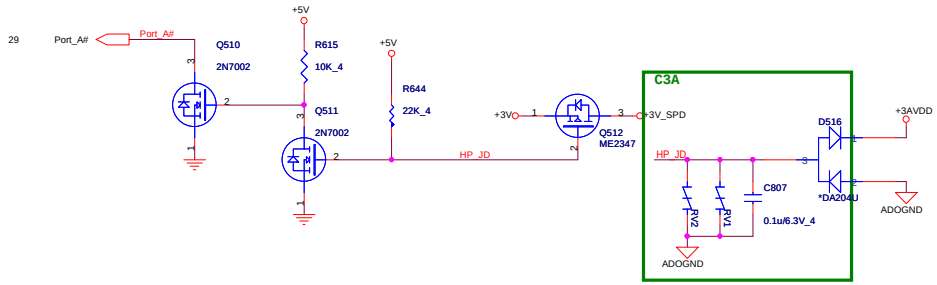
TE1M REV:A Stuff both for test

SYSTEM MIC

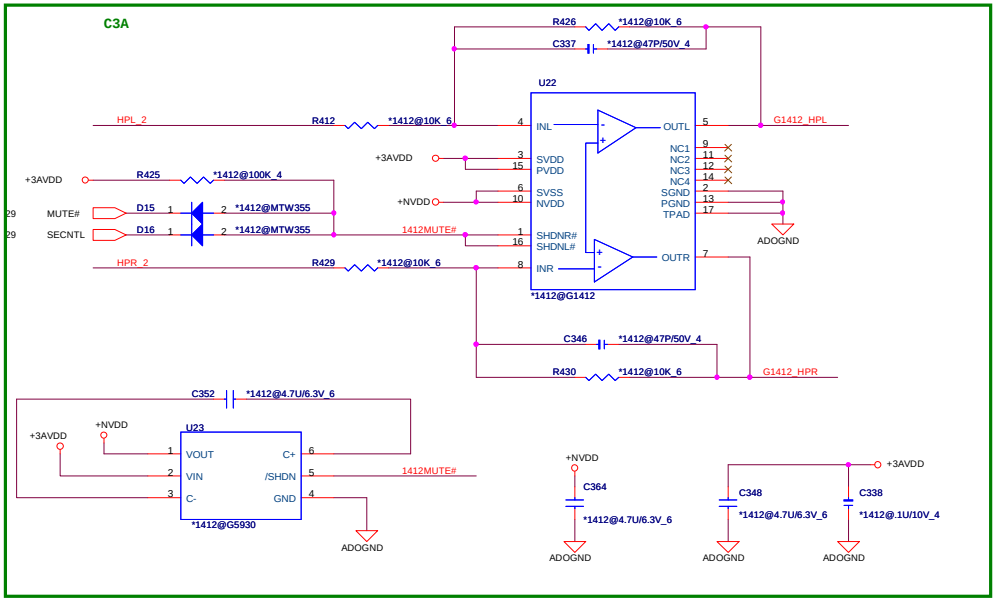


HP

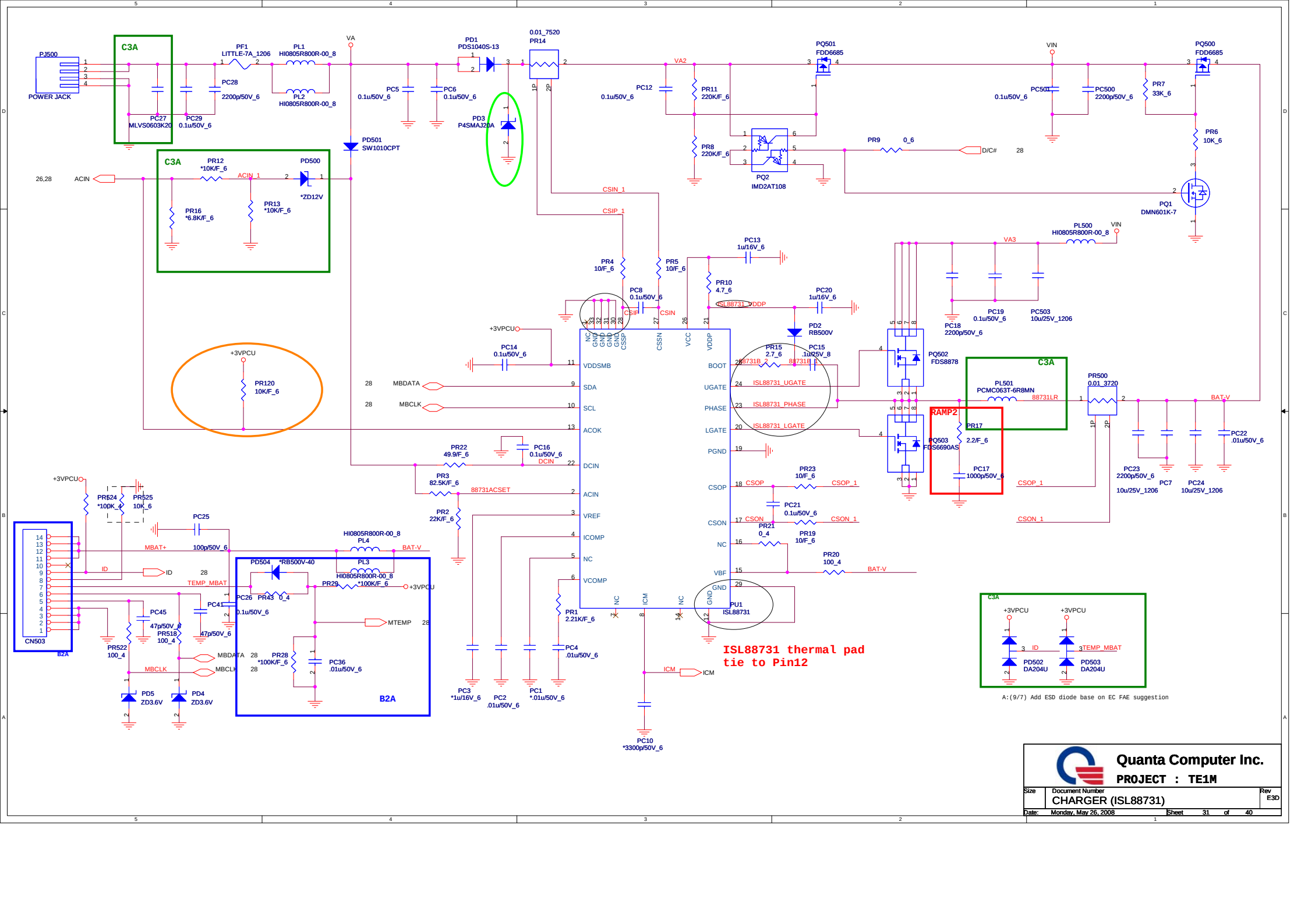


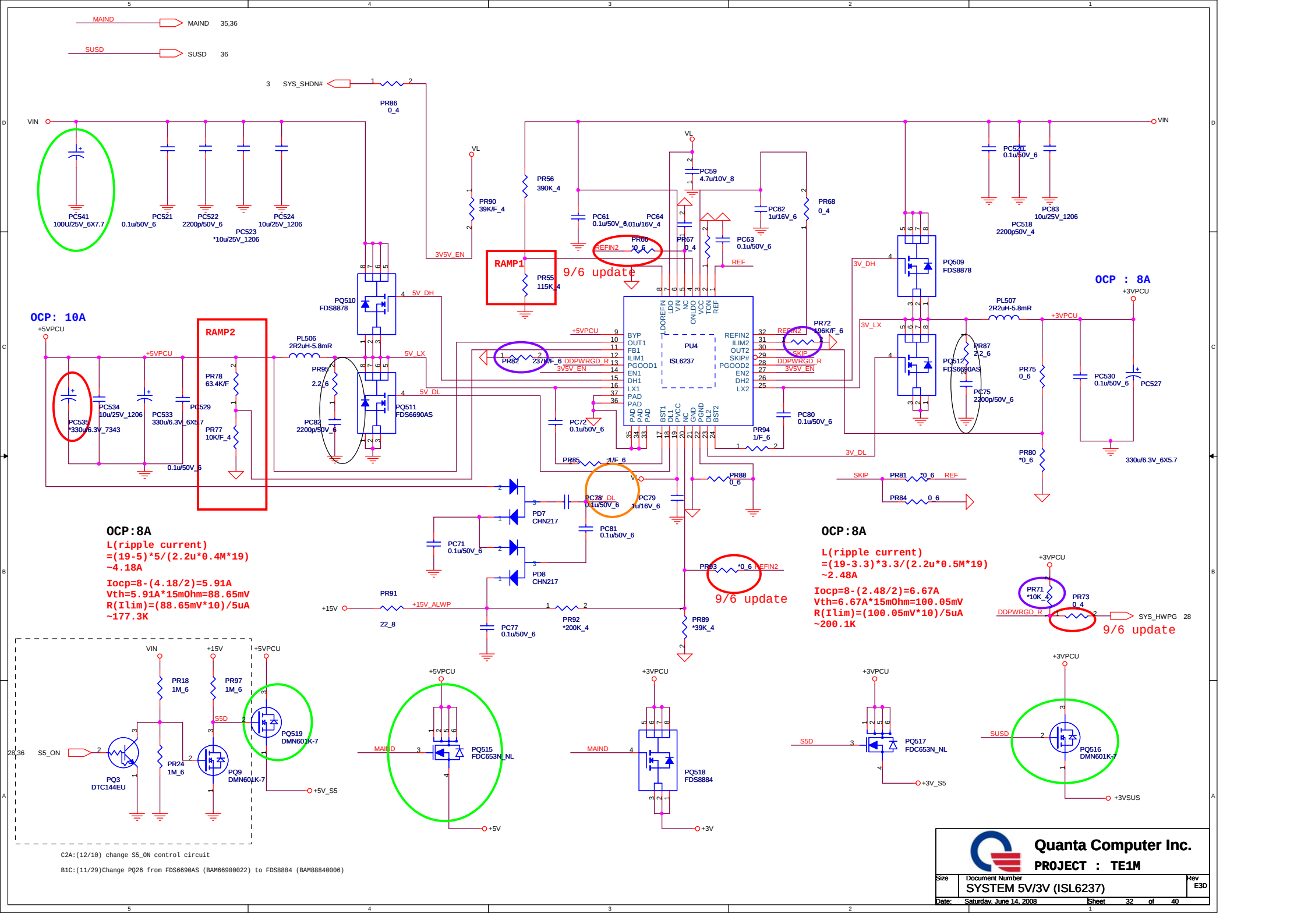


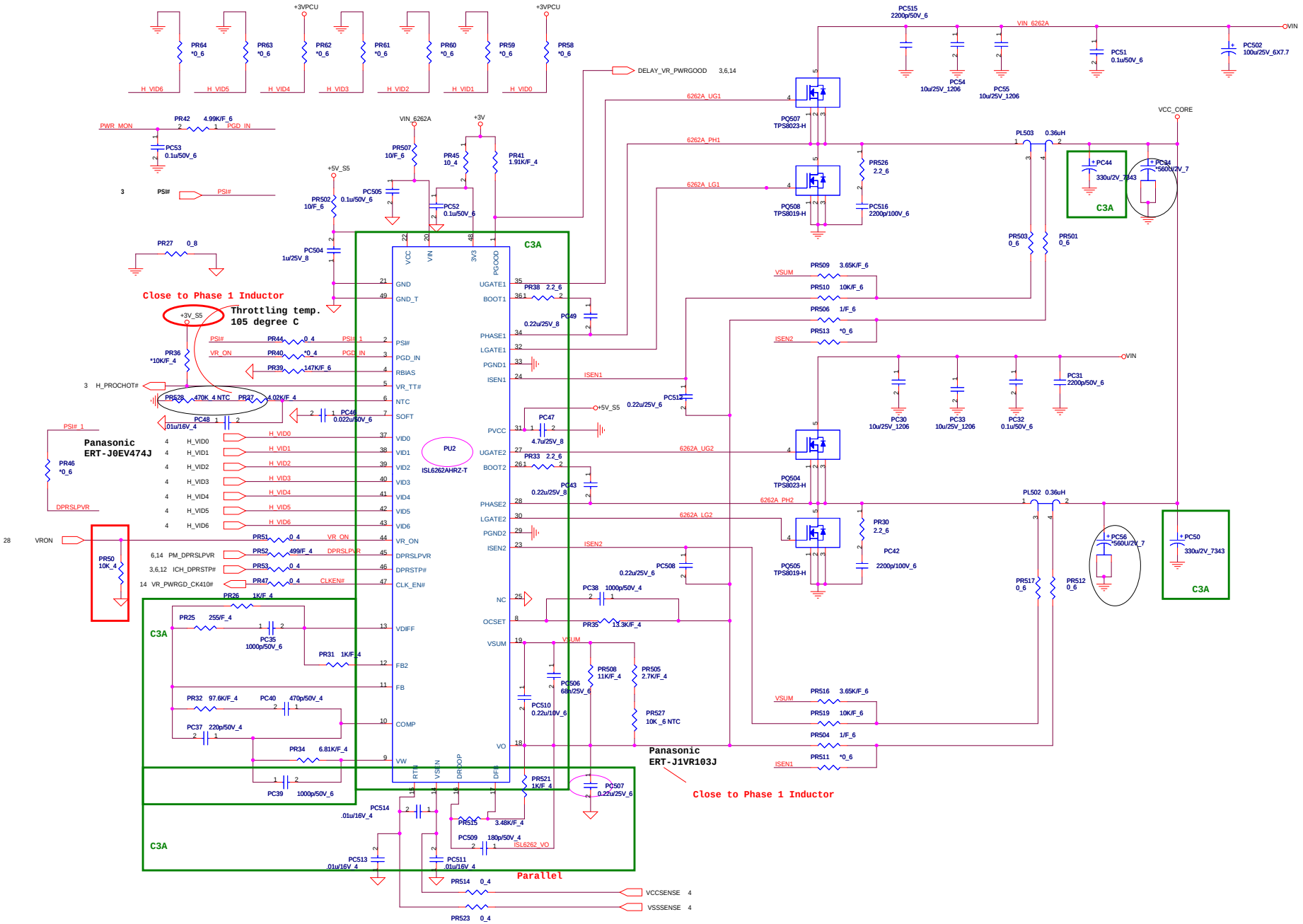
HP Amplifier

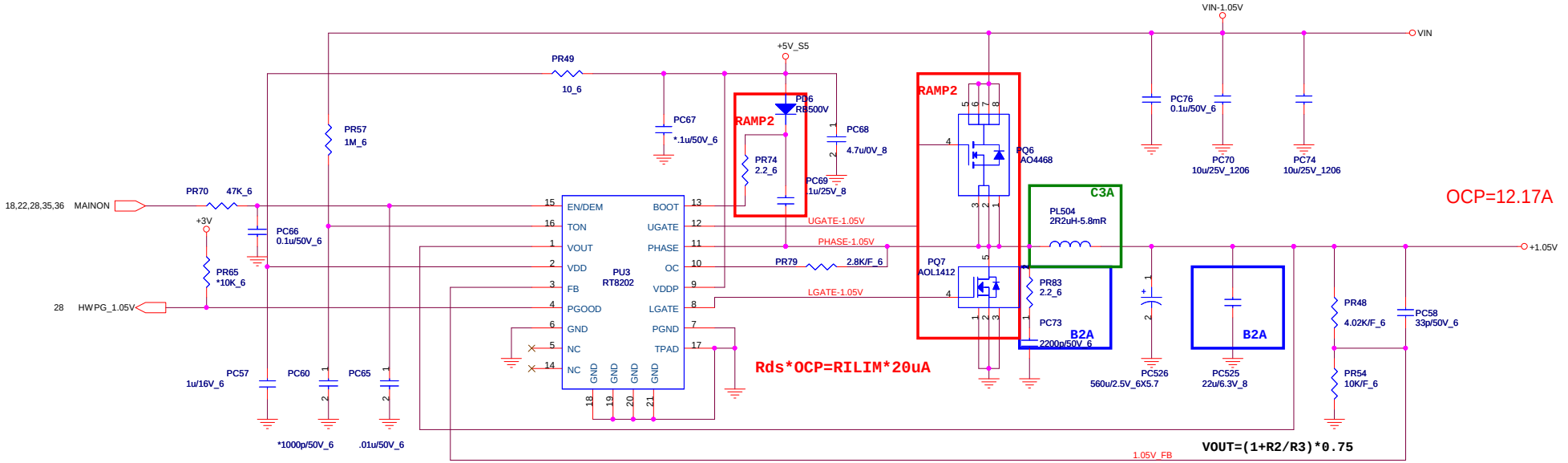


Quanta Computer Inc.		
PROJECT : TE1M		
Size	Document Number: Audio JACK/VR/FM	Rev: E3D
Date: Monday, May 26, 2008	Sheet 30 of 40	


PJ500
POWER JACK
C3A
PF1
LITTLE-7A_1206
PL1
HI0805R800R-00_8
PL2
HI0805R800R-00_8
PC28
2200p/50V_6
PC27
MLVS0603K20
PC29
0.1u/50V_6
VA
PC5
0.1u/50V_6
PC6
0.1u/50V_6
PD1
PDS1040S-13
PD3
P4SMAJ20A
0.01_7520
PR14
1P
2P
PD501
SW1010CPT
C3A
PR12
*10K/F_6
ACIN_1
PD500
*ZD12V
26,28
ACIN
PR16
*6.8K/F_6
PR13
*10K/F_6
PR120
10K/F_6
+3VPCU
CSIN_1
CSIP_1
VA2
PC12
0.1u/50V_6
PR11
220K/F_6
PR8
220K/F_6
PQ501
FDD6685
PQ2
IMD2AT108
PR9
0_6
D/C#
28
VIN
PC501
0.1u/50V_6
PC500
2200p/50V_6
PR7
33K_6
PQ500
FDD6685
PR6
10K_6
PQ1
DMN601K-7
PR4
10/F_6
PR5
10/F_6
PC8
0.1u/50V_6
CSIP
CSIN
PC13
1u/16V_6
PR10
4.7_6
ISL88731_VDDP
PC20
1u/16V_6
PD2
RB500V
PC14
0.1u/50V_6
28
MBDATA
MBCLK
PR22
49.9/F_6
PC16
0.1u/50V_6
DCIN
PR3
82.5K/F_6
88731ACSET
PR2
22K/F_6
PC3
*1u/16V_6
PC2
.01u/50V_6
PC1
*.01u/50V_6
PC4
.01u/50V_6
PR1
2.21K/F_6
PC10
*3300p/50V_6
ICM
NC
GND
GND
GND
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
PU1
ISL88731
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
CSOP_1
CSON_1
PR23
10/F_6
PC21
0.1u/50V_6
PR21
0_4
PR19
10/F_6
PR20
100_4
BAT-V
ISL88731 thermal pad
tie to Pin12
VA3
PL500
HI0805R800R-00_8
PC19
0.1u/50V_6
PC503
10u/25V_1206
PC18
2200p/50V_6
PQ502
FDS8878
PQ503
FDS6690AS
C3A
PL501
PCMC063T-6R8MN
88731LR
RAMP2
PR17
2.2/F_6
PC17
1000p/50V_6
PR500
0.01_3720
BAT-V
PC23
2200p/50V_6
PC7
PC24
10u/25V_1206
PC22
.01u/50V_6
+3VPCU
PR524
*100K_6
PR525
10K_6
PC25
100p/50V_6
MBAT+
ID
TEMP_MBAT
CN503
B2A
PC45
47p/50V_6
PR518
100_4
PC41
47p/50V_6
PR522
100_4
MBDATA
MBCLK
PD5
ZD3.6V
PD4
ZD3.6V
HI0805R800R-00_8
PL4
PL3
HI0805R800R-00_8
PD504
*RB500V-40
PR29
*100K/F_6
PC26
0.1u/50V_6
PR43
0_4
PR28
*100K/F_6
PC36
.01u/50V_6
MTEMP
B2A
C3A
+3VPCU
+3VPCU
ID
TEMP_MBAT
PD502
DA204U
PD503
DA204U
A:(9/7) Add ESD diode base on EC FAE suggestion
Quanta Computer Inc.
PROJECT : TE1M
Size
Document Number
CHARGER (ISL88731)
Rev
E3D
Date: Monday, May 26, 2008
Sheet 31 of 40


MAIND
MAIND 35,36
SUSD
SUSD 36
3 SYS_SHDN#
PR86 0_4
VIN
PC541 100U/25V_6X7.7
PC521 0.1u/50V_6
PC522 2200p/50V_6
PC523 *10u/25V_1206
PC524 10u/25V_1206
VL
PR90 39K/F_4
3V5V_EN
PR56 390K_4
PC61 0.1u/50V_6
PC64 0.01u/16V_4
PR66 *0_6
REFIN2
RAMP1
PR55 115K_4
9/6 update
PC59 4.7u/10V_8
PR67 0_4
PC62 1u/16V_6
PR68 0_4
PC63 0.1u/50V_6
REF
PC520 0.1u/50V_6
PC83 10u/25V_1206
PC518 2200p50V_4
OCP: 10A
OCP : 8A
+5VPCU
+3VPCU
RAMP2
PR78 63.4K/F
PR77 10K/F_4
PL506 2R2uH-5.8mR
PR95 2.2_6
PC82 2200p/50V_6
5V_DH
5V_LX
5V_DL
PQ510 FDS8878
PQ511 FDS6690AS
PC534 10u/25V_1206
PC533 330u/6.3V_6X5.7
PC529
PC535 *330u/6.3V_7343
0.1u/50V_6
PR82 237K/F_6
DDPWRGD_R
3V5V_EN
PU4
ISL6237
PR72 196K/F_6
SKIP
PC72 0.1u/50V_6
PC80 0.1u/50V_6
PR94 1/F_6
PR85 1/F_6
PR88 0_6
PC78 0.1u/50V_6
PC79 1u/16V_6
PC81 0.1u/50V_6
PD7 CHN217
PD8 CHN217
PC71 0.1u/50V_6
PR91 22_8
+15V
+15V_ALWP
PR92 *200K_4
PC77 0.1u/50V_6
PR89 *39K_4
PR93 *0_6
3V_DH
3V_LX
3V_DL
PQ509 FDS8878
PQ512 FDS6690AS
PL507 2R2uH-5.8mR
PR87 2.2_6
PC75 2200p/50V_6
PR75 0_6
PR80 *0_6
PC530 0.1u/50V_6
PC527
330u/6.3V_6X5.7
PR81 *0_6
PR84 0_6
OCP:8A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=8-(4.18/2)=5.91A
Vth=5.91A*15mOhm=88.65mV
R(Ilim)=(88.65mV*10)/5uA
~177.3K
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=100.05mV
R(Ilim)=(100.05mV*10)/5uA
~200.1K
PR71 *10K_4
PR73 0_4
DDPWRGD_R
SYS_HWPG 28
9/6 update
28,36 S5_ON
PR18 1M_6
PR97 1M_6
PR24 1M_6
S5D
PQ3 DTC144EU
PQ9 DMN601K-7
PQ519 DMN601K-7
+5V_S5
PQ515 FDC653N_NL
+5V
PQ518 FDS8884
+3V
PQ517 FDC653N_NL
+3V_S5
PQ516 DMN601K-7
SUSD
+3VSUS
C2A:(12/10) change S5_ON control circuit
B1C:(11/29)Change PQ26 from FDS6690AS (BAM66900022) to FDS8884 (BAM88840006)
Quanta Computer Inc.
PROJECT : TE1M
Size
Document Number
SYSTEM 5V/3V (ISL6237)
Rev
E3D
Date: Saturday, June 14, 2008
Sheet 32 of 40


Close to Phase 1 Inductor
Throttling temp.
105 degree C
Panasonic
ERT-J0EV474J
ISL6262AHRZ-T
PU2
C3A
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
Parallel
Quanta Computer Inc.
PROJECT : TE1M
CPU CORE(ISL6262A)
Saturday, June 14, 2008
Sheet 33 of 40

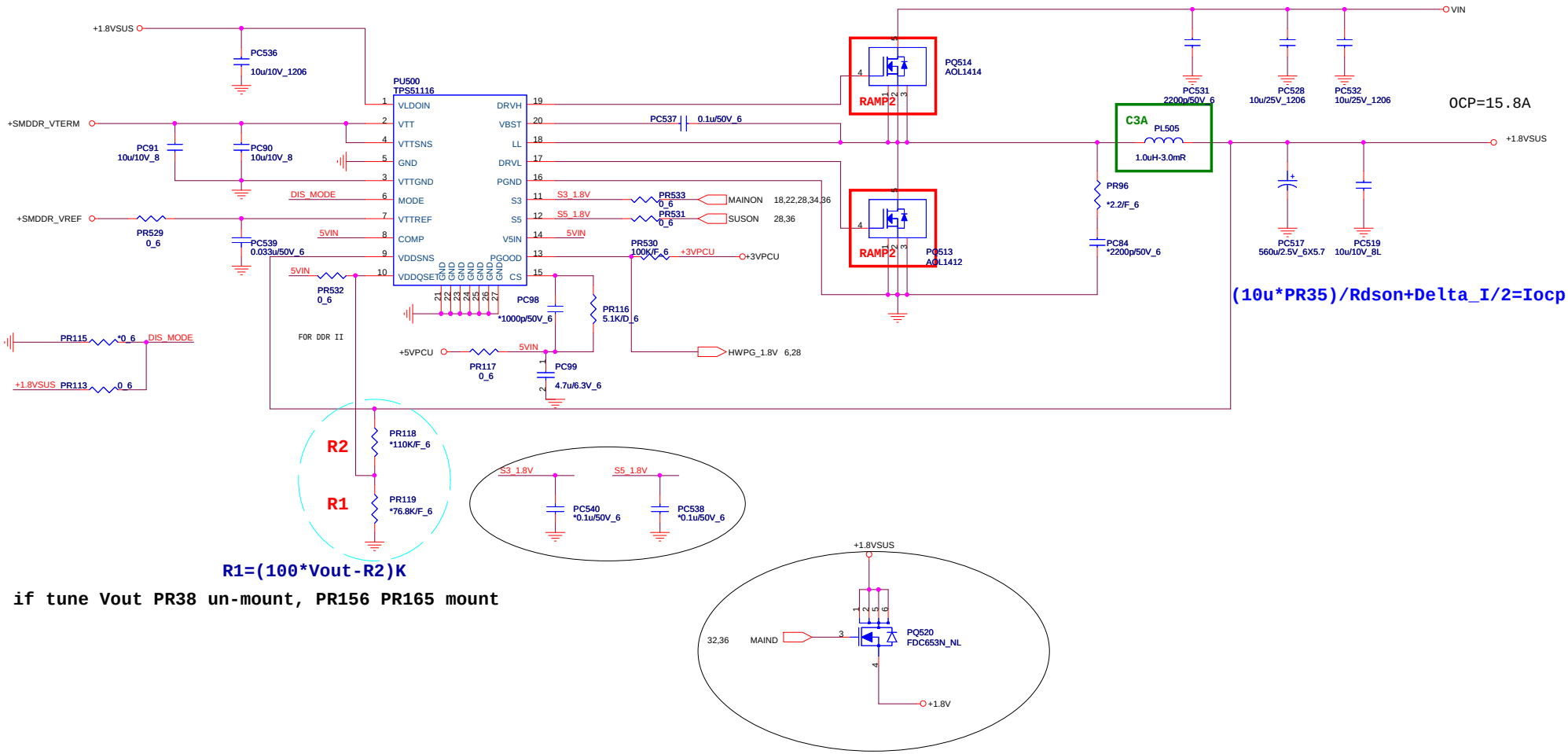


TON=3.85p*RTON*Vout/(Vin-0.5)

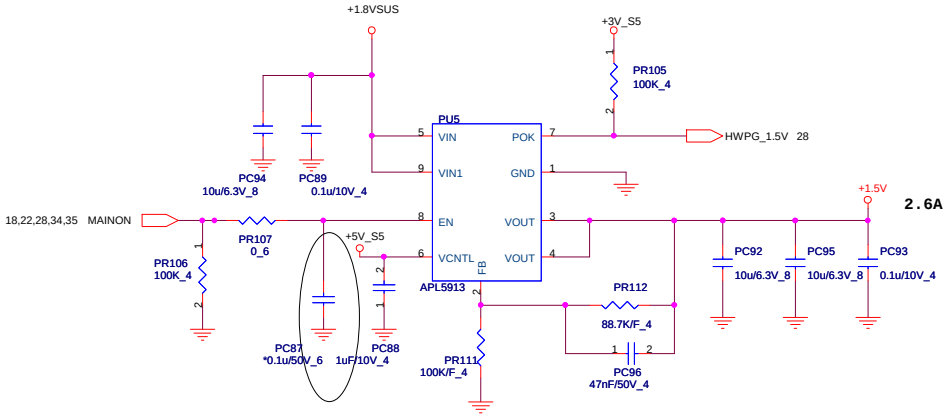
Frequency=Vout/(Vin*TON)

AO1412 Rds=4.6mOhm
12.17A OCP --- OC=2.8K(CS22803F914)

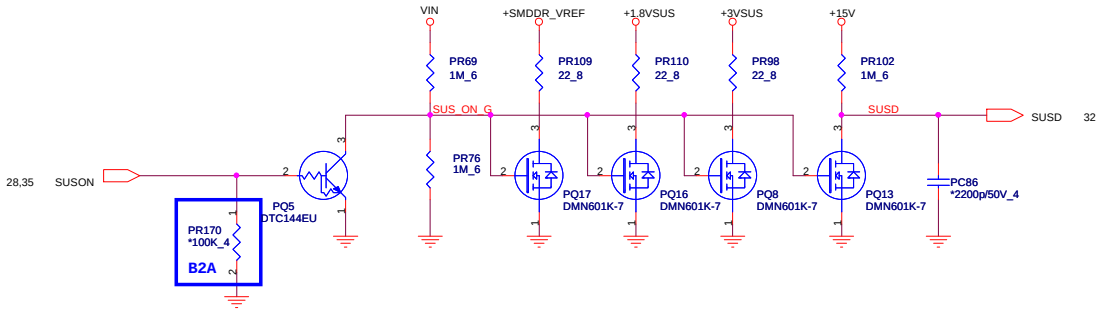
Quanta Computer Inc.		
PROJECT : TE1M		
Size	Document Number: VTT 1.05V (RT8202)	Rev: E3D
Date: Saturday, June 14, 2008	Sheet 34 of 40	

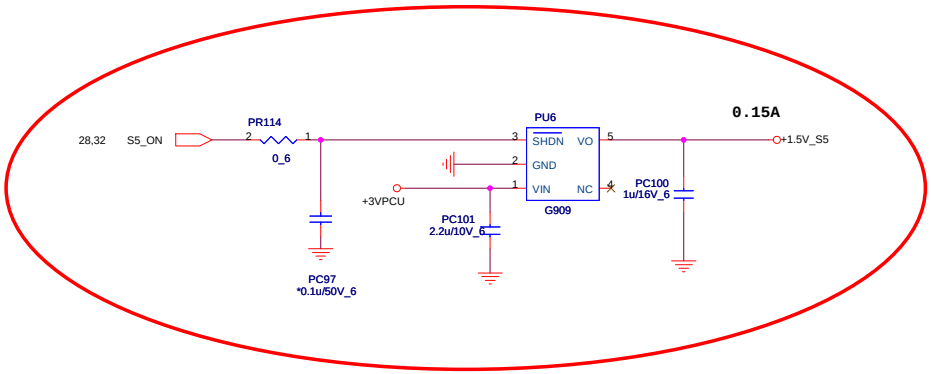


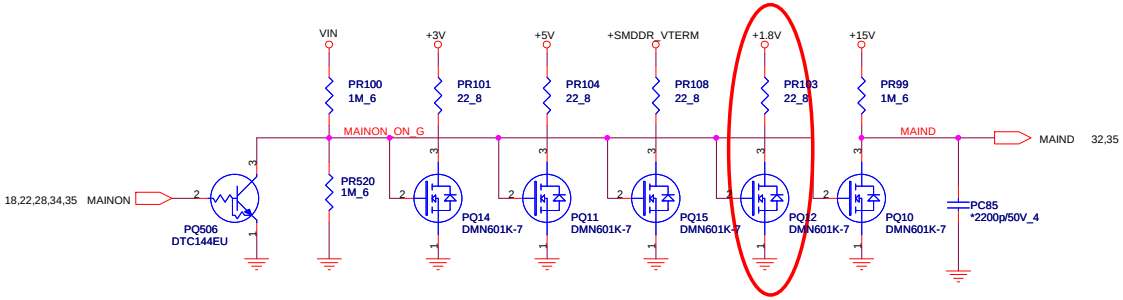
Quanta Computer Inc.		
PROJECT : TE1M		
Size	Document Number: DDR 1.8V(TPS51116)	Rev: E3D
Date: Monday, July 28, 2008	Sheet 35 of 40	



Vout =0.8(1+R1/R2)
=1.25V







Quanta Computer Inc.

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	Discharge/1.25/1.5	E3D

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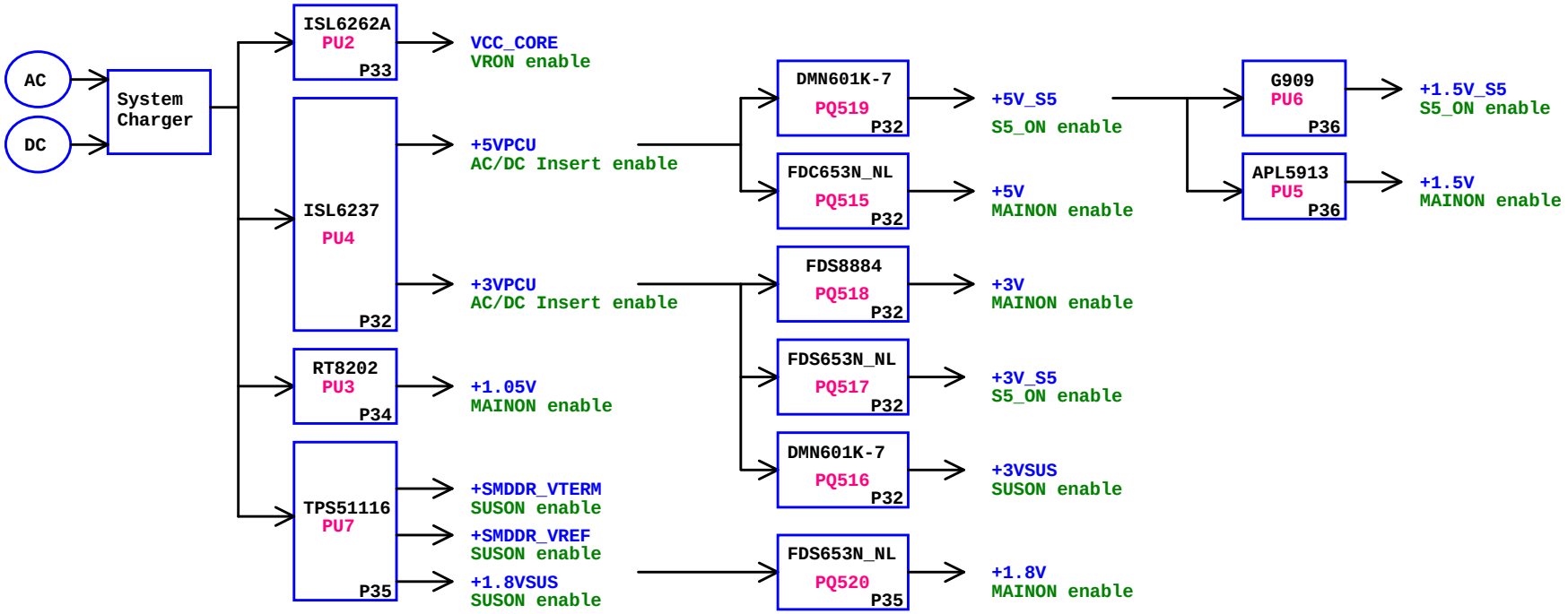
Power Tree Table



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH9M, HDMI, MMB, Power Board, RJ45/USB Board, LED Board, USB, CIR
+3VPCU	ICH9M, HALL SENSOR, LCD/LED Panel, KB, MMB, Kill SW, EC, SPI Flash, CIR, ID
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+1.8VSUS	GMCH, DDR
+SMDDR_VREF	GMCH, DDR
+SMDDR_VTERM	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH9M
+5V_S5	ICH9M, G-SENSOR
+5V	CPU, ICH9M, VGA, Camera, CRT, HDMI, SATA HDD, SATA ODD, PCMCIA, TP/LED Board, Felica, WiMAX LED, EC, INT SPK AMP, HP
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH9M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PCMCIA, Cardreader(OZ129T) Mini Card, KB, FP/LED Board, RJ45/USB Board, Bluetooth, New Card, PC Beep, EC, Codec(CX20561), HP, FM Tuner/MDC
+3V_S5	ICH9M, HDMI, Mini Card, RJ45/USB Board, New Card, Codec(CX20561)
+3VSUS	Codec(CX20561)
+1.8V	Cardreader(OZ129T)
+1.5V_S5	ICH9M, Codec(CX20561)