

Compal Confidential

HTW00 LA-2871 Schematics Document

Intel Dothan with 915PM(GM)/910GML + DDRII + ICH6M

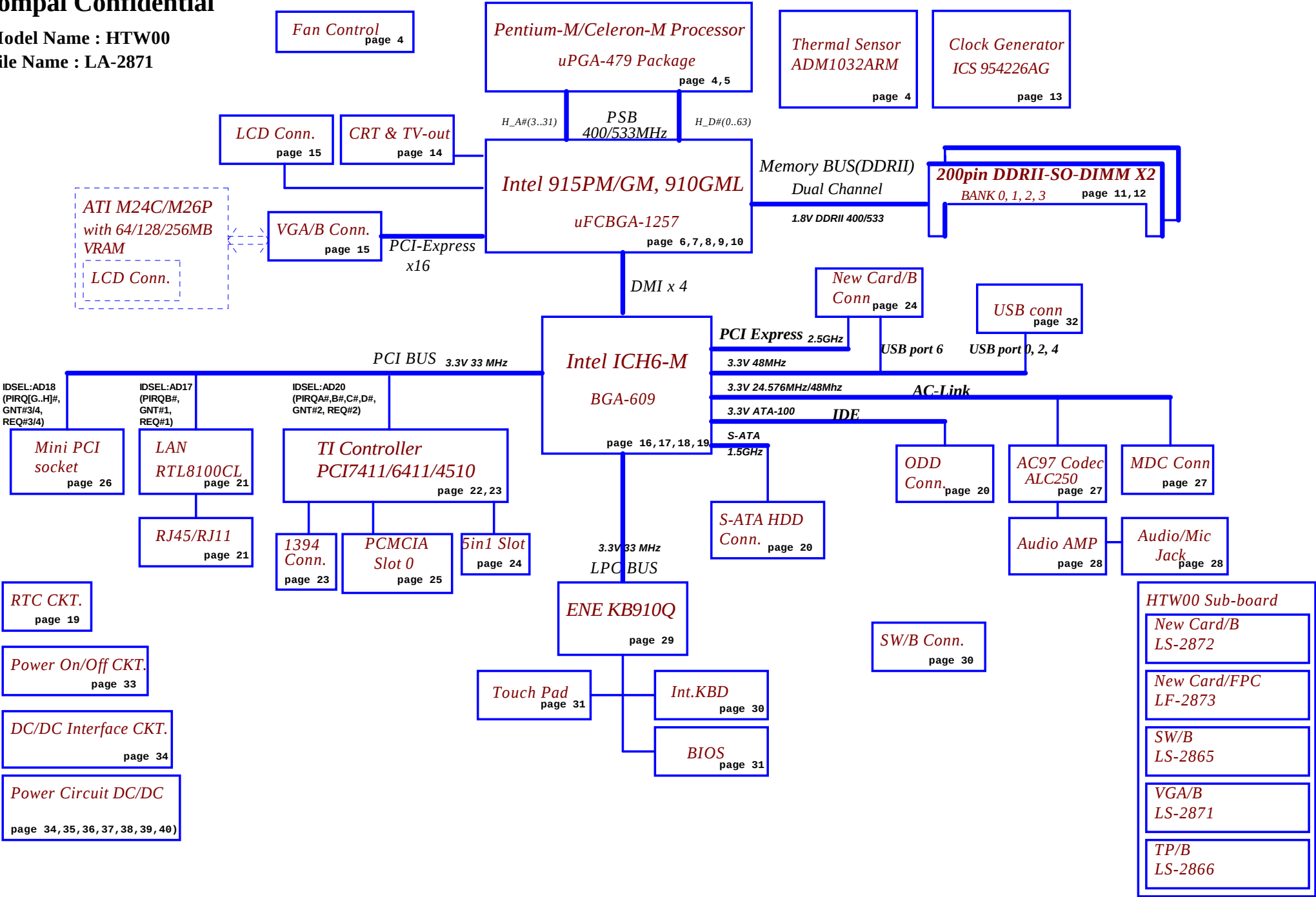
2005-08-22

REV: 1.0

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Model Name : HTW00
File Name : LA-2871



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
1394	D0	AD20	2	A,B,C,D
LAN	D1	AD17	3	F
CARD BUS	D4	AD20	2	A,B,C,D
5IN1	D4	AD20	2	A,B,C,D
Mini-PCI	D2	AD18	1	G,H

KB910 I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
SM1 24C16	A0H	1 0 1 0 0 0 0 X b
SM1 SMART BATTERY	16H	0 0 0 1 0 1 1 X b
SM2 ADM0132 CPU THERMAL MONITOR	98H	1 0 0 1 1 0 0 X b
SM2 GMT G781-1 VGA THERMAL MONITOR	9AH	1 0 0 1 1 0 1 X b

ICH6M SM Bus address

Device	Address
Clock Generator (ICS 954226)	1101 001Xb
DDRII DIMM0	1001 000Xb
DDRII DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

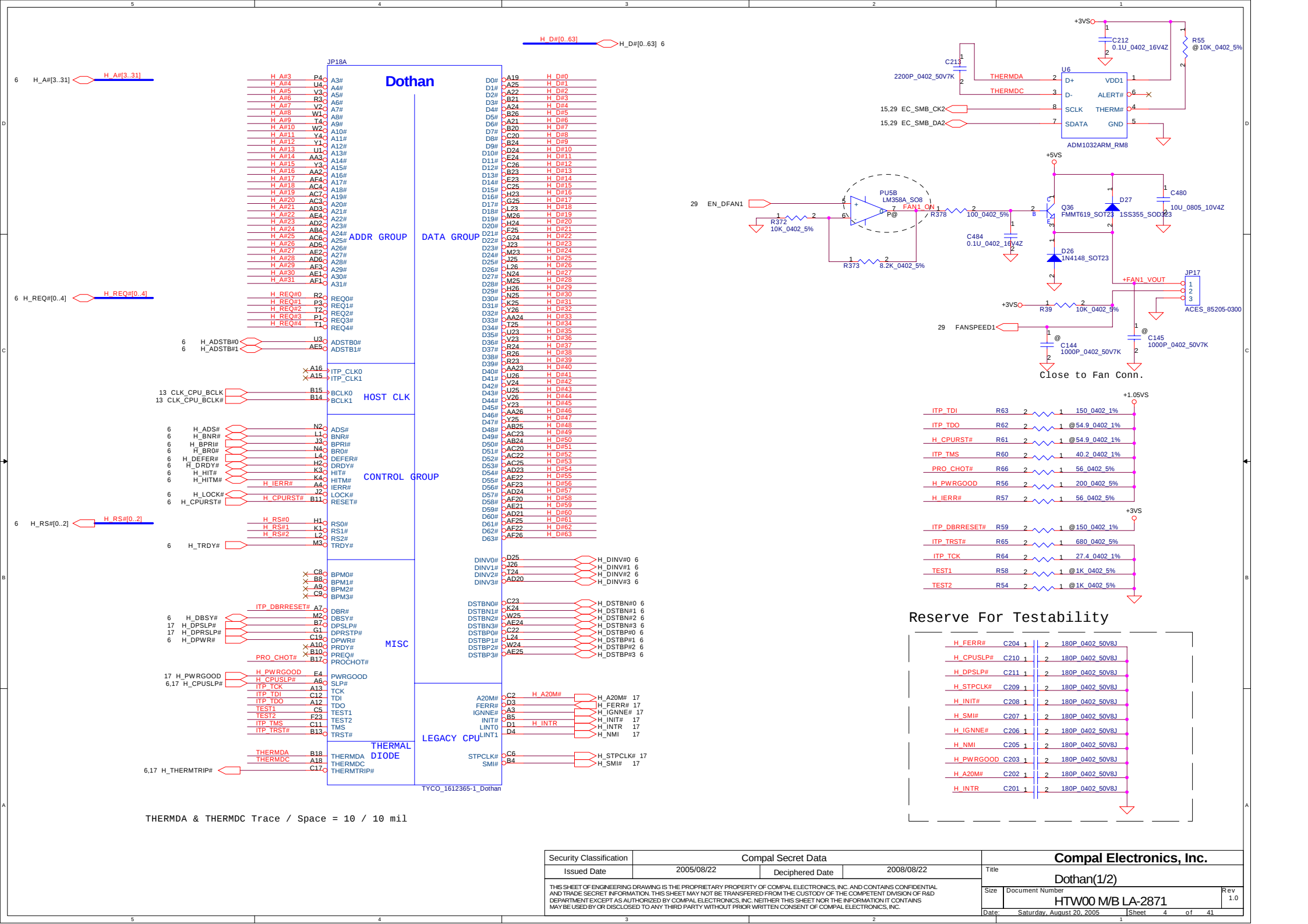
SKU ID Table

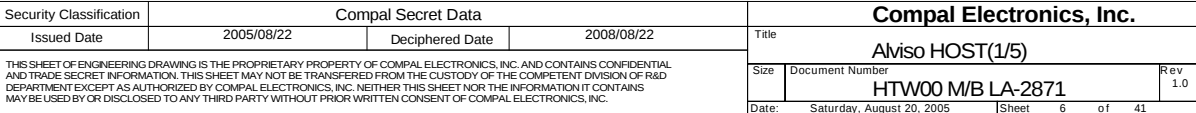
SKU ID	SKU
0	
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
VGA	6M@
Card Reader	5IN1@
Giga LAN	8100C@ 8110S@
New Card	NEWCARD@
IEEE1394	1394@
TV Tuner	TUNER@
INT MIC.	MIC@
KILL SW	WLAN@
CIR	CIR@
HWEQ	EQ@ NOEQ@

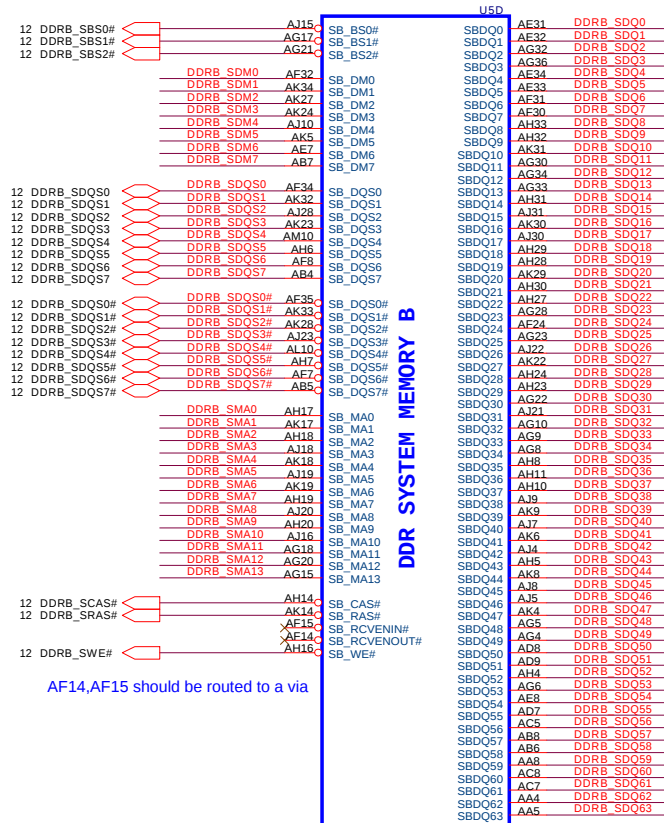
(TBD)

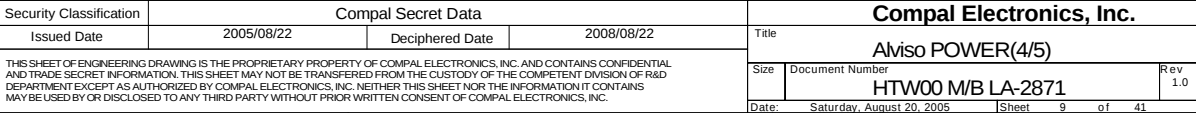


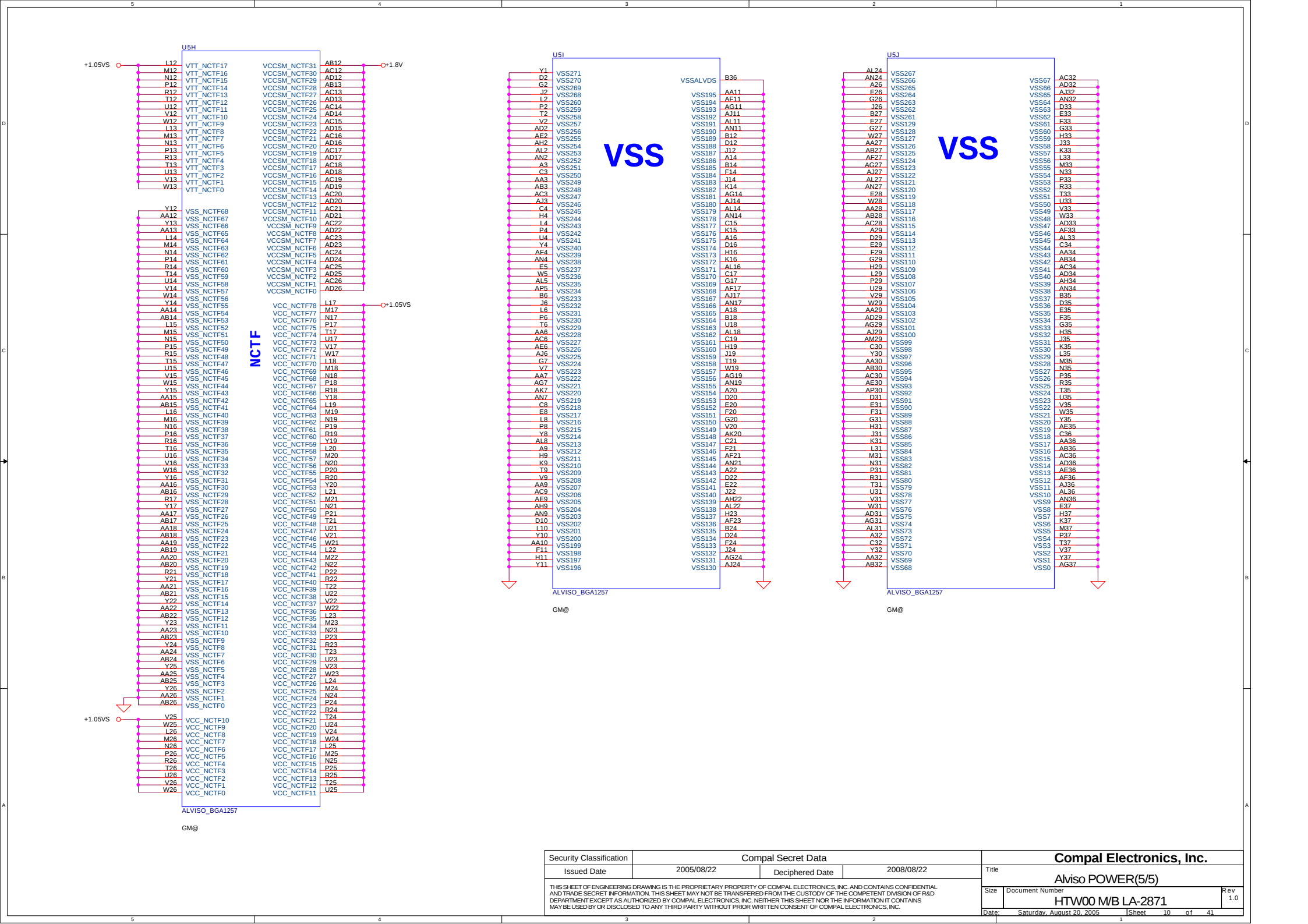


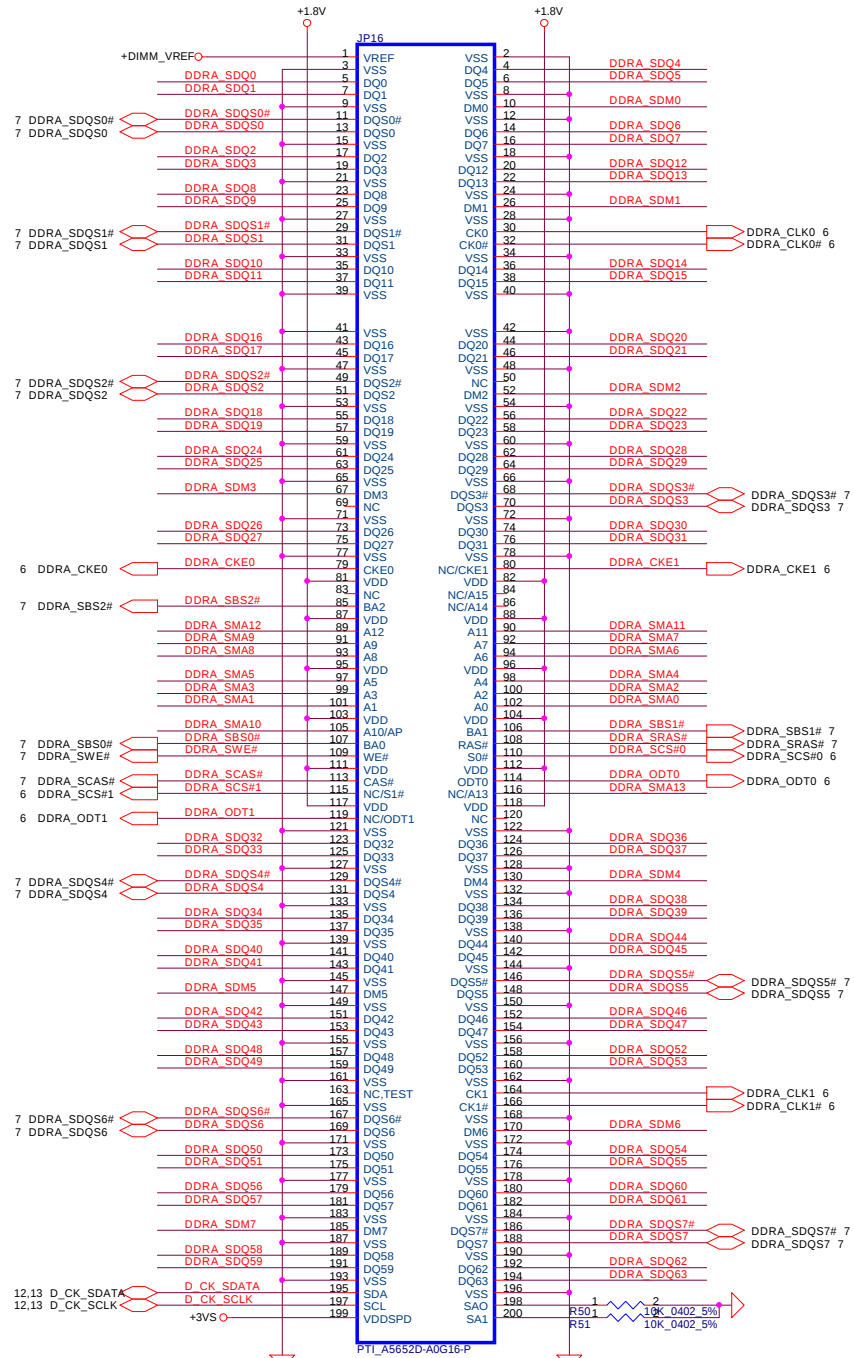
11 DDRA_SDQ[0..63]  DDRA_SDQ[0..63]
11 DDRA_SDM[0..7]  DDRA_SDM[0..7]
11 DDRA_SMA[0..13]  DDRA_SMA[0..13]

12 DDRB_SDQ[0..63]  DDRB_SDQ[0..63]
12 DDRB_SDM[0..7]  DDRB_SDM[0..7]
12 DDRB_SMA[0..13]  DDRB_SMA[0..13]

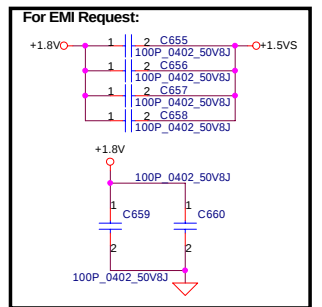
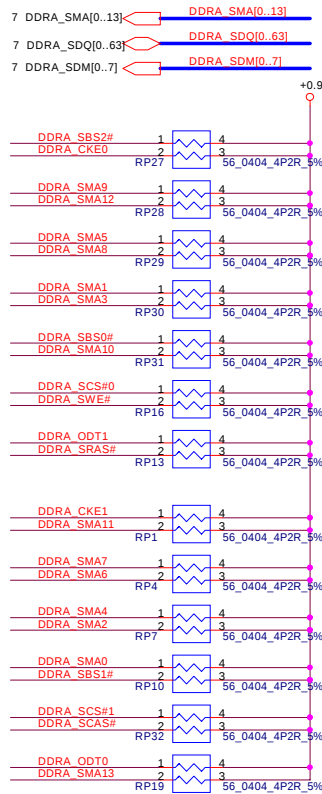
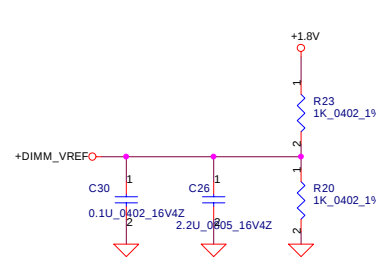




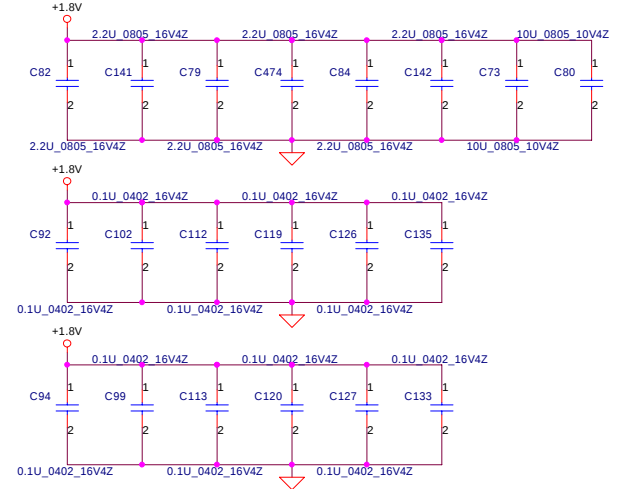




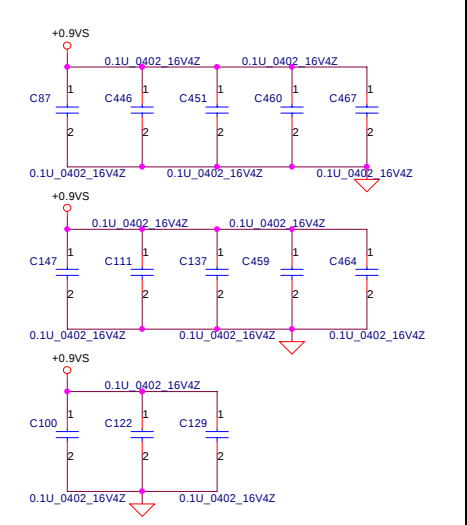
DIMM0 STD H:5.2mm (BOT)



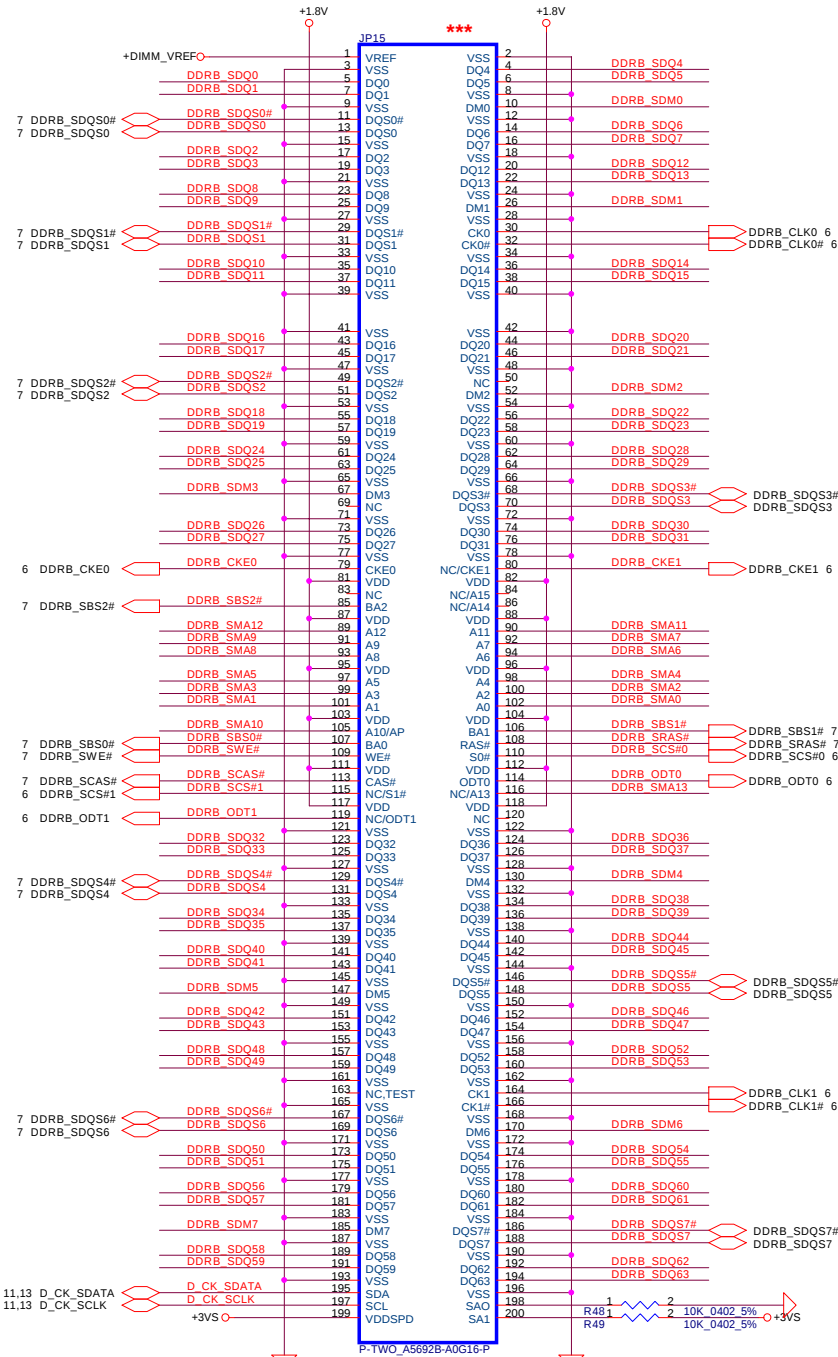
Layout note : Place one 0.1u cap close to every DDR-SODIMM pin
one 2.2u cap close to every 2.0 0.1u cap



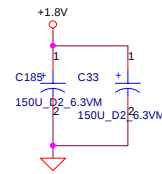
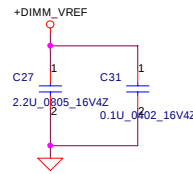
Layout note :
Place one cap close to every 2 pull up resistors termination to +0.9VS



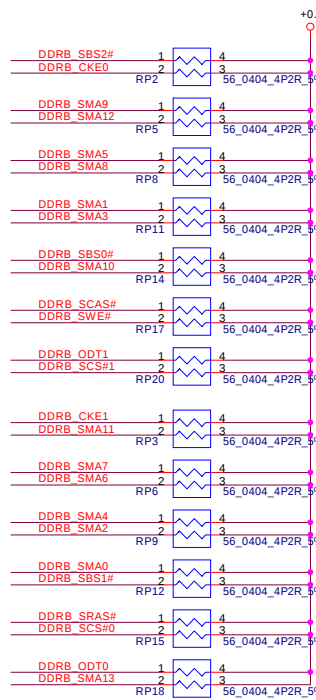
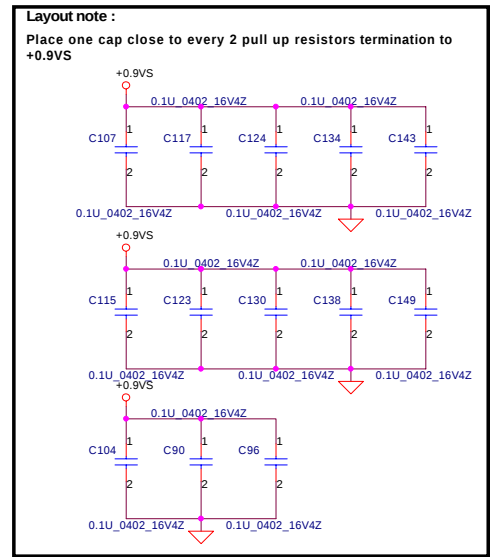
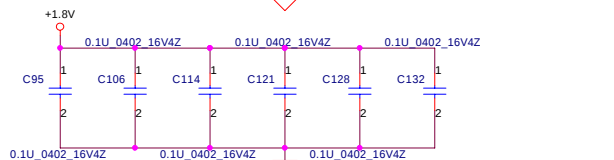
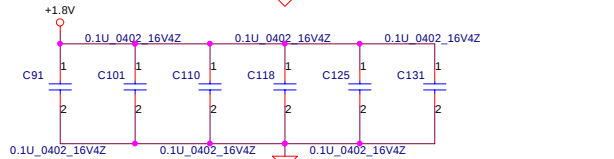
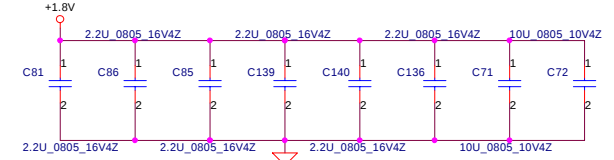
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Issued Date	2005/08/22	Deciphered Date	2008/08/22	Title	DDRII-SODIMM SLOT0
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DIMM1 STD H:9.2mm (BOT)

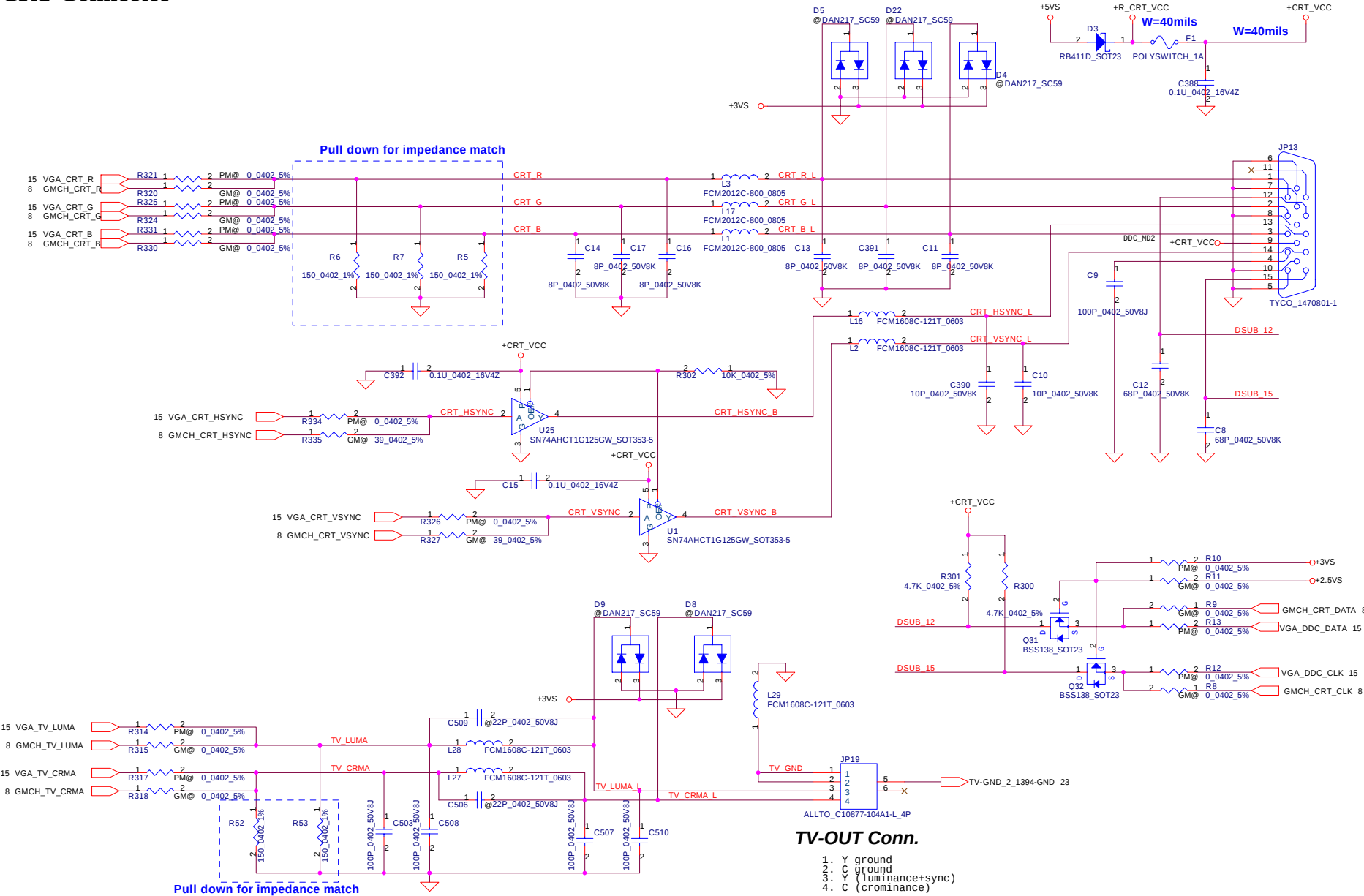


Layout note : Place one 0.1u cap close to every DDR-SODIMM pin
one 2.2u cap close to every 2 0.1u cap

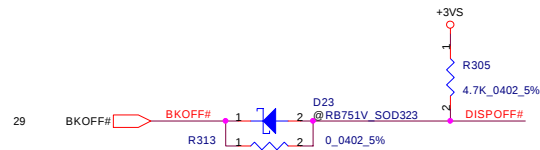
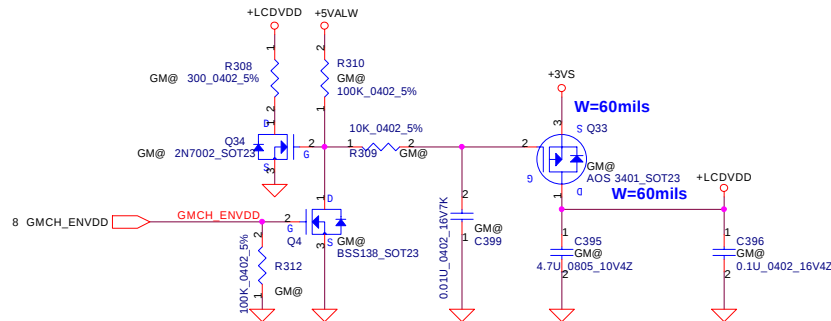


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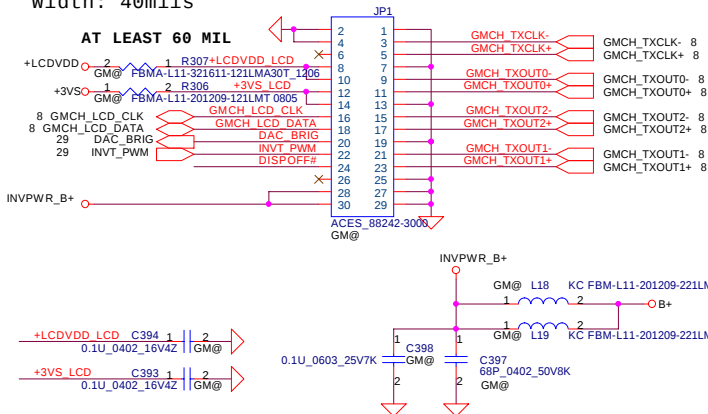
CRT Connector



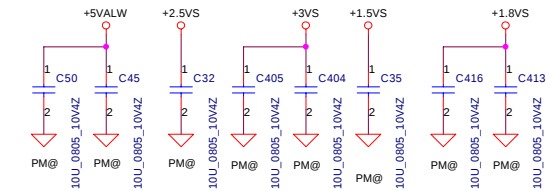
LCD POWER CIRCUIT



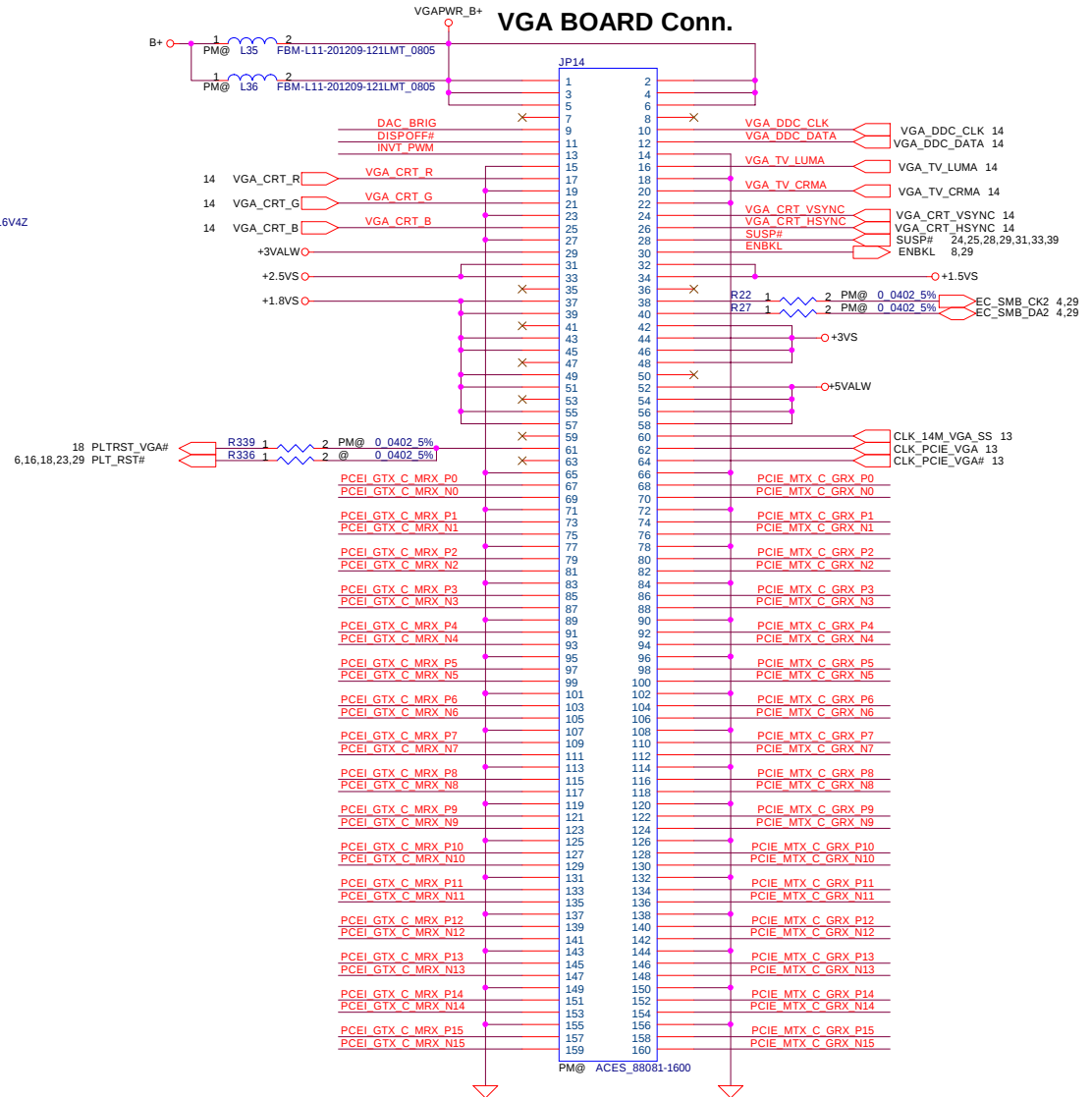
Width: 40mils



8 PCEI GTX_C_MRX_N[0..15] PCEI GTX_C_MRX N0..15
 8 PCEI GTX_C_MRX_P[0..15] PCEI GTX_C_MRX P0..15
 8 PCIE_MTX_C_GRX_N[0..15] PCIE MTX_C_GRX N0..15
 8 PCIE_MTX_C_GRX_P[0..15] PCIE MTX_C_GRX P0..15

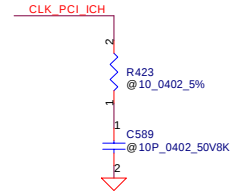
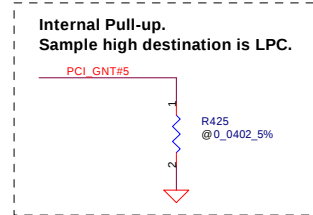
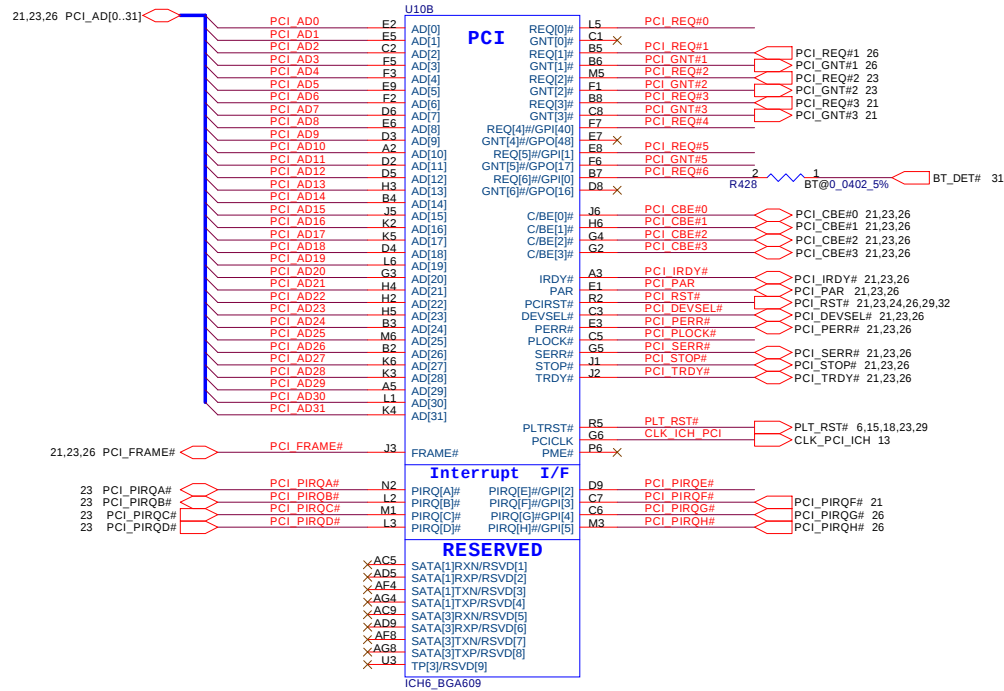
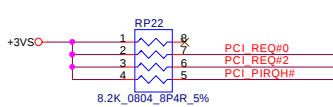
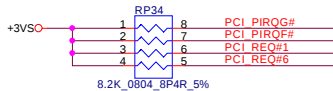
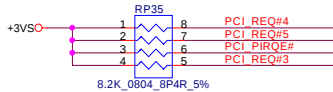
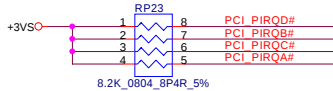
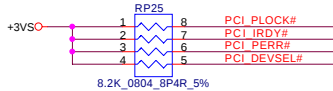
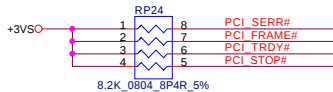


VGA BOARD Conn.

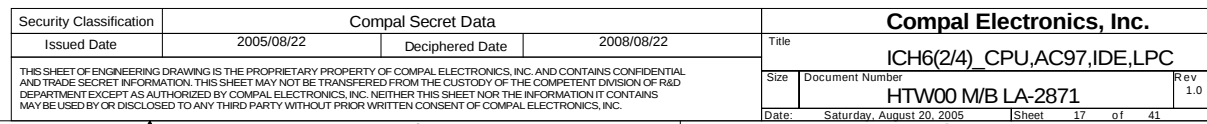


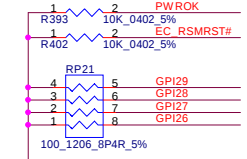
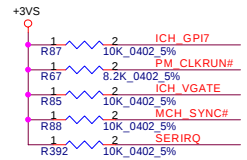
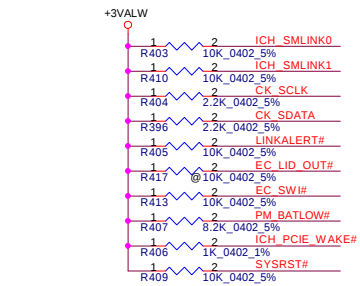
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2005/08/22		2008/08/22		Compal Electronics, Inc.	
2008/08/22		2008/08/22		VGA / LCD CONN.	
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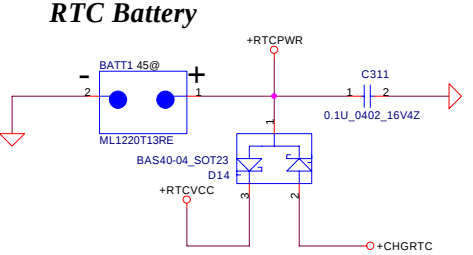
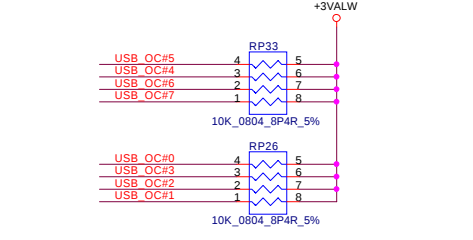
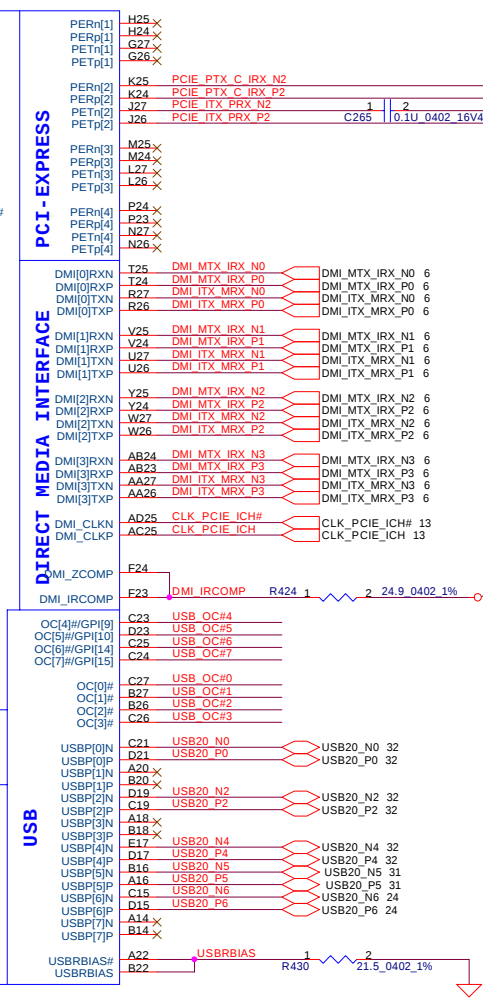
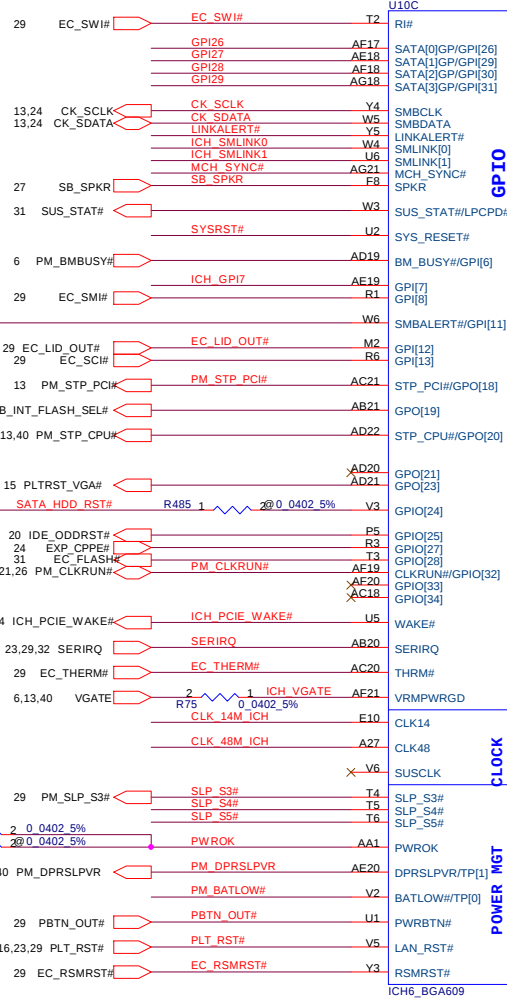
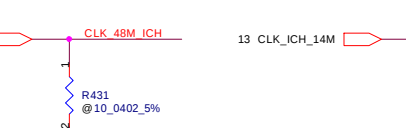
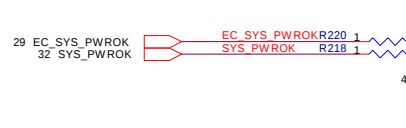
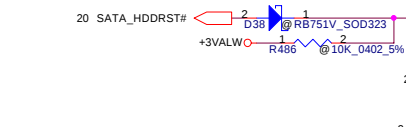
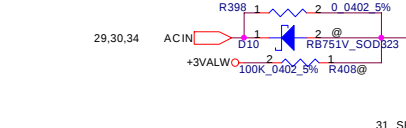


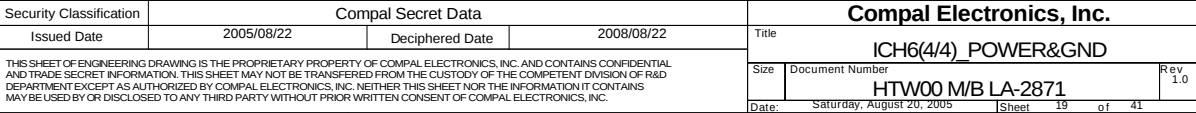
ICH6-M
(R3:SA828010890)
(R1:SA8280108B0)

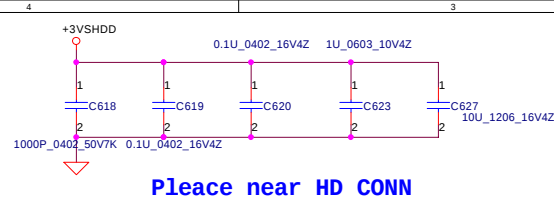




Intel new update







JP23

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22

GND A+ A- GND B- B+ GND

VCC3.3 VCC3.3 VCC3.3 GND GND VCC5 VCC5 GND RESERVED GND VCC12 VCC12 VCC12

SATA_ITS_C_DRX_P0 SATA_ITS_C_DRX_N0 SATA_DTX_IRX_N0 SATA_DTX_IRX_P0

+3VSHDD +5VSHDD

SUYIN_127043FB02G2082R 22P RV

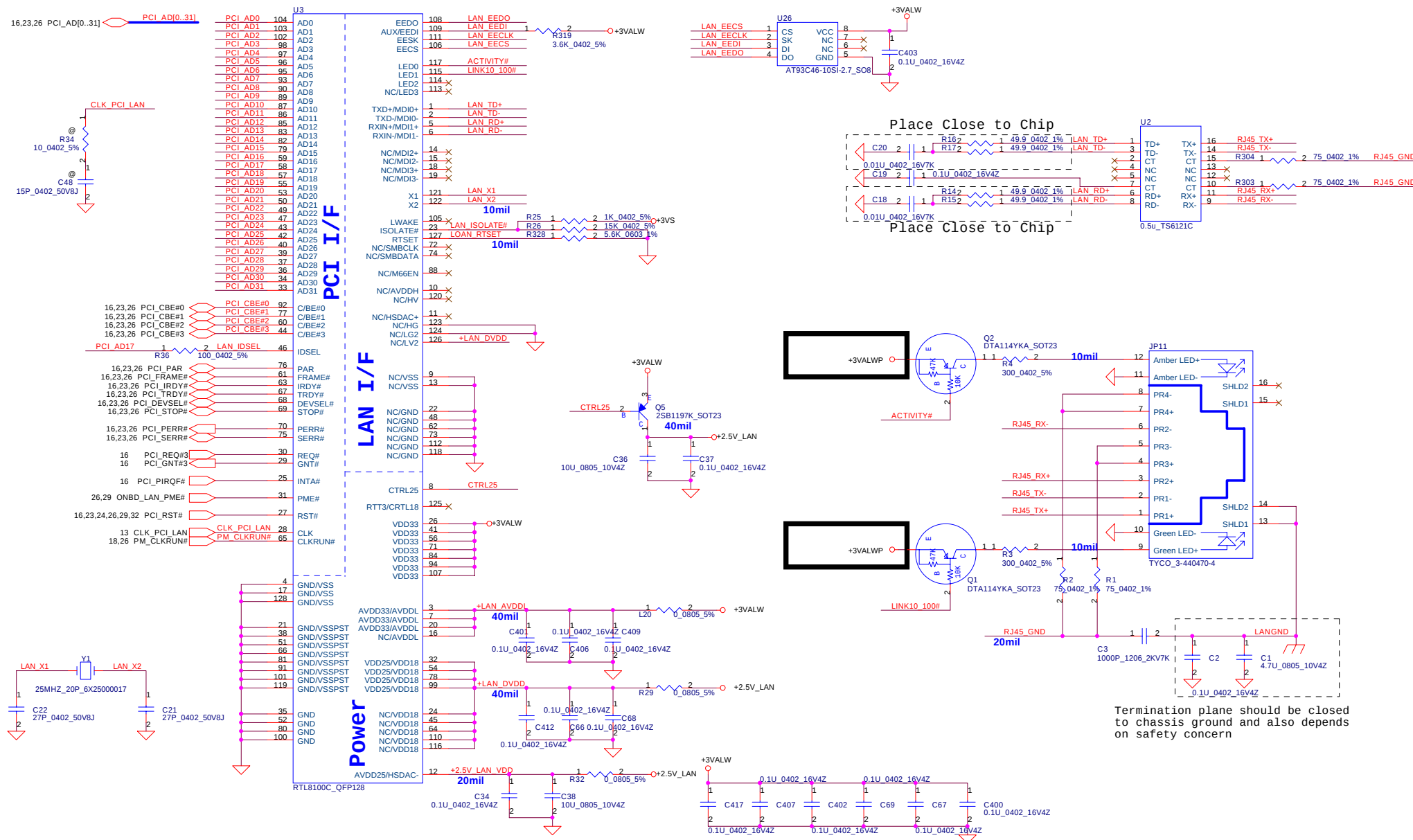
[illegible]

The schematic diagram illustrates the SATA_HDDRST# signal path, showing two identical driver stages. The top stage is driven by +5VSHDD and +5V, with a pull-up resistor R411 to +3VS. The bottom stage is driven by +3VSHDD and +3V. Both stages use MOSFETs Q44 and Q45 (top) and Q47 and Q48 (bottom), with current sources P115 and P116. The output of both stages is connected to the SATA_HDDRST# signal line.

The diagram shows a 5V regulator circuit. A +5VS input is connected to the input of a 7805 regulator. A 1000pF capacitor (C198) is connected between the input and ground. A 0.1uF capacitor (C199) is connected between the input and ground. The output of the 7805 regulator is connected to the input of a 7805 regulator. A 10uF capacitor (C200) is connected between the output and ground. The output of the 7805 regulator is connected to the input of a 7805 regulator. A 10uF capacitor (C200) is connected between the output and ground. The output of the 7805 regulator is connected to the input of a 7805 regulator. A 10uF capacitor (C200) is connected between the output and ground.

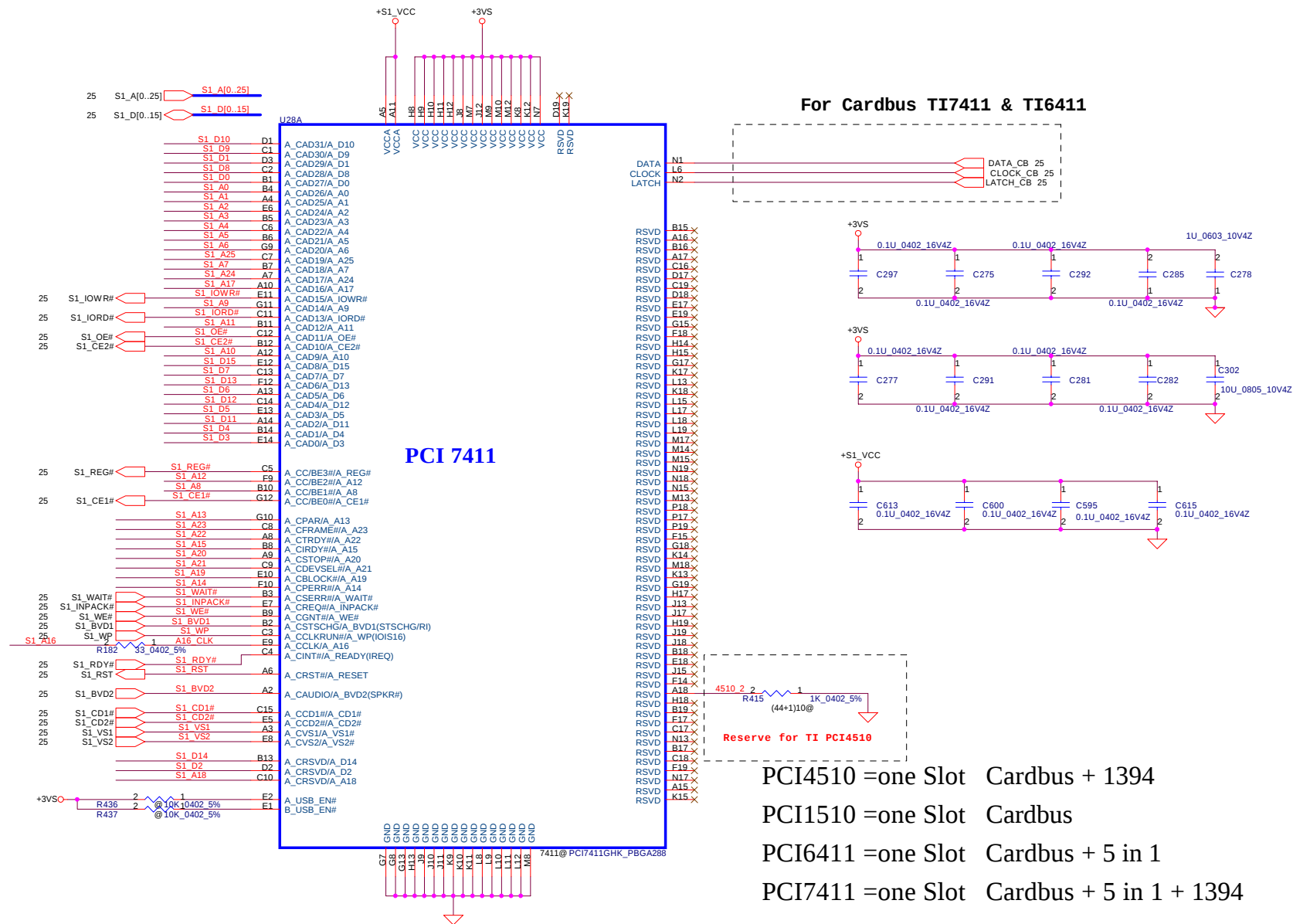
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2005/08/22	Deciphered Date	2008/08/22	Title	SATA/PATA-HDD, PATA ODD Connector	
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LAN RTL8100C(L)



Termination plane should be closed to chassis ground and also depends on safety concern

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Issued Date	2005/08/22	Deciphered Date	2008/08/22	Title
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Size	Document Number	HTW00 M/B LA-2871		Rev 1.0
Date:	Saturday, August 20, 2005	Sheet	21	of 41



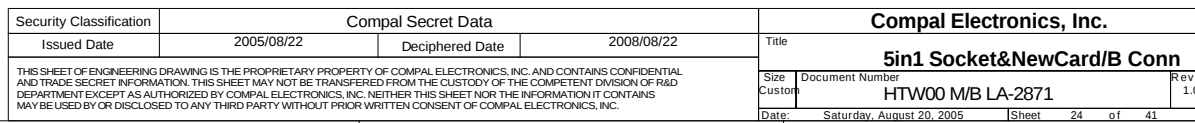
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/08/22	Deciphered Date	2008/08/22	Title	PCI7411-1 Slot0
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Date:	Saturday, August 20, 2005	Sheet	22	of	41



1

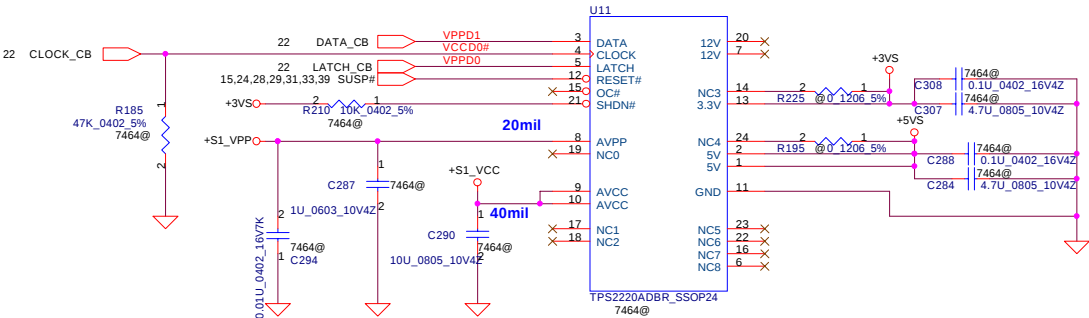


40mil $I_{max} = 0.75A$

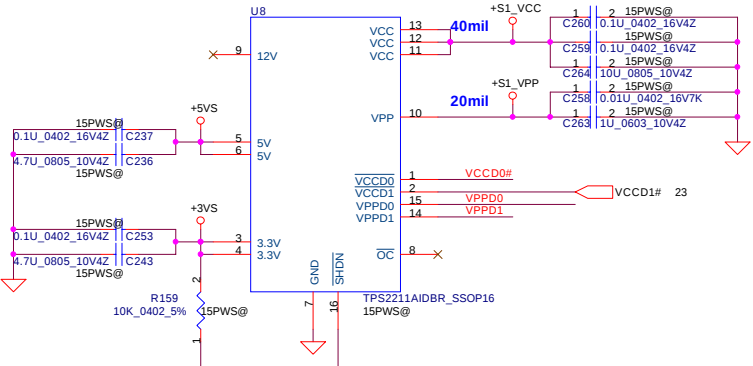


Power Switch for PCMCIA

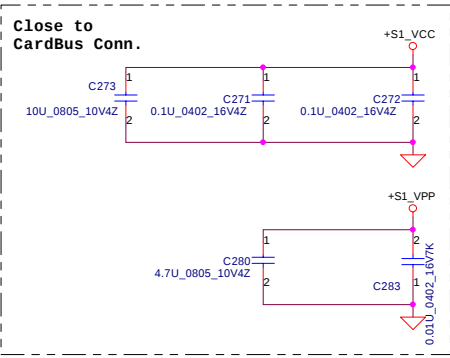
Power Switch for PCMCIA (PCI7411 & PCI6411 only)

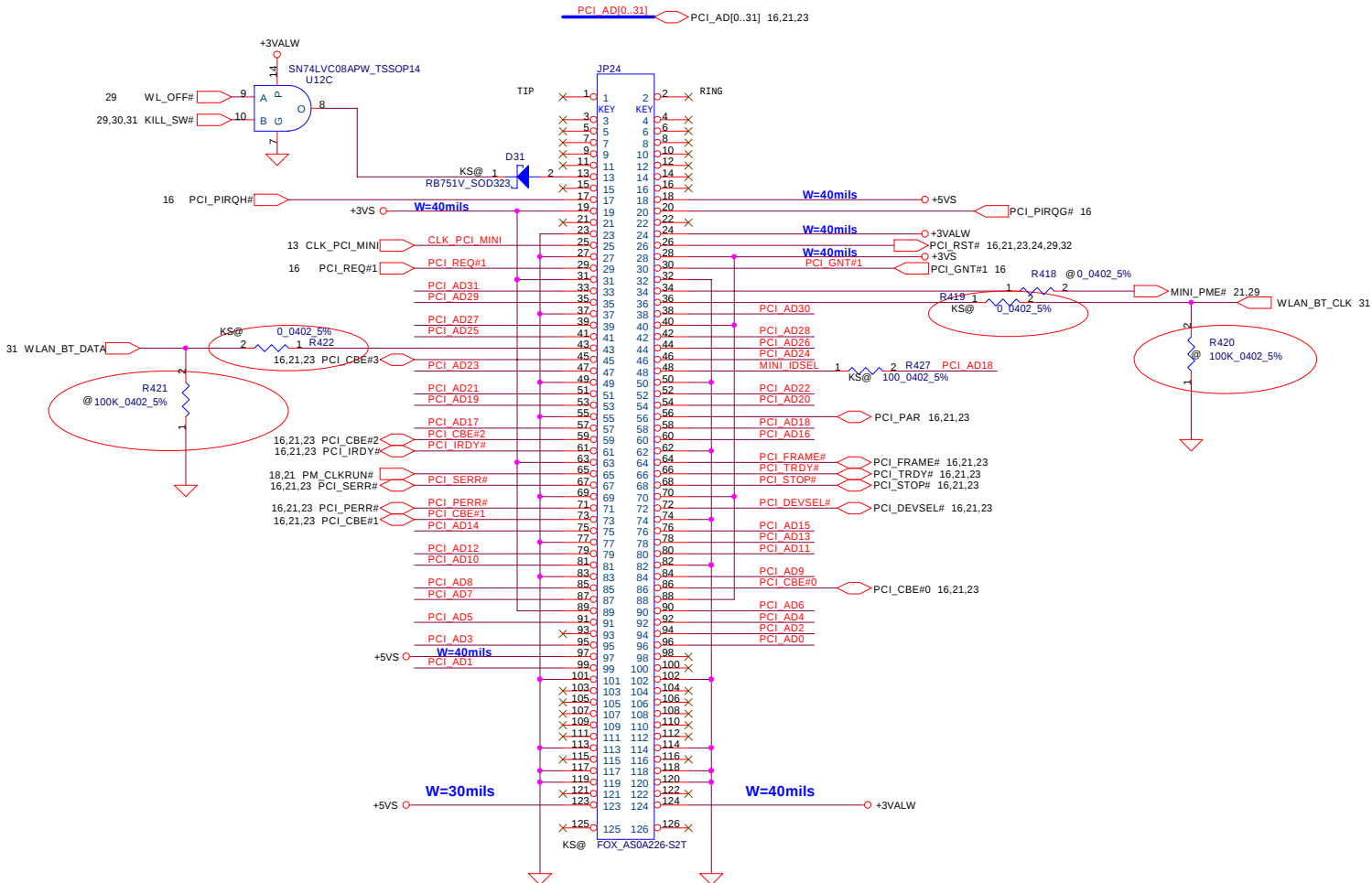
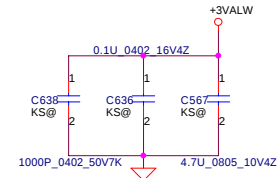
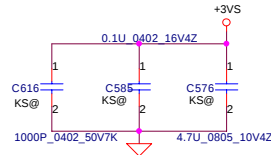
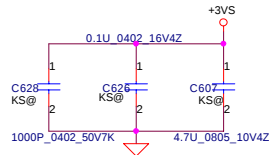
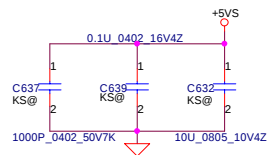


Power Switch for PCMCIA (PCI1510 & PCI4510 only)

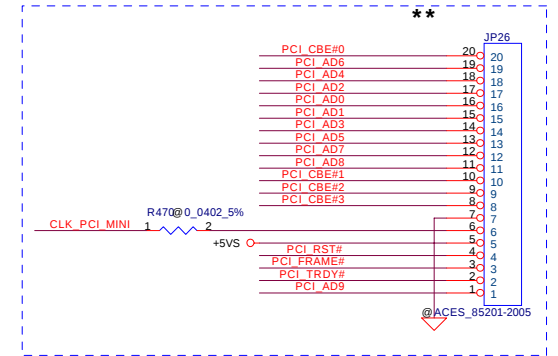


CardBus Socket





Port 80 Debug Card Connector

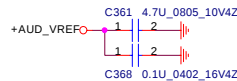


Place under MiniPCI Socket

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		41			

SPK_ID: HIGH: Harman/Kardom
Low: No Brand

Legend:
 29 - SPK_SEL
 28 - NBA_PLUG



29 BEEP#

23 PCM_SPK#

18 SB_SPKR

C363 1U_0402_6.3V4Z

C366 1U_0402_6.3V4Z

C362 1U_0402_6.3V4Z

R285 560_0402_5%

R287 560_0402_5%

R283 560_0402_5%

R278 10K_0402_5%

R286 2.2K_0402_5%

C356 10U_0805_10V4Z

C357 1U_0402_6.3V4Z

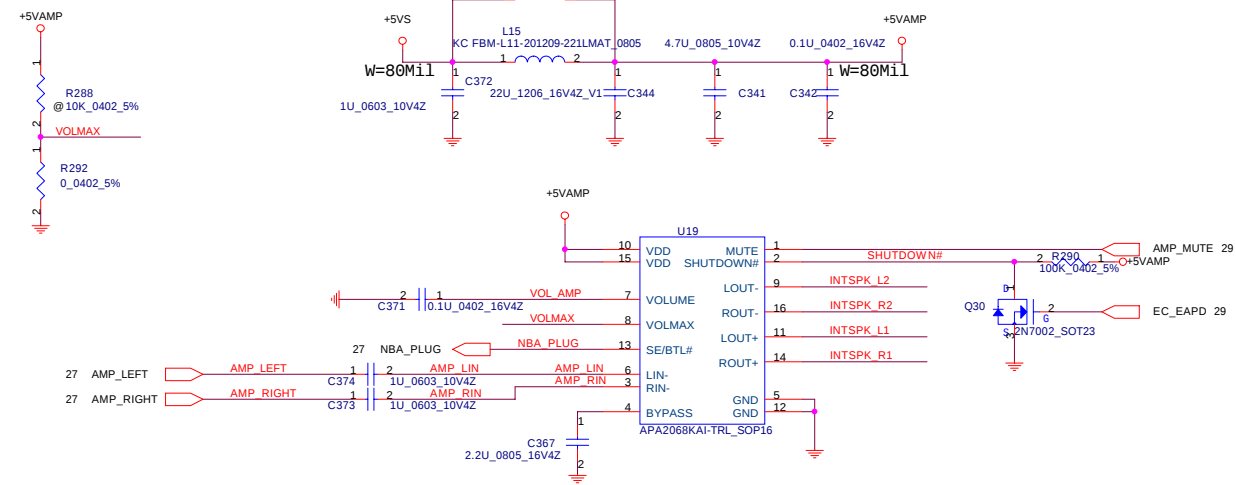
Q29 2SC2411K_SCS9

D20 RB751V_SOD323

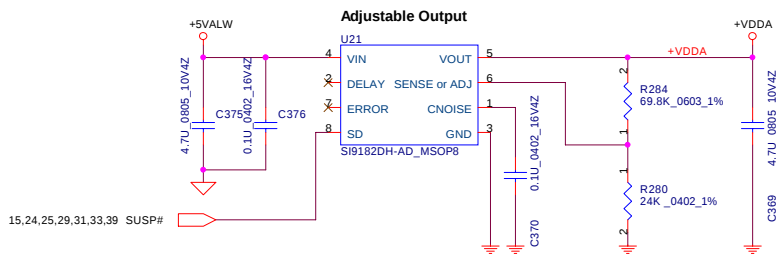
Connector for MDC Rev1.5

Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2005/08/22	Deciphered Date	2008/08/22	Title		AC97 Codec ALC250&MDC	
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				HTW00 M/B LA-2871			
Date:				Saturday, August 20, 2005	Sheet	27	of 41

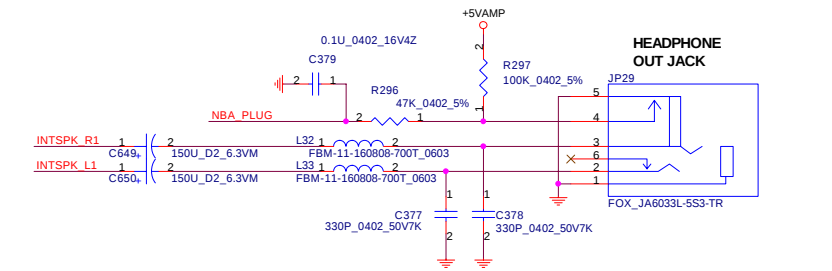
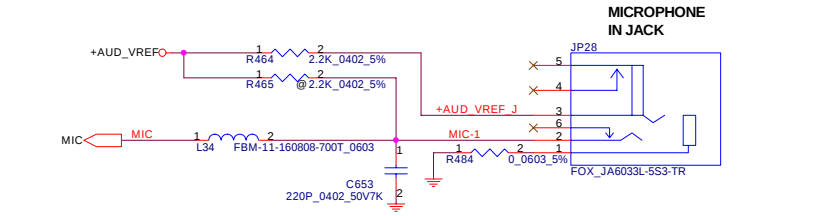
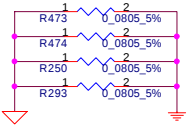
Audio AMP



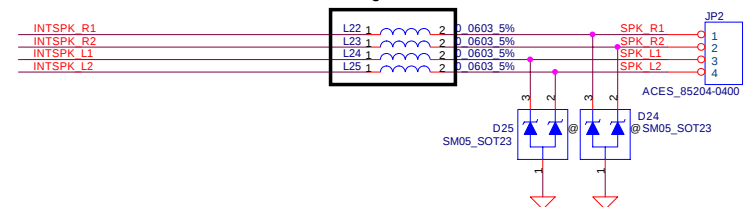
Regulator for CODEC



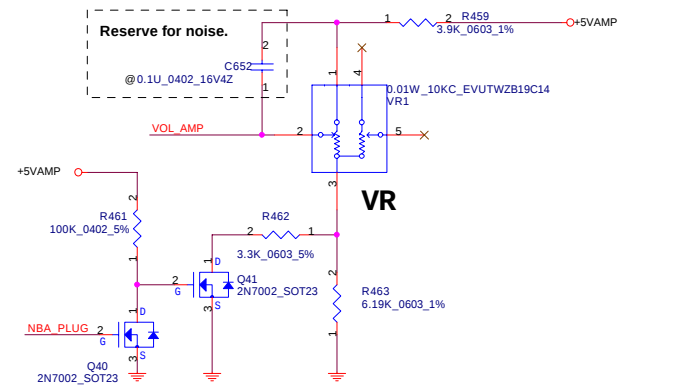
Moat Bridge



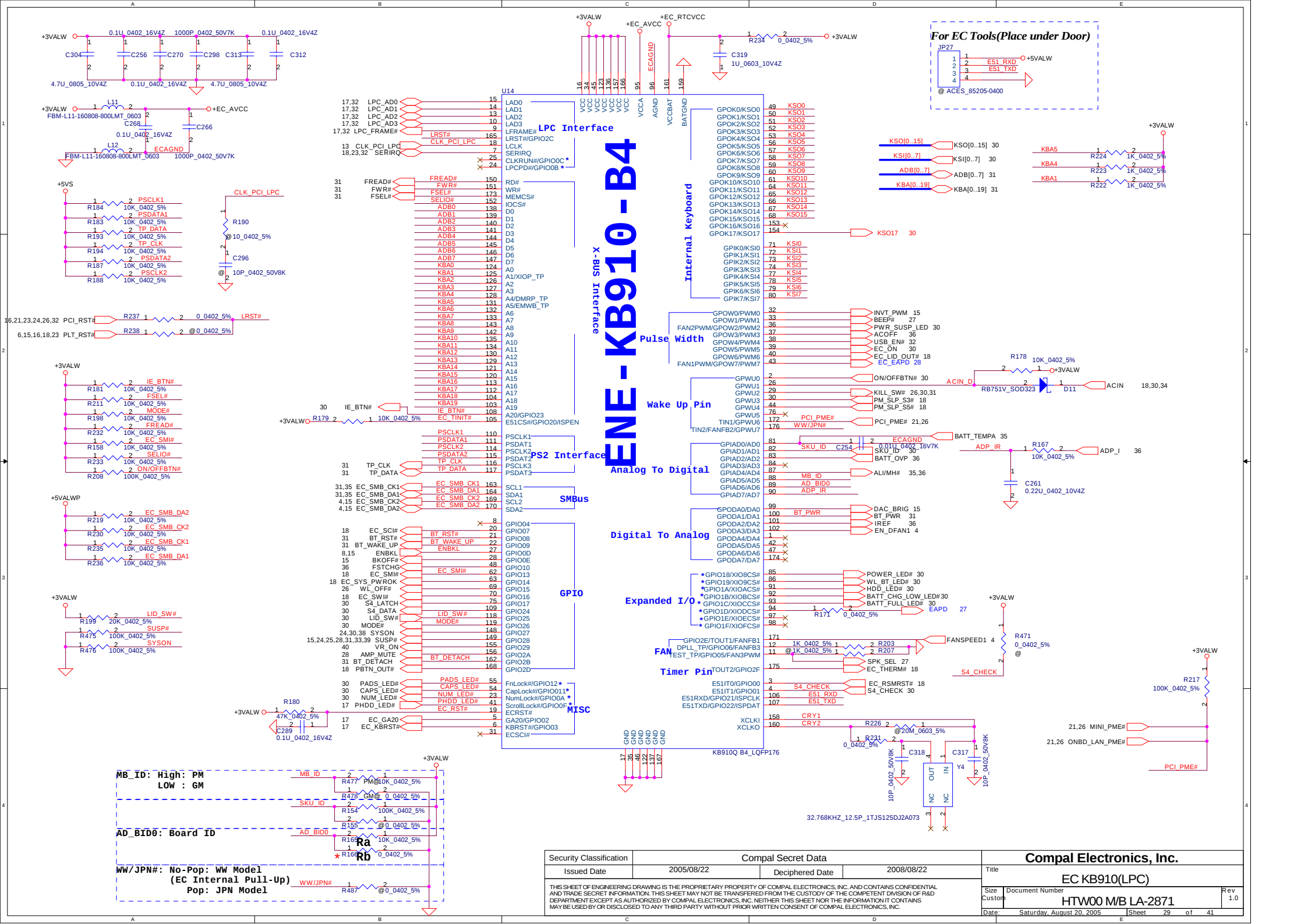
Speaker Connector



Variable Resistor



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[illegible]

+3VALW ○ 1 R467 KS@ 2 300 0402 5% 2 D37 HT-191UD AMBER 0603 1 KS@ WL_BT_LED# 29

The diagram shows two digital signals over time. The top signal, **PWR_SUSPLED1#**, is a purple line with a blue triangle at the start of a pulse labeled **D39**. The bottom signal, **PWR_LED 0#**, is a red line with a blue triangle at the start of a pulse labeled **D40**. Both signals have a '2' on the left and a '1' on the right of the pulse, indicating a 2-to-1 transition. The pulses are labeled **HT-191UD_AMBER_0603** and **HT-191NB_BLUE_0603** respectively.

The schematic diagram shows the internal circuit of the HT-191N8_BLUE_0603 LED driver. It starts with a +5VALW input connected to a resistor R272. The signal then passes through a diode D15 (HT-191N8_BLUE_0603) and a MOSFET Q22 (2N7002_SOT23) to the ACIN input. The circuit is labeled with various component values and identifiers, including 1, 2, 200_0402_5%, and 2N7002_SOT23.

Diagram of the ACES_85201-1205 pinout for JP3:

Pin	Signal	Component	Value
1	PWR_LED_1#		
2	PWR_SUSPLED#		
3	SKU_ID	SKU_ID	29
4	KSO17	KSO17	29
5	ON/OFF		
6	IETB#		
7	MODSTB#		
8	EC_PLAYB#IN		
9	KSIO	KSIO	29
10	EC_STOPB#IN		
11	KSII	KSII	29
12	EC_FRDB#IN		
13	KSII	KSII	29
14	EC_REVB#IN		
15	KSI2	KSI2	29
16	KSI3	KSI3	29

ACES_85201-1205

For EMI Request

The schematic diagram illustrates the RTC module circuit. Key components and connections include:

- RTCVREF:** Connected to the RTC module and the SYSON signal.
- SYSON:** A signal line connecting the RTC module to the SYSON pin.
- S4_LATCH:** A signal line connecting the RTC module to the S4_LATCH pin.
- S4_DATA:** A signal line connecting the RTC module to the S4_DATA pin.
- S4_CHECK:** A signal line connecting the RTC module to the S4_CHECK pin.
- ON/OFF:** A signal line connecting the RTC module to the ON/OFF pin.
- Resistors:** R458, R457, R454, R456, R453, R455, R452.
- Capacitors:** C645, C648, C644, C641, C640, C642.
- Diodes:** D35, D32, D33.
- Integrated Circuits:** U20, U29, U28.

[illegible]

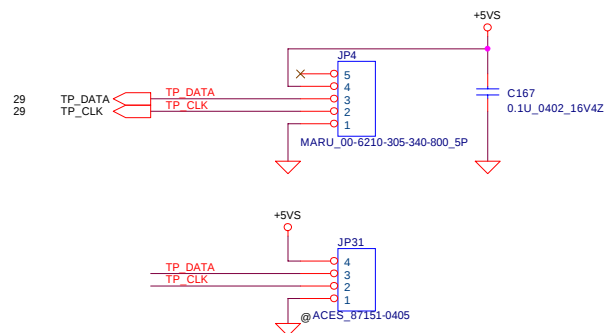
	2	1	PADS_LED#		NUM_LED#	1	2
100P_0402_50V8J	2	1	C514		C513	1	100P_0402_50V8J
100P_0402_50V8J	2	1	KS014		CAPS_LED#	1	
100P_0402_50V8J	2	1	C529		C528	1	100P_0402_50V8J
100P_0402_50V8J	2	1	KS011		KS015	1	
100P_0402_50V8J	2	1	C530		C517	1	100P_0402_50V8J
100P_0402_50V8J	2	1	KS09		KS010	1	
100P_0402_50V8J	2	1	C531		C515	1	100P_0402_50V8J
100P_0402_50V8J	2	1	KS17		KS08	1	
100P_0402_50V8J	2	1	C532		C516	1	100P_0402_50V8J
100P_0402_50V8J	2	1	KS07		KS013	1	
100P_0402_50V8J	2	1	C533		C518	1	100P_0402_50V8J
100P_0402_50V8J	2	1	KS14		KS03	1	100P_0402_50V8J
100P_0402_50V8J	2	1	C534		C519	1	100P_0402_50V8J
100P_0402_50V8J	2	1	KS15		KS012	1	
100P_0402_50V8J	2	1	C542		C520	1	100P_0402_50V8J
100P_0402_50V8J	2	1	KS05		KS16	1	
100P_0402_50V8J	2	1	C537		C541	1	100P_0402_50V8J
100P_0402_50V8J	2	1	KS10		KS06	1	
100P_0402_50V8J	2	1	C538		C546	1	100P_0402_50V8J
100P_0402_50V8J	2	1	KS01		KS13	1	
100P_0402_50V8J	2	1	C539		C547	1	100P_0402_50V8J
100P_0402_50V8J	2	1	KS12		KS00	1	100P_0402_50V8J
100P_0402_50V8J	2	1	C540		C548	1	100P_0402_50V8J
100P_0402_50V8J	2	1	KS04		KS11	1	
100P_0402_50V8J	2	1	C541		C543	1	100P_0402_50V8J
					KS02	1	
					C544	1	100P_0402_50V8J

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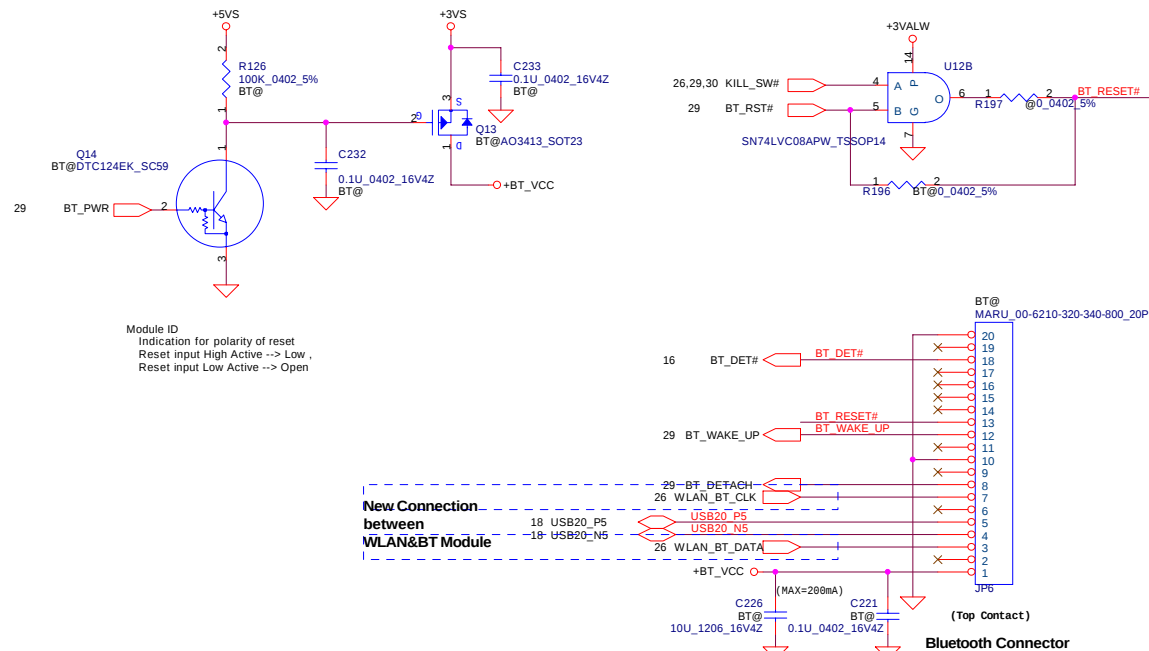
S4R/LID/KS/KB/LED/SW-B Conn

Size	Document Number	Rev
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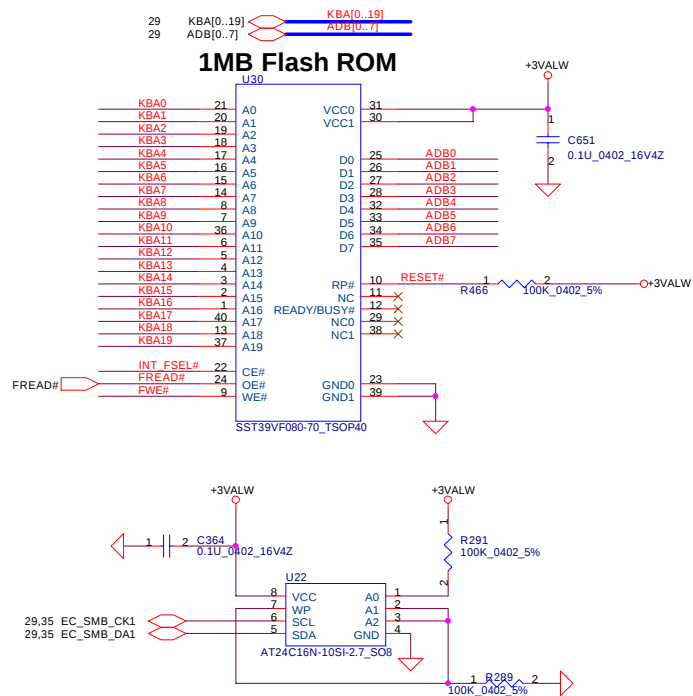
TP CONN.



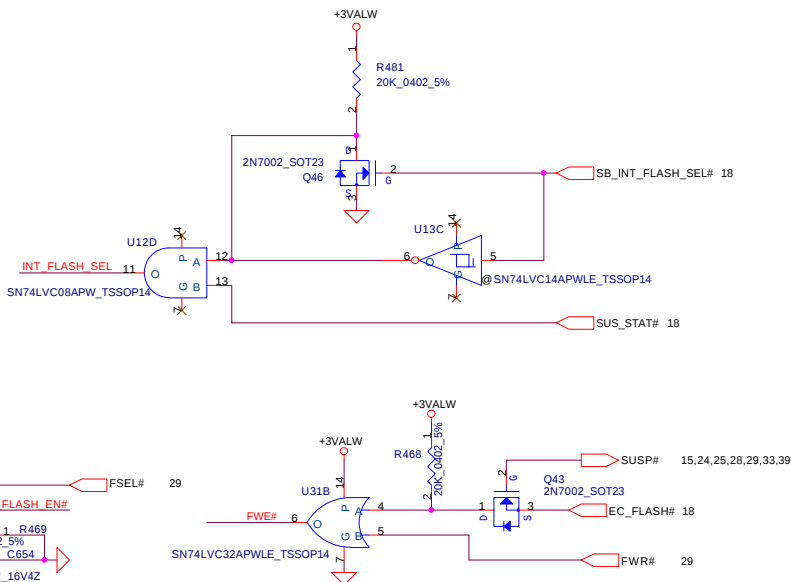
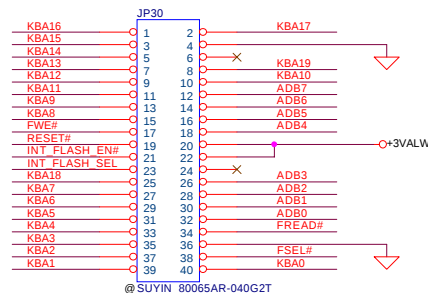
BlueTooth Interface



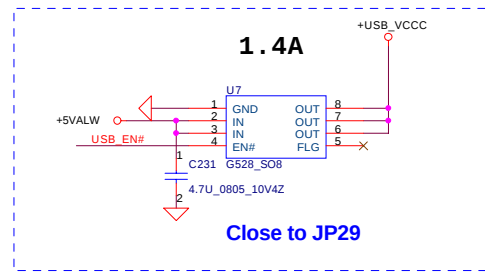
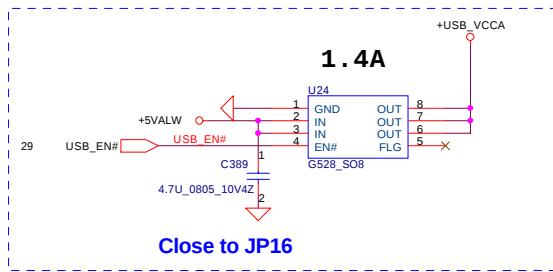
1MB Flash ROM



1MB ROM Socket



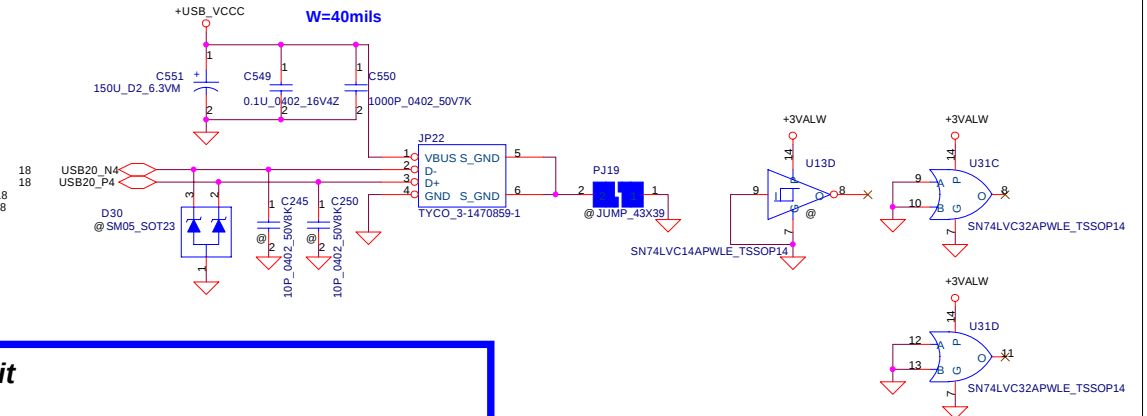
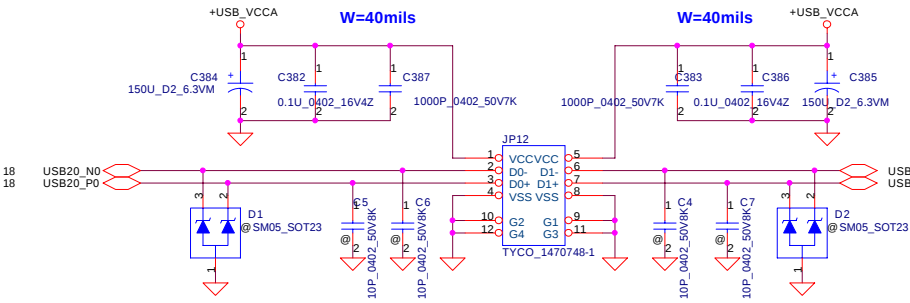
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2005/08/22	Deciphered Date	2008/08/22	Title	1MB BIOS/ TP Conn/ BT Conn	
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				HTW00 M/B LA-2871		1.
				Date:	Monday, August 22, 2005	Sheet 31 of 41



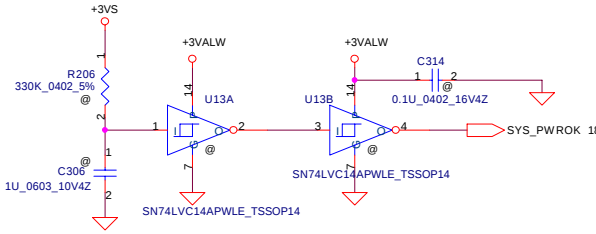
USB CONN. 1

USB CONN. 2

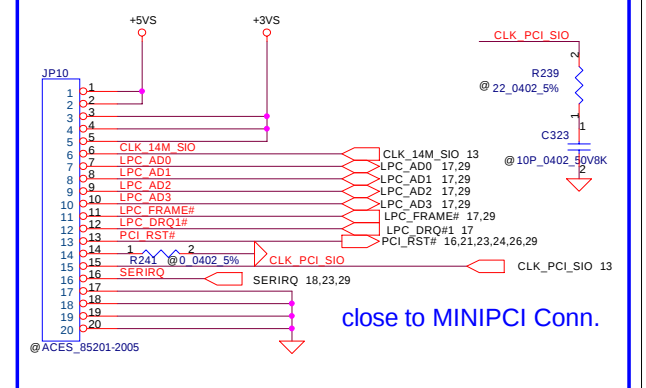
USB CONN. 3



Power OK Circuit



LPC Debug Port



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1



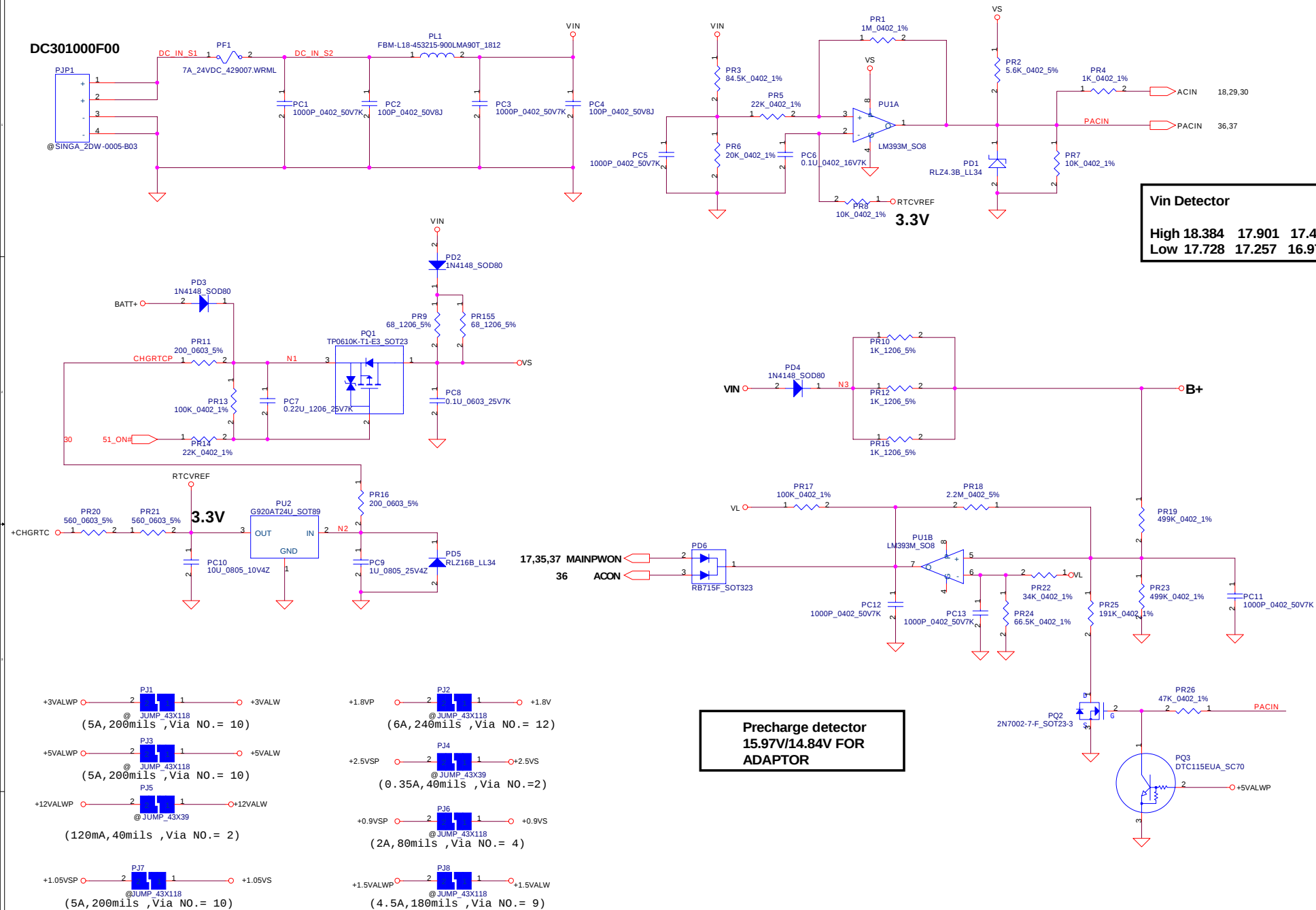
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4

4

DC301000F00



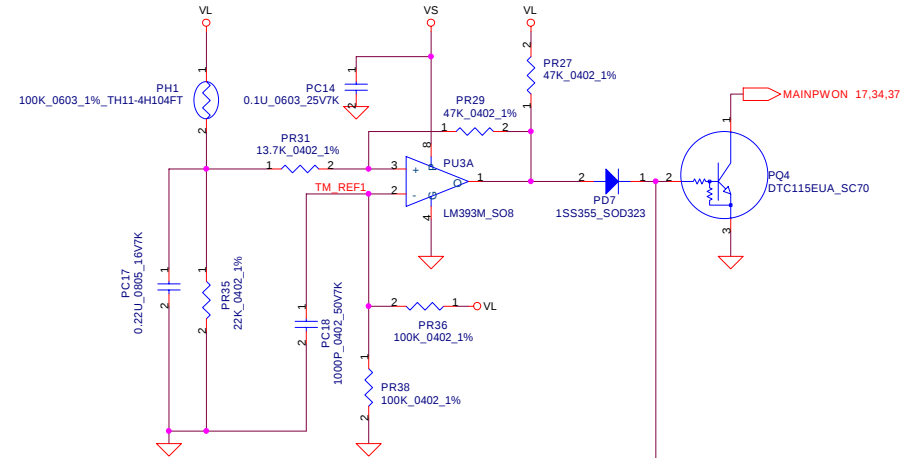
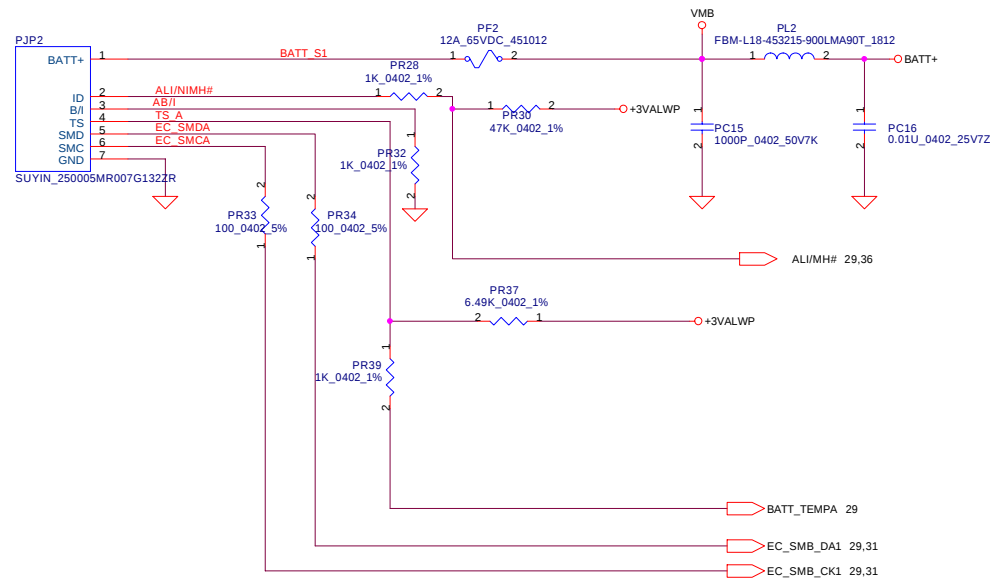
Vin Detector

High 18.384 17.901 17.430
Low 17.728 17.257 16.976

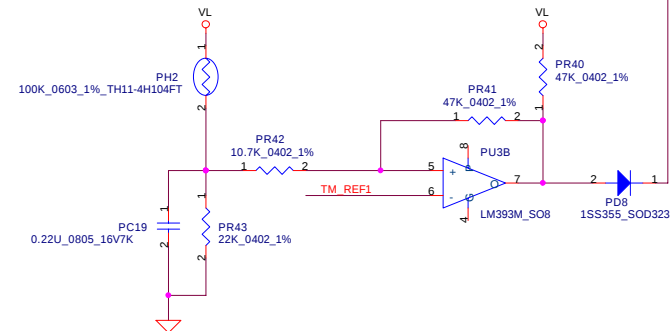
Precharge detector 15.97V/14.84V FOR ADAPTOR

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Date: Saturday, August 20, 2005					Sheet 34 of 41

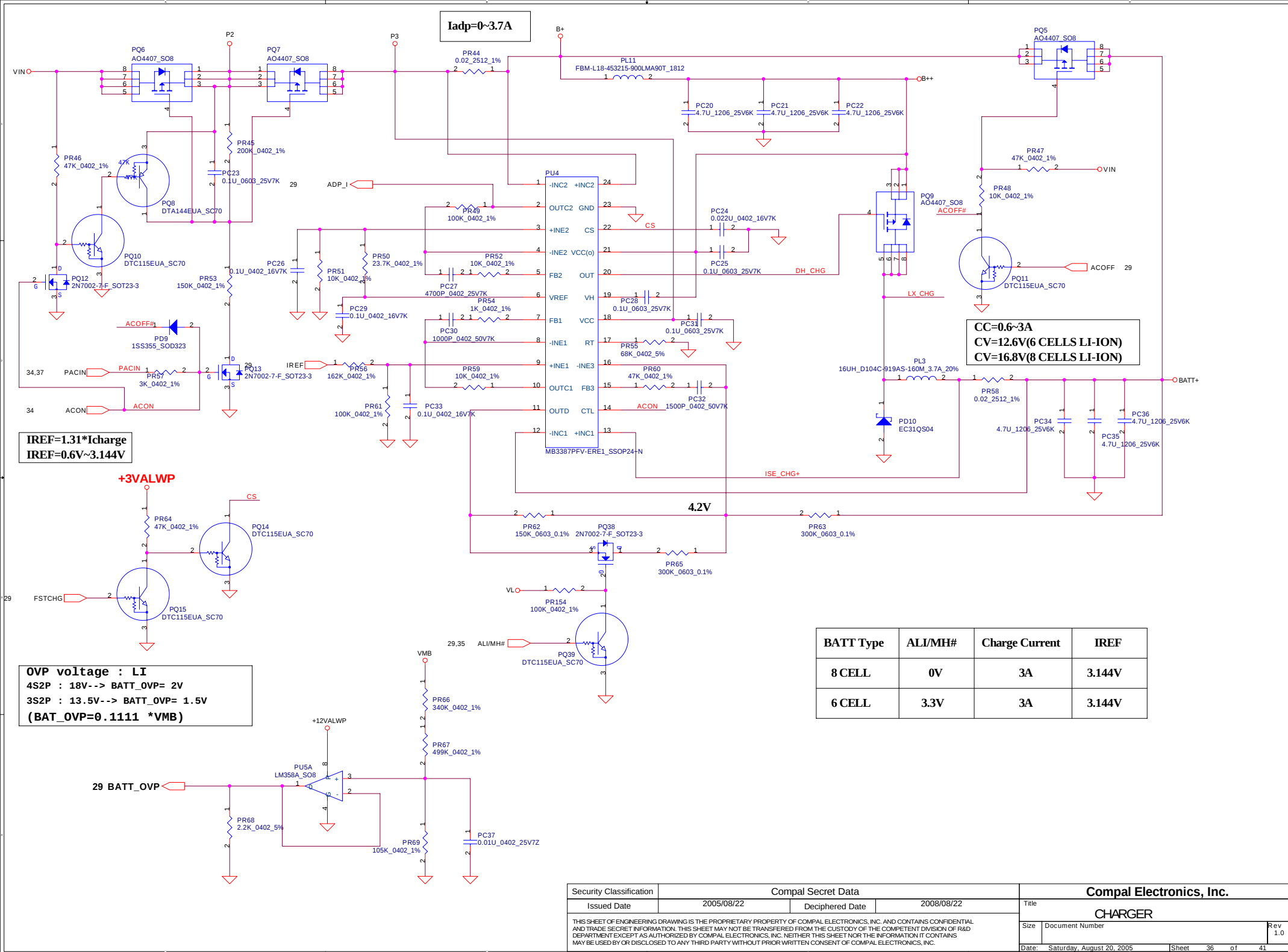
PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C

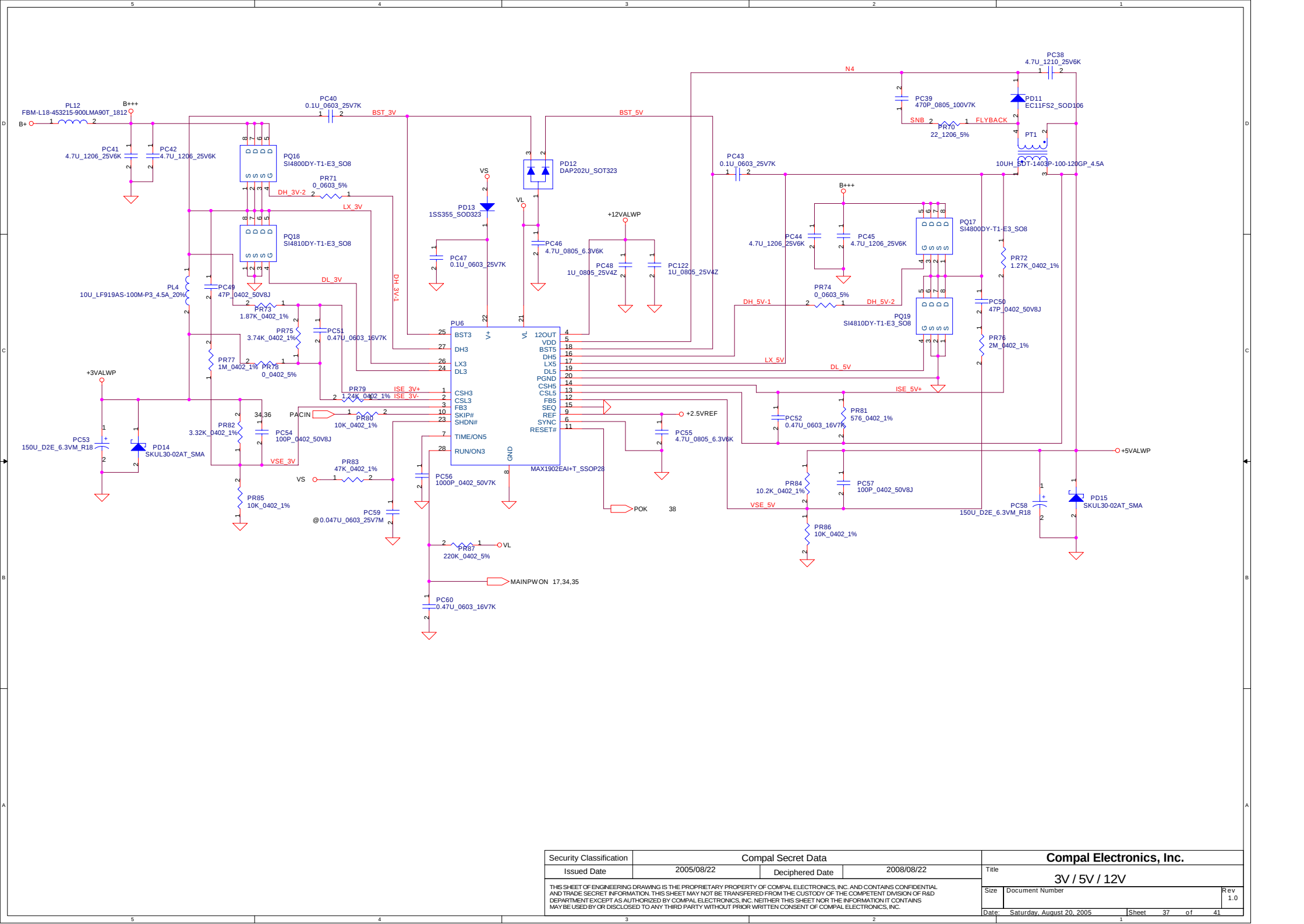


PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C

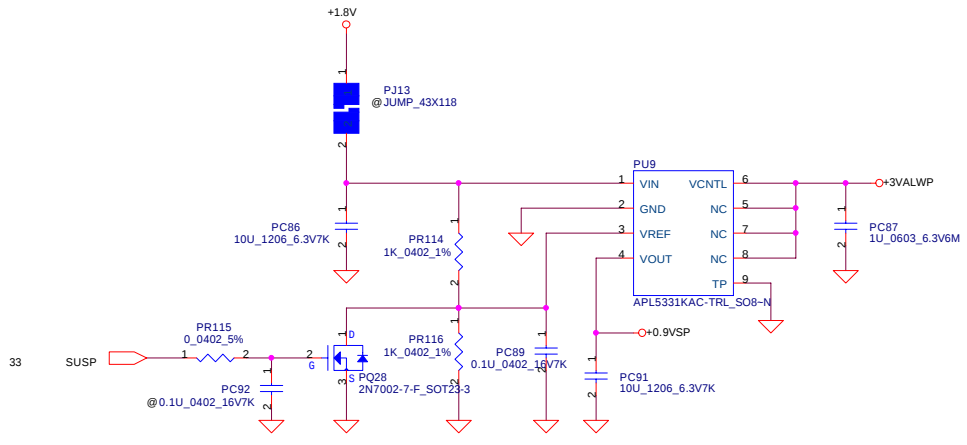
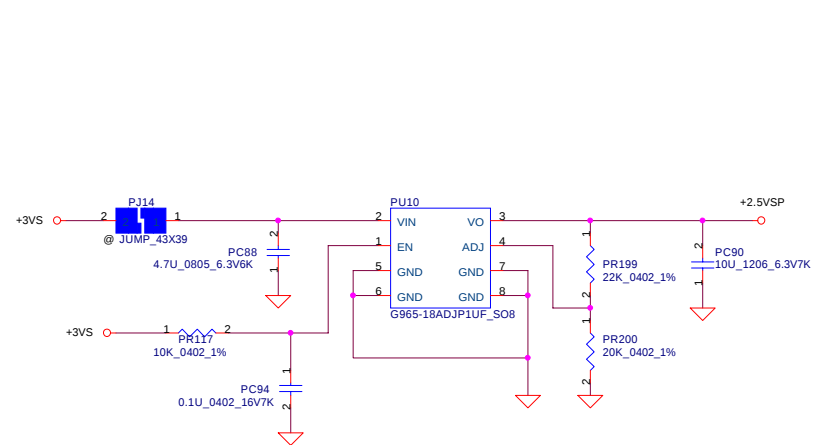
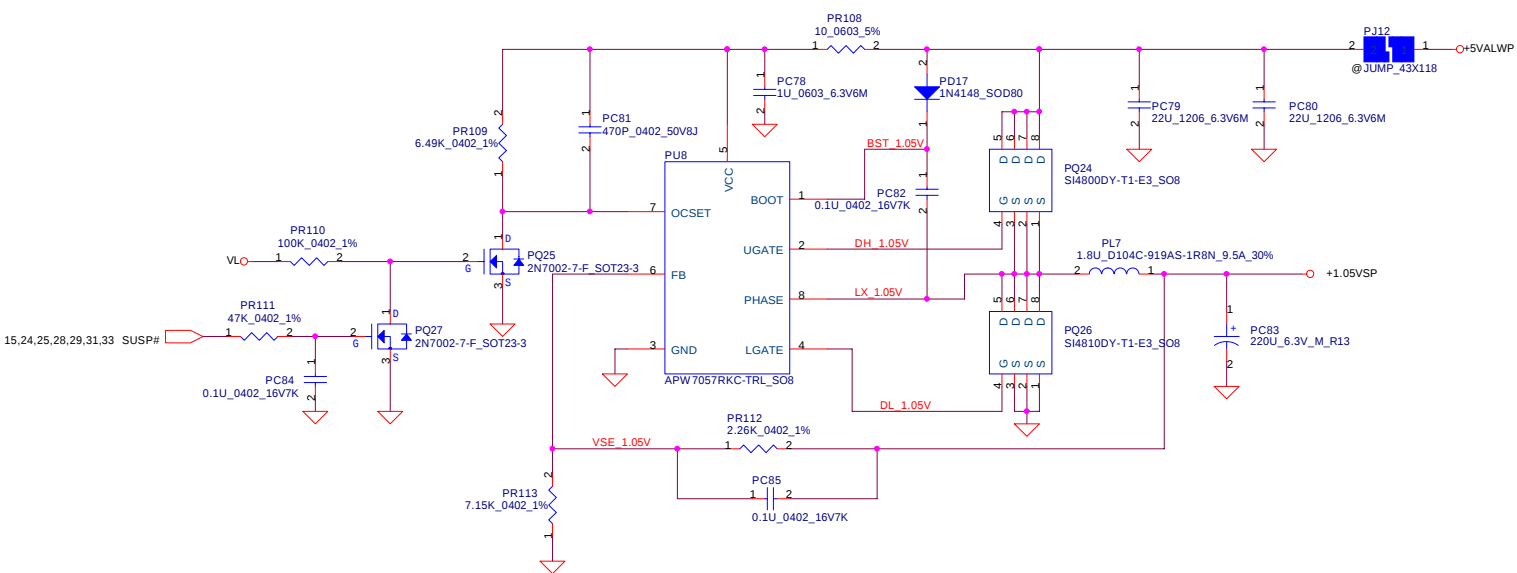


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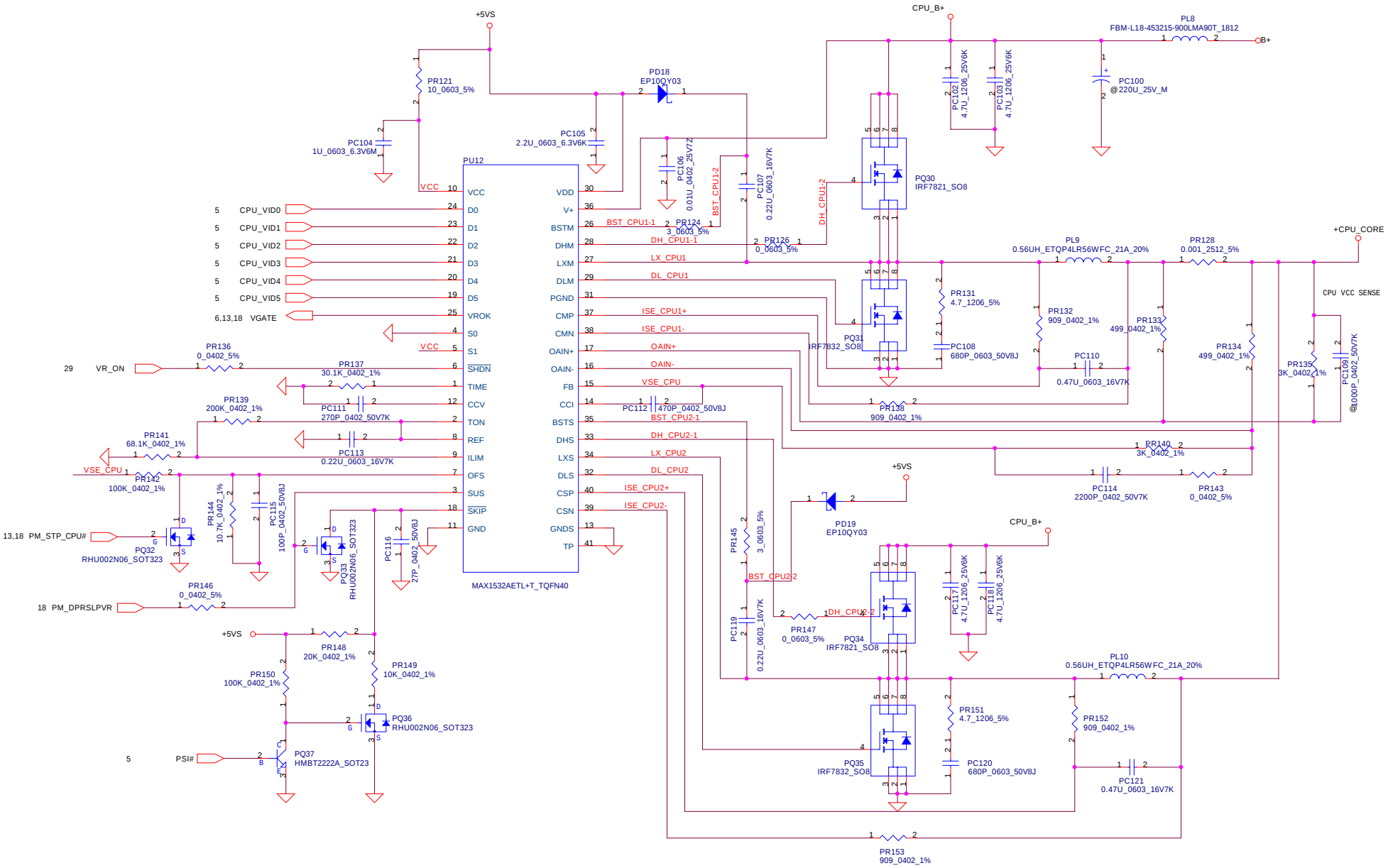




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							1.0
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POWER PIR LIST

	page	Reason for change	Modify list
DVT	36,37,38,40	For EMI request to reduce the power board band	Add bead PL11,PL12,PL13(SM010020720), add snubber 4.7ohm(SD001470B80)PR131,PR151 and 680P(SE024681J80)PC108,PC120 on CPU CORE
	47	Reduce the high frequency noise	Add booster resistor 3ohm(SD013300B80) PR90,PR91 on 1.8V/1.5V and PR124,PR145 on CPU CORE
	34	Add design margine	Change PC38 to 4.7U_1210(SE065475K80)
PVT			Add 68ohm(SD011680A80) PR155 and change PR9 to 68ohm
	39	Change +2.5VSP enable signal for HW request	Change +2.5VSP enable signal to +3VS
	40	For EMI request to reduce CPU power board band	Change PQ30,PQ34 to IRF7821(SB578210010); PQ31,PQ35 to IRF7832(SB578320010)
	40	For cost down	del PC100 and PR122,PR123,PR125,PR127,PR129,PR130

HW PIR LIST

HTW00 LA-2871 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	5/30	P29	ADD PULL DOWN 100K_0402_5% R475 ON SUSP#	TO PREVENT SUSP# FLOATING
2	5/30	P29	ADD PULL DOWN 100K_0402_5% R476 ON SYSON	TO PREVENT SYSON FLOATING
3	6/14	P17	CHANGE C241,C251 FROM 18PF TO 15PF	FINE TUNE RTC TIMING
4	7/01	P30	CHANGE LED TYPE FROM SIDE VIEW TO TOP VIEW	UPDATE LED LIBRARY
5	7/01	P30	CHANGE KB CONNECTOR EMI CAPS TO MOUNT	FOR EMI REQUEST
6	7/01	P27	ADD SPK_SEL CONNECTION BETWEEN EC AND CODEC	FOR CODEC EQ SELECTION FOR SPEAKER
7	7/01	P29	ADD MB_ID R477,R478 ON PIN88	FOR EC MB IDENTIFY
8	7/01	P17	CHANGE SATA DC COUPLING CAPS CAPACITANCE TO 3.9nf	TO MEET INTEL CRB RECOMMAND VALUE
9	7/01	P30	CHANGE LED RESISTOR R265, R266, R270, R272, RESISTANCE	TO INCREASE LED BRIGHTNESS
10	7/01	P20	ADD SATA HDD POWER CONTROL CIRCUIT	TO RESERVE BACKUP SOLUTION FOR SATA HDD RESET
11	7/01	P28	ADD R484 FOR MIC JACK GROUND PIN CLEAN	TO IMPROVE MIC SOUND QUALITY
12	7/01	P28	CHANGE U21 LDO POWER SOURCE FROM +5VALW TO +5VS	FOR POWER TRACE LAYOUT IMPROVE

HTW00 LA-2871 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	8/6	P28	CHANGE U21 PIN 4 FROM +5VS TO +5VALW	TO PREVENT NOISE FROM HDD SPIN UP
2	8/6	P15	CHANGE R306, R307 FROM RES TO BEAD	FOR EMI REQUEST
3	8/6	P21	CHANGE U2 FROM H-50P (H=2mm) TO TS6121C (H=4mm)	FOR COST POINT OF VIEW
4	8/6	P23	CHANGE D19 LED COLOR FROM GREEN TO BLUE	CUSTOMER SPEC CHANGE
5	8/6	P09	ADD R488 0_0603 BETWEEN +2.5VS_CRTDAC TO +2.5VS	TO IMPROVE CRT VIDEO QUALITY
6	8/6	P29	ADD PULL HIGH RES R487 ON PIN176 FOR WW/JPN# SELECT	TO CONTROL M/B CONFUIRATION
7	8/6	P30	CHANGE D15,D18,D40,D42 LED COLOR FROM GREEN TO BLUE	CUSTOMER SPEC CHANGE

HTW00 LA-2871 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	8/22	P20	CHANGE C661,C662,Q44,Q45,Q47,Q48,R411,R479,R480,R482 ,R483 FROM MOUNT TO RESERVE	REMOVE SATA-HDD POWER RESET FUNCTION FOR SW REQUEST
2	8/22	P18 P28	CHANGE D38,R485 FROM MOUNT TO RESERVE CHANGE R459 RESISTANCE FROM 4.53K TO 3.9K CHANGE R463 RESISTANCE FROM 4.22K TO 6.19K CHANGE R462 RESISTANCE FROM 4.87K TO 3.3K	TO REDUCE HEAD PHONE GAIN SETTING
3	8/22	P31	CHANGE JP4 AND JP6 VENDOR FROM ACES TO MANUNIX	FOR CUSTOMER'S REQUEST
4	8/22	P31	RESERVE JP31	FOR TEST ABILITY

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