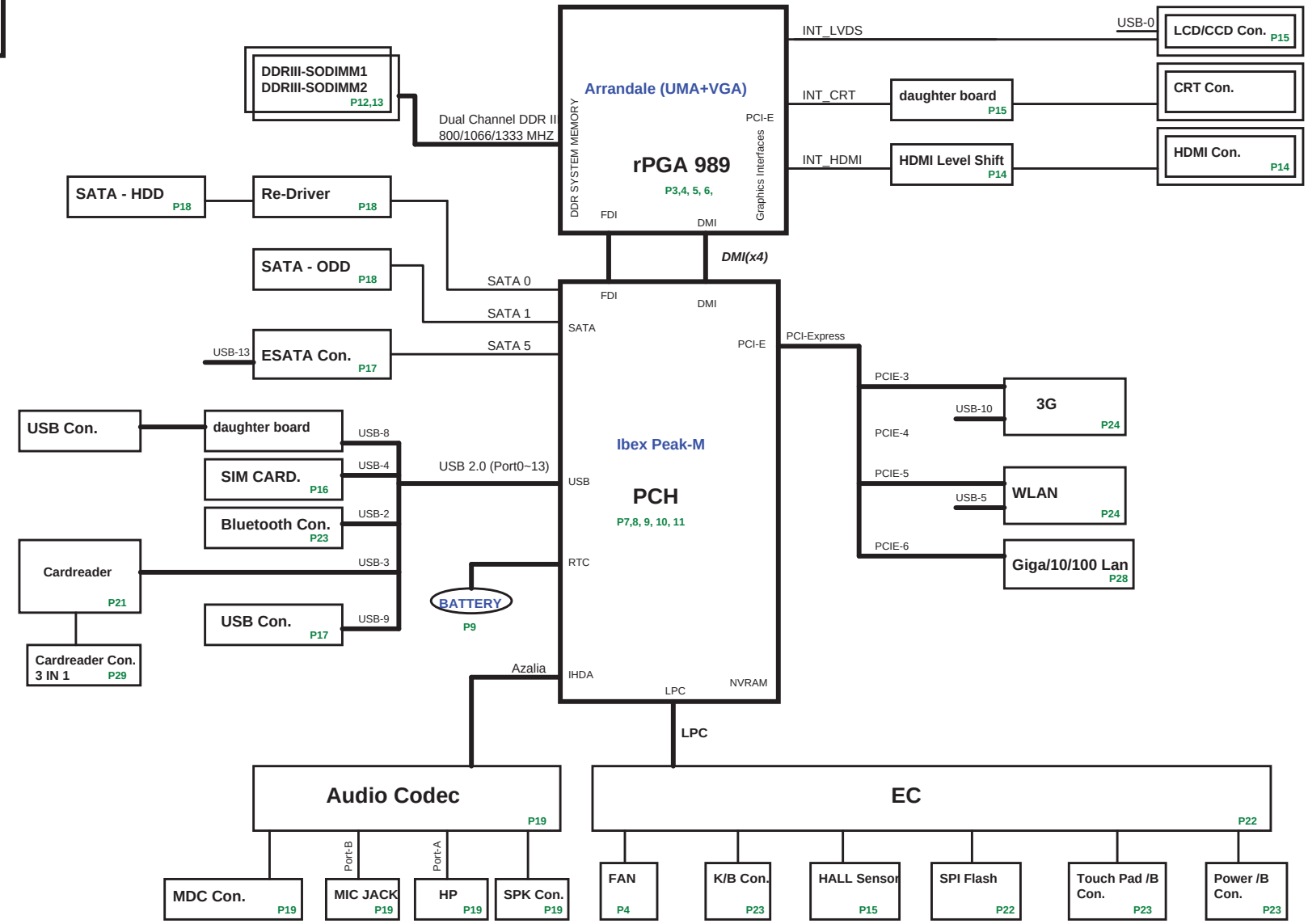
TE2 Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT



CK505 P2

POWER SYSTEM

ISL88731A	P25
RT8210B	P26
UP6163	P27
UP6111A	P28
RT015A	P29
ISL62882C	P30
RT8152C	P32

+VCC_CORE

+1.5V
+1.5VSUS

+VTT
+1.05V

+1.8V

+1.5V_S5

+3VPCU
+3V_S5
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF

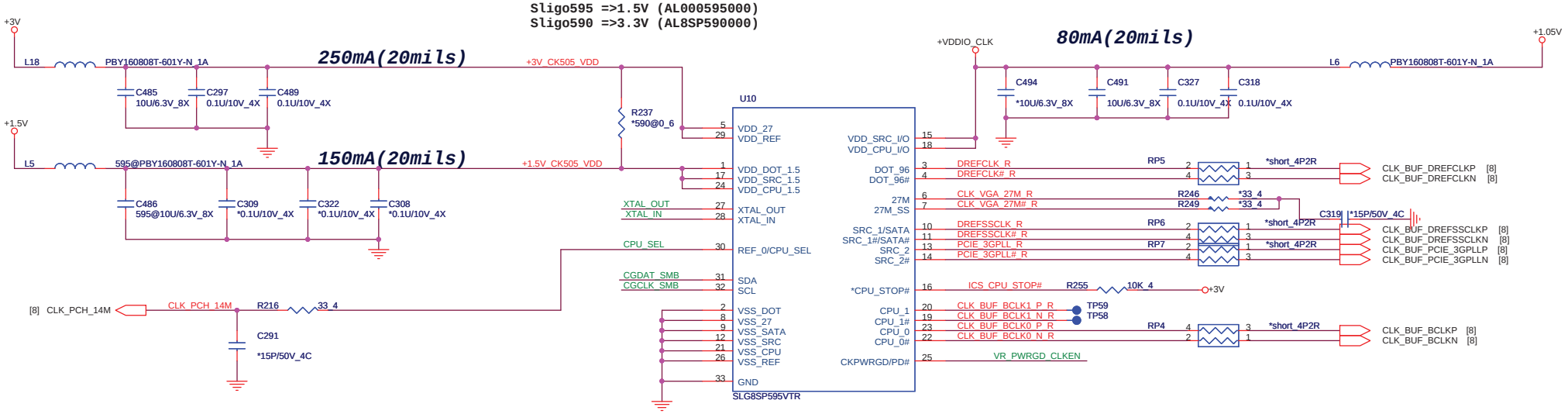
Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	Block Diagram	2A

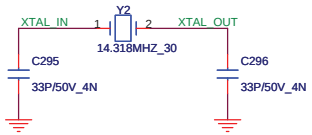
Date: Wednesday, March 10, 2010 Sheet 1 of 35

CLOCK Gen [CLK]

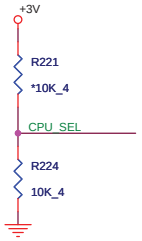
Pin1/17/24
Sligo595 =>1.5V (AL000595000)
Sligo590 =>3.3V (AL8SP590000)



CLK CRYSTAL

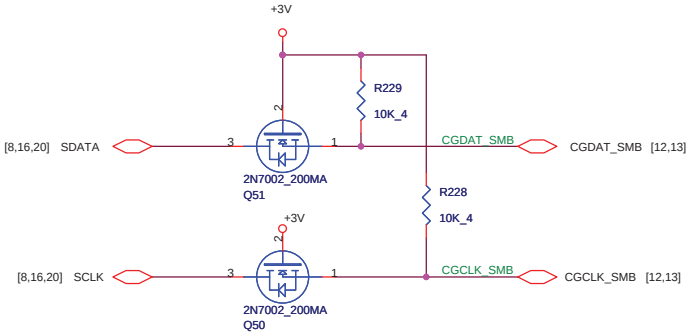


CLK CPU_SEL



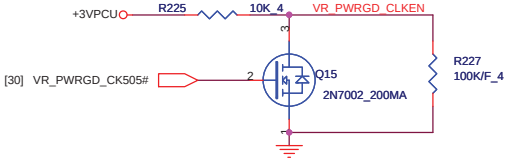
	0	1
CPU_SEL	CPU =133MHz (default)	CPU=100MHz

CLK I2C



CLK POWERGOOD

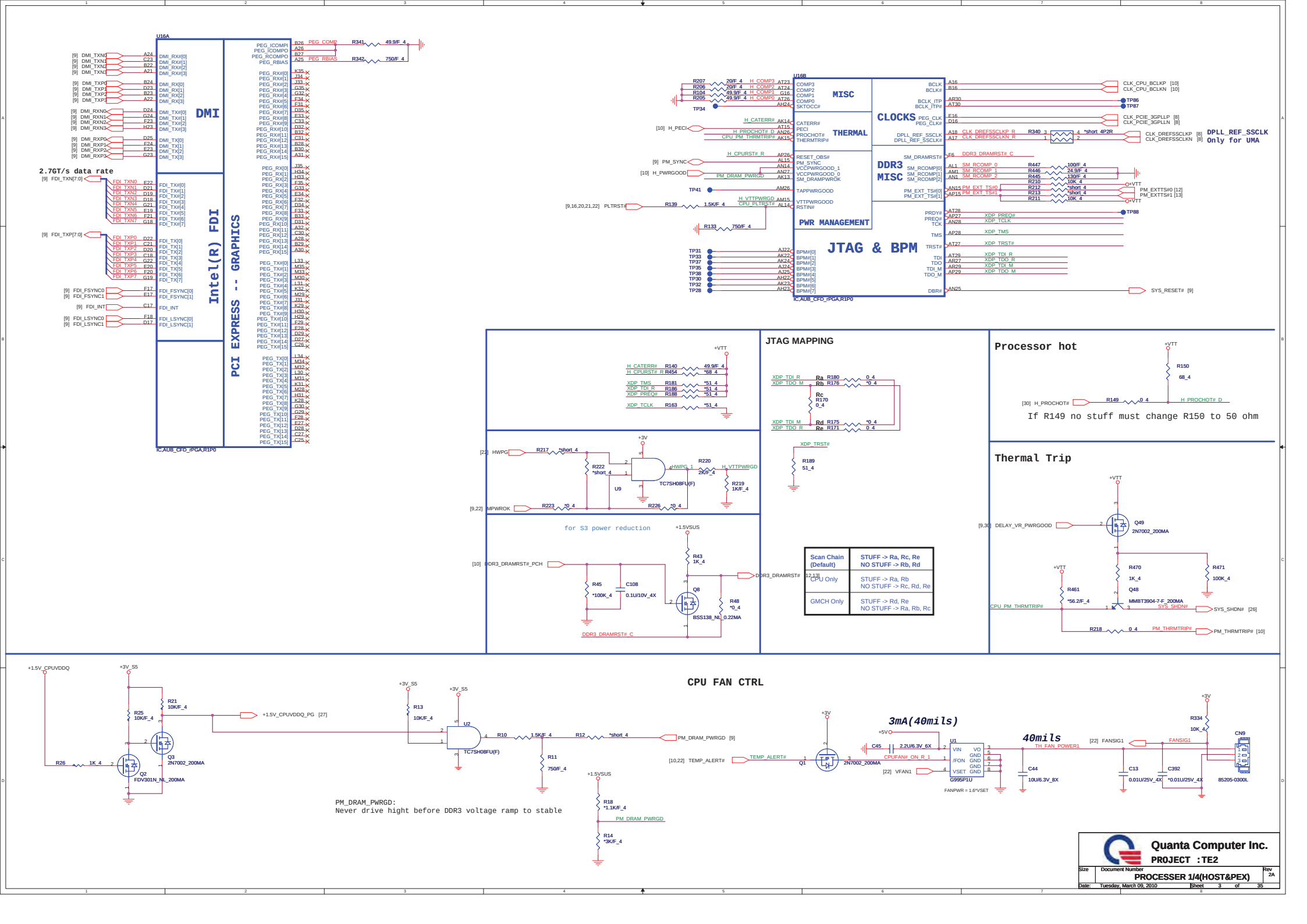
Change to +3VPCU
(follow CRB)



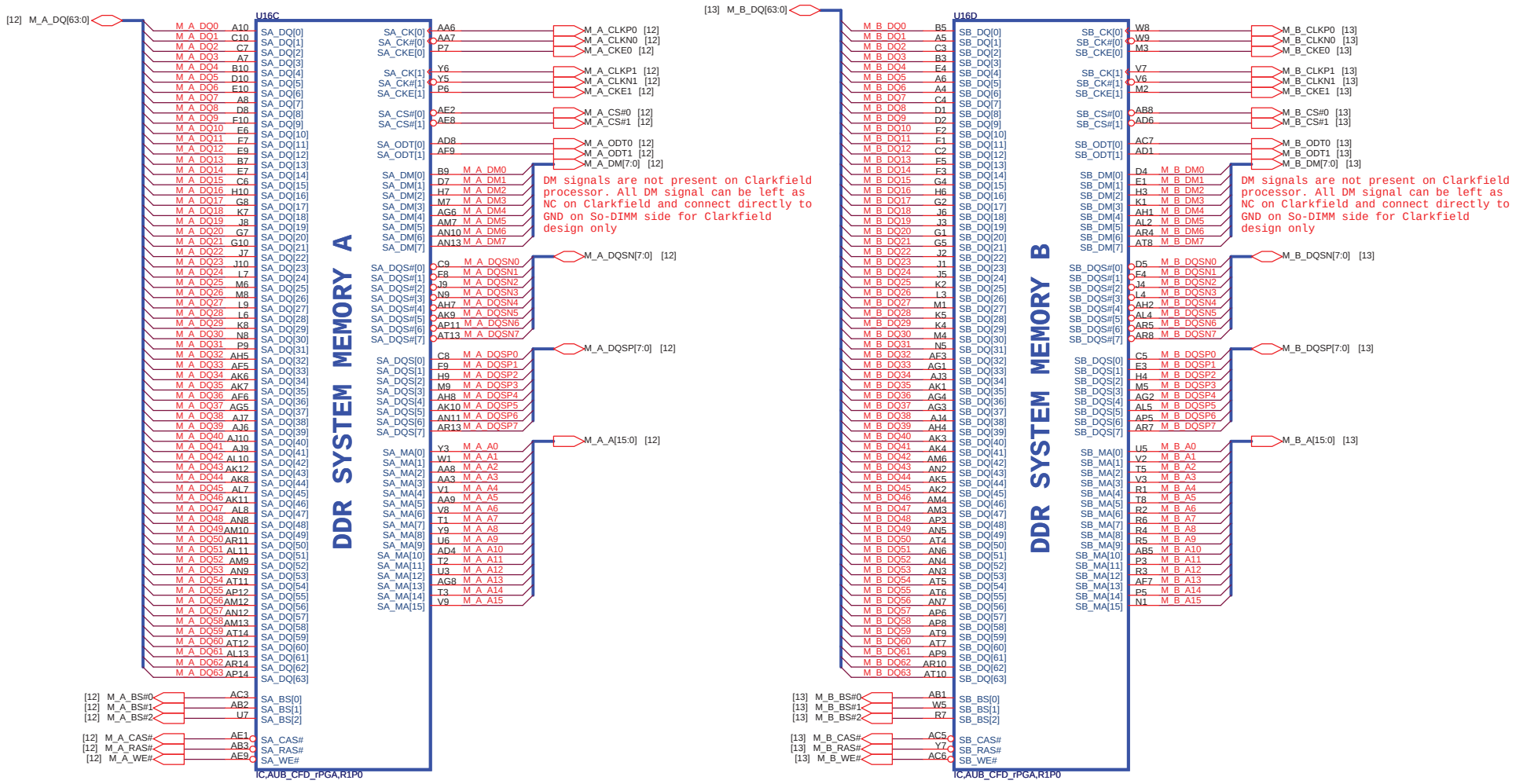
Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	CLOCK GENERATOR	2A

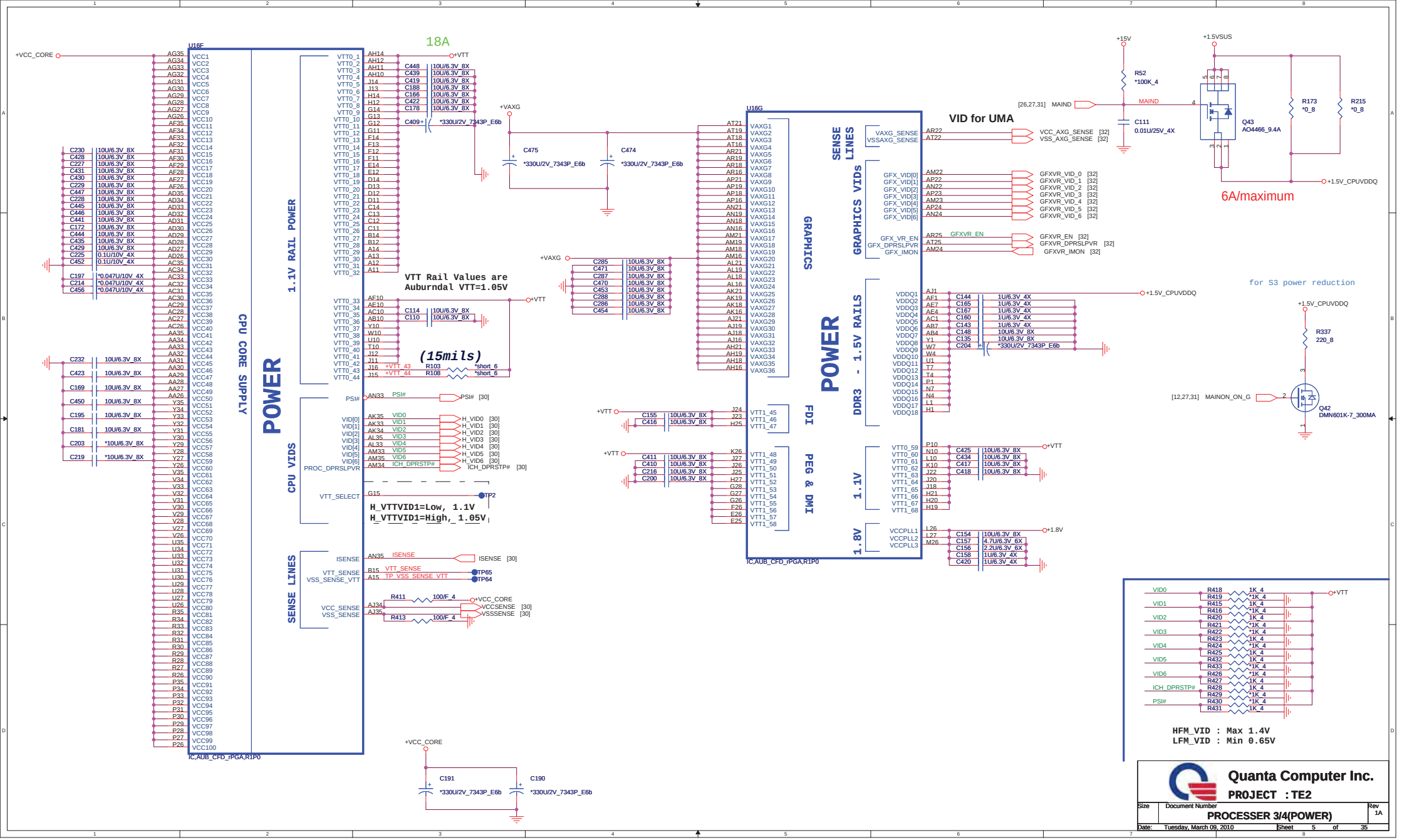
Date: Friday, March 19, 2010 Sheet 2 of 35


U16A
DMI
Intel(R) FDI
PCI EXPRESS -- GRAPHICS
2.7GT/s data rate
IC,AUB_CFD_rPGA,R1P0
U16B
MISC
THERMAL
CLOCKS
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
IC,AUB_CFD_rPGA,R1P0
DPLL_REF_SSCLK
Only for UMA
JTAG MAPPING
Scan Chain (Default)
STUFF -> Ra, Rc, Re
NO STUFF -> Rb, Rd
CPU Only
STUFF -> Ra, Rb
NO STUFF -> Rc, Rd, Re
GMCH Only
STUFF -> Rd, Re
NO STUFF -> Ra, Rb, Rc
Processor hot
If R149 no stuff must change R150 to 50 ohm
Thermal Trip
for S3 power reduction
CPU FAN CTRL
3mA(40mils)
40mils
PM_DRAM_PWRGD:
Never drive hight before DDR3 voltage ramp to stable
Quanta Computer Inc.
PROJECT :TE2
PROCESSER 1/4(HOST&PEX)
Size
Document Number
Rev
2A
Date: Tuesday, March 09, 2010
Sheet 3 of 35

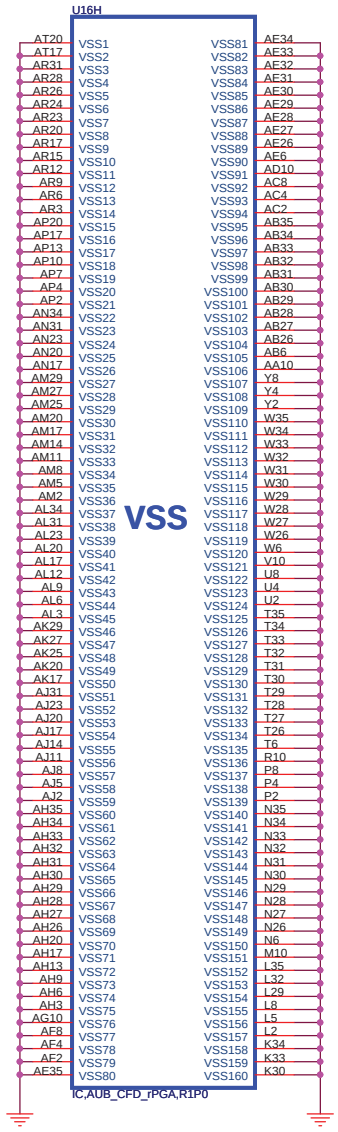
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

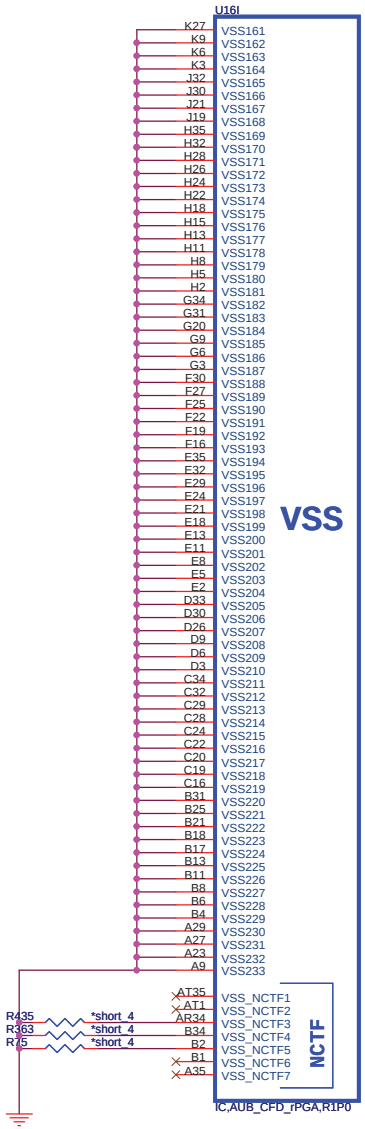


Quanta Computer Inc.			
PROJECT : TE2			
Size	Document Number		Rev
	PROCESSER 2/4(DDR)		2A
Date: Friday, February 26, 2010		Sheet 4 of 35	

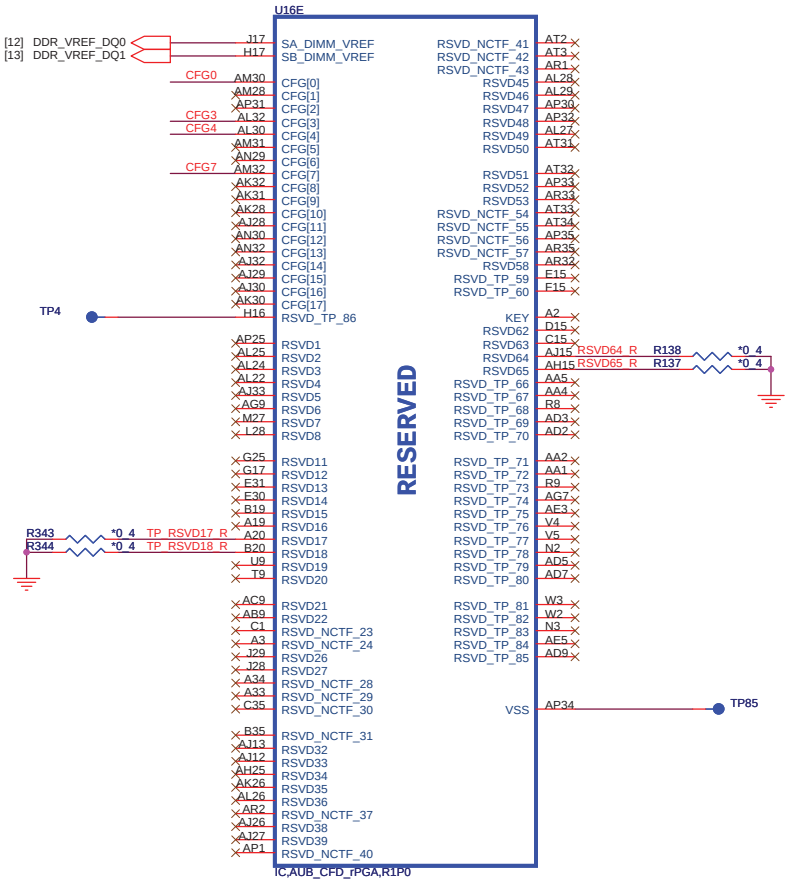

18A
U16F
POWER
CPU CORE SUPPLY
1.1V RAIL POWER
CPU VIDS
SENSE LINES
IC,AUB_CFD_rPGA,R1P0
VTT Rail Values are
Auburndal VTT=1.05V
(15mils)
H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V
U16G
POWER
GRAPHICS
FDI PEG & DMI
DDR3 - 1.5V RAILS
1.1V
1.8V
GRAPHICS VIDs
SENSE LINES
IC,AUB_CFD_rPGA,R1P0
VID for UMA
6A/maximum
for S3 power reduction
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V
Quanta Computer Inc.
PROJECT : TE2
PROCESSER 3/4(POWER)
Tuesday, March 09, 2010
Sheet 5 of 35
Rev 1A

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)





AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

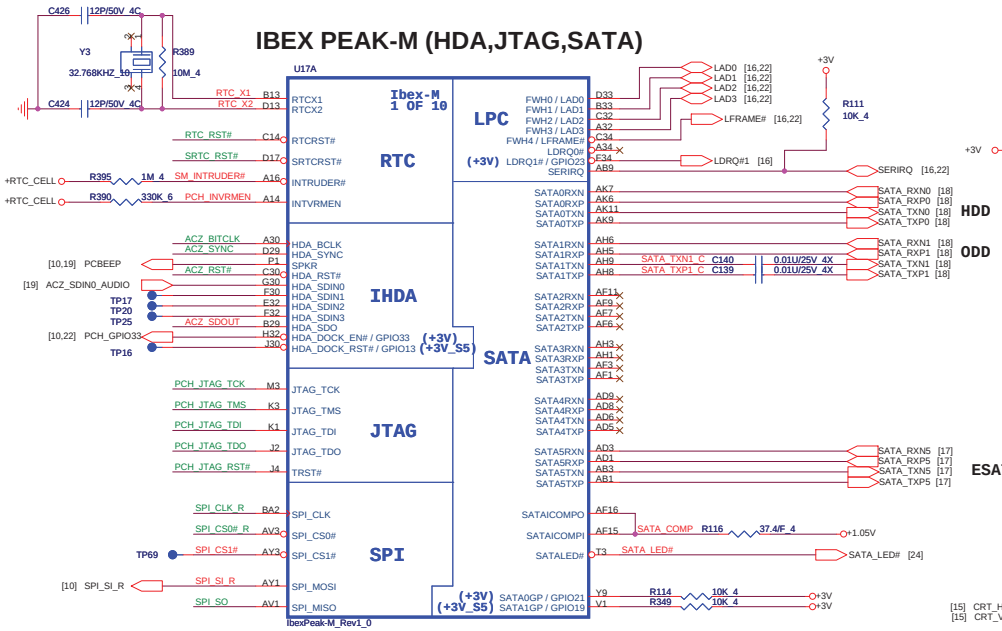
For Discrete only

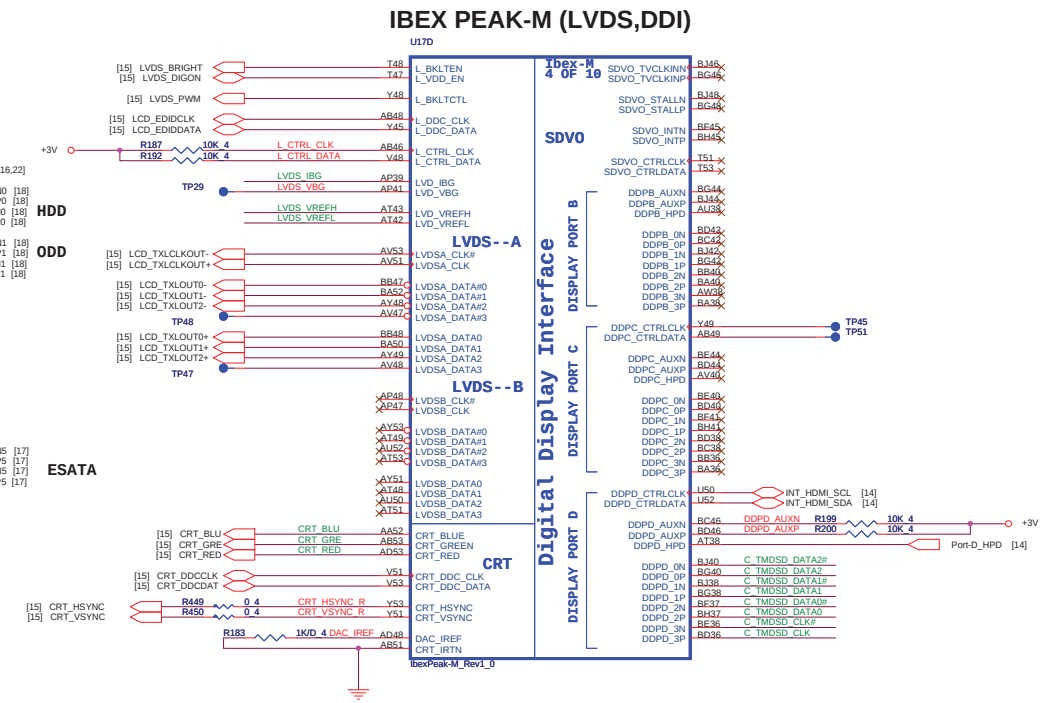
CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	PROCESSER 4/4 (GND)	2A
Date: Tuesday, March 09, 2010	Sheet 6 of 35	

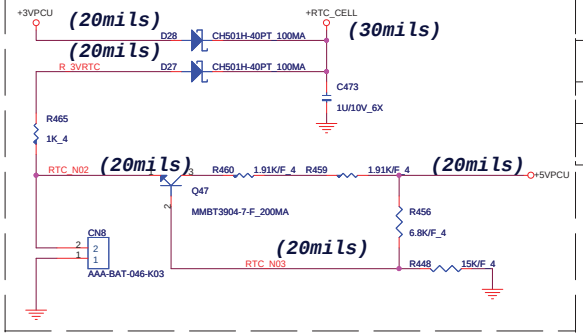
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs





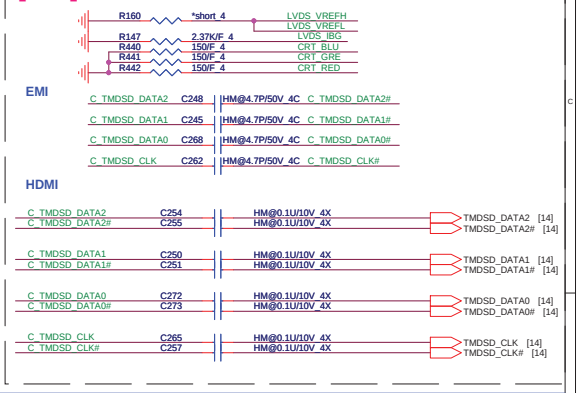
[RTC]

RTC BATTERY

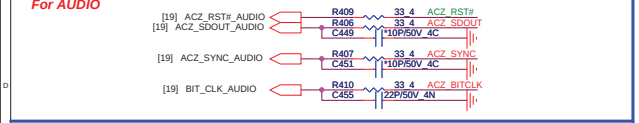


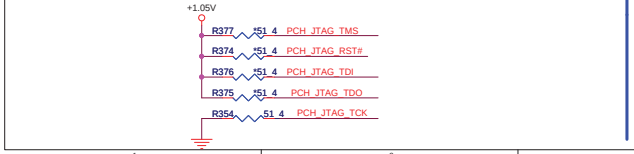
Port	Strap	How to enable Port?	How to disable Port?
LVDS	L_DDC_DATA	PU to 3.3V with 2.2k+/- 5%	NC
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port D	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
eDP	CFG[4]	PD to GND directly	NC

[UMA]



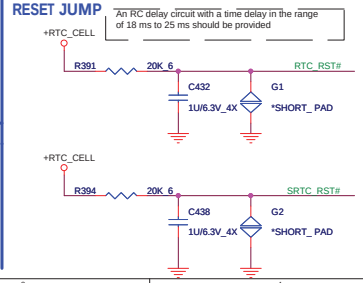
For AUDIO



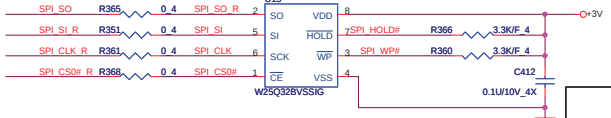


RESET JUMP

An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided



4M byte SPI ROM



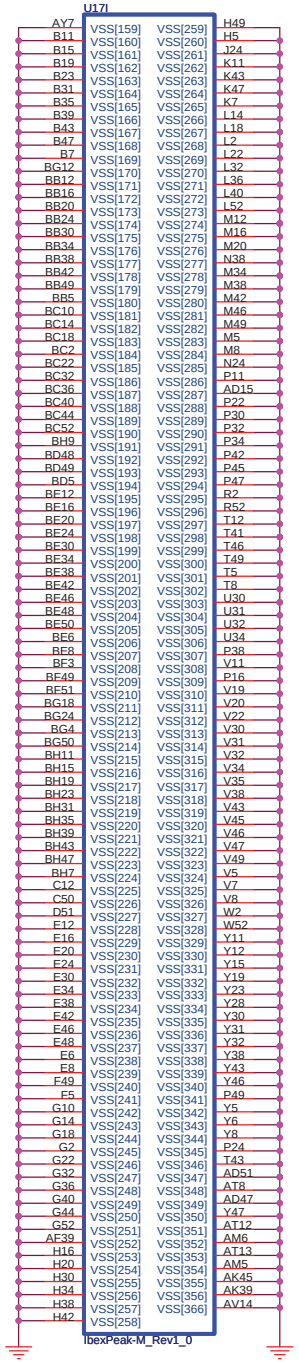
PCH	2MB	4MB	8MB
PM55	●		
HM55		●	
HM57/PM57		●	●
QM57/QS57			●

Quanta Computer Inc.
PROJECT : TE2

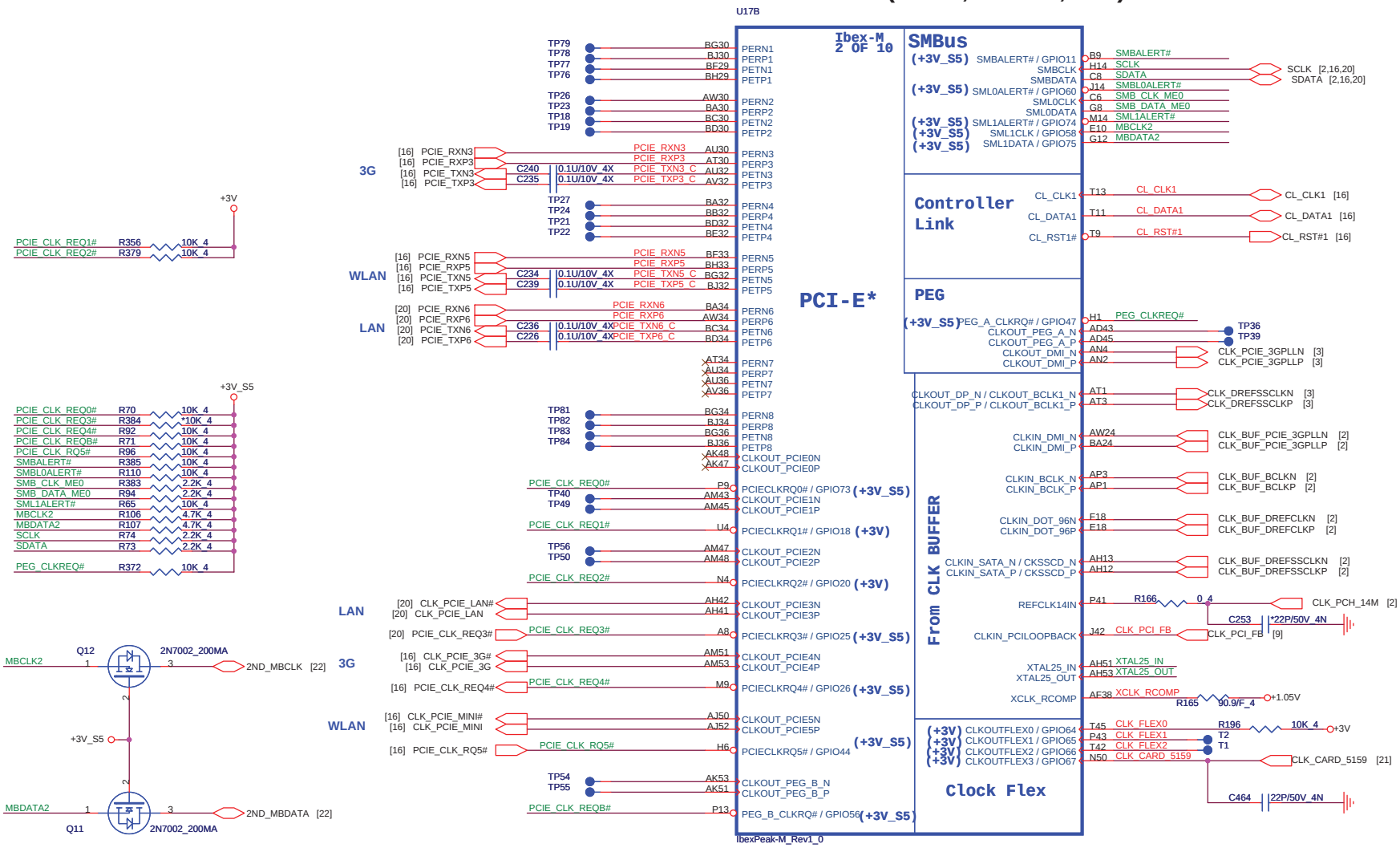
Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	2A

Date: Wednesday, March 10, 2010 Sheet 7 of 35

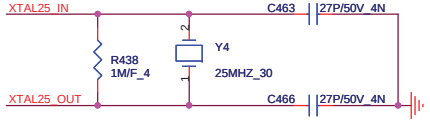
IBEX PEAK-M (GND)



IBEX PEAK-M (PCI-E,SMBUS,CLK)

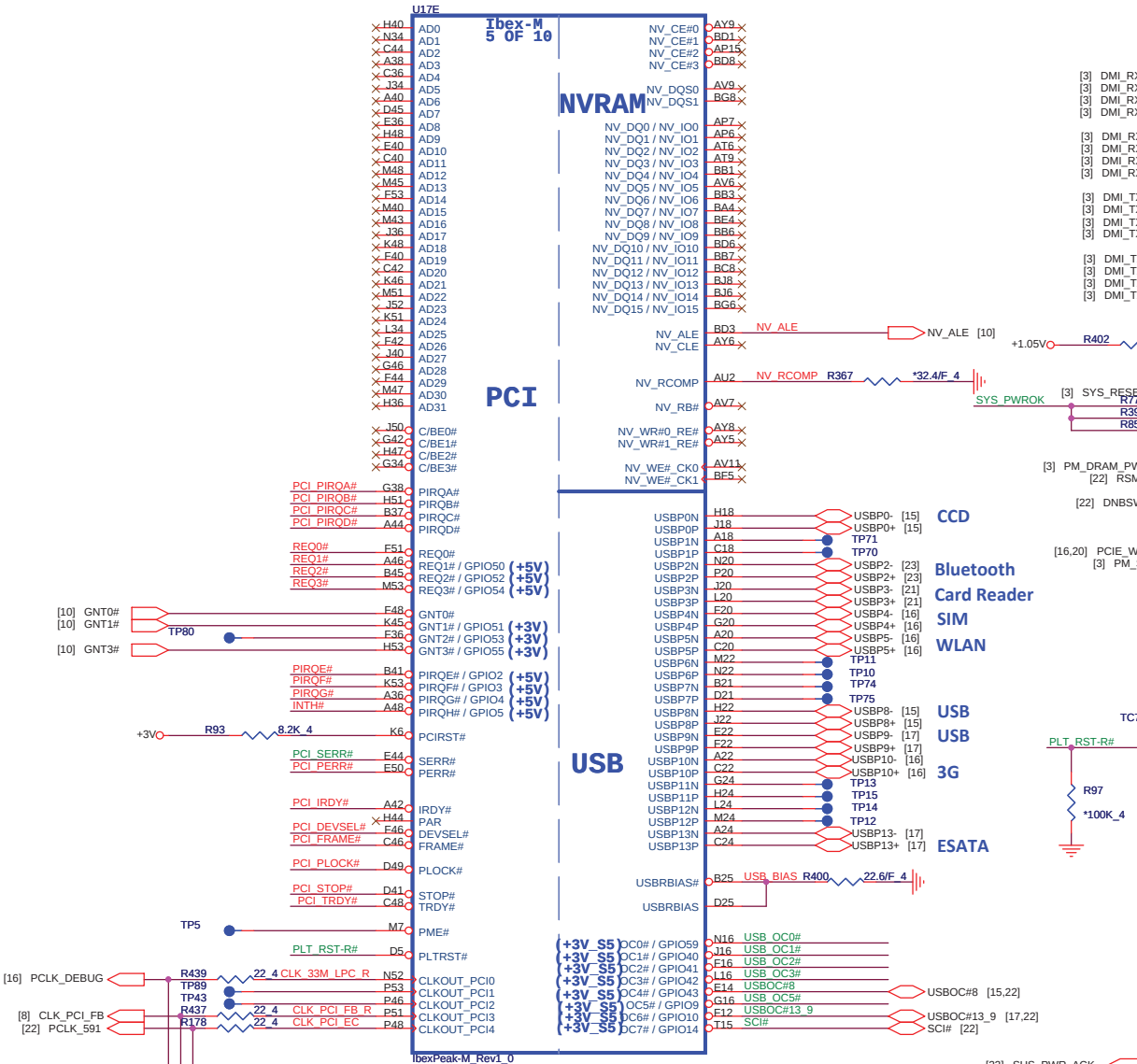


Placement close

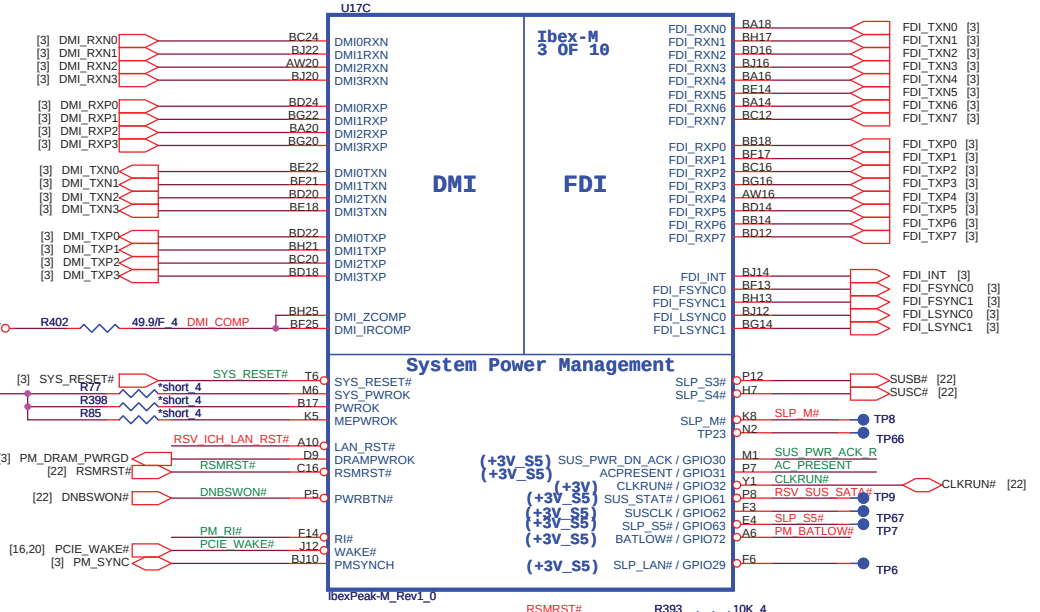


Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: PCH 2/5 (PCIE, SMBUS, CK)	Rev: 2A
Date: Wednesday, March 10, 2010	Sheet 8 of 35	

IBEX PEAK-M (PCI,USB,NVRAM)

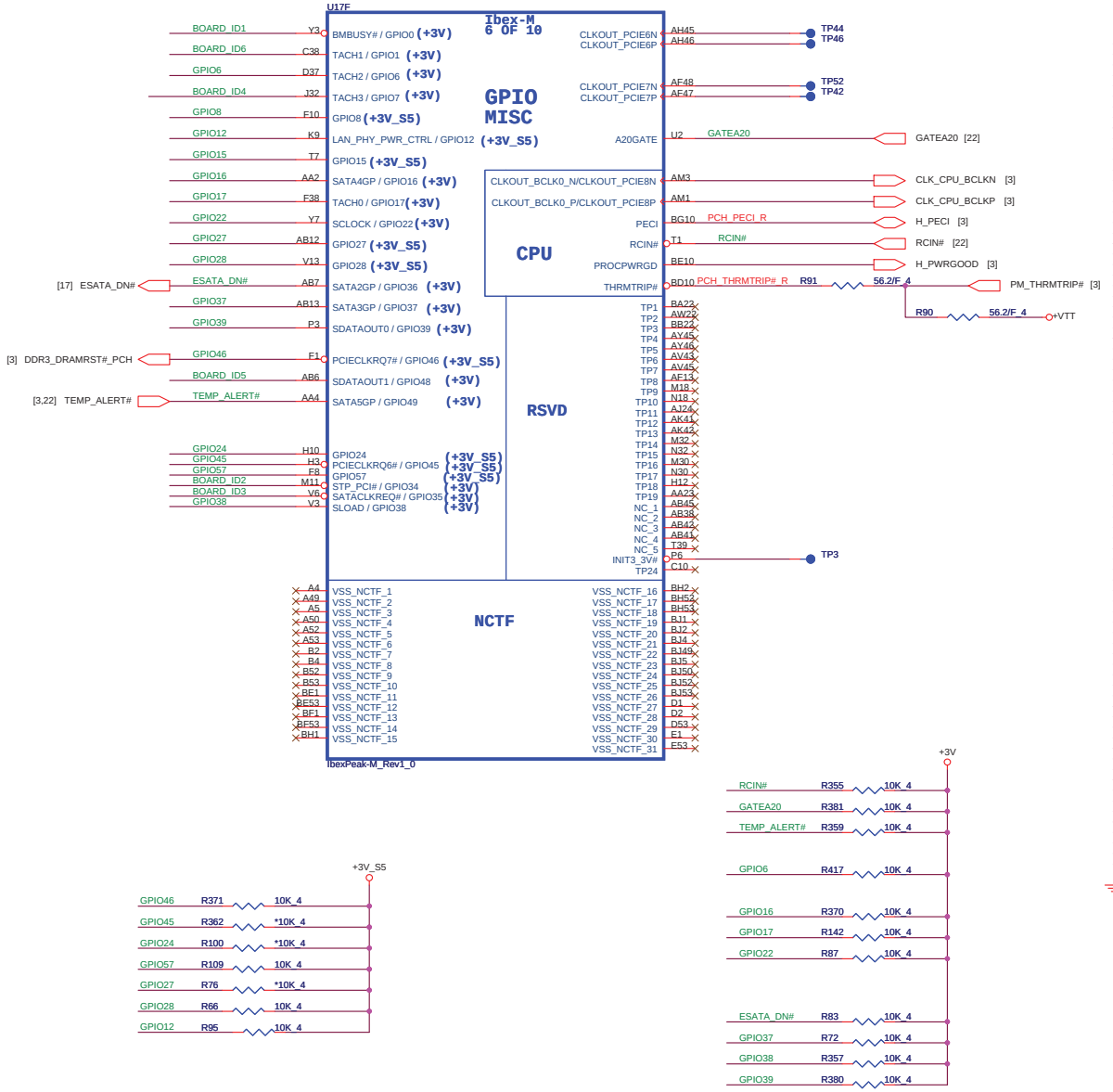


IBEX PEAK-M (DMI,FDI,GPIO)

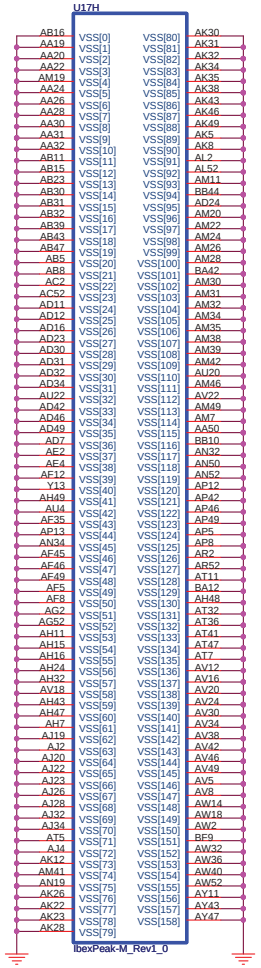


Quanta Computer Inc.	
PROJECT : TE2	
Size	Document Number: PCH 3/5 (PCI,ONFI,USB,DMI) — Rev: 2A
Date: Wednesday, March 10, 2010	Sheet 9 of 35

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



PCH Strap Pin Configuration Table

SPKR

[7,19] PCBEEP — *1K/F_4 — R364 — +3V

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

GNT3#/ GPIO55

[9] GNT3# — R452 — *10K/F_4

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

HDA_DOCK_EN #/GPIO33

[7,22] PCH_GPIO33 — R136 — 10K_4 — JP1 (2, 1) *SHORT PAD

0 = Top Block Swap Mode
1 = Default Mode (Internal pull-up)

GNT0#, GNT1#

[9] GNT0# — GNT0# R184 *1K/F_4
[9] GNT1# — GNT1# R185 *1K/F_4

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

SPI_MOSI

[7] SPI_SI_R — R348 — *1K_4 — +3V

NV_ALE

[9] NV_ALE — R98 — *10K_4 — +1.8V

1 = Enabled
0 = Disabled (Default)

GPIO8

GPIO8 — R81 — 10K_4 — +3V_S5

This signal has a weak internal pull up.
NOTE: This signal should not be pulled low

GPIO15

GPIO15 — R58 — 1K_4 — +3V_S5

0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

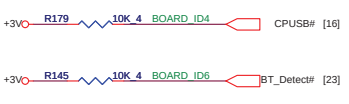
GPIO27

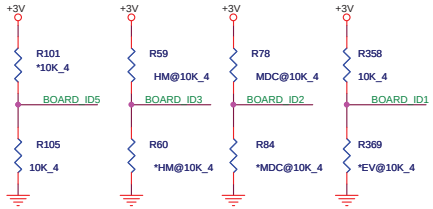
GPIO27 — R79 — *10K_4

0 = Disables the VccVRM. Need to use on-board filter circuits for analog rails.
1 = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.
This signal has a weak internal pull-up.

BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6
UMA SKU VGA SKU	H L					
W/ MDC W/O MDC		H L				
W/ HDMI W/O HDMI			H L			
W/O 3G W/ 3G				H L		
15" 14"					H L	
W/O BT W/ BT						H L





Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	2A
Date: Wednesday, March 10, 2010	Sheet 10 of 35	

+VCCA_DAC_1_2=69mA(15mils)

VCCCORE = 1.432A(80mils)

VCCALVDS= 59mA(15mils)

VCCLAN = 0.32A(30mils)

40mA(15mils)

VCCME = 1.849A(100mils)

VCC3_3 = 0.357A(30mils)

VCCVRM= 196mA(15mils)

VCCDMI= 31mA(15mils)

VCCPNAND= 156mA(15mils)

VCCIO = 3.062A(150mils)

68mA(15mils)

VCCME3_3= 85mA(15mils)

VCCIO = 3.062A(150mils)

37mA(15mils)

VCCSUS3_3 = 0.163A(20mils)

VCC3_3 = 0.357A(30mils)

V_CPU >1mA(15mils)

VCCRTC= 2mA(15mils)

VCCSUSHDA= 6mA(15mils)

V5REF_SUS< 1mA

V5REF< 1mA

VCCIO = 3.062A(150mils)

VCCME = 1.849A(100mils)

Reserve for clear CRT Power

POWER

Ibex-M 7 OF 10

CRT

LVDS

HVCMOS

DMI

NAND / SPI

VCC CORE

PCI E*

FDI

IbexPeak-M_Rev1_0

POWER

Ibex-M 10 OF 10

USB

SATA

PCI/GPIO/LPC

CPU

RTC

HDA

Clock and Miscellaneous

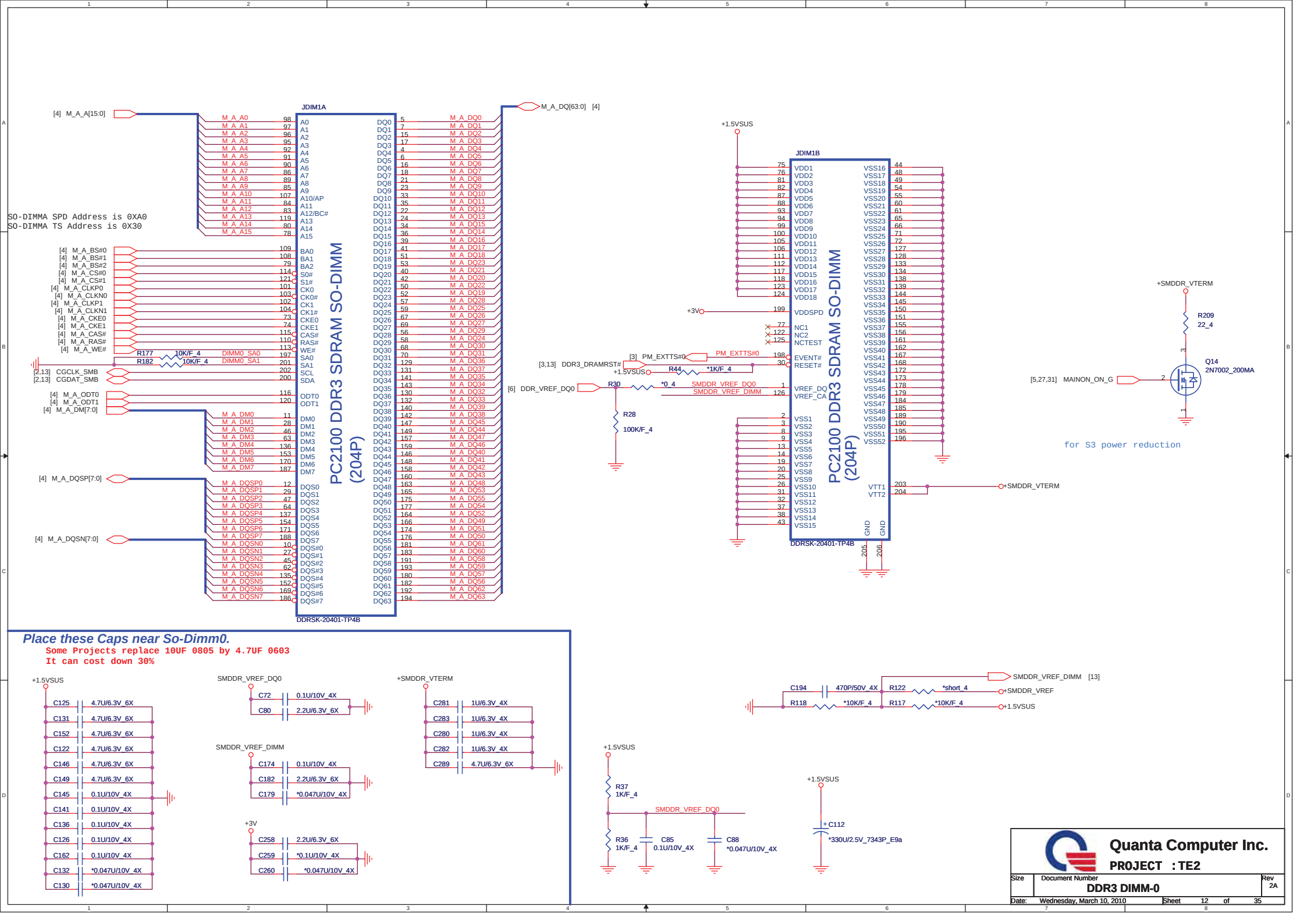
IbexPeak-M_Rev1_0

Quanta Computer Inc.

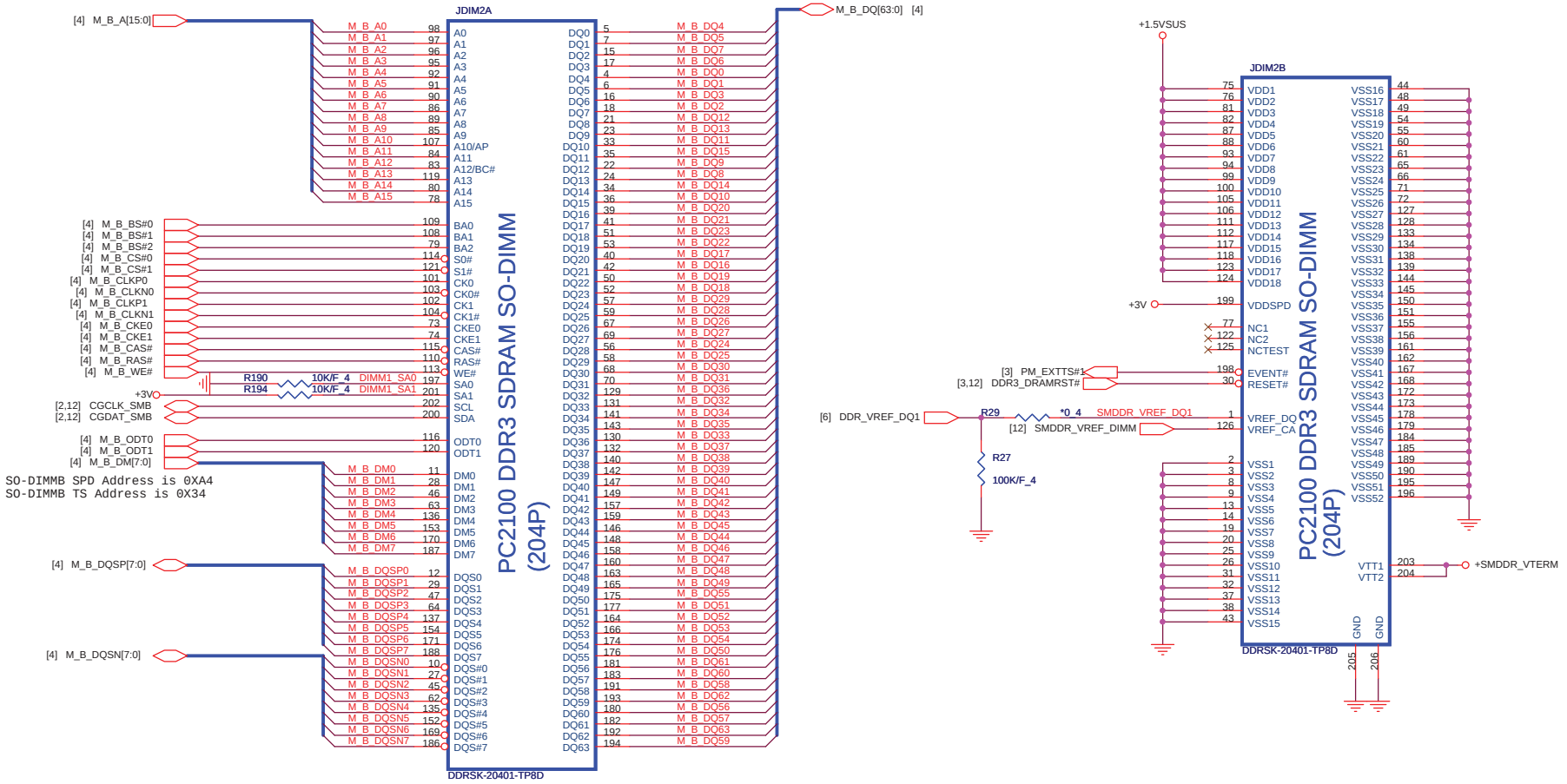
PROJECT : TE2

Size	Document Number	Rev
	PCH 5/5 (POWER)	2A

Date: Tuesday, March 09, 2010 Sheet 11 of 35

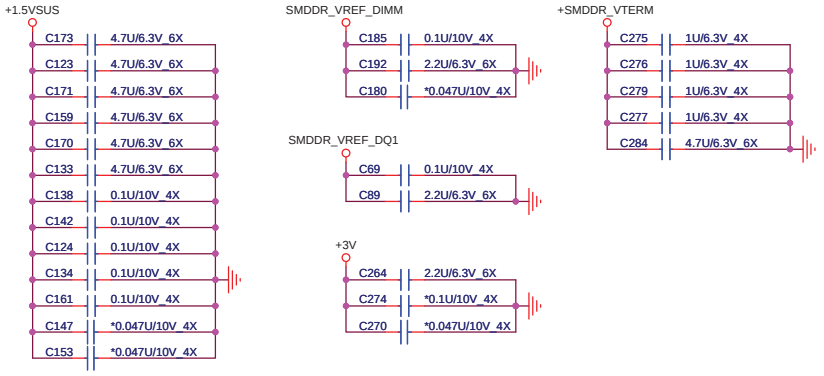


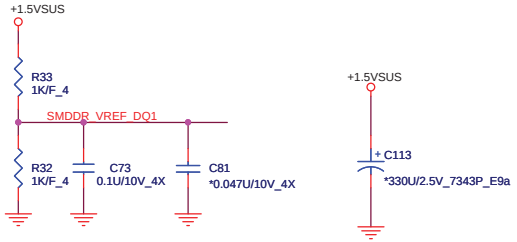
Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: DDR3 DIMM-0	Rev: 2A
Date: Wednesday, March 10, 2010	Sheet 12 of 35	



Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%





Quanta Computer Inc.

PROJECT : TE2

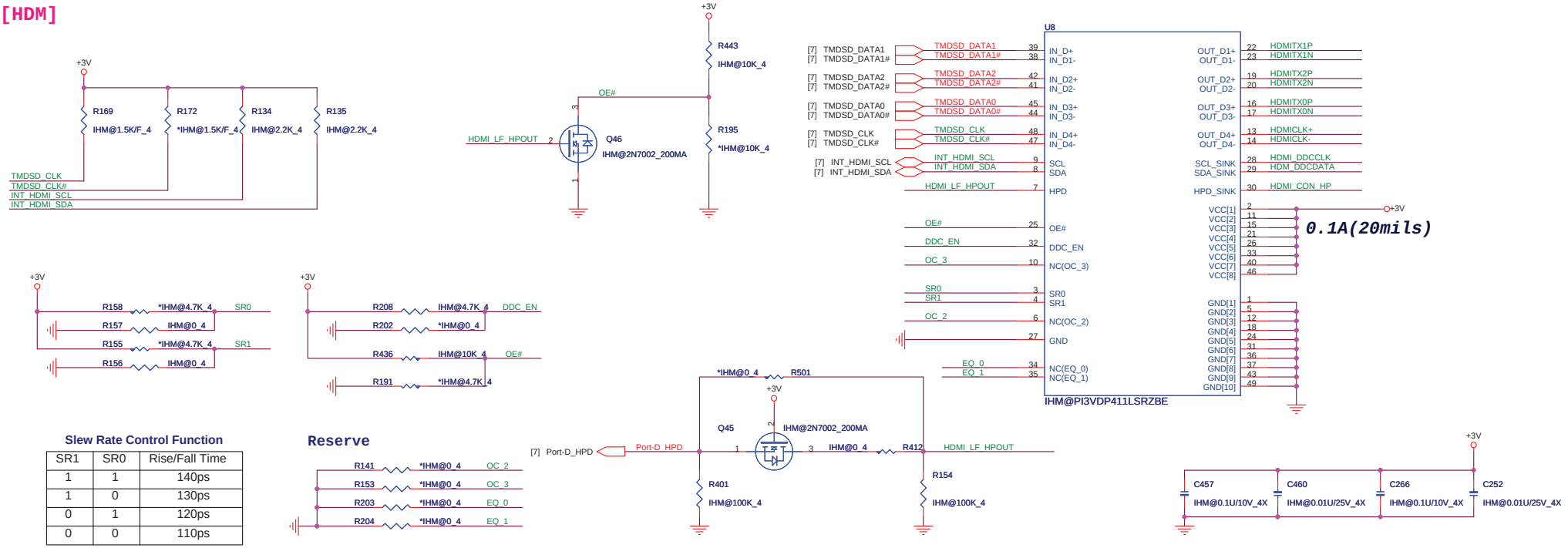
Size	Document Number	Rev
	DDR3 DIMM-1	2A

Date: Wednesday, March 10, 2010 Sheet 13 of 35

HDMI Conn

HDMI Level Shift UMA only

[HDM]

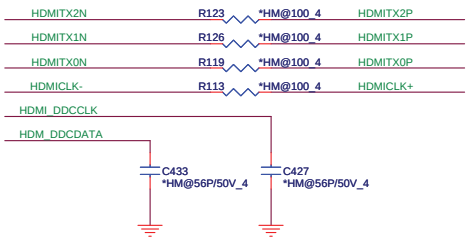


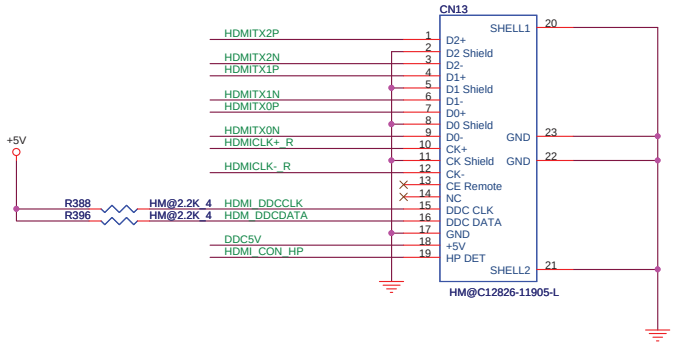
Slew Rate Control Function

SR1	SR0	Rise/Fall Time
1	1	140ps
1	0	130ps
0	1	120ps
0	0	110ps

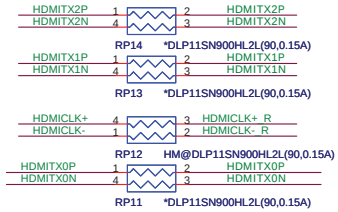
Reserve

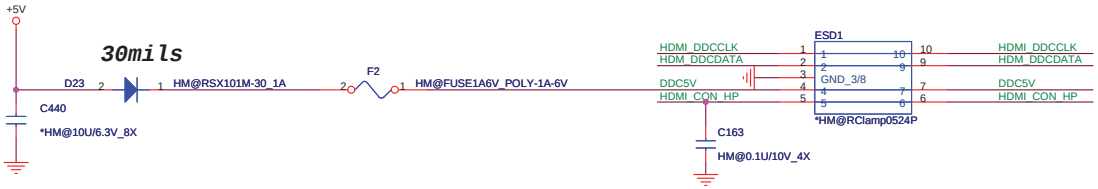
For EMI close to connector





Close to HDMI CONN





Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	HDMI CONN	2A

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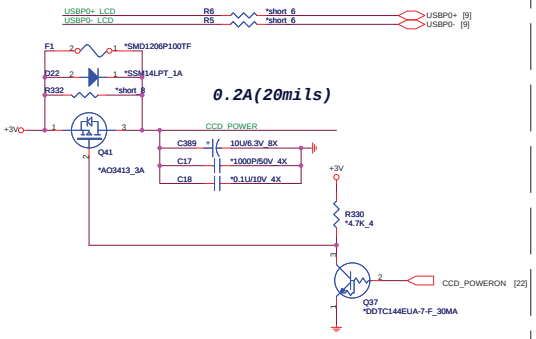
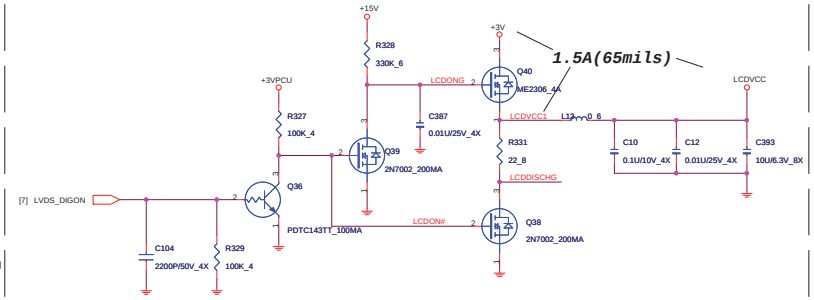
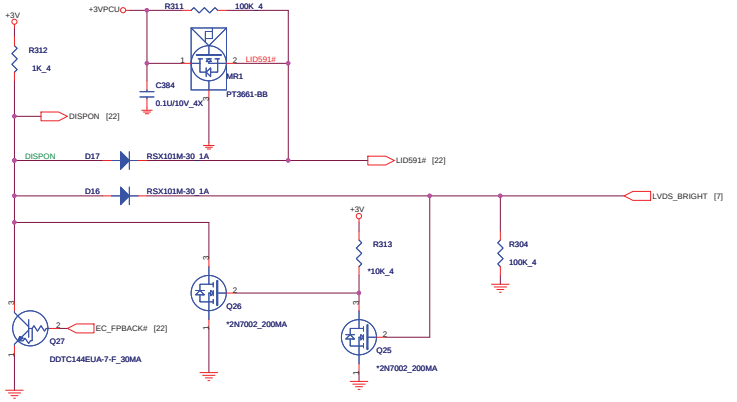
CCD [CCD]



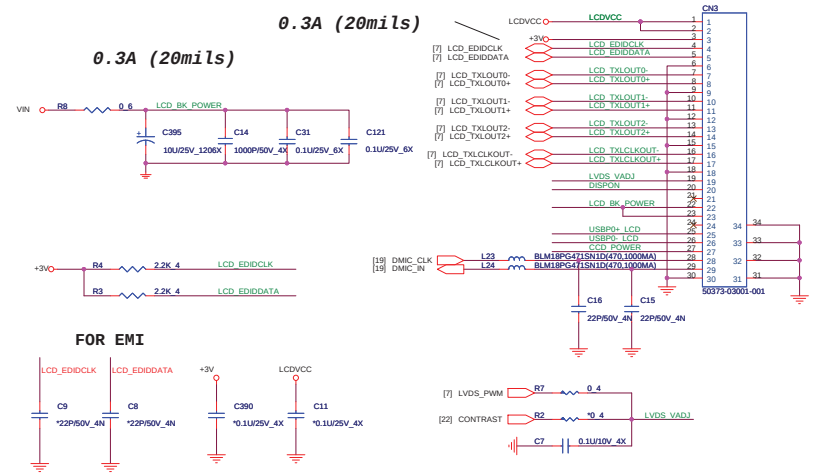
LCD POWER SWITCH [LDS]



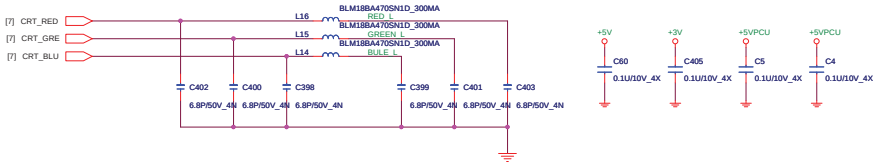
HALL SENSOR&BACK LIGHT SWITCH [HSR]



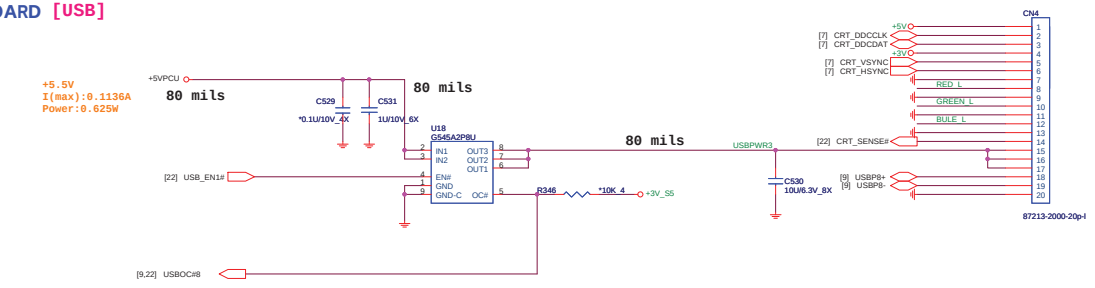
LCD Panel Module [LDS]



CRT [CRT]



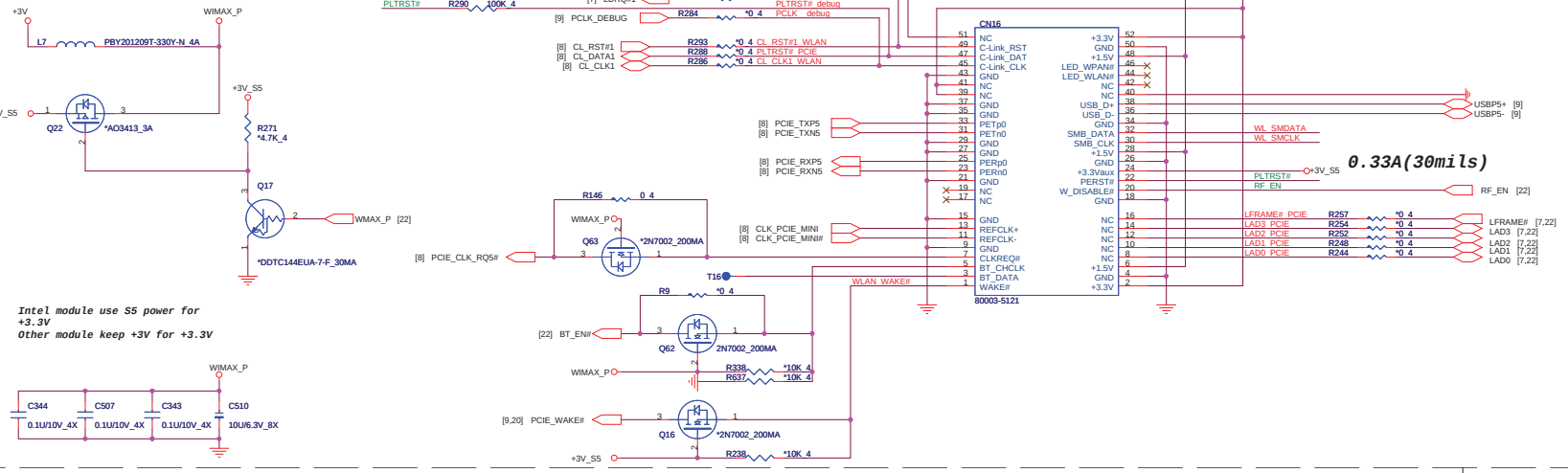
USB for CRT BOARD [USB]



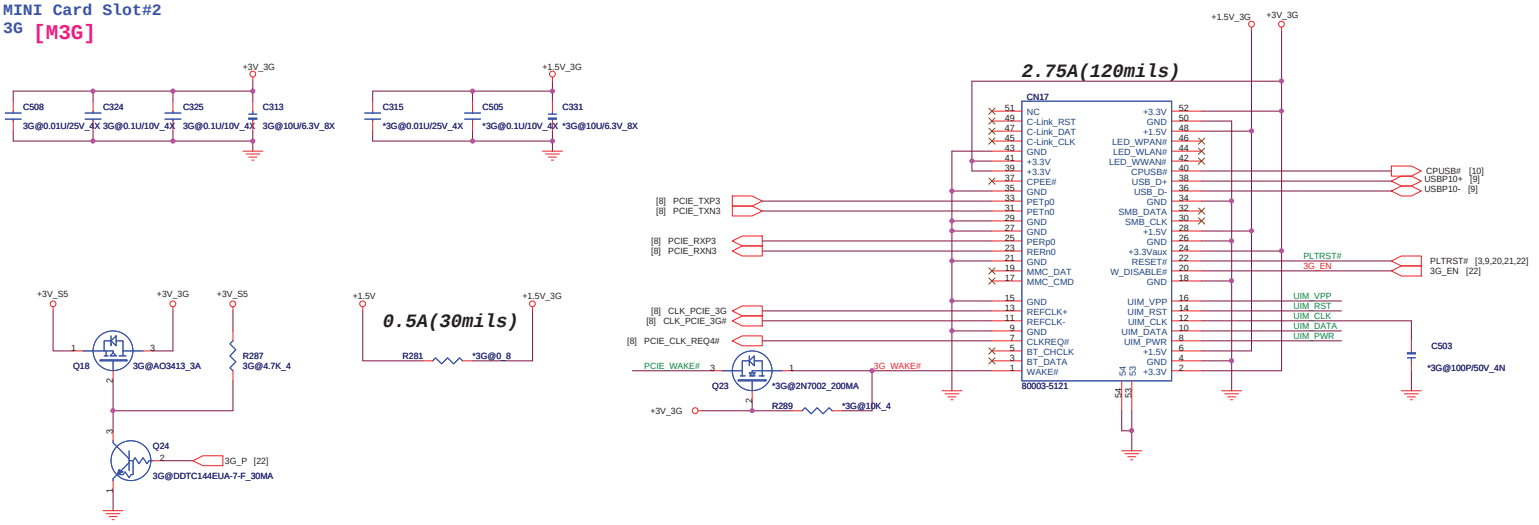
Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	LCD/LED Panel/CCD	2A
Date: Tuesday, March 09, 2010	Sheet 15 of 35	

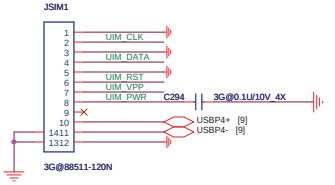
MINI Card Slot#1 (WiFi) [WLN]



MINI Card Slot#2 3G [M3G]



SIM CARD

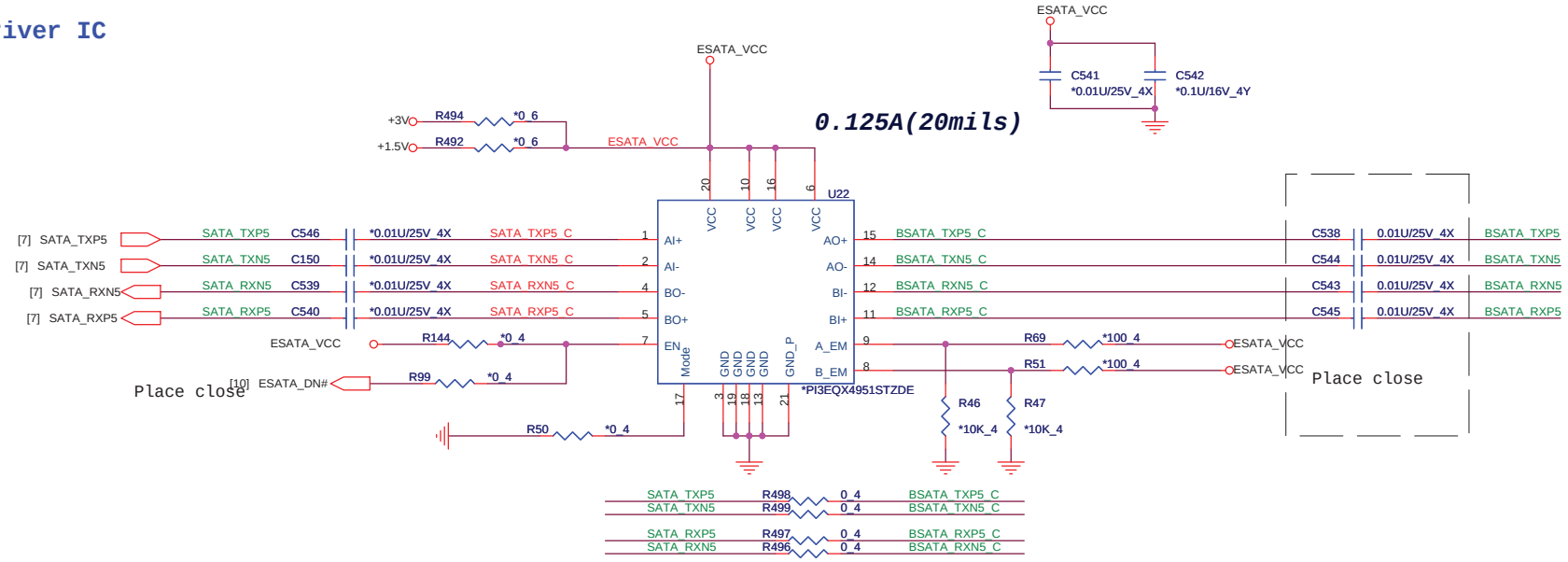


Quanta Computer Inc.
PROJECT : TE2

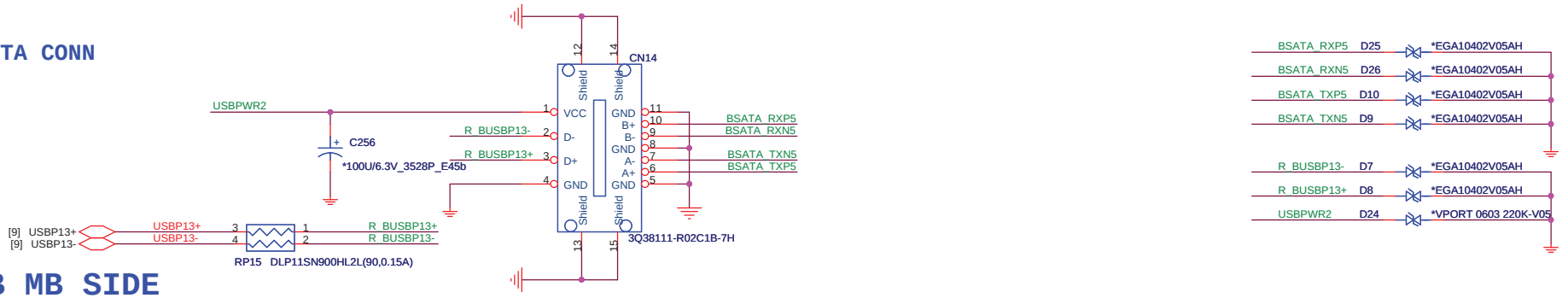
Size	Document Number	Rev
	MINI CARD(WLAN/3G/SIM Card)	2A
Date: Friday, March 19, 2010	Sheet 16 of 35	

E-SATA [ESA]

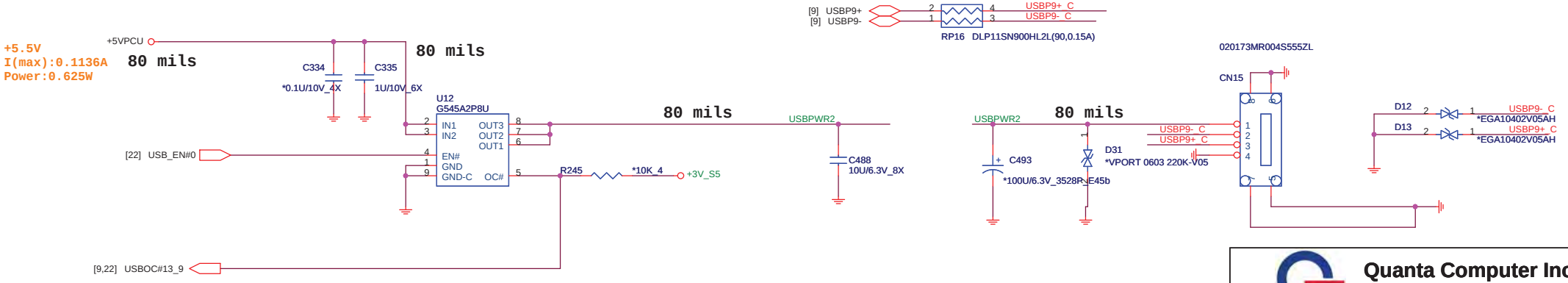
SATA HDD Re-driver IC



ESATA CONN



USB MB SIDE



Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: TP/SW/ESATA/USB+Audio/LED	Rev 2A
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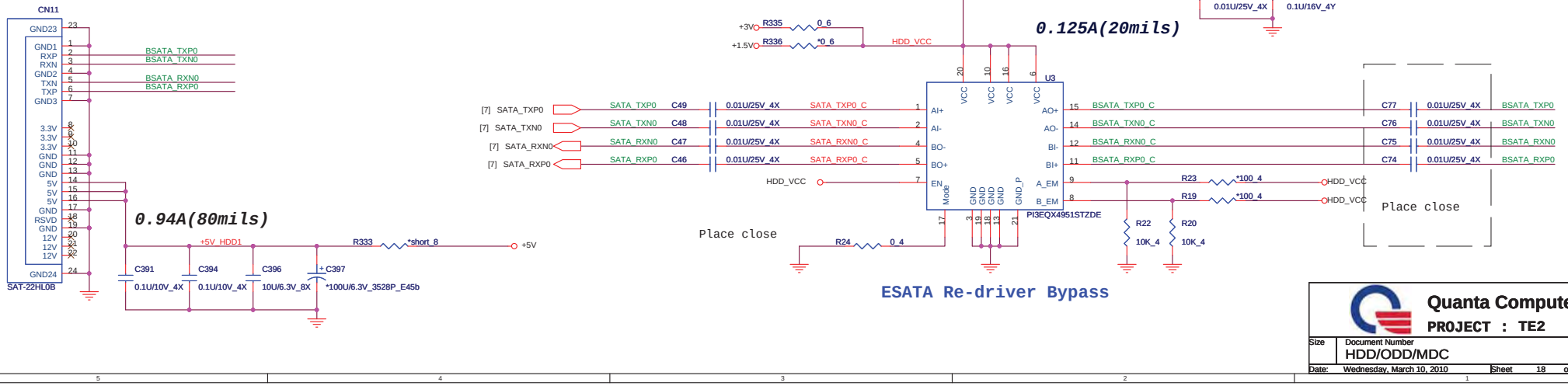
SATA ODD

[ODD]

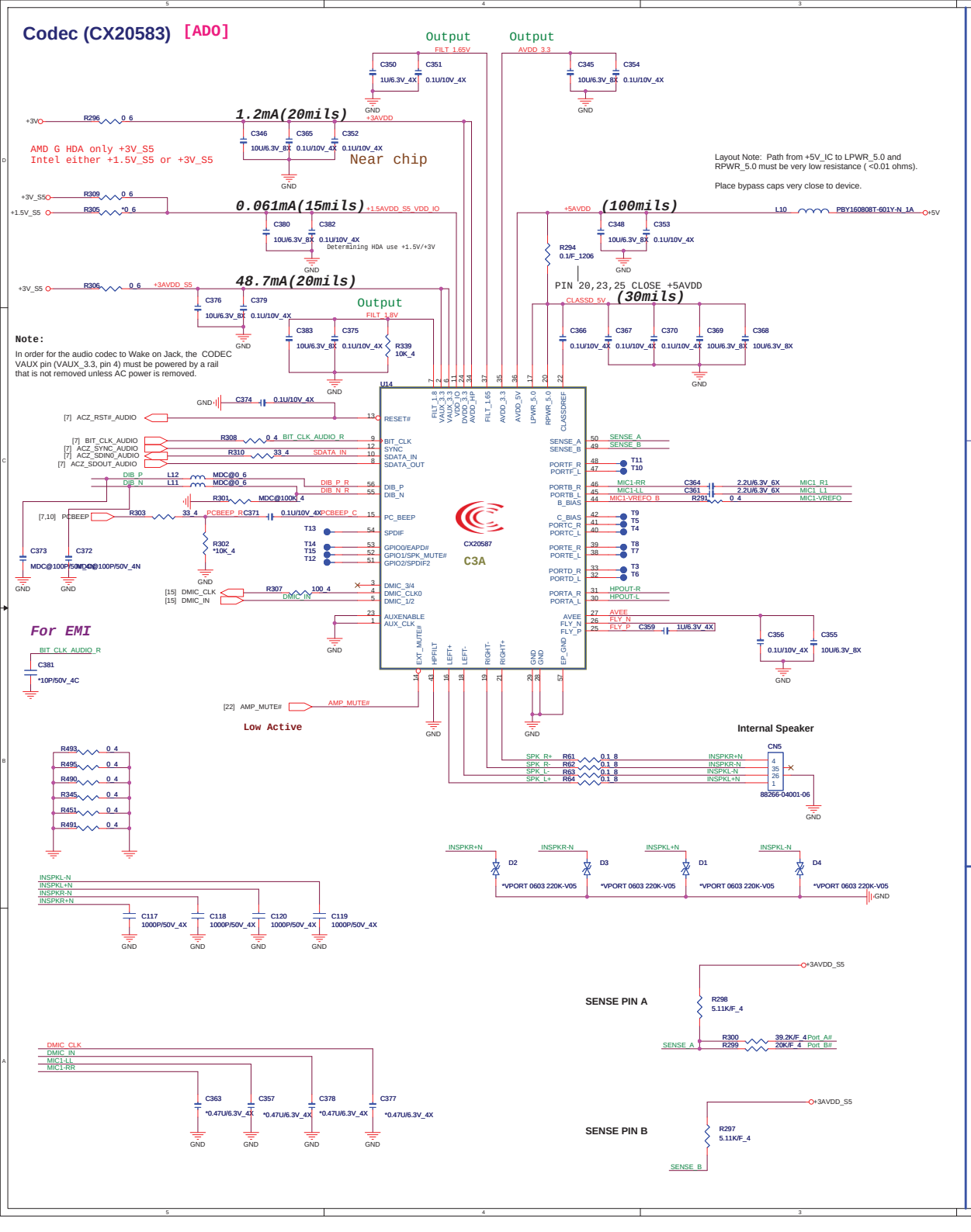
SATA HDD

[HDD]



Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: HDD/ODD/MDC	Rev: 2A
Date: Wednesday, March 10, 2010	Sheet 18 of 35	

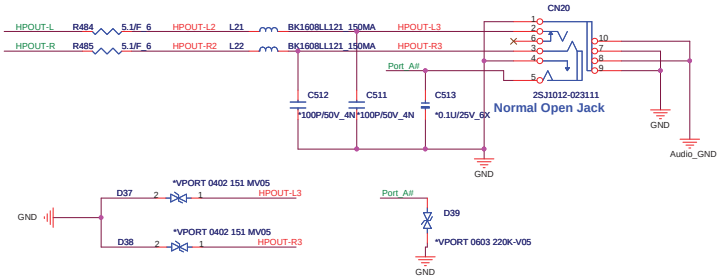
Codec (CX20583) [ADO]



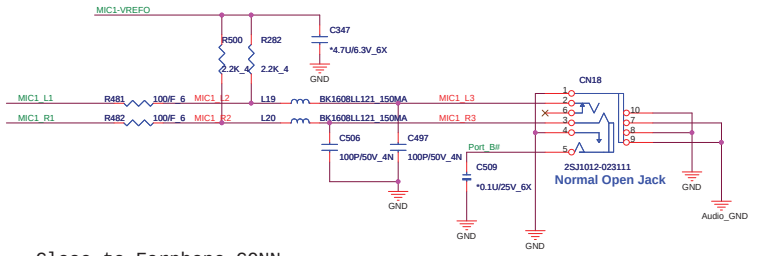
Layout Note: Path from +5V_IC to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms).

Place bypass caps very close to device.

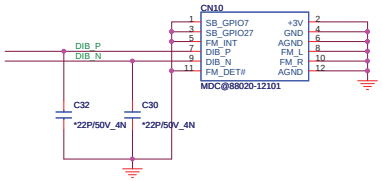
Earphone



External MIC



MDC



Quanta Computer Inc.			
PROJECT : TE2			
Size	Document Number: Codec (CX20583)		Rev: 2A
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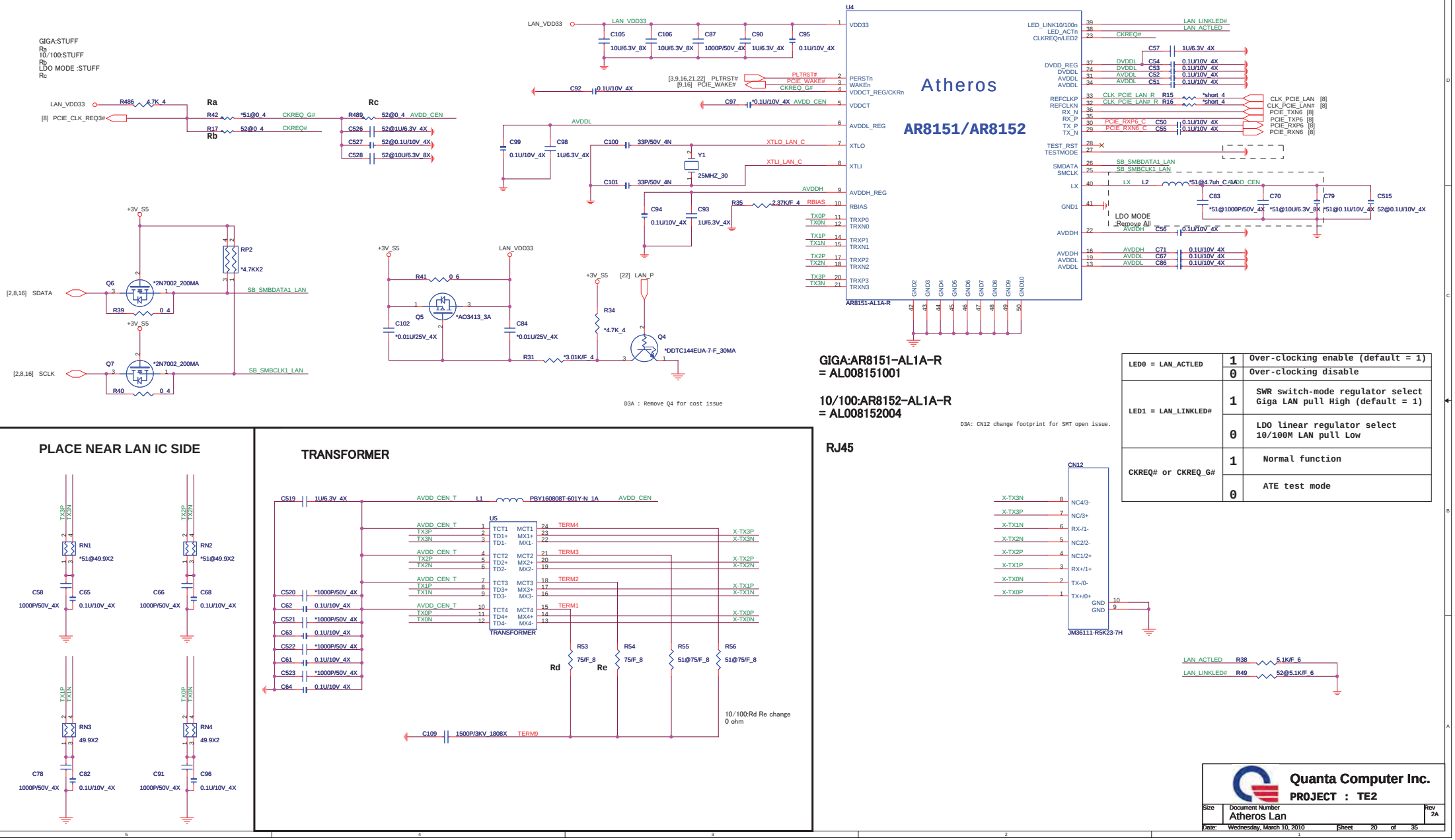
Atheros Lan



GIGA:AR8151-AL1A-R
= AL008151001

10/100:AR8152-AL1A-R
= AL008152004

D3A: CN12 change footprint for SMT open issue.

RJ45

LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

PLACE NEAR LAN IC SIDE

TRANSFORMER

Quanta Computer Inc.				
PROJECT : TE2				
Size	Document Number			Rev
	Atheros Lan			2A
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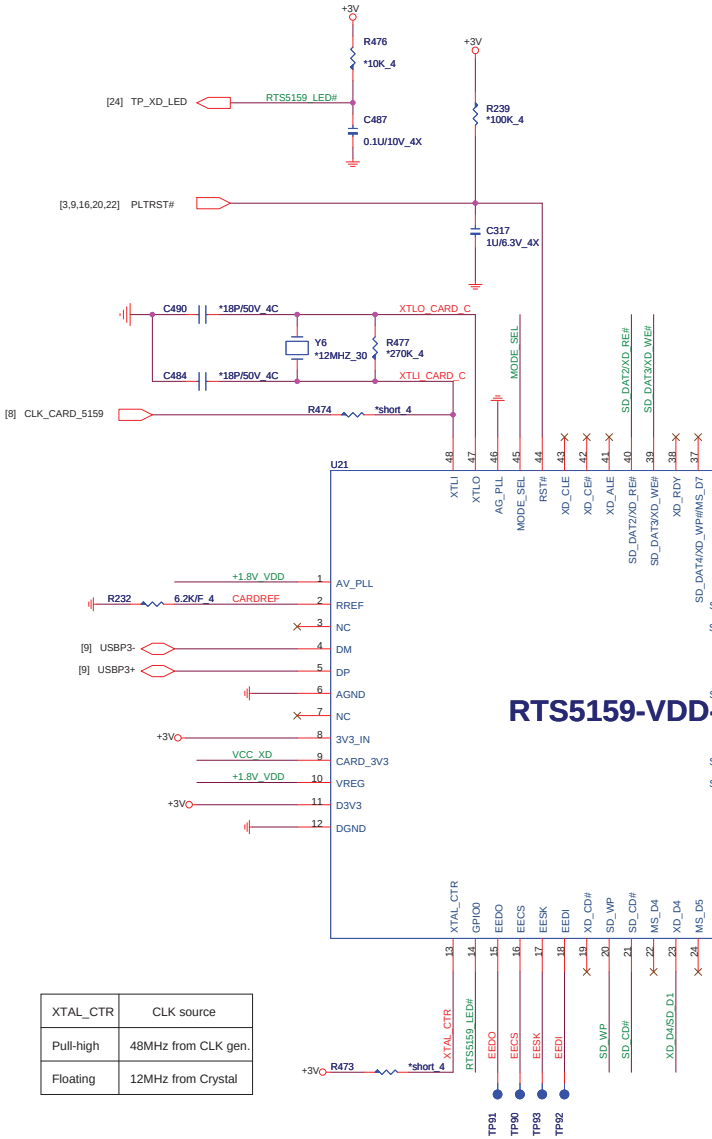
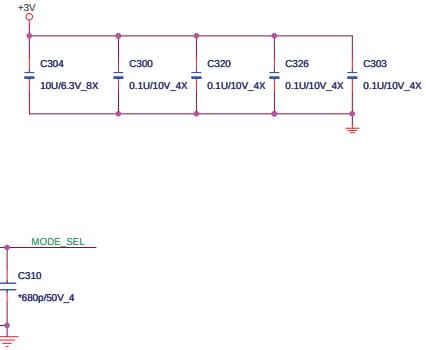
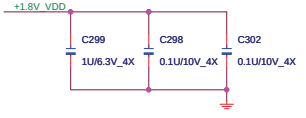
3 IN 1 CARD READER



XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal

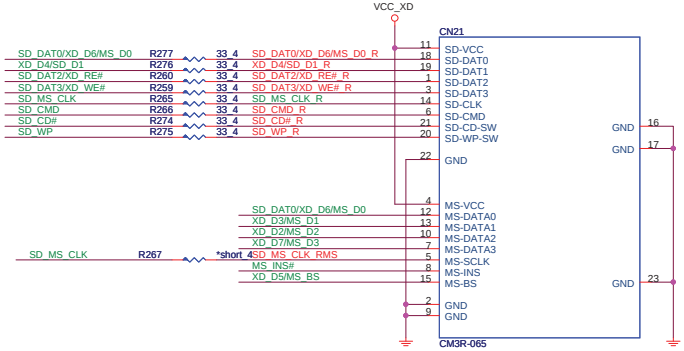


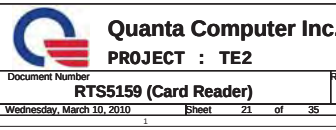


MODE_SEL (Please refer to Realtek Application Notes for more detail description)

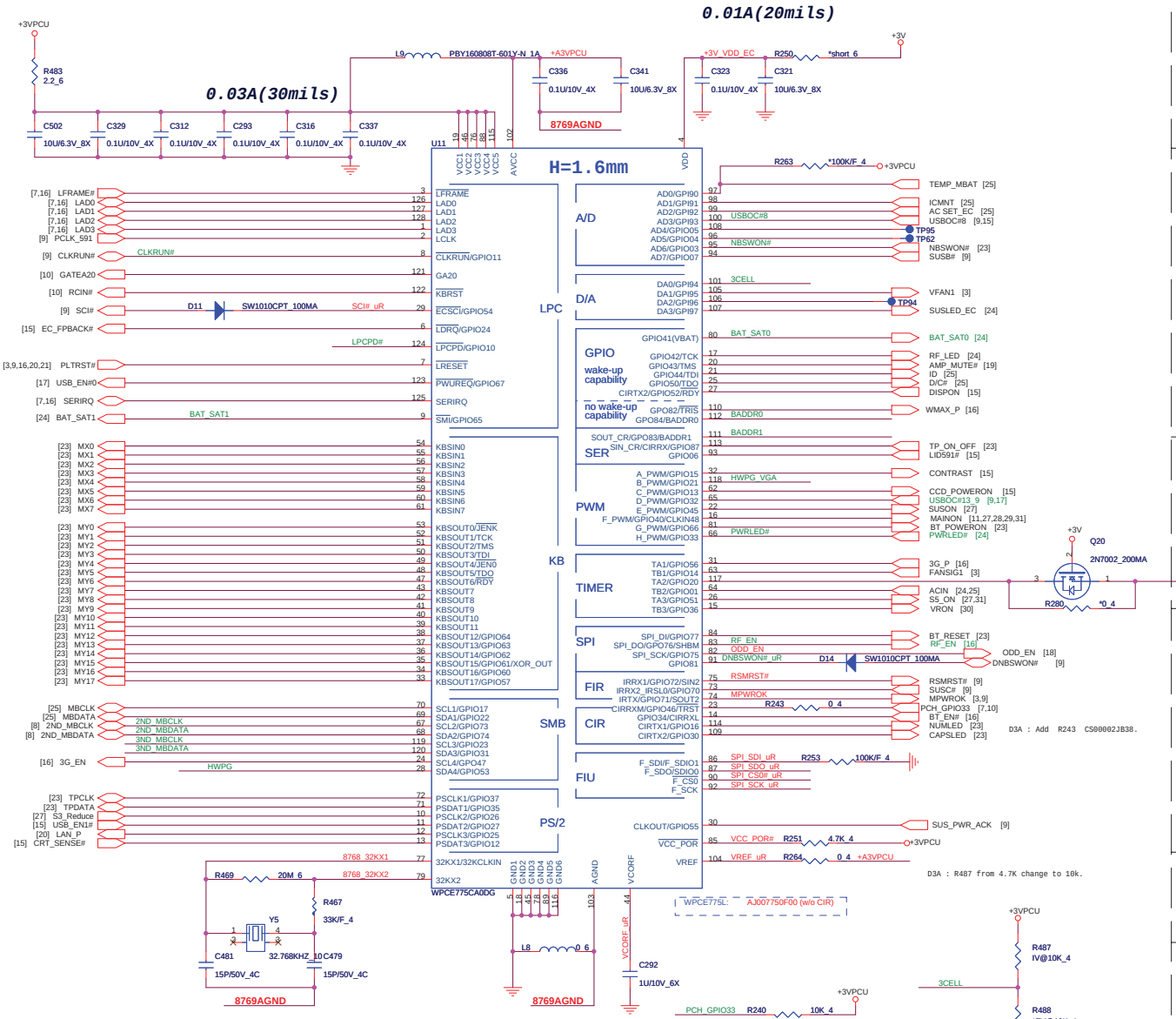
	R49	C73	Power mode
RTS 5159	0-ohm	NC	USB Auto De-link mode:

3 IN 1 CARD READER





EC [KBC]



SMBUS Table

SMBUS	Devices	Address
1	Battery	12H
2	CPU Board Thermal Sensor	
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H

SM BUS PU

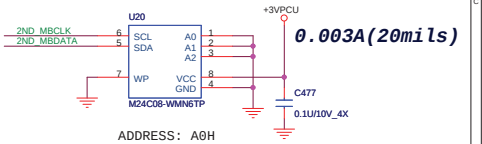
I/O Base Address

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

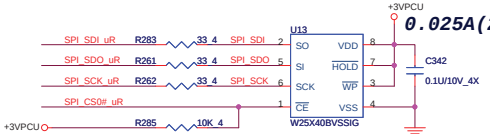
SHBM=0: Enable shared memory with host BIOS

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID



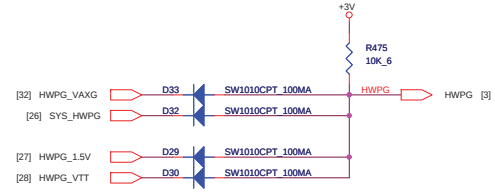
SPI FLASH



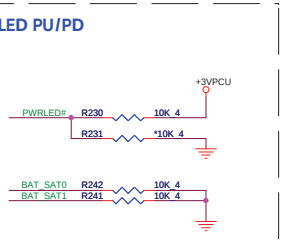
Intel	512KB	W25X40BVSSIG
AMD	2MB	W25Q16BVSSIG

INTERNAL KEYBOARD STRIP SET

HWPG



LED PU/PD



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	EC-WPC8763LDG/WPC8769L(O)	2A

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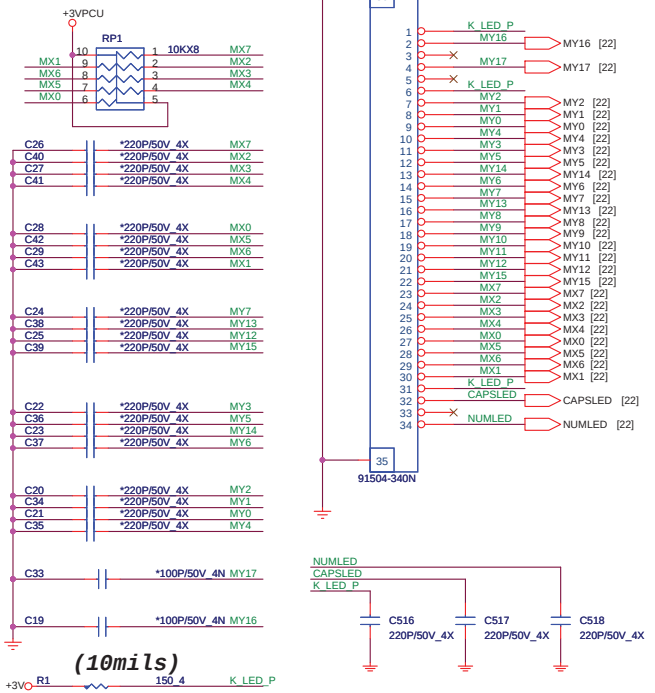
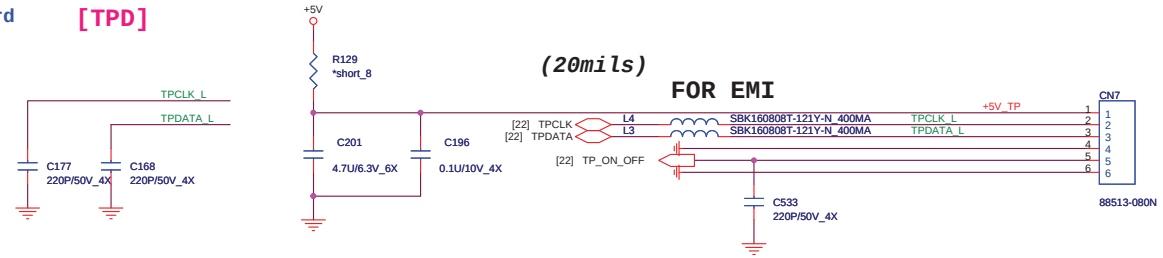
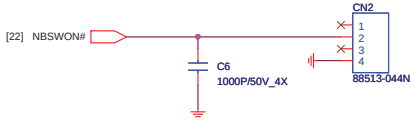
INT KeyBoard [KBC]



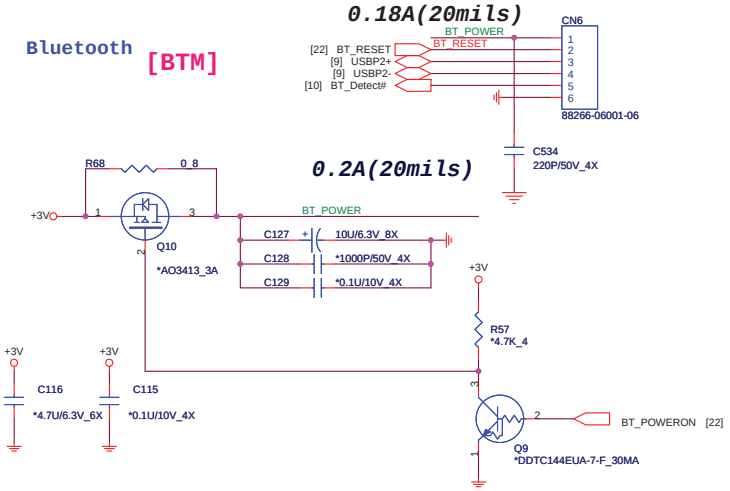
TP board [TPD]



Power board [PSW]

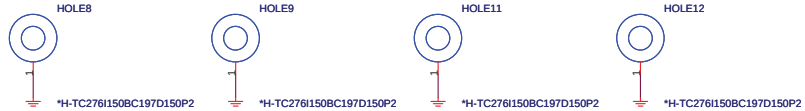


Bluetooth [BTM]

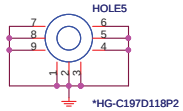


HOLE

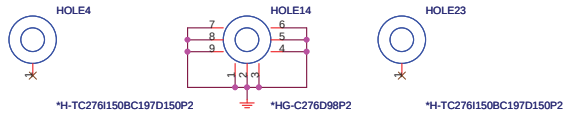
CPU



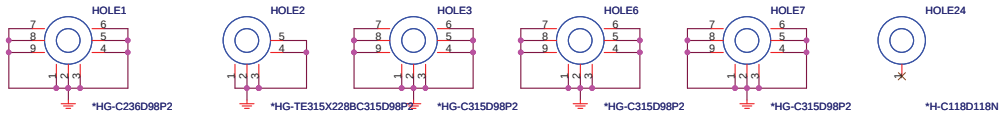
MDC

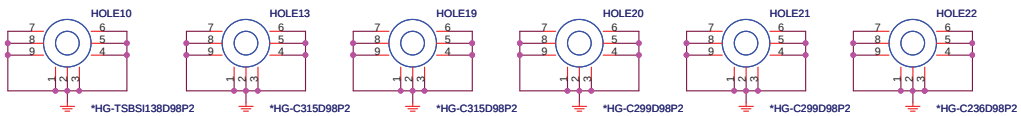


MINI CARD



HDD&ODD





Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	KB/TP&TP/PB/FL/LEB/MMB/B-CAS	2A

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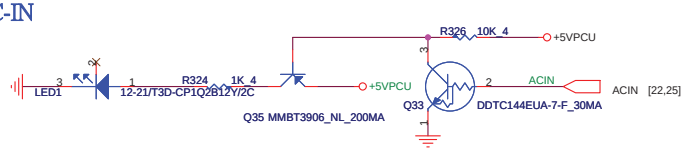
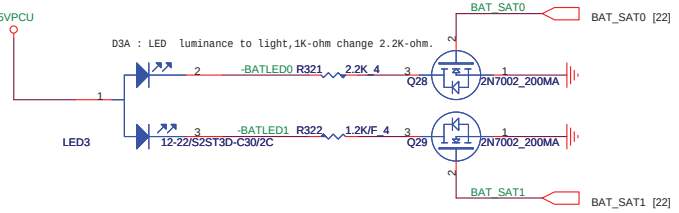
LED [LED]

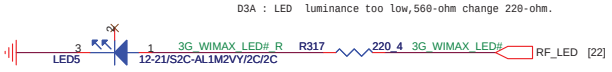
AC-IN



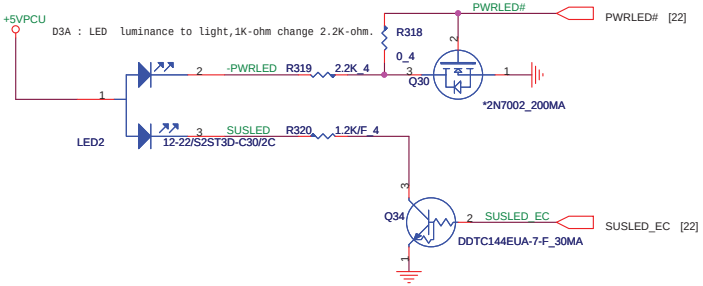
BATERRY



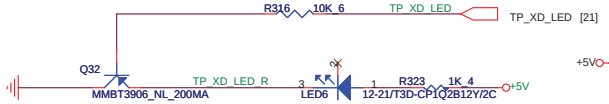
RF LED



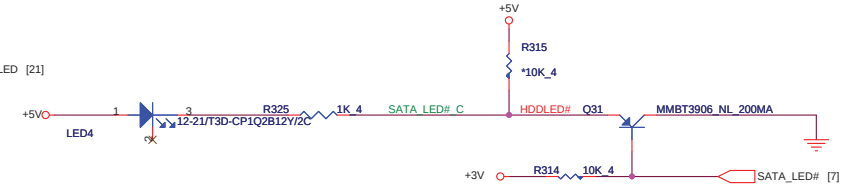
POWER



CARDREADER

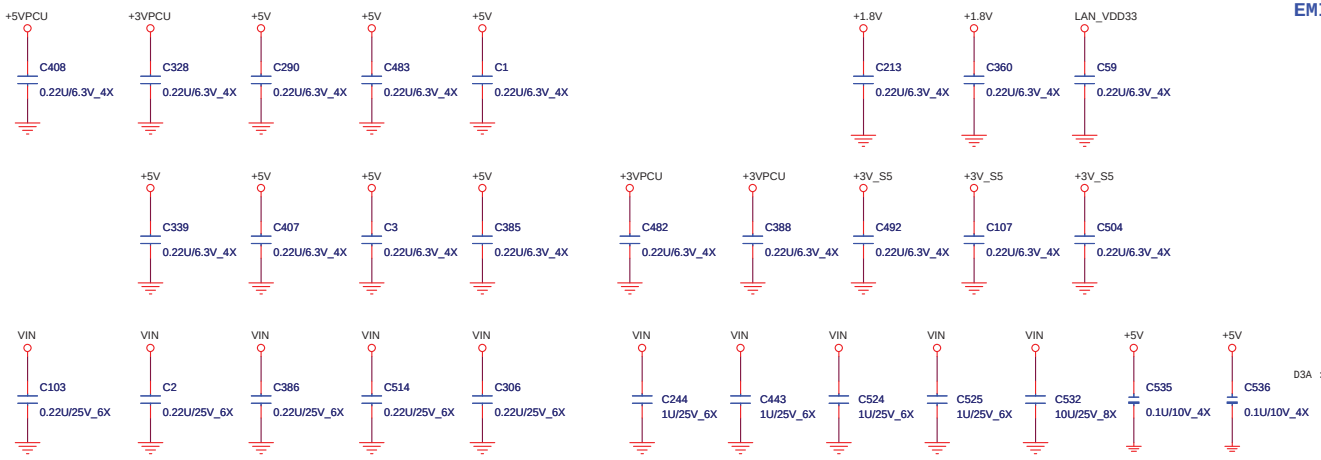


HDD/ODD

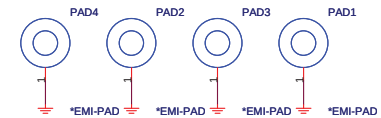


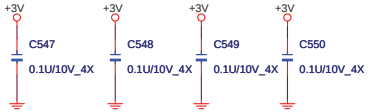
ESD Protect

EMI



EMI PAD





D3A : Add C547,C548,C549,C550 0.1u Cap for EMI issue.

Quanta Computer Inc.
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	LED/HOLE	2A

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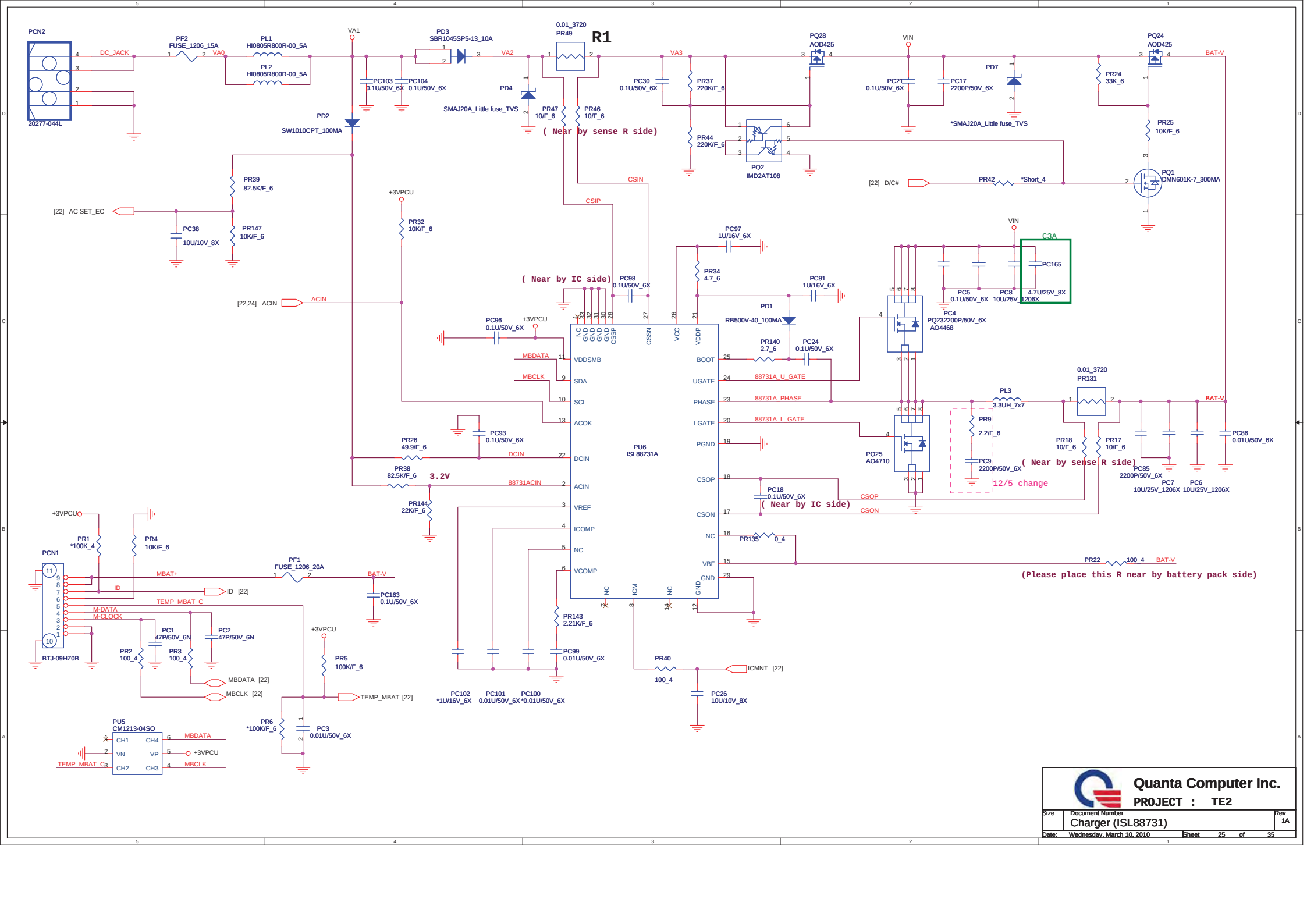

Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: Charger (ISL88731)	Rev: 1A
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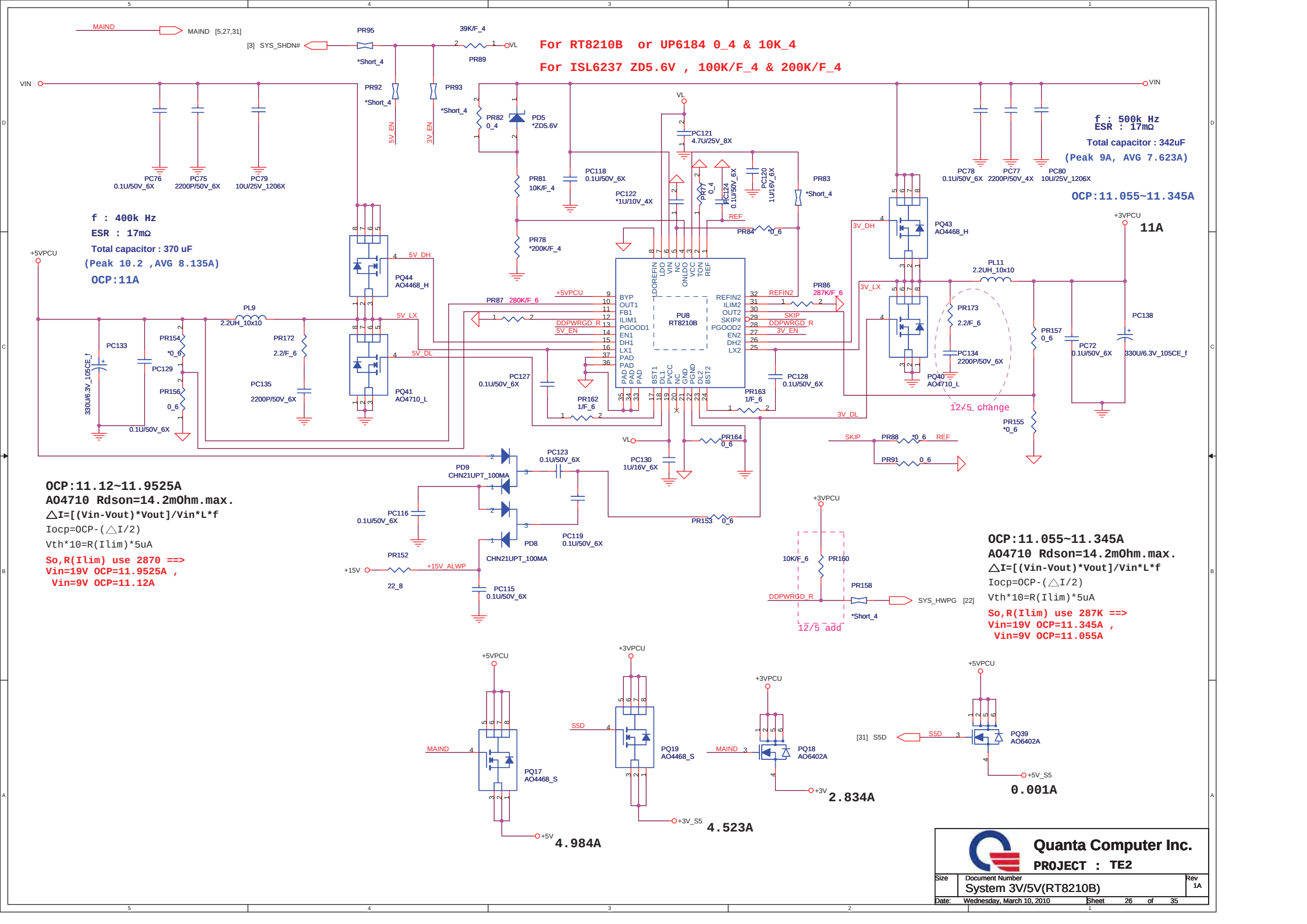
For RT8210B or UP6184 0_4 & 10K_4
For ISL6237 ZD5.6V , 100K/F_4 & 200K/F_4
f : 500k Hz
ESR : 17mΩ
Total capacitor : 342uF
(Peak 9A, AVG 7.623A)
OCP:11.055~11.345A
f : 400k Hz
ESR : 17mΩ
Total capacitor : 370 uF
(Peak 10.2 ,AVG 8.135A)
OCP:11A
11A
OCP:11.12~11.9525A
AO4710 Rdson=14.2mOhm.max.
△I=[(Vin-Vout)*Vout]/Vin*L*f
Iocp=OCP-(△I/2)
Vth*10=R(Ilim)*5uA
So,R(Ilim) use 2870 ==>
Vin=19V OCP=11.9525A ,
Vin=9V OCP=11.12A
OCP:11.055~11.345A
AO4710 Rdson=14.2mOhm.max.
△I=[(Vin-Vout)*Vout]/Vin*L*f
Iocp=OCP-(△I/2)
Vth*10=R(Ilim)*5uA
So,R(Ilim) use 287K ==>
Vin=19V OCP=11.345A ,
Vin=9V OCP=11.055A
12/5 change
12/5 add
4.984A
4.523A
2.834A
0.001A
PU8 RT8210B
PQ17 AO4468_S
PQ19 AO4468_S
PQ18 AO6402A
PQ39 AO6402A
PQ40 AO4710_L
PQ41 AO4710_L
PQ43 AO4468_H
PQ44 AO4468_H
PD5 *ZD5.6V
PD8 CHN21UPT_100MA
PD9 CHN21UPT_100MA
PL9 2.2UH_10x10
PL11 2.2UH_10x10
Quanta Computer Inc.
PROJECT : TE2
Size
Document Number
System 3V/5V(RT8210B)
Rev 1A
Date: Wednesday, March 10, 2010
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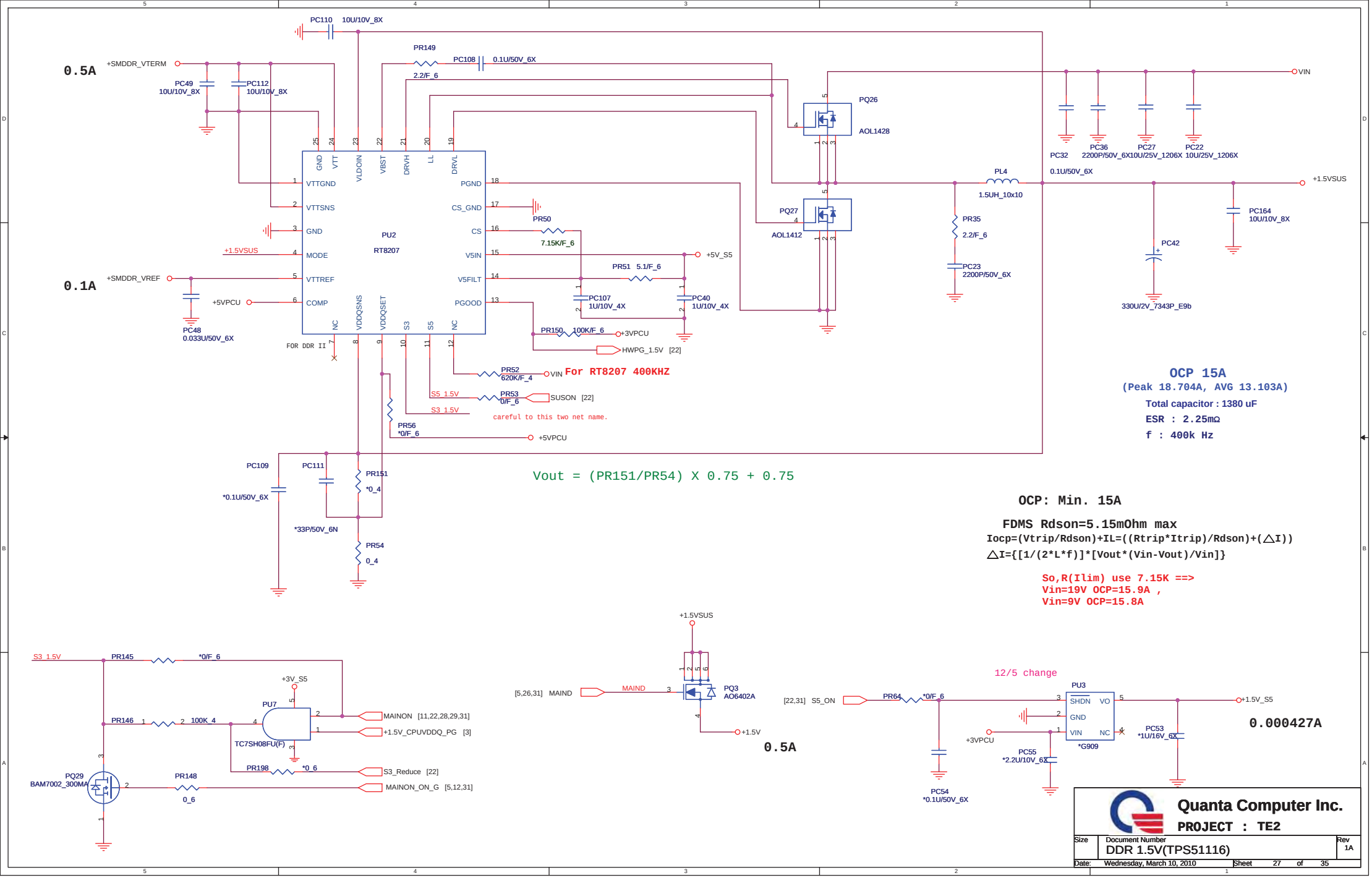
0.5A
0.1A
PU2
RT8207
PC110 10U/10V_8X
PR149
PC108 0.1U/50V_6X
2.2/F_6
+SMDDR_VTERM
PC49 10U/10V_8X
PC112 10U/10V_8X
+SMDDR_VREF
+5VPCU
PC48 0.033U/50V_6X
+1.5VSUS
PR50
7.15K/F_6
PR51 5.1/F_6
+5V_S5
PC107 1U/10V_4X
PC40 1U/10V_4X
PR150 100K/F_6
+3VPCU
HWPG_1.5V [22]
PR52 620K/F_4
VIN
For RT8207 400KHZ
S5_1.5V
PR53 0/F_6
SUSON [22]
S3_1.5V
careful to this two net name.
PR56 *0/F_6
+5VPCU
FOR DDR II
PQ26
AOL1428
PQ27
AOL1412
PL4
1.5UH_10x10
0.1U/50V_6X
+1.5VSUS
PR35
2.2/F_6
PC23 2200P/50V_6X
PC32
PC36 2200P/50V_6X
PC27 10U/25V_1206X
PC22 10U/25V_1206X
PC164 10U/10V_8X
PC42
330U/2V_7343P_E9b
OCP 15A
(Peak 18.704A, AVG 13.103A)
Total capacitor : 1380 uF
ESR : 2.25mΩ
f : 400k Hz
Vout = (PR151/PR54) X 0.75 + 0.75
PC109
*0.1U/50V_6X
PC111
*33P/50V_6N
PR151
*0_4
PR54
0_4
OCP: Min. 15A
FDMS Rdson=5.15mOhm max
Iocp=(Vtrip/Rdson)+IL=((Rtrip*Itrip)/Rdson)+(△I))
△I={[1/(2*L*f)]*[Vout*(Vin-Vout)/Vin]}
So,R(Ilim) use 7.15K ==>
Vin=19V OCP=15.9A ,
Vin=9V OCP=15.8A
S3_1.5V
PR145
*0/F_6
+3V_S5
PU7
TC7SH08FU(F)
PR146
100K_4
MAINON [11,22,28,29,31]
+1.5V_CPUVDDQ_PG [3]
PR198
*0_6
S3_Reduce [22]
PQ29
BAM7002_300MA
PR148
0_6
MAINON_ON_G [5,12,31]
+1.5VSUS
[5,26,31] MAIND
MAIND
PQ3
AO6402A
+1.5V
0.5A
12/5 change
[22,31] S5_ON
PR64
*0/F_6
PU3
SHDN
VO
GND
VIN
NC
*G909
+3VPCU
PC55
*2.2U/10V_6X
PC54
*0.1U/50V_6X
PC53
*1U/16V_6X
+1.5V_S5
0.000427A
Quanta Computer Inc.
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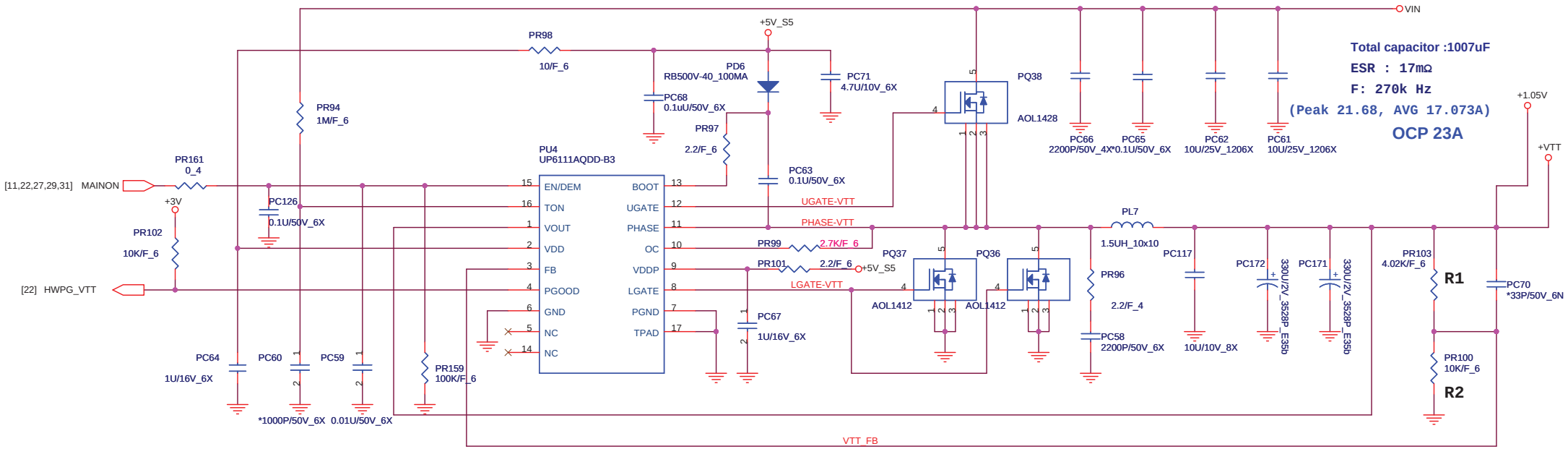
PC63 X V



VOUT=(1+R1/R2)*0.75

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

OCP:23.18~23.27A

FDMS0310 Rdson=5.15mOhm max

Iocp=(Vtrip/Rdson)+IL=((Rtrip*Itrip)/Rdson)+(△I))

△I={[1/(2*L*f)]*[Vout*(Vin-Vout)/Vin]}

Rdson*OCP=RIlim*20uA

So,R(Ilim) use 2.7K ==>

Vin=19V OCP=23.18A ,

Vin=9V OCP=23.27A

Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	+VTT (UP6111A)	1A
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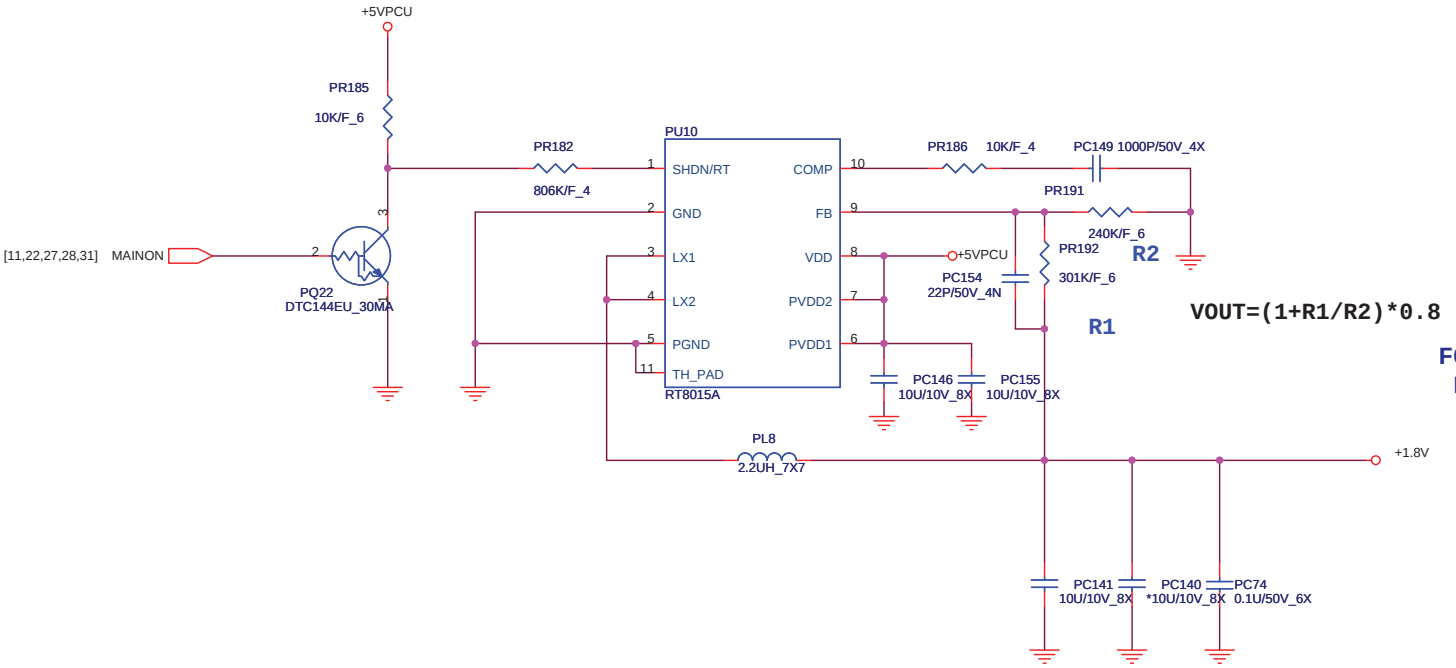

VOUT=(1+R1/R2)*0.8

OCP Fellow IC spec~3.7A

FOR UMA 0.194A
For VGA 1.345A

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Size	Document Number	Rev
	+1.8V (RT8015A)	1A

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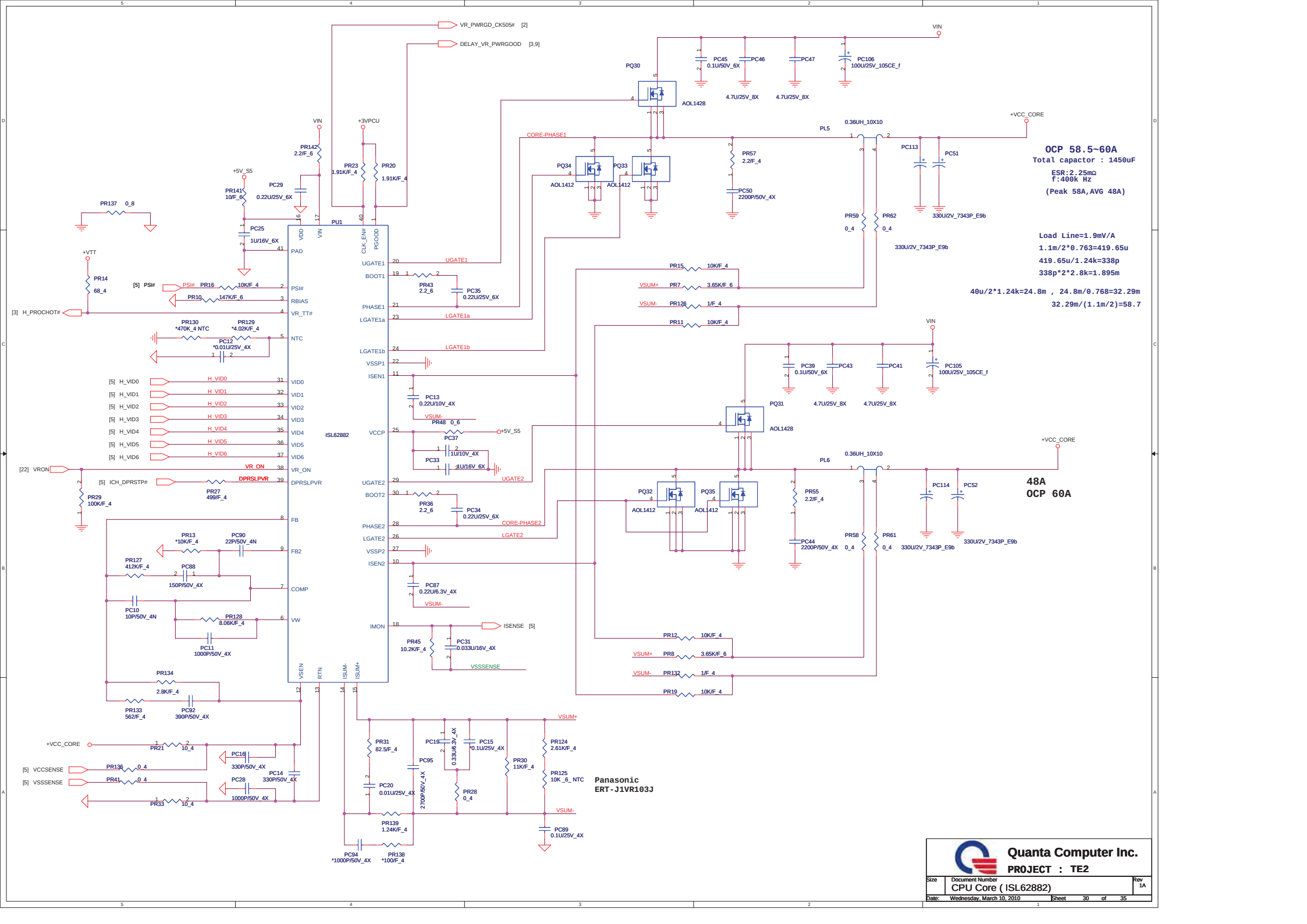
VR_PWRGD_CK505# [2]
DELAY_VR_PWRGOOD [3,9]
VIN
+3VPCU
+5V_S5
PU1
ISL62882
PR142 2.2/F_6
PR23 1.91K/F_4
PR20 1.91K/F_4
PR141 10/F_6
PC29 0.22U/25V_6X
PR137 0_8
PC25 1U/16V_6X
+VTT
PR14 68_4
[5] PSI#
PSI# PR16 10K/F_4
PR10 147K/F_6
[3] H_PROCHOT#
PR130 *470K_4 NTC
PR129 *4.02K/F_4
PC12 *0.01U/25V_4X
[5] H_VID0
[5] H_VID1
[5] H_VID2
[5] H_VID3
[5] H_VID4
[5] H_VID5
[5] H_VID6
[22] VRON
VR_ON
[5] ICH_DPRSTP#
DPRSLPVR
PR27 499/F_4
PR29 100K/F_4
PR13 *10K/F_4
PC90 22P/50V_4N
PR127 412K/F_4
PC88 150P/50V_4X
PC10 10P/50V_4N
PR128 8.06K/F_4
PC11 1000P/50V_4X
PR134 2.8K/F_4
PR133 562/F_4
PC92 390P/50V_4X
+VCC_CORE
PR21 10_4
PC16 330P/50V_4X
[5] VCCSENSE
PR136 0_4
PC14 330P/50V_4X
[5] VSSSENSE
PR41 0_4
PC28 1000P/50V_4X
PR33 10_4
VDD
VIN
CLK_EN#
PGOOD
PAD
UGATE1
BOOT1
PHASE1
LGATE1a
LGATE1b
VSSP1
ISEN1
VCCP
UGATE2
BOOT2
PHASE2
LGATE2
VSSP2
ISEN2
IMON
PSI#
RBIAS
VR_TT#
NTC
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VR_ON
DPRSLPVR
FB
FB2
COMP
VW
VSEN
RTN
ISUM-
ISUM+
UGATE1
LGATE1a
LGATE1b
UGATE2
LGATE2
CORE-PHASE1
CORE-PHASE2
PR43 2.2_6
PC35 0.22U/25V_6X
PC13 0.22U/10V_4X
VSUM-
PR48 0_6
PC37 1U/10V_4X
PC33 1U/16V_6X
PR36 2.2_6
PC34 0.22U/25V_6X
PC87 0.22U/6.3V_4X
PR45 10.2K/F_4
PC31 0.033U/16V_4X
ISENSE [5]
VSSSENSE
PR31 82.5/F_4
PC19 0.33U/6.3V_4X
PC15 *0.1U/25V_4X
PC95 2700P/50V_4X
PC20 0.01U/25V_4X
PR28 0_4
PR30 11K/F_4
PR124 2.61K/F_4
PR125 10K_6_NTC
PR139 1.24K/F_4
PC94 *1000P/50V_4X
PR138 *100/F_4
PC89 0.1U/25V_4X
VSUM+
PQ30
PQ34
PQ33
AOL1412
PC45 0.1U/50V_6X
PC46
PC47
4.7U/25V_8X
PC106 100U/25V_105CE_f
PL5 0.36UH_10X10
PR57 2.2/F_4
PC50 2200P/50V_4X
PR59 0_4
PR62 0_4
PC113
PC51
330U/2V_7343P_E9b
PR15 10K/F_4
PR7 3.65K/F_6
PR126 1/F_4
PR11 10K/F_4
PC39 0.1U/50V_6X
PC43
PC41
PC105 100U/25V_105CE_f
PQ31
PQ32
PQ35
PL6 0.36UH_10X10
PR55 2.2/F_4
PC44 2200P/50V_4X
PR58 0_4
PR61 0_4
PC114
PC52
PR12 10K/F_4
PR8 3.65K/F_6
PR132 1/F_4
PR19 10K/F_4
OCP 58.5~60A
Total capactor : 1450uF
ESR:2.25mΩ
f:400k Hz
(Peak 58A,AVG 48A)
Load Line=1.9mV/A
1.1m/2*0.763=419.65u
419.65u/1.24k=338p
338p*2*2.8k=1.895m
40u/2*1.24k=24.8m , 24.8m/0.768=32.29m
32.29m/(1.1m/2)=58.7
48A
OCP 60A
Panasonic
ERT-J1VR103J
Quanta Computer Inc.
PROJECT : TE2
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Document Number
CPU Core (ISL62882)
Rev 1A
Date: Wednesday, March 10, 2010
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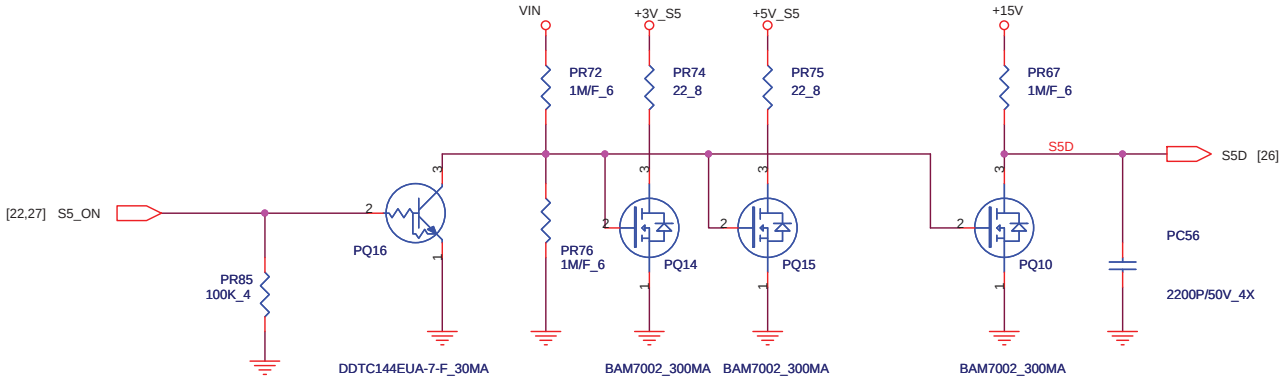

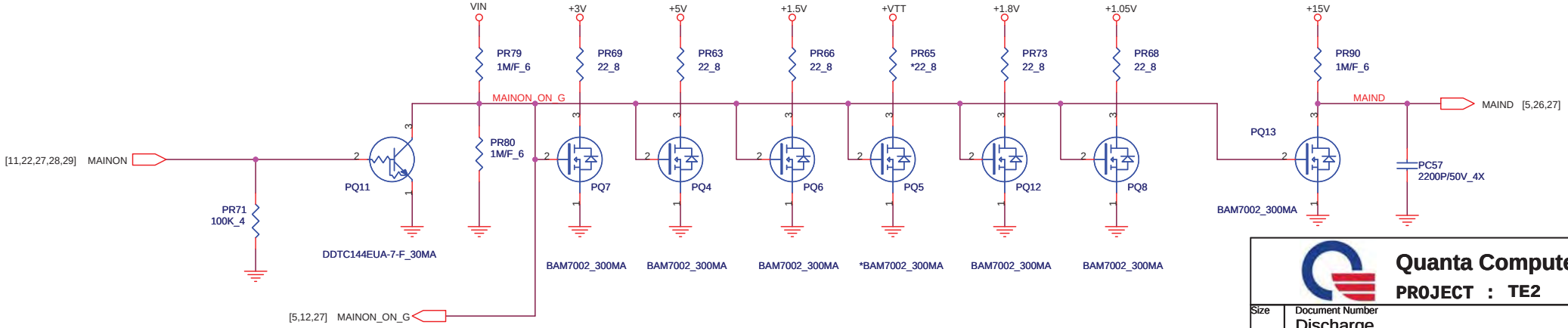

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Size	Document Number	Rev
	Discharge	1A

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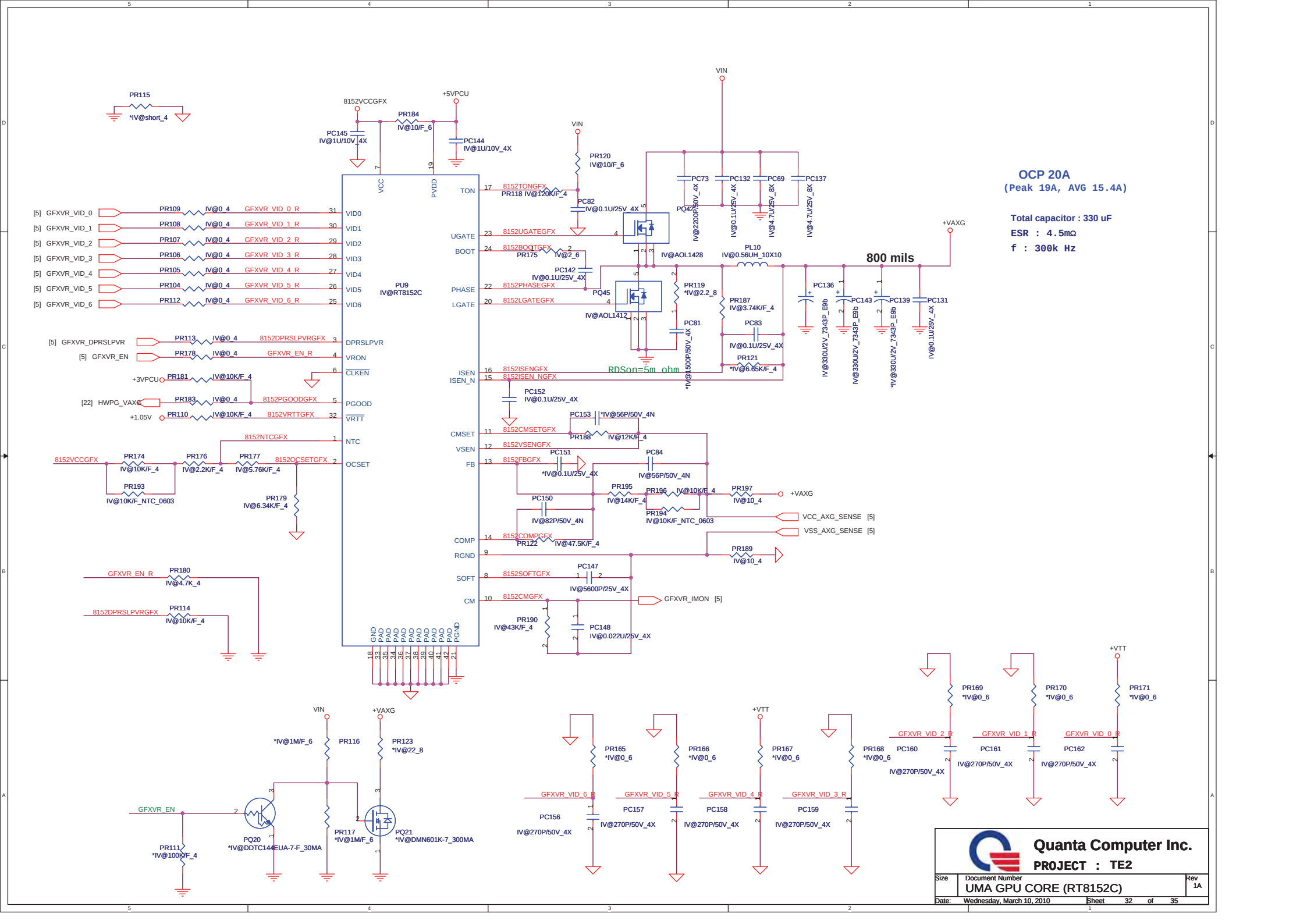
OCP 20A
(Peak 19A, AVG 15.4A)
Total capacitor : 330 uF
ESR : 4.5mΩ
f : 300k Hz
800 mils
RDSon=5m ohm
PU9
IV@RT8152C
Quanta Computer Inc.
PROJECT : TE2
UMA GPU CORE (RT8152C)
Size
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Rev
1A
Date: Wednesday, March 10, 2010
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2	Front Page	
3	Clock Generator	CLK
4-7	Processor	CPU
8-14	PCH	CLG
9	RTC	RTC
15-16	DDRIII SO-DIMM	DDR
17	VGA Connector	VGA
18	LCD Panel	LDS
	CRT & CRT BUS SWITCH	CRT
	CCD	CCD
	HALL SENSOR&BACK LIGHT SWITCH	HSR
19	Display Port	DPP
20	HDMI comm part	HDM
	HDMI for GM	HMG
21	SATA ODD	ODD
	Main SATA HDD & 2nd SATA HDD	HDD
	G-Sensor	H3D
22	5 IN 1 Card reader	MMC
	IEEE1394	FIW
23	MINI Card (Wi-Fi & WIMAX)	WLN
	MINI Card 2nd	MNC
	MINI Card 3nd	MNC
	TMA Connector	TMA
24	INT KeyBoard & K/B LED Power	KBC
	LED Board	LED
	TP&FP board	TPD,FPD
	Bluetooth Connector	BTM
	Felica Connector	FEC
	MMB Connector	MMB
	Power SW	PSW
	B-CAS Connector	BCS
25	New Card (Express Card)	EXC
	E-SATA comb USB	ESA
	USB Connector	USB
	Audio & USB Board	USB,ADO
	Light Sensor	LSN
	Satellite LED	LED
	RF LED / WIMAX LED / Kill SW	KSW
26	EC WP8763LDG/WPC8769L(O)	KBC
	CIR	CIR
27	Codec (CX20583)	ADO
28	FM Tunner	FMM
	Modem Connector	MDM
	HOLE	
29	Atheros LAN	LAN
30	NVRAM Connecyor	NVR
31	Charger (ISL6251A)	PWM
32	System 5V/3V (ISL6237)	PWM
33	CPU CORE (ISL62882)	PWM

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
+5V_TMA	+5V	MAIN_ON	S0
WIMAX_P	+3.3V	WMAX_P for EC	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_S5	+1.5V	S5_ON	S0~S5
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V~+1.1V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		GFXVR_EN	S0

GND PLANE	PAGE
GND_SIGNAL	32
CARD_GND	21
AGND_DC/DC	31
GND	ALL

PAGE	DESCRIPTION	BOI-FUNCTIONS
34	VAXG (ISL62881)	PWM
35	+VTT (UP6111A)	PWM
36	+1.05V (UP6111AQDD)	PWM
37	DDR 1.5V (TPS51116)	PWM
38	Discharge (1.5V_S5/1.8V)	PWM
39	Power Tree Table	
40	PCH Power Plane	
41	Power Management	
42	Change List	

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	POWER STAGE AND BOI-FUNCTION	2A

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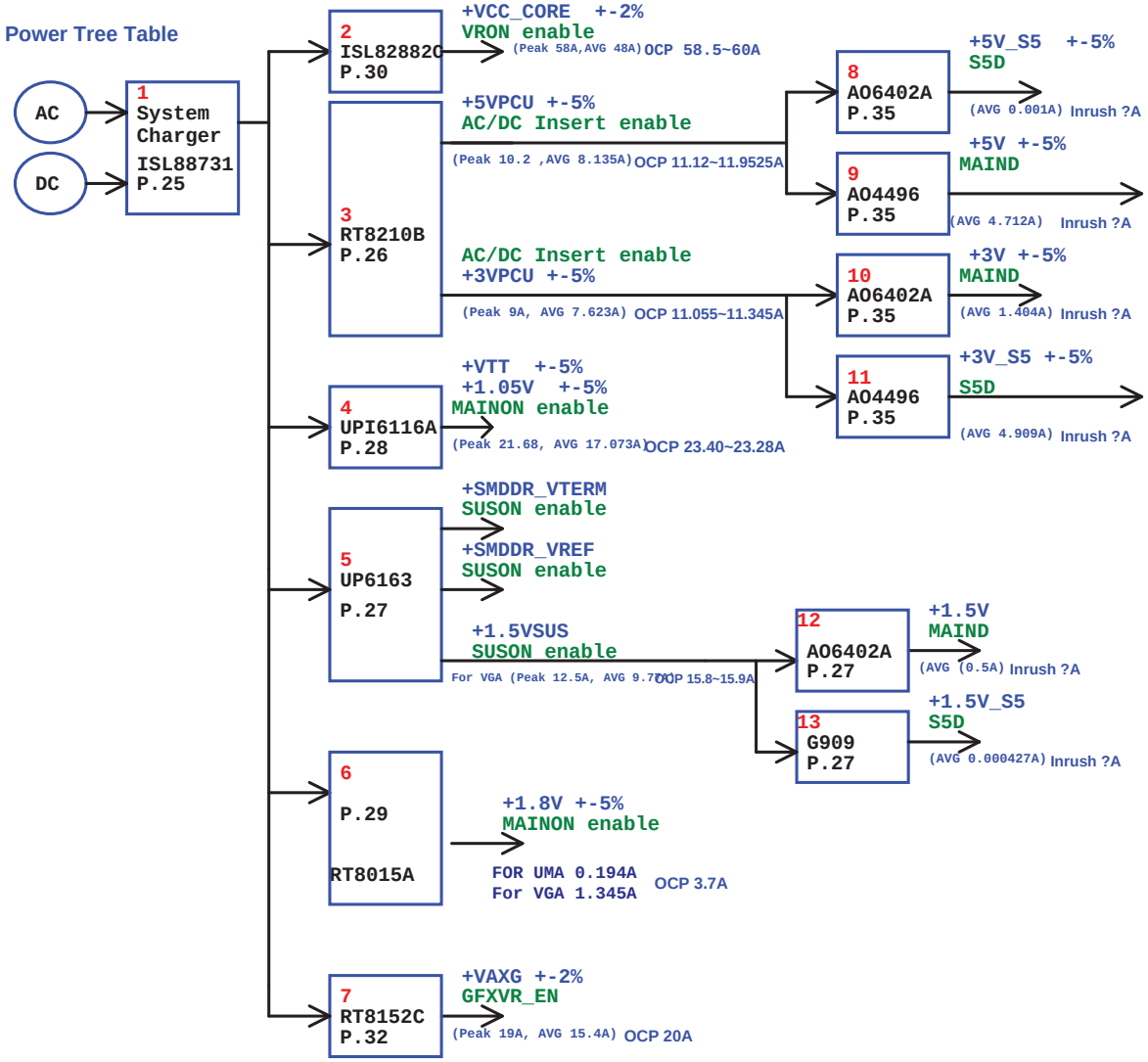
Power Tree Table



Power Distribution List

Power	Distribution

Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	Power Tree Table	2A

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CHANGE LIST

Model	REV	
TE2 MB	B2A	PAGE(16) : Add BT_EN# for combo RF control for BT
		PAGE(27) : Change DDR S3_1.5V ON circuit.
	C3A	PAGE(07) : Add ESATA re-driver IC
	D3A	PAGE(24) : LED luminance to light,R321、R319 1K-ohm change 2.2K-ohm.
		PAGE(24) : LED luminance too low,R317 560-ohm change 220-ohm.
		PAGE(19) : Add R61,R62,R63,R64 0.1-ohm to avoid speaker burn.
		PAGE(16) : Add Q62 to avoid leakage current.

MODEL TE2

PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	