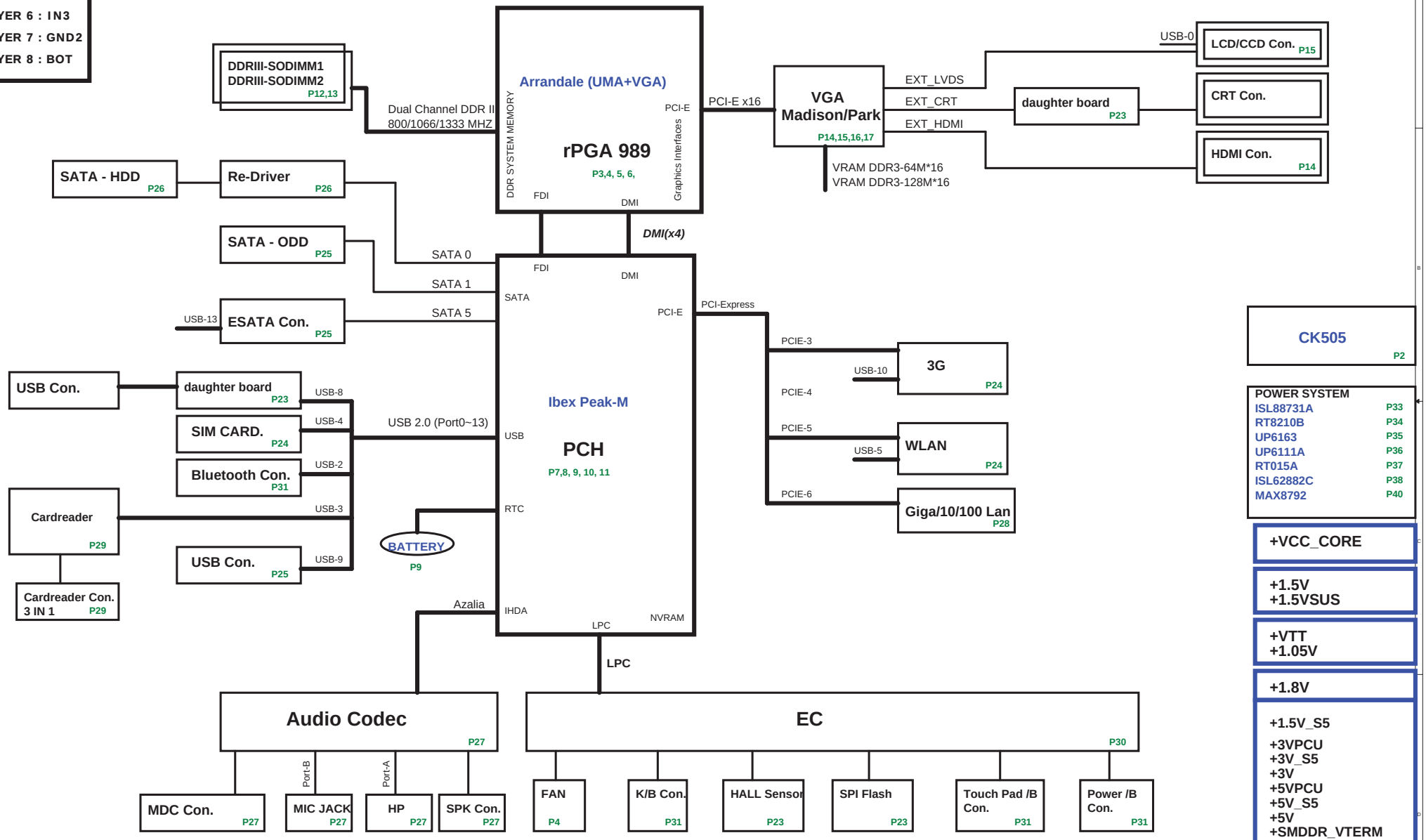
PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND1
- LAYER 3 : IN1
- LAYER 4 : VCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND2
- LAYER 8 : BOT

TE2D Block Diagram



CK505 P2

POWER SYSTEM

ISL88731A	P33
RT8210B	P34
UP6163	P35
UP6111A	P36
RT015A	P37
ISL62882C	P38
MAX8792	P40

+VCC_CORE

+1.5V
+1.5VSUS

+VTT
+1.05V

+1.8V

+1.5V_S5

+3VPCU
+3V_S5
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF

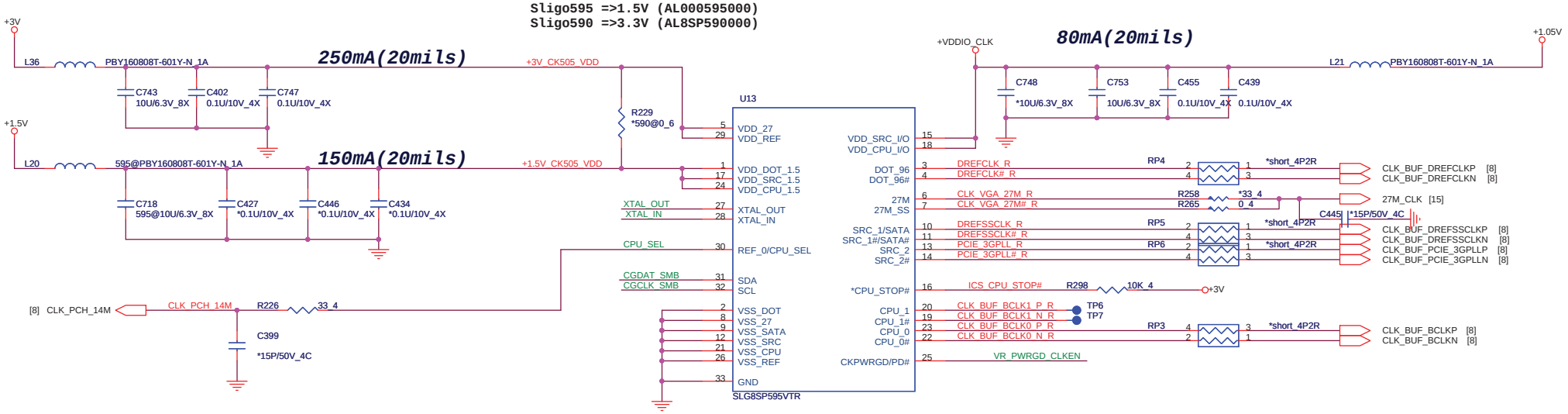
Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	Block Diagram	2A

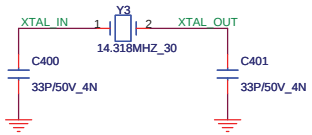
Date: Thursday, February 25, 2010 Sheet 1 of 43

CLOCK Gen [CLK]

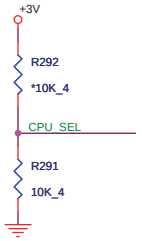
Pin1/17/24
Sligo595 =>1.5V (AL000595000)
Sligo590 =>3.3V (AL8SP590000)



CLK CRYSTAL

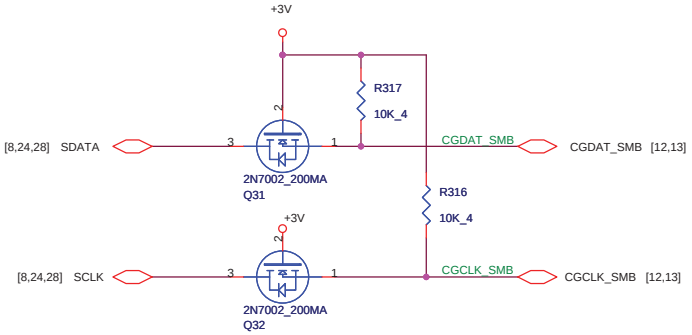


CLK CPU_SEL



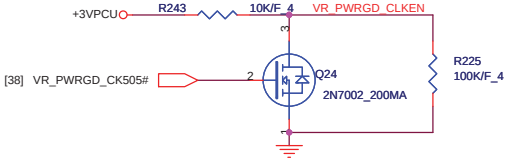
	0	1
CPU_SEL	CPU =133MHz (default)	CPU=100MHz

CLK I2C



CLK POWERGOOD

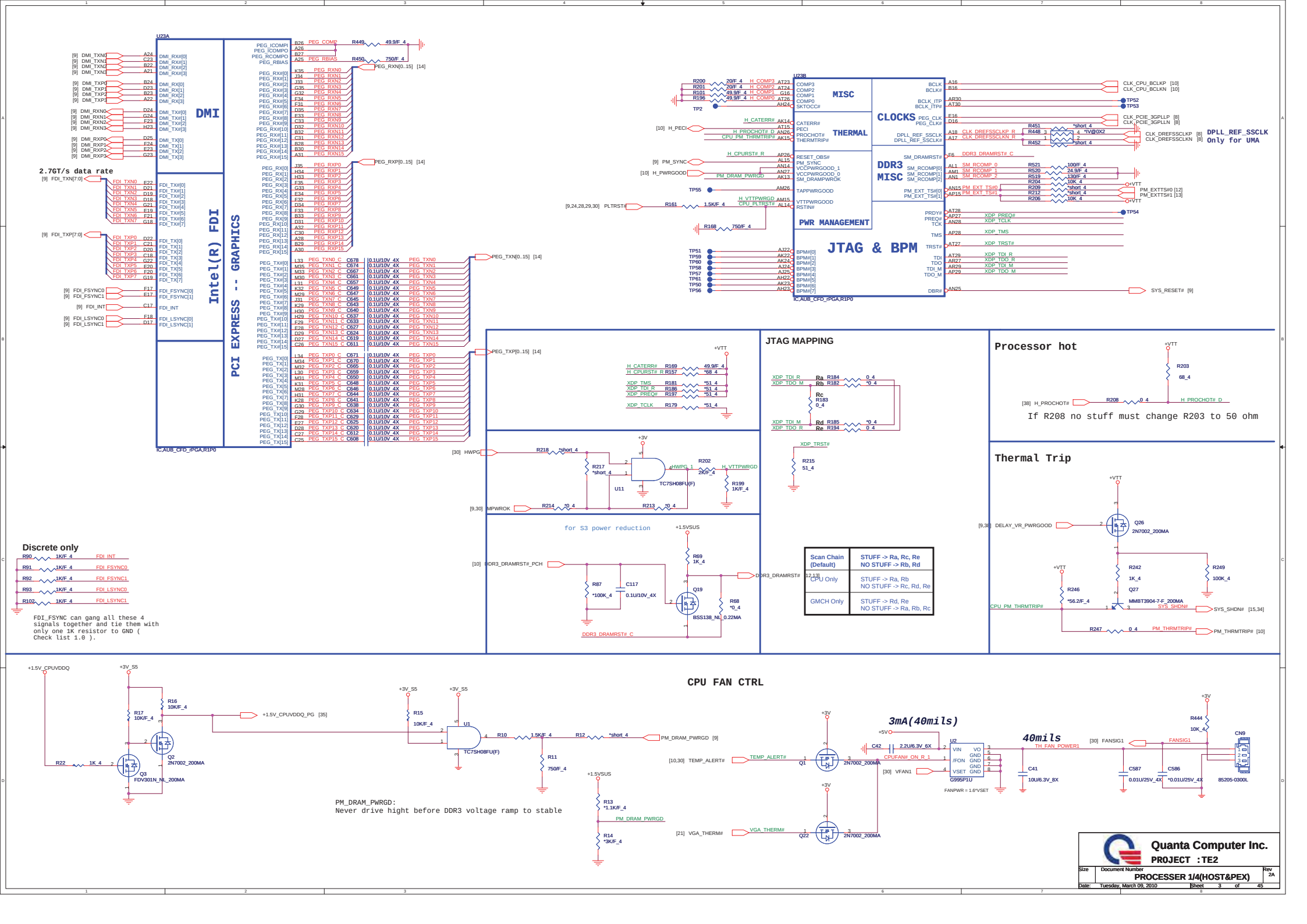
Change to +3VPCU
(follow CRB)



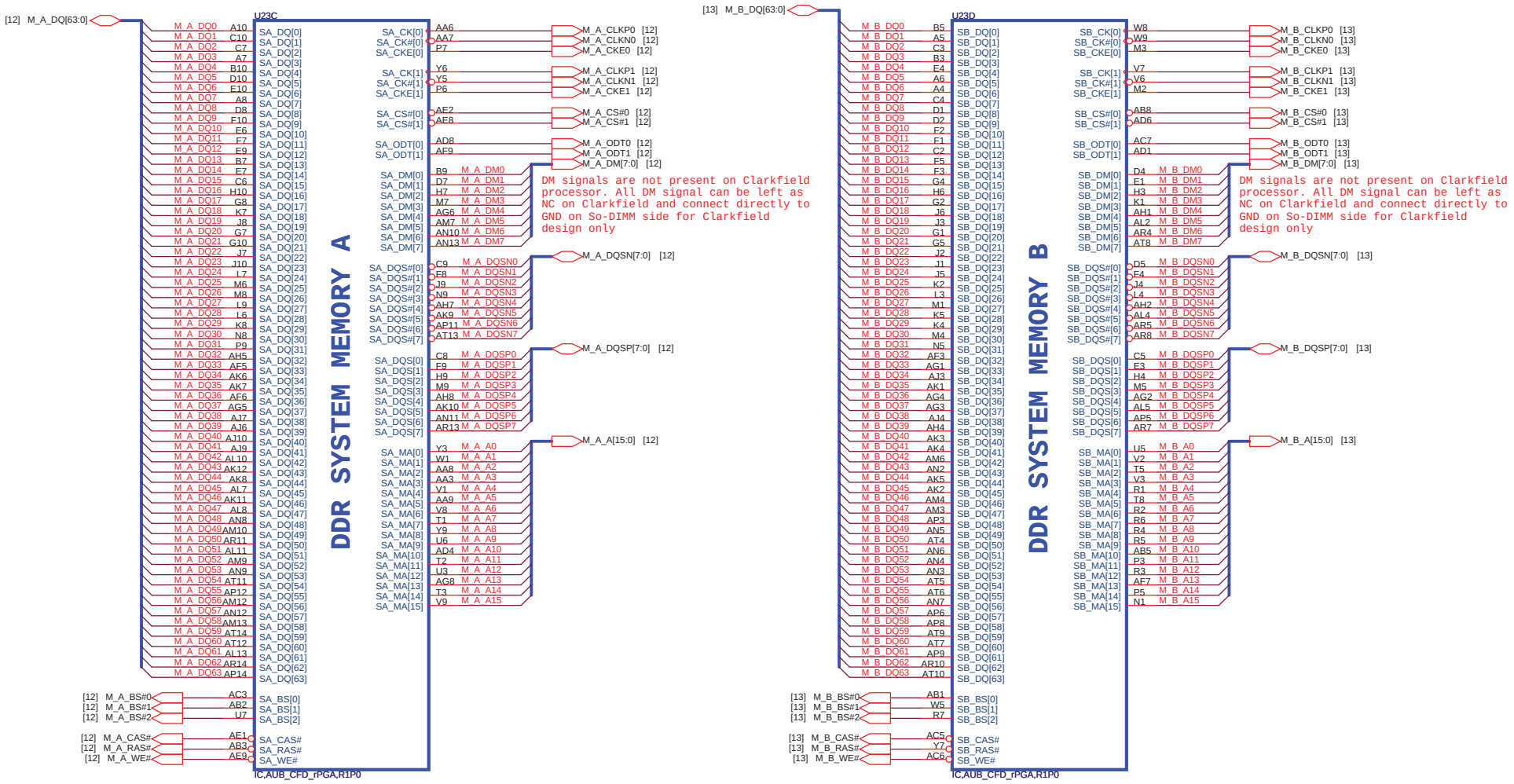
Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	CLOCK GENERATOR	2A

Date: Friday, March 19, 2010 Sheet 2 of 45


DMI
Intel(R) FDI
PCI EXPRESS -- GRAPHICS
MISC
THERMAL
CLOCKS
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
DPLL_REF_SSCLK
Only for UMA
2.7GT/s data rate
JTAG MAPPING
Processor hot
If R208 no stuff must change R203 to 50 ohm
Thermal Trip
Discrete only
FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).
for S3 power reduction
CPU FAN CTRL
3mA(40mils)
40mils
PM_DRAM_PWRGD:
Never drive hight before DDR3 voltage ramp to stable
Scan Chain (Default)
STUFF -> Ra, Rc, Re
NO STUFF -> Rb, Rd
CPU Only
STUFF -> Ra, Rb
NO STUFF -> Rc, Rd, Re
GMCH Only
STUFF -> Rd, Re
NO STUFF -> Ra, Rb, Rc
Quanta Computer Inc.
PROJECT :TE2
PROCESSER 1/4(HOST&PEX)
Tuesday, March 09, 2010
Sheet 3 of 45

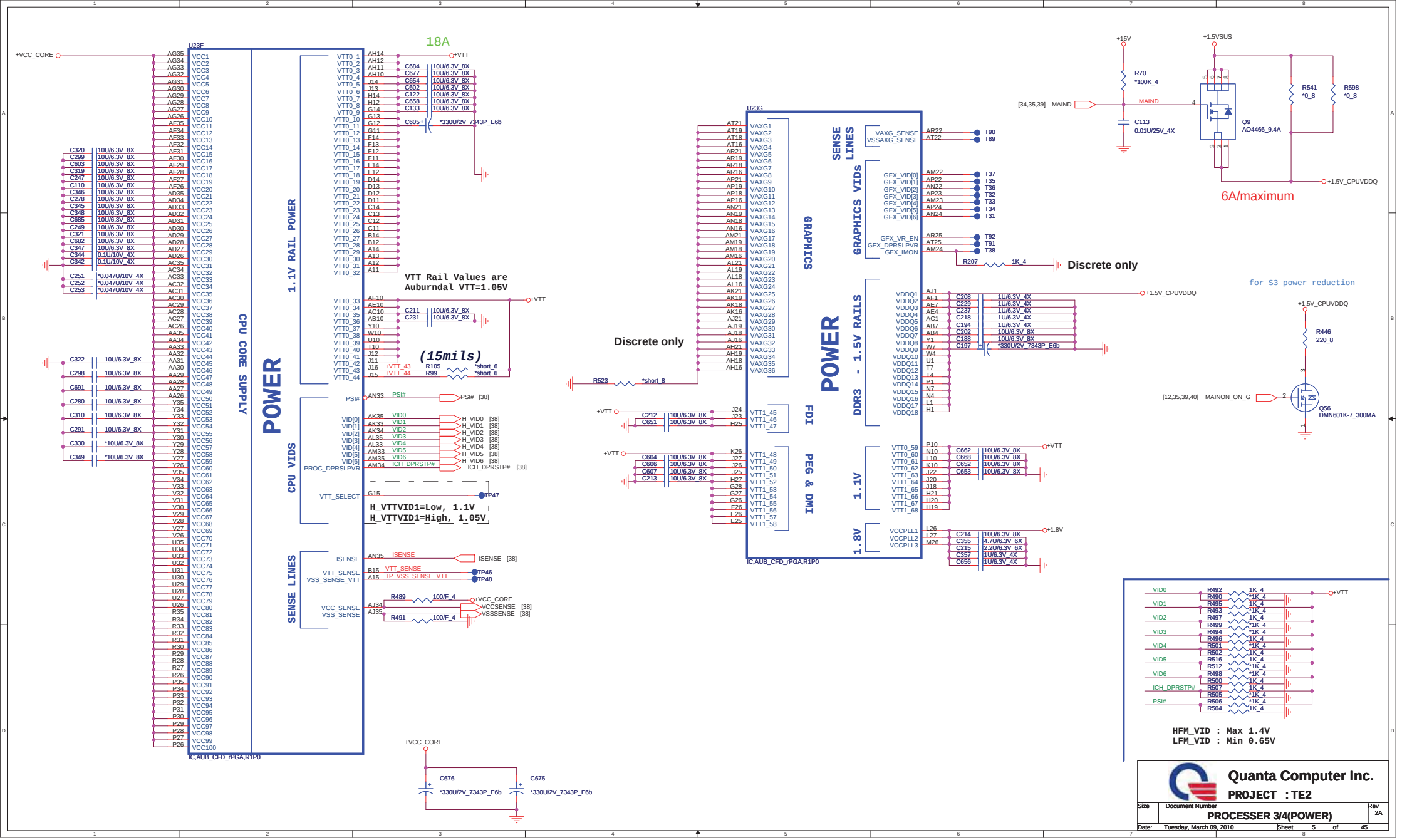
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



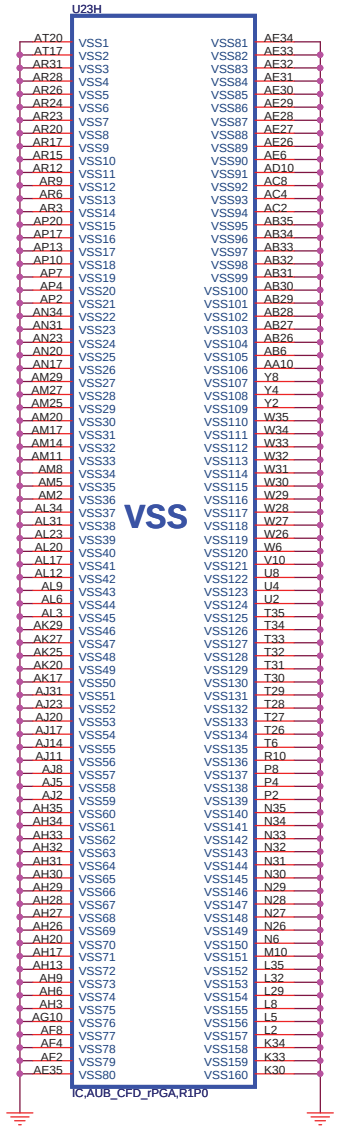
Quanta Computer Inc.

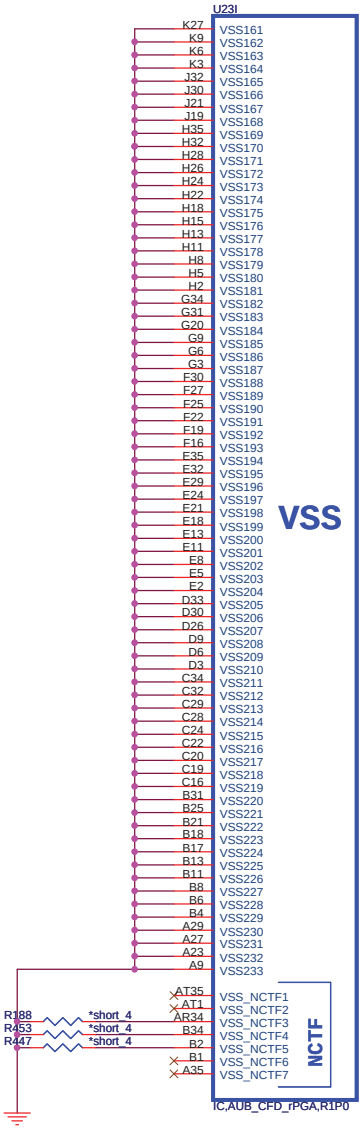
PROJECT : TE2

Size	Document Number	Rev
	PROCESSER 2/4(DDR)	2A
Date: Thursday, February 25, 2010	Sheet 4 of 45	

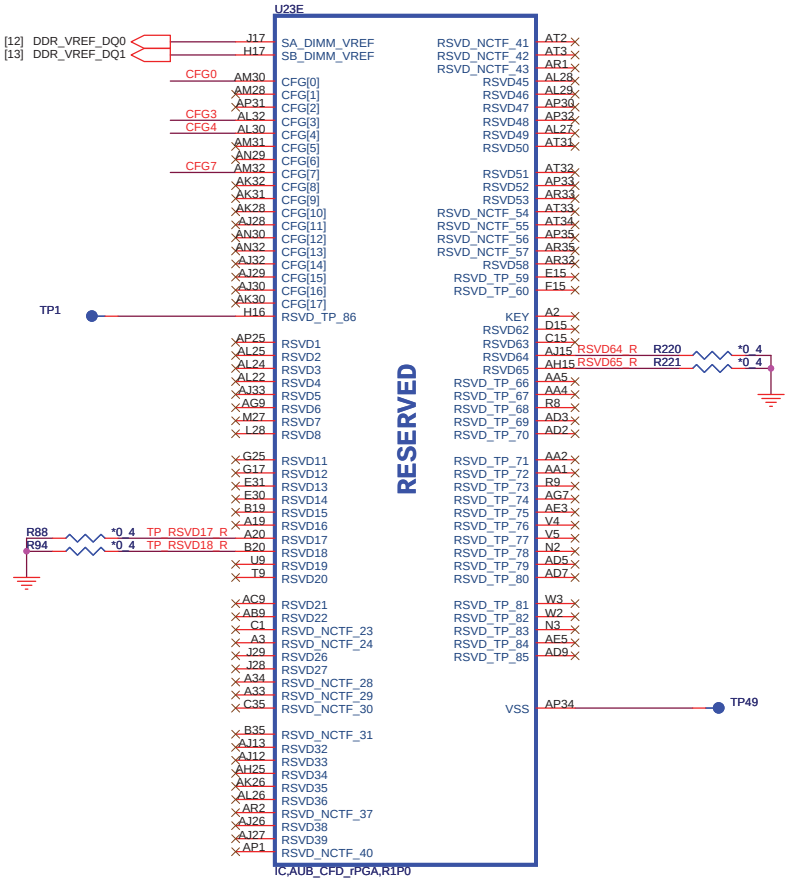

18A
U23F
POWER
CPU CORE SUPPLY
1.1V RAIL POWER
CPU VIDS
SENSE LINES
VTT Rail Values are
Auburndal VTT=1.05V
(15mils)
H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V
IC,AUB_CFD_rPGA,R1P0
U23G
POWER
GRAPHICS
SENSE LINES
GRAPHICS VIDs
DDR3 - 1.5V RAILS
FDI & PEG & DMI
1.1V
1.8V
Discrete only
Discrete only
for S3 power reduction
6A/maximum
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V
Quanta Computer Inc.
PROJECT : TE2
PROCESSER 3/4(POWER)
Tuesday, March 09, 2010
Sheet 5 of 45

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)





AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

For Discrete only

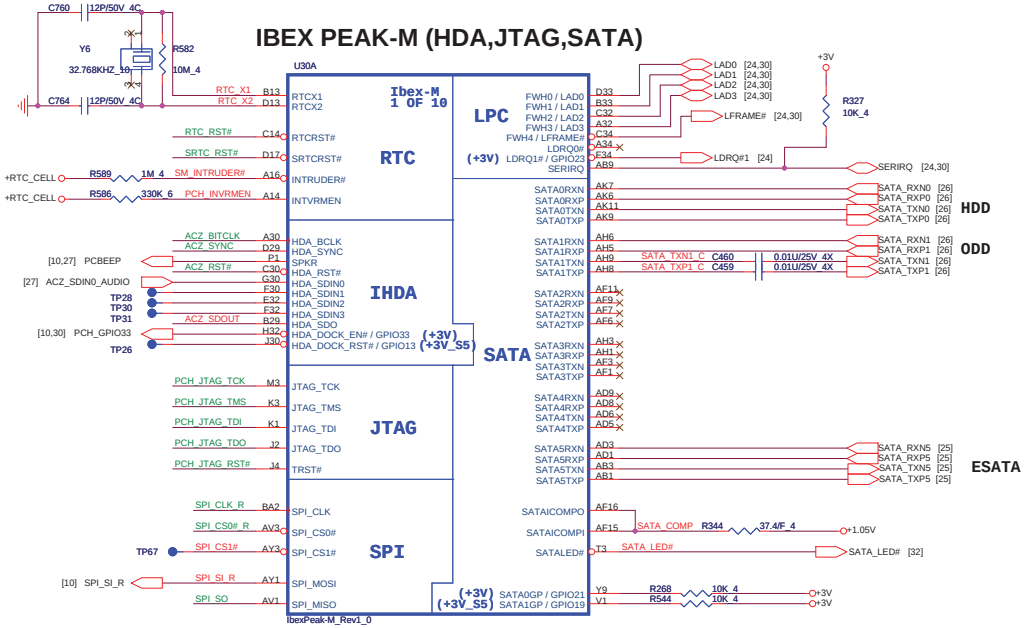
CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

Quanta Computer Inc.
PROJECT : TE2

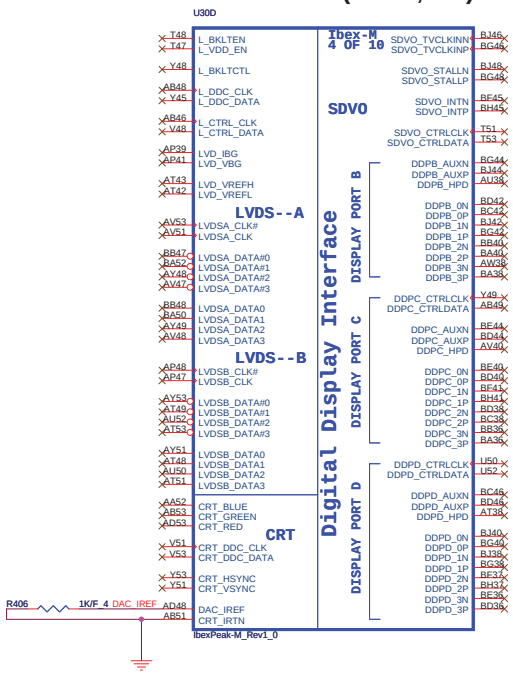
Size	Document Number	Rev
	PROCESSER 4/4 (GND)	2A
Date: Tuesday, March 09, 2010	Sheet 6 of 45	

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

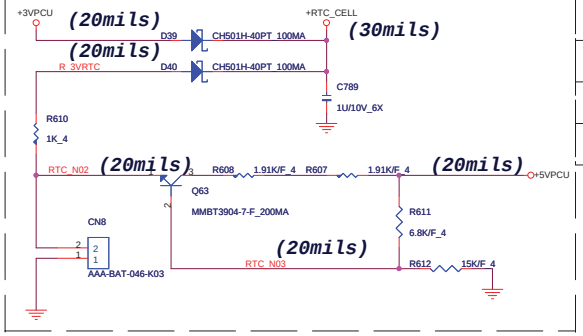


IBEX PEAK-M (LVDS,DDI)



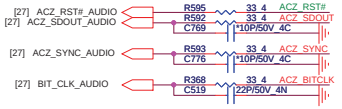
[RTC]

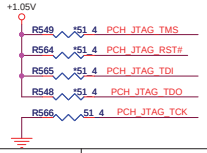
RTC BATTERY



Port	Strap	How to enable Port?	How to disable Port?
LVDS	L_DDC_DATA	PU to 3.3V with 2.2k+/- 5%	NC
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port D	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
eDP	CFG[4]	PD to GND directly	NC

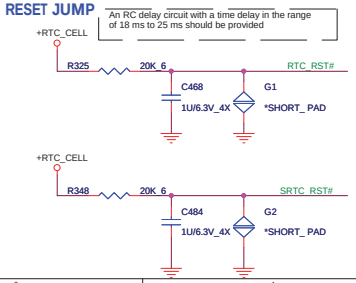
For AUDIO



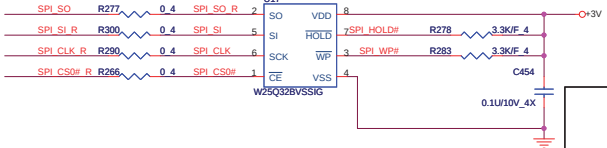


RESET JUMP

An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided



4M byte SPI ROM

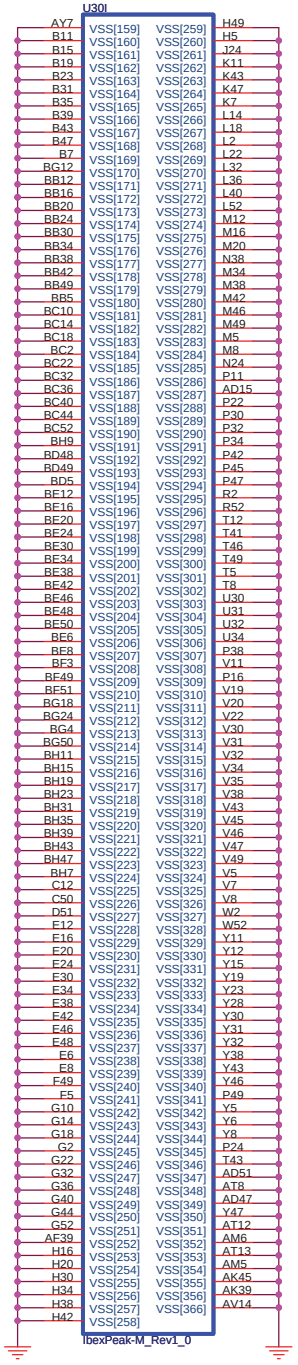


PCH	2MB	4MB	8MB
PM55	●		
HM55		●	
HM57/PM57		●	●
QM57/QS57			●

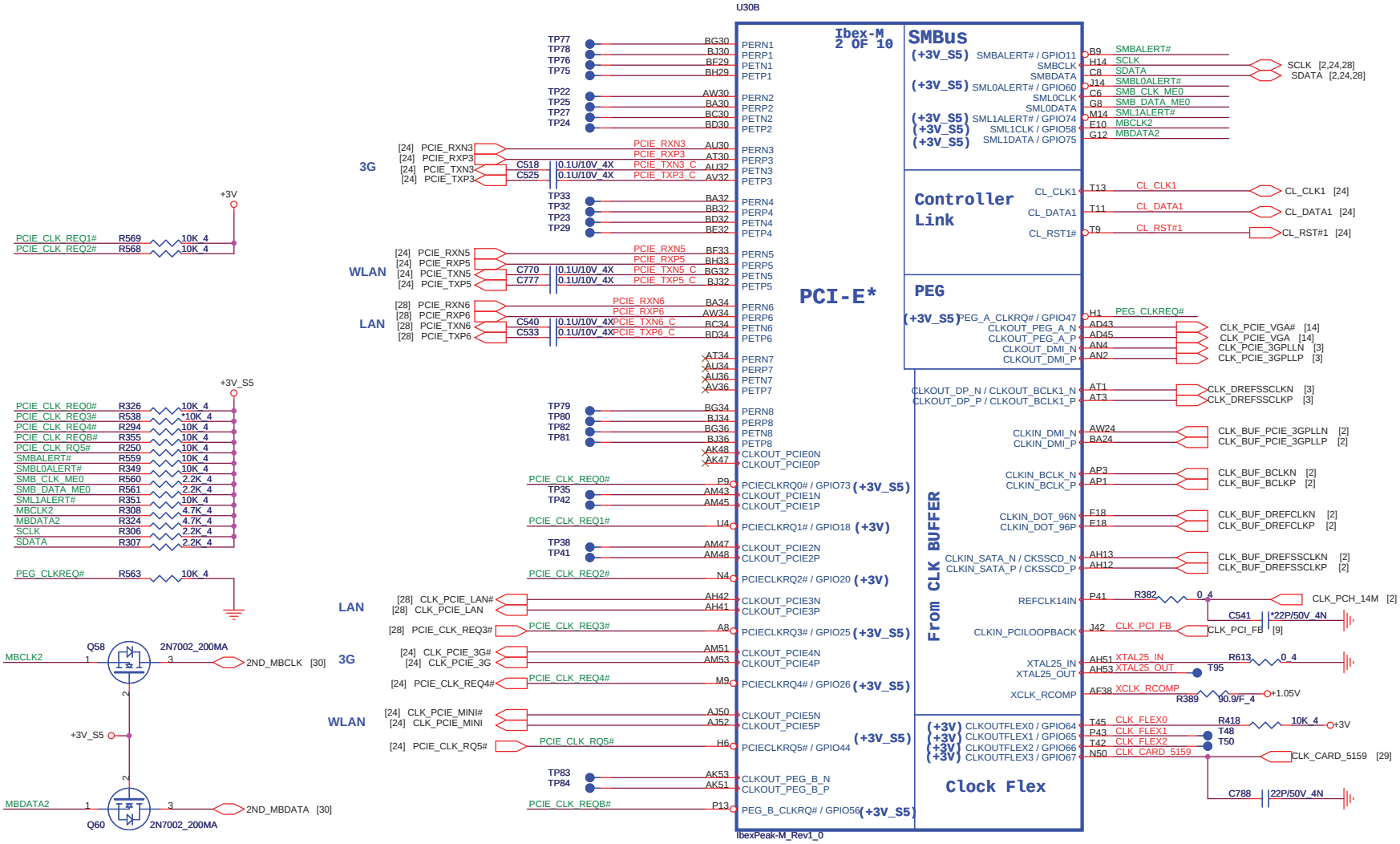
Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	2A
Date: Tuesday, March 09, 2010	Sheet 7 of 45	

IBEX PEAK-M (GND)

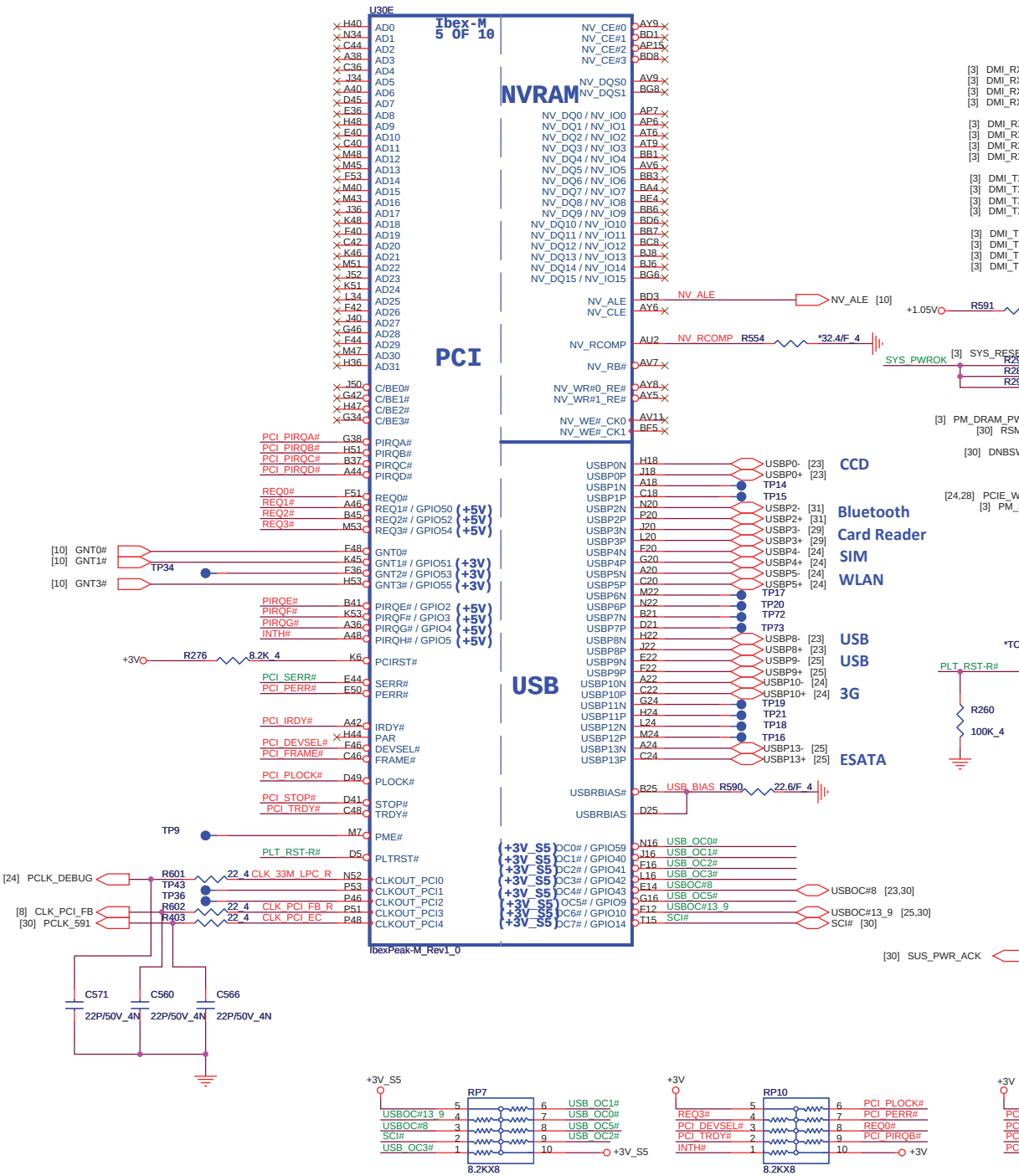


IBEX PEAK-M (PCI-E,SMBUS,CLK)

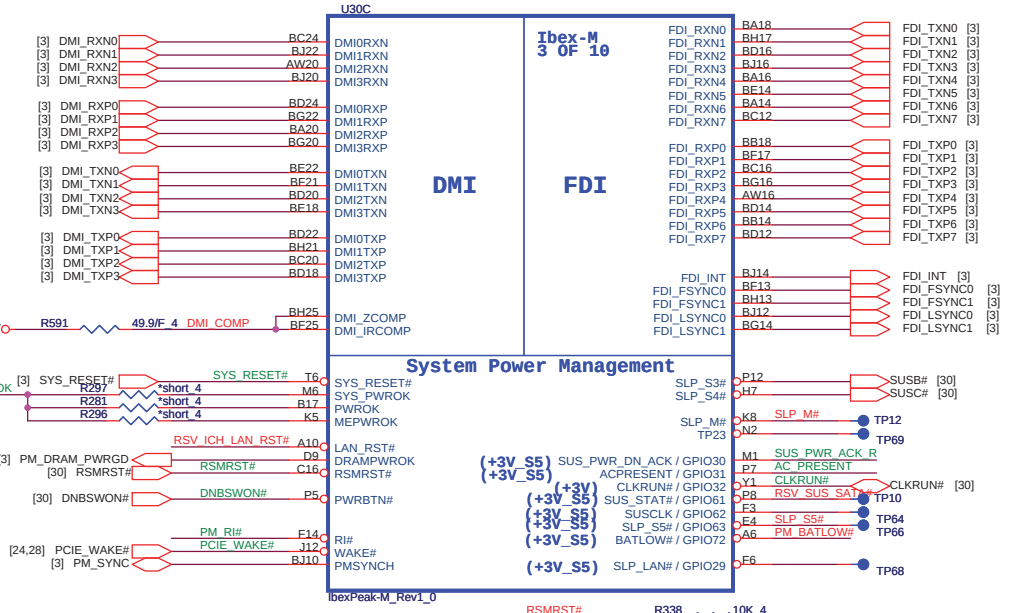


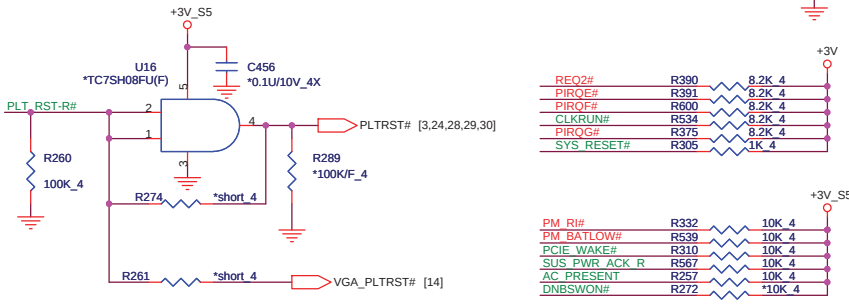
Quanta Computer Inc.	
PROJECT : TE2	
Size	Document Number: PCH 2/5 (PCIE, SMBUS, CK) — Rev: 2A
Date: Tuesday, March 09, 2010	Sheet 8 of 45

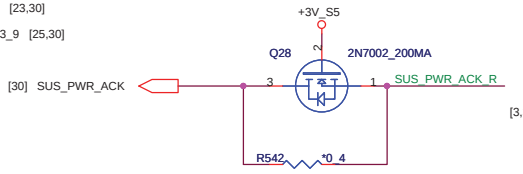
IBEX PEAK-M (PCI,USB,NVRAM)

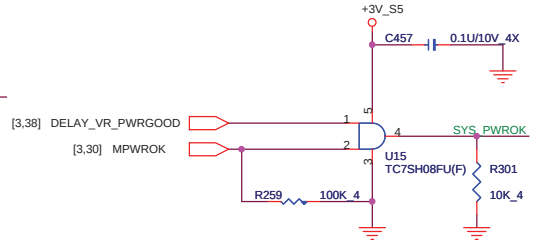


IBEX PEAK-M (DMI,FDI,GPIO)



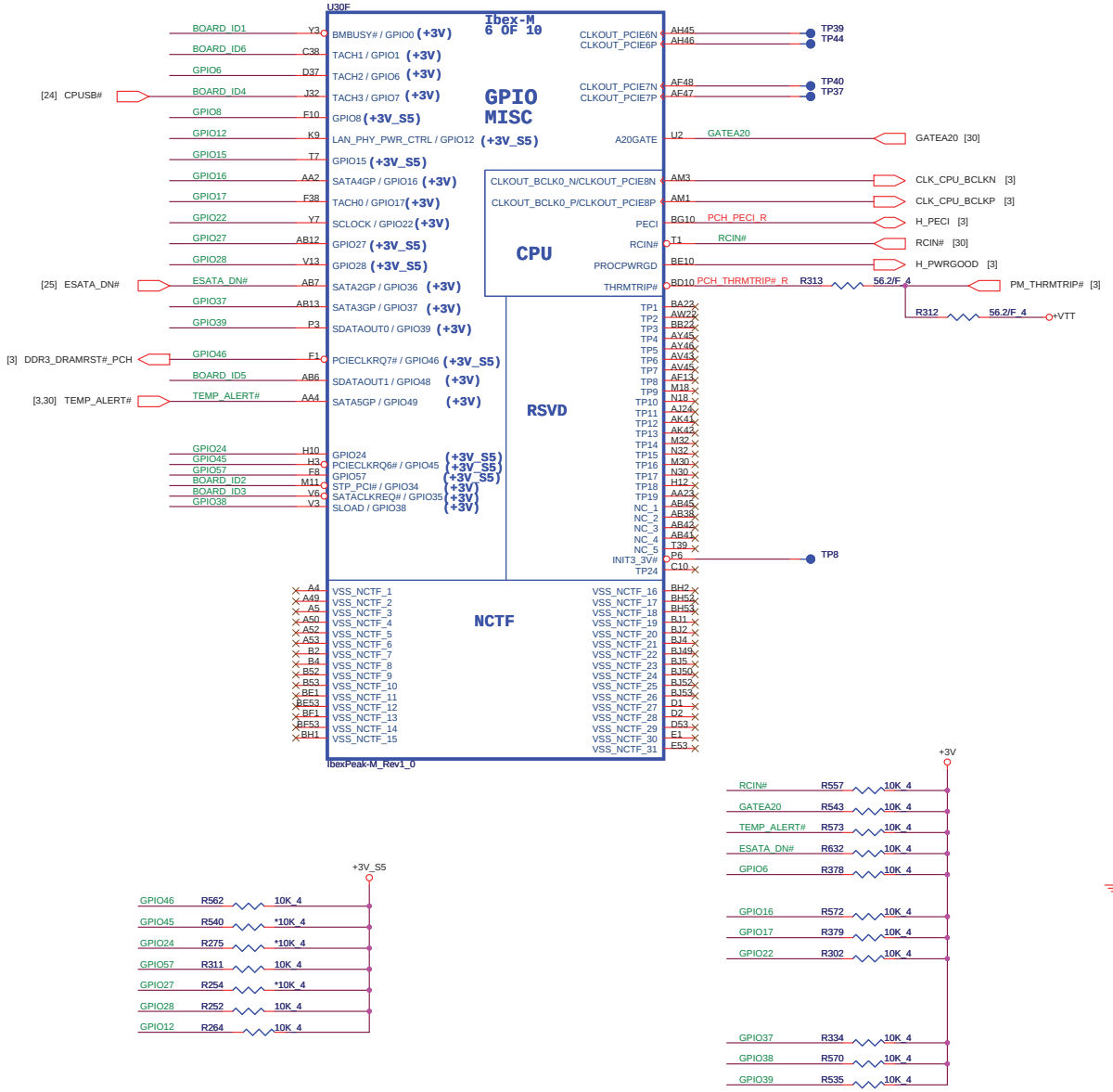




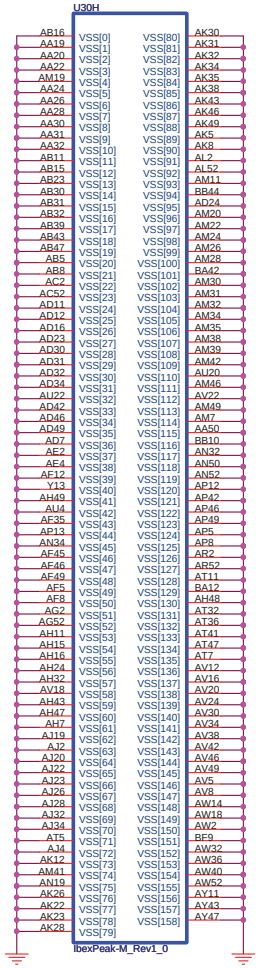


Quanta Computer Inc.			
PROJECT : TE2			
Size	Document Number		Rev
	PCH 3/5 (PCI,ONFI,USB,DMI)		2A
Date: Tuesday, March 09, 2010		Sheet 9 of 45	

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



PCH Strap Pin Configuration Table

SPKR

[7,27] PCBEEP — *1K/F_4 — R556 — +3V

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

GNT3#/ GPIO55

[9] GNT3# — R603 — *10K/F_4

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

HDA_DOCK_EN #/GPIO33

[7,30] PCH_GPIO33 — R371 — 1K_4 — JP1 (2, 1) *SHORT PAD

0 = Top Block Swap Mode
1 = Default Mode (Internal pull-up)

GNT0#, GNT1#

[9] GNT0# — GNT0# R397 *1K/F_4
[9] GNT1# — GNT1# R599 *1K/F_4

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

SPI_MOSI

[7] SPI_SI_R — R279 — *1K_4 — +3V

NV_ALE

[9] NV_ALE — R574 — *10K_4 — +1.8V

1 = Enabled
0 = Disabled (Default)

GPIO8

GPIO8 — R309 — 10K_4 — +3V_S5

This signal has a weak internal pull up.
NOTE: This signal should not be pulled low

GPIO15

GPIO15 — R267 — 1K_4 — +3V_S5

0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

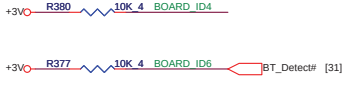
GPIO27

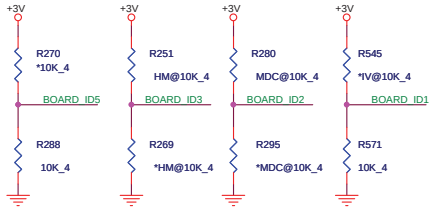
GPIO27 — R271 — *10K_4

0 = Disables the VccVRM. Need to use on-board filter circuits for analog rails.
1 = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.
This signal has a weak internal pull-up.

BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6
UMA SKU VGA SKU	H L					
W/ MDC W/O MDC		H L				
W/ HDMI W/O HDMI			H L			
W/O 3G W/ 3G				H L		
15" 14"					H L	
W/O BT W/ BT						H L





Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	2A
Date: Friday, March 19, 2010	Sheet 10 of 45	

+VCCA_DAC_1_2=69mA(15mils)

VCCCORE = 1.432A(80mils)

VCCALVDS= 59mA(15mils)

VCCLAN = 0.32A(30mils)

40mA(15mils)

VCC3_3 = 0.357A(30mils)

VCCVRM= 196mA(15mils)

VCCDMI= 61mA(15mils)

VCCPNAND= 156mA(15mils)

VCCIO = 3.062A(150mils)

68mA(15mils)

VCCME3_3= 85mA(15mils)

VCCIO = 3.062A(150mils)

37mA(15mils)

VCCSUS3_3 = 0.163A(20mils)

VCC3_3 = 0.357A(30mils)

V_CPU >1mA(15mils)

VCCRTC= 2mA(15mils)

VCCSUSHDA= 6mA(15mils)

V5REF_SUS< 1mA

V5REF< 1mA

VCCIO = 3.062A(150mils)

VCCME = 1.849A(100mils)

Reserve for clear CRT Power

C3A

POWER

Ibex-M 7 OF 10

Ibex-M 10 OF 10

U30G

U30J

CRT

LVDS

HVCMOS

DMI

NAND / SPI

VCC CORE

PCI E*

FDI

USB

SATA

PCI/GPIO/LPC

CPU

RTC

HDA

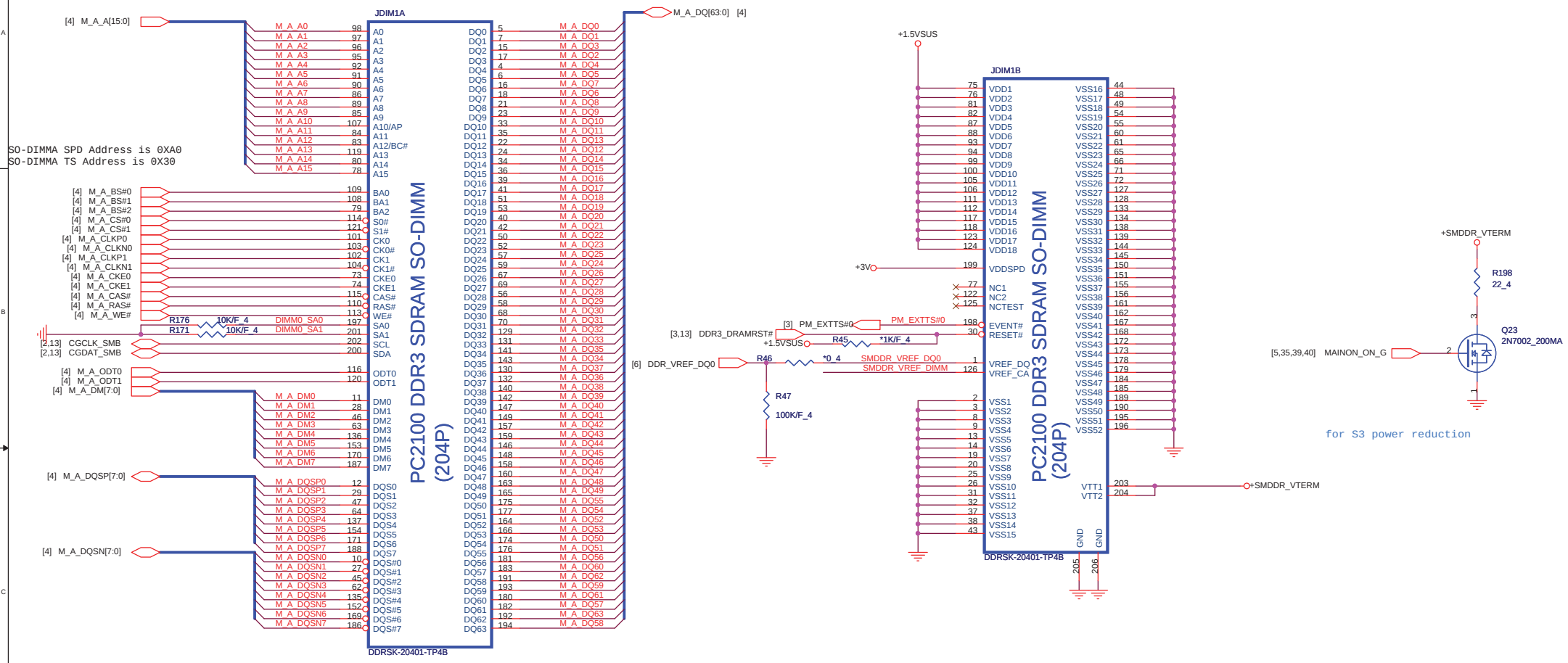
Clock and Miscellaneous

IbexPeak-M_Rev1_0

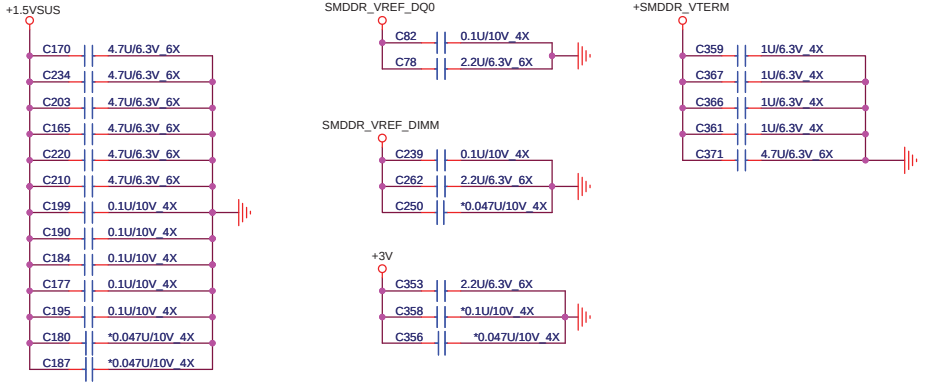
U21

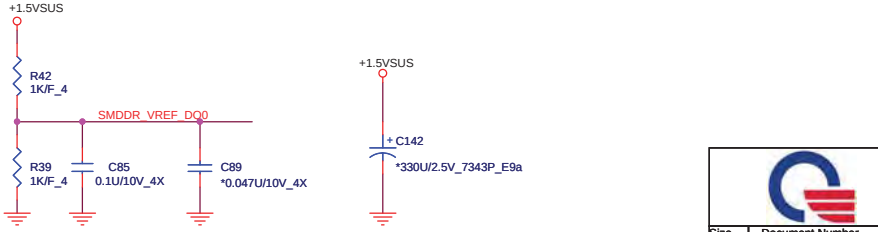
*G913C

Quanta Computer Inc.			
PROJECT : TE2			
Size	Document Number		Rev
	PCH 5/5 (POWER)		2A
Date: Wednesday, March 10, 2010		Sheet 11 of 45	

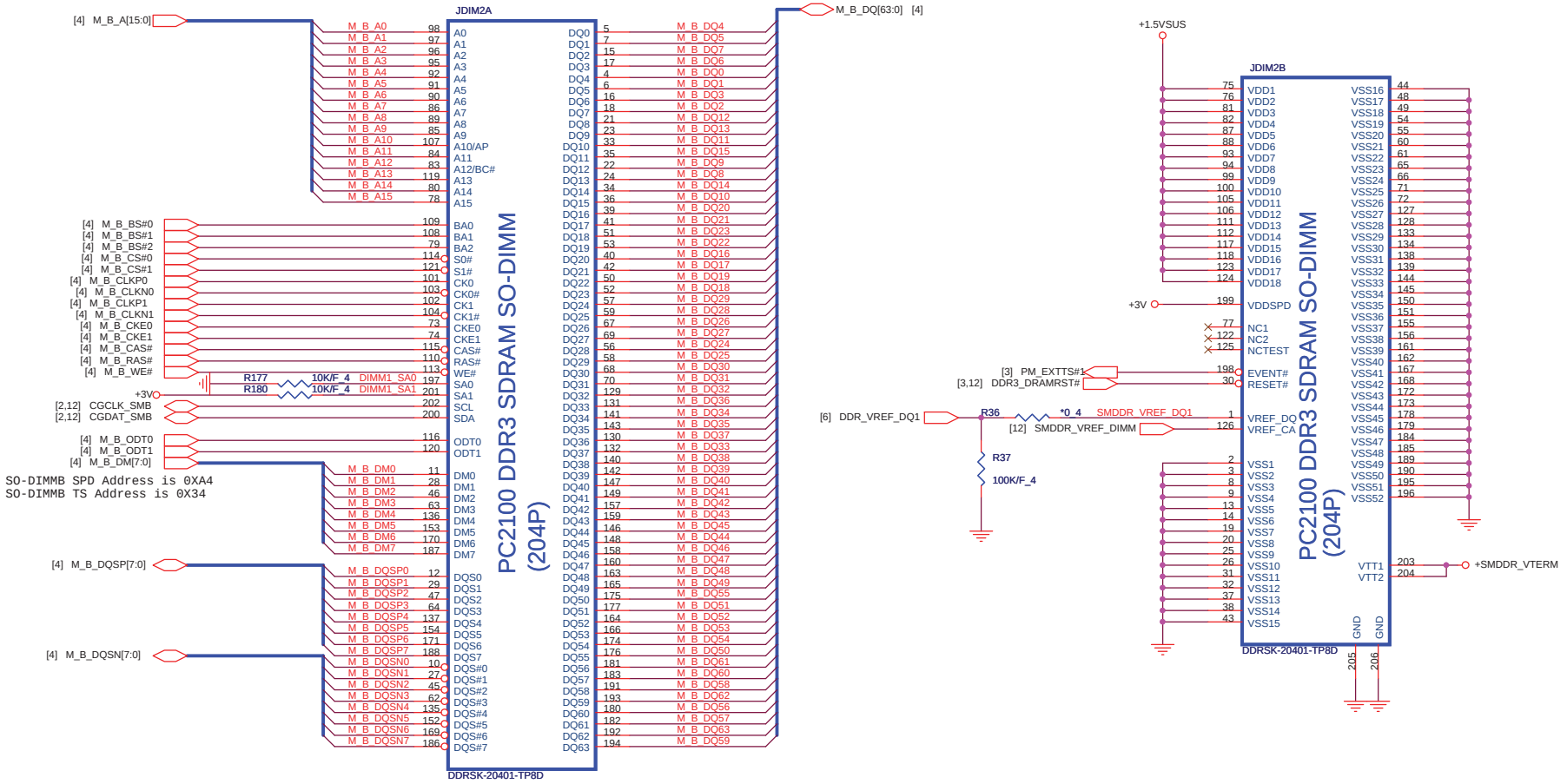


Place these Caps near So-Dimm0.

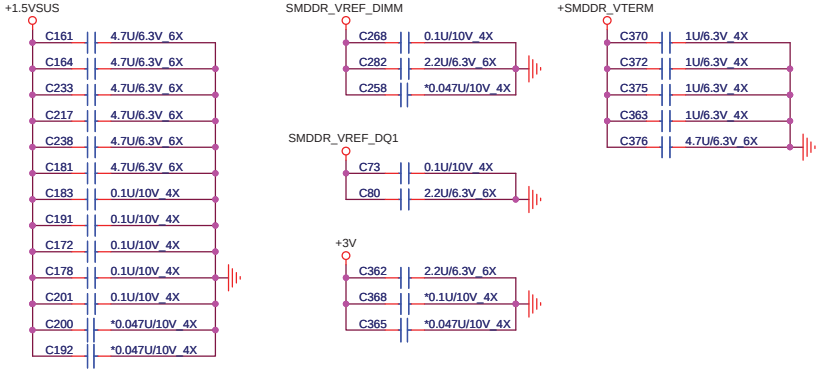


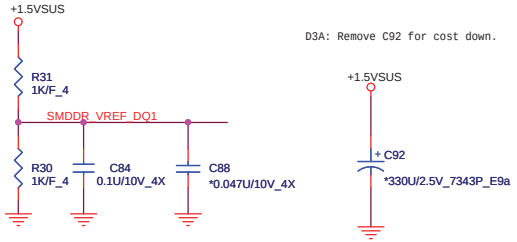


Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: DDR3 DIMM-0	Rev: 2A
Date: Wednesday, March 10, 2010	Sheet 12 of 43	



Place these Caps near So-Dimm1.

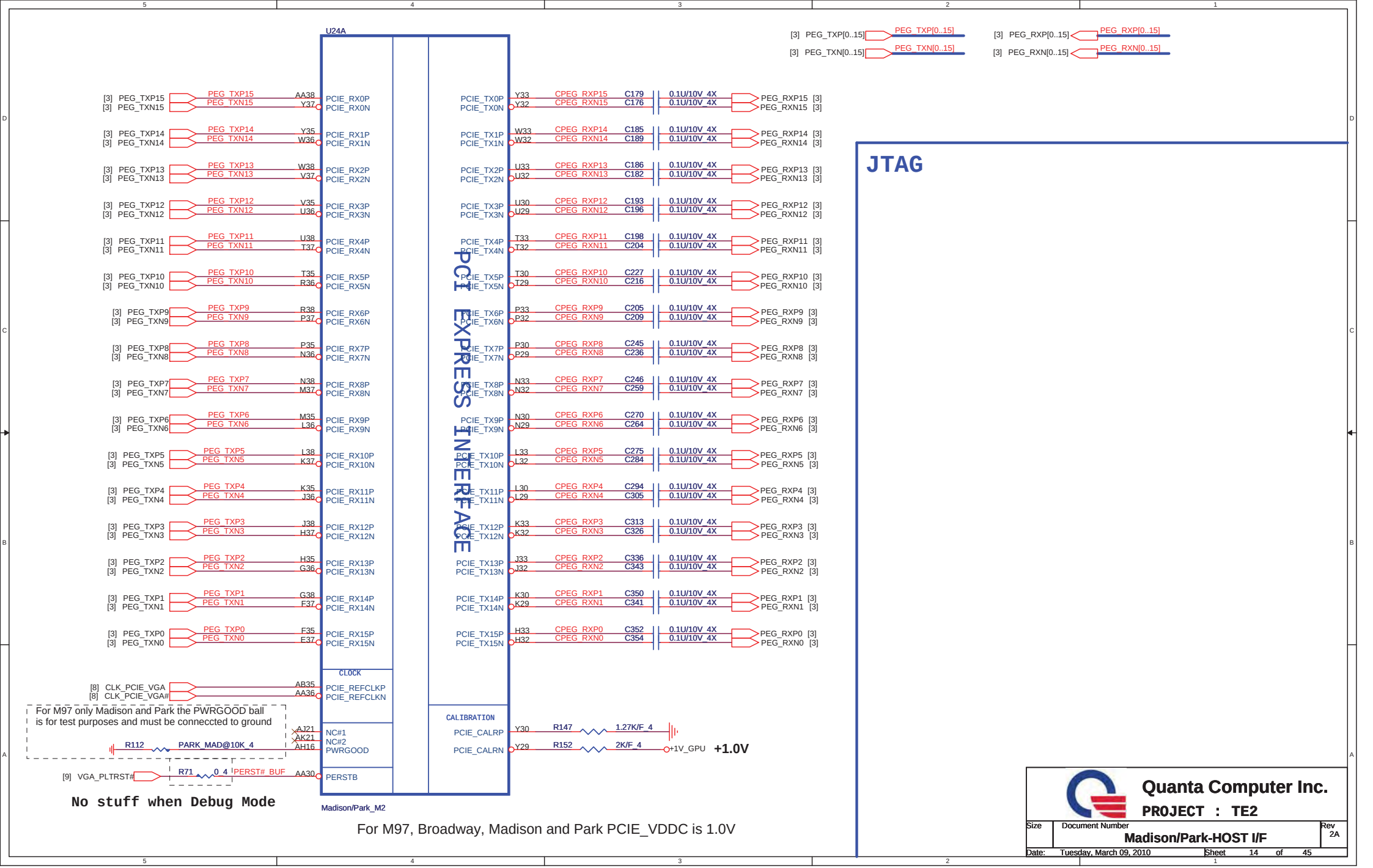




D3A: Remove C92 for cost down.

Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	DDR3 DIMM-1	2A
Date: Wednesday, March 10, 2010	Sheet 13 of 43	



For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

GPU Power-on sequence

1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V_GPU
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => +GPU_PWROK

JTAG SIGNAL STUFF OPTION FOR OPTION2

SIGNALS	NORMAL MODE	JTAG MODE (DEBUG
TESTEN	"1" (PU)	"1" (PU)
GPIO24_TRSTB	"0" (PD)	"1" (PU)
GPIO26_TCK	CLK	"1" (PU)
GPIO27_TMS	"1" (PU)	"1" (PU)

1.8V GPIO

NC on Park

SCL must be tied high if not used

DP

PLACE AC CAP CLOSE TO CONNECTOR

NC on Park

LVDS

HDMI DDC

Place close to Chip

HDMI

CRT

NC on Park

LVDS

NC on Park

+1.8V(20mA)

75mA (10mils)

125mA (10mils)

(1.8V@70mA AVDD)

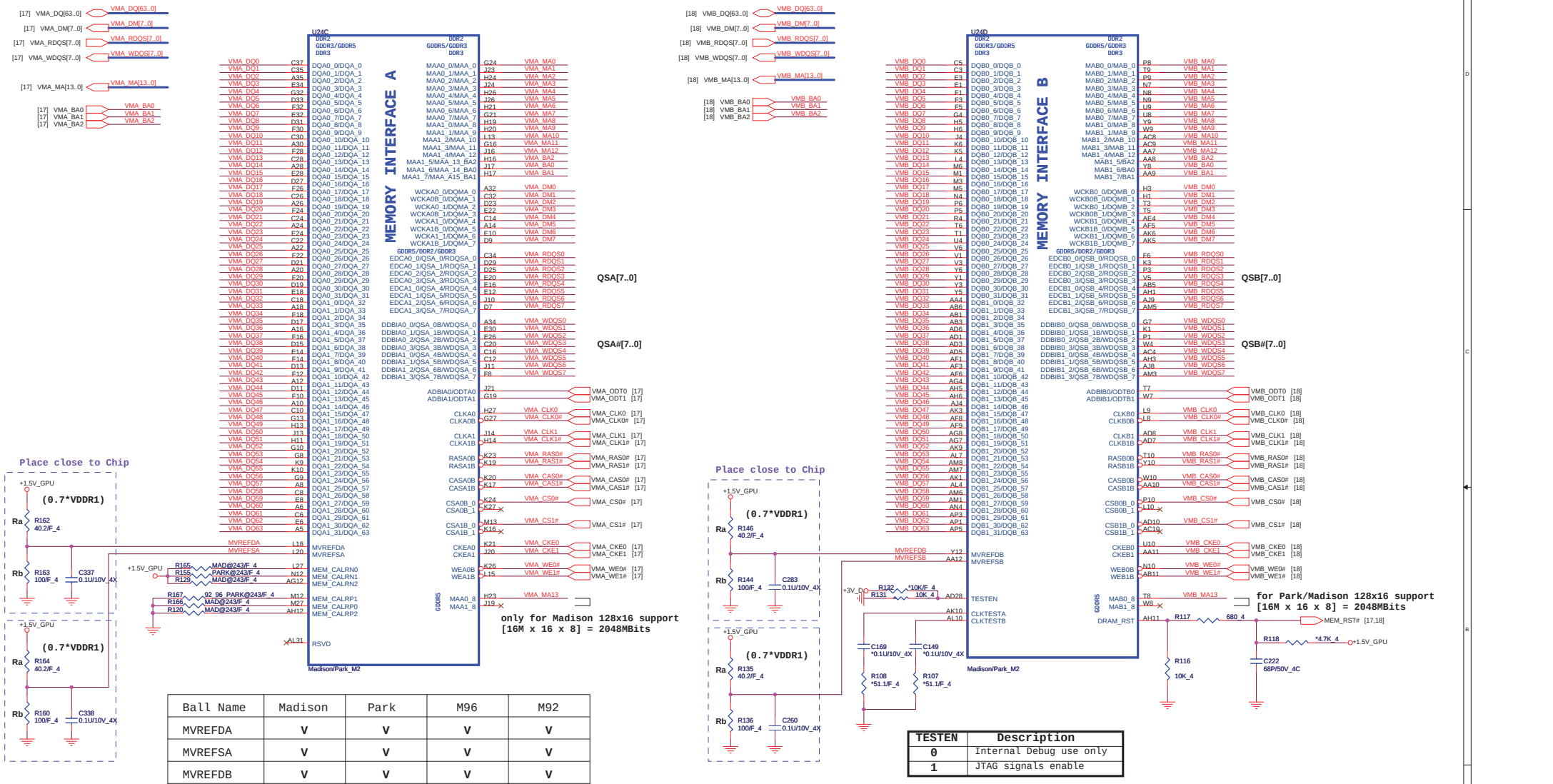
(1.8V@100mA VDD1DI)

(1.8V@2mA A2VDDQ)

(3.3V@130mA A2VDD)

Madison/Park_M2

Quanta Computer Inc.
PROJECT : TE2
Size: Document Number: Madison/Park-HOST I/F Rev: 2A
Date: Wednesday, March 10, 2010 Sheet 15 of 45

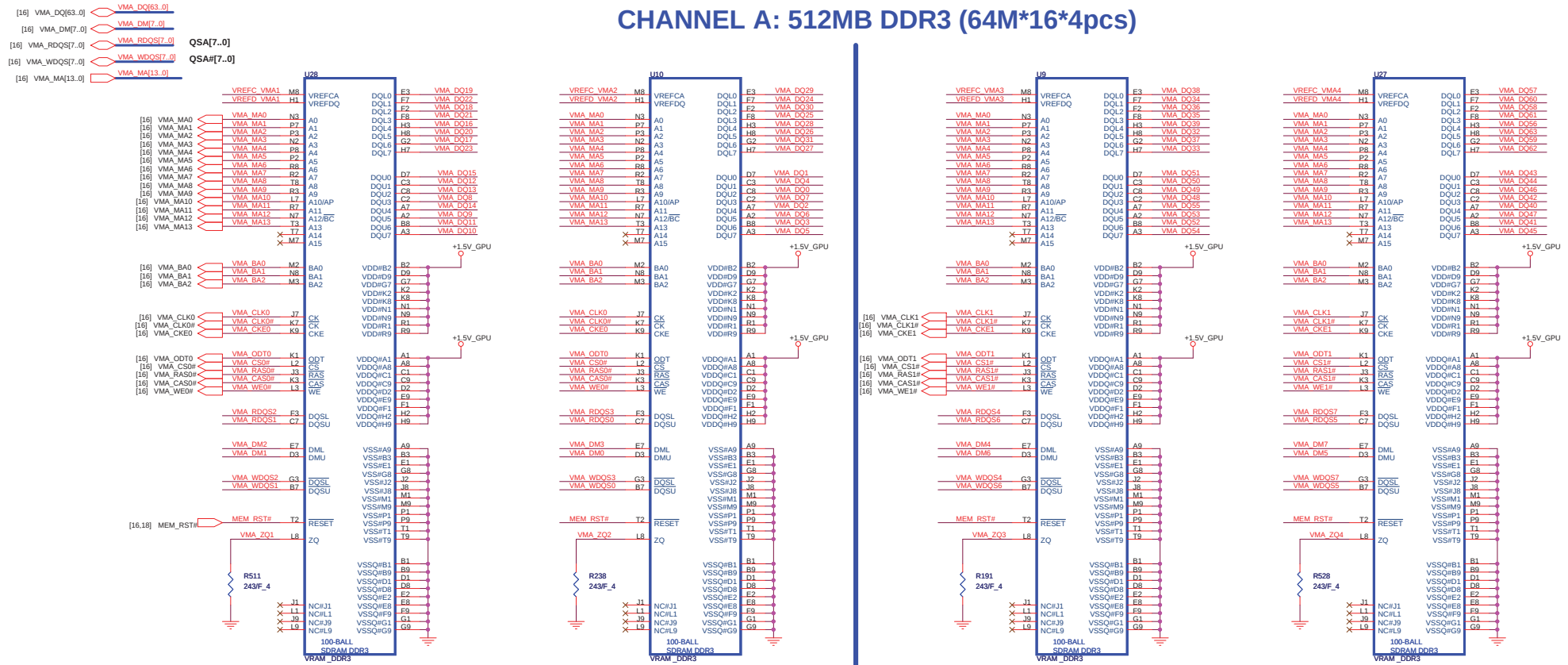


Ball Name	Madison	Park	M96	M92
MVREFDA	V	V	V	V
MVREFSA	V	V	V	V
MVREFDB	V	V	V	V
MVREFSB	V	V	V	V
MEM_CALRN0	V	V		
MEM_CALRN1	V	V		
MEM_CALRN2	V			
MEM_CALRP0	V	V		
MEM_CALRP1	V	V	V	V
MEM_CALRP2	V			

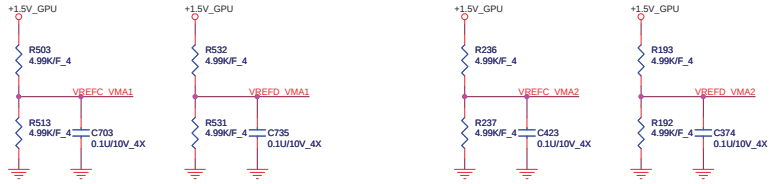
TESTEN	Description
0	Internal Debug use only
1	JTAG signals enable

Quanta Computer Inc.
PROJECT : TE2
Size | Document Number | Rev 2A
Madison/Park-MEM I/F
Date: Tuesday, March 09, 2010 | Sheet 16 of 45

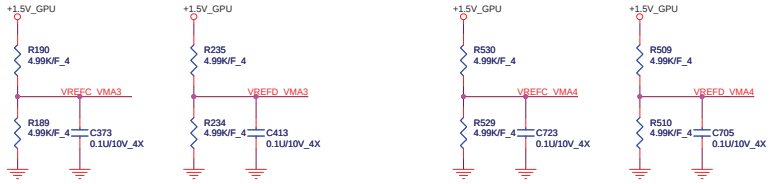
CHANNEL A: 512MB DDR3 (64M*16*4pcs)



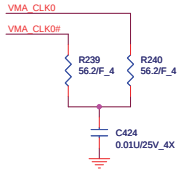
Group-A0 VREF



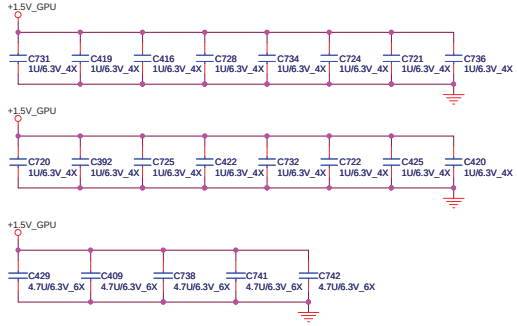
Group-A1 VREF



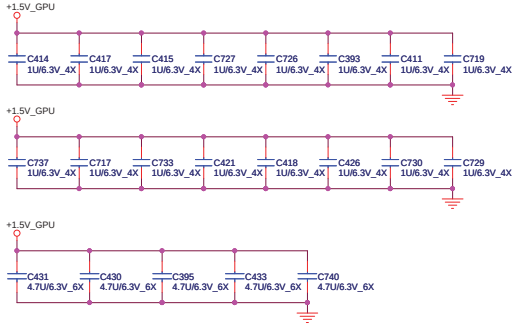
MEM_A0 CLK



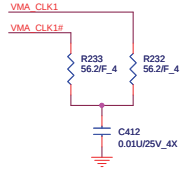
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK

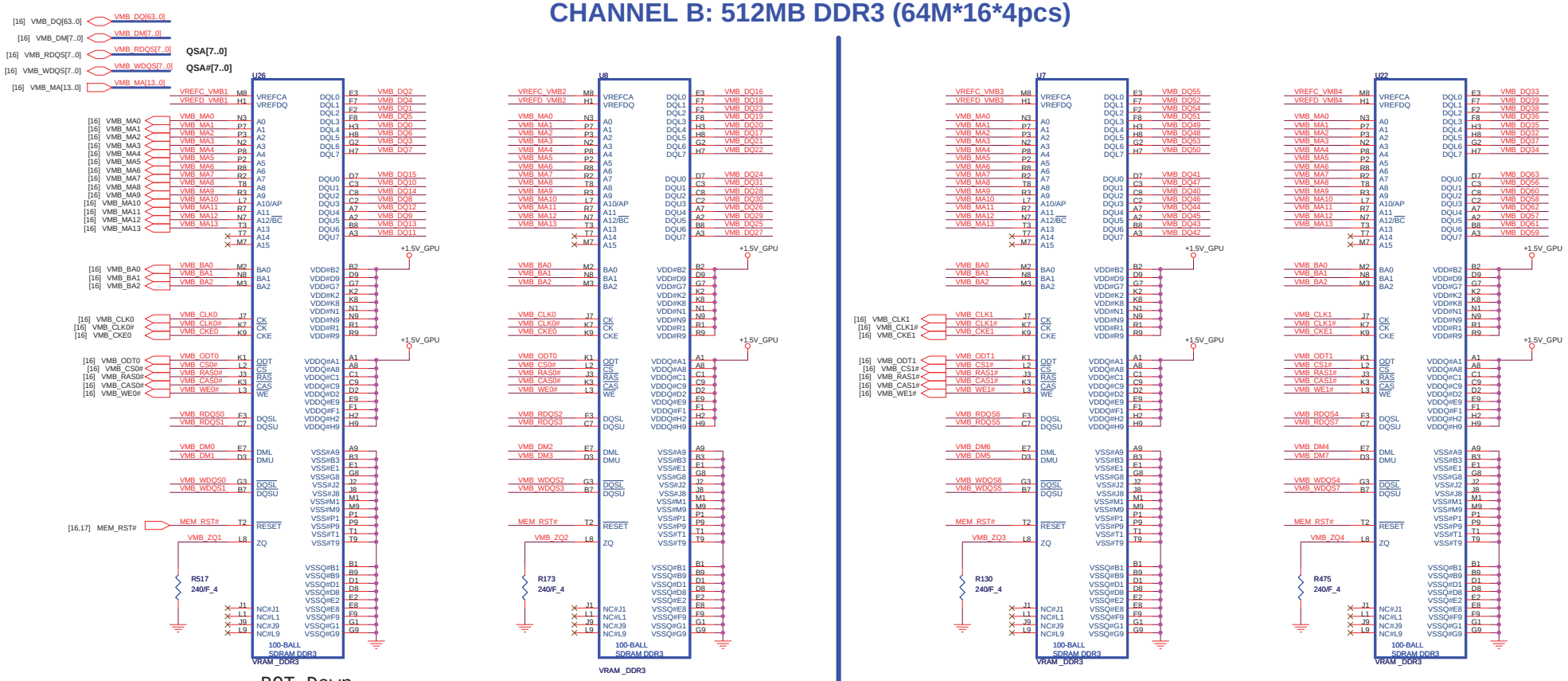


Quanta Computer Inc.

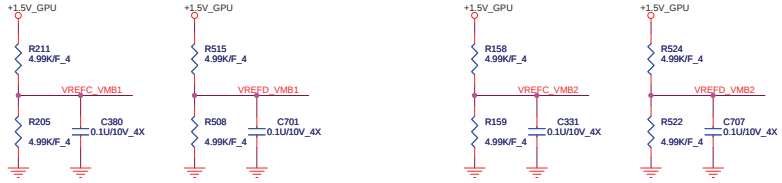
PROJECT : TE2

Size	Document Number	Rev
	VRAM_A: DDR3-64M*16*4PCS	2A
Date: Friday, March 19, 2010	Sheet 17 of 45	

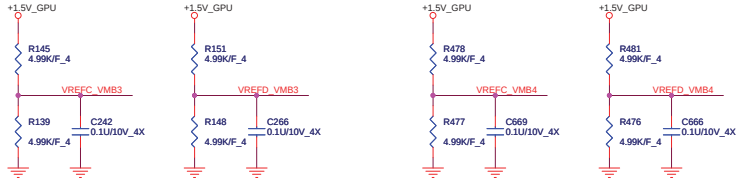
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



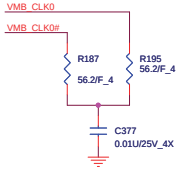
Group-B0 VREF



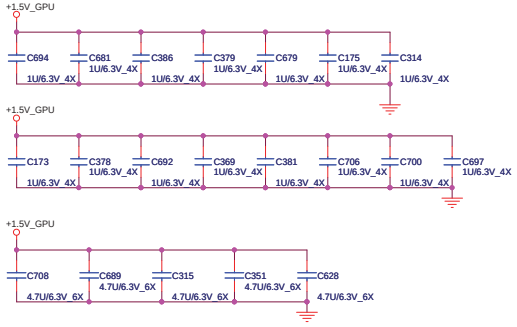
Group-B1 VREF



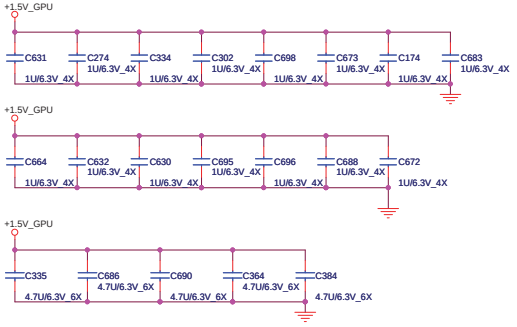
MEM_B0 CLK



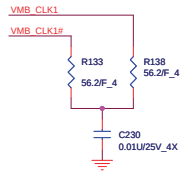
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	VRAM_B: DDR3-64M*16*4PCS	2A
Date: Wednesday, March 10, 2010	Sheet 18 of 45	

For Madison and Park VDDCI and VDDC can share one common regulator

VDD/VDDQ =1.5V at 1333
VDD/VDDQ =1.8V at 1600 and 1800

U24E

MEM I/O

VDDR1#1 VDDR1#2 VDDR1#3 VDDR1#4 VDDR1#5 VDDR1#6 VDDR1#7 VDDR1#8 VDDR1#9 VDDR1#10 VDDR1#11 VDDR1#12 VDDR1#13 VDDR1#14 VDDR1#15 VDDR1#16 VDDR1#17 VDDR1#18 VDDR1#19 VDDR1#20 VDDR1#21 VDDR1#22 VDDR1#23 VDDR1#24 VDDR1#25 VDDR1#26 VDDR1#27 VDDR1#28 VDDR1#29 VDDR1#30 VDDR1#31 VDDR1#32 VDDR1#33 VDDR1#34

LEVEL TRANSLATION

VDD_CT#1 VDD_CT#2 VDD_CT#3 VDD_CT#4

I/O

VDDR3#1 VDDR3#2 VDDR3#3 VDDR3#4

VDDR4#4 VDDR4#5 VDDR4#7 VDDR4#8

VDDR4#1 VDDR4#2 VDDR4#3 VDDR4#6

NC_VDDRHA NC_VSSRHA

NC_VDDRHB NC_VSSRHB

PLL

PCIE_PVDD

MPV18#1 MPV18#2

SPV18

SPV10

SPVSS

VOLTAGE SENESE

FB_VDDC

FB_VDDCI

FB_GND

Madison/Park_M2

PCIE

PCIE_VDDR#1 PCIE_VDDR#2 PCIE_VDDR#3 PCIE_VDDR#4 PCIE_VDDR#5 PCIE_VDDR#6 PCIE_VDDR#7 PCIE_VDDR#8

PCIE_VDDC#1 PCIE_VDDC#2 PCIE_VDDC#3 PCIE_VDDC#4 PCIE_VDDC#5 PCIE_VDDC#6 PCIE_VDDC#7 PCIE_VDDC#8 PCIE_VDDC#9 PCIE_VDDC#10 PCIE_VDDC#11 PCIE_VDDC#12

CORE

VDDC#1 VDDC#2 VDDC#3 VDDC#4 VDDC#5 VDDC#6 VDDC#7 VDDC#8 VDDC#9 VDDC#10 VDDC#11 VDDC#12 VDDC#13 VDDC#14 VDDC#15 VDDC#16 VDDC#17 VDDC#18 VDDC#19 VDDC#20 VDDC#21 VDDC#22 VDDC#23 VDDC#24 VDDC#25 VDDC#26 VDDC#27 VDDC#28 VDDC#29 VDDC#30 VDDC#31 VDDC#32 VDDC#33 VDDC#34 VDDC#35 VDDC#36 VDDC#37 VDDC#38 VDDC#39 VDDC#40 VDDC#41 VDDC#42 VDDC#43 VDDC#44 VDDC#45 VDDC#46 VDDC#47 VDDC#48 VDDC#49 VDDC#50 VDDC#51 VDDC#52 VDDC#53 VDDC#54 VDDC#55 VDDC#56 VDDC#57 VDDC#58

ISOLATED CORE I/O

VDDCI#1 VDDCI#2 VDDCI#3 VDDCI#4 VDDCI#5 VDDCI#6 VDDCI#7 VDDCI#8 VDDCI#9 VDDCI#10 VDDCI#11 VDDCI#12 VDDCI#13 VDDCI#14 VDDCI#15 VDDCI#16 VDDCI#17 VDDCI#18 VDDCI#19 VDDCI#20 VDDCI#21 VDDCI#22

POWER

+1.5V_GPU

(1.5V@5A_VDDR1)

C432 4.7U/6.3V_6X C739 4.7U/6.3V_6X C663 4.7U/6.3V_6X

C279 1U/6.3V_4X C339 1U/6.3V_4X C387 1U/6.3V_4X C710 1U/6.3V_4X C709 1U/6.3V_4X C398 1U/6.3V_4X

C388 0.1U/10V_4X C660 0.1U/10V_4X C680 0.1U/10V_4X C290 0.1U/10V_4X C257 0.1U/10V_4X

+1.8V_GPU

120 ohm/300mA

L33 BLM15BD121SN1D_300MA

(1.8V@110mA VDD_CT)

VDDC_CT

C618 4.7U/6.3V_6X C226 1U/6.3V_4X C244 0.1U/10V_4X

+3V_O

(3.3V@60mA)

C228 4.7U/6.3V_6X C225 1U/6.3V_4X C223 1U/6.3V_4X

120 ohm/300mA

L16 BLM15BD121SN1D_300MA

(1.8V@170mA)

VDDR4

C232 1U/6.3V_4X C241 0.1U/10V_4X

+1.5V_GPU M96 ONLY

L43 96@HCB1608KF-181T15_1.5A

+VDDRHA

C793 96@0.1U/10V_4X

+VDDRHB

L42 9X@HCB1608KF-181T15_1.5A

C795 9X@0.1U/10V_4X

120 ohm/300mA

L8 BLM15BD121SN1D_300MA

(1.8V@40mA PCIE_PVDD)

PCIE_PVDD

C138 4.7U/6.3V_6X C145 1U/6.3V_4X C139 0.1U/10V_4X

Park,Madison ONLY

120 ohm/300mA

L19 PARK_MAD@BLM15BD121SN1D_300MA

(1.8V@150mA MPV18)

MPV18

C389 PARK_MAD@4.7U/6.3V_6X C390 PARK_MAD@1U/6.3V_4X C391 PARK_MAD@0.1U/10V_4X

Park,Madison ONLY

120 ohm/300mA

L13 PARK_MAD@BLM15BD121SN1D_300MA

(1.8V@75mA SPV18)

SPV18

C147 PARK_MAD@4.7U/6.3V_6X C163 PARK_MAD@0.1U/10V_4X

SPV10

[40] VGA_CORE_P

T26

[40] VSS_VCORE_P_SENSE

+1V_GPU

L9 PARK_MAD@BLM15BD121SN1D_300MA

+VGPU_CORE

L44 9X@BLM15BD121SN1D_300MA

120 ohm/300mA

(1.0V@120mA SPV10)

C146 4.7U/6.3V_6X C162 0.1U/10V_4X

(1.8V@400mA PCIE_VDDR)

PCIE_VDDR

180 ohm/1.5A

L3 HCB1608KF-181T15_1.5A

C263 0.1U/10V_4X C125 0.1U/10V_4X C115 1U/6.3V_4X C114 1U/6.3V_4X C112 4.7U/6.3V_6X

(1.0V@2A PCIE_VDDC)

+1V_GPU

C324 1U/6.3V_4X C340 1U/6.3V_4X C309 1U/6.3V_4X C333 1U/6.3V_4X C297 1U/6.3V_4X C312 4.7U/6.3V_6X

+VGPU_CORE

(30A or more)

C286 1U/6.3V_4X C285 1U/6.3V_4X C304 1U/6.3V_4X C325 1U/6.3V_4X C295 1U/6.3V_4X

C318 1U/6.3V_4X C307 1U/6.3V_4X C308 1U/6.3V_4X C306 1U/6.3V_4X C296 1U/6.3V_4X C303 1U/6.3V_4X C261 1U/6.3V_4X C328 1U/6.3V_4X C292 1U/6.3V_4X C317 1U/6.3V_4X

C271 4.7U/6.3V_6X C273 4.7U/6.3V_6X C269 4.7U/6.3V_6X C277 4.7U/6.3V_6X C293 4.7U/6.3V_6X

+VGPU_CORE

(DDR3 1.12V@4A VDDCI) or more

ISOLATED_CORE

R470 0_8

R471 0_8

C248 1U/6.3V_4X C327 1U/6.3V_4X C316 1U/6.3V_4X C255 1U/6.3V_4X

C272 4.7U/6.3V_6X C235 4.7U/6.3V_6X

U24F

GND

PCIE_VSS#1 PCIE_VSS#2 PCIE_VSS#3 PCIE_VSS#4 PCIE_VSS#5 PCIE_VSS#6 PCIE_VSS#7 PCIE_VSS#8 PCIE_VSS#9 PCIE_VSS#10 PCIE_VSS#11 PCIE_VSS#12 PCIE_VSS#13 PCIE_VSS#14 PCIE_VSS#15 PCIE_VSS#16 PCIE_VSS#17 PCIE_VSS#18 PCIE_VSS#19 PCIE_VSS#20 PCIE_VSS#21 PCIE_VSS#22 PCIE_VSS#23 PCIE_VSS#24 PCIE_VSS#25 PCIE_VSS#26 PCIE_VSS#27 PCIE_VSS#28 PCIE_VSS#29 PCIE_VSS#30 PCIE_VSS#31 PCIE_VSS#32 PCIE_VSS#33 PCIE_VSS#34 PCIE_VSS#35

GND#100 GND#101 GND#102 GND#103 GND#104 GND#105 GND#106 GND#107 GND#108 GND#109 GND#110 GND#111 GND#112 GND#113 GND#114 GND#115 GND#116 GND#117 GND#118 GND#119 GND#120 GND#121 GND#122 GND#123 GND#124 GND#125 GND#126 GND#127 GND#128 GND#129 GND#130 GND#131 GND#132 GND#133 GND#134 GND#135 GND#136 GND#137 GND#138 GND#139 GND#140 GND#141 GND#142 GND#143 GND#144 GND#145 GND#146 GND#147 GND#148 GND#149 GND#150 GND#151 GND#153 GND#154 GND#155 GND#156 GND#157 GND#158 GND#159 GND#160 GND#161 GND#163 GND#164 GND#165 GND#166 GND#167 GND#168 GND#169 GND#170 GND#171 GND#172 GND#173 GND#174 GND#175 GND#152 GND#162

GND#1 GND#2 GND#3 GND#4 GND#5 GND#6 GND#7 GND#8 GND#9 GND#10 GND#11 GND#12 GND#13 GND#14 GND#15 GND#16 GND#17 GND#18 GND#19 GND#20 GND#21 GND#22 GND#23 GND#24 GND#25 GND#26 GND#27 GND#28 GND#29 GND#30 GND#31 GND#32 GND#33 GND#34 GND#35 GND#36 GND#37 GND#38 GND#39 GND#40 GND#41 GND#42 GND#43 GND#44 GND#45 GND#46 GND#47 GND#48 GND#49 GND#50 GND#51 GND#52 GND#53 GND#54 GND#55 GND#56 GND#57 GND#58 GND#59 GND#60 GND#61 GND#62 GND#63 GND#64 GND#65 GND#66 GND#67 GND#68 GND#69 GND#70 GND#71 GND#72 GND#73 GND#74 GND#75 GND#76 GND#77 GND#78 GND#79 GND#80 GND#81 GND#82 GND#83 GND#84 GND#85 GND#86 GND#87 GND#88 GND#89 GND#90 GND#91 GND#92 GND#93 GND#94 GND#95 GND#96 GND#97 GND#98 GND#99

VSS_MECH#1 VSS_MECH#2 VSS_MECH#3

Madison/Park_M2

PowerXpress control signal for Madsion and Park only
If not used, can be disconnected. (AL21 pin)

PX_EN = LOW, turn on
PX_EN = HIGH, turn off

R104 *0_4

Pin AL21 to Ground for Broadway

Route as differential Pair

GPU all PWROK

+3V

R58 10K_4

R41 10K_4

Q10 DMN601K-7_300MA

GPU_PWROK [30]

+1.8V_GPU

Q8 DDTC144EUA-F-7_30MA

GPU +3V power

R410 9X@0_4

R82 *EV@0_4

R83 *EV@0_4

+1.5V_GPU

[30,40] GPU_VRON

C116 9X@1U/6.3V_4X

Q17 9X@DDTC144EUA-7-F_30MA

R61 9X@4.7K_4

Q18 9X@AO3413_3A

R89 PARK_MAD@0_8

0.5A

+3V_D

C137 *EV@10U/6.3V_8X

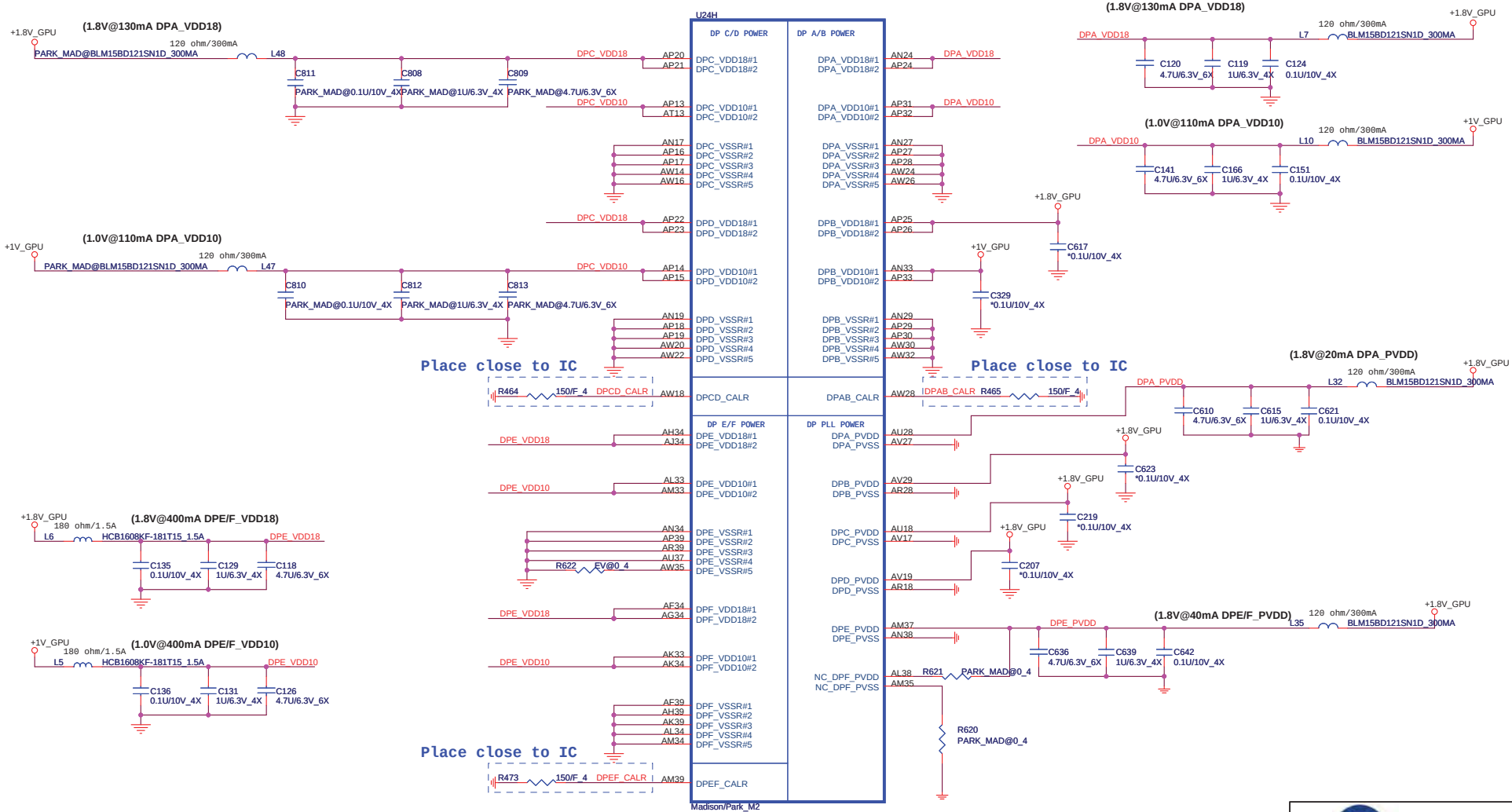
C134 *EV@1U/6.3V_4X

C128 *EV@0.1U/10V_4X

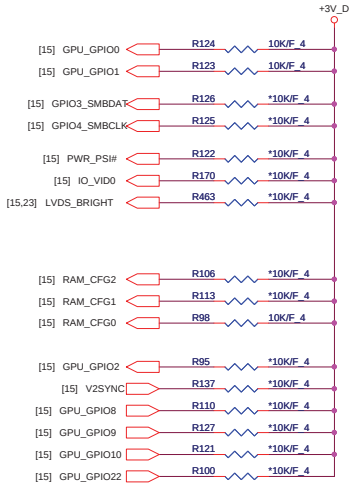
Quanta Computer Inc.
PROJECT : TE2

Size: Document Number: Madison/Park PWR_GND Rev: 2A

Date: Tuesday, March 09, 2010 Sheet 19 of 45


U24H
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
Madison/Park_M2
(1.8V@130mA DPA_VDD18)
(1.0V@110mA DPA_VDD10)
(1.8V@20mA DPA_PVDD)
(1.8V@400mA DPE/F_VDD18)
(1.0V@400mA DPE/F_VDD10)
(1.8V@40mA DPE/F_PVDD)
Place close to IC
Place close to IC
Place close to IC
+1.8V_GPU
+1V_GPU
120 ohm/300mA
180 ohm/1.5A
PARK_MAD@BLM15BD121SN1D_300MA
HCB1608KF-181T15_1.5A
DPC_VDD18
DPC_VDD10
DPD_VDD18
DPD_VDD10
DPE_VDD18
DPE_VDD10
DPA_VDD18
DPA_VDD10
DPA_PVDD
DPE_PVDD
DPCD_CALR
DPDE_CALR
DPAB_CALR
DPEF_CALR
R464 150/F_4
R465 150/F_4
R473 150/F_4
R622 EV@0_4
R621 PARK_MAD@0_4
R620 PARK_MAD@0_4
DPF
M92,M96-->NC
Madison,Park-->1.8V and GND
Quanta Computer Inc.
PROJECT : TE2
Madison/Park DPPW_GND
Rev 2A
Date: Tuesday, March 09, 2010
Sheet 20 of 45

PIN STRAPS



Memory Aperture size	
RAM_CFG[2:0]	Size
000	128MB
001	256MB
010	64MB
011	32MB

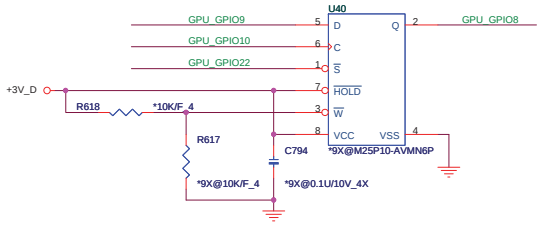
ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

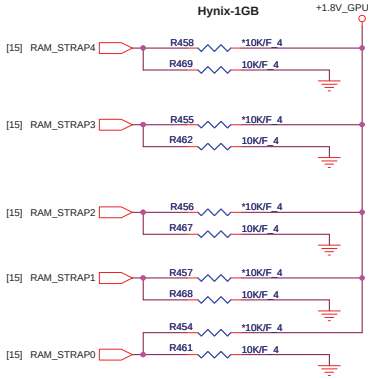
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA VIP: Video Capture Port Interface	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

EEPROM

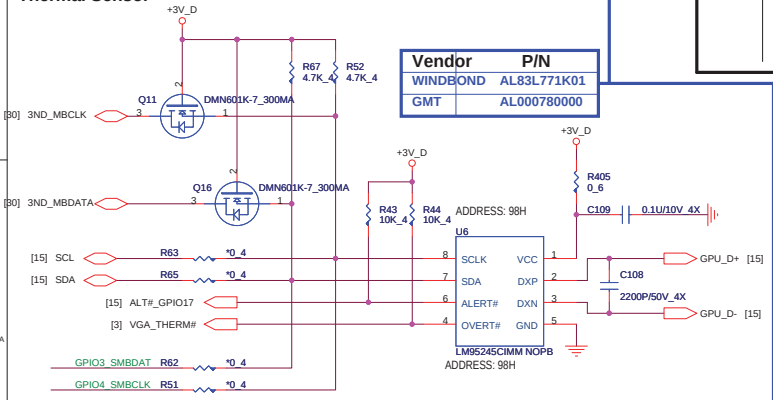


DDR3 Memory TYPE

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	RAM_STRAP4 15"	RAM_STRAP4 14"
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW00 (64M*16)	512MB	0	1	0	0	0	1
			1GB	0	0	0	0	0	1
Samsung	K4W1G1646E-HC12	AKD5LGGT502 (64M*16)	512MB	0	1	0	1	0	1
			1GB	0	0	0	1	0	1
									1



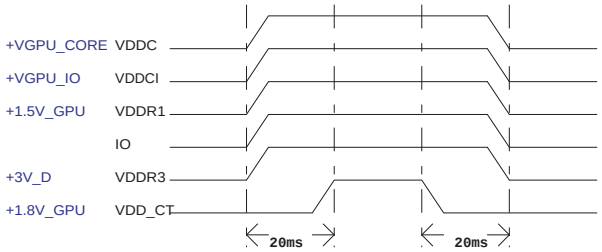
Thermal Sensor



Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

+1V

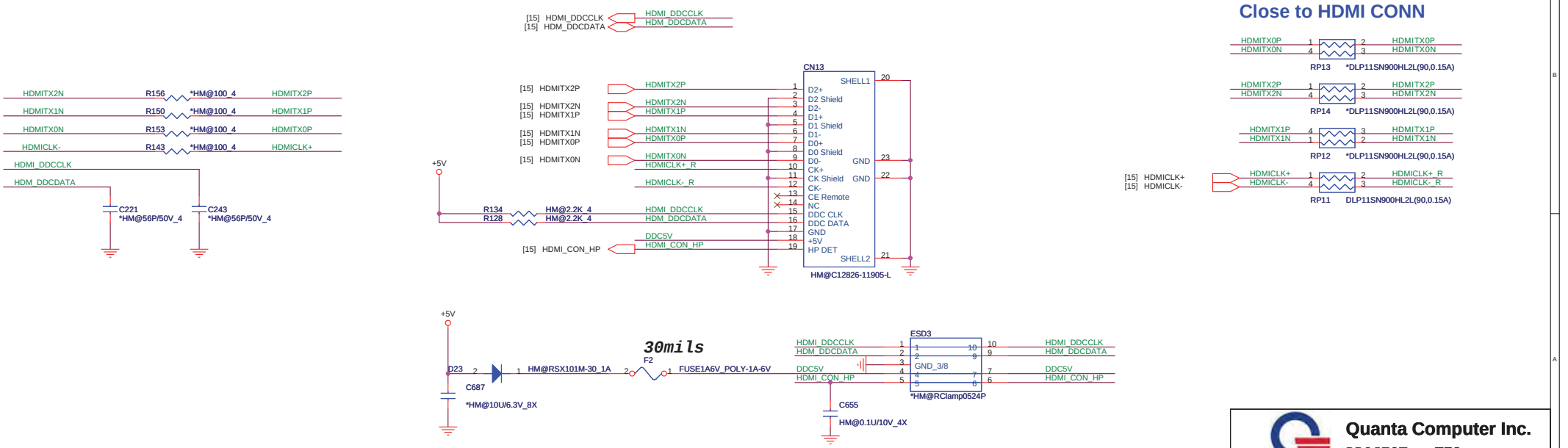
Power Up/Down Sequence



Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	Memory strip/Thermal/HDCP	2A
Date: Tuesday, March 09, 2010	Sheet 21 of 45	

HDMI Conn



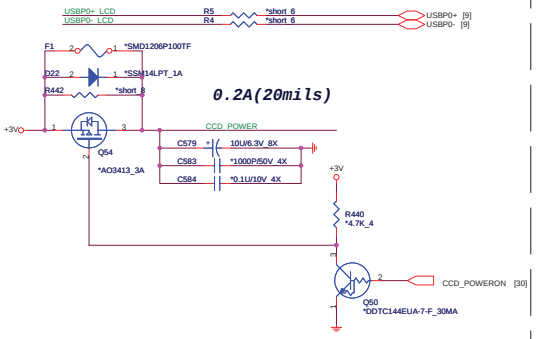
Quanta Computer Inc.

PROJECT : TE2

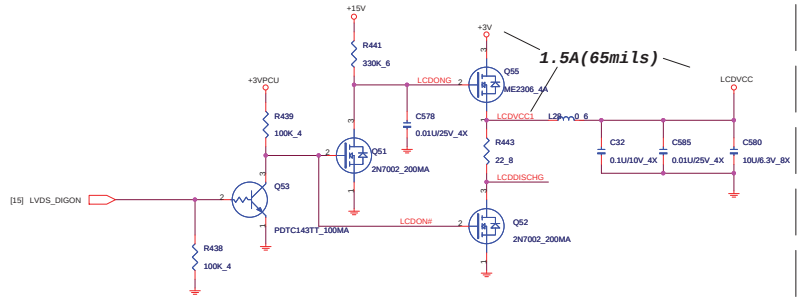
Size	Document Number	Rev
	HDMI CONN	2A

Date: Wednesday, March 10, 2010 Sheet 22 of 45

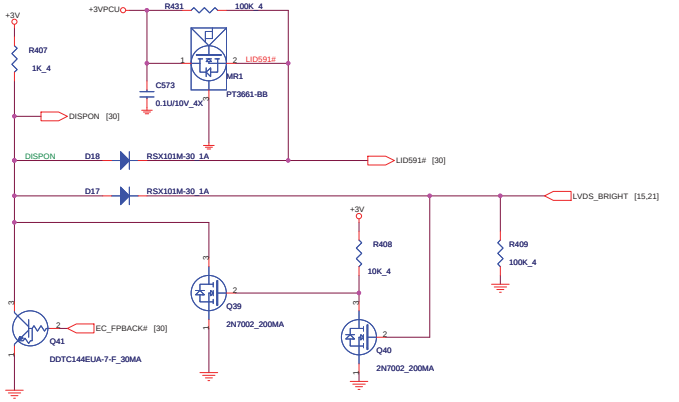
CCD [CCD]



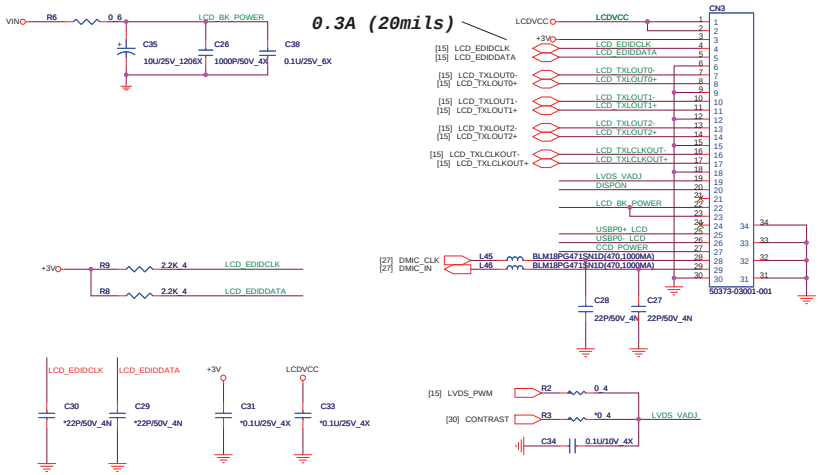
LCD POWER SWITCH [LDS]



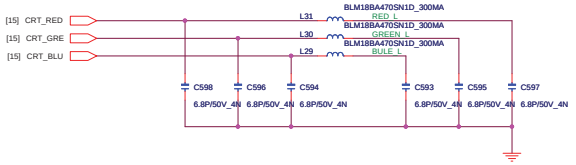
HALL SENSOR&BACK LIGHT SWITCH [HSR]

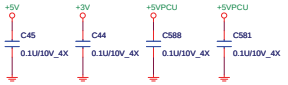


LCD Panel Module [LDS]

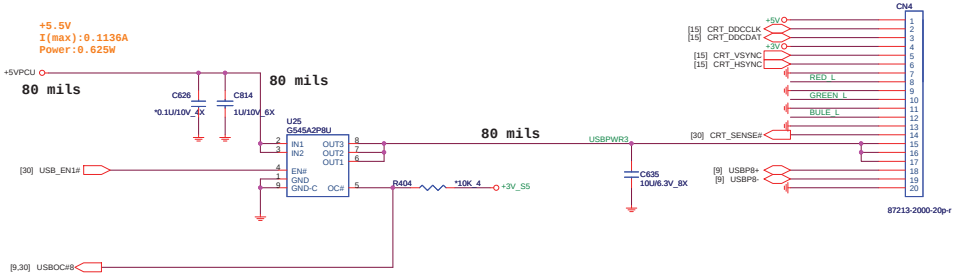


CRT [CRT]





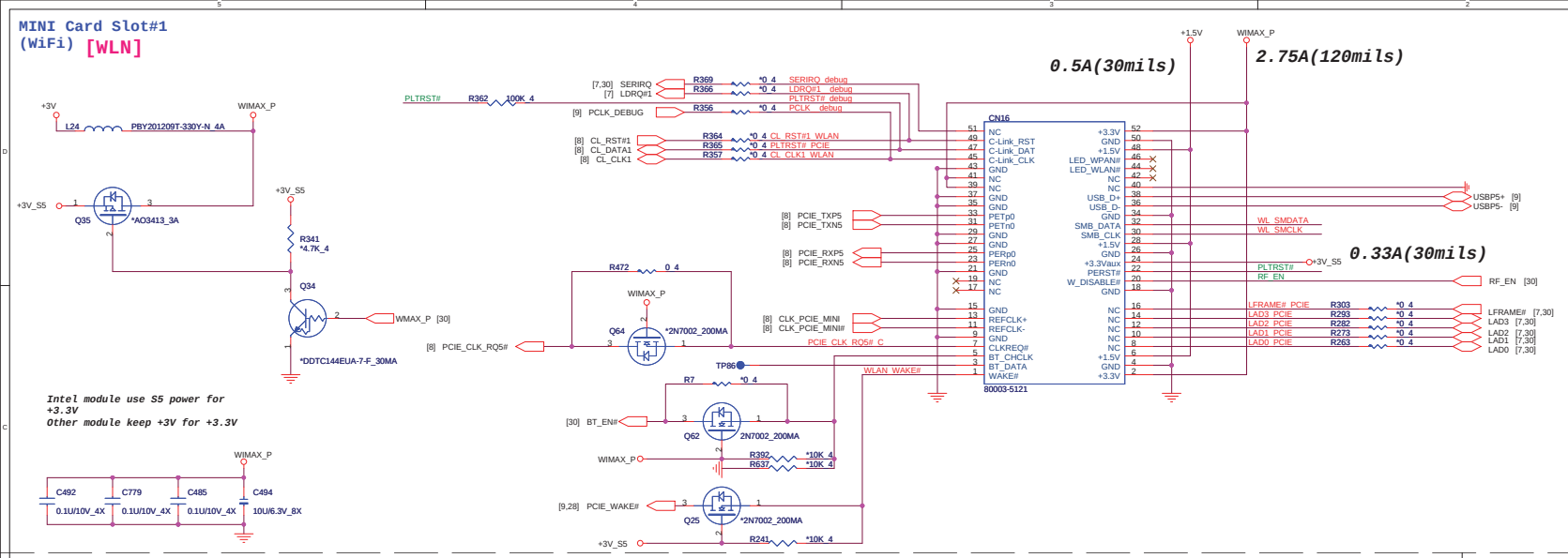
USB To CRT Board[USB]

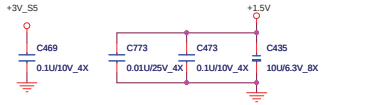


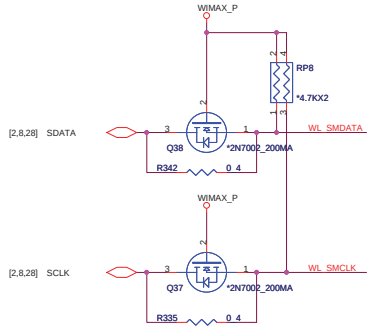
Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	LCD/LED Panel/CCD	2A
Date: Tuesday, March 09, 2010	Sheet 23 of 45	

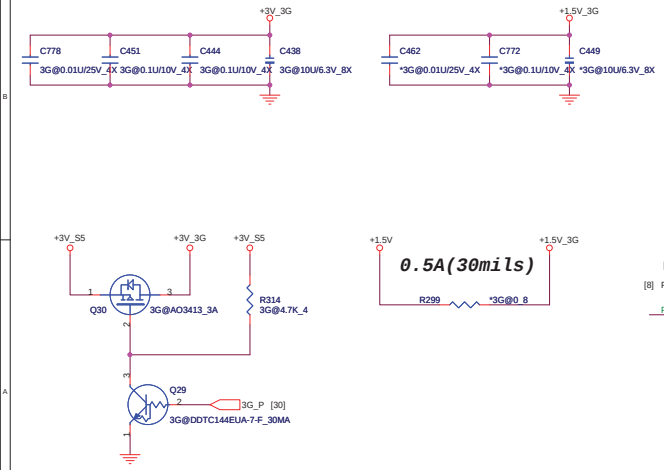
MINI Card Slot#1 (WiFi) [WLN]

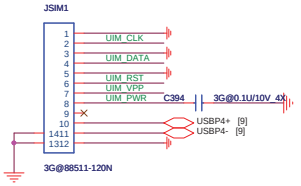






MINI Card Slot#2 3G [M3G]



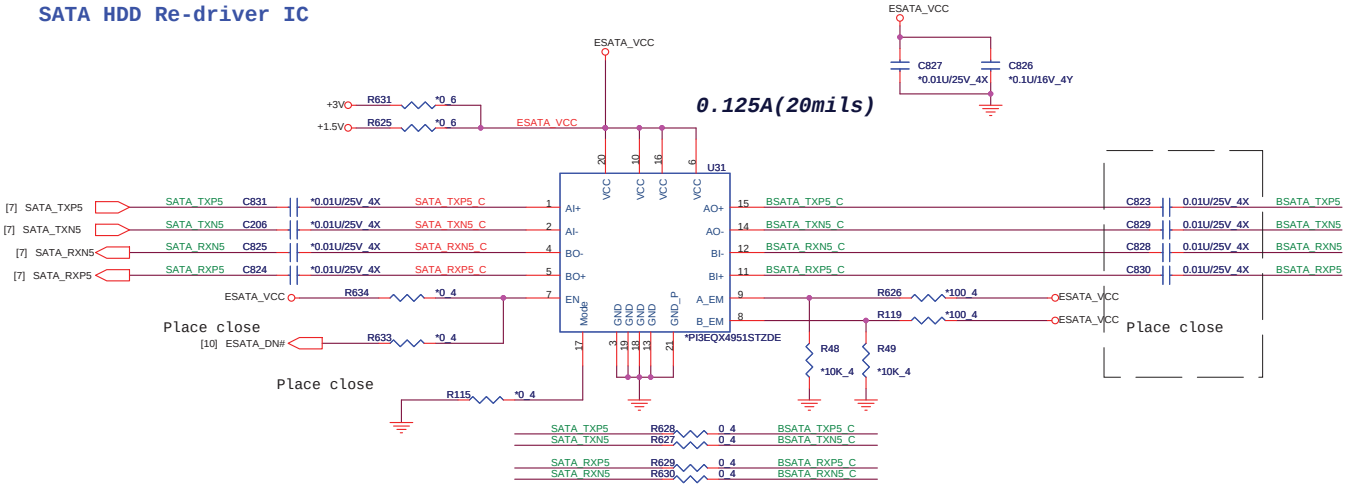


SIM CARD

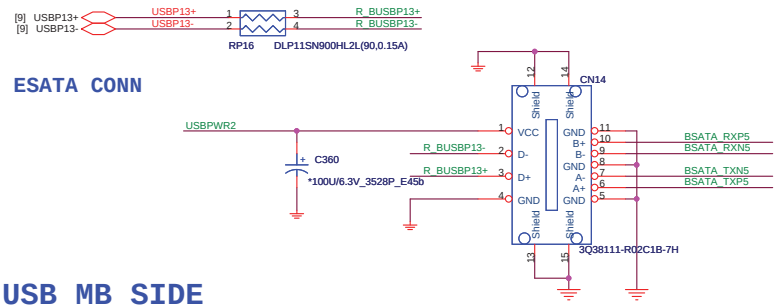
Quanta Computer Inc.
PROJECT : TE2
Size | Document Number: MINI CARD(WLAN/3G/SIM Card) | Rev 2A
Date: Friday, March 19, 2010 | Sheet 24 of 45

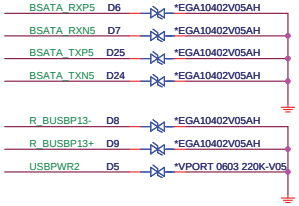
E-SATA [ESA]

SATA HDD Re-driver IC

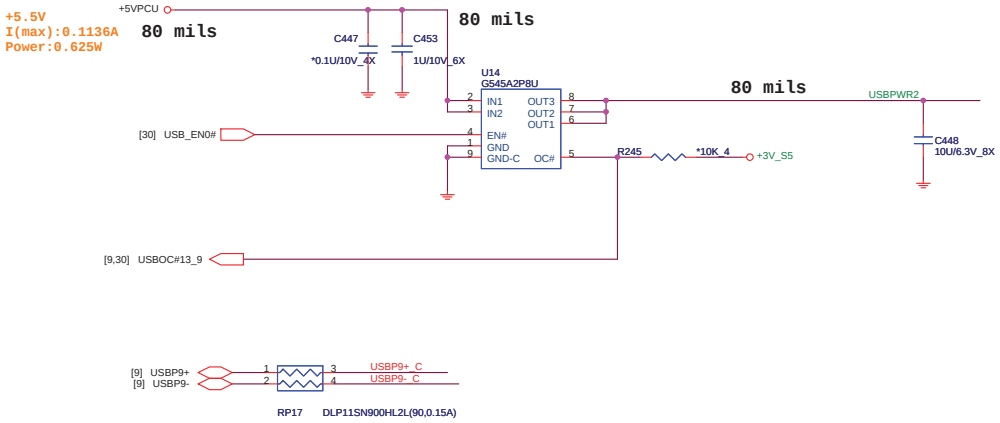


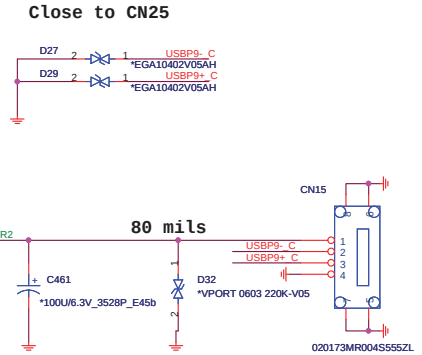
ESATA CONN





USB MB SIDE





Quanta Computer Inc.
PROJECT : TE2

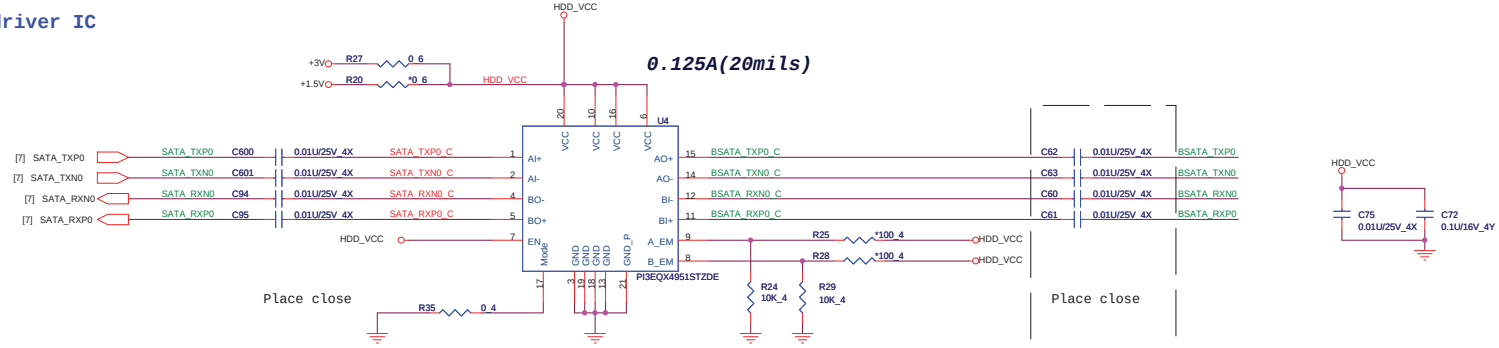
Size	Document Number	Rev
	TP/SW/ESATA/USB+Audio/LED	2A

Date: Tuesday, March 09, 2010 Sheet 25 of 45

SATA ODD

[ODD]

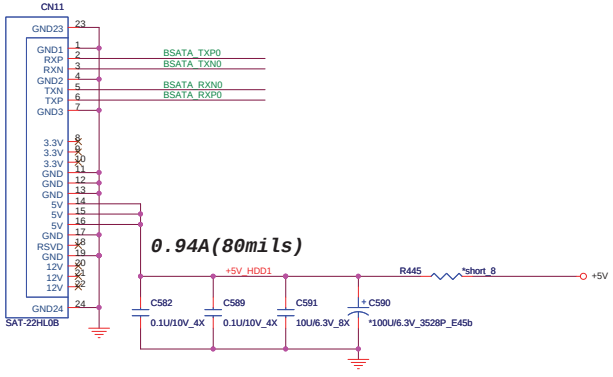
SATA HDD Re-driver IC



ESATA Re-driver Bypass

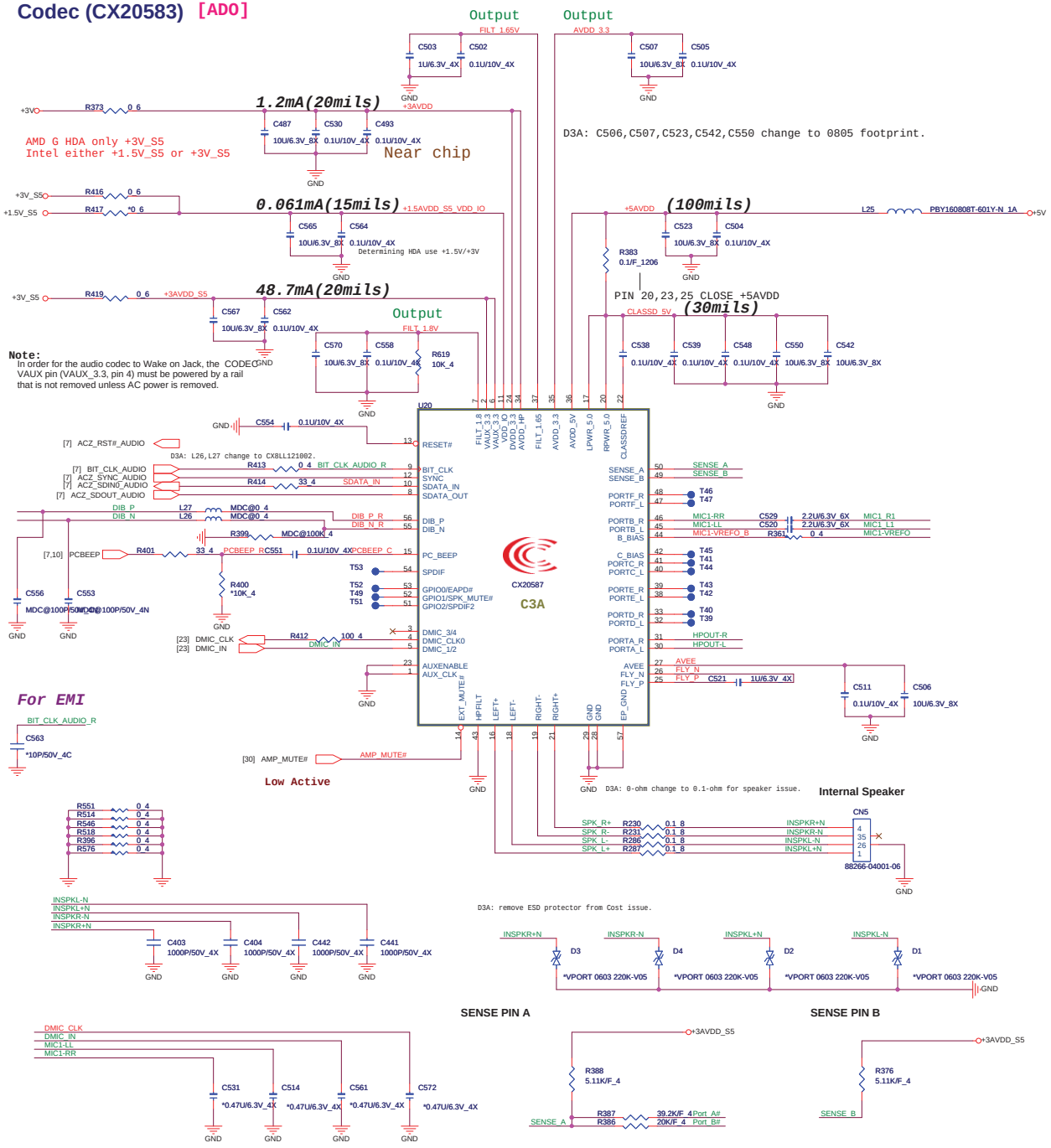
SATA HDD

[HDD]



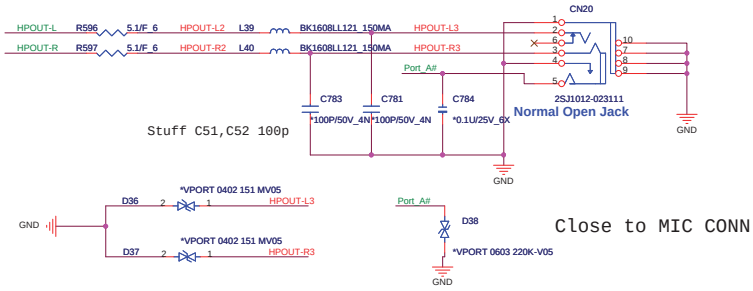
Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: HDD/ODD/MDC	Rev: 2A
Date: Tuesday, March 09, 2010	Sheet 26 of 45	

Codec (CX20583) [ADO]

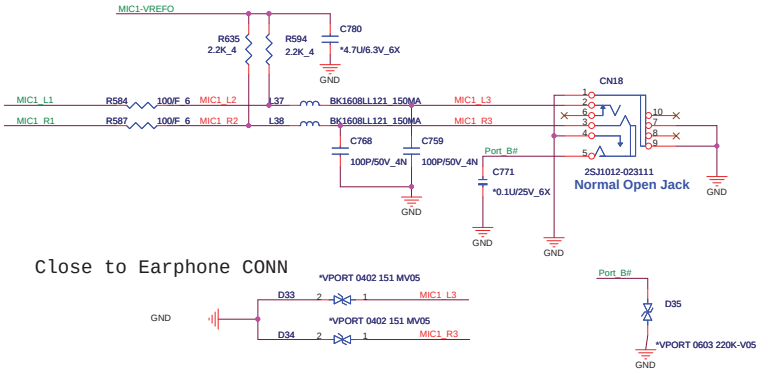


AUDIO JACK

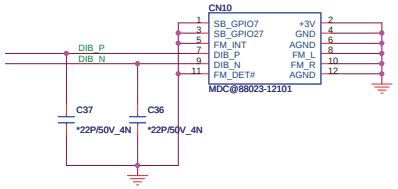
Earphone



External MIC



MDC

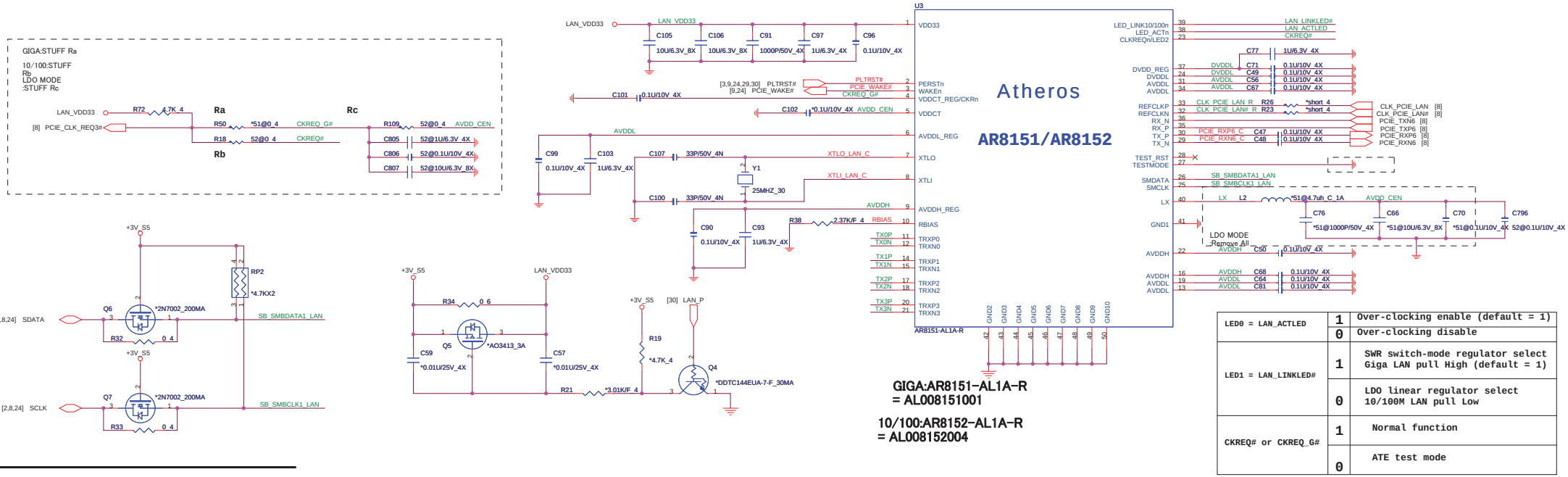


Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	Codec (CX20583)	2A

Date: Friday, March 19, 2010 Sheet 27 of 45

Atheros Lan

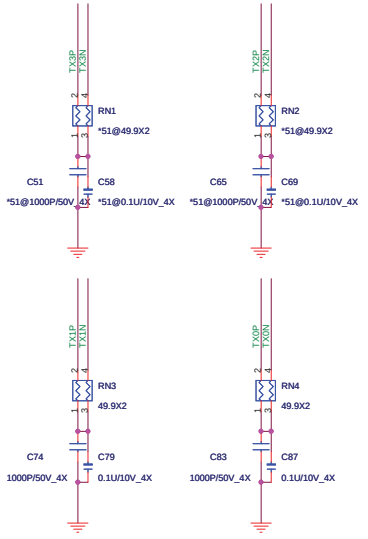


LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

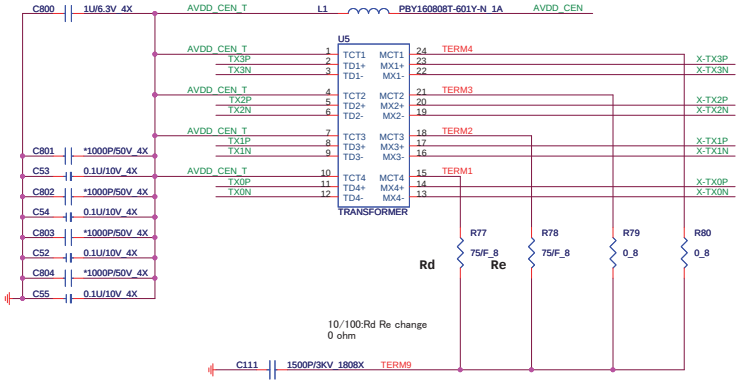
GIGA:AR8151-AL1A-R
= AL008151001

10/100:AR8152-AL1A-R
= AL008152004

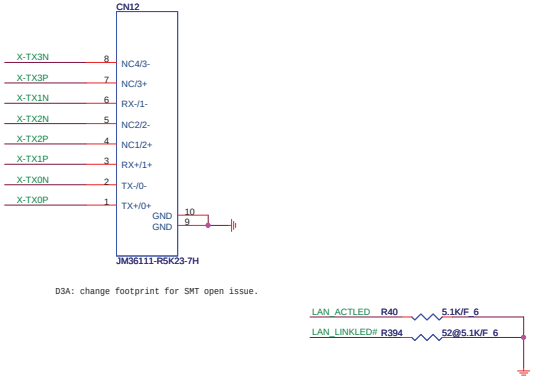
PLACE NEAR LAN IC SIDE



TRANSFORMER

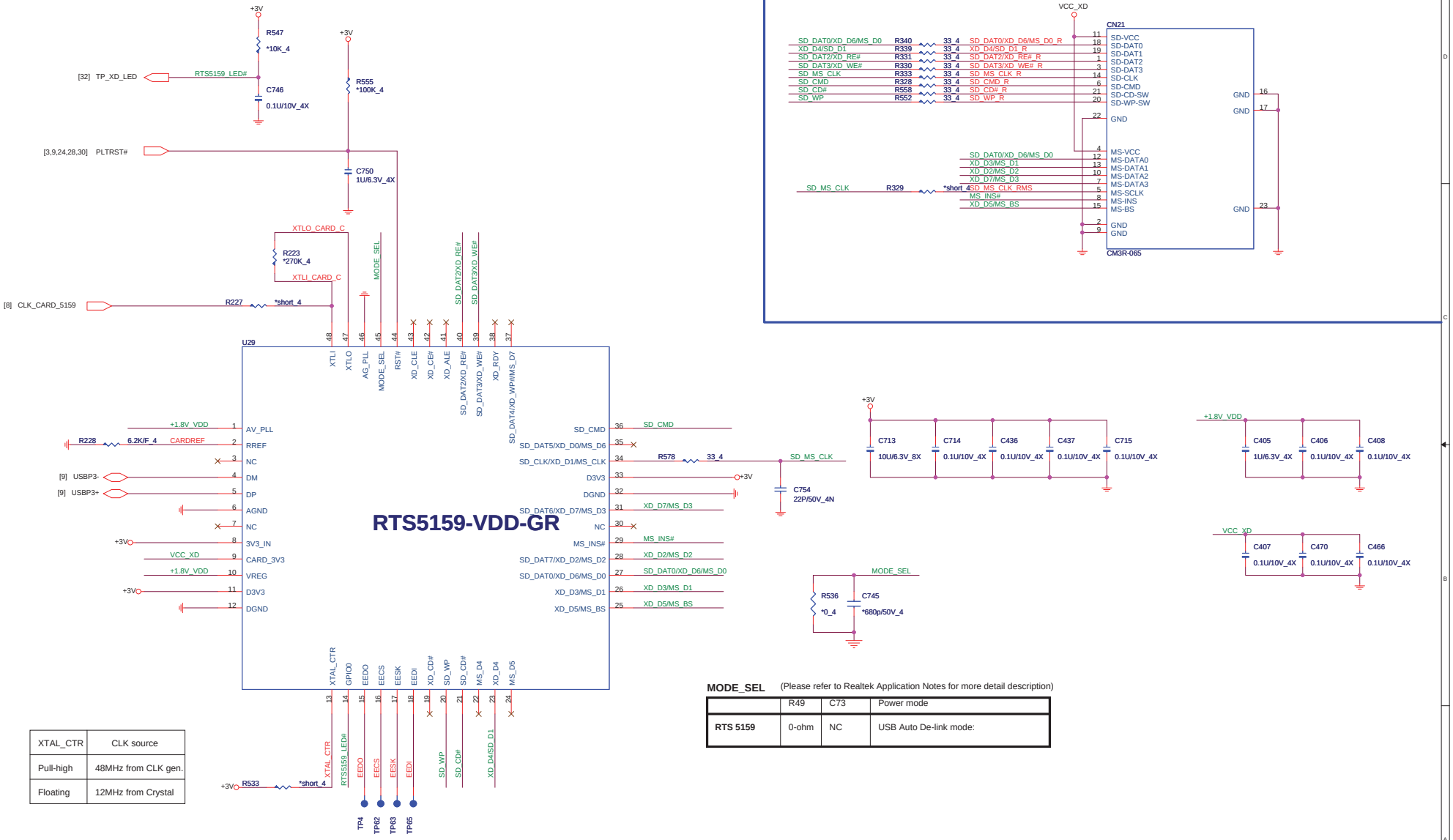


RJ45



Quanta Computer Inc.			
PROJECT : TE2			
Size	Document Number		Rev
	Atheros Lan		2A
Date:	Wednesday, March 10, 2010	Sheet 28 of 45	

3 IN 1 CARD READER



XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal

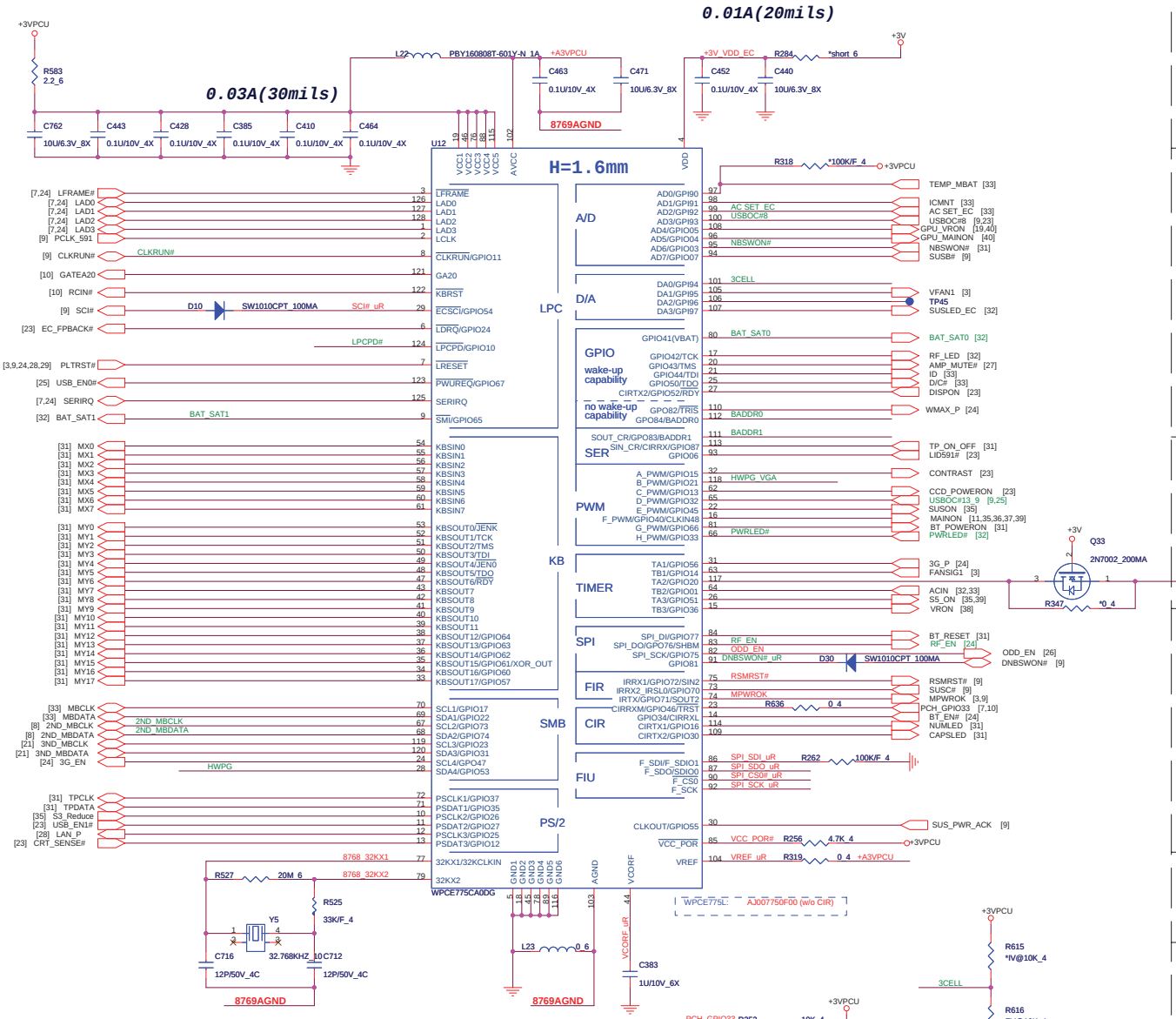
MODE_SEL (Please refer to Realtek Application Notes for more detail description)

	R49	C73	Power mode
RTS 5159	0-ohm	NC	USB Auto De-link mode:

3 IN 1 CARD READER

Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: RTS5159 (Card Reader)	Rev 2A
Date: Tuesday, March 09, 2010	Sheet 29 of 45	

EC [KBC]



SMBUS Table

SMBUS	Devices	Address
1	Battery	12H
2	CPU Board Thermal Sensor	98H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H

SM BUS PU

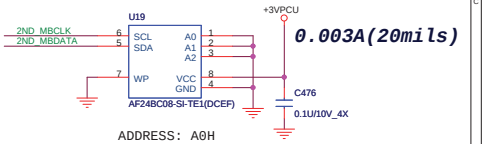
I/O Base Address

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

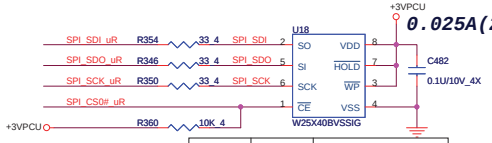
SHBM=0: Enable shared memory with host BIOS

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID

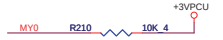


SPI FLASH

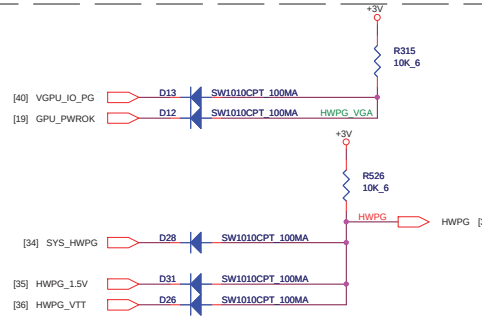


Intel	512KB	W25X40BVSSIG
AMD	2MB	W25Q16BVSSIG

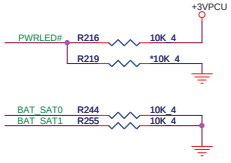
INTERNAL KEYBOARD STRIP SET



HWPG

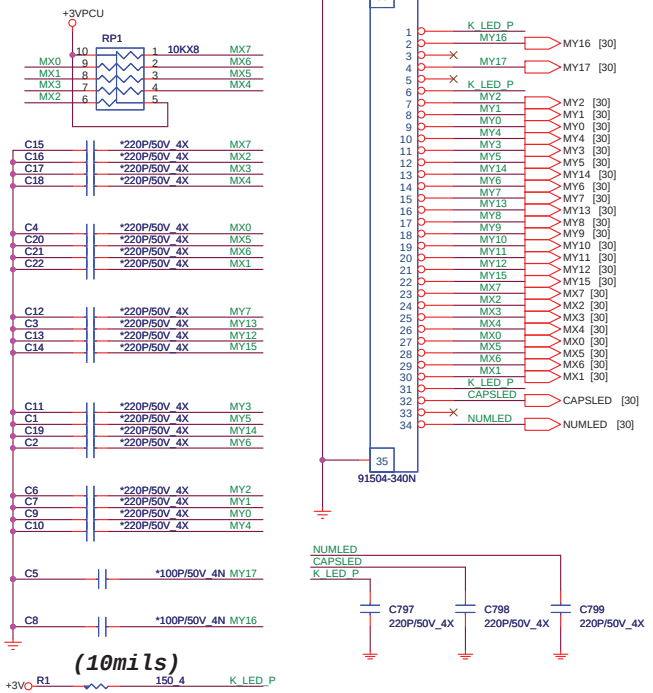


LED PU/PD

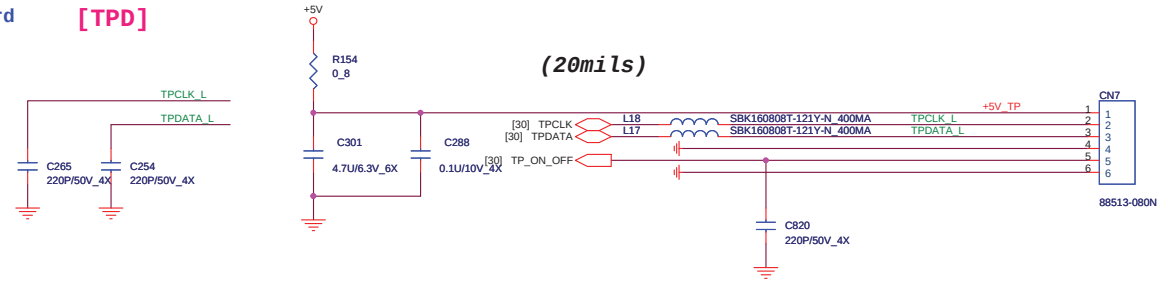


Quanta Computer Inc. PROJECT : TE2			
Size	Document Number		Rev
	EC-WPC8763LDG/WPC8769L(O)		2A
Date: Wednesday, March 10, 2010		Sheet 30 of 45	

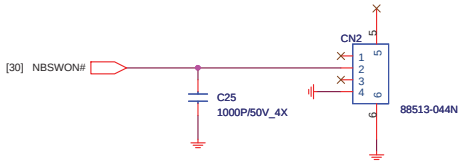
INT KeyBoard [KBC]



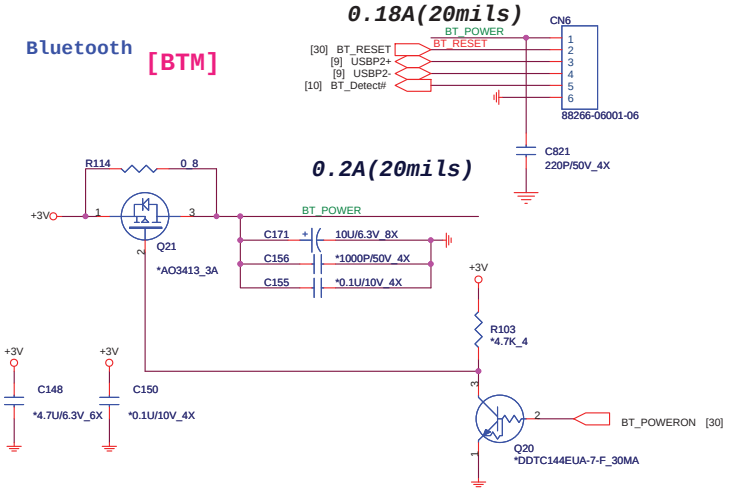
TP board [TPD]



Power board [PSW]

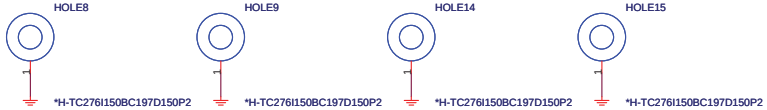


Bluetooth [BTM]

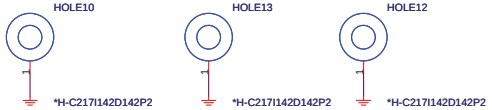


HOLE

CPU

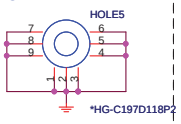


VGA

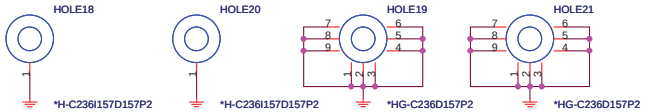


HDD&ODD

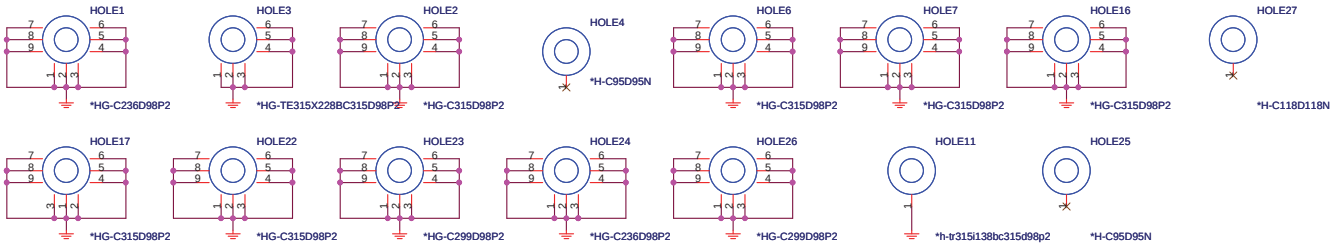
MDC



MINI CARD



EMI PAD



Quanta Computer Inc.

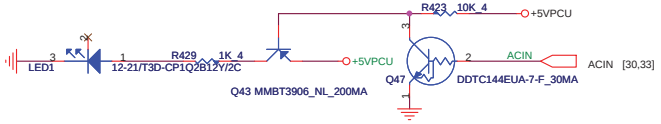
PROJECT : TE2

Size	Document Number	Rev
	KB/TP&TP/PB/FL/LEB/MMB/B-CAS	2A

Date: Wednesday, March 10, 2010 Sheet 31 of 45

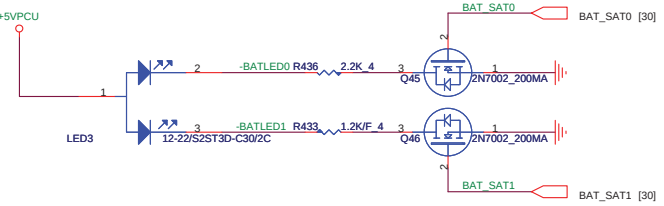
LED [LED]

AC-IN



BATERRY

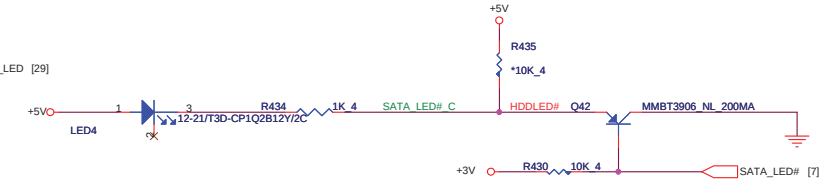
D3A : LED luminance to light,1K-ohm change 2.2K-ohm.



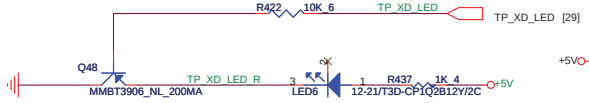
RF LED

D3A : LED luminance to light,560-ohm change 220-ohm.

HDD/ODD

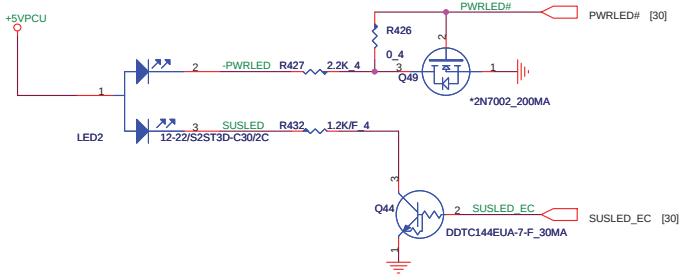


CARDREADER

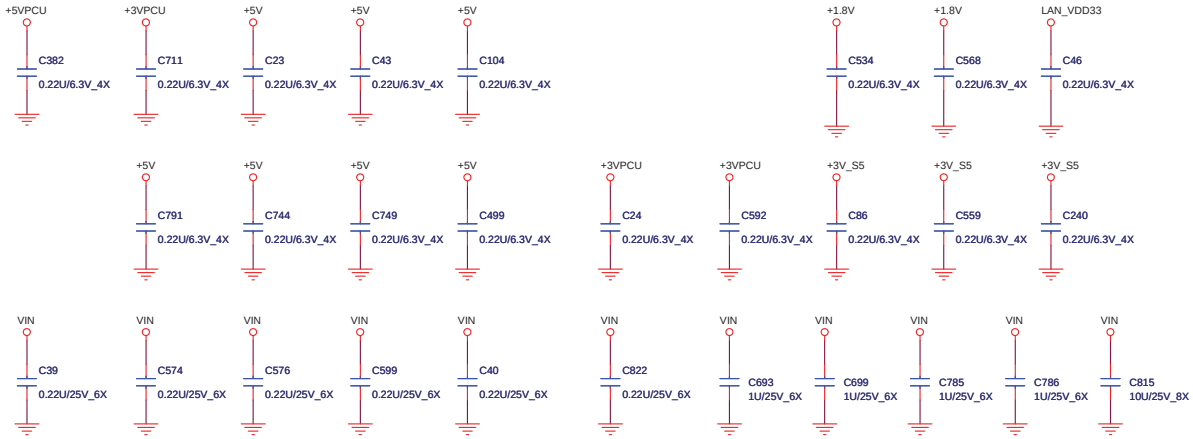


POWER

D3A : LED luminance to light,1K-ohm change 2.2K-ohm.

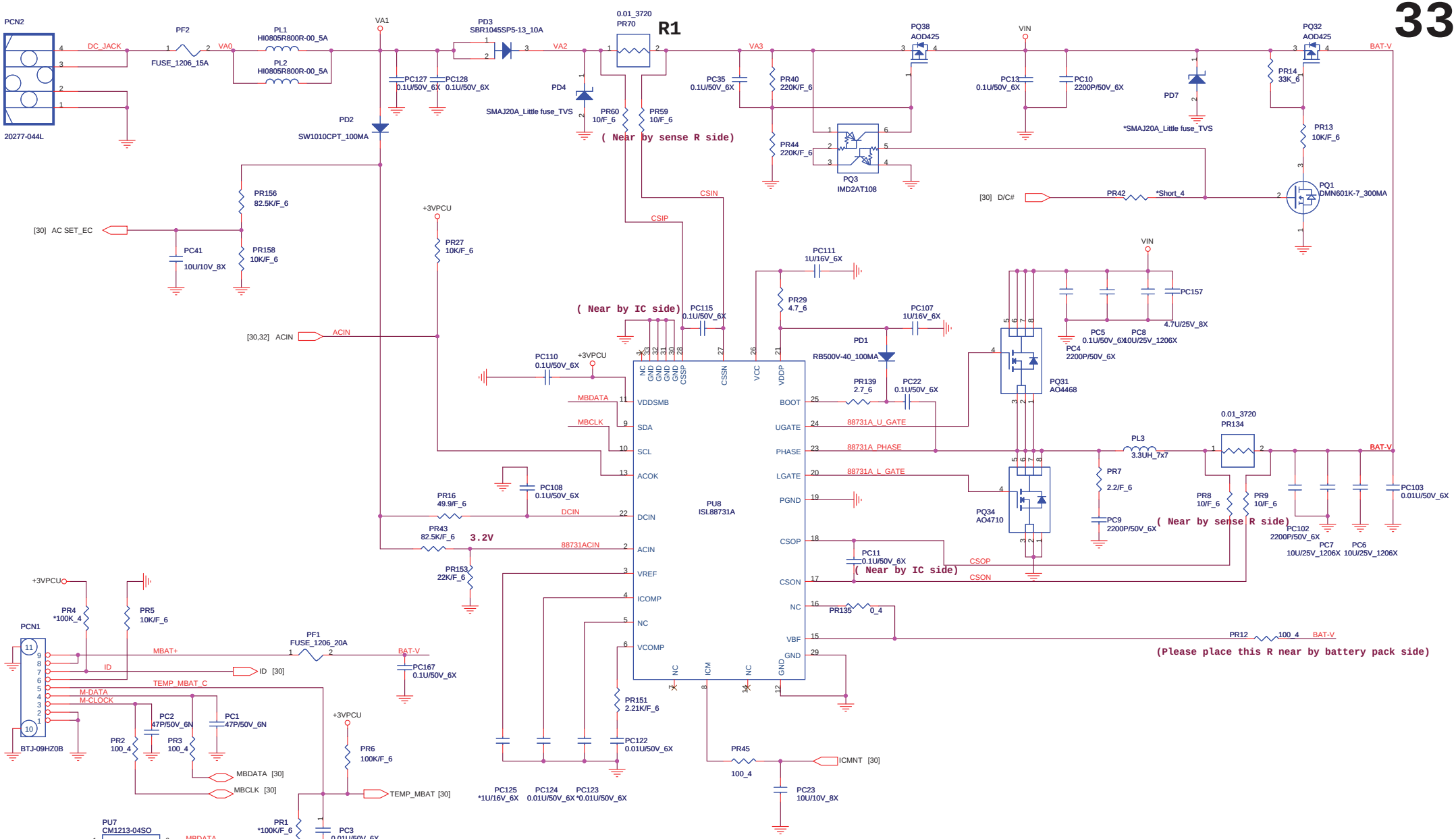


ESD Protect



Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	LED/HOLE	2A
Date: Tuesday, March 09, 2010	Sheet 32 of 45	



Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	Charger (ISL88731)	1A

Date: Wednesday, March 10, 2010 Sheet 33 of 43

For RT8210B or UP6184 0_4 & 10K_4

For ISL6237 ZD5.6V , 100K/F_4 & 200K/F_4

09/10/15

f : 400k Hz
ESR : 17mΩ
Total capacitor : 370 uF
(Peak 10.2 ,AVG 8.135A)
OCP:11A

f : 500k Hz
ESR : 17mΩ
Total capacitor : 342uF
(Peak 9A, AVG 7.623A)
OCP:11.055~11.345A

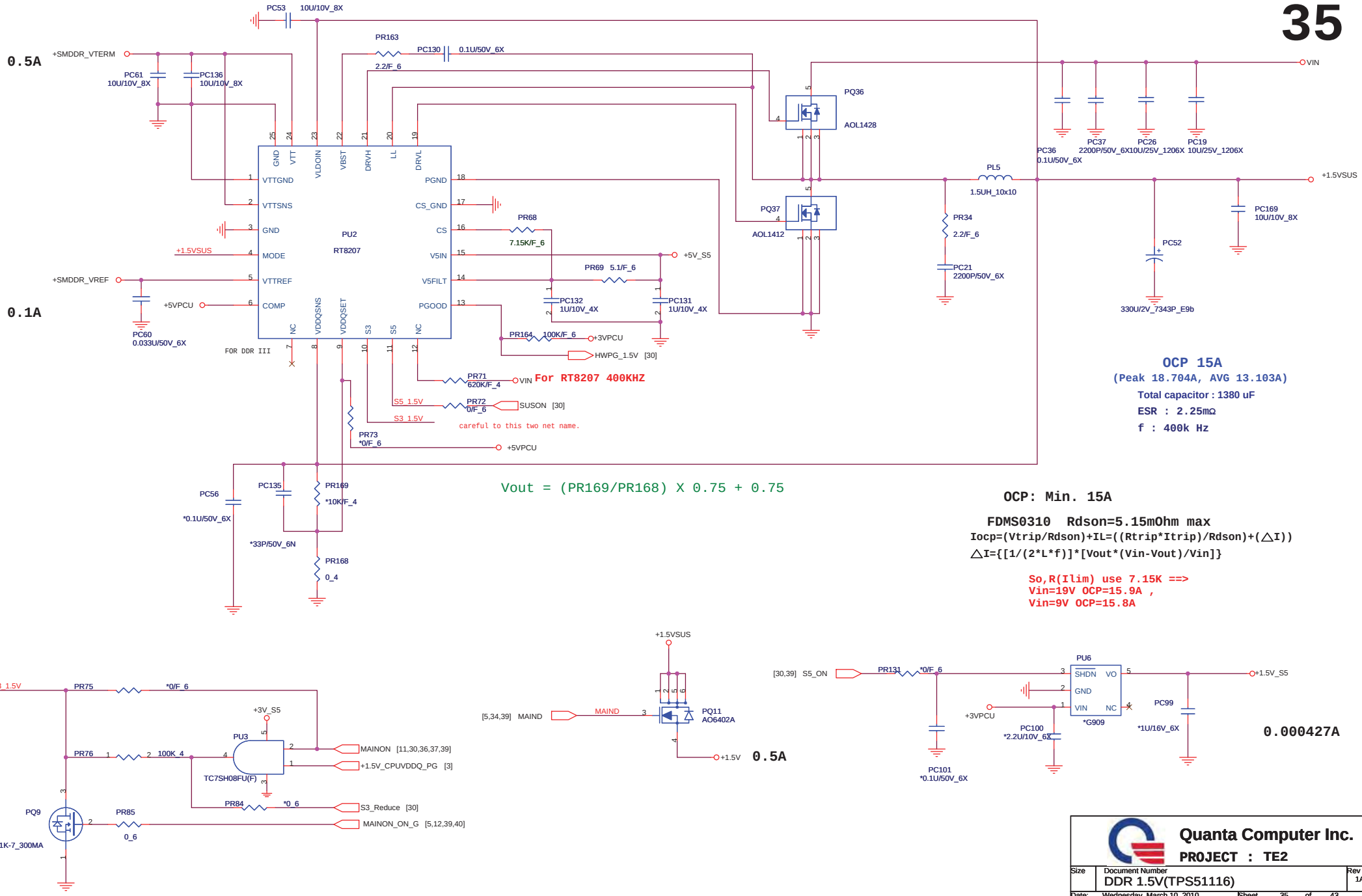
OCP:11.12~11.9525A
AO4710 Rdson=14.2mOhm.max.
△I=[(Vin-Vout)*Vout]/Vin*L*f
Iocp=OCP-(△I/2)
Vth*10=R(Ilim)*5uA
So,R(Ilim) use 2870 ==>
Vin=19V OCP=11.9525A ,
Vin=9V OCP=11.12A

F=500K
Rilim=Ilim*LRdson*10/5uA

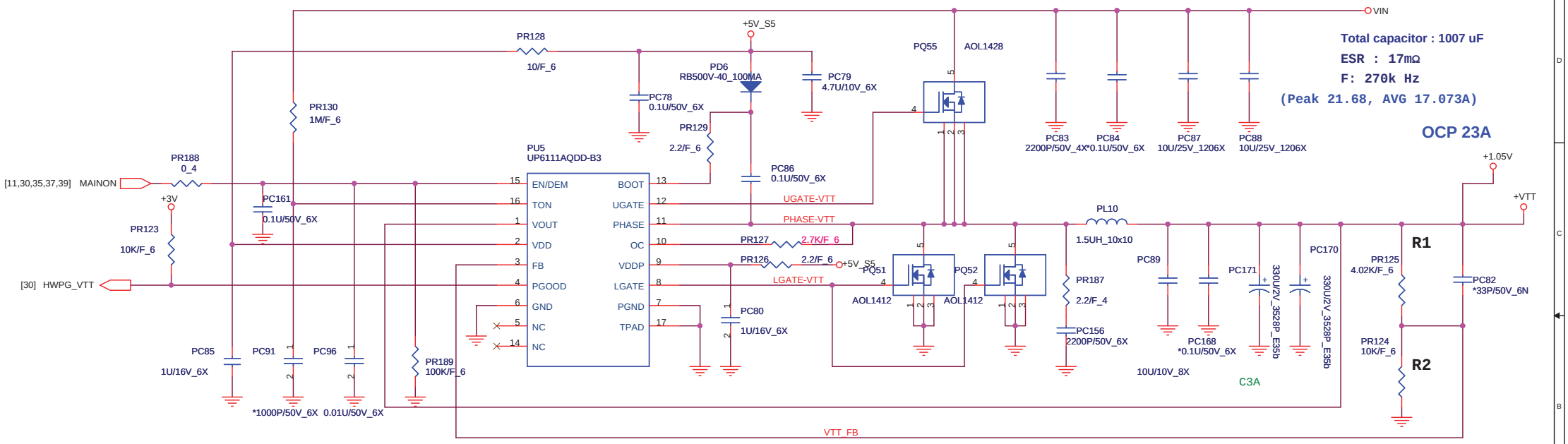
OCP:11.055~11.345A
AO4710 Rdson=14.2mOhm.max.
△I=[(Vin-Vout)*Vout]/Vin*L*f
Iocp=OCP-(△I/2)
Vth*10=R(Ilim)*5uA
So,R(Ilim) use 287K ==>
Vin=19V OCP=11.345A ,
Vin=9V OCP=11.055A

11A
2.834A
4.523A
4.984A
0.001A

Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: System 3V/5V(RT8210B)	Rev 1A
Date: Wednesday, March 10, 2010	Sheet 34 of 43	



Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: DDR 1.5V(TPS51116)	Rev: 1A
Date: Wednesday, March 10, 2010	Sheet 35 of 43	



VOUT=(1+R1/R2)*0.75

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

OCP:23.18~23.27A

FDMS0310 Rdson=5.15mOhm max

Iocp=(Vtrip/Rdson)+IL=((Rtrip*Itrip)/Rdson)+(△I))

△I={[1/(2*L*f)]*[Vout*(Vin-Vout)/Vin]}

Rdson*OCP=RIlim*20uA

So,R(Ilim) use 2.7K ==>

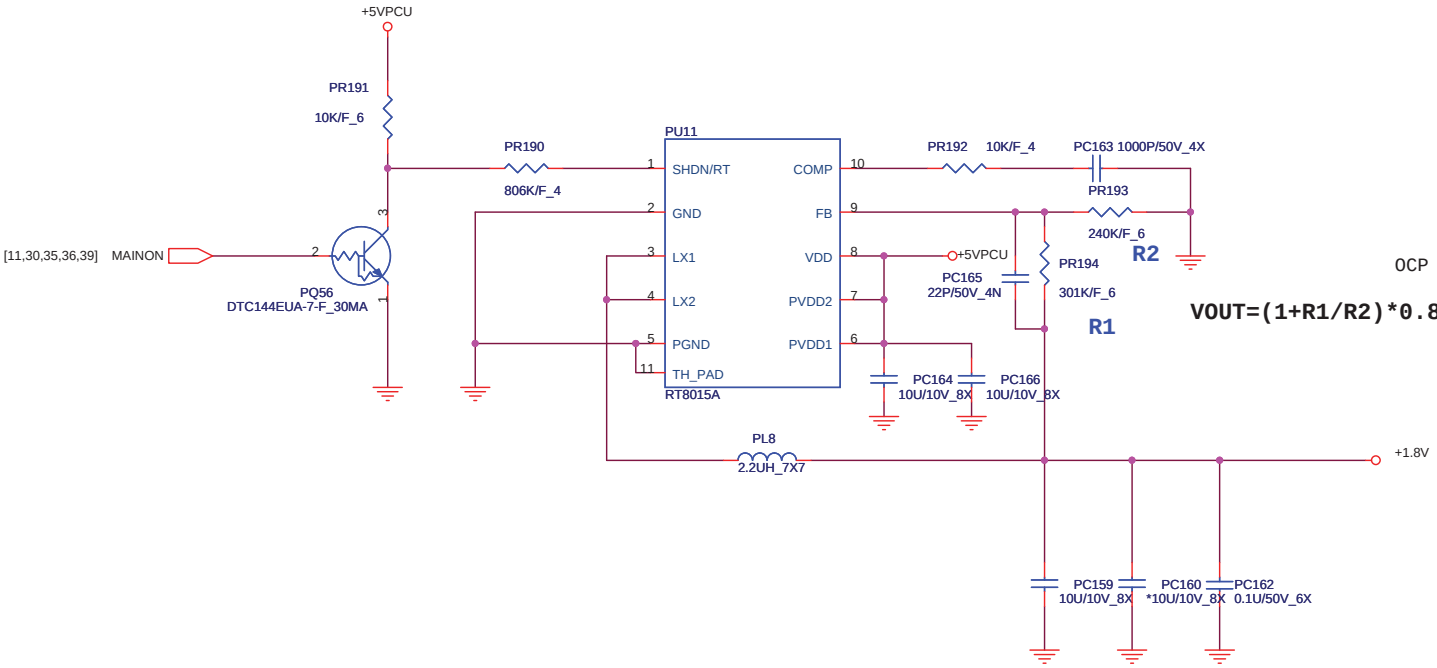
Vin=19V OCP=23.18A ,

Vin=9V OCP=23.27A

Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	+VTT (UP6111A)	1A
Date: Wednesday, March 10, 2010	Sheet 36 of 43	

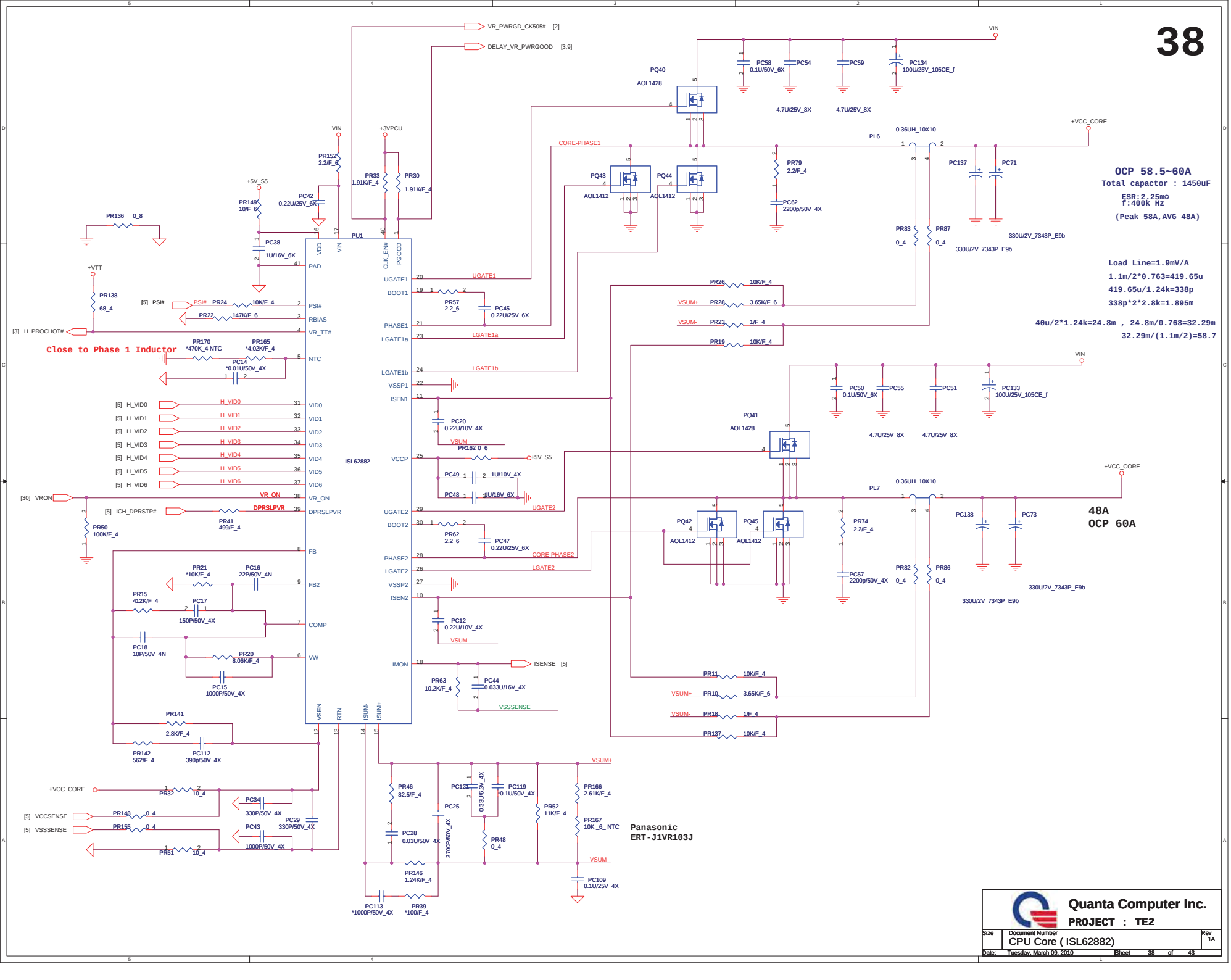


OCP Fellow IC spec~3.7A

VOUT=(1+R1/R2)*0.8

FOR UMA 0.194A
For VGA 1.345A

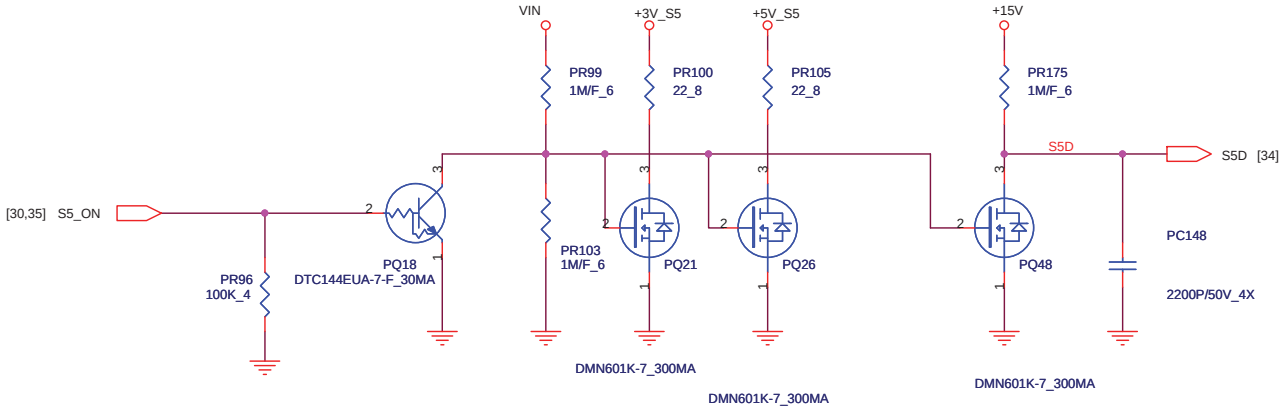
Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: +1.8V (RT8015A)	Rev: 1A
Date: Wednesday, March 10, 2010	Sheet 37 of 43	

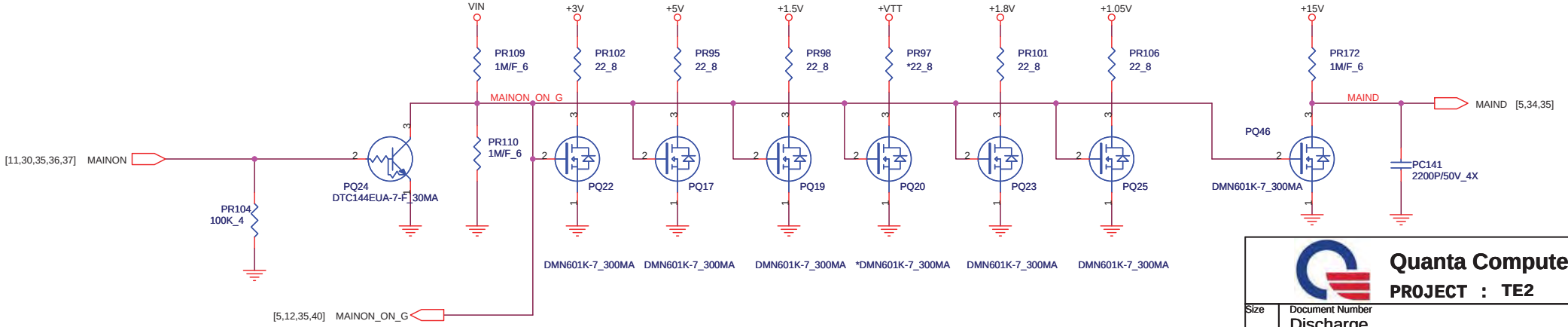


Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	CPU Core (ISL62882)	1A

Date: Tuesday, March 09, 2010 Sheet 38 of 43

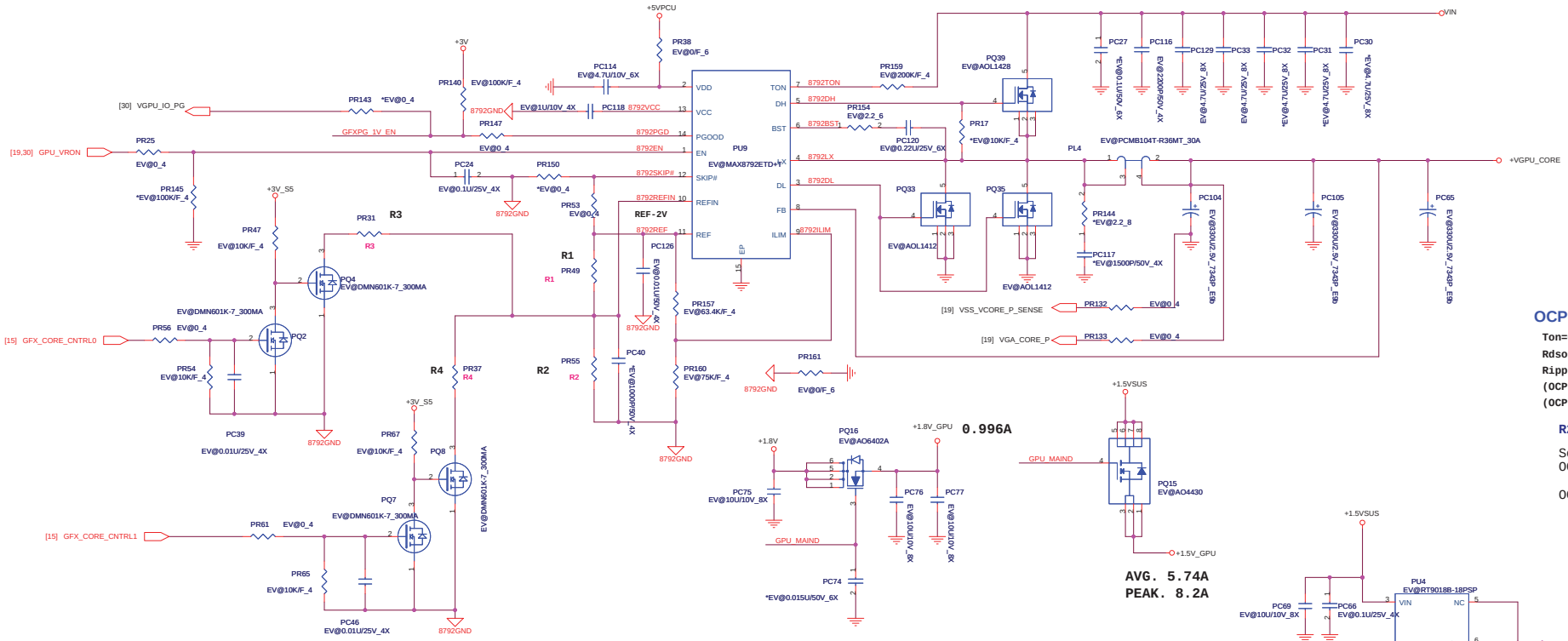




Quanta Computer Inc.

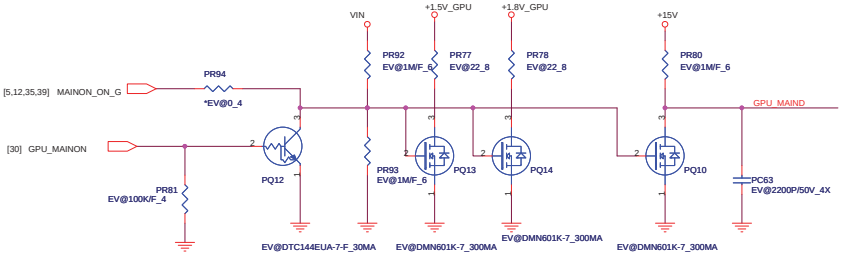
PROJECT : TE2

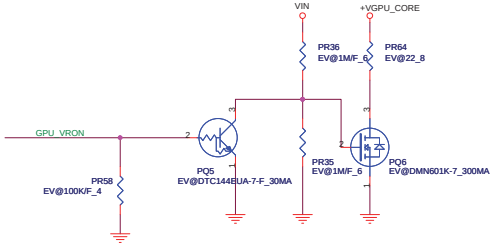
Size	Document Number	Rev
	Discharge	1A
Date: Thursday, February 25, 2010	Sheet 39 of 43	



GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	Madison/Park	M92	M96
LOW	LOW	0.9V	0.9V	0.95V
HIGH	LOW	0.95V	0.95V	0.95V
LOW	HIGH	1.12V	1.1V	1.0V
HIGH	HIGH	N/A	1.2V	1.1V

		Madison/Park	M92	M96
R1	PR49	39.2K CS33922FB15	39.2K CS33922FB15	39.2K CS33922FB15
R2	PR55	60.4K CS36042FB10	60.4K CS36042FB10	49.9K CS34992FB10
R3	PR31	309K CS43092FB16	270K CS42702FB10	249K CS42492FB18
R4	PR37	88.7K CS38872FB18	93.1K CS39312FB15	140K CS41402FB14





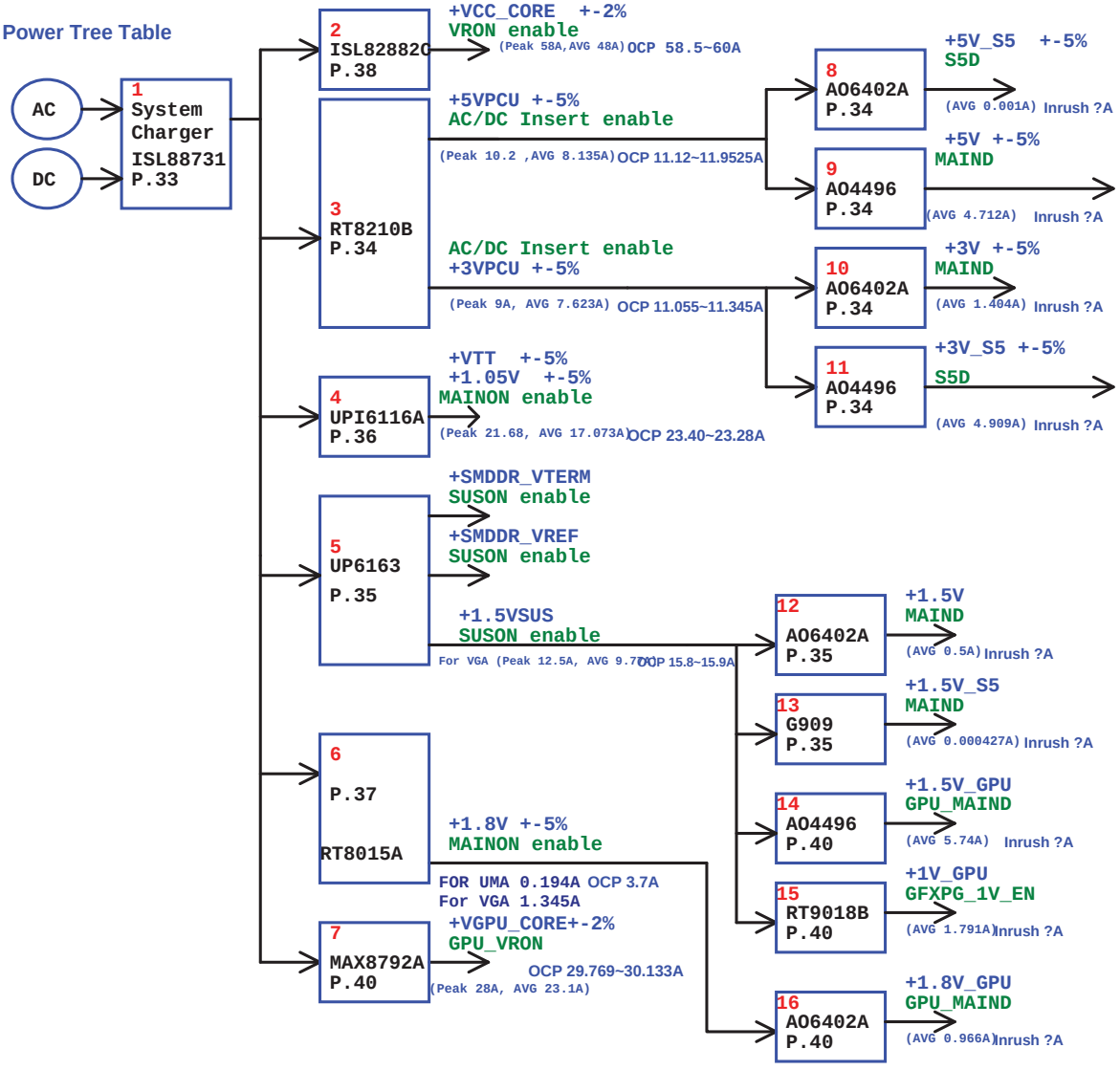
PCIE_VDDC
M92,M96-->1.1V
Madison,Park-->1.0V

	Madison,Park	M92,M96
PR91	25.5K/F_4 (CS32552FB11)	39.2K/F_4 (CS33922FB15)
PR89	100K/F_4 (CS41002FB28)	100K/F_4 (CS41002FB28)

Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	+VGPU_CORE(MAX8792)	1A
Date: Wednesday, March 10, 2010	Sheet 40 of 43	

Power Tree Table



Power Distribution List

Power	Distribution

Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	Power Tree Table	2A

Date: Thursday, February 25, 2010 Sheet 41 of 43

Table of Contents

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
+5V_TMA	+5V	MAIN_ON	S0
WIMAX_P	+3.3V	WMAX_P for EC	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_S5	+1.5V	S5_ON	S0~S5
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V~+1.1V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		GFXVR_EN	S0

GND PLANE	PAGE
GND_SIGNAL	32
CARD_GND	21
AGND_DC/DC	31
GND	ALL

Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	POWER STAGE AND BOI-FUNCTION	2A

Date: Thursday, February 25, 2010 Sheet 42 of 43

Model	REV	CHANGE LIST
TE2D MB	B2A	PAGE (16) : Add BT_EN# for combo RF control for BT PAGE (27) : Change DDR S3_1.5V ON circuit.
	C3A	PAGE (07) : Add ESATA re-driver IC
	D3A	PAGE(32) : LED luminance to light,R436、R427 1K-ohm change 2.2K-ohm. PAGE(32) : LED luminance too low,R428 560-ohm change 220-ohm. PAGE(27) : Add R230,R231,R286,R287 0.1-ohm to avoid speaker burn. PAGE(16):Add Q62 to avoid leakage current.

MODEL TE2

PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	

DOC NO. 204					
PROJECT MODEL :	TE2	APPROVED BY:	Mosy Li	DATE:	2009/10/27
PART NUMBER:		DRAWING BY:	Mosy Li	REVISON:	1A

Quanta Computer Inc.
PROJECT : TE2
Size | Document Number: Change list | Rev 2A
Date: Friday, March 19, 2010 | Sheet 31 of 33