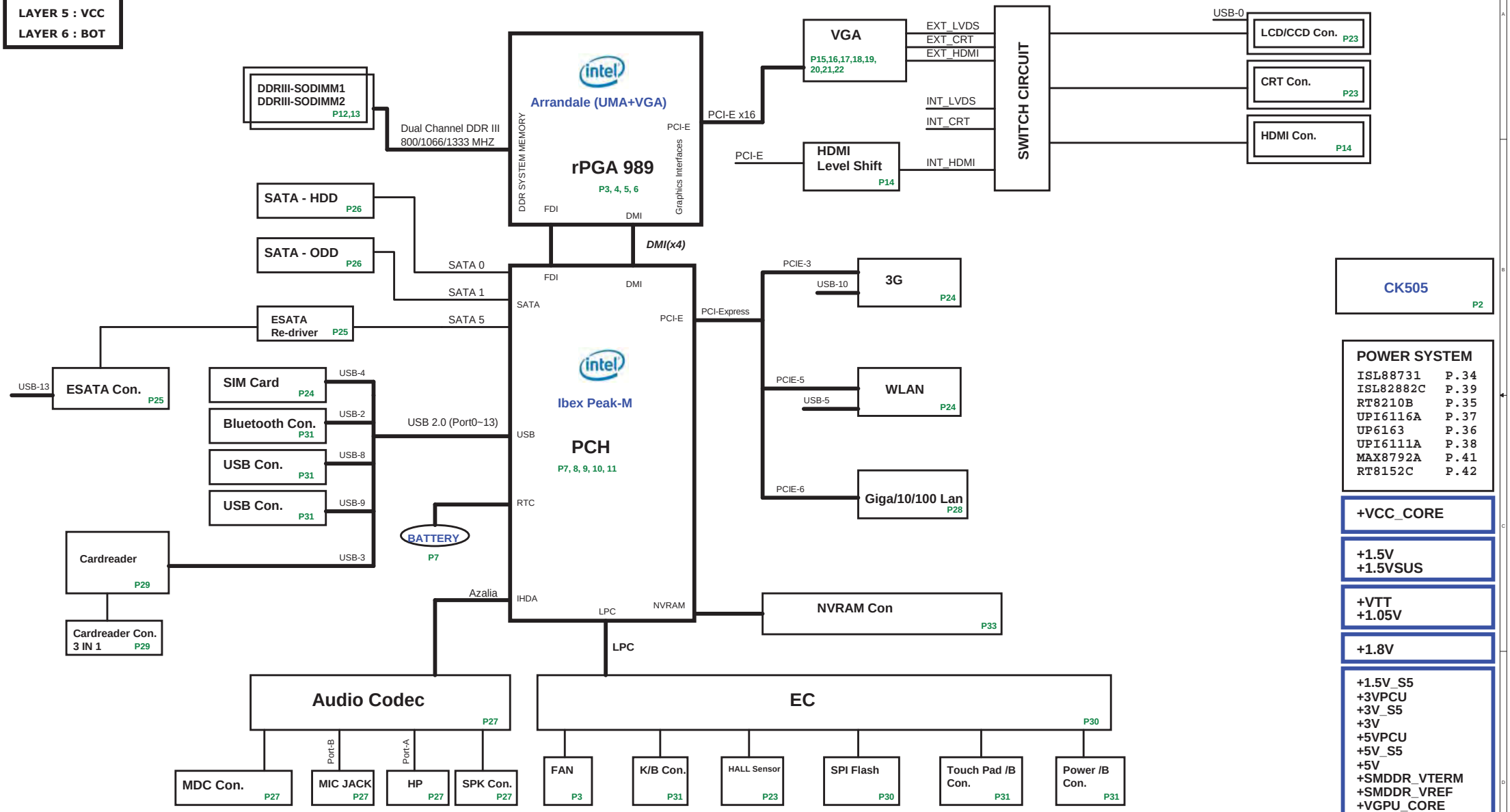
BL6 Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT



CK505 P2

POWER SYSTEM

ISL88731	P.34
ISL82882C	P.39
RT8210B	P.35
UPI6116A	P.37
UP6163	P.36
UPI6111A	P.38
MAX8792A	P.41
RT8152C	P.42

+VCC_CORE

+1.5V
+1.5VSUS

+VTT
+1.05V

+1.8V

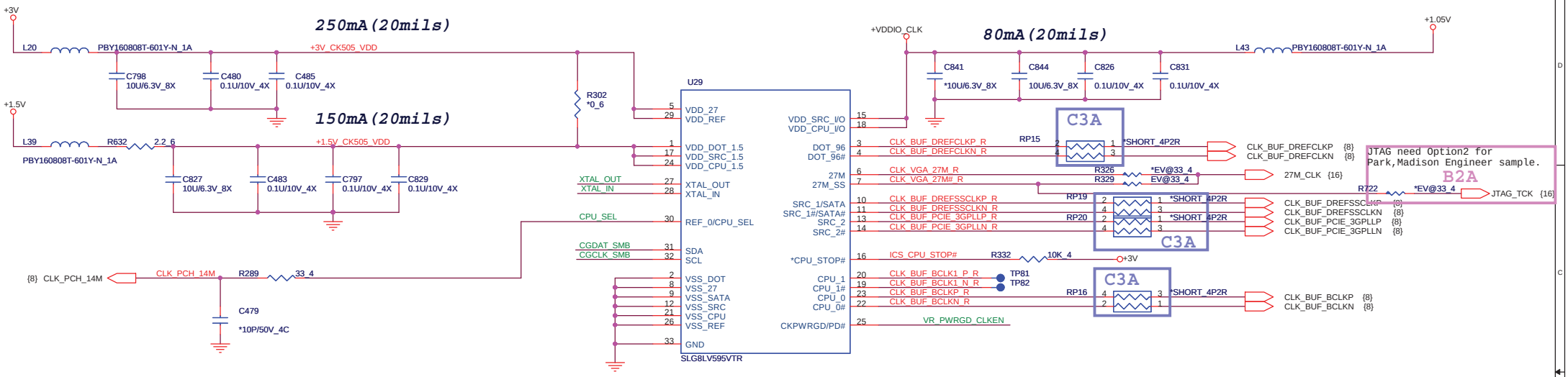
+1.5V_S5
+3VPCU
+3V_S5
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF
+VGPU_CORE
+VAXG

Quanta Computer Inc.
PROJECT : BL6

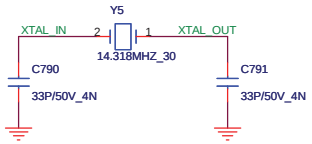
Size	Document Number	Rev
	Block Diagram	A1A

Date: Wednesday, April 07, 2010 Sheet 1 of 45

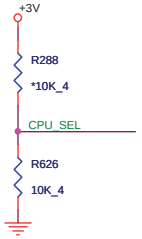
CLOCK Gen



CLK CRYSTAL

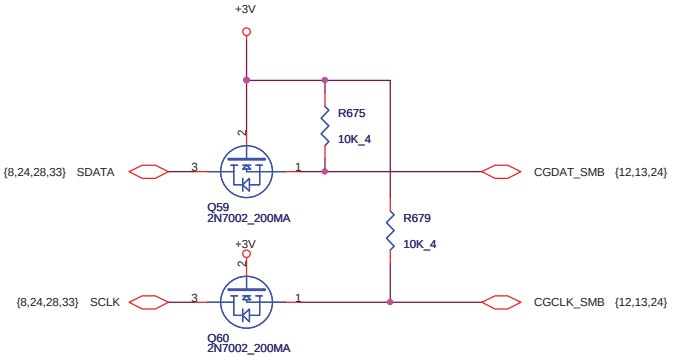


CLK CPU_SEL



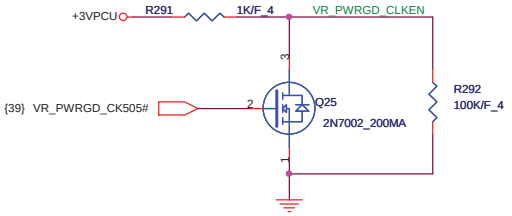
	0	1
CPU_SEL	CPU =133MHz (default)	CPU=100MHz

CLK I2C



CLK POWERGOOD

Change to +3VPCU
(follow CRB)



Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	CLOCK GENERATOR	A1A
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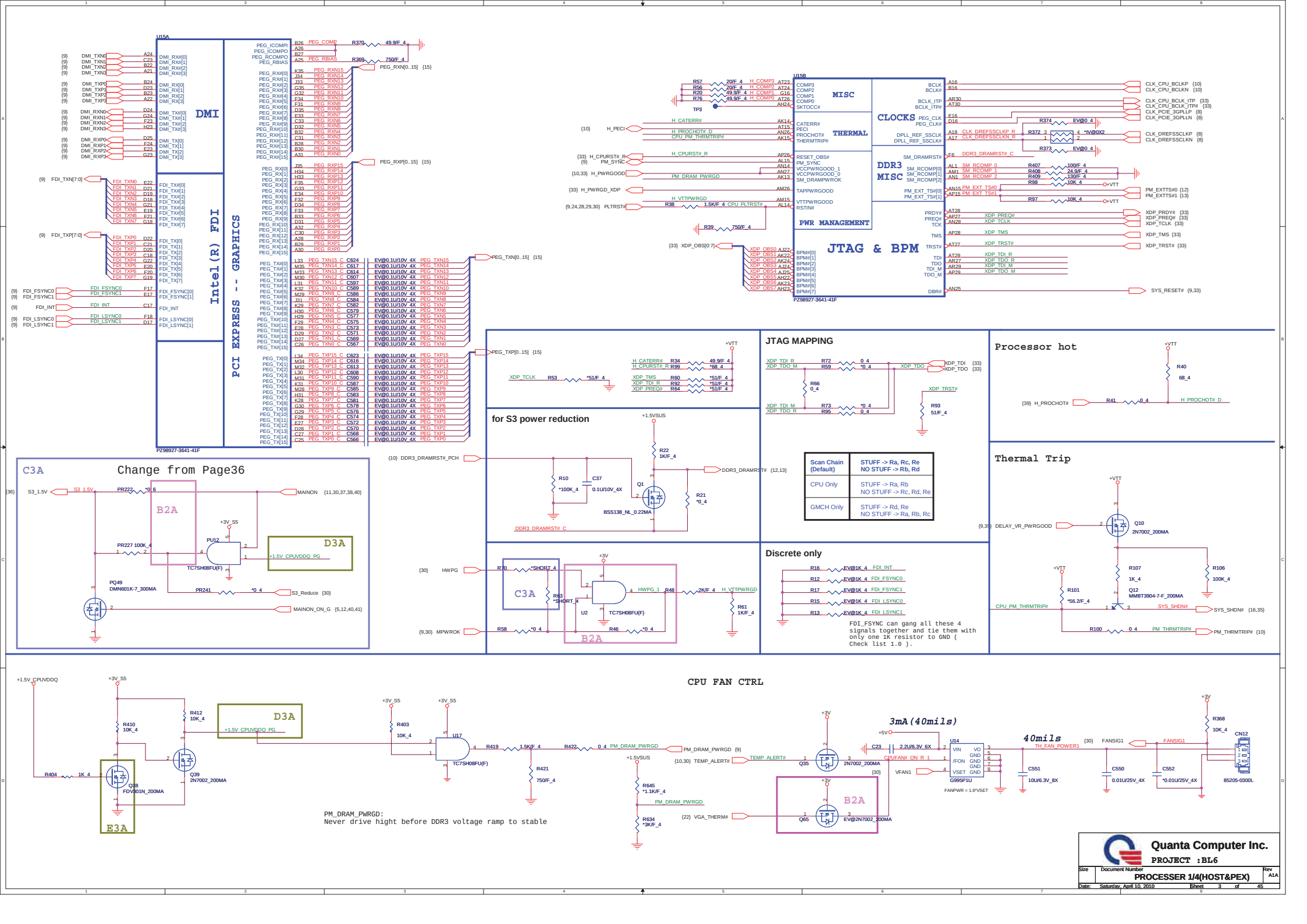
U15A
DMI
Intel(R) FDI
PCI EXPRESS -- GRAPHICS
PZ98927-3641-41F
U15B
MISC
THERMAL
CLOCKS
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
PZ98927-3641-41F
JTAG MAPPING
Processor hot
Thermal Trip
for S3 power reduction
Discrete only
Change from Page36
C3A
B2A
D3A
E3A
CPU FAN CTRL
3mA(40mils)
40mils
Scan Chain (Default)
STUFF -> Ra, Rc, Re
NO STUFF -> Rb, Rd
CPU Only
STUFF -> Ra, Rb
NO STUFF -> Rc, Rd, Re
GMCH Only
STUFF -> Rd, Re
NO STUFF -> Ra, Rb, Rc
FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).
PM_DRAM_PWRGD:
Never drive hight before DDR3 voltage ramp to stable
Quanta Computer Inc.
PROJECT :BL6
PROCESSER 1/4(HOST&PEX)
Size
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Rev
A1A
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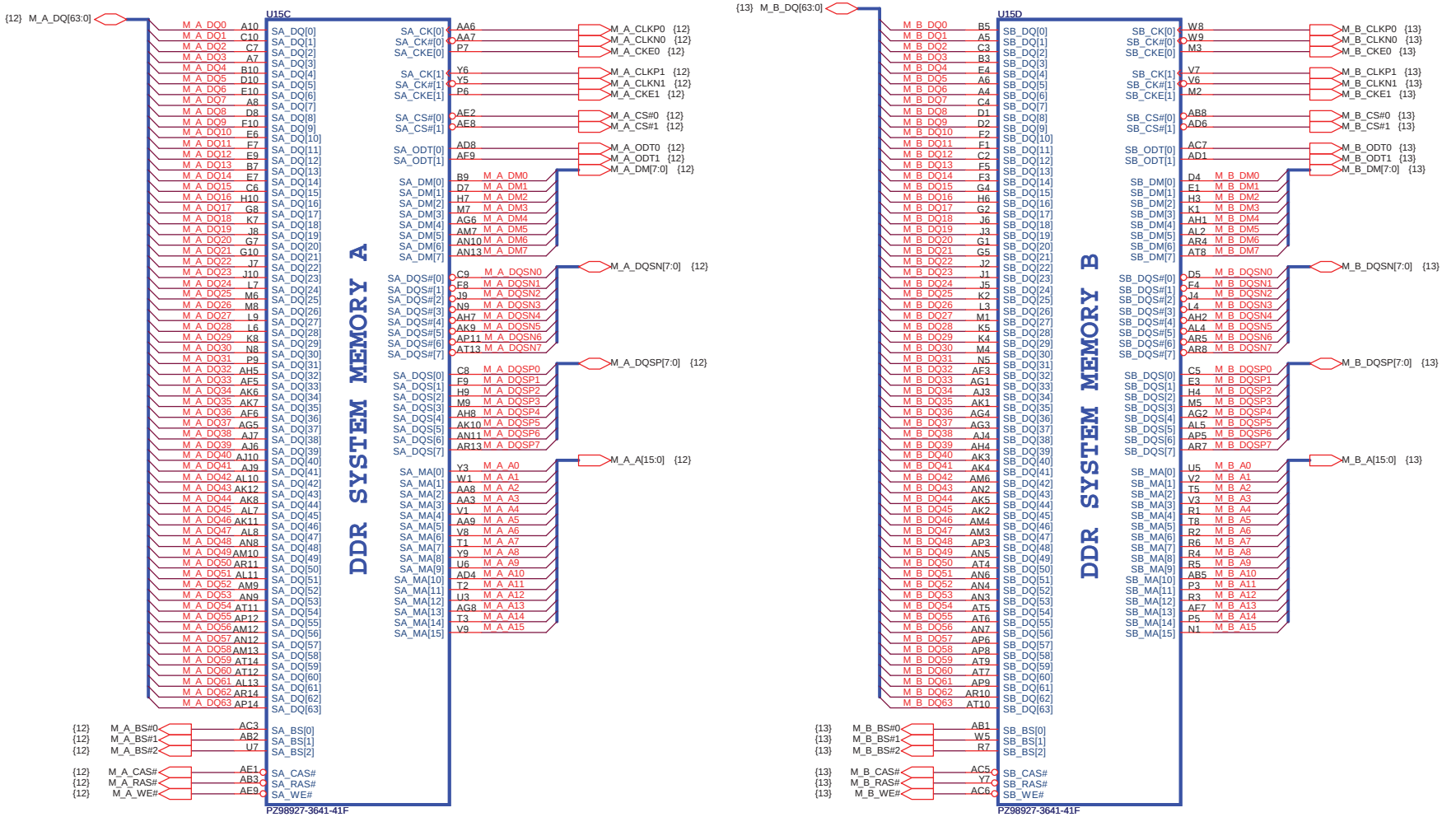
Sheet 3 of 45

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

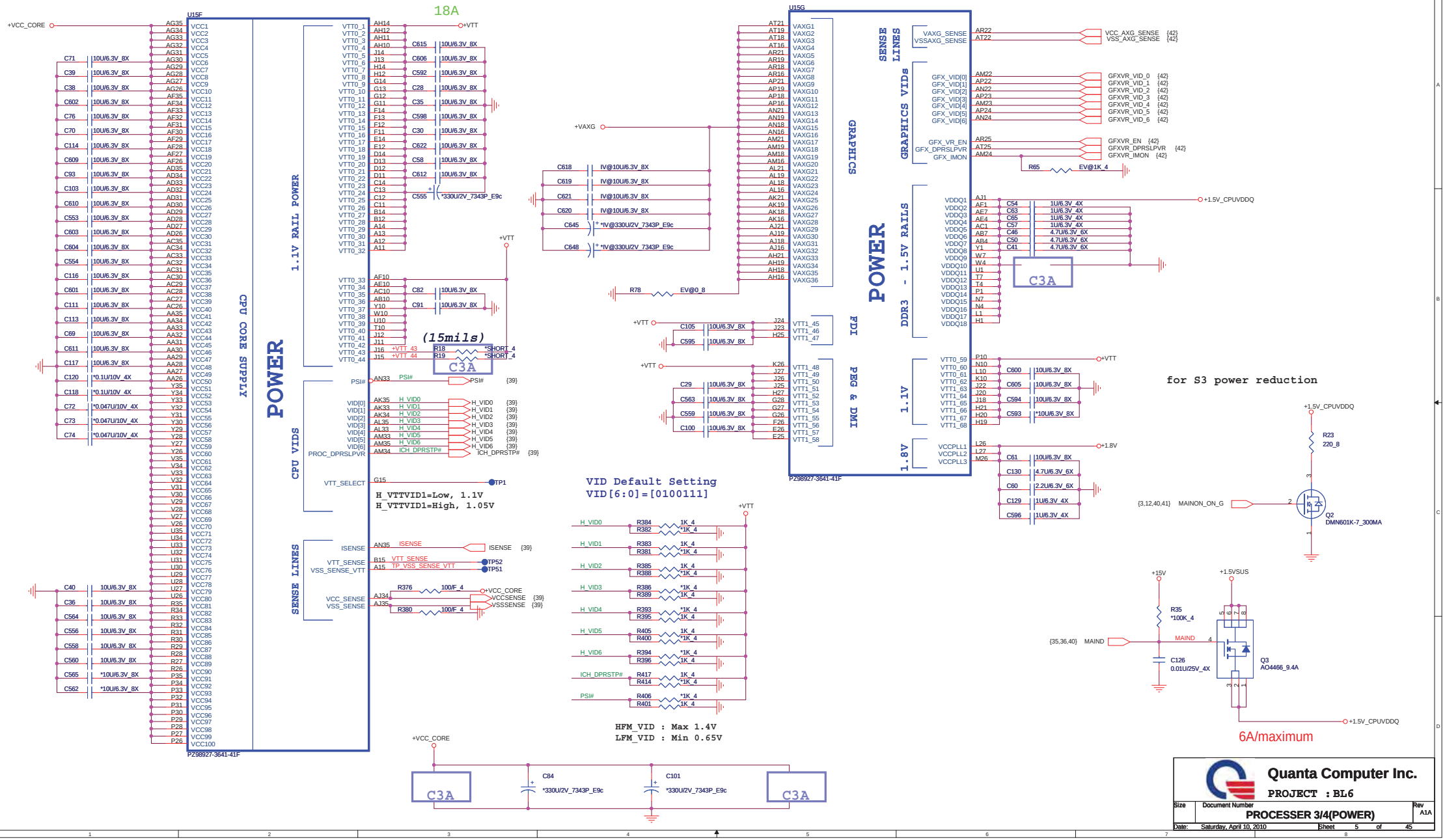


Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	PROCESSER 2/4(DDR)	A1A

Date: Saturday, April 10, 2010 Sheet 4 of 45


18A
U15F
POWER
CPU CORE SUPPLY
1.1V RAIL POWER
CPU VIDS
SENSE LINES
P298927-3641-41F
(15mils)
C3A
H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V
VID Default Setting
VID[6:0]=[0100111]
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V
U15G
POWER
GRAPHICS
SENSE LINES
GRAPHICS VIDs
DDR3 - 1.5V RAILS
PDI
PEG & DMI
1.1V
1.8V
for S3 power reduction
Quanta Computer Inc.
PROJECT : BL6
PROCESSER 3/4(POWER)
Size
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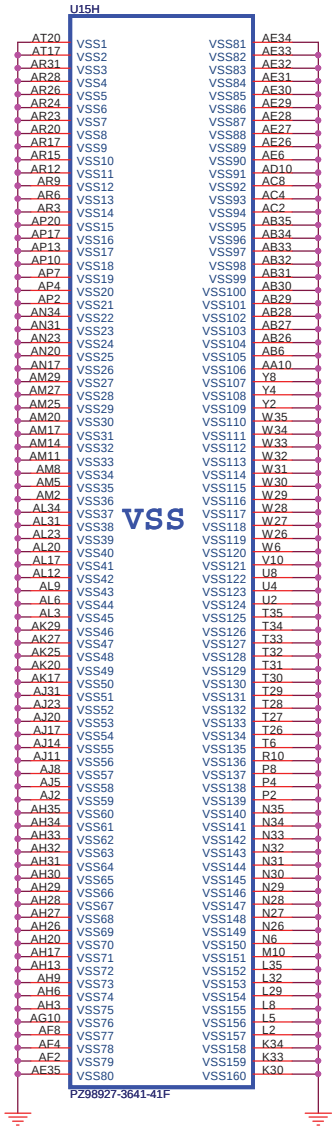
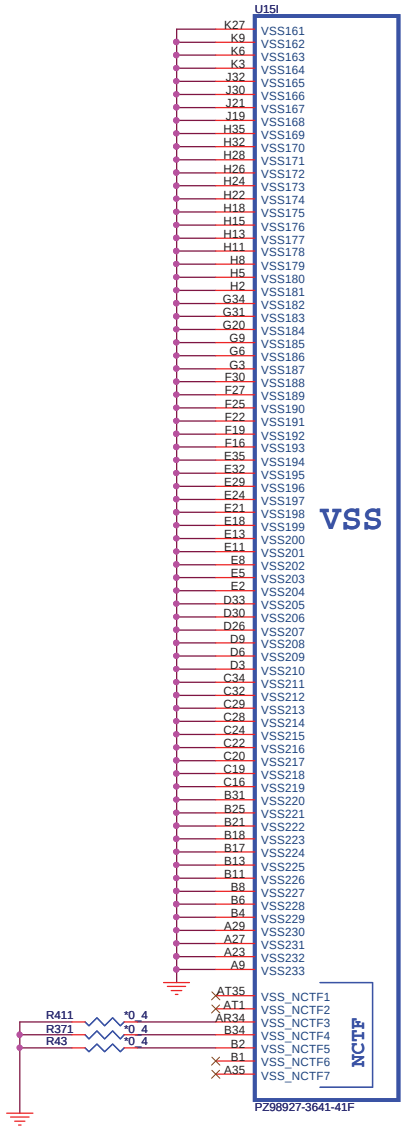
Sheet 5 of 45

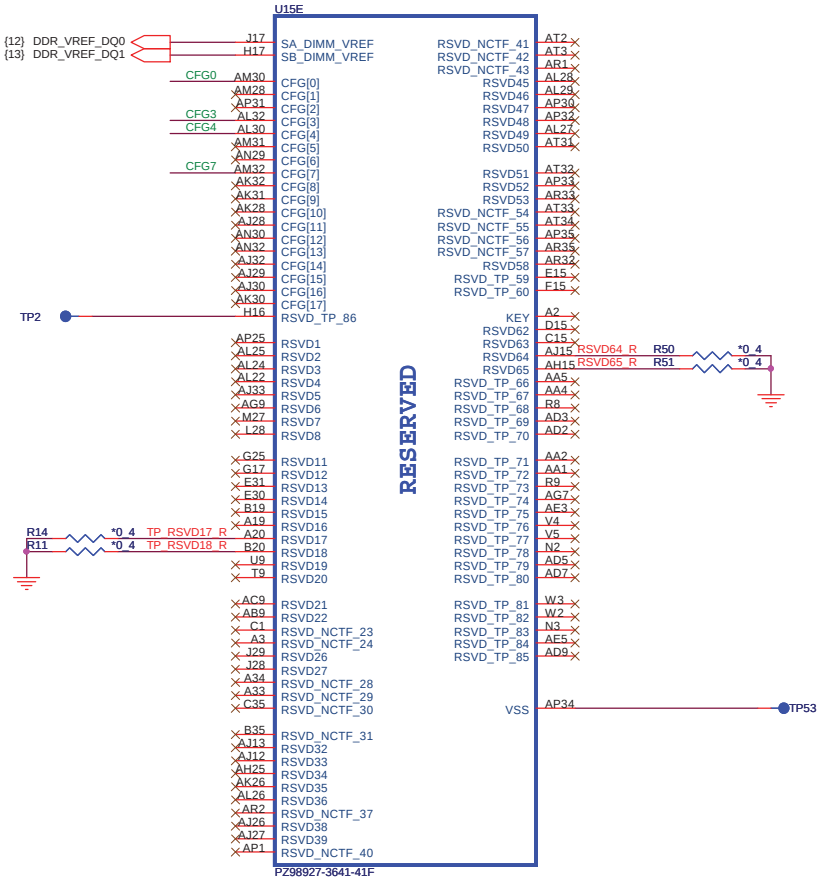
6A/maximum

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)





AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	**Lane Numbers Reversed 15 -> 0 , 14 -> 1**

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	PROCESSER 4/4 (GND)	1A
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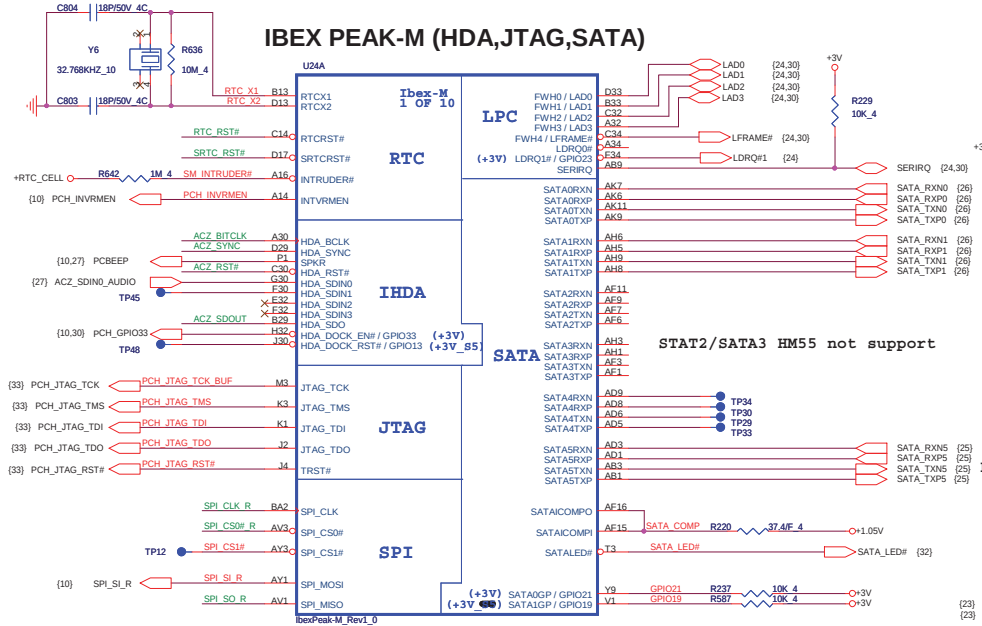
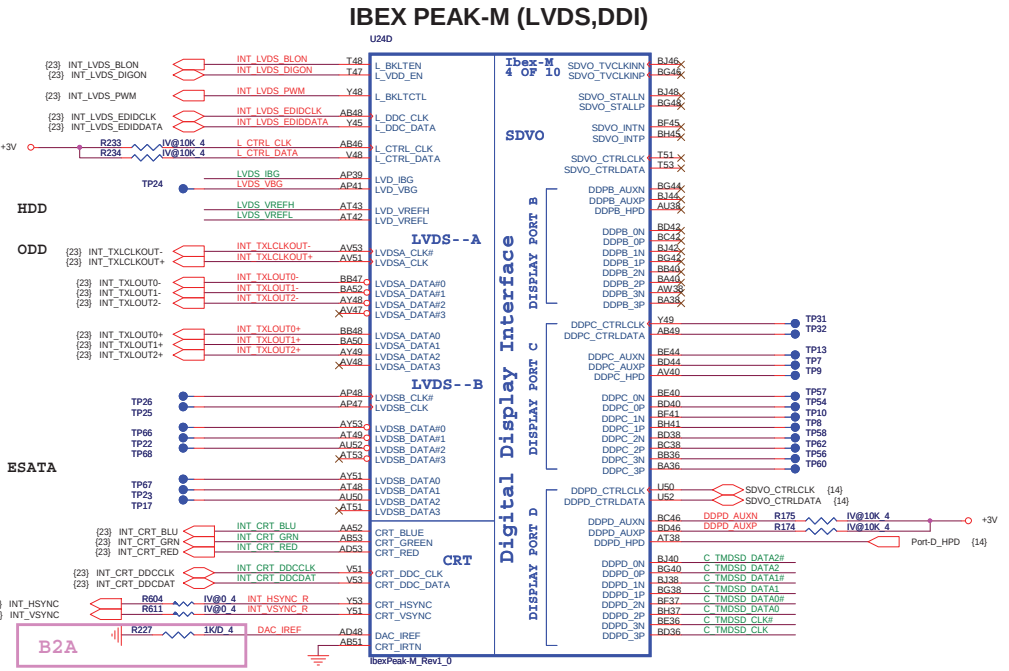
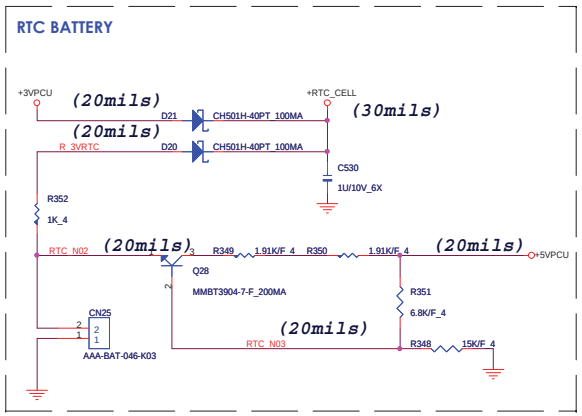
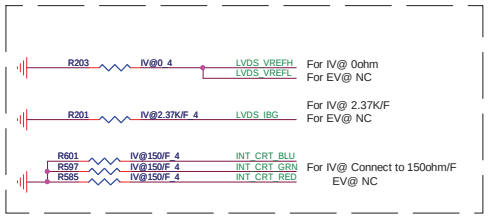
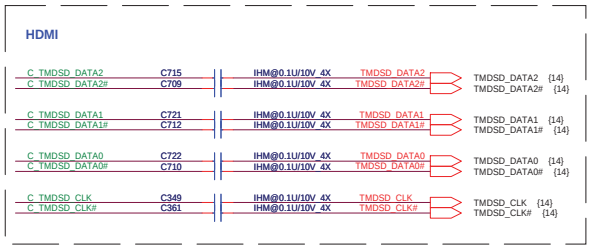


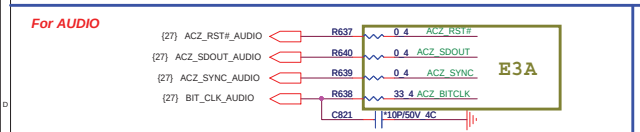


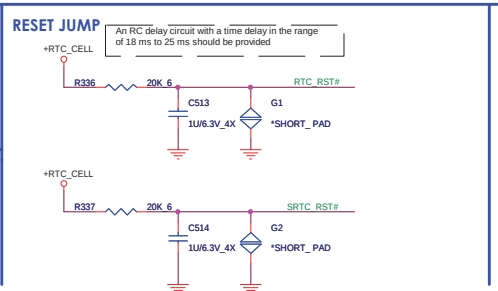
Port	Strap	How to enable Port?	How to disable Port?
LVDS	L_DDC_DATA	PU to 3.3V with 2.2k+/- 5%	NC
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port D	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
eDP	CFG[4]	PD to GND directly	NC

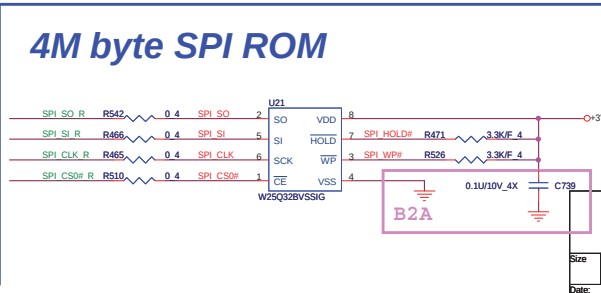












PCH	2MB	4MB	8MB
PM55	●		
HM55		●	
HM57/PM57		●	●
QM57/QS57			●

Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	A1A

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IBEX PEAK-M (GND)

U24I

AY7	VSS[159]	VSS[259]	H49
B11	VSS[160]	VSS[260]	H5
B15	VSS[161]	VSS[261]	J24
B19	VSS[162]	VSS[262]	K11
B23	VSS[163]	VSS[263]	K43
B31	VSS[164]	VSS[264]	K47
B35	VSS[165]	VSS[265]	K7
B39	VSS[166]	VSS[266]	L14
B43	VSS[167]	VSS[267]	L18
B47	VSS[168]	VSS[268]	L2
B7	VSS[169]	VSS[269]	L22
BG12	VSS[170]	VSS[270]	L32
BB12	VSS[171]	VSS[271]	L36
BB16	VSS[172]	VSS[272]	L40
BB20	VSS[173]	VSS[273]	L52
BB24	VSS[174]	VSS[274]	M12
BB30	VSS[175]	VSS[275]	M16
BB34	VSS[176]	VSS[276]	M20
BB38	VSS[177]	VSS[277]	N38
BB42	VSS[178]	VSS[278]	M34
BB49	VSS[179]	VSS[279]	M38
BB5	VSS[180]	VSS[280]	M42
BC10	VSS[181]	VSS[281]	M46
BC14	VSS[182]	VSS[282]	M49
BC18	VSS[183]	VSS[283]	M5
BC2	VSS[184]	VSS[284]	M8
BC22	VSS[185]	VSS[285]	N24
BC32	VSS[186]	VSS[286]	P11
BC36	VSS[187]	VSS[287]	AD15
BC40	VSS[188]	VSS[288]	P22
BC44	VSS[189]	VSS[289]	P30
BC52	VSS[190]	VSS[290]	P32
BH9	VSS[191]	VSS[291]	P34
BD48	VSS[192]	VSS[292]	P42
BD49	VSS[193]	VSS[293]	P45
BD5	VSS[194]	VSS[294]	P47
BE12	VSS[195]	VSS[295]	R2
BE16	VSS[196]	VSS[296]	R52
BE20	VSS[197]	VSS[297]	T12
BE24	VSS[198]	VSS[298]	T41
BE30	VSS[199]	VSS[299]	T46
BE34	VSS[200]	VSS[300]	T49
BE38	VSS[201]	VSS[301]	T5
BE42	VSS[202]	VSS[302]	T8
BE46	VSS[203]	VSS[303]	U30
BE48	VSS[204]	VSS[304]	U31
BE50	VSS[205]	VSS[305]	U32
BF6	VSS[206]	VSS[306]	U34
BF8	VSS[207]	VSS[307]	P38
BF3	VSS[208]	VSS[308]	V11
BF49	VSS[209]	VSS[309]	P16
BF51	VSS[210]	VSS[310]	V19
BG18	VSS[211]	VSS[311]	V20
BG24	VSS[212]	VSS[312]	V22
BG4	VSS[213]	VSS[313]	V30
BG50	VSS[214]	VSS[314]	V31
BH11	VSS[215]	VSS[315]	V32
BH15	VSS[216]	VSS[316]	V34
BH19	VSS[217]	VSS[317]	V35
BH23	VSS[218]	VSS[318]	V38
BH31	VSS[219]	VSS[319]	V43
BH35	VSS[220]	VSS[320]	V45
BH39	VSS[221]	VSS[321]	V46
BH43	VSS[222]	VSS[322]	V47
BH47	VSS[223]	VSS[323]	V49
BH7	VSS[224]	VSS[324]	V5
C12	VSS[225]	VSS[325]	V7
C50	VSS[226]	VSS[326]	V8
D51	VSS[227]	VSS[327]	W2
E12	VSS[228]	VSS[328]	W52
E16	VSS[229]	VSS[329]	Y11
E20	VSS[230]	VSS[330]	Y12
E24	VSS[231]	VSS[331]	Y15
E30	VSS[232]	VSS[332]	Y19
E34	VSS[233]	VSS[333]	Y23
E38	VSS[234]	VSS[334]	Y28
E42	VSS[235]	VSS[335]	Y30
E46	VSS[236]	VSS[336]	Y31
F48	VSS[237]	VSS[337]	Y32
F6	VSS[238]	VSS[338]	Y38
E8	VSS[239]	VSS[339]	Y43
F49	VSS[240]	VSS[340]	Y46
F5	VSS[241]	VSS[341]	P49
G10	VSS[242]	VSS[342]	Y5
G14	VSS[243]	VSS[343]	Y6
G18	VSS[244]	VSS[344]	Y8
G2	VSS[245]	VSS[345]	P24
G22	VSS[246]	VSS[346]	T43
G32	VSS[247]	VSS[347]	AD51
G36	VSS[248]	VSS[348]	AT8
G40	VSS[249]	VSS[349]	AD47
G44	VSS[250]	VSS[350]	Y47
G52	VSS[251]	VSS[351]	AT12
AF39	VSS[252]	VSS[352]	AM6
H16	VSS[253]	VSS[353]	AT13
H20	VSS[254]	VSS[354]	AM5
H30	VSS[255]	VSS[355]	AK45
H34	VSS[256]	VSS[356]	AK39
H38	VSS[257]	VSS[366]	AV14
H42	VSS[258]		

IbexPeak-M_Rev1_0

IBEX PEAK-M (PCI-E,SMBUS,CLK)

U24B

Ibex-M 2 OF 10

TP63 TP61 TP55 TP59 → BG30 BJ30 BF29 BH29
TP19 TP16 TP14 TP11 → AW30 BA30 BC30 BD30

3G: {24} PCIE_RXN3 / {24} PCIE_RXP3 / {24} PCIE_TXN3 / {24} PCIE_TXP3 — C364 *3G@0.1U/10V_4X, C365 *3G@0.1U/10V_4X — PCIE_TXN3_C AU32, PCIE_TXP3_C AV32 — B2A

PCIE_RXN3 AU30, PCIE_RXP3 AT30, BA32, BB32, BD32, BE32

WLAN: {24} PCIE_RXN5 / {24} PCIE_RXP5 / {24} PCIE_TXN5 / {24} PCIE_TXP5 — C343 0.1U/10V_4X, C342 0.1U/10V_4X — PCIE_TXN5_C BG32, PCIE_TXP5_C BJ32

PCIE_RXN5 BF33, PCIE_RXP5 BH33

LAN: {28} PCIE_RXN6 / {28} PCIE_RXP6 / {28} PCIE_TXN6 / {28} PCIE_TXP6 — C379 0.1U/10V_4X, C378 0.1U/10V_4X — PCIE_TXN6_C BC34, PCIE_TXP6_C BD34

PCIE_RXN6 BA34, PCIE_RXP6 AW34, AT34, AU34, AU36, AV36

PCIE7/PCIE8 HM55 not support

B2A: TP74 TP87 → BG34 BJ34 BG36 BJ36

CLKOUT_PCIE0N AK48, CLKOUT_PCIE0P AK47

PCIE_CLK_REQ0# → P9 — PCIECLKRQ0# / GPIO73 (+3V_S5)
TP21 TP27 → AM43 AM45 — CLKOUT_PCIE1N, CLKOUT_PCIE1P
PCIE_CLK_REQ1# → U4 — PCIECLKRQ1# / GPIO18 (+3V)
TP28 TP20 → AM47 AM48 — CLKOUT_PCIE2N, CLKOUT_PCIE2P
PCIE_CLK_REQ2# → N4 — PCIECLKRQ2# / GPIO20 (+3V)

LAN: {28} CLK_PCIE_LAN# / {28} CLK_PCIE_LAN → AH42 AH41 — CLKOUT_PCIE3N, CLKOUT_PCIE3P
{28} PCIE_CLK_REQ3# → PCIE_CLK_REQ3# A8 — PCIECLKRQ3# / GPIO25 (+3V_S5)

3G: {24} CLK_PCIE_3G# / {24} CLK_PCIE_3G → AM51 AM53 — CLKOUT_PCIE4N, CLKOUT_PCIE4P
{24} PCIE_CLK_REQ4# → PCIE_CLK_REQ4# M9 — PCIECLKRQ4# / GPIO26 (+3V_S5)

WLAN: {24} CLK_PCIE_MINI# / {24} CLK_PCIE_MINI → AJ50 AJ52 — CLKOUT_PCIE5N, CLKOUT_PCIE5P
{24} PCIE_CLK_RQ5# → PCIE_CLK_RQ5# H6 — PCIECLKRQ5# / GPIO44 (+3V_S5)

TP70 TP71 → AK53 AK51 — CLKOUT_PEG_B_N, CLKOUT_PEG_B_P
PCIE_CLK_REQB# → P13 — PEG_B_CLKRQ# / GPIO56 (+3V_S5)

IbexPeak-M_Rev1_0

PCI-E*

SMBus

(+3V_S5) SMBALERT# / GPIO11 — B9 SMBALERT#
SMBCLK — H14 SCLK — SCLK {2,24,28,33}
SMBDATA — C8 SDATA — SDATA {2,24,28,33}
(+3V_S5) SML0ALERT# / GPIO60 — J14 SMBL0ALERT#
SML0CLK — C6 SMB_CLK_ME0
SML0DATA — G8 SMB_DATA_ME0
(+3V_S5) SML1ALERT# / GPIO74 — M14 SML1ALERT#
(+3V_S5) SML1CLK / GPIO58 — E10 MBCLK2
(+3V_S5) SML1DATA / GPIO75 — G12 MBDATA2

Controller Link

CL_CLK1 — T13 CL_CLK1 — CL_CLK1 {24}
CL_DATA1 — T11 CL_DATA1 — CL_DATA1 {24}
CL_RST1# — T9 CL_RST#1 — CL_RST#1 {24}

PEG

(+3V_S5) PEG_A_CLKRQ# / GPIO47 — H1 PEG_CLKREQ#
CLKOUT_PEG_A_N — AD43 — CLK_PCIE_VGA# {15}
CLKOUT_PEG_A_P — AD45 — CLK_PCIE_VGA {15}
CLKOUT_DMI_N — AN4 — CLK_PCIE_3GPLLN {3}
CLKOUT_DMI_P — AN2 — CLK_PCIE_3GPLLP {3}

From CLK BUFFER

CLKOUT_DP_N / CLKOUT_BCLK1_N — AT1 — CLK_DREFSSCLKN {3}
CLKOUT_DP_P / CLKOUT_BCLK1_P — AT3 — CLK_DREFSSCLKP {3}
CLKIN_DMI_N — AW24 — CLK_BUF_PCIE_3GPLLN {2}
CLKIN_DMI_P — BA24 — CLK_BUF_PCIE_3GPLLP {2}
CLKIN_BCLK_N — AP3 — CLK_BUF_BCLKN {2}
CLKIN_BCLK_P — AP1 — CLK_BUF_BCLKP {2}
CLKIN_DOT_96N — F18 — CLK_BUF_DREFCLKN {2}
CLKIN_DOT_96P — E18 — CLK_BUF_DREFCLKP {2}
CLKIN_SATA_N / CKSSCD_N — AH13 — CLK_BUF_DREFSSCLKN {2}
CLKIN_SATA_P / CKSSCD_P — AH12 — CLK_BUF_DREFSSCLKP {2}
REFCLK14IN — P41 — CLK_PCH_14M {2}
CLKIN_PCILOOPBACK — J42 CLK_PCI_FB — CLK_PCI_FB {9}
XTAL25_IN — AH51 XTAL25_IN
XTAL25_OUT — AH53 XTAL25_OUT
XCLK_RCOMP — AF38 XCLK_RCOMP — R226 90.9/F_4 — +1.05V

Clock Flex

(+3V) CLKOUTFLEX0 / GPIO64 — T45 CLK_FLEX0 — R235 10K_4 — +3V
(+3V) CLKOUTFLEX1 / GPIO65 — P43 CLK_FLEX1 — T34
(+3V) CLKOUTFLEX2 / GPIO66 — T42 CLK_FLEX2 — T33
(+3V) CLKOUTFLEX3 / GPIO67 — N50 CLK_FLEX3 — R257 22_4 — 48M_CARD {29}

48M_Card Reserve for cardreader 48MHZ

+3V_S5
C3A: MBDATA2 — 2ND_MBDATA {30} — Q15 2N7002_200MA
MBCLK2 — 2ND_MBCLK {30} — Q13 2N7002_200MA

+3V
PCIE_CLK_REQ1# R588 10K_4
PCIE_CLK_REQ2# R600 10K_4

+3V_S5
SMBALERT# R650 10K_4
SCLK R311 2.2K_4
SDATA R654 2.2K_4
SMBL0ALERT# R300 10K_4
SMB_CLK_ME0 R631 2.2K_4
SMB_DATA_ME0 R623 2.2K_4
SML1ALERT# R310 10K_4
MBCLK2 R299 2.2K_4
MBDATA2 R313 2.2K_4

+3V_S5
PCIE_CLK_REQ0# R309 10K_4
B2A: PCIE_CLK_REQ3# R653 *10K_4
PCIE_CLK_REQ4# R276 10K_4
PCIE_CLK_REQB# R301 10K_4
PCIE_CLK_RQ5# R619 10K_4
PEG_CLKREQ# R615 IV@10K_4
PEG_CLKREQ# R610 EV@10K_4

Placement close

R560 EV@0_4
XTAL25_IN — C749 IV@27P/50V_4N
R552 IV@1M/F_4
Y4 IV@25MHZ_30
XTAL25_OUT — C747 IV@27P/50V_4N
B2A

Quanta Computer Inc.
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	PCH 2/5 (PCIE, SMBUS, CK)	A1A
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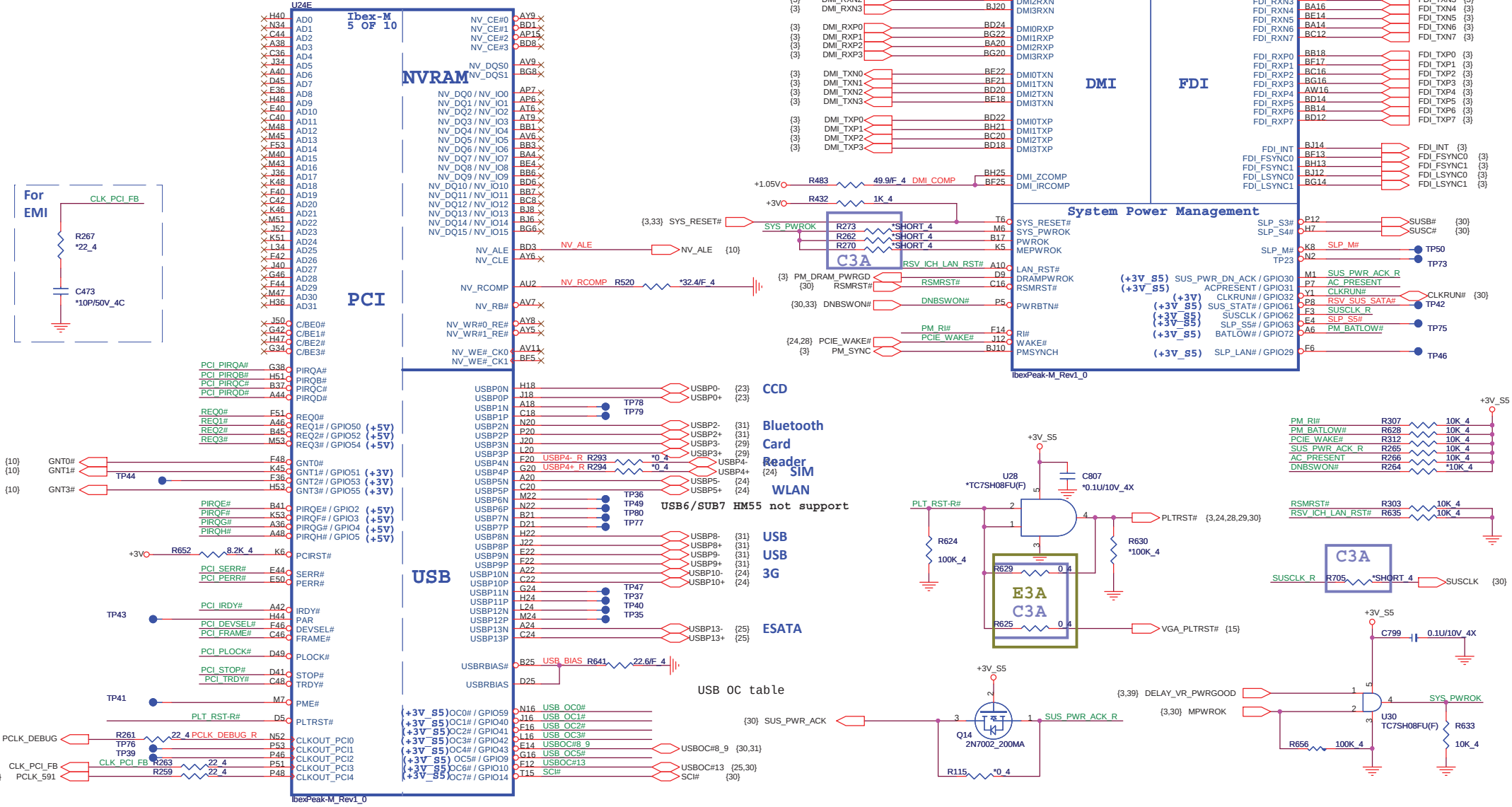
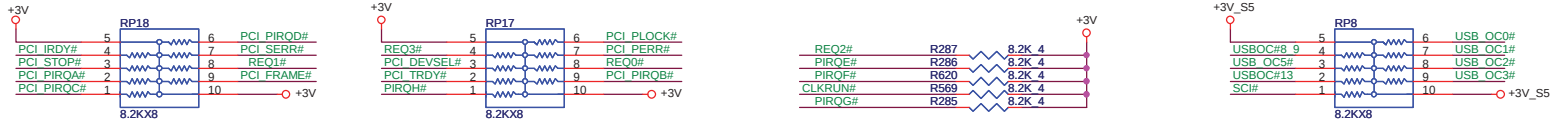
IBEX PEAK-M (PCI,USB,NVRAM)



IBEX PEAK-M (DMI,FDI,GPIO)



Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	PCH 3/5 (PCI,ONFI,USB,DMI)	A1A
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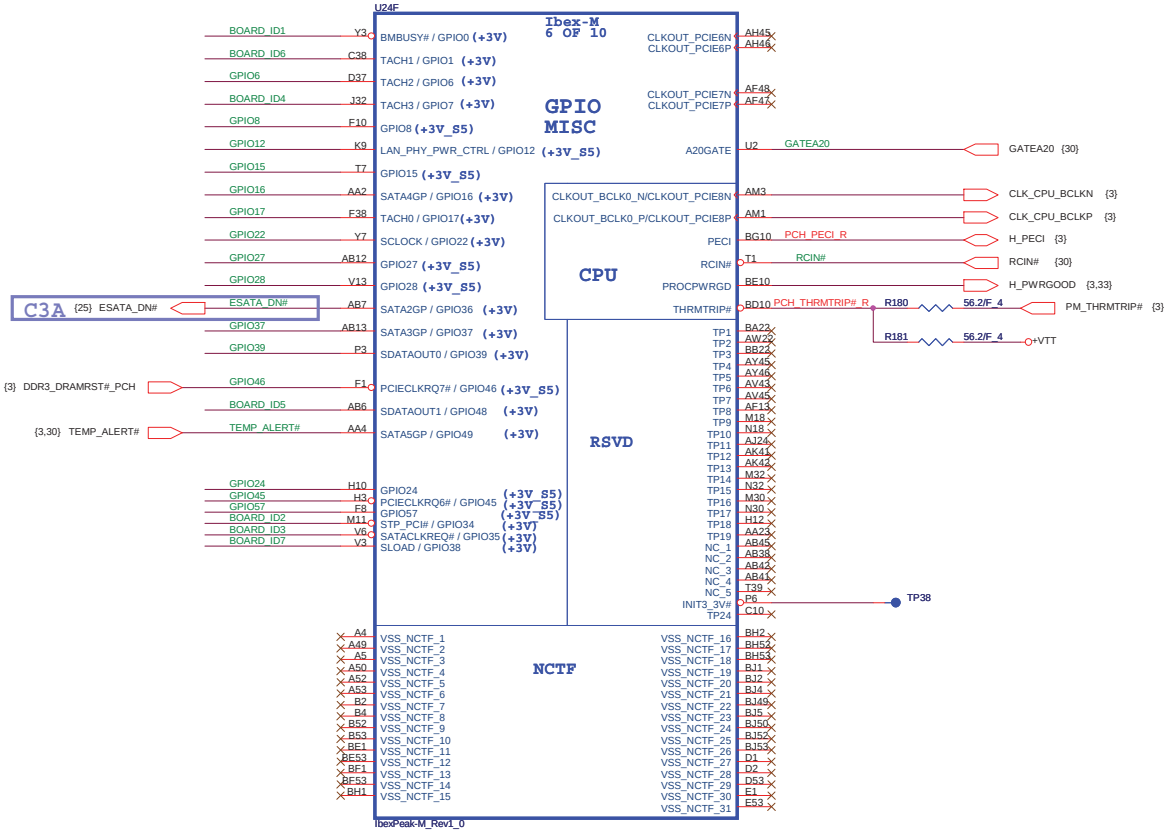
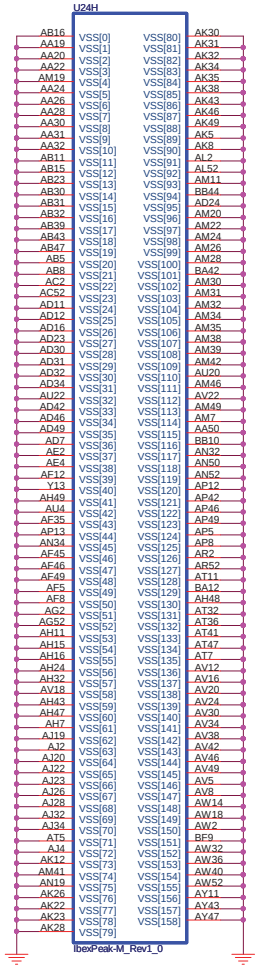
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



PCH Strap Pin Configuration Table

SPKR

{7,27} PCBEEP — R592 *1K_4 — +3V

Reboot option at power-up

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

GNT3#/ GPIO55

{9} GNT3# — R622 *10K_4

Top-Block Swap Override

0 = Top Block Swap Mode
1 = Default Mode (Internal pull-up)

HDA_DOCK_EN #/GPIO33

{7,30} PCH_GPIO33 — R282 1K_4 — E3A — JP1 *SHORT PAD

Flash Descriptor Security Override

0 = Flash Descriptor Security will be overridden
1 = Security measure defined in the Flash Descriptor will be enabled.

GNT0#, GNT1#

{9} GNT0# — R272 *1K_4
{9} GNT1# — R621 *1K_4

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI

SPI_MOSI

{7} SPI_SI_R — R504 *1K_4 — +3V

TPM Functionality Disable

1 = Enabled
0 = Disable

NV_ALE

{9} NV_ALE — R496 *10K_4 — +1.8V

IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable

1 = Enabled
0 = Disabled (Default)

GPIO8

GPIO8 — R298 10K_4 — +3V_S5

Reserved

This signal has a weak internal pull up.
NOTE: This signal should not be pulled low

GPIO15

GPIO15 — R248 1K_4 — +3V_S5

Reserved

0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

GPIO27

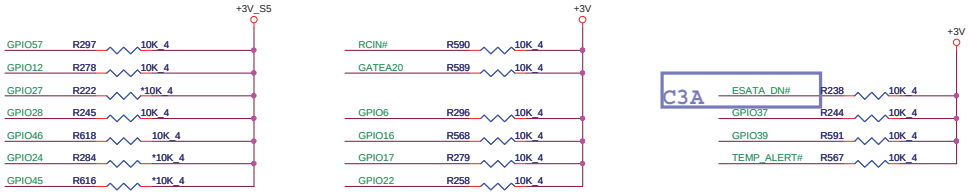
GPIO27 — R232 *10K_4

On-Die PLL Voltage Regulator

0 = Disables the VccVRM. Need to use on-board filter circuits for analog rails.
1 = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.
This signal has a weak internal pull-up.

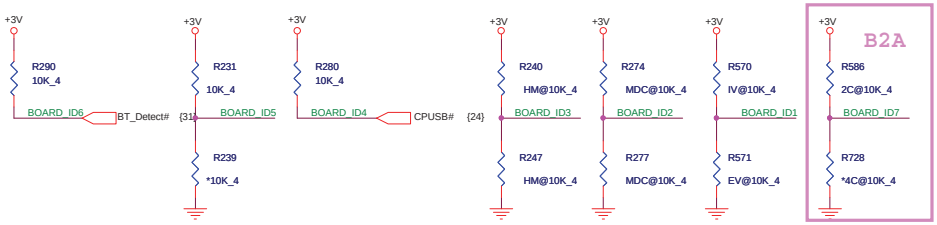
+RTC_CELL — R644 330K_6 — PCH_INVRMEN — {7}

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs



BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7
UMA SKU VGA SKU	H L						
W/ MDC W/O MDC		H L					
W/ HDMI W/O HDMI			H L				
W/O 3G W/ 3G				H L			
15" 14"					H L		
W/O BT W/ BT						H L	
2 Core 4 Core							H L



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	PCH 4/5 (GPIO & Strap)	A1A

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+VCCA_DAC_1_2=69mA(15mils)

VCCCORE = 1.432A(80mils)

VCCTX_LVDS= 59mA(15mils)

VCCIO = 3.062A(150mils)

VCCALVDS= 59mA(15mils)

VCCLAN = 0.32A(30mils)

VCCSUS3_3 = 0.163A(20mils)

40mA(15mils)

VCC3_3 = 0.357A(30mils)

VCCVRM= 196mA(15mils)

VCCME = 1.849A(100mils)

VCCDMI= 61mA(15mils)

V5REF_SUS< 1mA

VCCPNAND= 156mA(15mils)

68mA(15mils)

V5REF< 1mA

VCCME3_3= 85mA(15mils)

VCCIO = 3.062A(150mils)

VCC3_3 = 0.357A(30mils)

Isolate the power supply for pins AF32,AF34,AH34
Reduce the jitter on HDMI interface for
1080P 60Hz Deep color mode.

VCCSUS3_3 = 0.163A(20mils)

37mA(15mils)

68mA(15mils)

VCC3_3 = 0.357A(30mils)

V_CPU >1mA(15mils)

VCCIO = 3.062A(150mils)

VCCRTC= 2mA(15mils)

VCCME = 1.849A(100mils)

VCCSUSHDA= 6mA(15mils)

Reserve for clear CRT Power

Plcaement close to U52

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	PCH 5/5 (POWER)		A1A
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H=4

JDIM1A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP4B

JDIM1B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP4B

for S3 power reduction

Place these Caps near So-Dimm0.

Quanta Computer Inc.		
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H=8

JDIM2A

{4} M_B_A[15:0]

M_B_A0 98
M_B_A1 97
M_B_A2 96
M_B_A3 95
M_B_A4 92
M_B_A5 91
M_B_A6 90
M_B_A7 86
M_B_A8 89
M_B_A9 85
M_B_A10 107
M_B_A11 84
M_B_A12 83
M_B_A13 119
M_B_A14 80
M_B_A15 78

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 A14 A15

{4} M_B_BS#0 109
{4} M_B_BS#1 108
{4} M_B_BS#2 79
{4} M_B_CS#0 114
{4} M_B_CS#1 121
{4} M_B_CLKP0 101
{4} M_B_CLKN0 103
{4} M_B_CLKP1 102
{4} M_B_CLKN1 104
{4} M_B_CKE0 73
{4} M_B_CKE1 74
{4} M_B_CAS# 115
{4} M_B_RAS# 110
{4} M_B_WE# 113

BA0 BA1 BA2 S0# S1# CK0 CK0# CK1 CK1# CKE0 CKE1 CAS# RAS# WE#

R77 10K/F_4 DIMM1_SA0 197
R83 10K/F_4 DIMM1_SA1 201

SA0 SA1

+3V

{2,12,24} CGCLK_SMB 202
{2,12,24} CGDAT_SMB 200

SCL SDA

{4} M_B_ODT0 116
{4} M_B_ODT1 120

ODT0 ODT1

{4} M_B_DM[7:0]

M_B_DM0 11
M_B_DM1 28
M_B_DM2 46
M_B_DM3 63
M_B_DM4 136
M_B_DM5 153
M_B_DM6 170
M_B_DM7 187

DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7

{4} M_B_DQSP[7:0]

M_B_DQSP0 12
M_B_DQSP1 29
M_B_DQSP2 47
M_B_DQSP3 64
M_B_DQSP4 137
M_B_DQSP5 154
M_B_DQSP6 171
M_B_DQSP7 188

DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7

{4} M_B_DQSN[7:0]

M_B_DQSN0 10
M_B_DQSN1 27
M_B_DQSN2 45
M_B_DQSN3 62
M_B_DQSN4 135
M_B_DQSN5 152
M_B_DQSN6 169
M_B_DQSN7 186

DQS#0 DQS#1 DQS#2 DQS#3 DQS#4 DQS#5 DQS#6 DQS#7

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP8D

M_B_DQ[63:0] {4}

M_B_DQ0 5
M_B_DQ1 7
M_B_DQ2 15
M_B_DQ3 17
M_B_DQ4 4
M_B_DQ5 6
M_B_DQ6 16
M_B_DQ7 18
M_B_DQ8 21
M_B_DQ9 23
M_B_DQ10 33
M_B_DQ11 35
M_B_DQ12 22
M_B_DQ13 24
M_B_DQ14 34
M_B_DQ15 36
M_B_DQ16 39
M_B_DQ17 41
M_B_DQ18 51
M_B_DQ19 53
M_B_DQ20 40
M_B_DQ21 42
M_B_DQ22 50
M_B_DQ23 52
M_B_DQ24 57
M_B_DQ25 59
M_B_DQ26 67
M_B_DQ27 69
M_B_DQ28 56
M_B_DQ29 58
M_B_DQ30 68
M_B_DQ31 70
M_B_DQ32 129
M_B_DQ33 131
M_B_DQ34 141
M_B_DQ35 143
M_B_DQ36 130
M_B_DQ37 132
M_B_DQ38 140
M_B_DQ39 142
M_B_DQ40 147
M_B_DQ41 149
M_B_DQ42 157
M_B_DQ43 159
M_B_DQ44 146
M_B_DQ45 148
M_B_DQ46 158
M_B_DQ47 160
M_B_DQ48 163
M_B_DQ49 165
M_B_DQ50 175
M_B_DQ51 177
M_B_DQ52 164
M_B_DQ53 166
M_B_DQ54 174
M_B_DQ55 176
M_B_DQ56 181
M_B_DQ57 183
M_B_DQ58 191
M_B_DQ59 193
M_B_DQ60 180
M_B_DQ61 182
M_B_DQ62 192
M_B_DQ63 194

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

H=8

+1.5VSUS

JDIM2B

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

+3V

VDDSPD 199

NC1 77
NC2 122
NCTEST 125

{3} PM_EXTTS#1 198
{3,12} DDR3_DRAMRST# 30

EVENT# RESET#

{6} DDR_VREF_DQ1

R4 *0_6 SMDDR_VREF_DQ1 1
{12} SMDDR_VREF_DIMM 126

VREF_DQ VREF_CA

R5 *4C@100K_4

VSS1 2
VSS2 3
VSS3 8
VSS4 9
VSS5 13
VSS6 14
VSS7 19
VSS8 20
VSS9 25
VSS10 26
VSS11 31
VSS12 32
VSS13 37
VSS14 38
VSS15 43

VSS16 44
VSS17 48
VSS18 49
VSS19 54
VSS20 55
VSS21 60
VSS22 61
VSS23 65
VSS24 66
VSS25 71
VSS26 72
VSS27 127
VSS28 128
VSS29 133
VSS30 134
VSS31 138
VSS32 139
VSS33 144
VSS34 145
VSS35 150
VSS36 151
VSS37 155
VSS38 156
VSS39 161
VSS40 162
VSS41 167
VSS42 168
VSS43 172
VSS44 173
VSS45 178
VSS46 179
VSS47 184
VSS48 185
VSS49 189
VSS50 190
VSS51 195
VSS52 196

VTT1 203 +SMDDR_VTERM
VTT2 204

GND 205
GND 206

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP8D

Place these Caps near So-Dimm1.

+1.5VSUS

C87 4.7U/6.3V_6X
C48 4.7U/6.3V_6X
C56 4.7U/6.3V_6X
C83 4.7U/6.3V_6X
C88 4.7U/6.3V_6X
C64 4.7U/6.3V_6X
C52 0.1U/10V_4X
C66 0.1U/10V_4X
C44 0.1U/10V_4X
C78 0.1U/10V_4X
C45 0.1U/10V_4X
C97 *0.047U/10V_4X
C75 *0.047U/10V_4X

SMDDR_VREF_DIMM

C121 0.1U/10V_4X
C123 2.2U/6.3V_6X
C122 *0.047U/10V_4X

SMDDR_VREF_DQ1

C31 0.1U/10V_4X
C27 2.2U/6.3V_6X

+3V

C163 2.2U/6.3V_6X
C169 *0.1U/10V_4X
C164 *0.047U/10V_4X

+SMDDR_VTERM

C176 1U/6.3V_4X
C187 1U/6.3V_4X
C175 1U/6.3V_4X
C188 1U/6.3V_4X
C190 *10U/6.3V_8X
C185 4.7U/6.3V_6X
C180 4.7U/6.3V_6X
C177 *0.047U/10V_4X
C178 *0.047U/10V_4X

+1.5VSUS

R3 1K/F_4

SMDDR_VREF_DQ1

R2 1K/F_4
C24 0.1U/10V_4X
C33 *0.047U/10V_4X

+1.5VSUS

+ C580 *330U/2.5V_7343P_E9a

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	DDR3 DIMM-1	A1A
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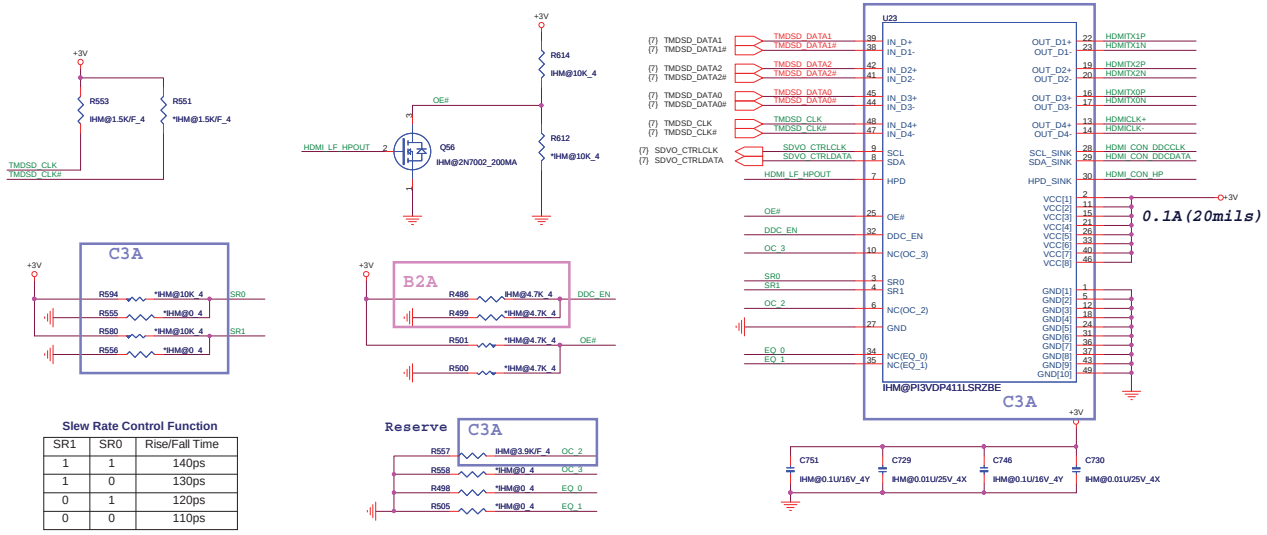
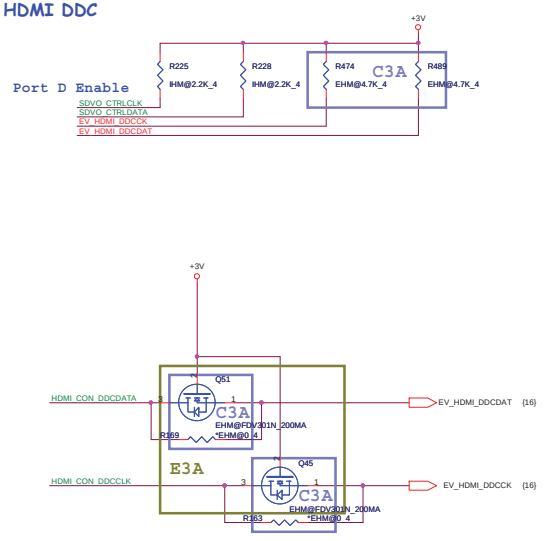
HDMI Level Shift



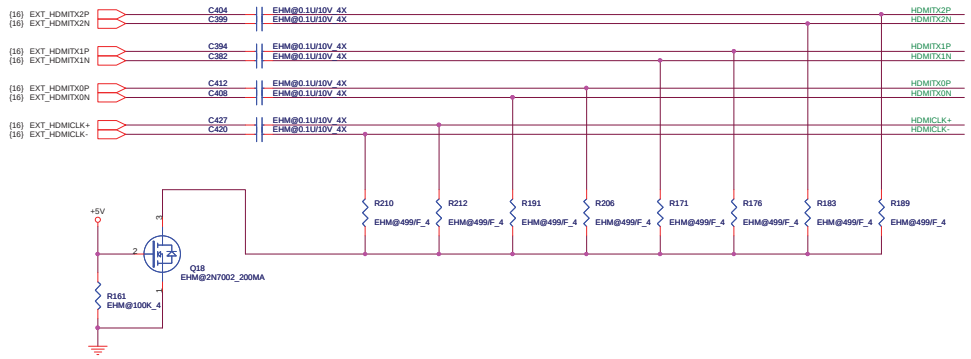
Slew Rate Control Function

SR1	SR0	Rise/Fall Time
1	1	140ps
1	0	130ps
0	1	120ps
0	0	110ps

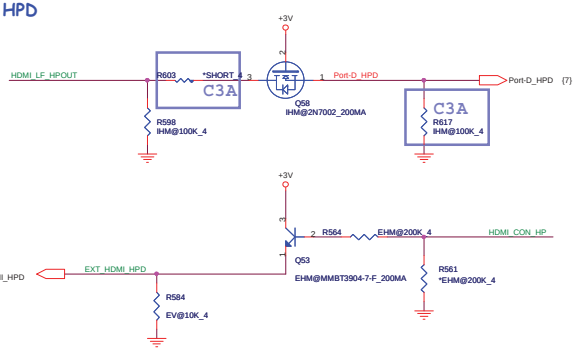
HDMI DDC



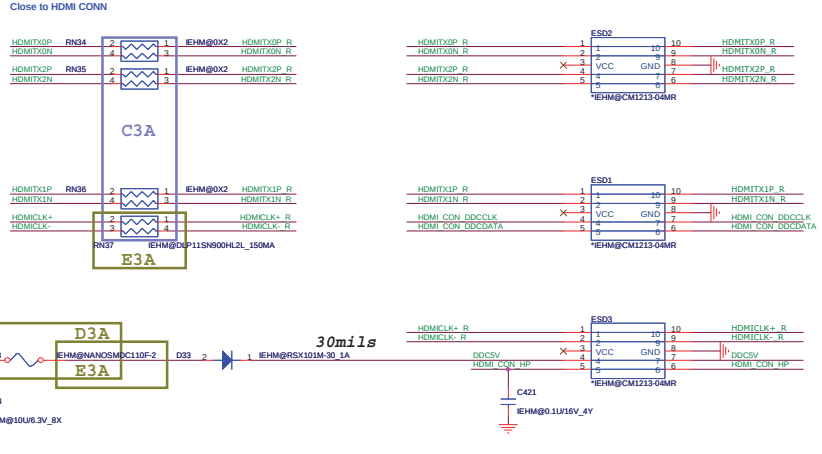
Discrete HDMI

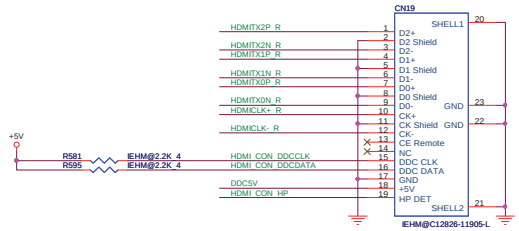


HDMI HPD



Close to HDMI CONN





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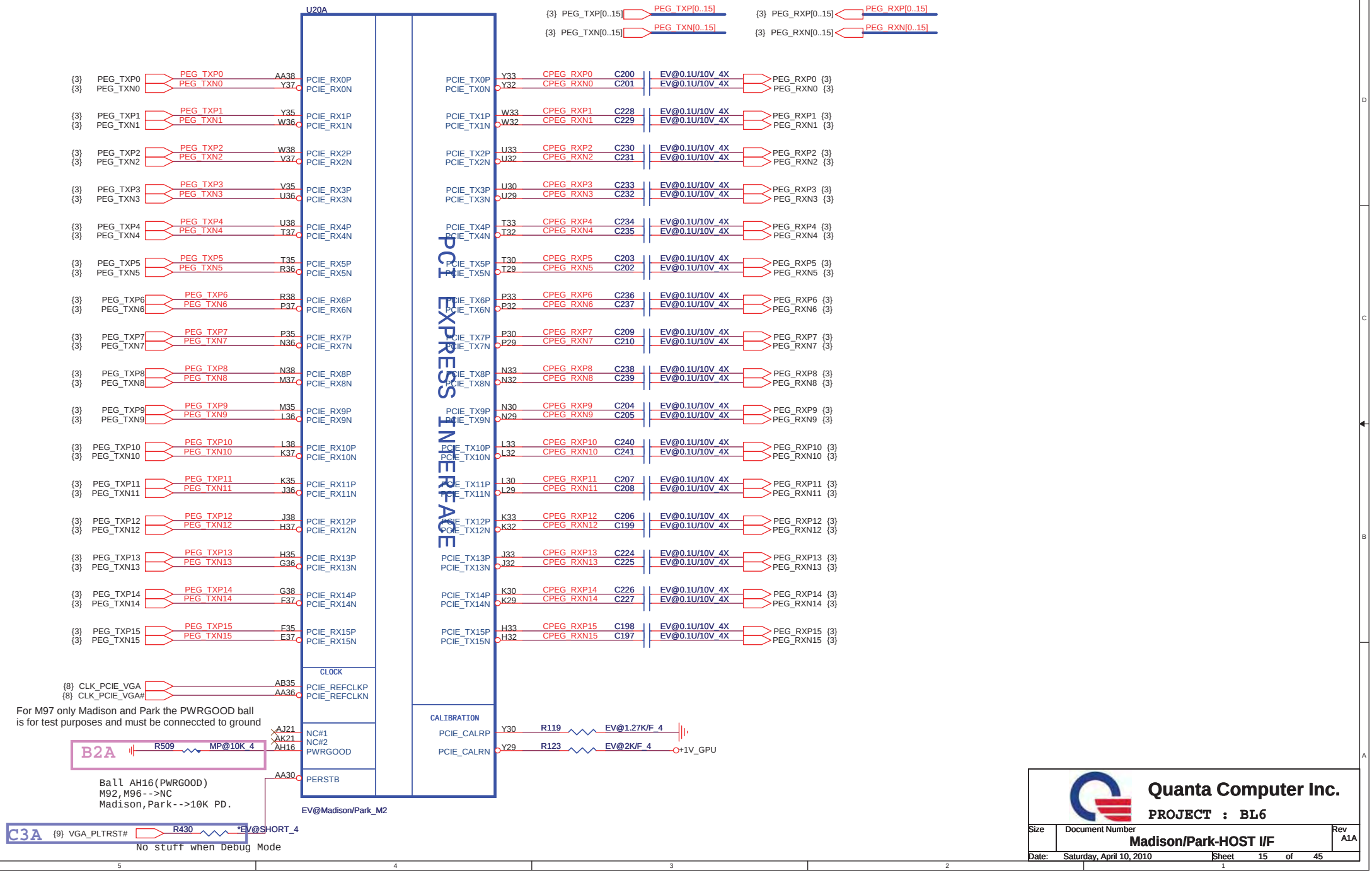
U20A
PCI EXPRESS INTERFACE
{3} PEG_TXP[0..15]
PEG_TXP[0..15]
{3} PEG_TXN[0..15]
PEG_TXN[0..15]
{3} PEG_RXP[0..15]
PEG_RXP[0..15]
{3} PEG_RXN[0..15]
PEG_RXN[0..15]
PEG_TXP0 AA38 PCIE_RX0P
PEG_TXN0 Y37 PCIE_RX0N
PEG_TXP1 Y35 PCIE_RX1P
PEG_TXN1 W36 PCIE_RX1N
PEG_TXP2 W38 PCIE_RX2P
PEG_TXN2 V37 PCIE_RX2N
PEG_TXP3 V35 PCIE_RX3P
PEG_TXN3 U36 PCIE_RX3N
PEG_TXP4 U38 PCIE_RX4P
PEG_TXN4 T37 PCIE_RX4N
PEG_TXP5 T35 PCIE_RX5P
PEG_TXN5 R36 PCIE_RX5N
PEG_TXP6 R38 PCIE_RX6P
PEG_TXN6 P37 PCIE_RX6N
PEG_TXP7 P35 PCIE_RX7P
PEG_TXN7 N36 PCIE_RX7N
PEG_TXP8 N38 PCIE_RX8P
PEG_TXN8 M37 PCIE_RX8N
PEG_TXP9 M35 PCIE_RX9P
PEG_TXN9 L36 PCIE_RX9N
PEG_TXP10 L38 PCIE_RX10P
PEG_TXN10 K37 PCIE_RX10N
PEG_TXP11 K35 PCIE_RX11P
PEG_TXN11 J36 PCIE_RX11N
PEG_TXP12 J38 PCIE_RX12P
PEG_TXN12 H37 PCIE_RX12N
PEG_TXP13 H35 PCIE_RX13P
PEG_TXN13 G36 PCIE_RX13N
PEG_TXP14 G38 PCIE_RX14P
PEG_TXN14 F37 PCIE_RX14N
PEG_TXP15 F35 PCIE_RX15P
PEG_TXN15 E37 PCIE_RX15N
PCIE_TX0P Y33 CPEG_RXP0 C200 EV@0.1U/10V_4X PEG_RXP0 {3}
PCIE_TX0N Y32 CPEG_RXN0 C201 EV@0.1U/10V_4X PEG_RXN0 {3}
PCIE_TX1P W33 CPEG_RXP1 C228 EV@0.1U/10V_4X PEG_RXP1 {3}
PCIE_TX1N W32 CPEG_RXN1 C229 EV@0.1U/10V_4X PEG_RXN1 {3}
PCIE_TX2P U33 CPEG_RXP2 C230 EV@0.1U/10V_4X PEG_RXP2 {3}
PCIE_TX2N U32 CPEG_RXN2 C231 EV@0.1U/10V_4X PEG_RXN2 {3}
PCIE_TX3P U30 CPEG_RXP3 C233 EV@0.1U/10V_4X PEG_RXP3 {3}
PCIE_TX3N U29 CPEG_RXN3 C232 EV@0.1U/10V_4X PEG_RXN3 {3}
PCIE_TX4P T33 CPEG_RXP4 C234 EV@0.1U/10V_4X PEG_RXP4 {3}
PCIE_TX4N T32 CPEG_RXN4 C235 EV@0.1U/10V_4X PEG_RXN4 {3}
PCIE_TX5P T30 CPEG_RXP5 C203 EV@0.1U/10V_4X PEG_RXP5 {3}
PCIE_TX5N T29 CPEG_RXN5 C202 EV@0.1U/10V_4X PEG_RXN5 {3}
PCIE_TX6P P33 CPEG_RXP6 C236 EV@0.1U/10V_4X PEG_RXP6 {3}
PCIE_TX6N P32 CPEG_RXN6 C237 EV@0.1U/10V_4X PEG_RXN6 {3}
PCIE_TX7P P30 CPEG_RXP7 C209 EV@0.1U/10V_4X PEG_RXP7 {3}
PCIE_TX7N P29 CPEG_RXN7 C210 EV@0.1U/10V_4X PEG_RXN7 {3}
PCIE_TX8P N33 CPEG_RXP8 C238 EV@0.1U/10V_4X PEG_RXP8 {3}
PCIE_TX8N N32 CPEG_RXN8 C239 EV@0.1U/10V_4X PEG_RXN8 {3}
PCIE_TX9P N30 CPEG_RXP9 C204 EV@0.1U/10V_4X PEG_RXP9 {3}
PCIE_TX9N N29 CPEG_RXN9 C205 EV@0.1U/10V_4X PEG_RXN9 {3}
PCIE_TX10P L33 CPEG_RXP10 C240 EV@0.1U/10V_4X PEG_RXP10 {3}
PCIE_TX10N L32 CPEG_RXN10 C241 EV@0.1U/10V_4X PEG_RXN10 {3}
PCIE_TX11P L30 CPEG_RXP11 C207 EV@0.1U/10V_4X PEG_RXP11 {3}
PCIE_TX11N L29 CPEG_RXN11 C208 EV@0.1U/10V_4X PEG_RXN11 {3}
PCIE_TX12P K33 CPEG_RXP12 C206 EV@0.1U/10V_4X PEG_RXP12 {3}
PCIE_TX12N K32 CPEG_RXN12 C199 EV@0.1U/10V_4X PEG_RXN12 {3}
PCIE_TX13P J33 CPEG_RXP13 C224 EV@0.1U/10V_4X PEG_RXP13 {3}
PCIE_TX13N J32 CPEG_RXN13 C225 EV@0.1U/10V_4X PEG_RXN13 {3}
PCIE_TX14P K30 CPEG_RXP14 C226 EV@0.1U/10V_4X PEG_RXP14 {3}
PCIE_TX14N K29 CPEG_RXN14 C227 EV@0.1U/10V_4X PEG_RXN14 {3}
PCIE_TX15P H33 CPEG_RXP15 C198 EV@0.1U/10V_4X PEG_RXP15 {3}
PCIE_TX15N H32 CPEG_RXN15 C197 EV@0.1U/10V_4X PEG_RXN15 {3}
CLOCK
{8} CLK_PCIE_VGA AB35 PCIE_REFCLKP
{8} CLK_PCIE_VGA# AA36 PCIE_REFCLKN
For M97 only Madison and Park the PWRGOOD ball
is for test purposes and must be connecctd to ground
B2A
R509 MP@10K_4
AJ21 NC#1
AK21 NC#2
AH16 PWRGOOD
Ball AH16(PWRGOOD)
M92,M96-->NC
Madison,Park-->10K PD.
AA30 PERSTB
C3A
{9} VGA_PLTRST#
R430 *EV@SHORT_4
No stuff when Debug Mode
CALIBRATION
PCIE_CALRP Y30 R119 EV@1.27K/F_4
PCIE_CALRN Y29 R123 EV@2K/F_4 +1V_GPU
EV@Madison/Park_M2
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B2A

JTAG SIGNAL STUFF OPTION FOR OPTION2

SIGNALS	NORMAL MODE	JTAG MODE (DEBU
TESTEN	"1" (PU)	"1" (PU)
GPIO24_TRSTB	"0" (PD)	"1" (PU)
GPIO26_TCK	CLK	"1" (PU)
GPIO27_TMS	"1" (PU)	"1" (PU)

1.8V GPIO

B2A
NC on Park
M92,M96,Madison support

B2A
NC on Park
M92,M96,Madison support

B2A
Park Channel D-->No support
M92 Channel C&D-->No support

U20B

MUTI GFX
DVPCNTL_MVP_0
DVPCNTL_MVP_1
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCLK
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23

DPA
TXCAP_DPA3P
TXCAM_DPA3N
TX0P_DPA2P
TX0M_DPA2N
TX1P_DPA1P
TX1M_DPA1N
TX2P_DPA0P
TX2M_DPA0N

DPB
TXCBP_DPB3P
TXCBM_DPB3N
TX3P_DPB2P
TX3M_DPB2N
TX4P_DPB1P
TX4M_DPB1N
TX5P_DPB0P
TX5M_DPB0N

DPC
TXCCP_DPC3P
TXCCM_DPC3N
TX0P_DPC2P
TX0M_DPC2N
TX1P_DPC1P
TX1M_DPC1N
TX2P_DPC0P
TX2M_DPC0N

DPD
TXCDP_DPD3P
TXCDM_DPD3N
TX3P_DPD2P
TX3M_DPD2N
TX4P_DPD1P
TX4M_DPD1N
TX5P_DPD0P
TX5M_DPD0N

HDMI

I2C
SCL
SDA

GENERAL PURPOSE I/O
GPIO_0
GPIO_1
GPIO_2
GPIO_3_SMBDATA
GPIO_4_SMBCLK
GPIO_5_AC_BATT
GPIO_6
GPIO_7_BLON
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15_PWRCNTL_0
GPIO_16_SSIN
GPIO_17_THERMAL_INT
GPIO_18_HPD3
GPIO_19_CTF
GPIO_20_PWRCNTL_1
GPIO_21_BB_EN
GPIO_22_ROMCSB
GPIO_23_CLKREQB
JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4
GENERICF
GENERICG

HPD1

VREFG

PLL/CLOCK
DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
XTALIN
XTALOUT

THERMAL
DPLUS
DMINUS
TS_FDO
TSVDD
TSVSS

EV@Madison/Park_M2

U20G

LVDS CONTROL
VARY_BL
DIGON

LVTMDP
TXCLK_UP_DPF3P
TXCLK_UN_DPF3N
TXOUT_U0P_DPF2P
TXOUT_U0N_DPF2N
TXOUT_U1P_DPF1P
TXOUT_U1N_DPF1N
TXOUT_U2P_DPF0P
TXOUT_U2N_DPF0N
TXOUT_U3P
TXOUT_U3N
TXCLK_LP_DPE3P
TXCLK_LN_DPE3N
TXOUT_L0P_DPE2P
TXOUT_L0N_DPE2N
TXOUT_L1P_DPE1P
TXOUT_L1N_DPE1N
TXOUT_L2P_DPE0P
TXOUT_L2N_DPE0N
TXOUT_L3P
TXOUT_L3N

LVDS

EV@Madison/Park_M2

SCL must be tied high if not used

R473 EV@10K/F_4
R469 EV@10K/F_4

SYS_SHDN# {3,35}
Q46 *EV@2N7002_200MA
VGA_TEMP_FAIL

B2A
{22} GFX_CORE_CNTRL2

B2A
M92,M96 GPIO_21 pin control BB function.Park,Madison no suport.

B2A
M96,Madison-->support
Ball AH26-->HPD5
Ball AH24-->HPD6
M92,Park-->No support

TjMax = 110
change by VBIOS

C3A
R478 *EV@SHORT_4

R479 EV@10K/F_4
R172 *EV@10K/F_4
CLK_VGA_27M_SS_R

B2A
R724 *EV@10K_4
R723 *EV@10K_4
JTAG need Option2 for Park,Madison Engineer sample

C3A
R461 *EV@SHORT_4

R108 EV@100/F_4
R445 EV@120/F_4
27M_CLK

R514 EV@499/F_4
R517 EV@249/F_4
C735 EV@0.1U/10V_4X

Place close to Chip

+1.8V(20mA)
L5 EV@BLM15BD121SN1D_300MA
C218 EV@10U/6.3V_8X
C242 EV@1U/6.3V_4X
C279 EV@0.1U/10V_4X

5mA (5mils)
L12 EV@BLM15BD121SN1D_300MA
C265 EV@10U/6.3V_8X
C267 EV@1U/6.3V_4X
C268 EV@0.1U/10V_4X

C684 *EV@27P/50V_4N
Y3 *EV@27MHZ_20
C682 *EV@27P/50V_4N
R448 *EV@1M/F_4
R449 *EV@0_4
R447 *EV@0_4

L14 EV@BLM15BD121SN1D_300MA
C274 EV@10U/6.3V_8X
C272 EV@1U/6.3V_4X
C273 EV@0.1U/10V_4X

B2A
Madison,Park-->125mA (10mils)
M92,M96-->300mA(20mils)

R121 EV@715/F_4
C275 EV@0.1U/10V_4X
(3.3V@130mA A2VDD)

R438 EV@150/F_4
R437 EV@150/F_4
R436 EV@150/F_4
R105 EV@499/F_4

(1.8V@70mA AVDD)
L4 EV@BLM15BD121SN1D_300MA
C220 EV@0.1U/10V_4X
C214 EV@1U/6.3V_4X
C211 EV@10U/6.3V_8X

(1.8V@45mA VDD1DI/ 50mA VFF2D)
L3 EV@BLM15BD121SN1D_300MA
C193 EV@0.1U/10V_4X
C196 EV@1U/6.3V_4X
C189 EV@10U/6.3V_8X

(1.8V@1.5mA A2VDDQ)
L10 EV@BLM15BD121SN1D_300MA
C276 *EV@0.1U/10V_4X
C255 *EV@1U/6.3V_4X

B2A
Port 3
M96,Madison,Park-->support
M92-->No support
Port 4
M96,Madison-->support
M92,Park-->No support

B2A
Port7
Madison-->support
M92,M96,Park-->No support

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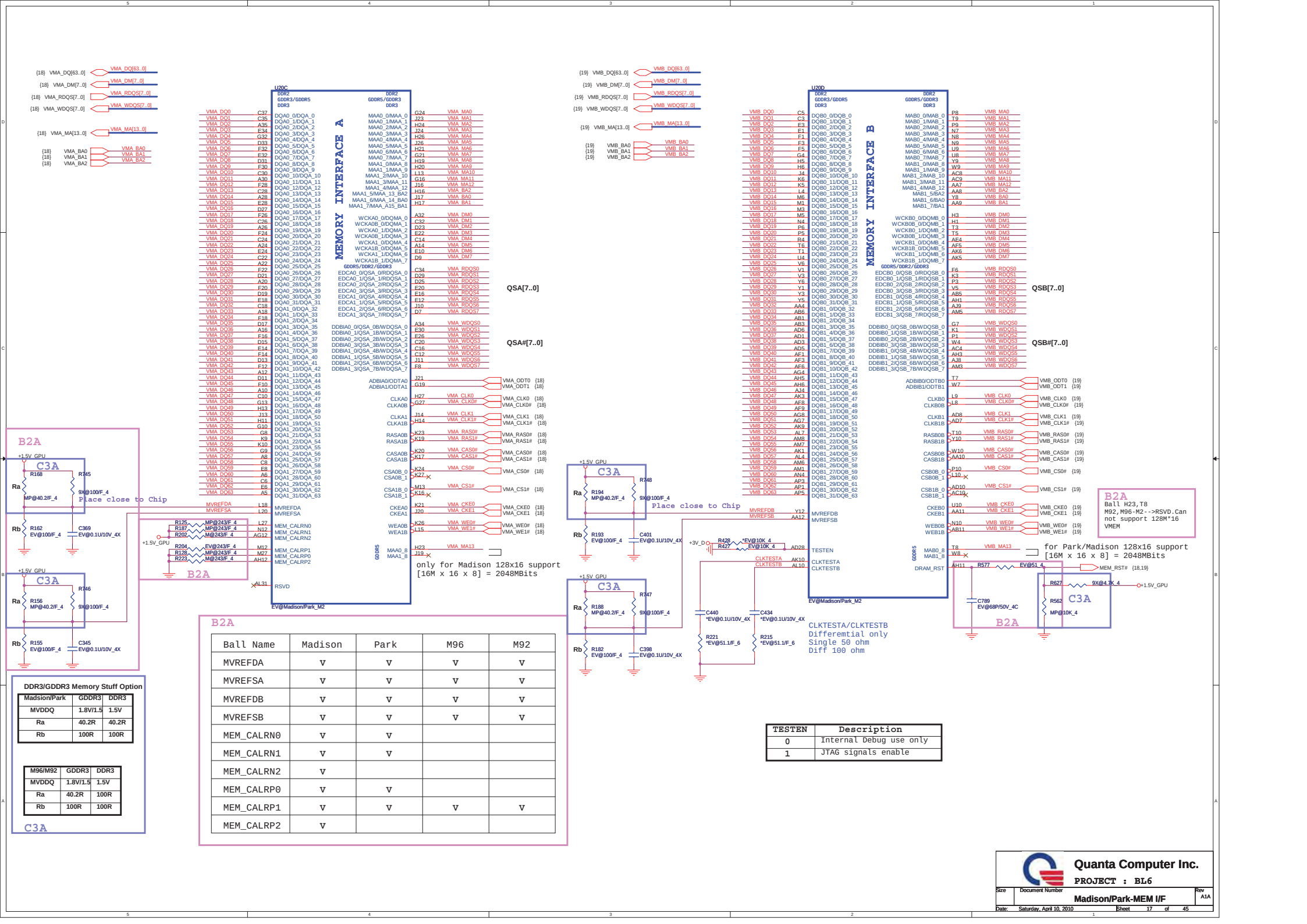

DDR3/GDDR3 Memory Stuff Option

Madsion/Park	GDDR3	DDR3
MVDDQ	1.8V/1.5	1.5V
Ra	40.2R	40.2R
Rb	100R	100R

M96/M92	GDDR3	DDR3
MVDDQ	1.8V/1.5	1.5V
Ra	40.2R	100R
Rb	100R	100R

Ball Name	Madison	Park	M96	M92
MVREFDA	V	V	V	V
MVREFSA	V	V	V	V
MVREFDB	V	V	V	V
MVREFSB	V	V	V	V
MEM_CALRN0	V	V		
MEM_CALRN1	V	V		
MEM_CALRN2	V			
MEM_CALRP0	V	V		
MEM_CALRP1	V	V	V	V
MEM_CALRP2	V			

TESTEN	Description
0	Internal Debug use only
1	JTAG signals enable

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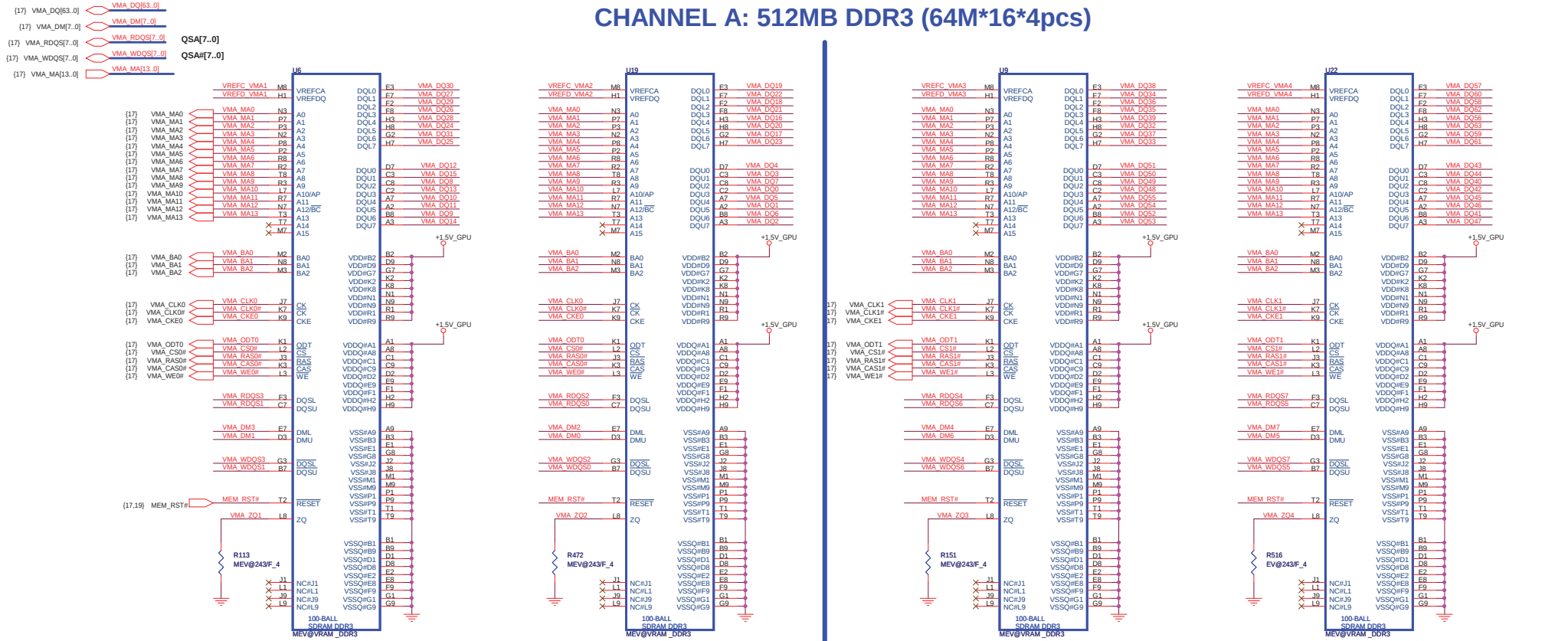
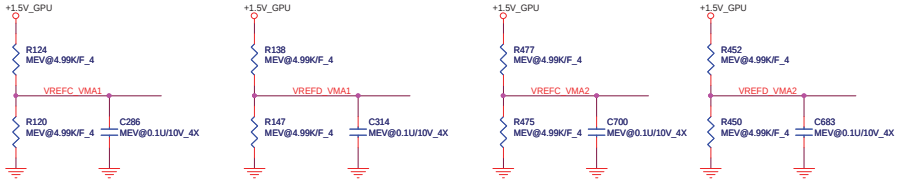
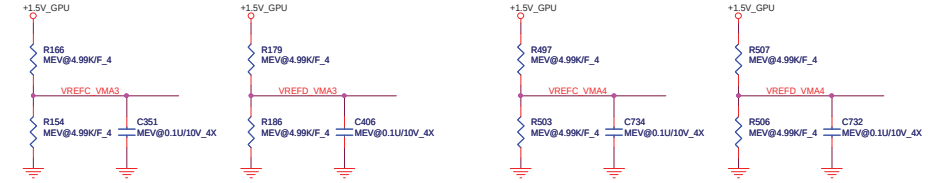
CHANNEL A: 512MB DDR3 (64M*16*4pcs)



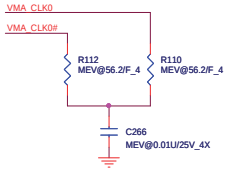
Group-A0 VREF



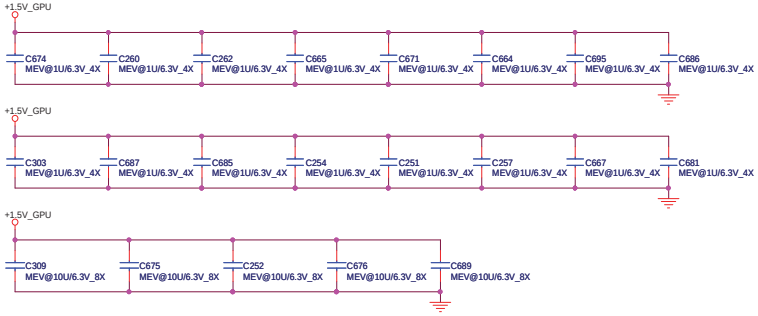
Group-A1 VREF



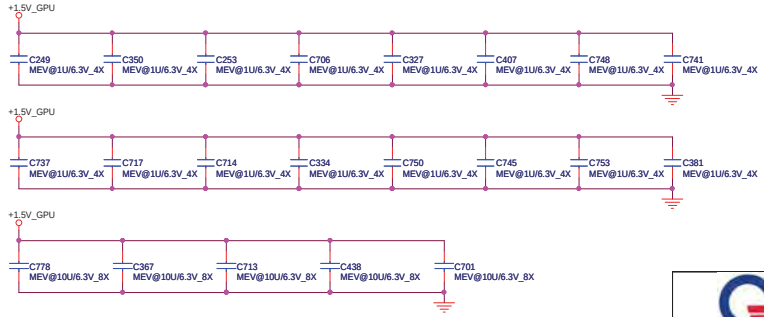
MEM_A0 CLK



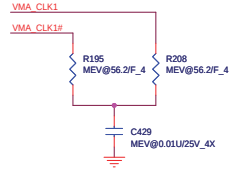
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



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	VRAM_A: DDR3-64M*16*4PCS	A1A

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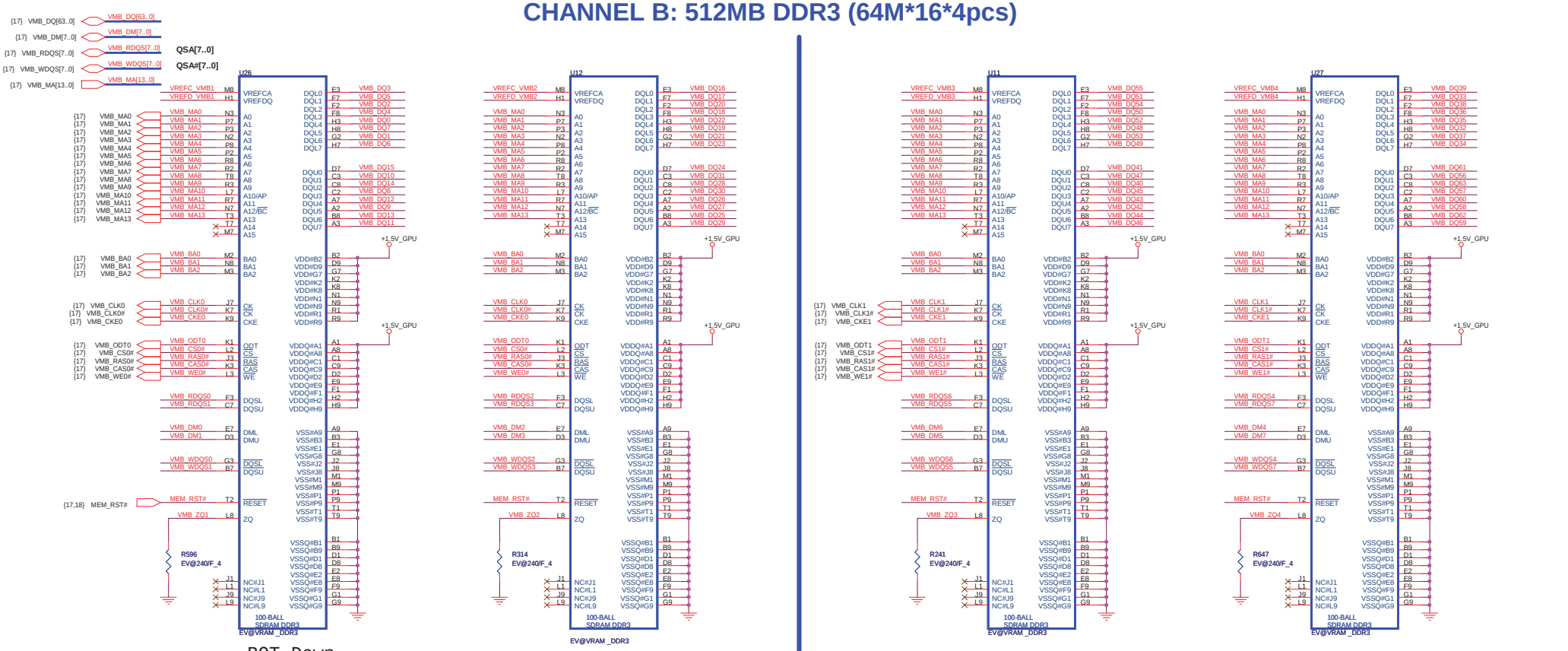
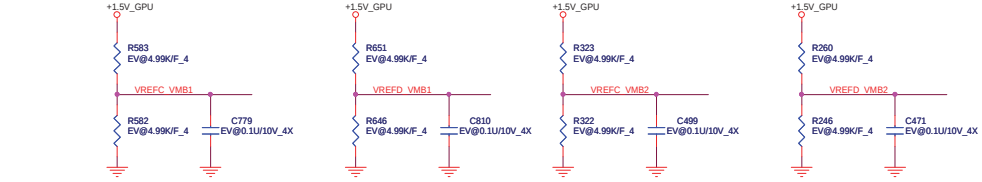
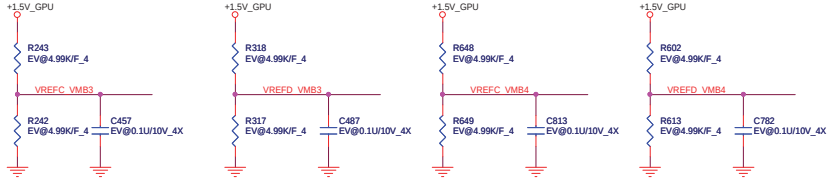
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



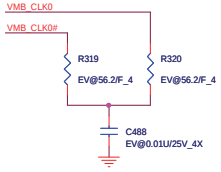
Group-B0 VREF



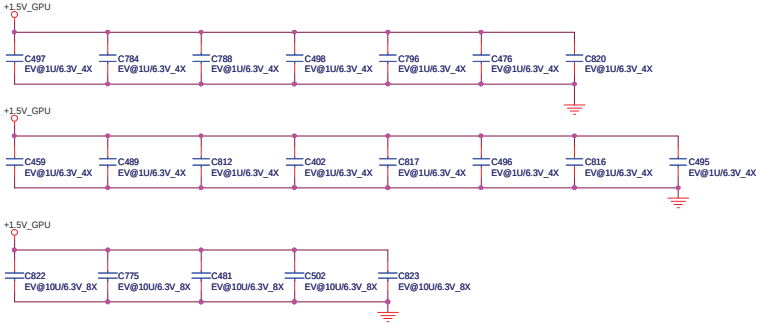
Group-B1 VREF



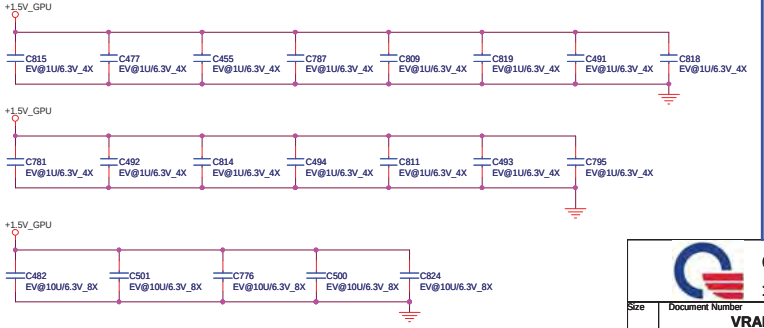
MEM_B0 CLK



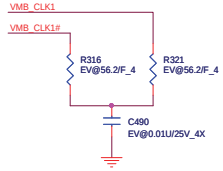
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



Quanta Computer Inc.

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	VRAM_B: DDR3-64M*16*4PCS	A1A

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For Madison and Park VDDCI and VDDC can share one common regulator

VDD/VDDQ =1.5V at 1333
VDD/VDDQ =1.8V at 1600 and 1800

(1.5V@3.4A_VDDR1)

(1.8V@400mA PCIE_VDDR)

(1.0V@2A PCIE_VDDC)

(30A or more)

(1.8V@17mA VDD_CT)

(3.3V@60mA)

(1.8V@170mA)

(1.8V@40mA PCIE_PVDD)

(1.8V@150mA MPV18)

(1.8V@50mA SPV18)

(1.0V@100mA SPV10)

(DDR3 1.12V@4A VDDCI) or more

VDDCI:33.6A

GND

POWER

Route as differential Pair

GPU +3V power
0.5A

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Madison/Park PWR_GND

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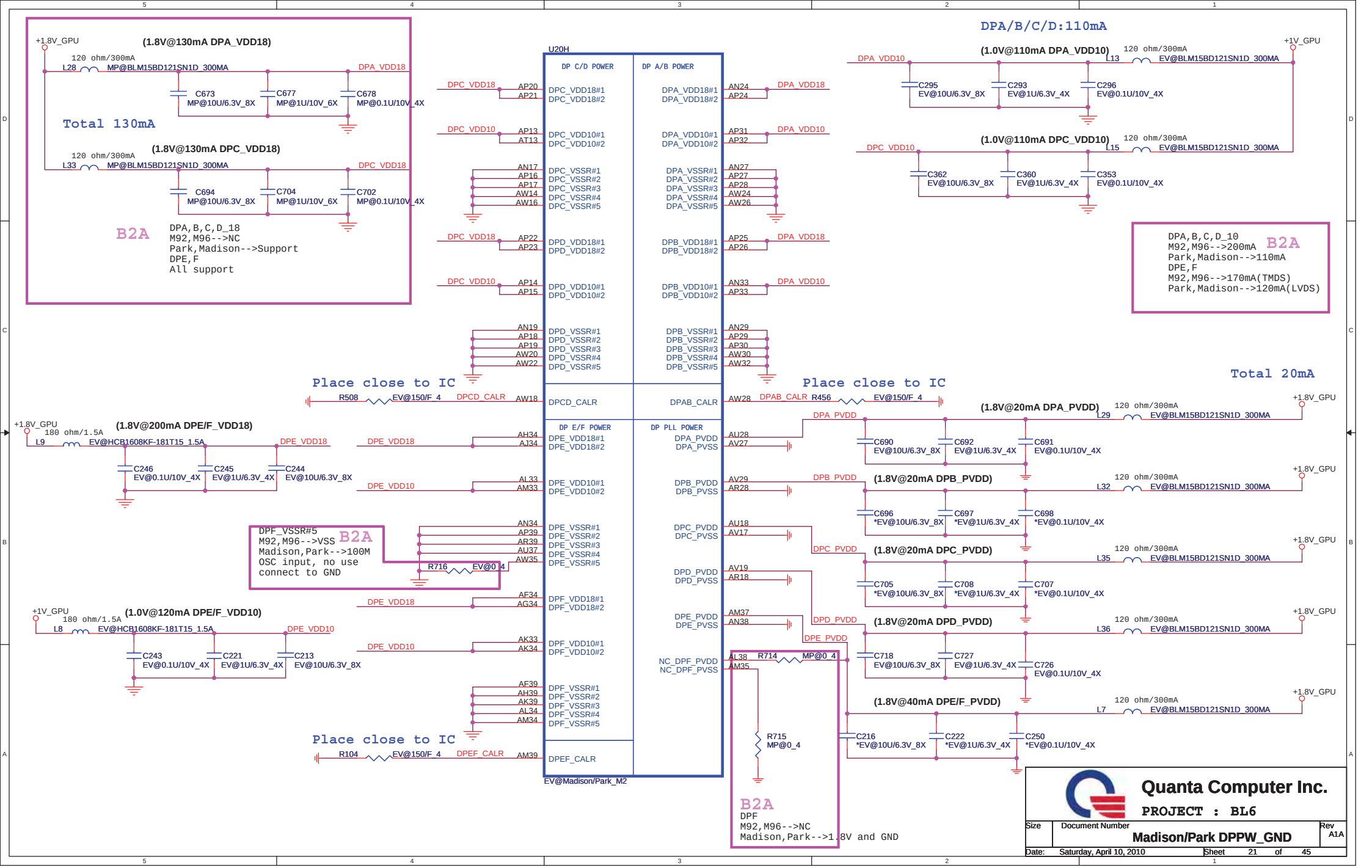
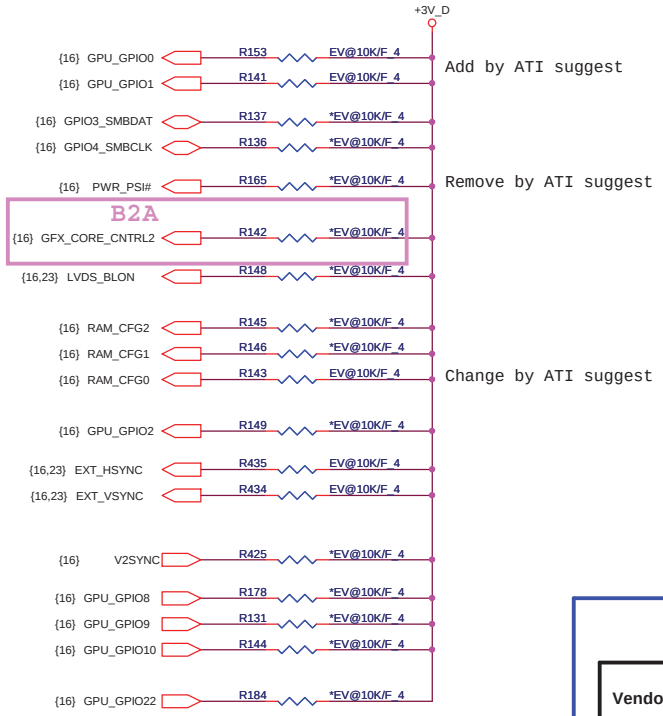

(1.8V@130mA DPA_VDD18)
+1.8V_GPU
120 ohm/300mA
L28 MP@BLM15BD121SN1D_300MA
DPA_VDD18
C673 MP@10U/6.3V_8X
C677 MP@1U/10V_6X
C678 MP@0.1U/10V_4X
Total 130mA
(1.8V@130mA DPC_VDD18)
120 ohm/300mA
L33 MP@BLM15BD121SN1D_300MA
DPC_VDD18
C694 MP@10U/6.3V_8X
C704 MP@1U/10V_6X
C702 MP@0.1U/10V_4X
B2A
DPA,B,C,D_18
M92,M96-->NC
Park,Madison-->Support
DPE,F
All support
U20H
DP C/D POWER
DP A/B POWER
DPC_VDD18 AP20 AP21 DPC_VDD18#1 DPC_VDD18#2
DPA_VDD18#1 DPA_VDD18#2 AN24 AP24 DPA_VDD18
DPC_VDD10 AP13 AT13 DPC_VDD10#1 DPC_VDD10#2
DPA_VDD10#1 DPA_VDD10#2 AP31 AP32 DPA_VDD10
AN17 AP16 AP17 AW14 AW16 DPC_VSSR#1 DPC_VSSR#2 DPC_VSSR#3 DPC_VSSR#4 DPC_VSSR#5
DPA_VSSR#1 DPA_VSSR#2 DPA_VSSR#3 DPA_VSSR#4 DPA_VSSR#5 AN27 AP27 AP28 AW24 AW26
DPC_VDD18 AP22 AP23 DPD_VDD18#1 DPD_VDD18#2
DPB_VDD18#1 DPB_VDD18#2 AP25 AP26 DPA_VDD18
DPC_VDD10 AP14 AP15 DPD_VDD10#1 DPD_VDD10#2
DPB_VDD10#1 DPB_VDD10#2 AN33 AP33 DPA_VDD10
AN19 AP18 AP19 AW20 AW22 DPD_VSSR#1 DPD_VSSR#2 DPD_VSSR#3 DPD_VSSR#4 DPD_VSSR#5
DPB_VSSR#1 DPB_VSSR#2 DPB_VSSR#3 DPB_VSSR#4 DPB_VSSR#5 AN29 AP29 AP30 AW30 AW32
Place close to IC
R508 EV@150/F_4 DPCD_CALR AW18 DPCD_CALR
DPAB_CALR AW28 DPAB_CALR R456 EV@150/F_4
DP E/F POWER
DP PLL POWER
DPE_VDD18#1 DPE_VDD18#2 AH34 AJ34 DPE_VDD18
DPA_PVDD DPA_PVSS AU28 AV27
DPE_VDD10#1 DPE_VDD10#2 AL33 AM33 DPE_VDD10
DPB_PVDD DPB_PVSS AV29 AR28
DPC_PVDD DPC_PVSS AU18 AV17
DPD_PVDD DPD_PVSS AV19 AR18
DPE_PVDD DPE_PVSS AM37 AN38
NC_DPF_PVDD NC_DPF_PVSS AL38 AM35
DPF_VSSR#5
M92,M96-->VSS
Madison,Park-->100M
OSC input, no use
connect to GND
B2A
R716 EV@0_4
AN34 AP39 AR39 AU37 AW35 DPE_VSSR#1 DPE_VSSR#2 DPE_VSSR#3 DPE_VSSR#4 DPE_VSSR#5
DPE_VDD18 AF34 AG34 DPF_VDD18#1 DPF_VDD18#2
DPE_VDD10 AK33 AK34 DPF_VDD10#1 DPF_VDD10#2
AF39 AH39 AK39 AL34 AM34 DPF_VSSR#1 DPF_VSSR#2 DPF_VSSR#3 DPF_VSSR#4 DPF_VSSR#5
Place close to IC
R104 EV@150/F_4 DPEF_CALR AM39 DPEF_CALR
EV@Madison/Park_M2
(1.8V@200mA DPE/F_VDD18)
+1.8V_GPU
180 ohm/1.5A
L9 EV@HCB1608KF-181T15_1.5A
DPE_VDD18
C246 EV@0.1U/10V_4X
C245 EV@1U/6.3V_4X
C244 EV@10U/6.3V_8X
(1.0V@120mA DPE/F_VDD10)
+1V_GPU
180 ohm/1.5A
L8 EV@HCB1608KF-181T15_1.5A
DPE_VDD10
C243 EV@0.1U/10V_4X
C221 EV@1U/6.3V_4X
C213 EV@10U/6.3V_8X
R714 MP@0_4
R715 MP@0_4
B2A
DPF
M92,M96-->NC
Madison,Park-->1.8V and GND
DPA/B/C/D:110mA
(1.0V@110mA DPA_VDD10)
DPA_VDD10
120 ohm/300mA
L13 EV@BLM15BD121SN1D_300MA
+1V_GPU
C295 EV@10U/6.3V_8X
C293 EV@1U/6.3V_4X
C296 EV@0.1U/10V_4X
(1.0V@110mA DPC_VDD10)
DPC_VDD10
120 ohm/300mA
L15 EV@BLM15BD121SN1D_300MA
C362 EV@10U/6.3V_8X
C360 EV@1U/6.3V_4X
C353 EV@0.1U/10V_4X
B2A
DPA,B,C,D_10
M92,M96-->200mA
Park,Madison-->110mA
DPE,F
M92,M96-->170mA(TMDS)
Park,Madison-->120mA(LVDS)
Total 20mA
Place close to IC
(1.8V@20mA DPA_PVDD)
DPA_PVDD
120 ohm/300mA
L29 EV@BLM15BD121SN1D_300MA
+1.8V_GPU
C690 EV@10U/6.3V_8X
C692 EV@1U/6.3V_4X
C691 EV@0.1U/10V_4X
(1.8V@20mA DPB_PVDD)
DPB_PVDD
L32 EV@BLM15BD121SN1D_300MA
C696 *EV@10U/6.3V_8X
C697 *EV@1U/6.3V_4X
C698 *EV@0.1U/10V_4X
(1.8V@20mA DPC_PVDD)
DPC_PVDD
L35 EV@BLM15BD121SN1D_300MA
C705 *EV@10U/6.3V_8X
C708 *EV@1U/6.3V_4X
C707 *EV@0.1U/10V_4X
(1.8V@20mA DPD_PVDD)
DPD_PVDD
L36 EV@BLM15BD121SN1D_300MA
C718 EV@10U/6.3V_8X
C727 EV@1U/6.3V_4X
C726 EV@0.1U/10V_4X
(1.8V@40mA DPE/F_PVDD)
DPE_PVDD
L7 EV@BLM15BD121SN1D_300MA
C216 *EV@10U/6.3V_8X
C222 *EV@1U/6.3V_4X
C250 *EV@0.1U/10V_4X
Quanta Computer Inc.
PROJECT : BL6
Size
Document Number
Madison/Park DPPW_GND
Rev A1A
Date: Saturday, April 10, 2010
Sheet 21 of 45

PIN STRAPS



Memory Aperture size	
RAM_CFG[2:0]	Size
000	128MB
001	256MB
010	64MB
011	32MB

ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

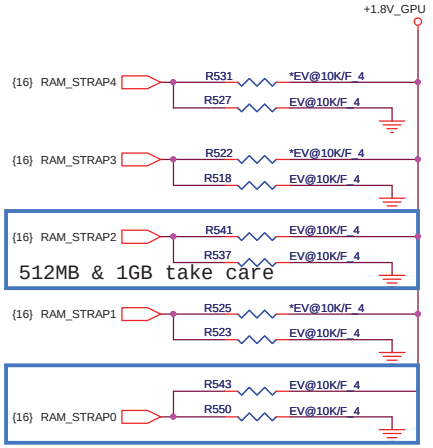
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

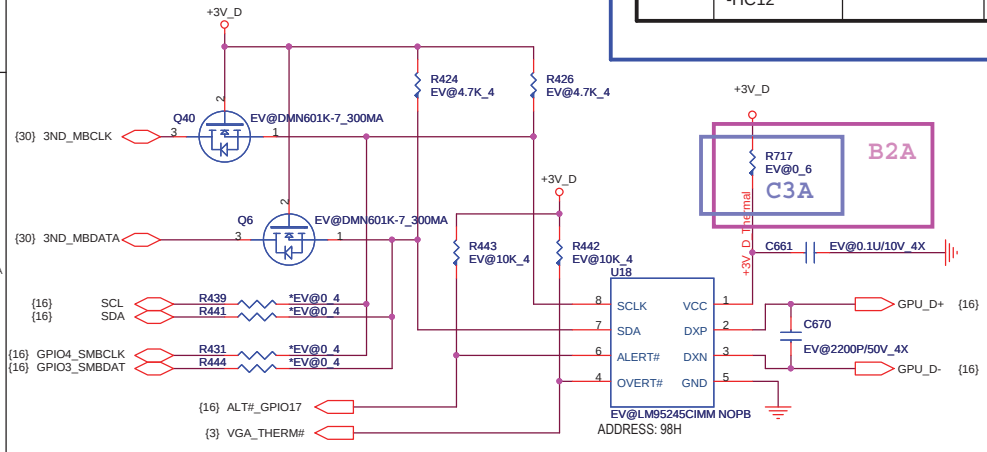
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA VIP: Video Capture Port Interface	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

DDR3 Memory TYPE

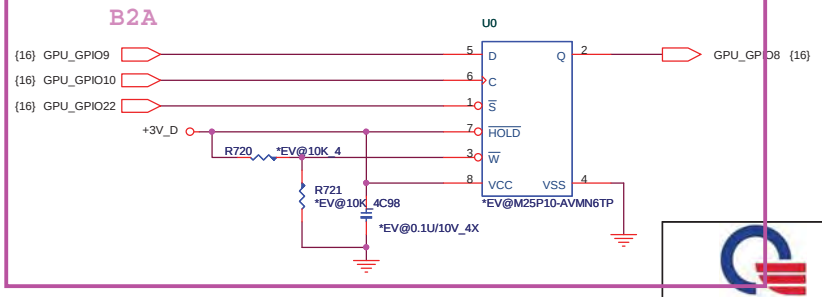
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	RAM_STRAP4 15"	RAM_STRAP4 14"
Hynix	H5TQ1G63BFR -12C	AKD5LZGTW00 (64M*16)	512MB	0	1	0	0	0	1
			1GB	0	0	0	0	0	1
			2GB	0	0	1	0	0	1
Samsung	K4W1G1646E -HC12	AKD5LGGT502 (64M*16)	512MB	0	1	0	1	0	1
			1GB	0	0	0	1	0	1
	K4W2G1646B -HC12	AKD5MGGT501	2GB	0	0	1	1	0	1



Thermal Sensor



EEPROM

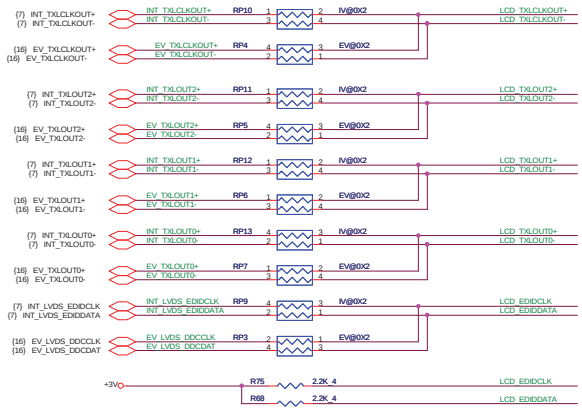


Quanta Computer Inc.

PROJECT : BL6

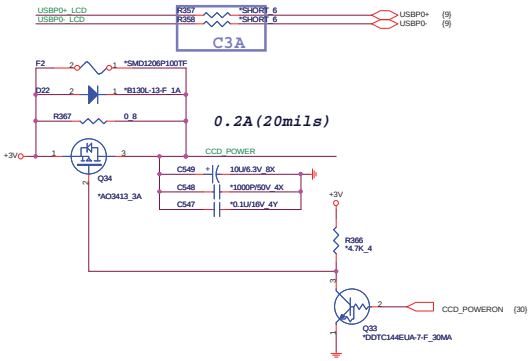
Size	Document Number	Rev
	Memory strip/Thermal/HDCP	A1A
Date: Saturday, April 10, 2010	Sheet 22 of 45	

LVDS Signals

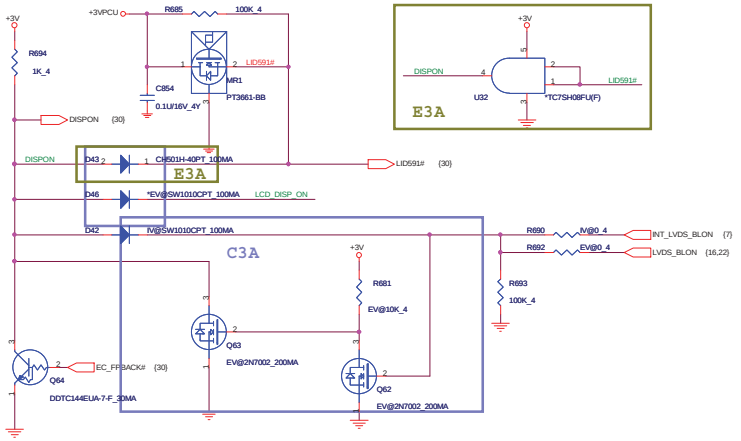


LVDS Enable

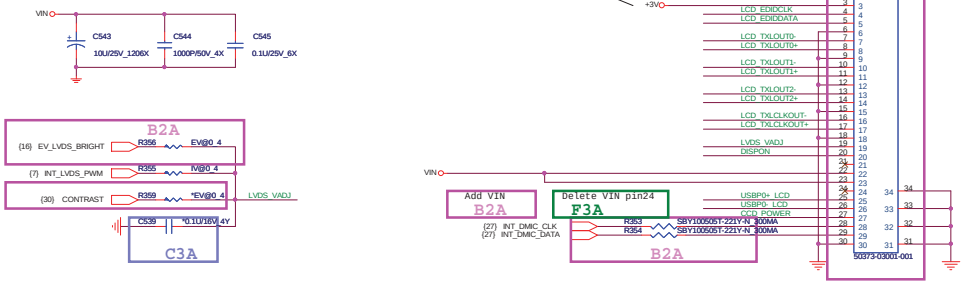
CCD



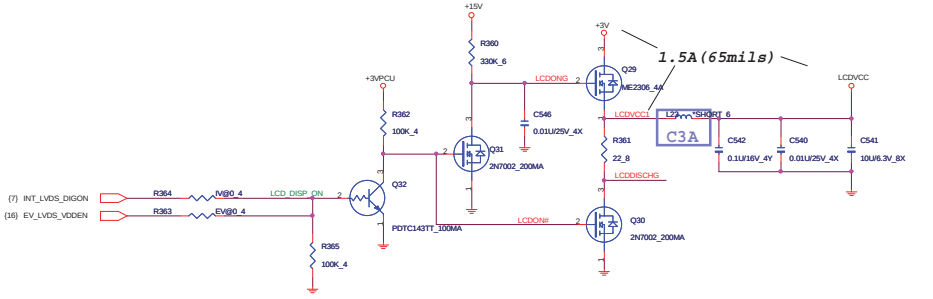
HALL SENSOR&BACK LIGHT SWITCH



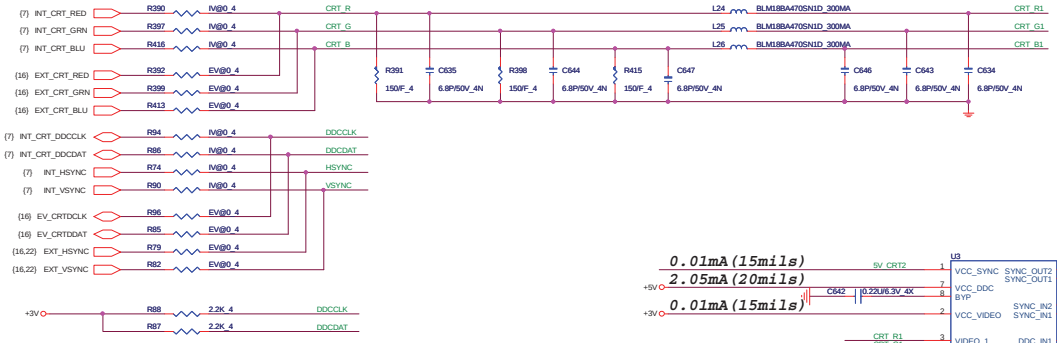
LCD Panel Module

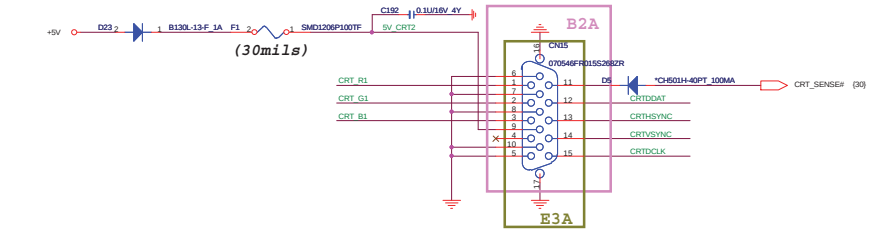


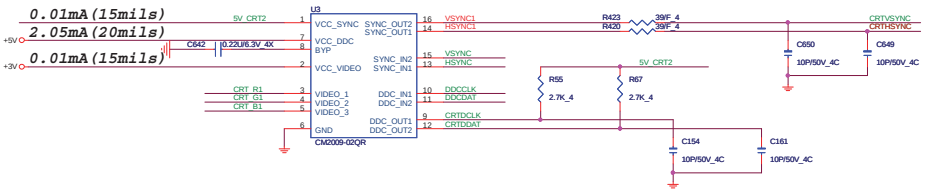
LCD POWER SWITCH

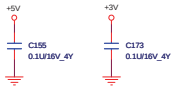


CRT









Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	LCD/LED Panel/CCD	A1A
Date: Saturday, April 10, 2010	Sheet 23 of 45	

MINI Card Slot#1 (WiFi)

Before RAMP must to remove debug card component

0.5A(30mils)

2.75A(120mils)

0.33A(30mils)

Intel module use S5 power for +3.3V
Other module keep +3V for +3.3V

MINI Card Slot#2 3G

2.75A(120mils)

0.5A(30mils)

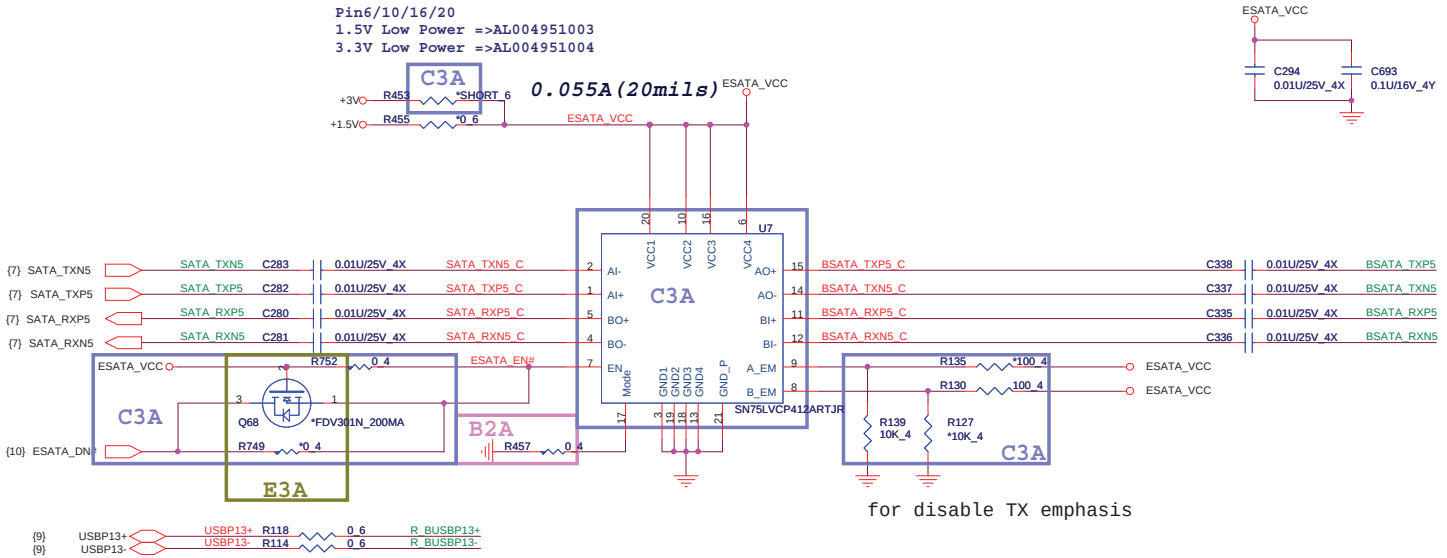
SIM CARD board to board

3G CONN

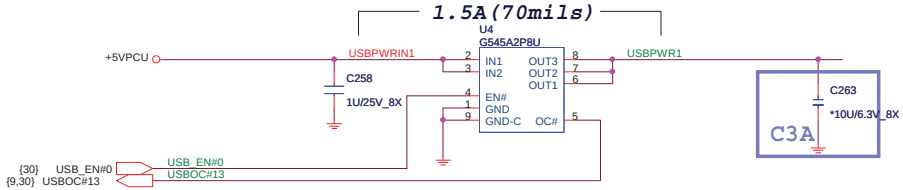
Close to 3G MINI Card

Quanta Computer Inc.	
PROJECT : BL6	
Size	Document Number: MINI CARD(WLAN/3G/SIM Card) — Rev A1A
Date: Saturday, April 10, 2010	Sheet 24 of 45

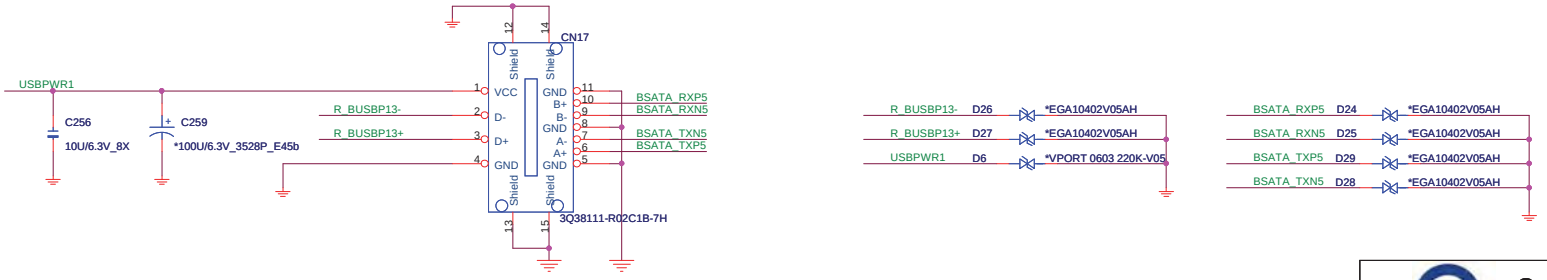
ESATA Re-driver IC



for disable TX emphasis



ESATA CONN

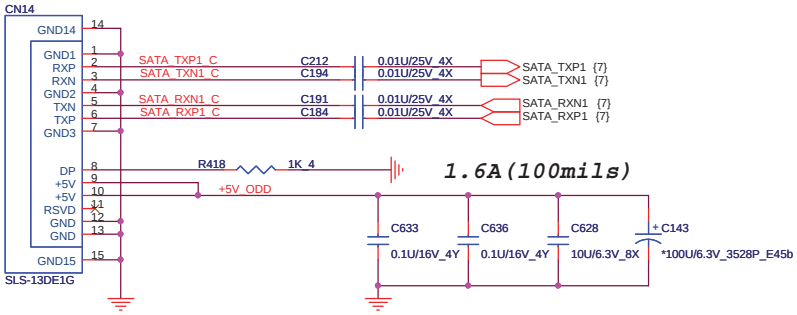


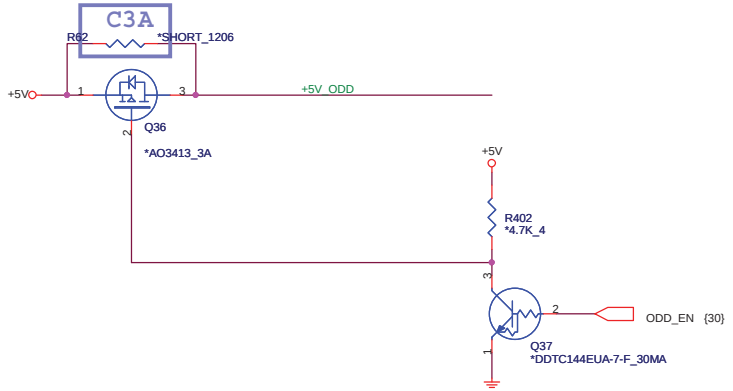
Quanta Computer Inc.

PROJECT : BL6

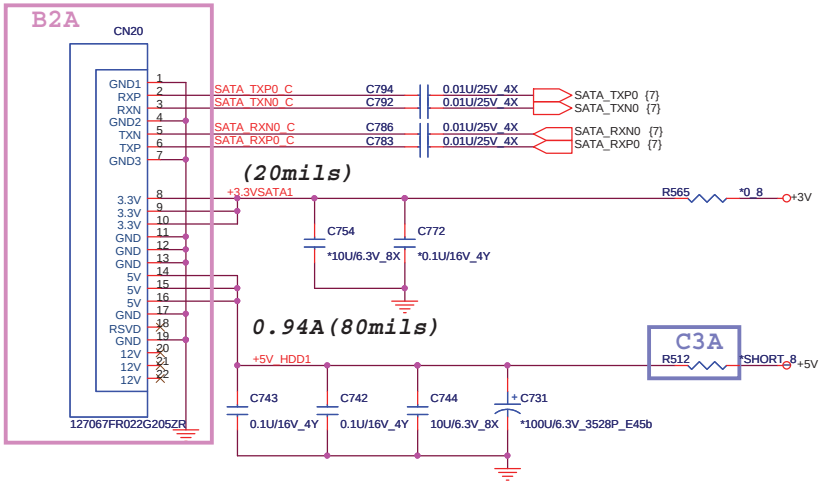
Size	Document Number	Rev
	TP/SW/ESATA/USB+Audio/LED	A1A
Date: Saturday, April 10, 2010	Sheet 25 of 45	

SATA ODD

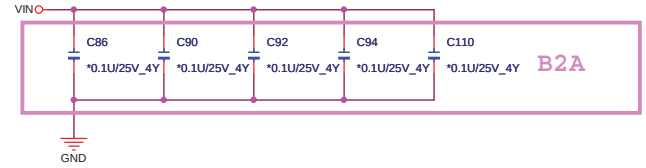


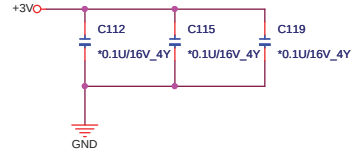


SATA HDD



EMI





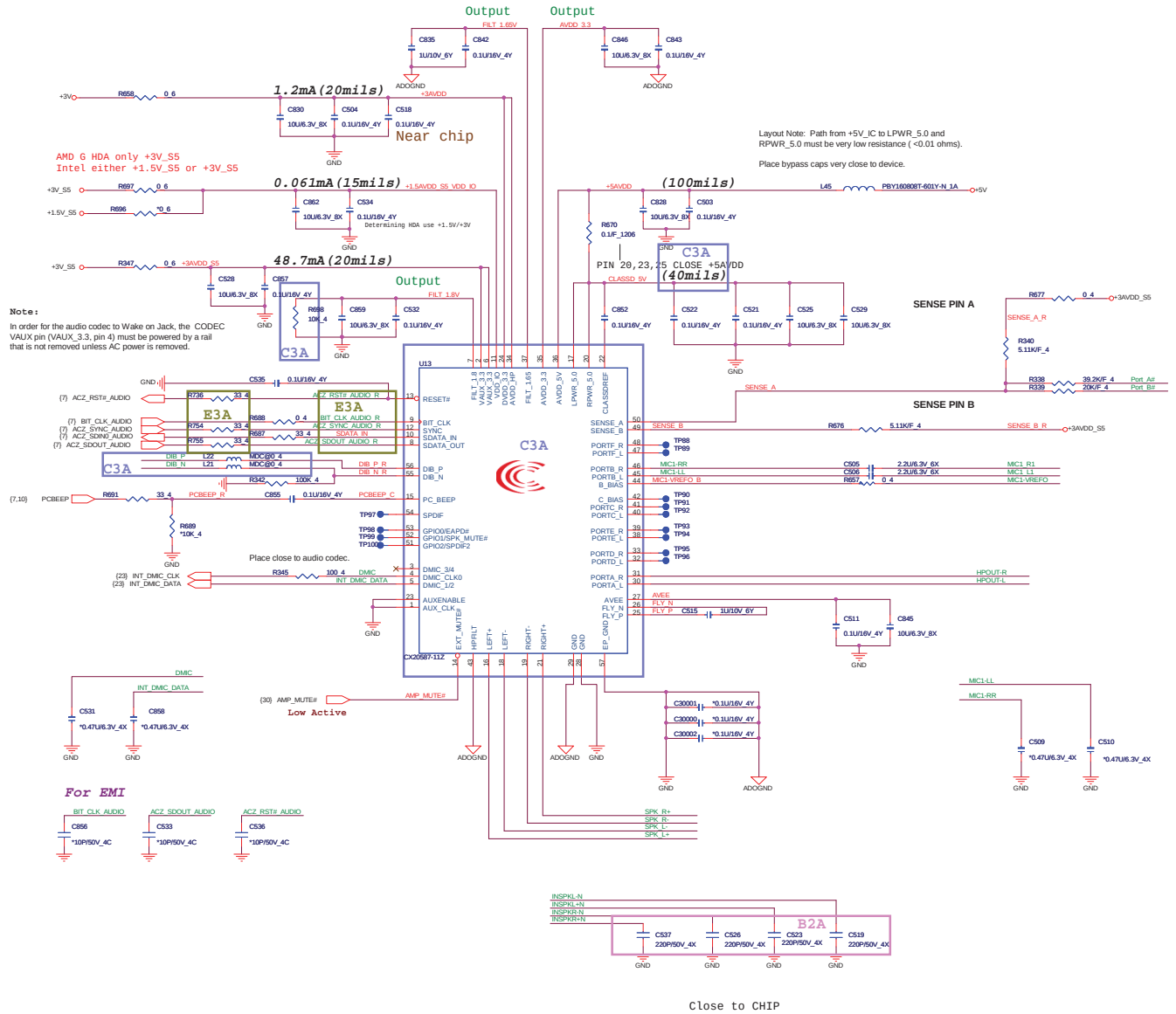
Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	HDD/ODD/EMI	A1A

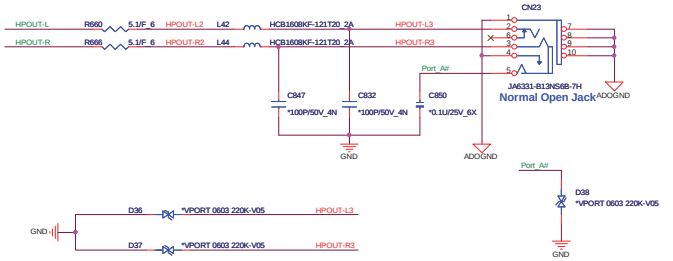
Date: Saturday, April 10, 2010 Sheet 26 of 45

Codec (CX20587)

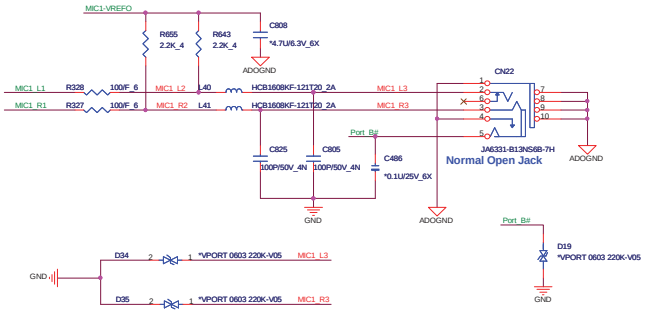


AUDIO JACKS

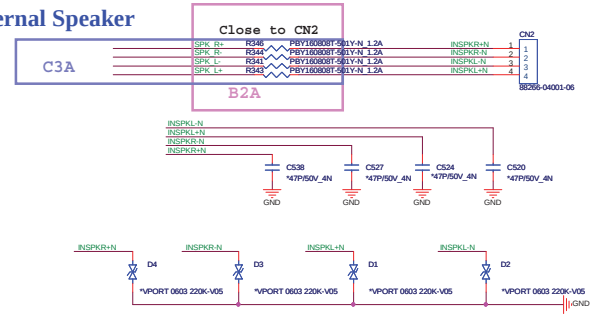
Earphone



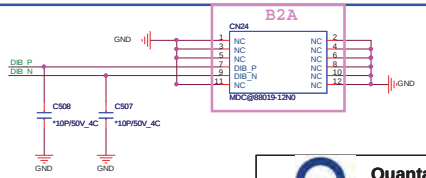
External MIC



Internal Speaker



MDC

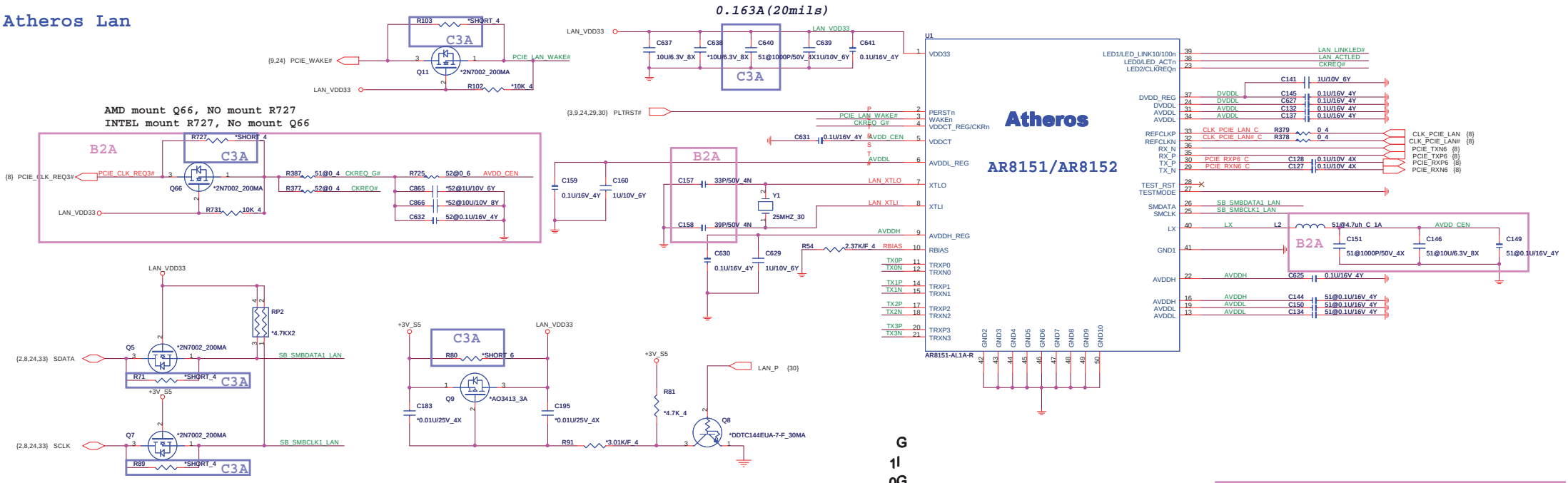


Quanta Computer Inc.		
PROJECT : BL6		
Size	Document Number: Audio Codec (CX20583)	Rev: A1A
Date: Saturday, April 10, 2010	Sheet 27 of 45	

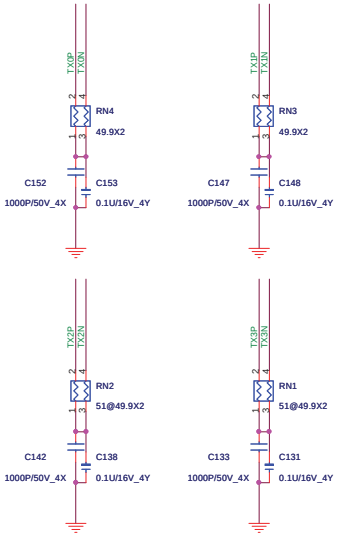
Atheros Lan

0.163A(20mils)

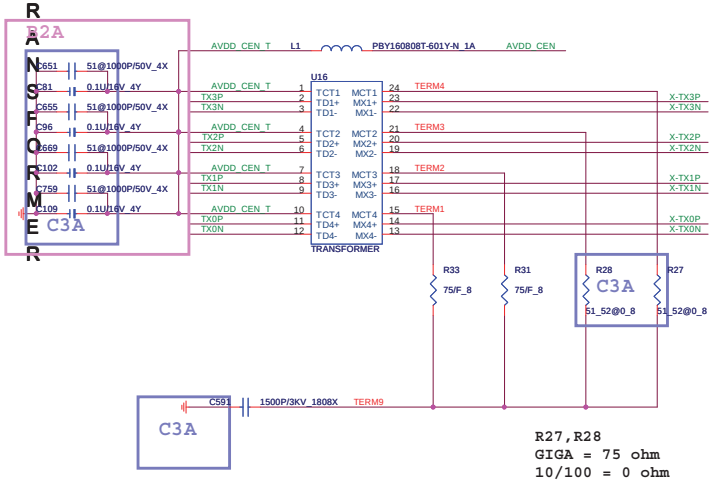
AMD mount Q66, NO mount R727
INTEL mount R727, No mount Q66



PLACE NEAR LAN IC SIDE

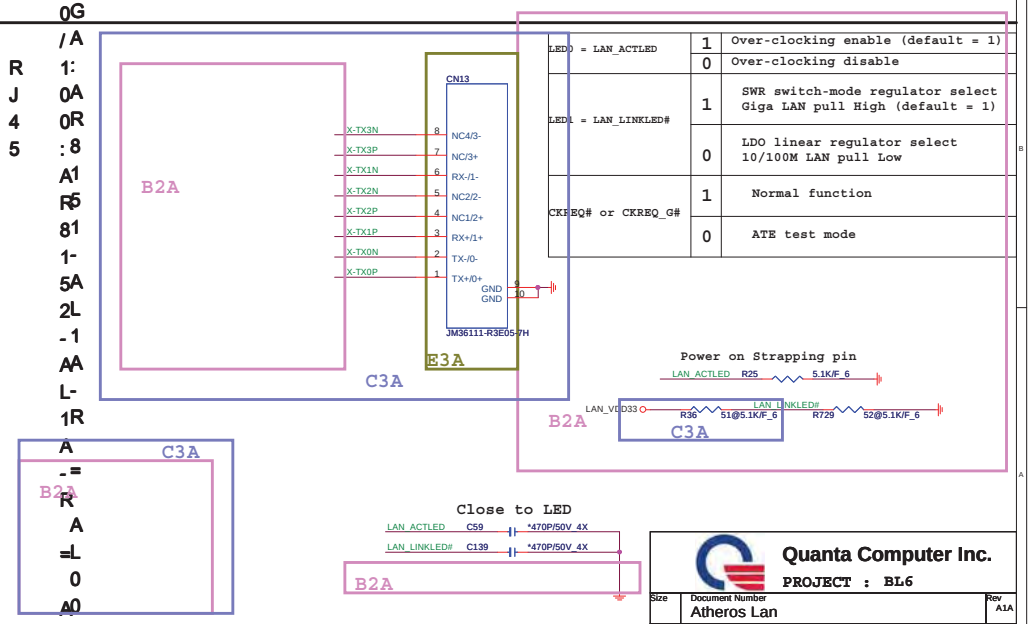


TRANSFORMER



R27,R28
GIGA = 75 ohm
10/100 = 0 ohm

RJ45



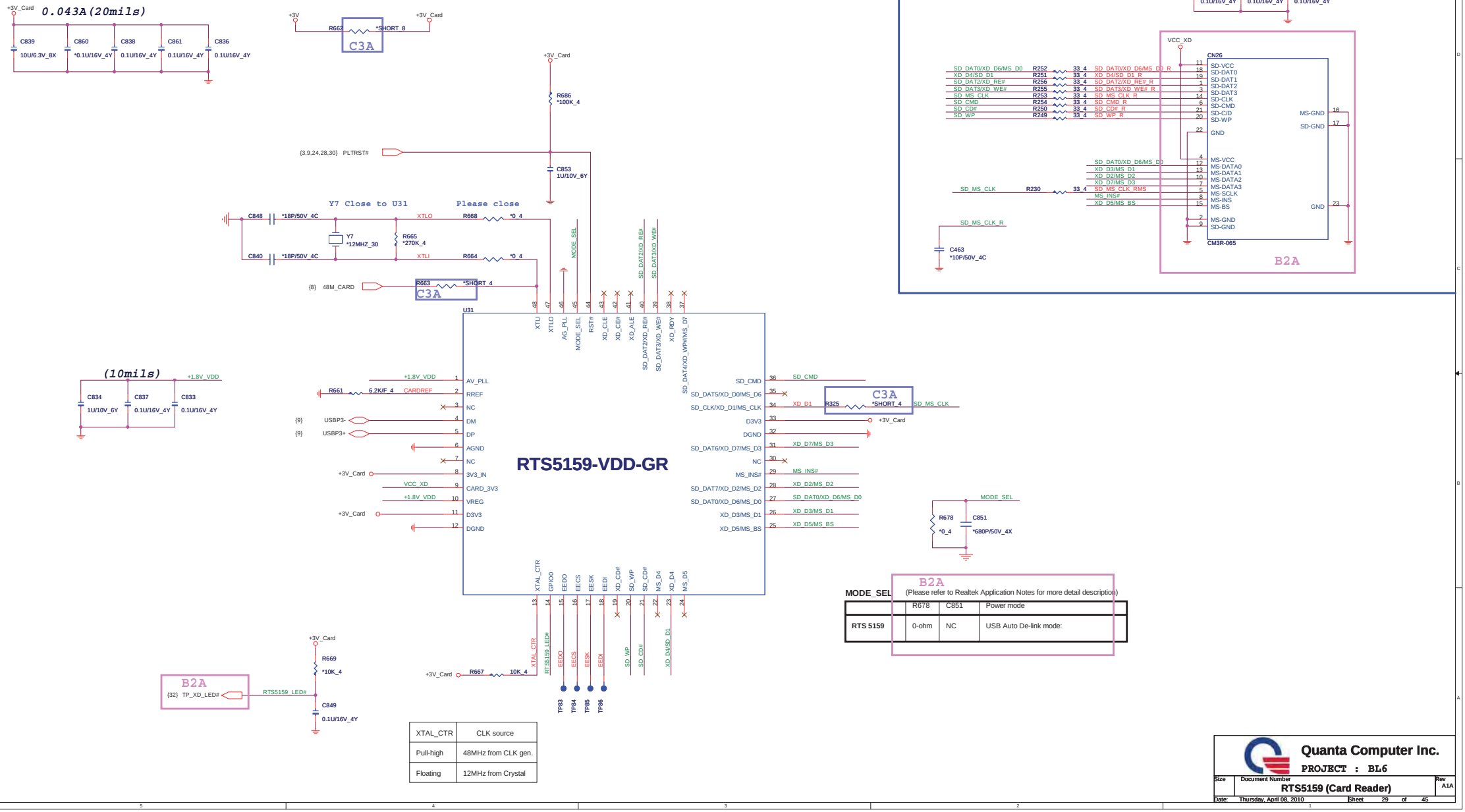
LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

Close to LED

GIGA/A1:0A0R:8A1R581-1-5A2L-1AAL-1RA-=RA=L0A0L801058102150210004

Quanta Computer Inc.	PROJECT : BL6
Size	Document Number: Atheros Lan — Rev: A1A
Date: Saturday, April 10, 2010	Sheet 28 of 45

5 IN 1 CARD READER

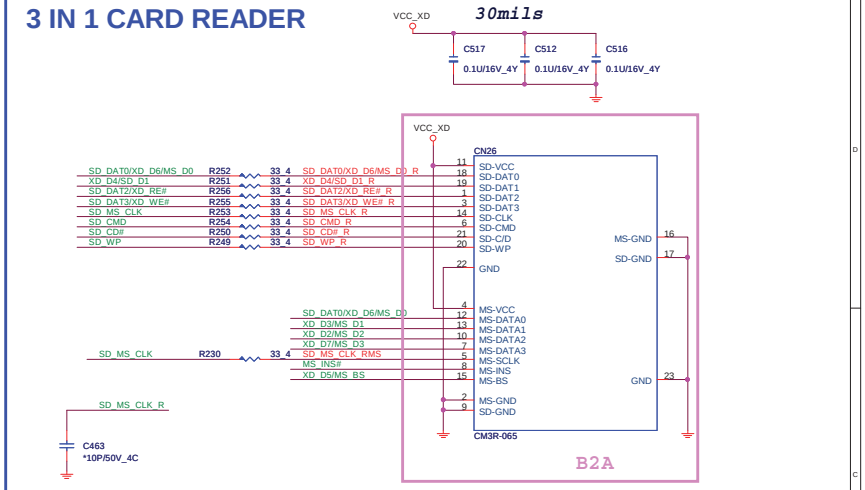


MODE_SEL	R678	C851	Power mode
RTS 5159	0-ohm	NC	USB Auto De-link mode:

B2A
(Please refer to Realtek Application Notes for more detail description)

XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal

3 IN 1 CARD READER



EC

SMBUS Table

SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	AMD SMBus	98H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H

SM BUS PU

I/O Base Address

BADDR1-0	I/O Address	
	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID

SPI FLASH

Intel	512KB	W25X40BVSSIG
AMD	2MB	W25Q16BVSSIG

INTERNAL KEYBOARD STRIP SET

HWPG

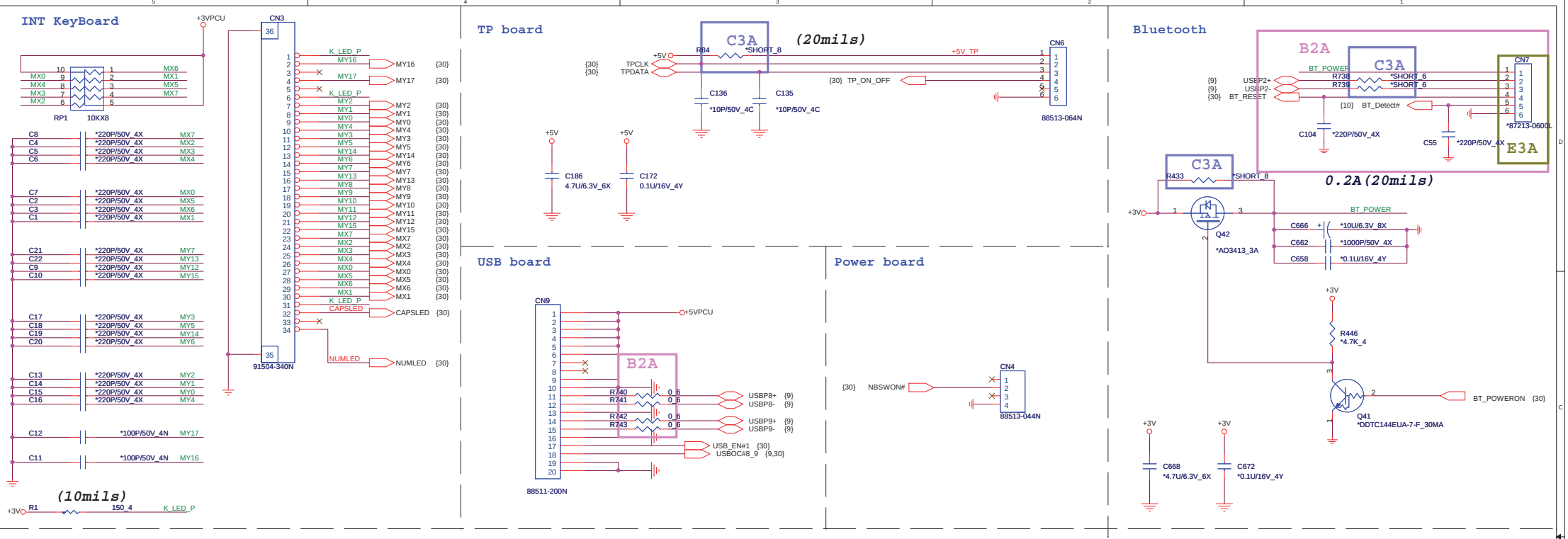
LED PU/PD

Close to U16

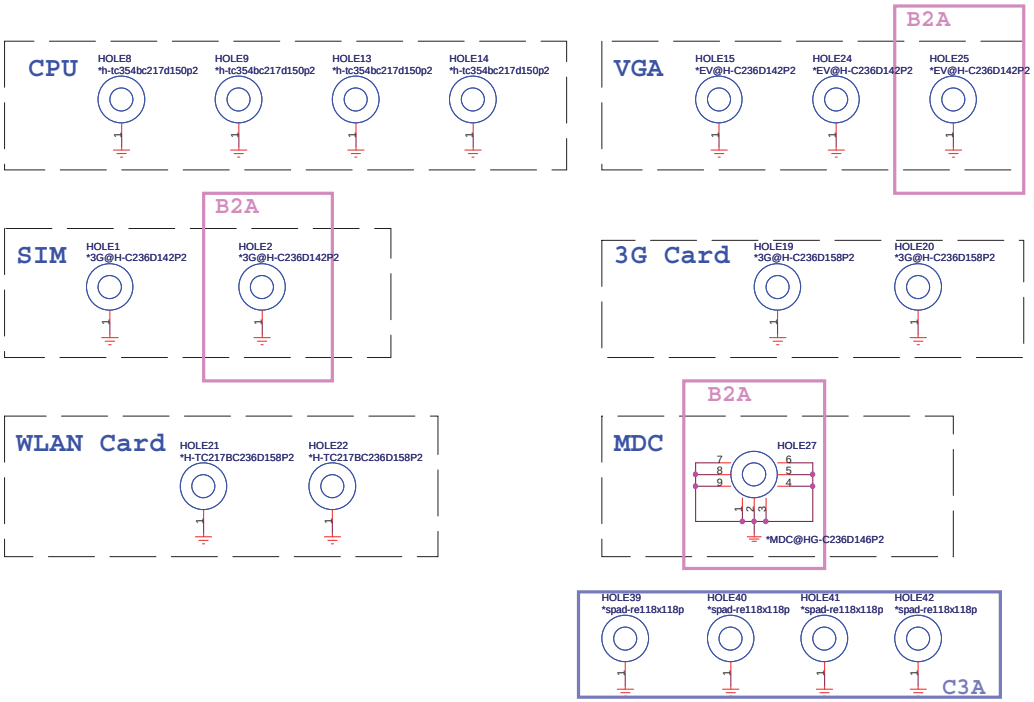
Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	EC-WPC8763LDG/WPC8769L(O)	A1A

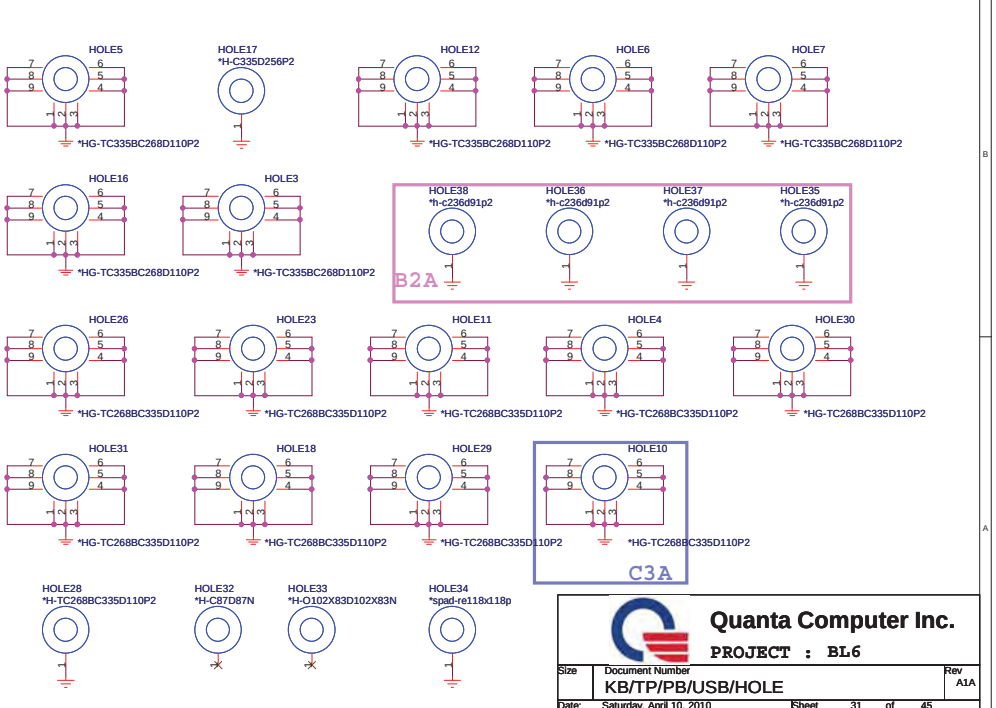
Date: Saturday, April 10, 2010 Sheet 30 of 45



NUT



HOLE



Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	KB/TP/PB/USB/HOLE	A1A
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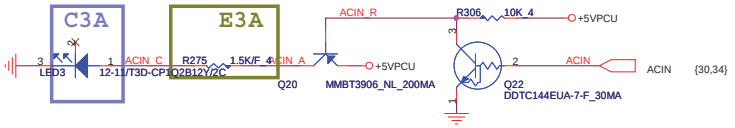
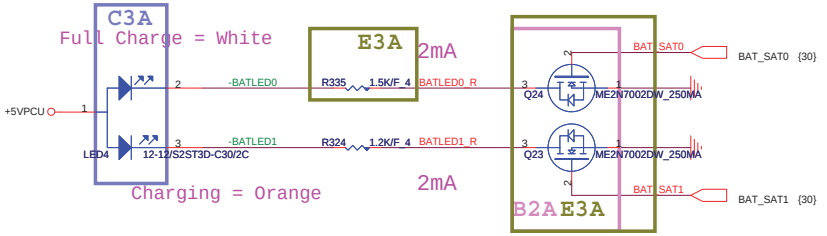
LED

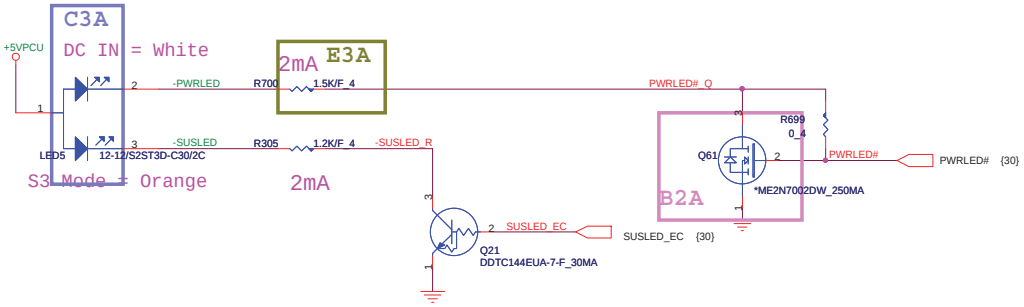
AC-IN



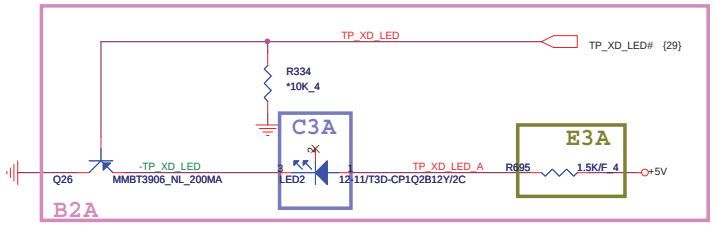
BATERRY



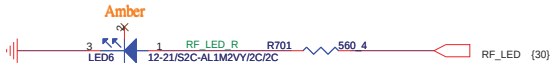
POWER



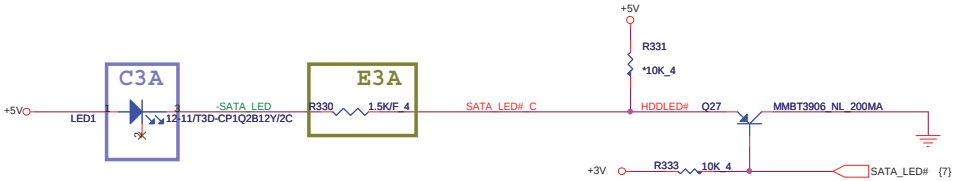
CARDREADER



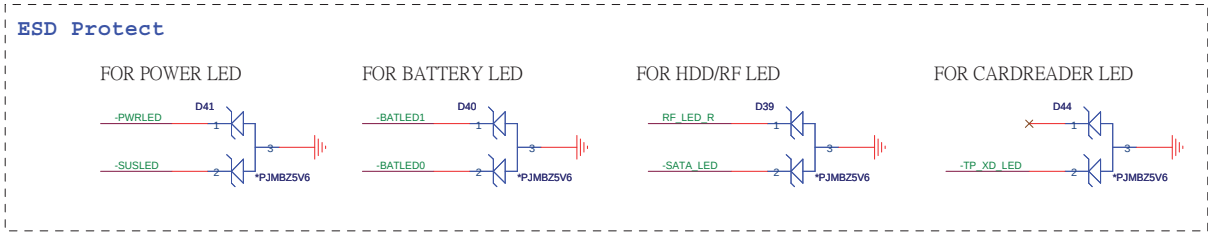
RF LED



HDD/ODD

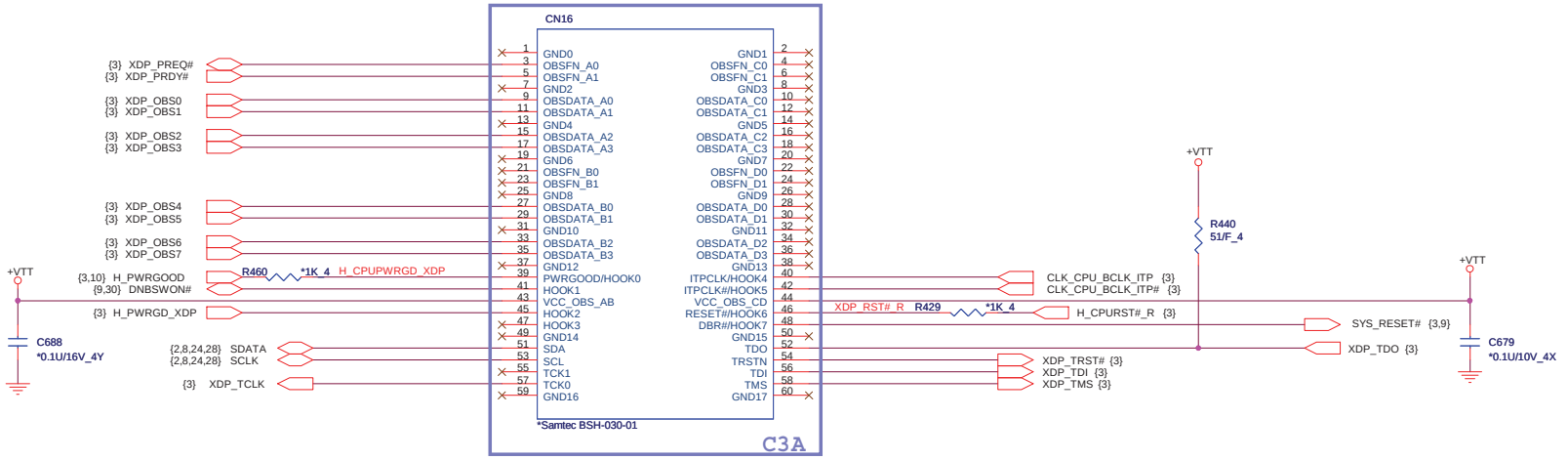


ESD Protect



Quanta Computer Inc.		
PROJECT : BL6		
Size	Document Number: LED	Rev: A1A
Date: Thursday, April 08, 2010	Sheet 32 of 45	

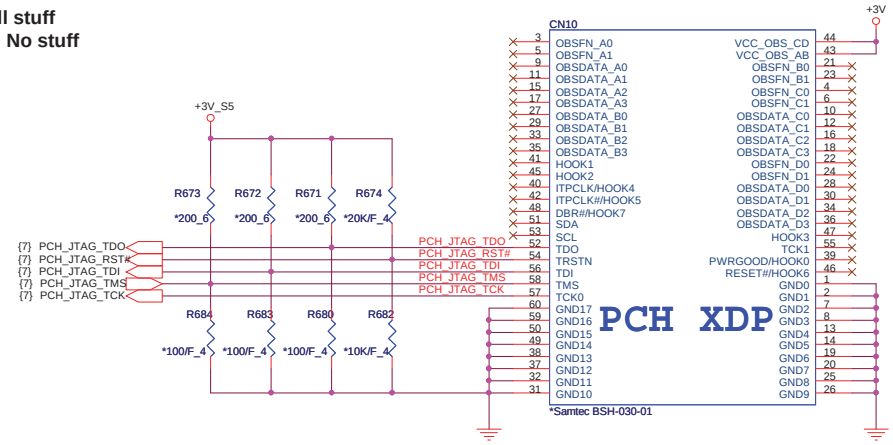
CPU XDP



Feature Set	SKU Name (S)				
	Q57	H57	H55	P55	P57
BraidWood	Y	Y	N	N	Y

PCH XDP

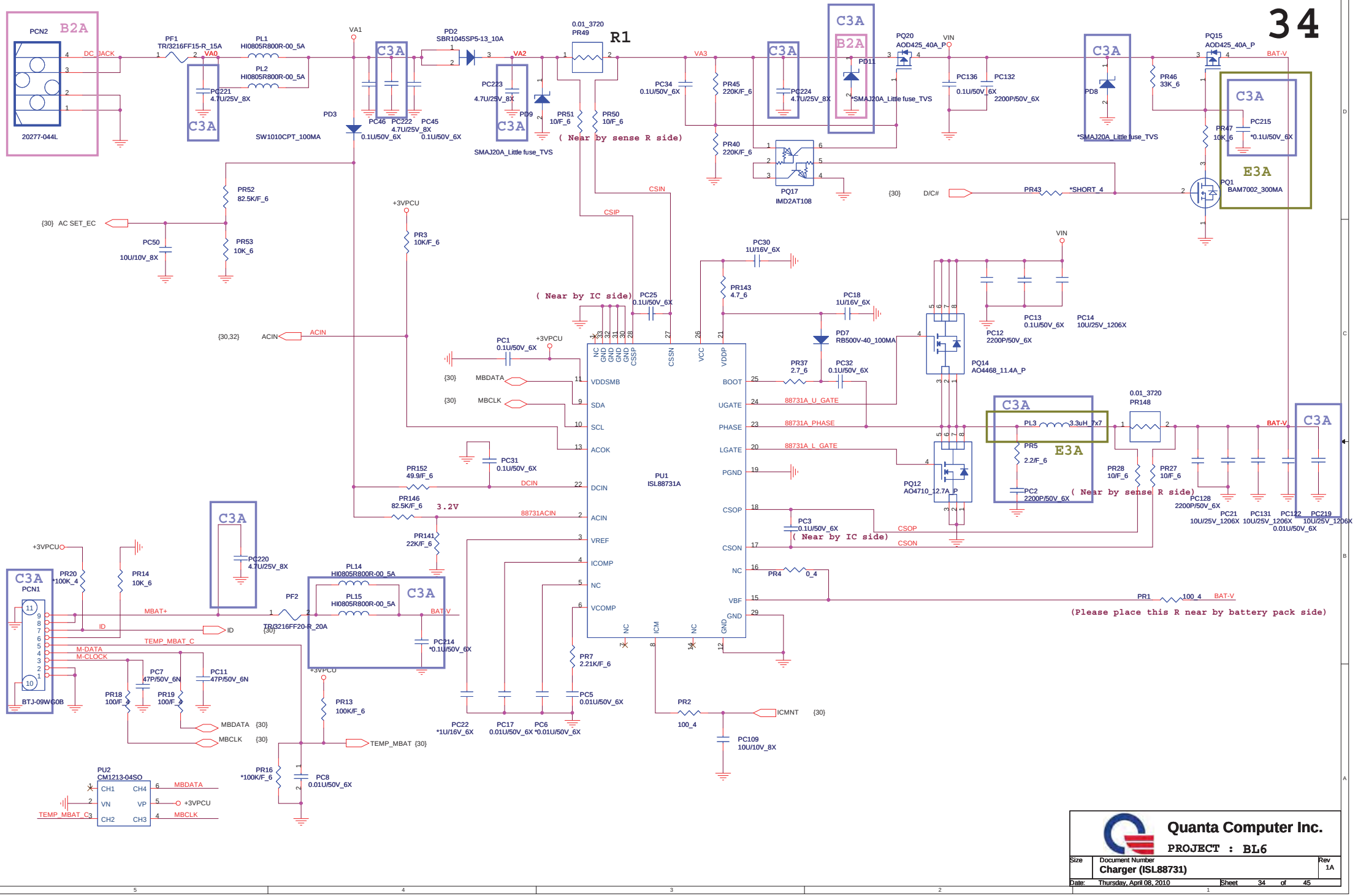
Note: For ES1/ES2 version all stuff
Production version all No stuff

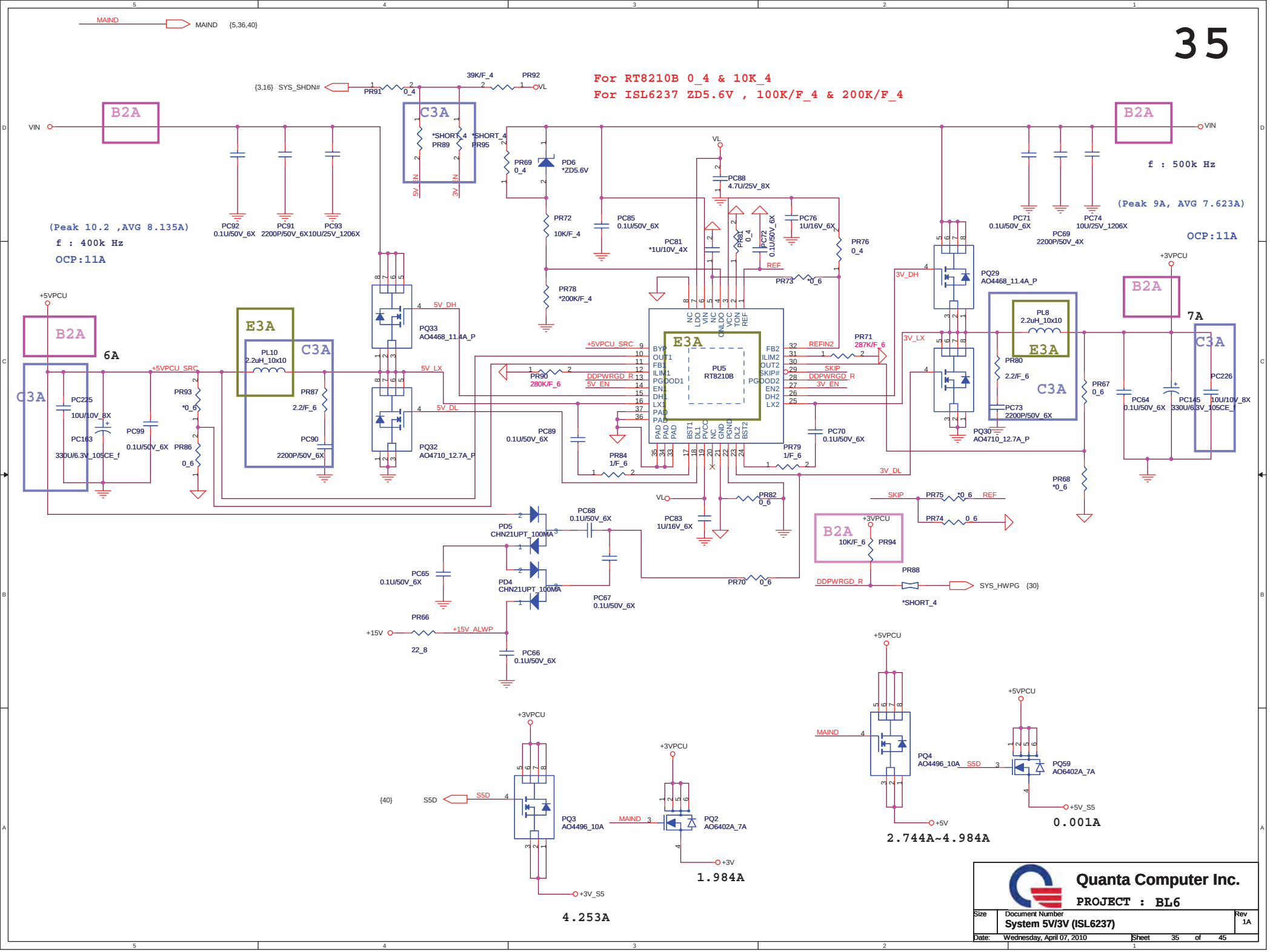


Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	NVRAM Connector	A1A
Date: Wednesday, April 07, 2010	Sheet 33 of 45	


34
PCN2
B2A
20277-044L
DC_JACK
PF1
TR/3216FF15-R_15A
PL1
HI0805R800R-00_5A
PL2
HI0805R800R-00_5A
VA0
VA1
VA2
VA3
PC221
4.7U/25V_8X
C3A
SW1010CPT_100MA
PD3
PC46
PC222
4.7U/25V_8X
PC45
0.1U/50V_6X
PD2
SBR1045SP5-13_10A
PC223
4.7U/25V_8X
PD9
SMAJ20A_Little fuse_TVS
0.01_3720
PR49
R1
PR51
10/F_6
PR50
10/F_6
(Near by sense R side)
PC34
0.1U/50V_6X
PR45
220K/F_6
PR40
220K/F_6
PC224
4.7U/25V_8X
PQ17
IMD2AT108
PD11
*SMAJ20A_Little fuse_TVS
PQ20
AOD425_40A_P
VIN
PC136
0.1U/50V_6X
PC132
2200P/50V_6X
PD8
*SMAJ20A_Little fuse_TVS
PR46
33K_6
PQ15
AOD425_40A_P
BAT-V
PR47
10K_6
PC215
*0.1U/50V_6X
E3A
PQ1
BAM7002_300MA
{30} D/C#
PR43
*SHORT_4
CSIN
CSIP
PR52
82.5K/F_6
{30} AC SET_EC
PC50
10U/10V_8X
PR53
10K_6
+3VPCU
PR3
10K/F_6
PC30
1U/16V_6X
PR143
4.7_6
(Near by IC side)
PC25
0.1U/50V_6X
PC18
1U/16V_6X
PD7
RB500V-40_100MA
PC13
0.1U/50V_6X
PC14
10U/25V_1206X
PC12
2200P/50V_6X
PQ14
AO4468_11.4A_P
{30,32} ACIN
PC1
0.1U/50V_6X
{30} MBDATA
{30} MBCLK
PU1
ISL88731A
NC
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
ICM
PR37
2.7_6
PC32
0.1U/50V_6X
88731A_U_GATE
88731A_PHASE
88731A_L_GATE
PC31
0.1U/50V_6X
PR152
49.9/F_6
DCIN
PR146
82.5K/F_6
3.2V
88731ACIN
PR141
22K/F_6
PC3
0.1U/50V_6X
(Near by IC side)
CSOP
CSON
PR4
0_4
PR1
100_4
BAT-V
(Please place this R near by battery pack side)
PQ12
AO4710_12.7A_P
PL3
3.3uH_7x7
PR5
2.2/F_6
PC2
2200P/50V_6X
(Near by sense R side)
0.01_3720
PR148
PR28
10/F_6
PR27
10/F_6
PC128
2200P/50V_6X
PC21
10U/25V_1206X
PC131
10U/25V_1206X
PC122
10U/25V_1206X
PC219
0.01U/50V_6X
PC220
4.7U/25V_8X
PL14
HI0805R800R-00_5A
PL15
HI0805R800R-00_5A
PF2
TR/3216FF20-R_20A
{30}
PC214
*0.1U/50V_6X
PCN1
BTJ-09WG0B
PR20
*100K_4
PR14
10K_6
MBAT+
ID
TEMP_MBAT_C
M-DATA
M-CLOCK
PC7
47P/50V_6N
PC11
47P/50V_6N
PR18
100/F_2
PR19
100/F_2
MBDATA {30}
MBCLK {30}
PR13
100K/F_6
TEMP_MBAT {30}
PR7
2.21K/F_6
PC5
0.01U/50V_6X
PC22
*1U/16V_6X
PC17
0.01U/50V_6X
PC6
*0.01U/50V_6X
PR2
100_4
ICMNT {30}
PC109
10U/10V_8X
PU2
CM1213-04SO
CH1
CH4
VN
VP
CH2
CH3
MBDATA
+3VPCU
MBCLK
TEMP_MBAT_C
PR16
*100K/F_6
PC8
0.01U/50V_6X
Quanta Computer Inc.
PROJECT : BL6
Size
Document Number
Charger (ISL88731)
Rev
1A
Date: Thursday, April 08, 2010
Sheet 34 of 45


35
For RT8210B 0_4 & 10K_4
For ISL6237 ZD5.6V , 100K/F_4 & 200K/F_4
MAIND {5,36,40}
{3,16} SYS_SHDN#
VIN
B2A
C3A
E3A
PR91 0_4
39K/F_4 PR92
VL
*SHORT_4 PR89
*SHORT_4 PR95
PR69 0_4
PD6 *ZD5.6V
PR72 10K/F_4
PR78 *200K/F_4
PC92 0.1U/50V_6X
PC91 2200P/50V_6X
PC93 10U/25V_1206X
(Peak 10.2 ,AVG 8.135A)
f : 400k Hz
OCP:11A
PC85 0.1U/50V_6X
PC81 *1U/10V_4X
PC88 4.7U/25V_8X
PR81 0_4
PC72 0.1U/50V_6X
PC76 1U/16V_6X
PR76 0_4
REF
PR73 *0_6
PU5 RT8210B
PR90 280K/F_6
PR71 287K/F_6
REFIN2
SKIP
DDPWRGD_R
3V_EN
5V_EN
PC89 0.1U/50V_6X
PR84 1/F_6
PR79 1/F_6
PC70 0.1U/50V_6X
PR82 0_6
PC83 1U/16V_6X
PR70 0_6
PQ33 AO4468_11.4A_P
PQ32 AO4710_12.7A_P
5V_DH
5V_LX
5V_DL
+5VPCU
6A
PC225 10U/10V_8X
PC163 330U/6.3V_105CE_f
PC99 0.1U/50V_6X
PR93 *0_6
PR86 0_6
PL10 2.2uH_10x10
PR87 2.2/F_6
PC90 2200P/50V_6X
PC71 0.1U/50V_6X
PC69 2200P/50V_4X
PC74 10U/25V_1206X
f : 500k Hz
(Peak 9A, AVG 7.623A)
OCP:11A
+3VPCU
7A
PQ29 AO4468_11.4A_P
PQ30 AO4710_12.7A_P
PL8 2.2uH_10x10
PR80 2.2/F_6
PC73 2200P/50V_6X
PR67 0_6
PC64 0.1U/50V_6X
PC145 330U/6.3V_105CE_f
PC226 10U/10V_8X
PR68 *0_6
3V_DH
3V_LX
3V_DL
PR75 *0_6
PR74 0_6
PR94 10K/F_6
PR88 *SHORT_4
SYS_HWPG {30}
PD5 CHN21UPT_100MA
PD4 CHN21UPT_100MA
PC68 0.1U/50V_6X
PC65 0.1U/50V_6X
PC67 0.1U/50V_6X
PR66 22_8
+15V
+15V_ALWP
PC66 0.1U/50V_6X
PQ4 AO4496_10A
PQ59 AO6402A_7A
+5V
+5V_S5
2.744A~4.984A
0.001A
PQ3 AO4496_10A
PQ2 AO6402A_7A
+3V
+3V_S5
1.984A
4.253A
{40} S5D
Quanta Computer Inc.
PROJECT : BL6
Size
Document Number
System 5V/3V (ISL6237)
Rev 1A
Date: Wednesday, April 07, 2010
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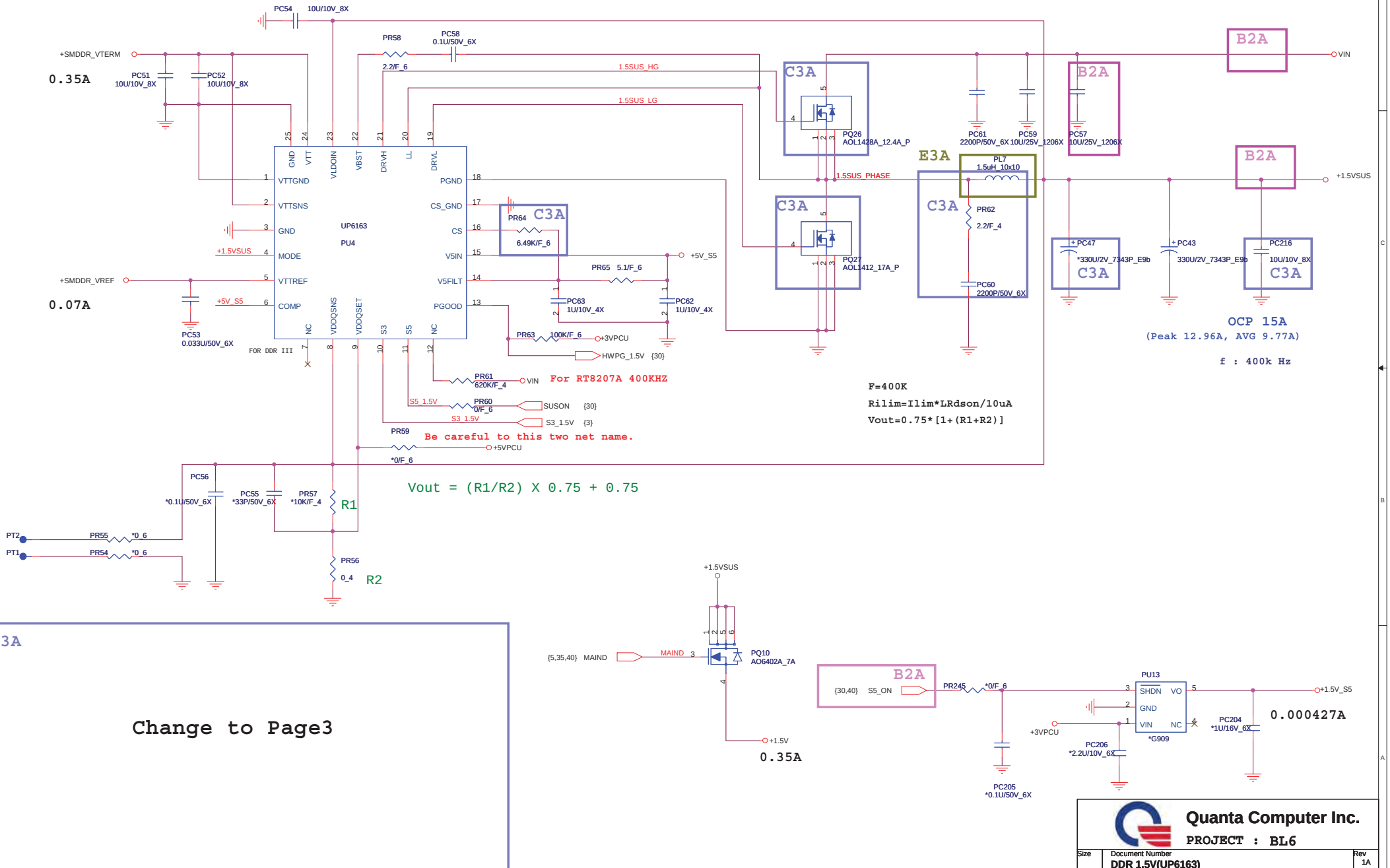
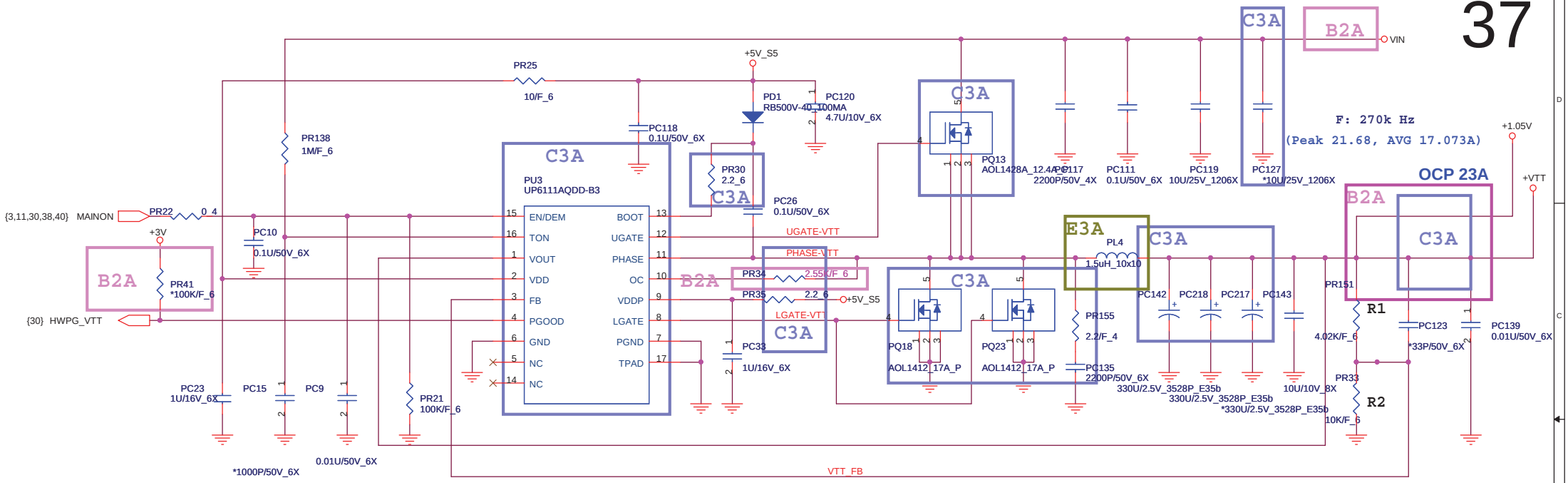


Quanta Computer Inc.		
PROJECT : BL6		
Size	Document Number: DDR 1.5V(UP6163)	Rev: 1A
Date: Wednesday, April 07, 2010	Sheet 36 of 45	



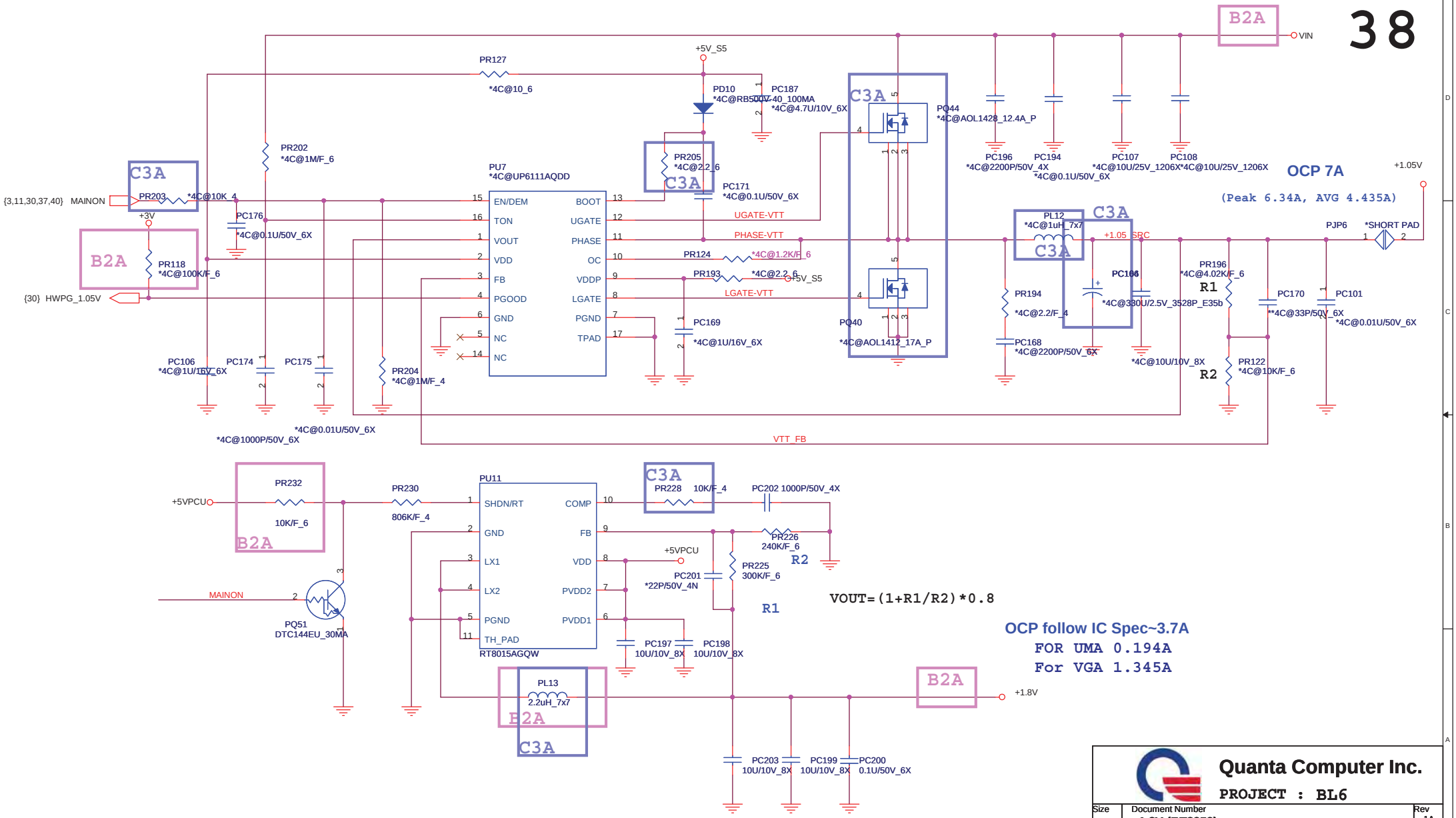
$$VOUT = (1 + R1/R2) * 0.75$$

Quanta Computer Inc.

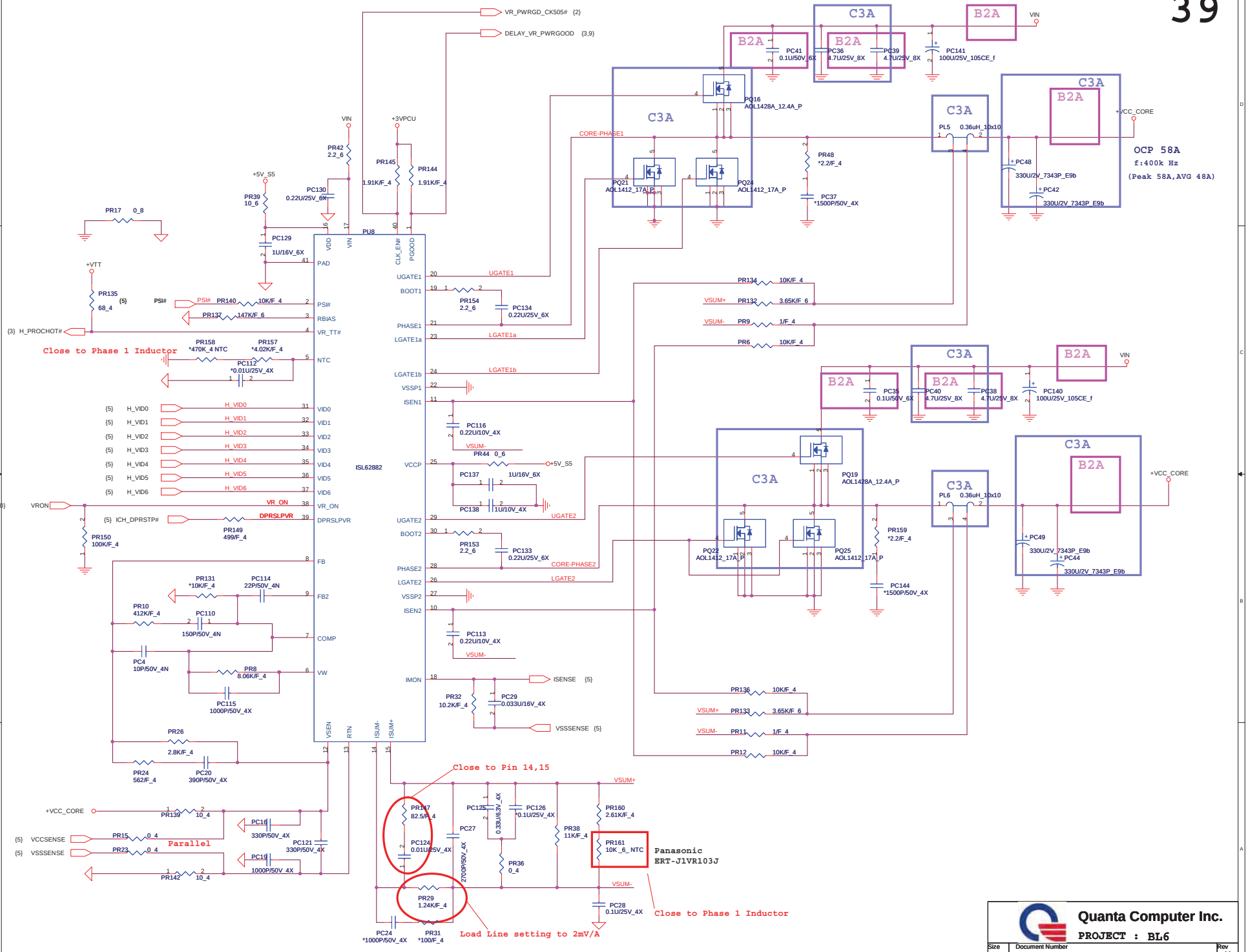
PROJECT : BL6

Size	Document Number	Rev
	+VTT (UP6111A)	1A

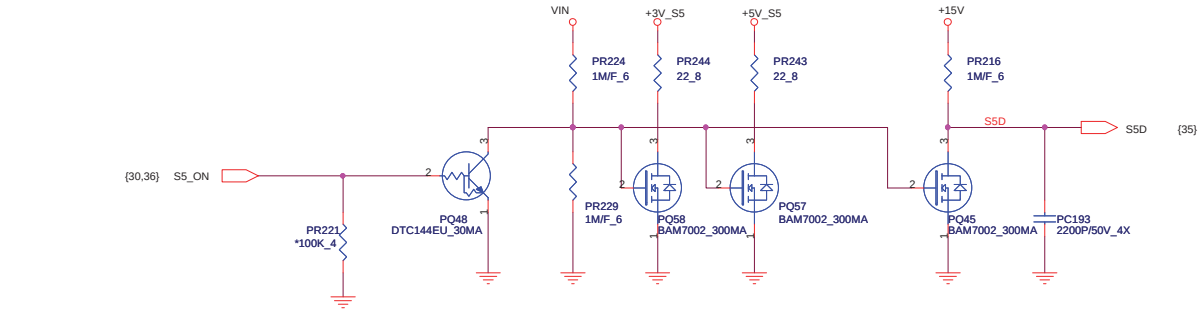
Date: Wednesday, April 07, 2010 Sheet 37 of 45

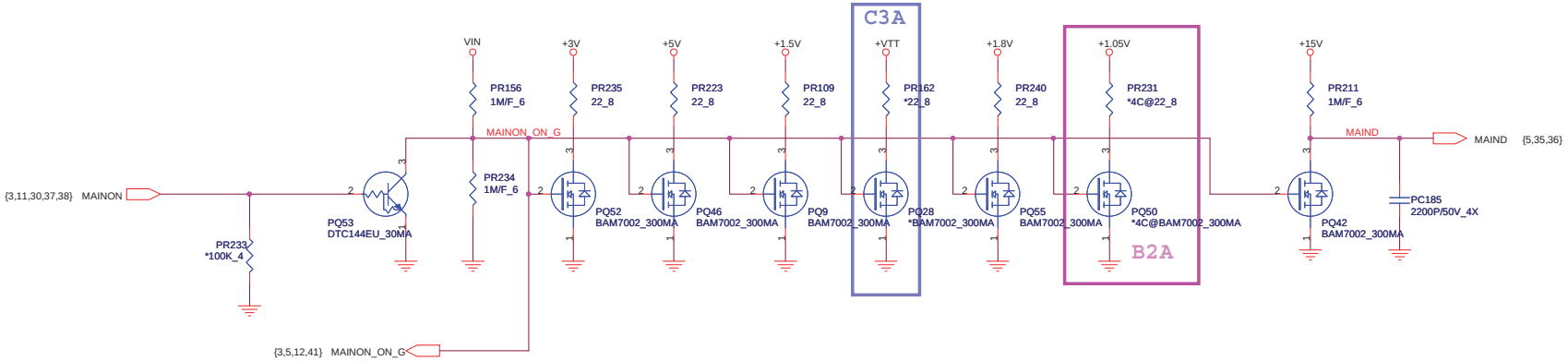


Quanta Computer Inc.		
PROJECT : BL6		
Size	Document Number: +1.8V (RT8253)	Rev: 1A
Date: Wednesday, April 07, 2010	Sheet 38 of 45	



Quanta Computer Inc.			
PROJECT : BL6			
Size	Document Number: CPU Core (ISL62882)		Rev: 1A
Date: Wednesday, April 07, 2010		Sheet 39 of 45	



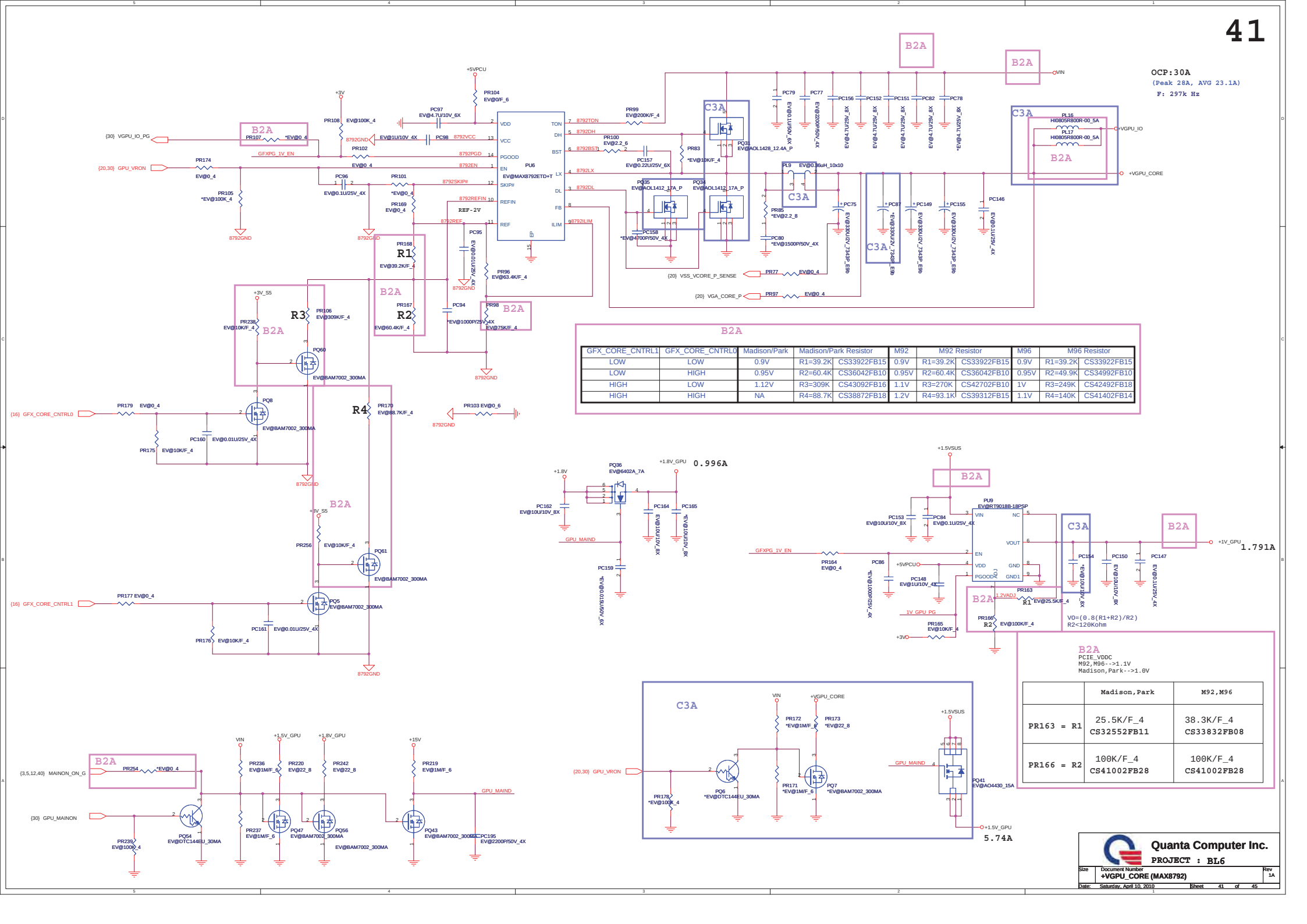


Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	Discharge (1.5V_S5/1.8V)	1A

Date: Wednesday, April 07, 2010 Sheet 40 of 45



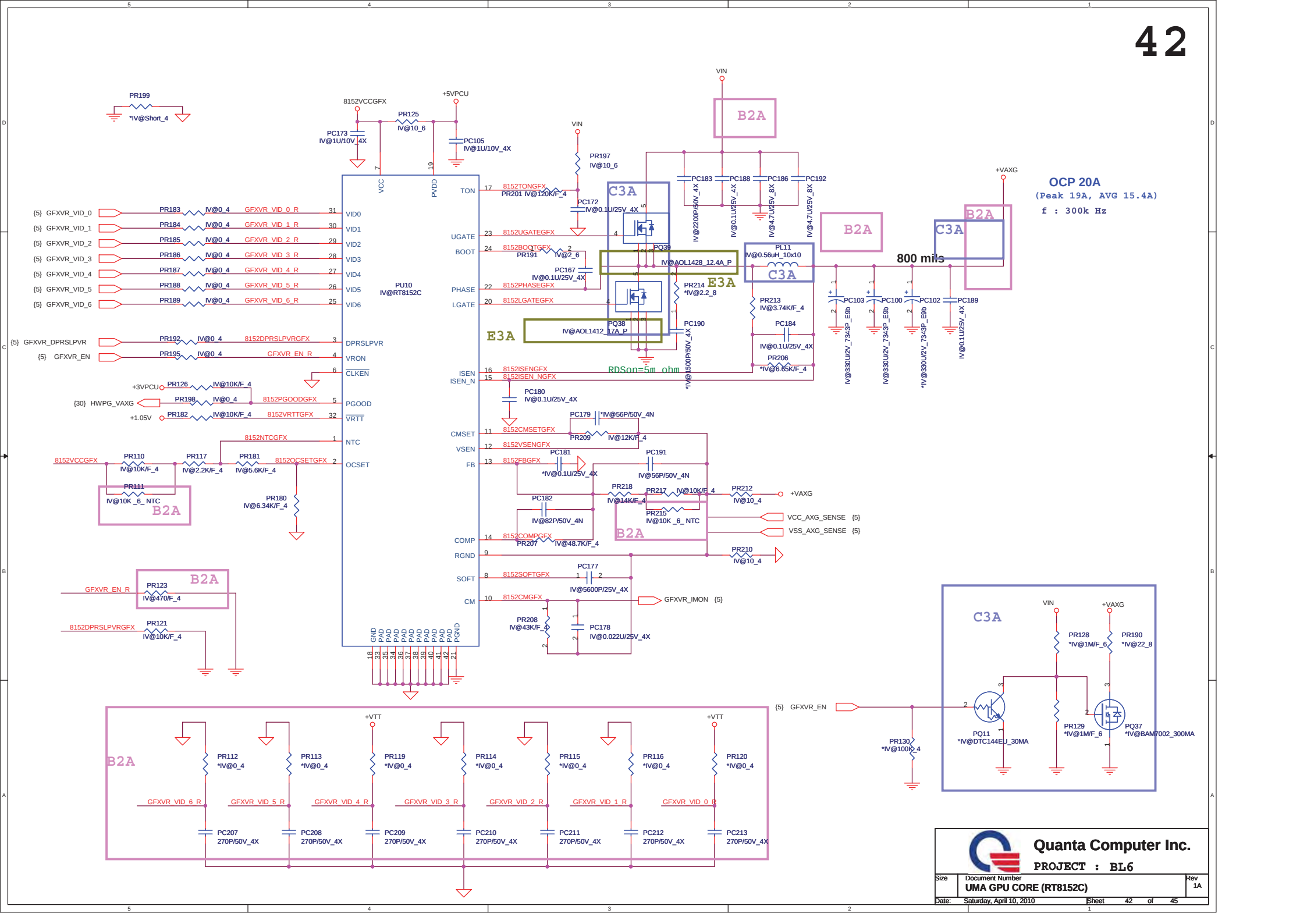
GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	Madison/Park	Madison/Park Resistor		M92	M92 Resistor		M96	M96 Resistor	
LOW	LOW	0.9V	R1=39.2K	CS33922FB15	0.9V	R1=39.2K	CS33922FB15	0.9V	R1=39.2K	CS33922FB15
LOW	HIGH	0.95V	R2=60.4K	CS36042FB10	0.95V	R2=60.4K	CS36042FB10	0.95V	R2=49.9K	CS34992FB10
HIGH	LOW	1.12V	R3=309K	CS43092FB16	1.1V	R3=270K	CS42702FB10	1V	R3=249K	CS42492FB18
HIGH	HIGH	NA	R4=88.7K	CS38872FB18	1.2V	R4=93.1K	CS39312FB15	1.1V	R4=140K	CS41402FB14

PCIE_VDDC
M92,M96-->1.1V
Madison,Park-->1.0V

	Madison,Park	M92,M96
PR163 = R1	25.5K/F_4 CS32552FB11	38.3K/F_4 CS33832FB08
PR166 = R2	100K/F_4 CS41002FB28	100K/F_4 CS41002FB28

Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	+VGPU_CORE (MAX8792)	1A
Date: Saturday, April 10, 2010	Sheet 41 of 45	



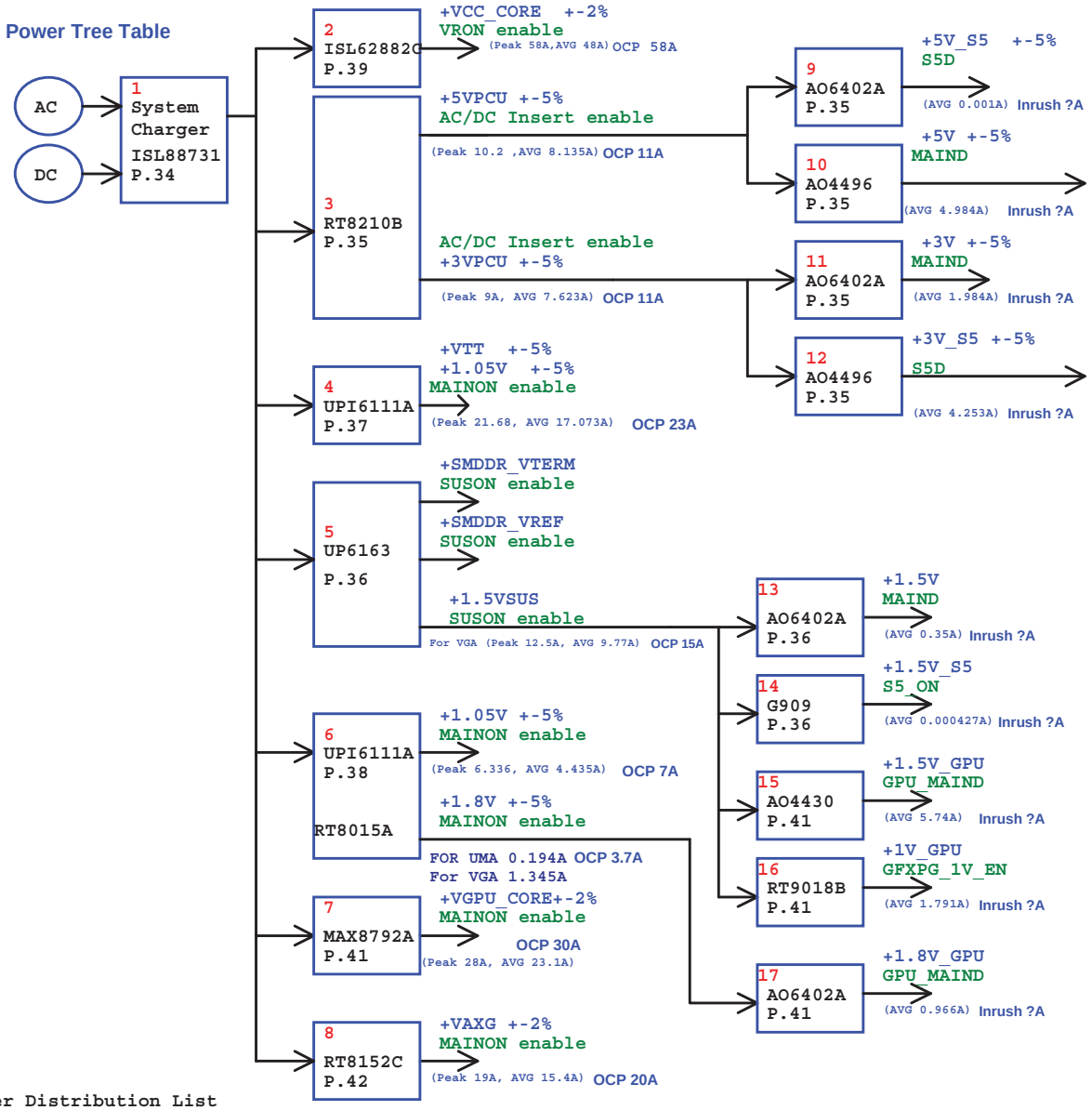
Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	UMA GPU CORE (RT8152C)	1A

Date: Saturday, April 10, 2010 Sheet 42 of 45

Power Tree Table



Power Distribution List

Power	Distribution

Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	Power Tree Table	1A

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