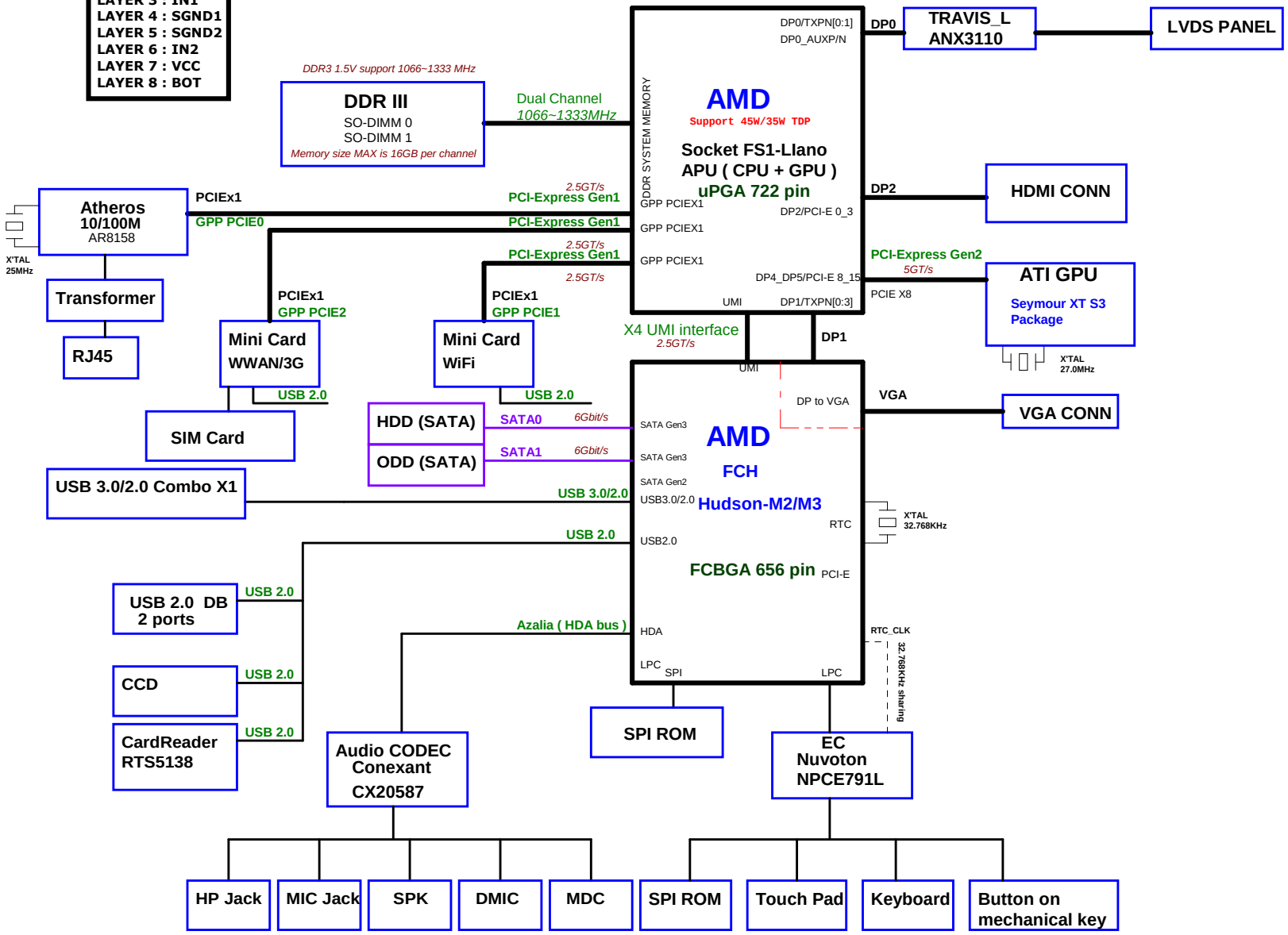
BLOCK DIAGRAM

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : SGND1
LAYER 5 : SGND2
LAYER 6 : IN2
LAYER 7 : VCC
LAYER 8 : BOT

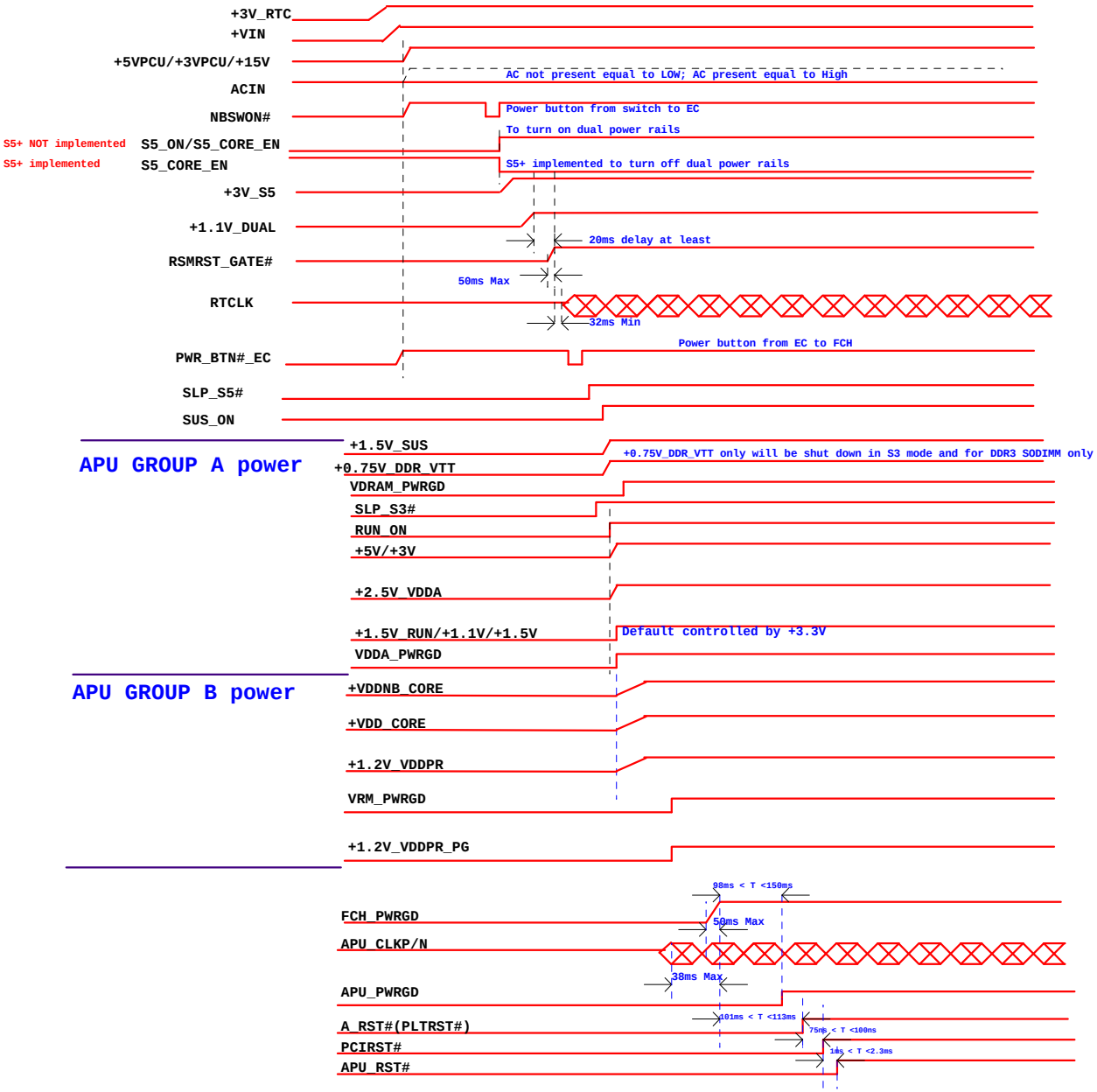


Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	System Block Diagram	1C

Date: Tuesday, April 19, 2011 Sheet 1 of 53

BLF/BLFD Power On Sequence: S5 > S0



APU Power on sequence required:

Llano APU:
1.Group A (+1.5V_SUS, +2.5V_VDDA) ramp before Group B (+VDD_CORE, +VDDNB_CORE, +1.2V_VDDPR)

HUDSON-M2/M3:
1.+3V_S5 ramp before +1.1V_DUAL
2.+3V ramp before +1.1V
3.+3V_RTC must ramp at least 5 secs before the +3V_S5

Seymour XT S3 package Power-on sequence

All power rails reach nominal within 20ms

1 => +3V_GPU
2 => +VGPU_CORE/+1V_GPU
3 => +VGPU_CORE PWRGD to enable +1.5V_GPU
4.=> +1V_GPU PWRGD to enable +1.8V_GPU

NOTE

1.+3V to turn on +3V_GPU

2.+3V_GPU ready to enable +VGPU_CORE/+1V_GPU
(+1V_GPU will ramp up before +VGPU_CORE)

3.+VGPU_CORE PWRGD to enable +1.5V_GPU

3.+1V_GPU PWRGD to enable +1.8V_GPU

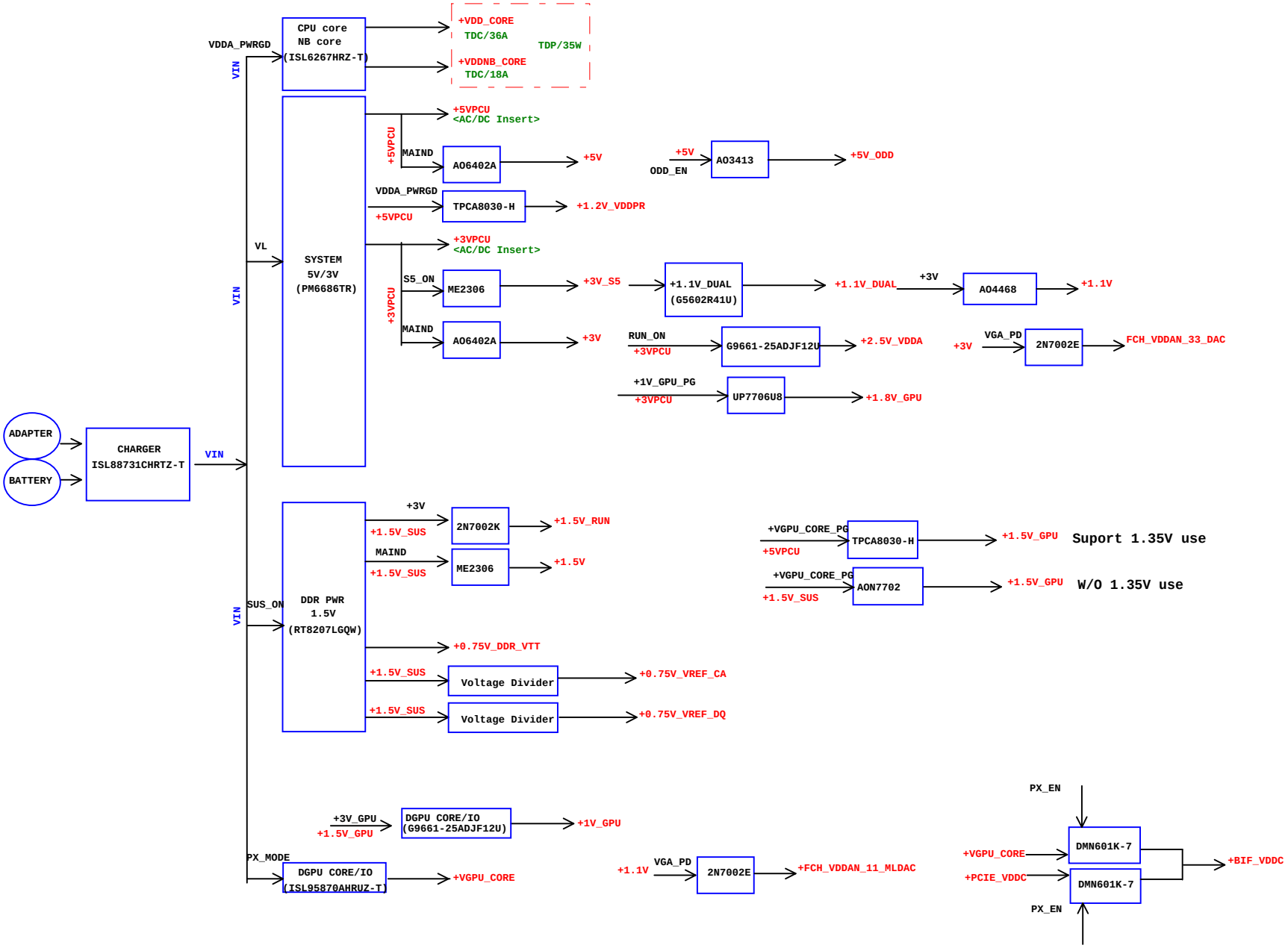
TRAVIS_L ANX3110 power on sequecne

1.+3V must lead +1.2V_TRAVIS

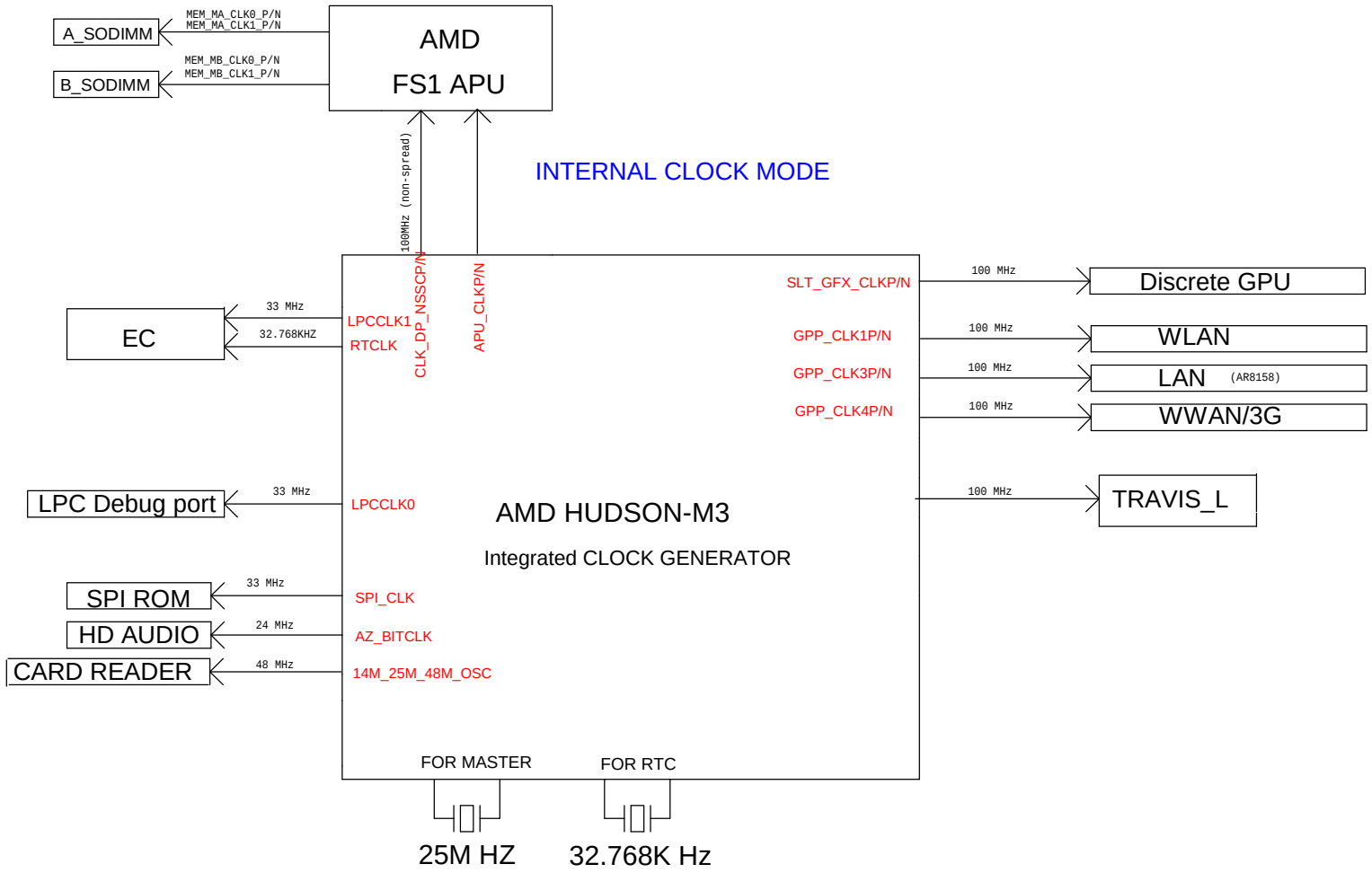
2.+1.2V_TRAVIS must lead TRAVIS_RST#

NOTE: FCH must output PCIE_RST#_TRAVIS or APU_PCIE_RST# after +1.2V_TRAVIS ready

Quanta Computer Inc.
PROJECT : BLF_BLFD
Size | Document Number: POWER SEQUENCE | Rev 1C
Date: Tuesday, April 19, 2011 | Sheet 2 of 53



Quanta Computer Inc.
PROJECT : BLF_BLFD
Size | Document Number | Rev
Power Tree | 1C
Date: Tuesday, April 19, 2011 | Sheet 3 of 53

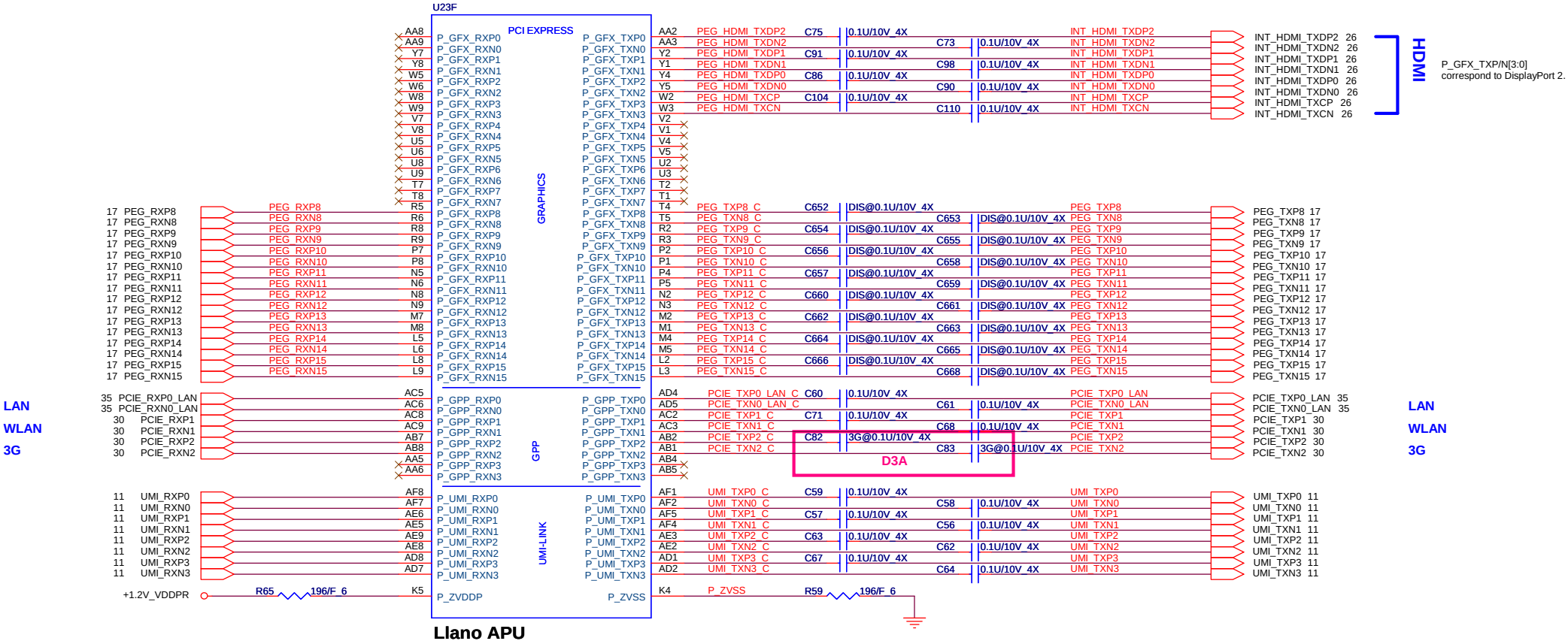


Quanta Computer Inc.

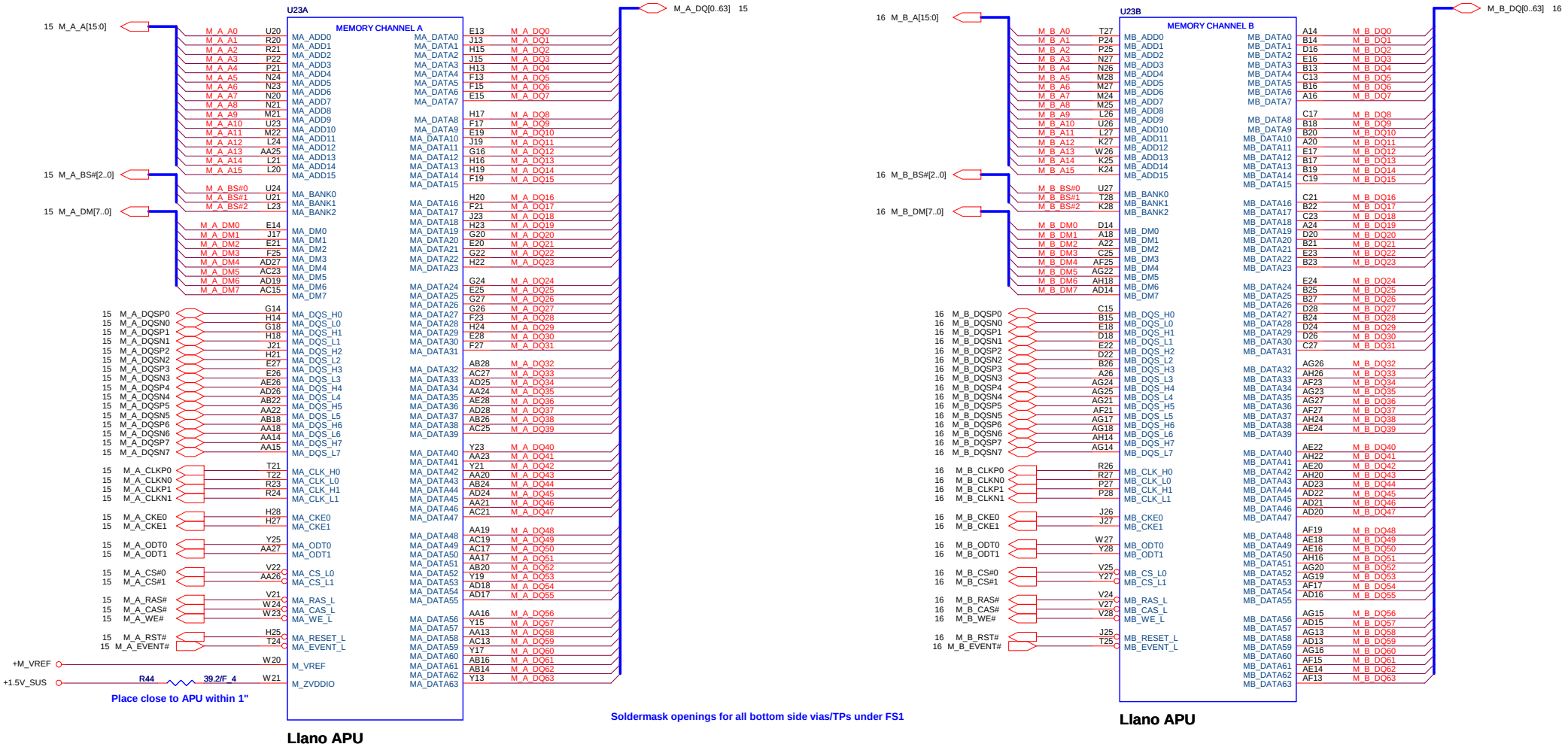
PROJECT : BLF_BLFD

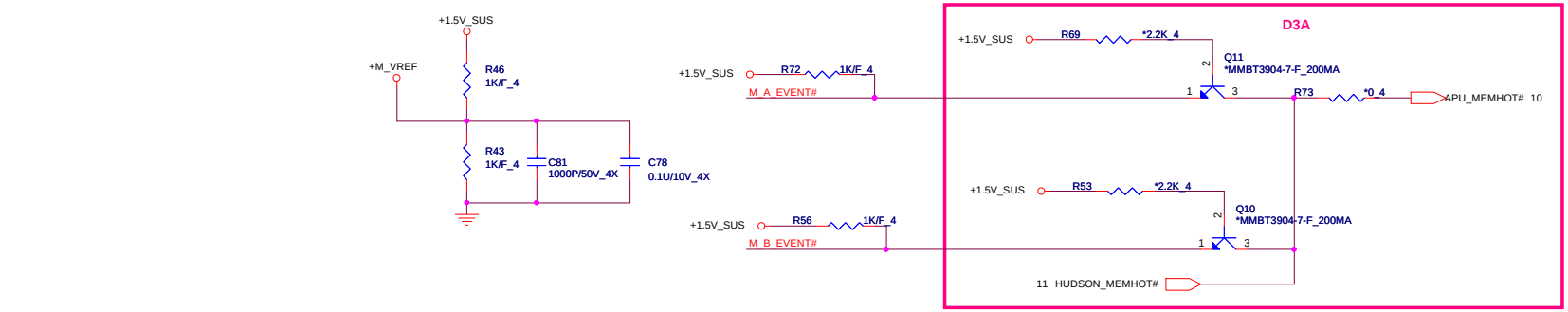
Size	Document Number	Rev
	Clock Distribution Diagram	1C

Date: Tuesday, April 19, 2011 Sheet 4 of 53



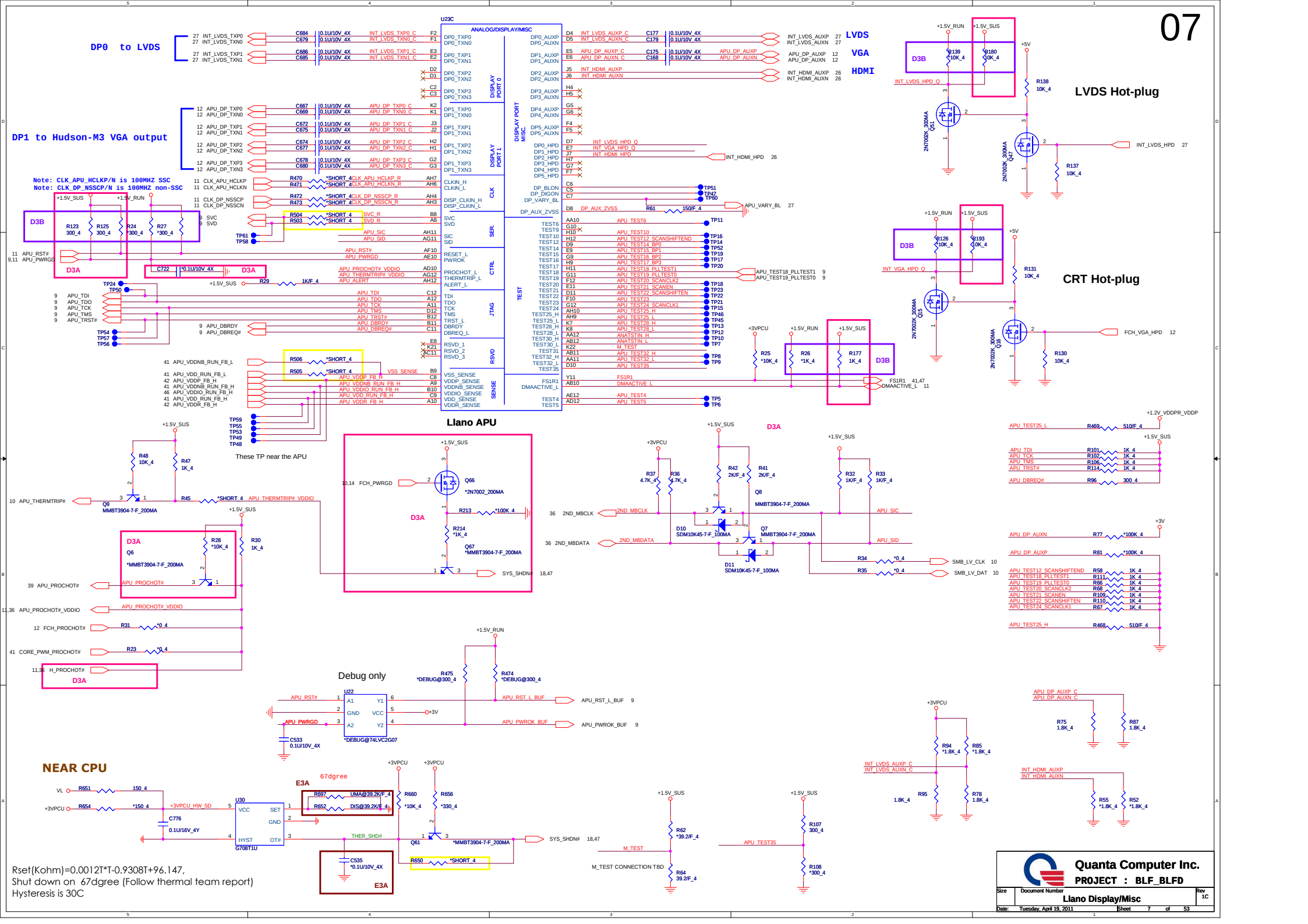
Quanta Computer Inc.		
PROJECT : BLF_BLFD		
Size	Document Number: Llano PCIE/UMI/GPP	Rev: 1C
Date: Tuesday, April 19, 2011	Sheet 5 of 53	





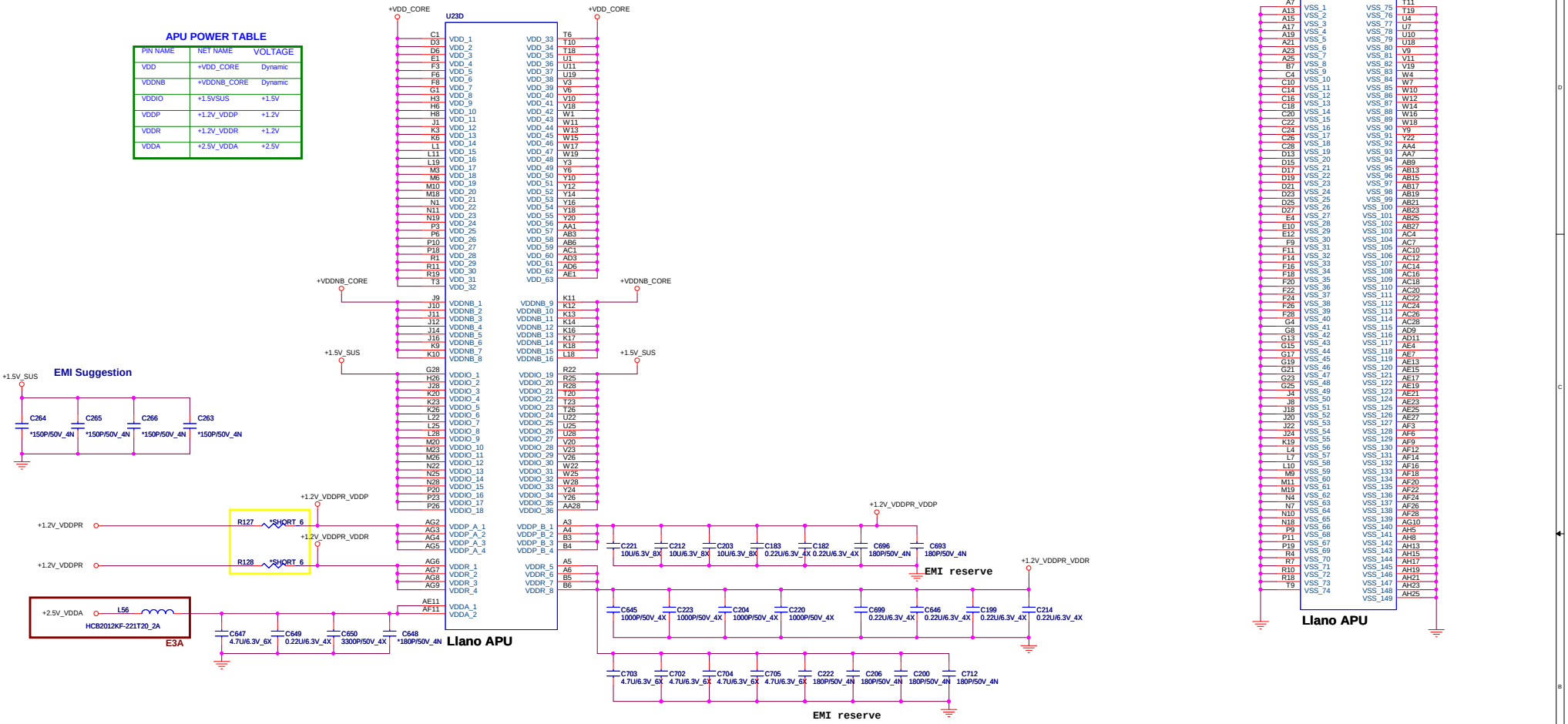
Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	Llano DDR3 MEM I/F	1C
Date: Tuesday, April 19, 2011	Sheet 6 of 53	

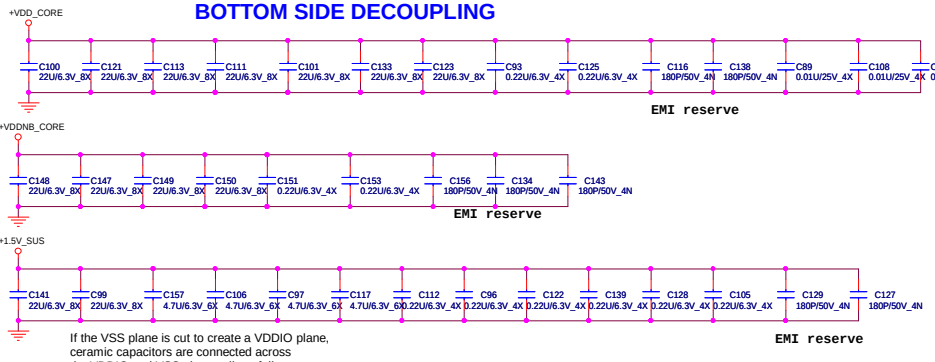

DP0 to LVDS
DP1 to Hudson-M3 VGA output
LVDS
VGA
HDMI
Note: CLK_APU_HCLKP/N is 100MHZ SSC
Note: CLK_DP_NSSCP/N is 100MHZ non-SSC
U23C
ANALOG/DISPLAY/MISC
DISPLAY PORT 0
DISPLAY PORT 1
DISPLAY PORT MISC.
CLK
SER.
CTRL
JTAG
RSVD
SENSE
TEST
Llano APU
LVDS Hot-plug
CRT Hot-plug
These TP near the APU
Debug only
NEAR CPU
67dgree
E3A
Rset(Kohm)=0.0012T*T-0.9308T+96.147,
Shut down on 67dgree (Follow thermal team report)
Hysteresis is 30C
Quanta Computer Inc.
PROJECT : BLF_BLFD
Llano Display/Misc
Date: Tuesday, April 19, 2011
Sheet 7 of 53

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	Dynamic
VDDNB	+VDDNB_CORE	Dynamic
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

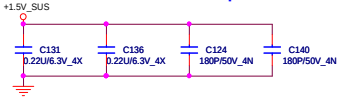


BOTTOM SIDE DECOUPLING



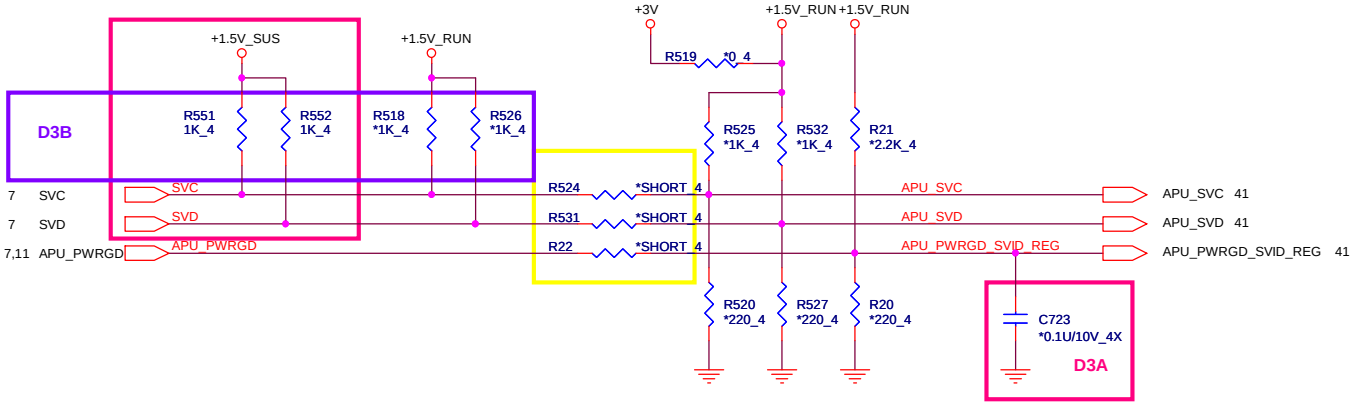
DECOUPLING between PROCESSOR and DIMMs

Across VDDIO and VSS split



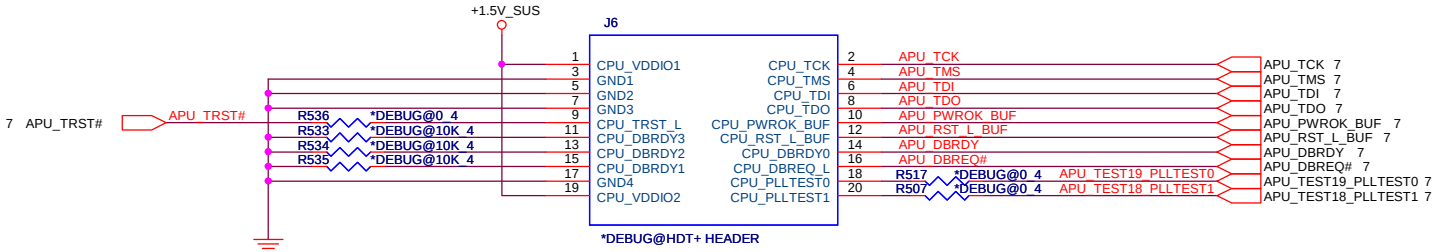
Quanta Computer Inc.
PROJECT : BLF_BLFD
Size | Document Number: Llano POWER/GND | Rev 1C
Date: Tuesday, April 19, 2011 | Sheet 8 of 53

VID Override Circuit



HDT+ Connector

Debug only



Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	Llano DEBUG&OTHER	1C
Date: Tuesday, April 19, 2011	Sheet 9 of 53	

NC,no install by default

remove pull hi (chip internal have pull hi)

HUDSON-M2
Part 4 of 5

HUB3
HUB2
HUB1

Reserve USB2.0/3.0 option
3G
SIM Card
WLAN
CCD on LVDS
Card Reader
USB 2.0 x1
TO USB daughter board
TO USB daughter board
USB 3.0 x1

HD audio interface is +3V_S5 voltage

Note:LLB#, WAKE# and PWR_BTN need pull up to +3VPCU only if S5+ mode is supported

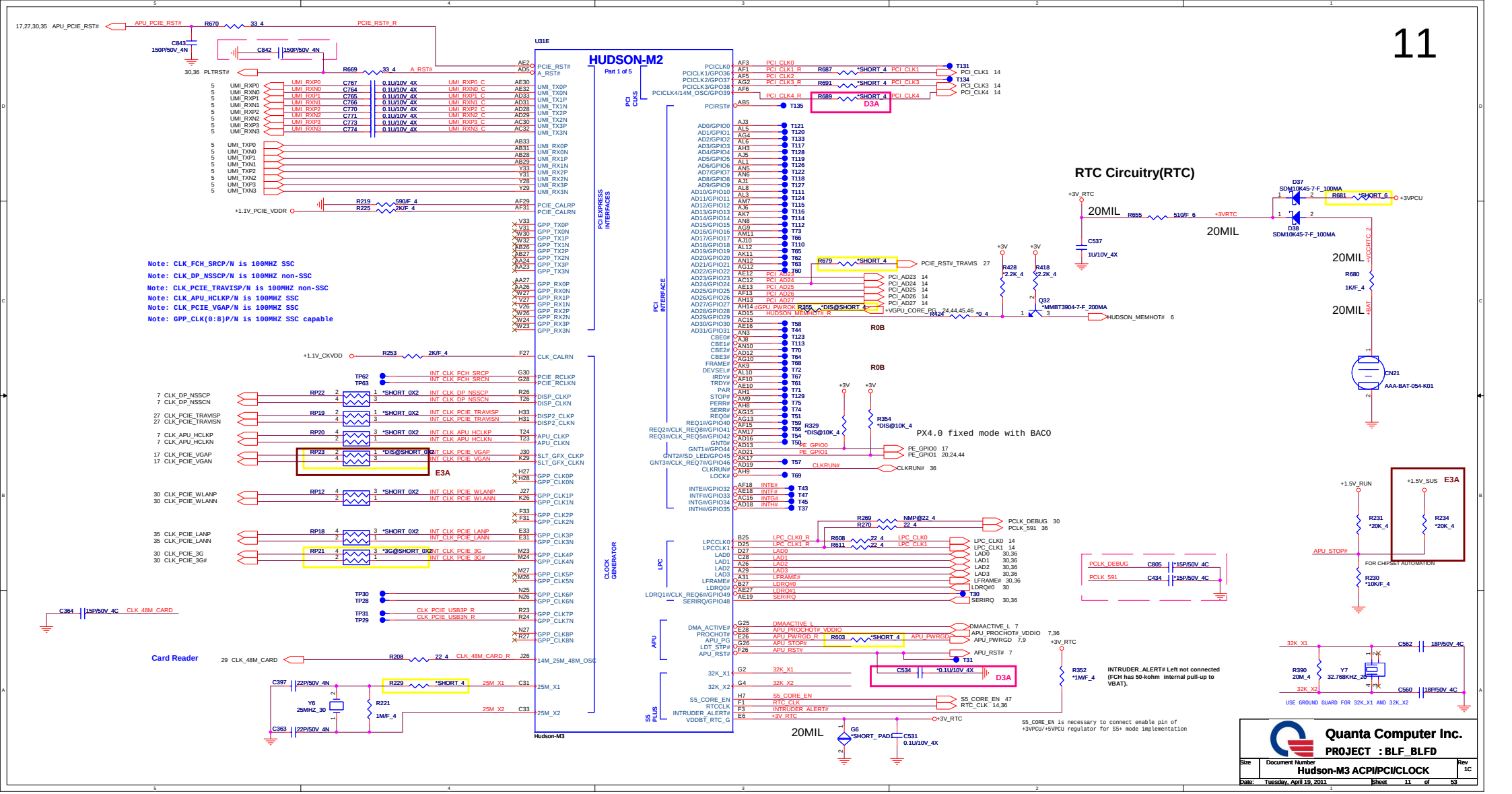
Provided test points from checklist

To Azalia

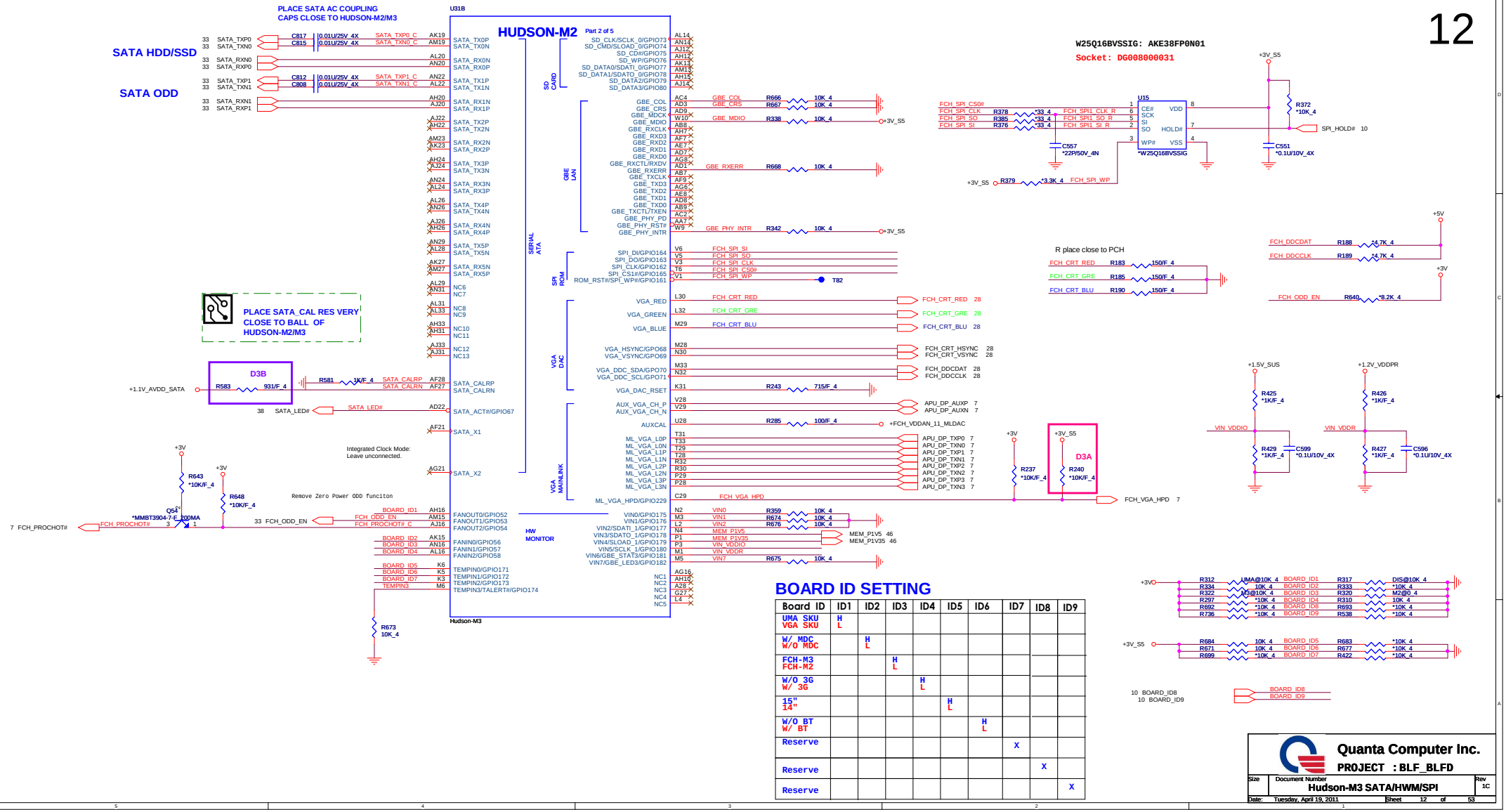
Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	Hudson-M3 GPIO/USB/AZ/RGMII	1C

Date: Tuesday, April 19, 2011 Sheet 10 of 53



Quanta Computer Inc.	
PROJECT : BLF_BLFD	
Size	Document Number: Hudson-M3 ACPI/PCI/CLOCK — Rev: 1C
Date: Tuesday, April 19, 2011	Sheet 11 of 53



BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9
UMA SKU VGA SKU	H L								
W/ MDC W/O MDC		H L							
FCH-M3 FCH-M2			H L						
W/O 3G W/ 3G				H L					
15" 14"					H L				
W/O BT W/ BT						H L			
Reserve							X		
Reserve								X	
Reserve									X

Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	Hudson-M3 SATA/HWM/SPI	1C

Date: Tuesday, April 19, 2011 Sheet 12 of 53

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

VDDQ--3.3V I/O power

VDD-- S/B CORE power

CKVDD_1.1V-- Internal clock Generator I/O power

PCIE_VDDR--PCIE I/O power

AVDD_SATA--SATA phy power

S5_3.3--3.3v standby power

S5_1.1V--1.1V standby power

S5 plus mode

HUDSON-M2 Part 3 of 5

HUDSON-M2 Part 5 of 5

32 mA Max

233 mA Max

Quanta Computer Inc.

PROJECT : BLF_BLFD

Hudson-M3 POWER/GND

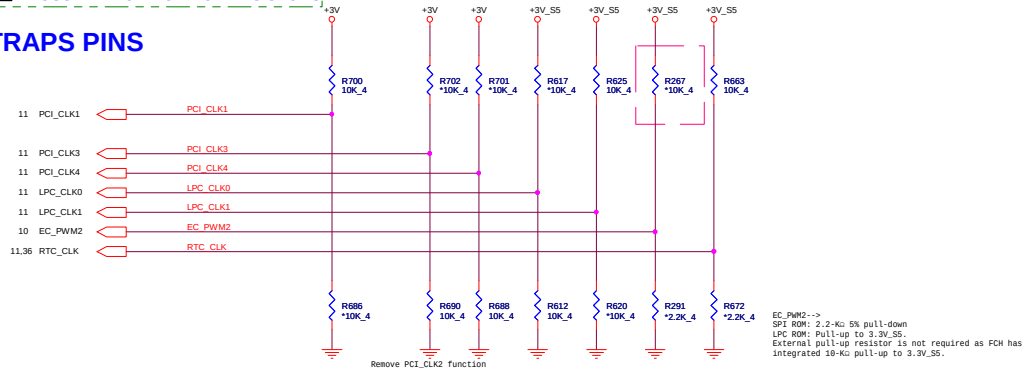
Size: | Document Number | Rev 1C

Date: Tuesday, April 19, 2011 | Sheet 13 of 53

13

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS

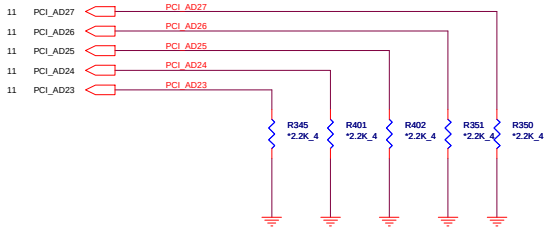


REQUIRED STRAPS

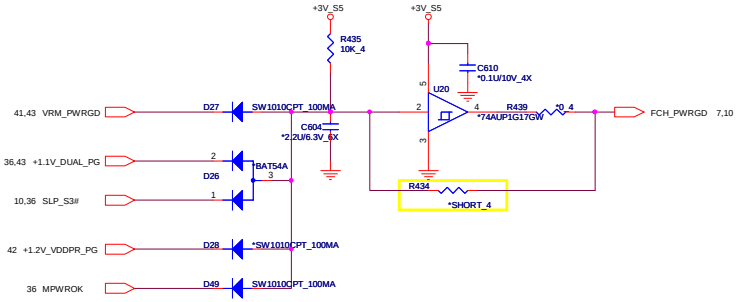
	--------	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



FCH PWRGD CKT

Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	Hudson-M3 STRAP/PWRGD	1C

Date: Tuesday, April 19, 2011 Sheet 14 of 53

DDR_STD(DDR)

JDIM6A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP4B

6 M_A_A[15:0]

M_A_A0 98 A0
M_A_A1 97 A1
M_A_A2 96 A2
M_A_A3 95 A3
M_A_A4 92 A4
M_A_A5 91 A5
M_A_A6 90 A6
M_A_A7 86 A7
M_A_A8 89 A8
M_A_A9 85 A9
M_A_A10 107 A10/AP
M_A_A11 84 A11
M_A_A12 83 A12/BC#
M_A_A13 119 A13
M_A_A14 80 A14
M_A_A15 78 A15

6 M_A_BS#0 109 BA0
6 M_A_BS#1 108 BA1
6 M_A_BS#2 79 BA2
6 M_A_CS#0 114 S0#
6 M_A_CS#1 121 S1#
6 M_A_CLKP0 101 CK0
6 M_A_CLKN0 103 CK0#
6 M_A_CLKP1 102 CK1
6 M_A_CLKN1 104 CK1#
6 M_A_CKE0 73 CKE0
6 M_A_CKE1 74 CKE1
6 M_A_CAS# 115 CAS#
6 M_A_RAS# 110 RAS#
6 M_A_WE# 113 WE#

R19 10K_4
R18 10K_4
DIMM0_SA0 197 SA0
DIMM0_SA1 201 SA1
10,16,30 SMB_RUN_CLK 202 SCL
10,16,30 SMB_RUN_DAT 200 SDA

+1.5V_SUS
R196 *0_4
6 M_A_ODT0 116 ODT0
6 M_A_ODT1 120 ODT1
+1.5V_SUS
R198 *0_4
E3A

6 M_A_DM0 11 DM0
6 M_A_DM1 28 DM1
6 M_A_DM2 46 DM2
6 M_A_DM3 63 DM3
6 M_A_DM4 136 DM4
6 M_A_DM5 153 DM5
6 M_A_DM6 170 DM6
6 M_A_DM7 187 DM7

6 M_A_DQSP[7:0]

M_A_DQSP0 12 DQS0
M_A_DQSP1 29 DQS1
M_A_DQSP2 47 DQS2
M_A_DQSP3 64 DQS3
M_A_DQSP4 137 DQS4
M_A_DQSP5 154 DQS5
M_A_DQSP6 171 DQS6
M_A_DQSP7 188 DQS7

6 M_A_DQSN[7:0]

M_A_DQSN0 10 DQS#0
M_A_DQSN1 27 DQS#1
M_A_DQSN2 45 DQS#2
M_A_DQSN3 62 DQS#3
M_A_DQSN4 135 DQS#4
M_A_DQSN5 152 DQS#5
M_A_DQSN6 169 DQS#6
M_A_DQSN7 186 DQS#7

DQ0 5 M_A_DQ0
DQ1 7 M_A_DQ1
DQ2 15 M_A_DQ2
DQ3 17 M_A_DQ3
DQ4 4 M_A_DQ4
DQ5 6 M_A_DQ5
DQ6 16 M_A_DQ6
DQ7 18 M_A_DQ7
DQ8 21 M_A_DQ8
DQ9 23 M_A_DQ9
DQ10 33 M_A_DQ10
DQ11 35 M_A_DQ11
DQ12 22 M_A_DQ12
DQ13 24 M_A_DQ13
DQ14 34 M_A_DQ14
DQ15 36 M_A_DQ15
DQ16 39 M_A_DQ16
DQ17 41 M_A_DQ17
DQ18 51 M_A_DQ18
DQ19 53 M_A_DQ19
DQ20 40 M_A_DQ20
DQ21 42 M_A_DQ21
DQ22 50 M_A_DQ22
DQ23 52 M_A_DQ23
DQ24 57 M_A_DQ24
DQ25 59 M_A_DQ25
DQ26 67 M_A_DQ26
DQ27 69 M_A_DQ27
DQ28 56 M_A_DQ28
DQ29 58 M_A_DQ29
DQ30 68 M_A_DQ30
DQ31 70 M_A_DQ31
DQ32 129 M_A_DQ32
DQ33 131 M_A_DQ33
DQ34 141 M_A_DQ34
DQ35 143 M_A_DQ35
DQ36 130 M_A_DQ36
DQ37 132 M_A_DQ37
DQ38 140 M_A_DQ38
DQ39 142 M_A_DQ39
DQ40 147 M_A_DQ40
DQ41 149 M_A_DQ41
DQ42 157 M_A_DQ42
DQ43 159 M_A_DQ43
DQ44 146 M_A_DQ44
DQ45 148 M_A_DQ45
DQ46 158 M_A_DQ46
DQ47 160 M_A_DQ47
DQ48 163 M_A_DQ48
DQ49 165 M_A_DQ49
DQ50 175 M_A_DQ50
DQ51 177 M_A_DQ51
DQ52 164 M_A_DQ52
DQ53 166 M_A_DQ53
DQ54 174 M_A_DQ54
DQ55 176 M_A_DQ55
DQ56 181 M_A_DQ56
DQ57 183 M_A_DQ57
DQ58 191 M_A_DQ58
DQ59 193 M_A_DQ59
DQ60 180 M_A_DQ60
DQ61 182 M_A_DQ61
DQ62 192 M_A_DQ62
DQ63 194 M_A_DQ63

M_A_DQ[0..63] 6

+1.5V_SUS
+0.75V_VREF_CA
R40 1K/F_4
R38 *SHORT_6
R39 1K/F_4
C72 470P/50V_4X

+1.5V_SUS
+0.75V_VREF_DQ
R133 1K/F_4
R132 *SHORT_6
R135 1K/F_4
C239 470P/50V_4X

JDIM6B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP4B

+1.5V_SUS
2.48A

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

+3V
VDDSPD 199

NC1 77
NC2 122
NCTEST 125

6 M_A_EVENT# 198 EVENT#
6 M_A_RST# 30 RESET#

+0.75V_VREF_DQ 1 VREF_DQ
+0.75V_VREF_CA 126 VREF_CA

VSS1 2
VSS2 3
VSS3 8
VSS4 9
VSS5 13
VSS6 14
VSS7 19
VSS8 20
VSS9 25
VSS10 26
VSS11 31
VSS12 32
VSS13 37
VSS14 38
VSS15 43

VSS16 44
VSS17 48
VSS18 49
VSS19 54
VSS20 55
VSS21 60
VSS22 61
VSS23 65
VSS24 66
VSS25 71
VSS26 72
VSS27 127
VSS28 128
VSS29 133
VSS30 134
VSS31 138
VSS32 139
VSS33 144
VSS34 145
VSS35 150
VSS36 151
VSS37 155
VSS38 156
VSS39 161
VSS40 162
VSS41 167
VSS42 168
VSS43 172
VSS44 173
VSS45 178
VSS46 179
VSS47 184
VSS48 185
VSS49 189
VSS50 190
VSS51 195
VSS52 196

VTT1 203
VTT2 204
+0.75V_DDR_VTT

GND 205
GND 206

Place these Caps near So-Dimm0.

+1.5V_SUS
C103 10U/6.3V_6X
C79 10U/6.3V_6X
C88 10U/6.3V_6X
C85 1U/10V_4X
C107 1U/10V_4X
C135 10U/6.3V_6X
C673 *330U/2V_7343P_E6132
C144 10U/6.3V_8X
EC26 1500P/50V_4X
EC27 1500P/50V_4X
C120 10U/6.3V_6X
C145 10U/6.3V_6X
C114 *10U/6.3V_6X
C118 1U/10V_4X
C94 1U/10V_4X
E3A

+0.75V_VREF_CA
C76 0.1U/10V_4X
C74 1000P/50V_4X

EMI Suggestion

+1.5V_SUS
C243 *150P/50V_4N
C250 *150P/50V_4N
C251 *150P/50V_4N
C252 *150P/50V_4N
C253 *150P/50V_4N
C254 *150P/50V_4N
C255 *150P/50V_4N

+3V
C53 2.2U/6.3V_6X
C52 0.1U/10V_4X

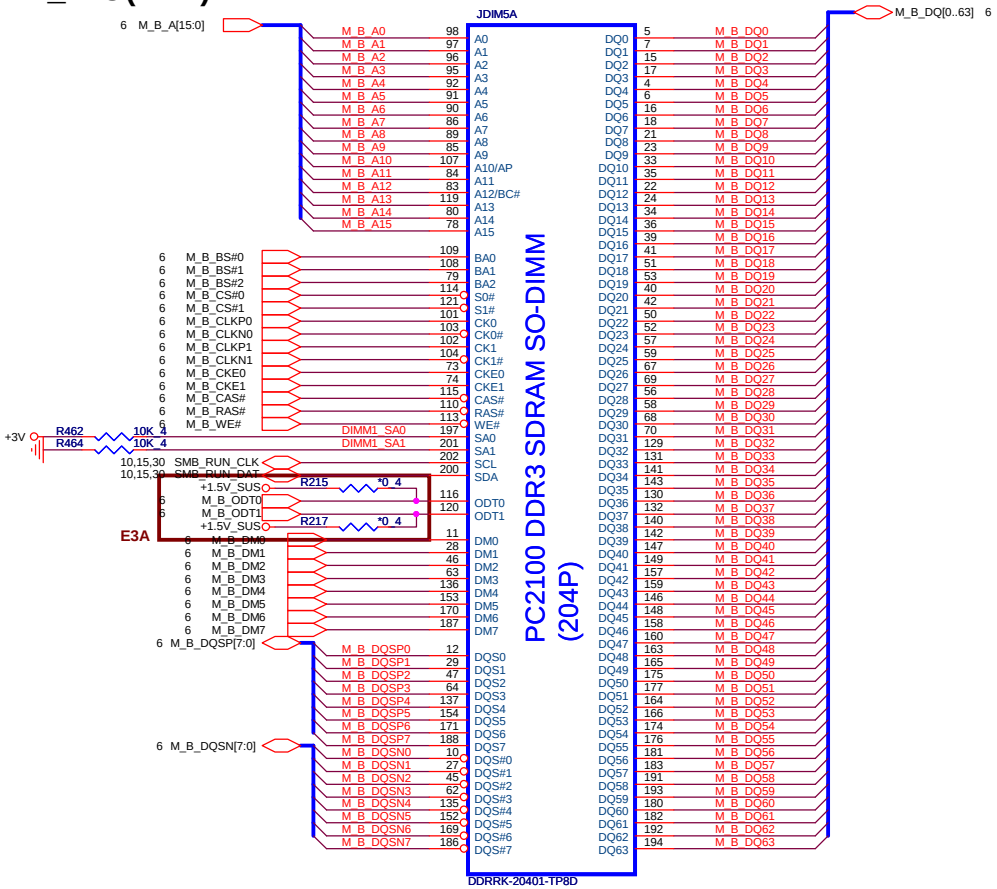
+0.75V_DDR_VTT
C23 1U/6.3V_4X
C27 1U/6.3V_4X
C28 1U/6.3V_4X
C51 1U/6.3V_4X
C24 10U/6.3V_6X
C26 10U/6.3V_6X

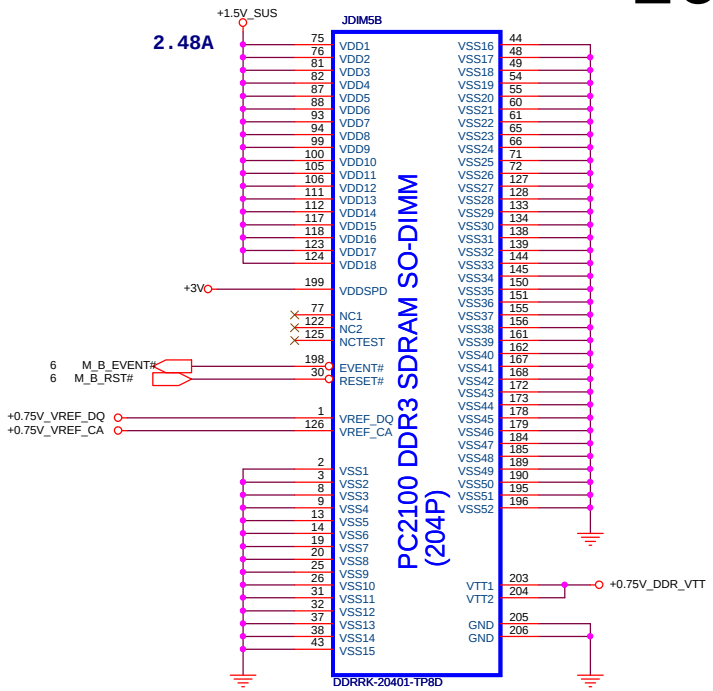
+0.75V_VREF_DQ
C216 0.1U/10V_4X
C213 1000P/50V_4X

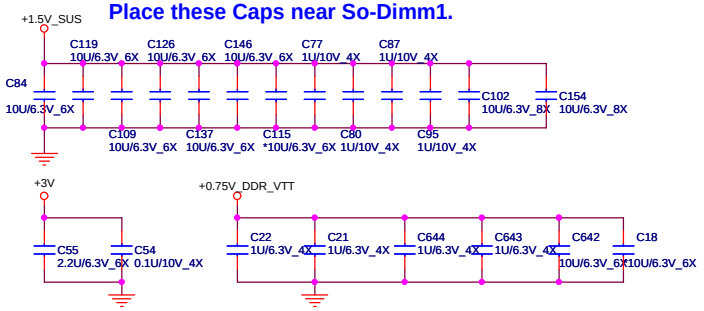
Quanta Computer Inc.
PROJECT : BLF_BLFD

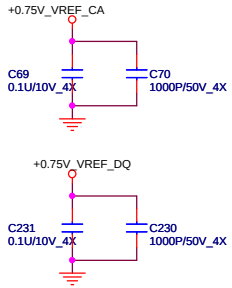
Size	Document Number	Rev
	DDRIII SO-DIMM-0	1C
Date: Tuesday, April 19, 2011	Sheet 15 of 53	

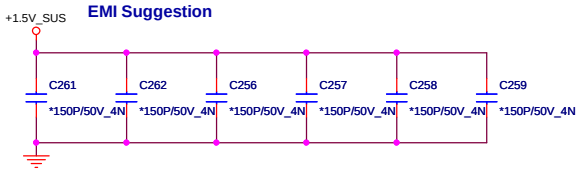
DDR_RVS(DDR)



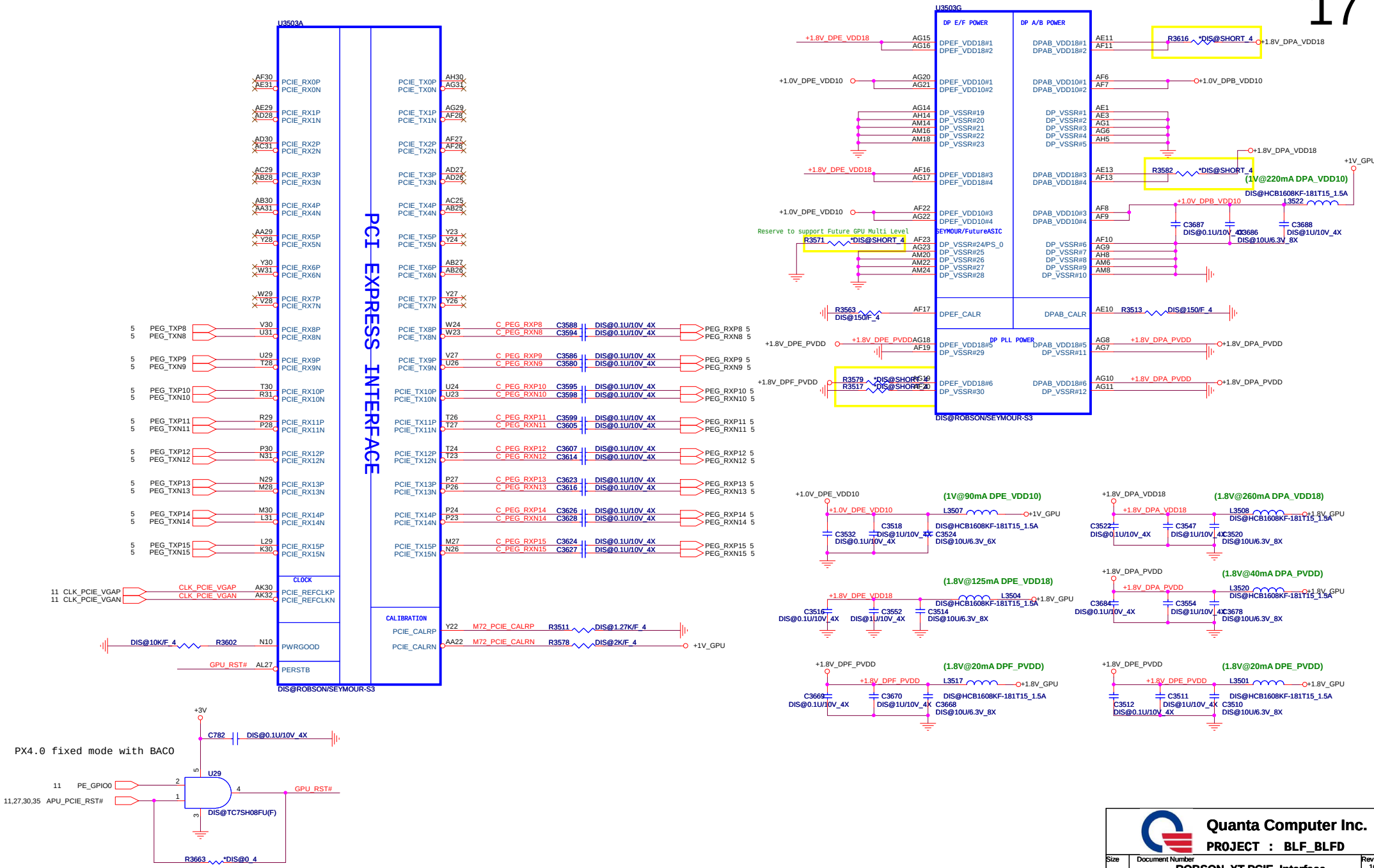




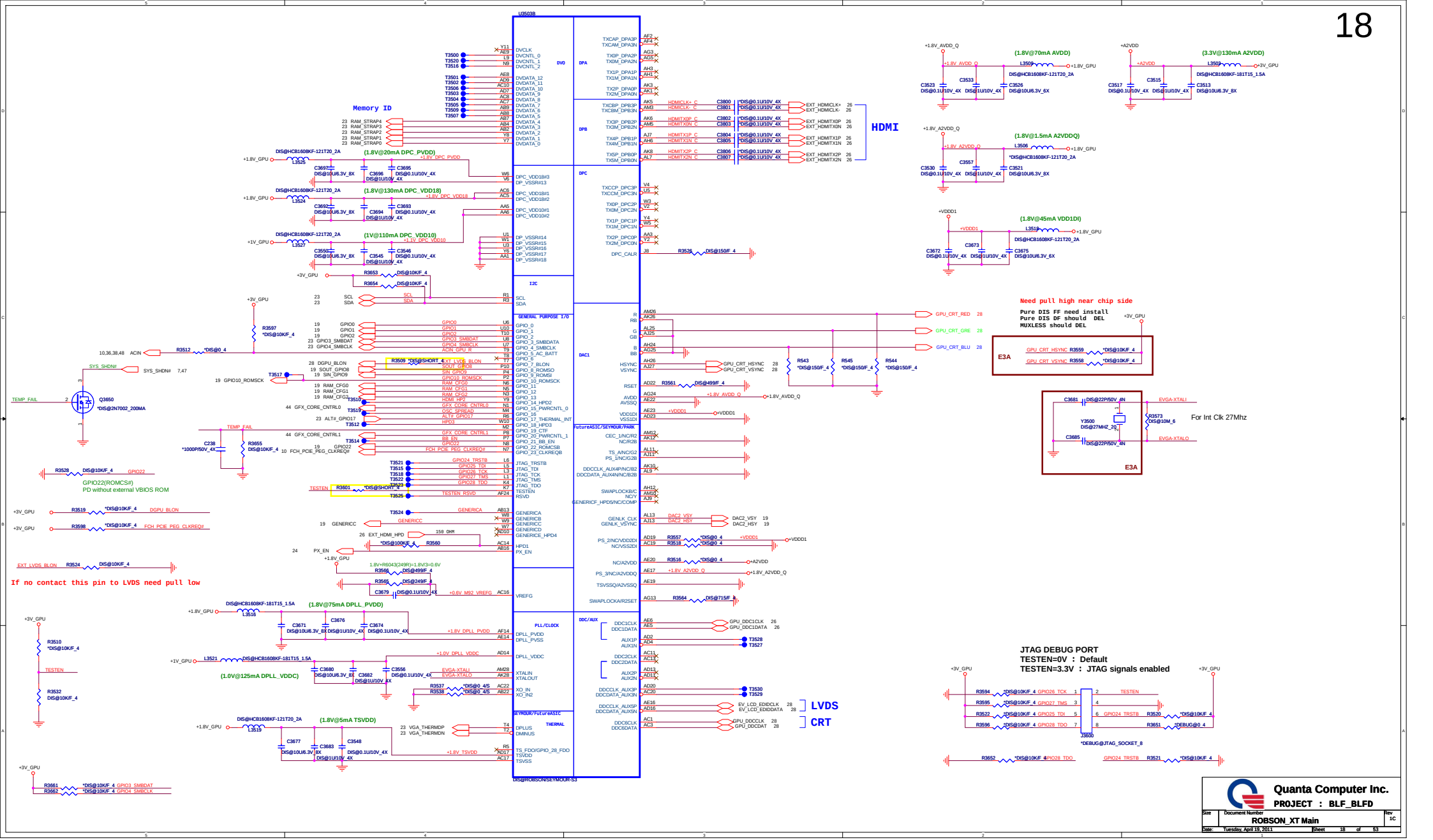




Quanta Computer Inc.		
PROJECT : BLF_BLFD		
Size	Document Number: DDRIII SO-DIMM-1	Rev: 1C
Date: Tuesday, April 19, 2011	Sheet 16 of 53	



Quanta Computer Inc.		
PROJECT : BLF_BLFD		
Size	Document Number: ROBSON_XT PCIE_Interface	Rev: 1C
Date: Tuesday, April 19, 2011	Sheet 17 of 53	


U3503B
Memory ID
(1.8V@20mA DPC_PVDD)
(1.8V@130mA DPC_VDD18)
(1V@110mA DPC_VDD10)
HDMI
LVDS
CRT
Need pull high near chip side
Pure DIS FF need install
Pure DIS DF should DEL
MUXLESS should DEL
For Int Clk 27Mhz
JTAG DEBUG PORT
TESTEN=0V : Default
TESTEN=3.3V : JTAG signals enabled
(1.8V@75mA DPLL_PVDD)
(1.0V@125mA DPLL_VDDC)
(1.8V@5mA TSVDD)
If no contact this pin to LVDS need pull low
GPIO22(ROMCS#)
PD without external VBIOS ROM
(1.8V@70mA AVDD)
(3.3V@130mA A2VDD)
(1.8V@1.5mA A2VDDQ)
(1.8V@45mA VDD1DI)
Quanta Computer Inc.
PROJECT : BLF_BLFD
ROBSON_XT Main
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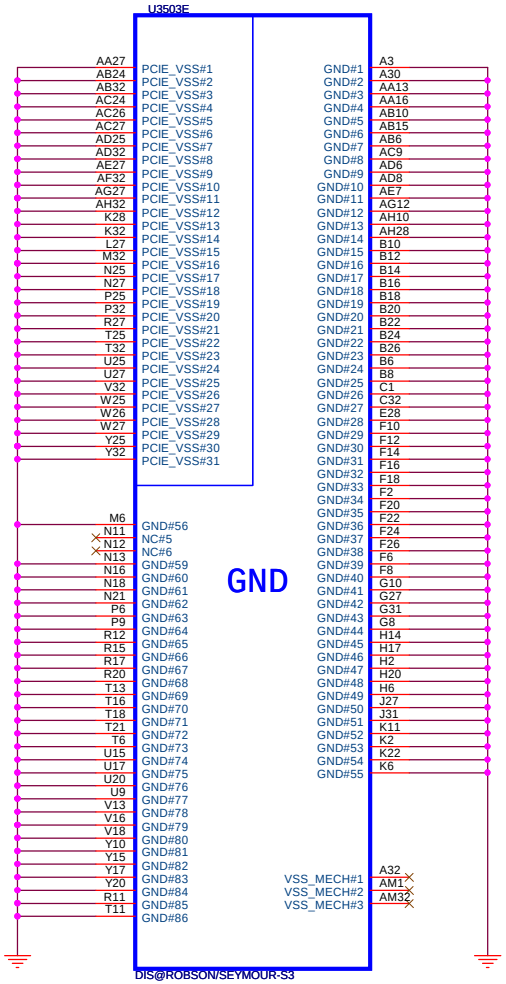
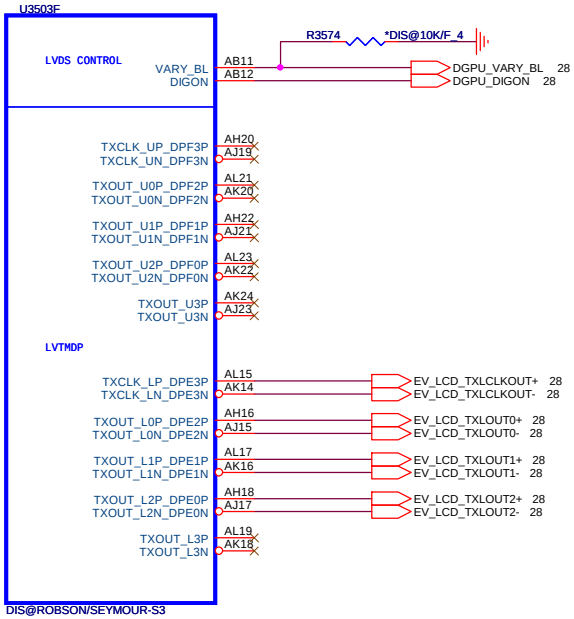
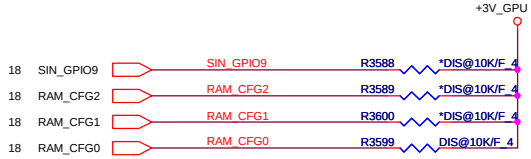
Reserve only for MUXLESS







CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

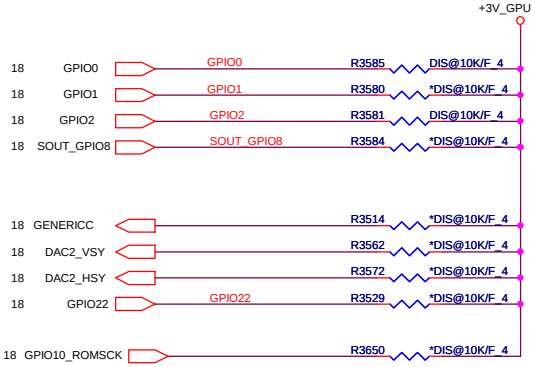
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

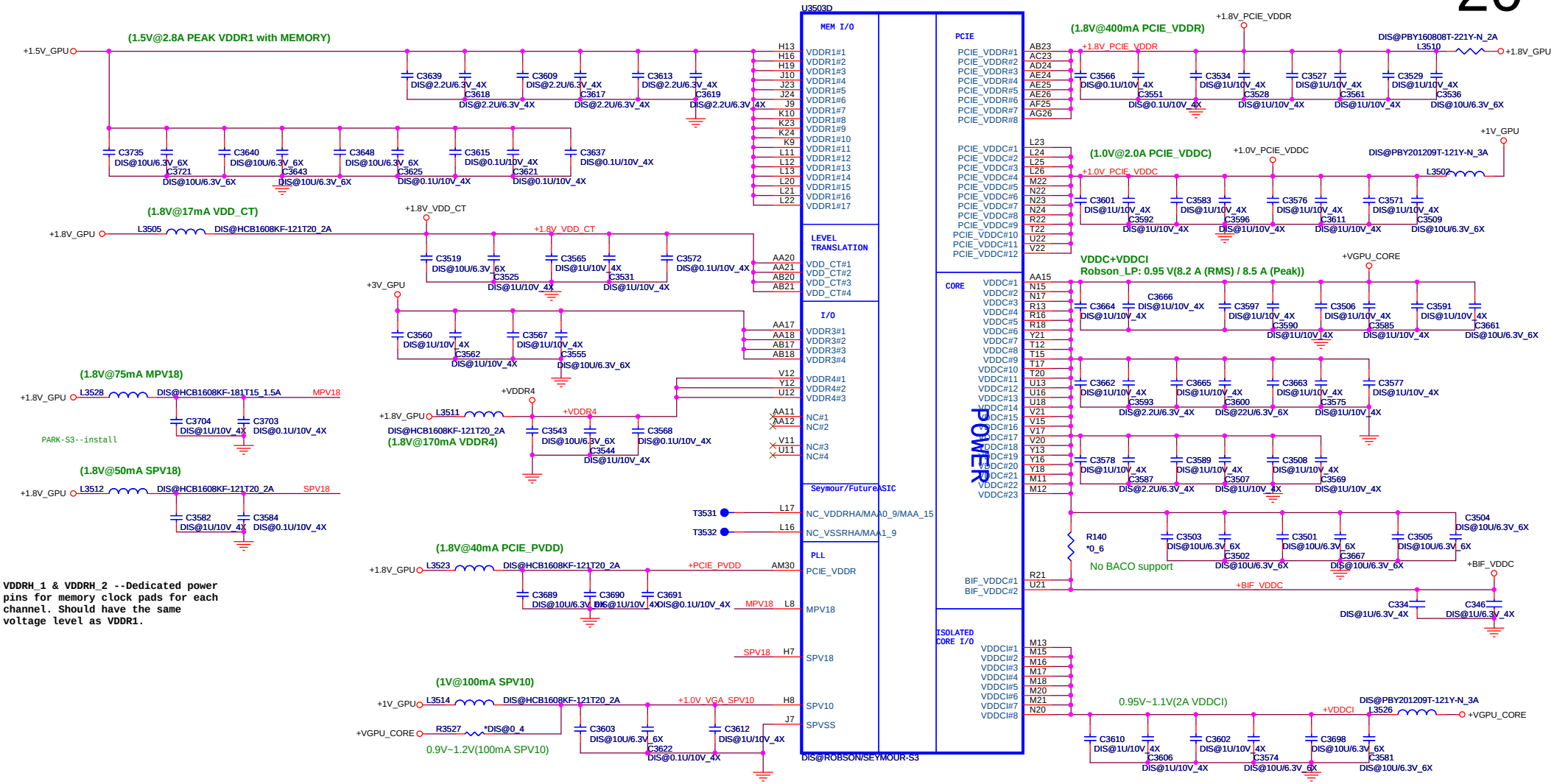
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	ROBSON_XT GND / LVDS/ Straps	1C
Date: Tuesday, April 19, 2011	Sheet 19 of 53	

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%

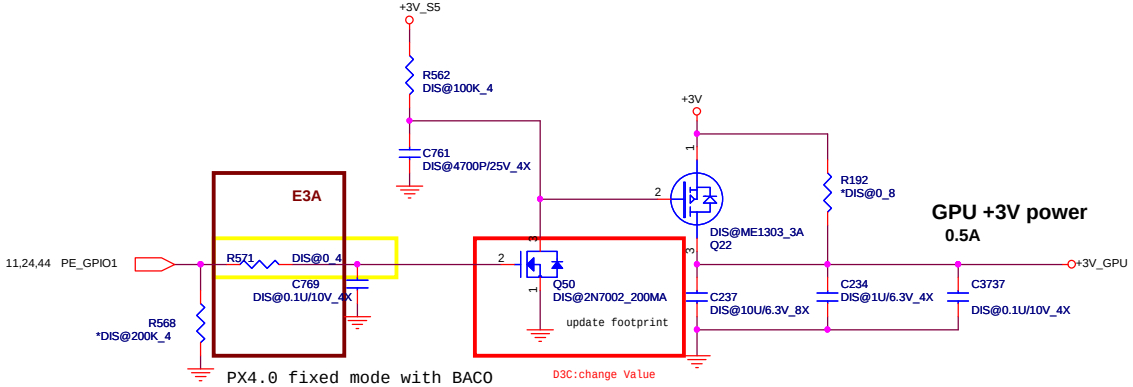


VDDRH_1 & VDDRH_2 --Dedicated power pins for memory clock pads for each channel. Should have the same voltage level as VDDR1.

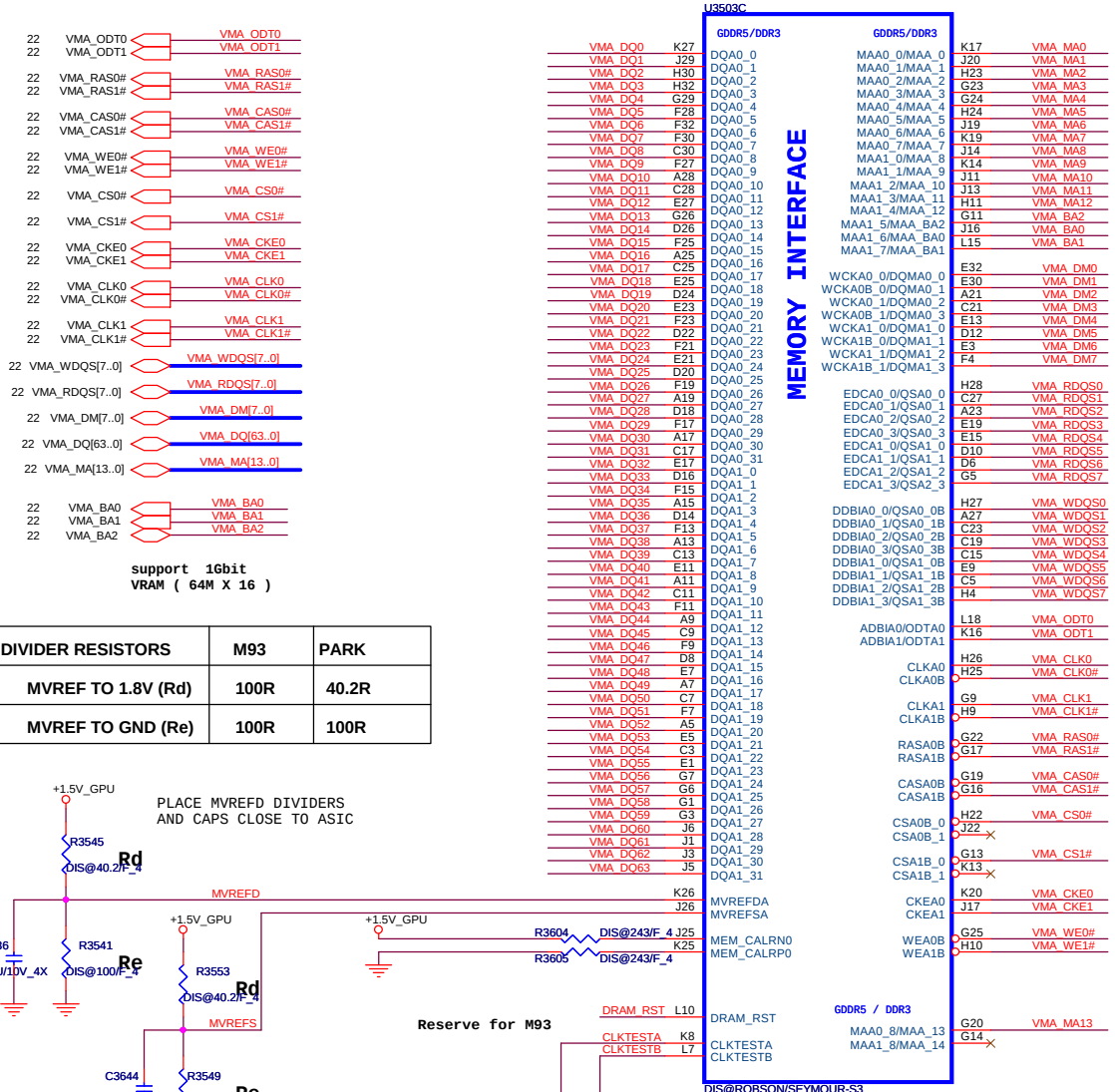
VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)

PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%

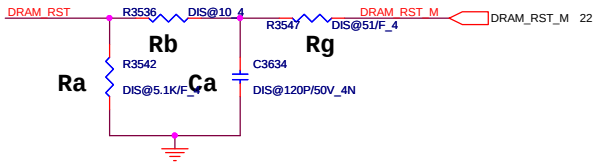


Quanta Computer Inc.			
PROJECT : BLF_BLFD			
Size	Document Number		Rev
	ROBSON_Power_and_NC		1C
Date: Tuesday, April 19, 2011		Sheet 20 of 53	



DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R

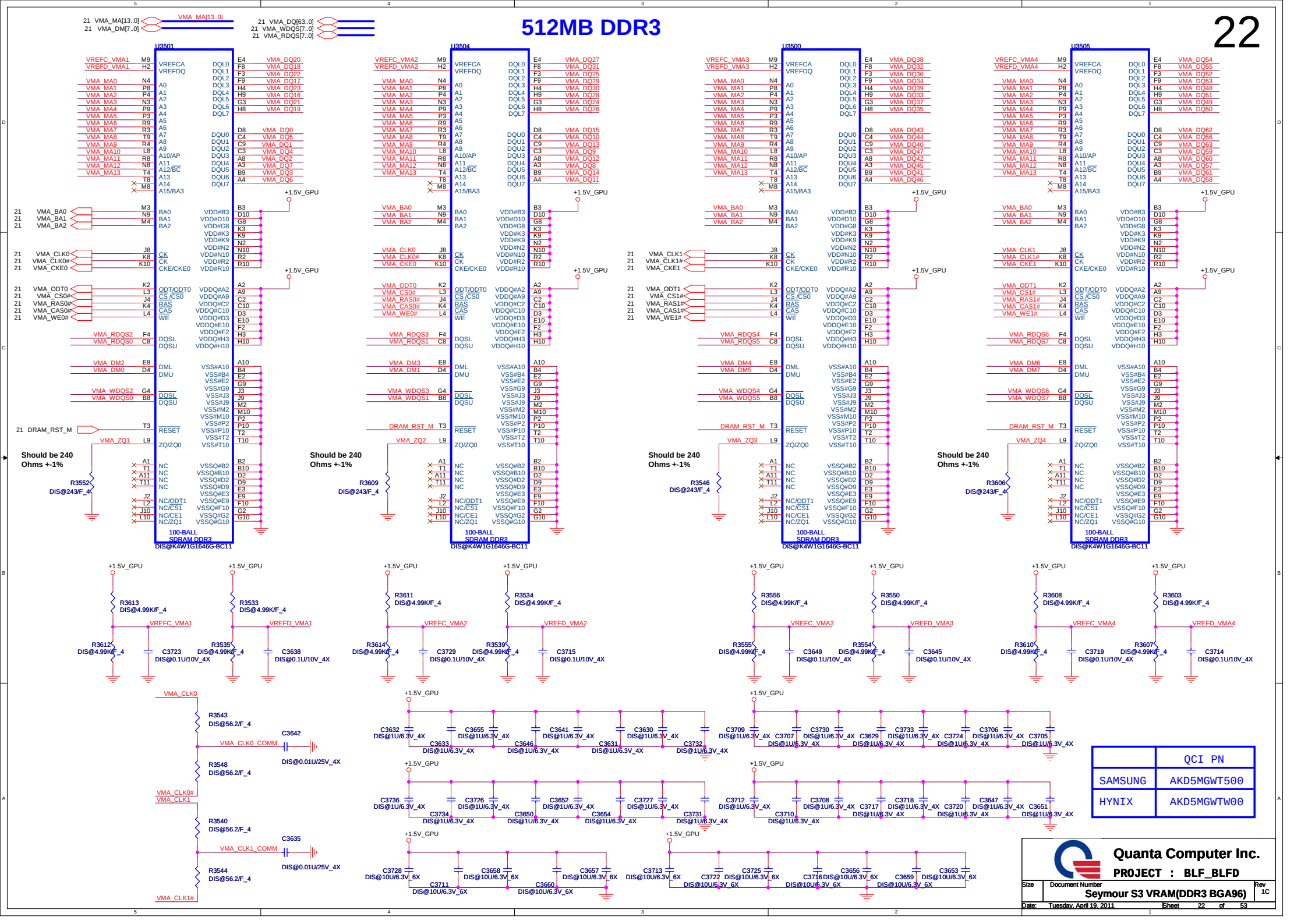
Designator	Robson
Ra	5K
Rb	10R
Ca	120pF
Rg	51R



Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	ROBSON/MEM_Interface	1C
Date: Tuesday, April 19, 2011	Sheet 21 of 53	

512MB DDR3



	QCI PN
SAMSUNG	AKD5MGWT500
HYNIX	AKD5MGWTW00

Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	Seymour S3 VRAM(DDR3 BGA96)	1C
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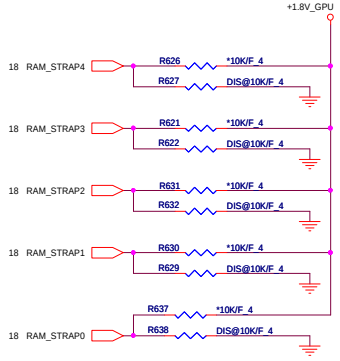
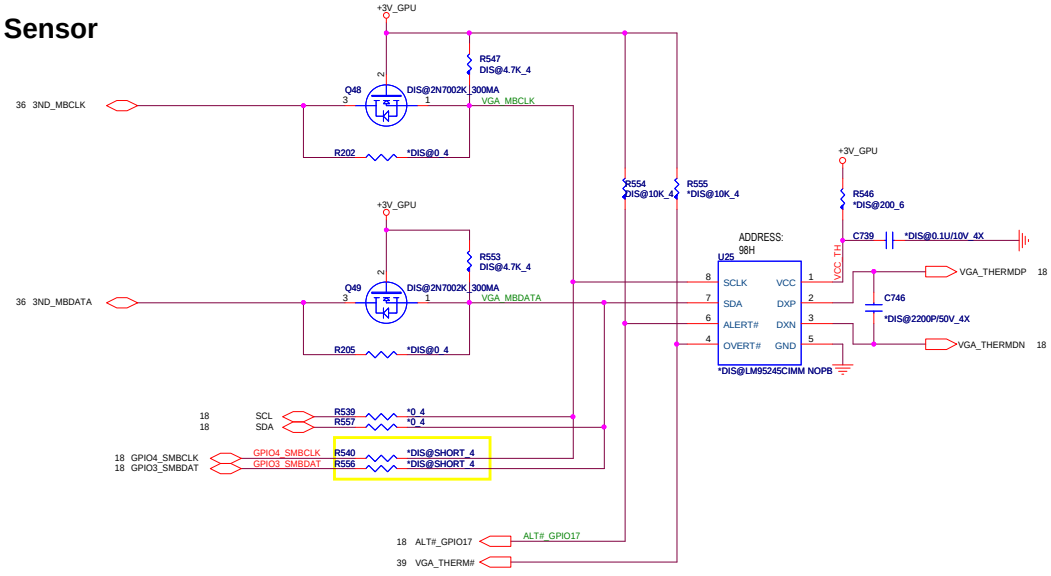
VRAM Memory TYPE

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	RAM_STRAP4 15"	RAM_STRAP4 14"
Hynix	H5TQ1G63DFR-11C	AKD5LZWTW02 (64M*16-1Gb)	512MB	0	1	0	0	0	1
	H5TQ2G63BFR-11C	AKD5MGWTW00 (128M*16-2Gb)	1GB	0	0	0	0	0	1
Samsung	K4W1G1646G-BC11	AKD5EGGT500 (64M*16-1Gb)	512MB	0	1	0	1	0	1
	K4W2G1646C-HC11	AKD5MGWT500 (128M*16-2Gb)	1GB	0	0	0	1	0	1



Thermal Sensor



Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	Blank	1C

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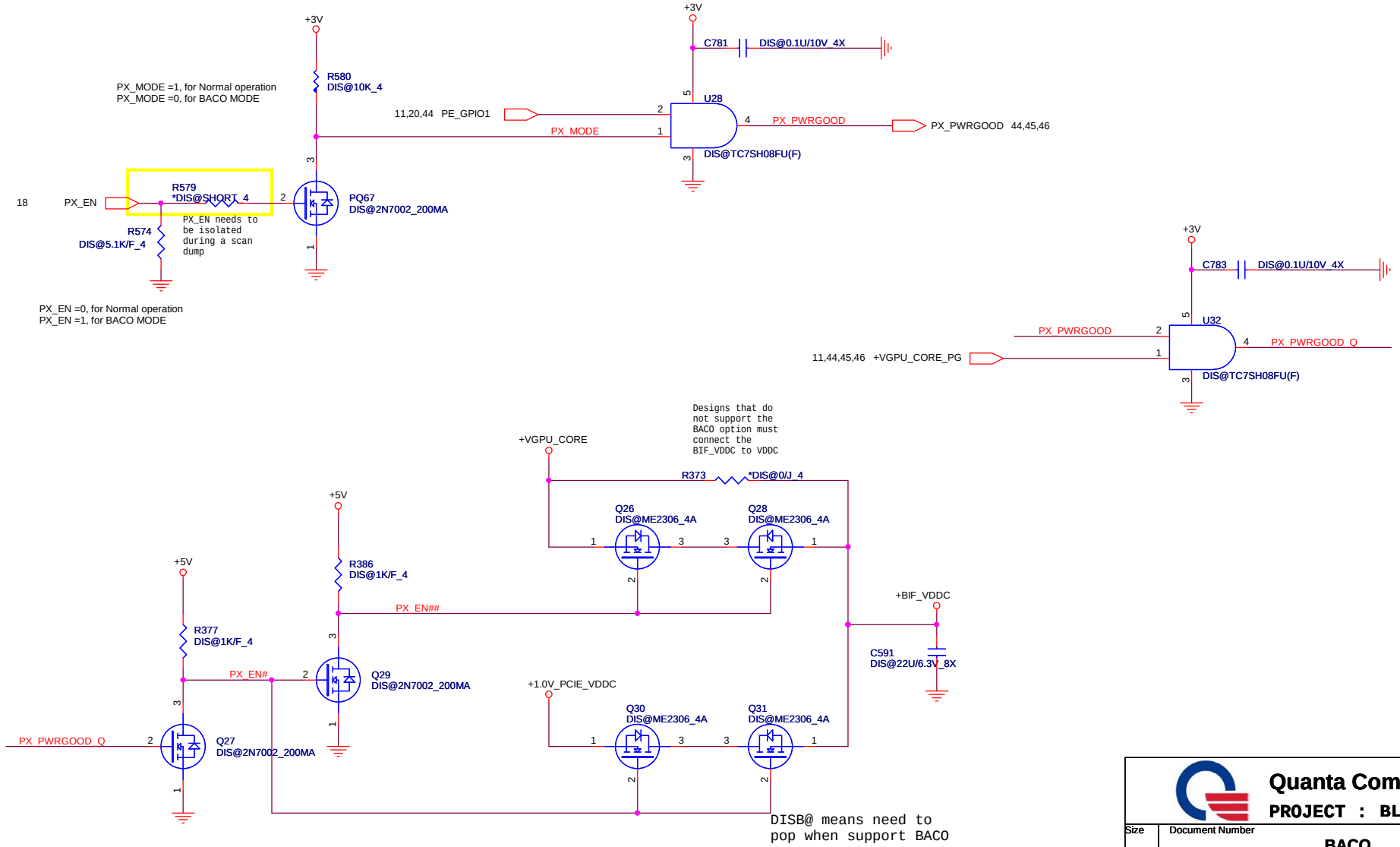

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PROJECT : BLF_BLFD

Size	Document Number	Rev
	BACO	1C

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Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	Blank	1C
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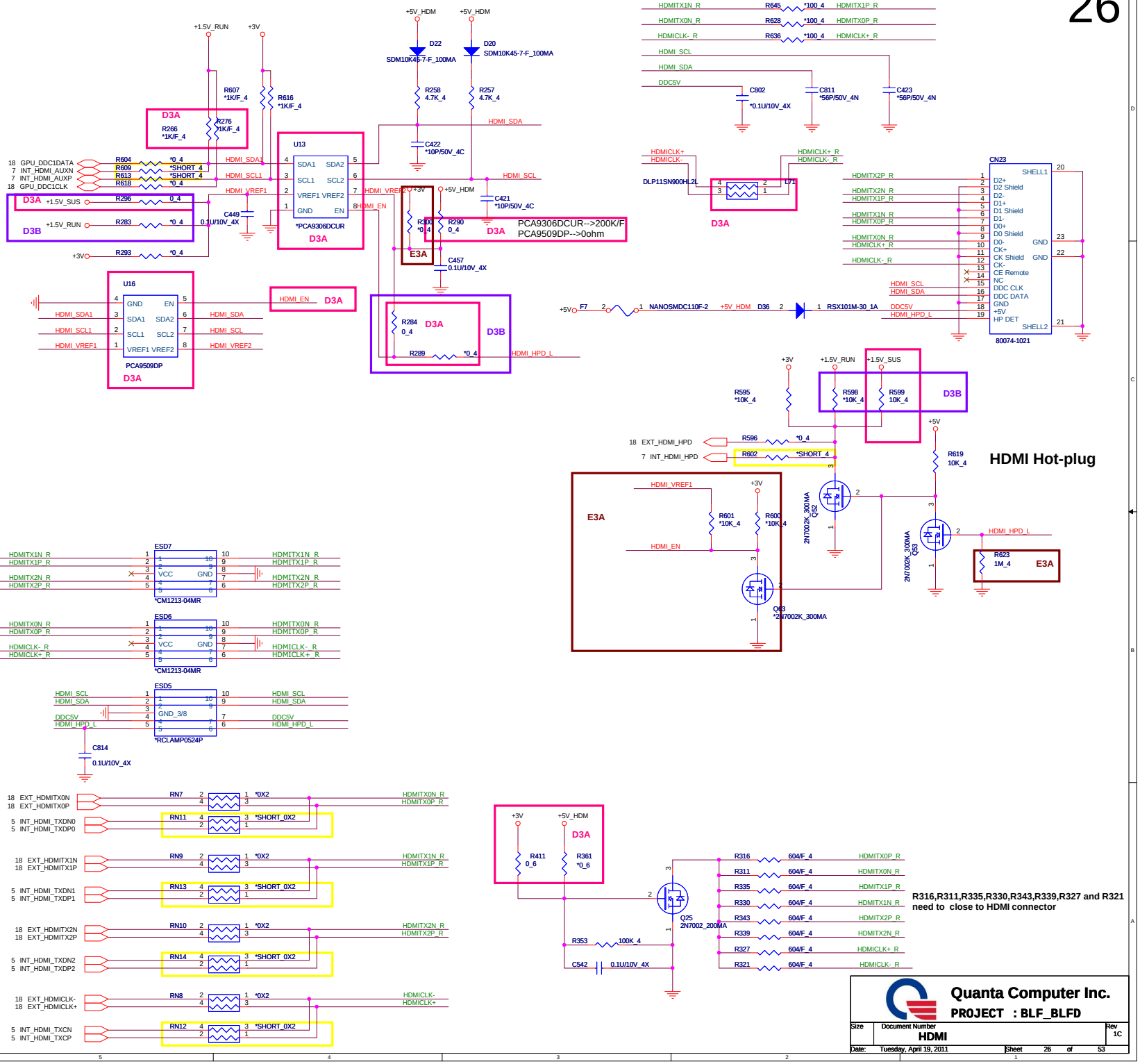
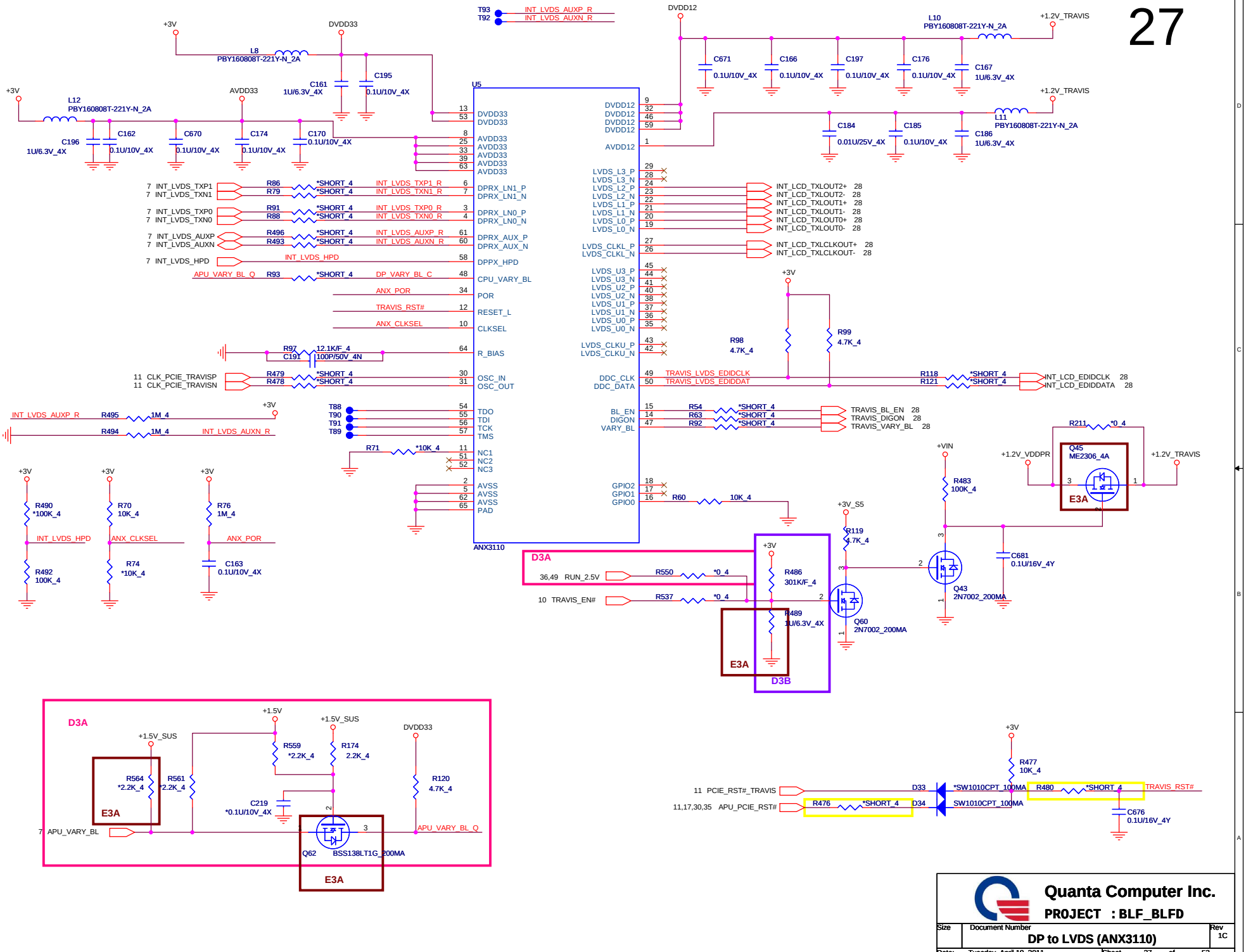
HDMI



Quanta Computer Inc.

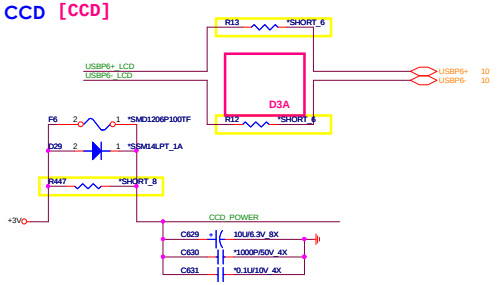
PROJECT : BLF_BLFD

Size	Document Number	Rev
	HDMI	1C
Date: Tuesday, April 19, 2011	Sheet 26 of 53	

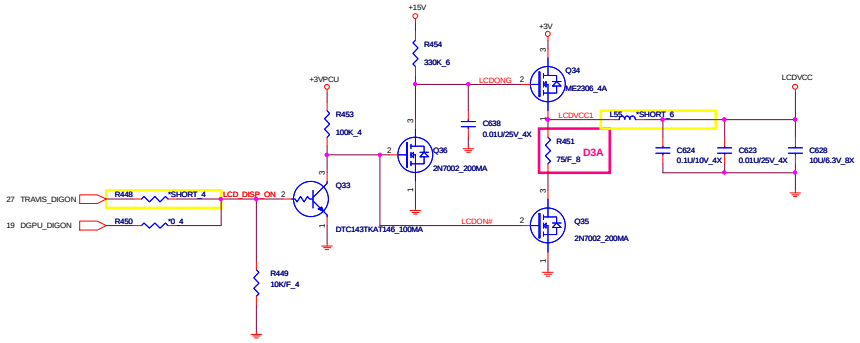


Quanta Computer Inc.		
PROJECT : BLF_BLFD		
Size	Document Number	Rev
	DP to LVDS (ANX3110)	1C
Date: Tuesday, April 19, 2011	Sheet 27 of 53	

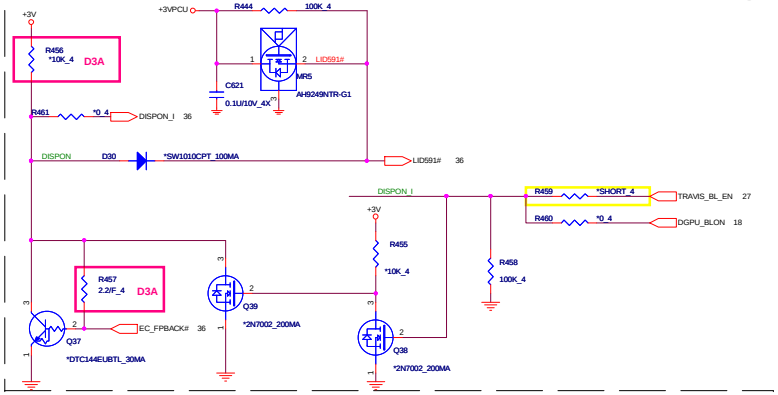
CCD [CCD]



LCD POWER SWITCH [LDS]

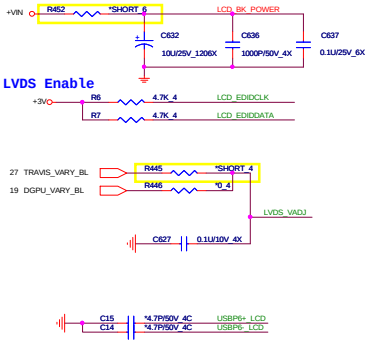


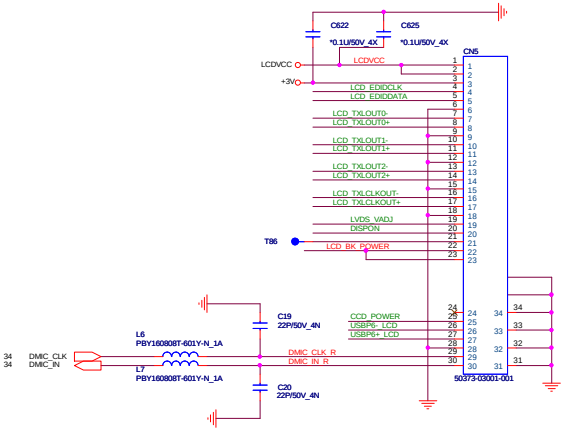
HALL SENSOR&BACK LIGHT SWITCH [HSR]

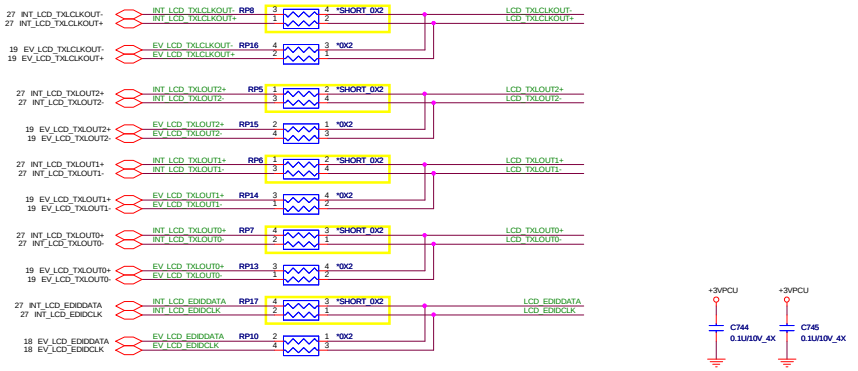


[LDS]

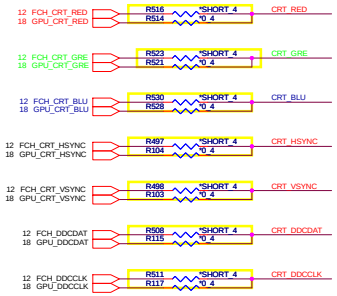
LCD Panel Module

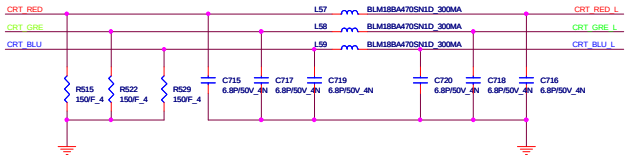


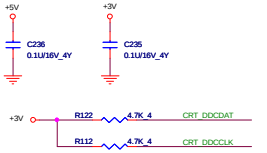


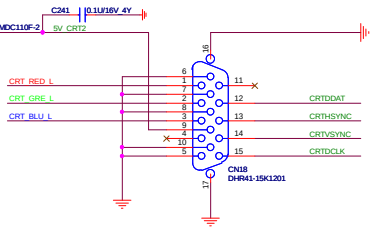


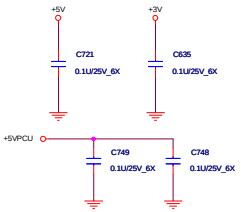
CRT [CRT]

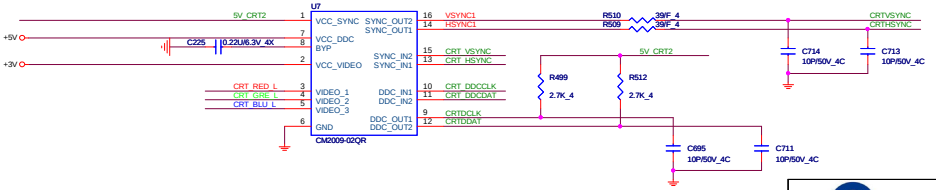












Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	LVDS/CCD/CRT/USB	1C
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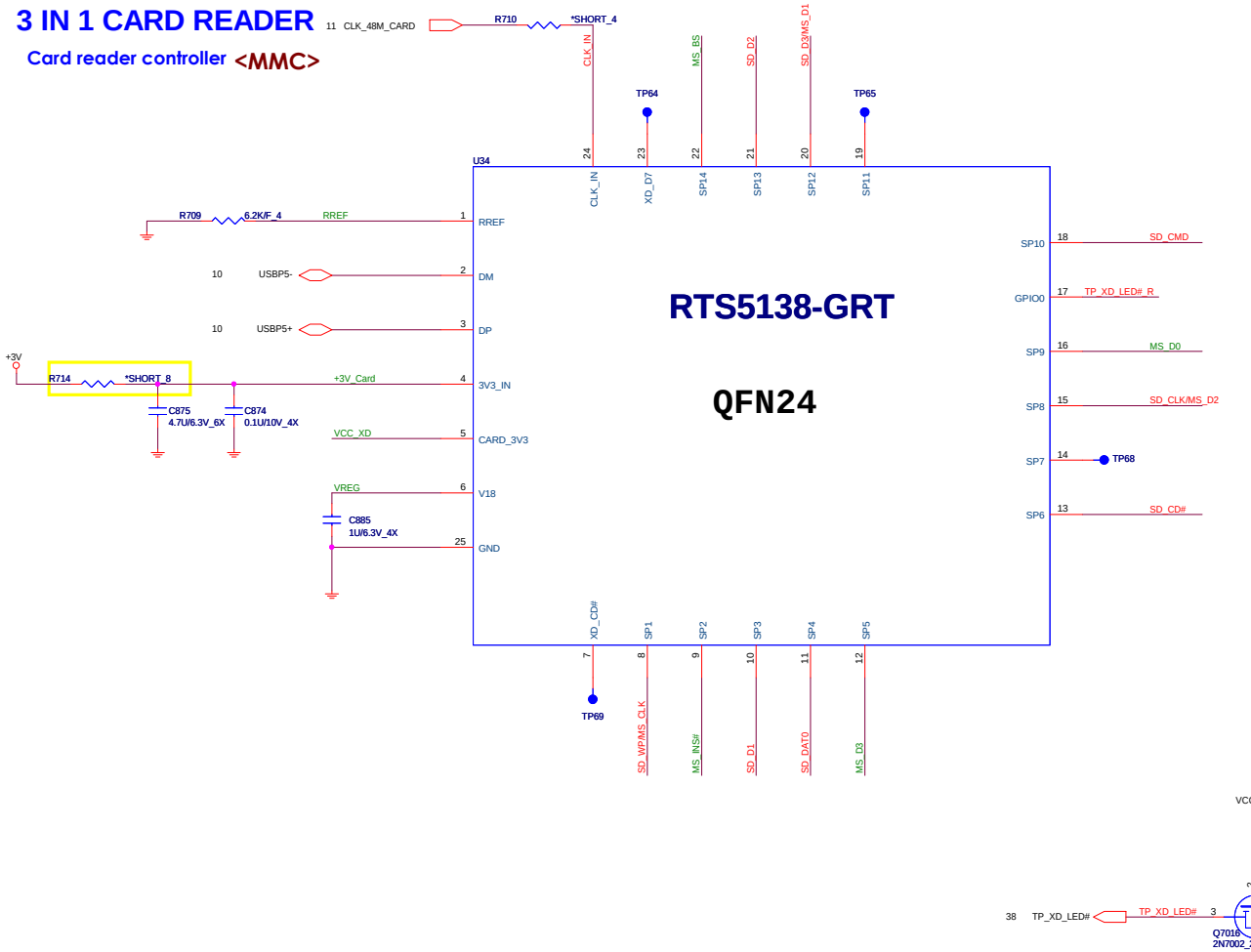
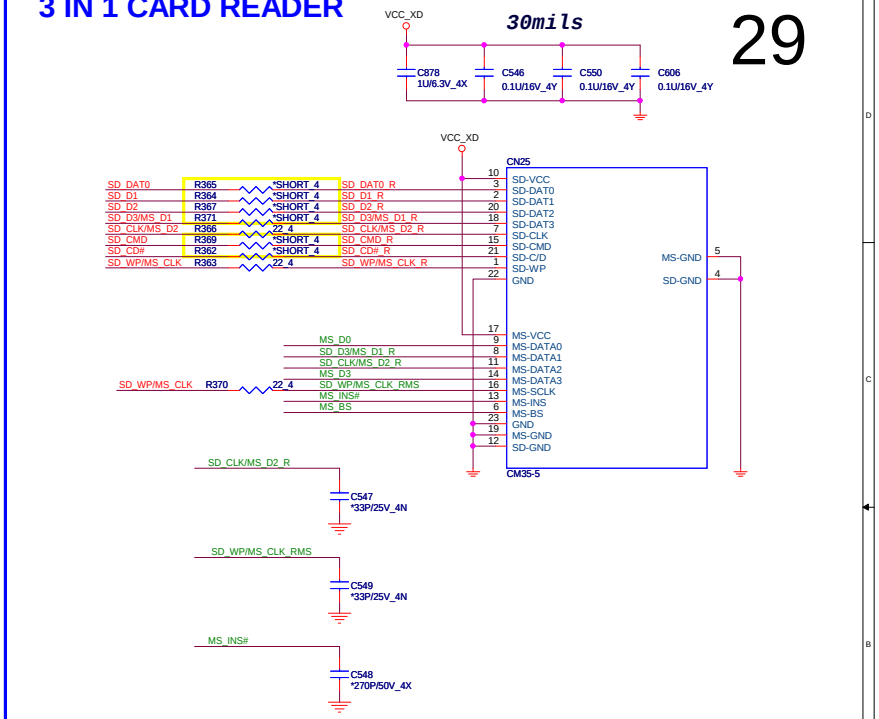
3 IN 1 CARD READER

Card reader controller <MMC>



3 IN 1 CARD READER

29

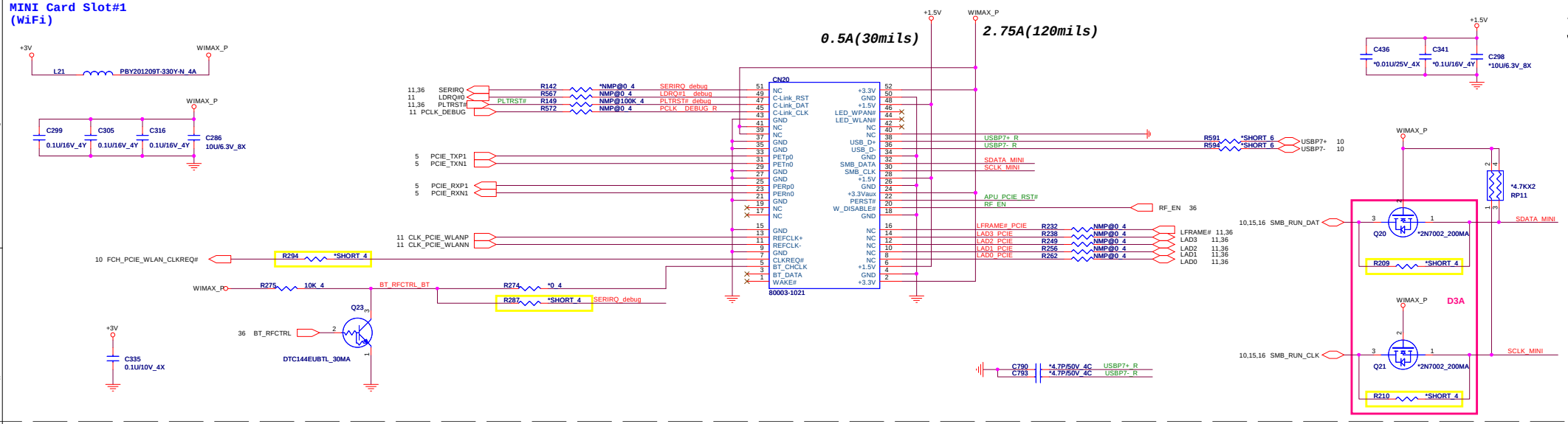


Quanta Computer Inc.

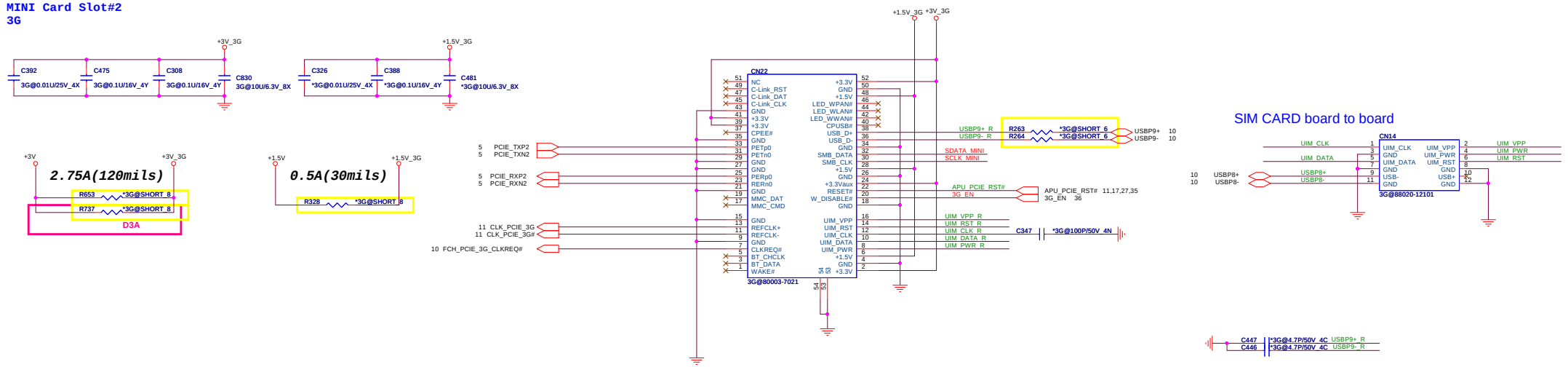
PROJECT : BLF_BLFD

Size	Document Number	Rev
	RTS5138 (Card Reader)	1C
Date: Tuesday, April 19, 2011	Sheet 29 of 53	

MINI Card Slot#1 (WiFi)

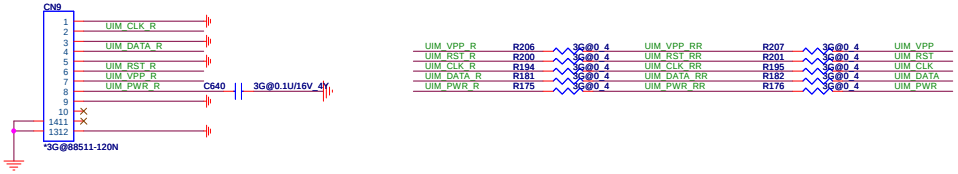


MINI Card Slot#2 3G



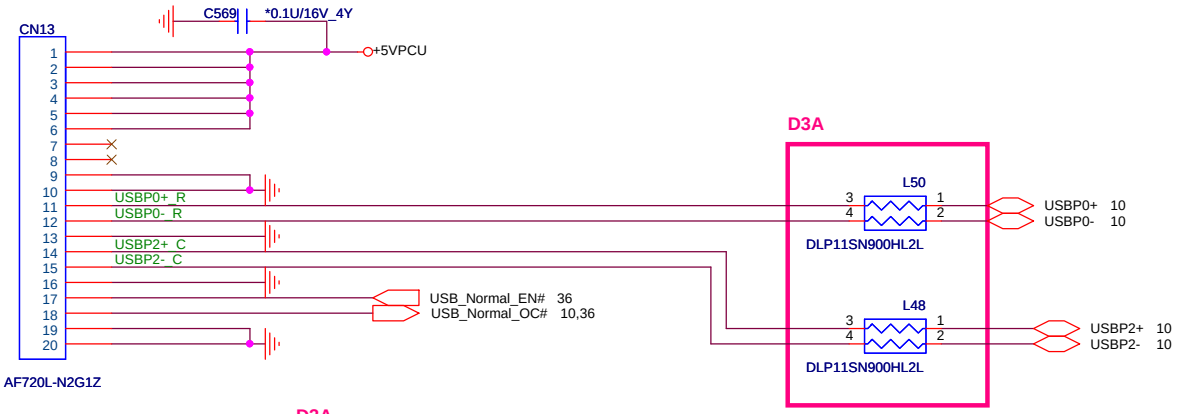
SIM CARD board to board

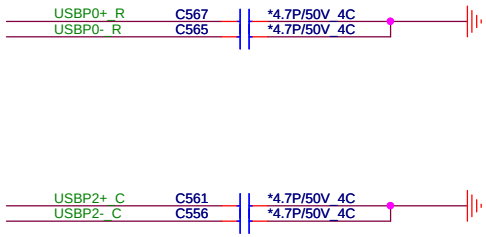
3G CONN

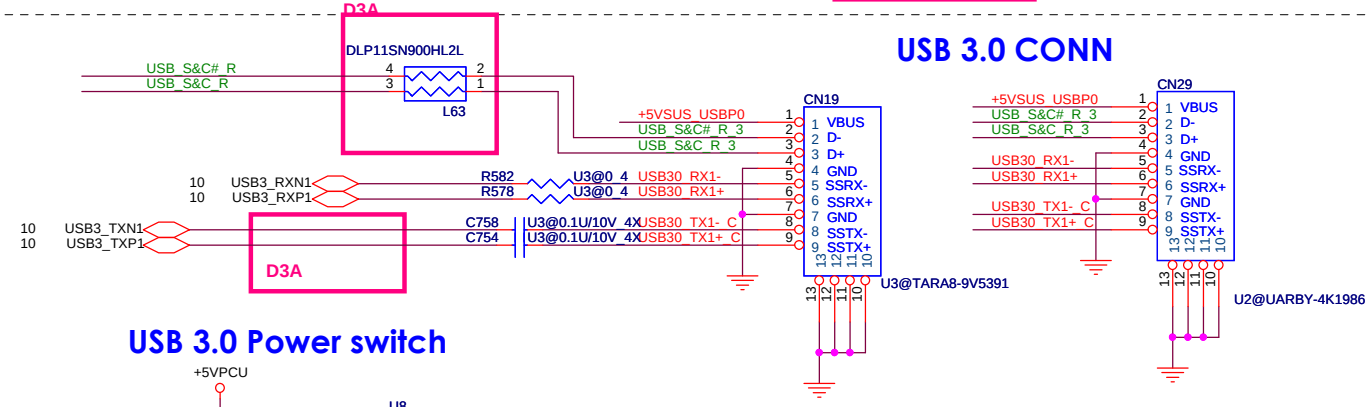


Quanta Computer Inc.	
PROJECT : BLF_BLFD	
Size	Document Number: MINI Card(WLAN/3G/SIM) — Rev 1C
Date: Tuesday, April 19, 2011	Sheet 30 of 53

USB board

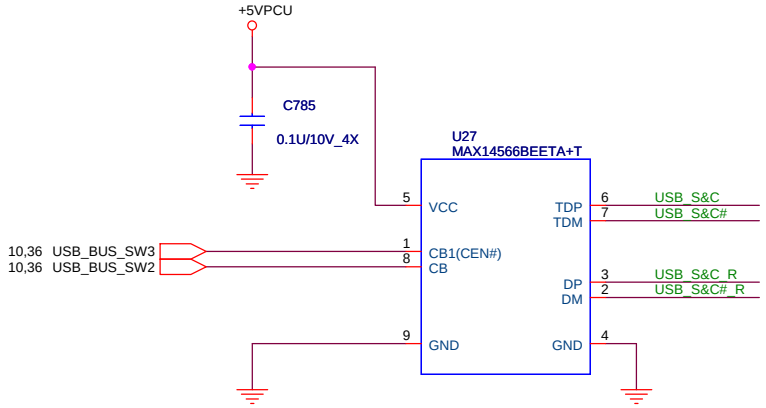




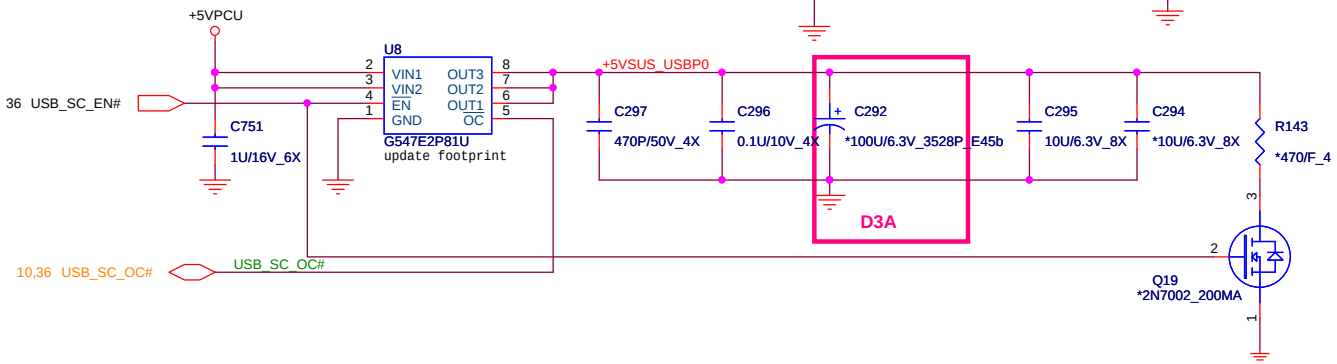


USB 3.0 CONN

USB Sleep & Charge MAXIM solution



USB 3.0 Power switch



CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	USB2.0X1+USB3.0X1	1C

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Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	BLANK	1C
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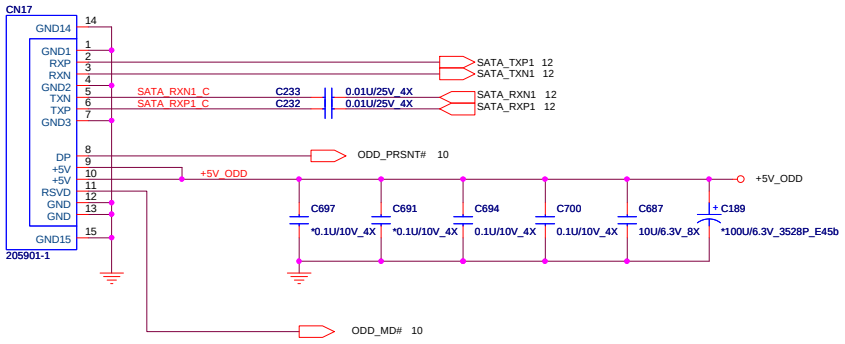
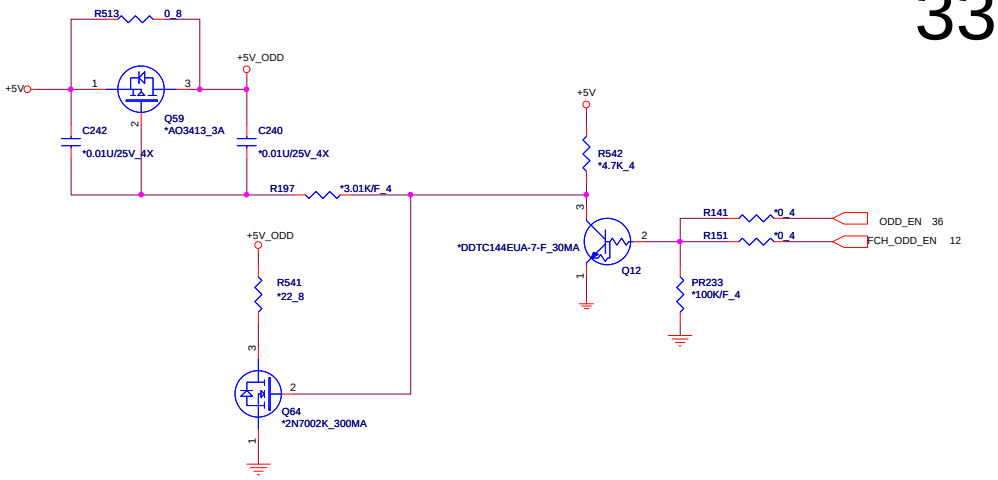
SATA ODD

[ODD]

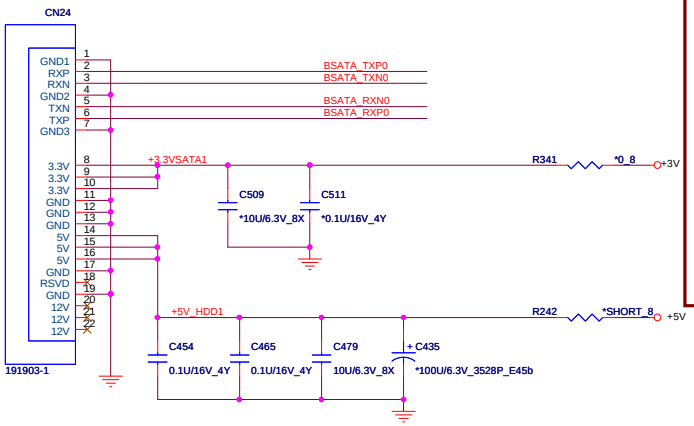


ODD Zero power .

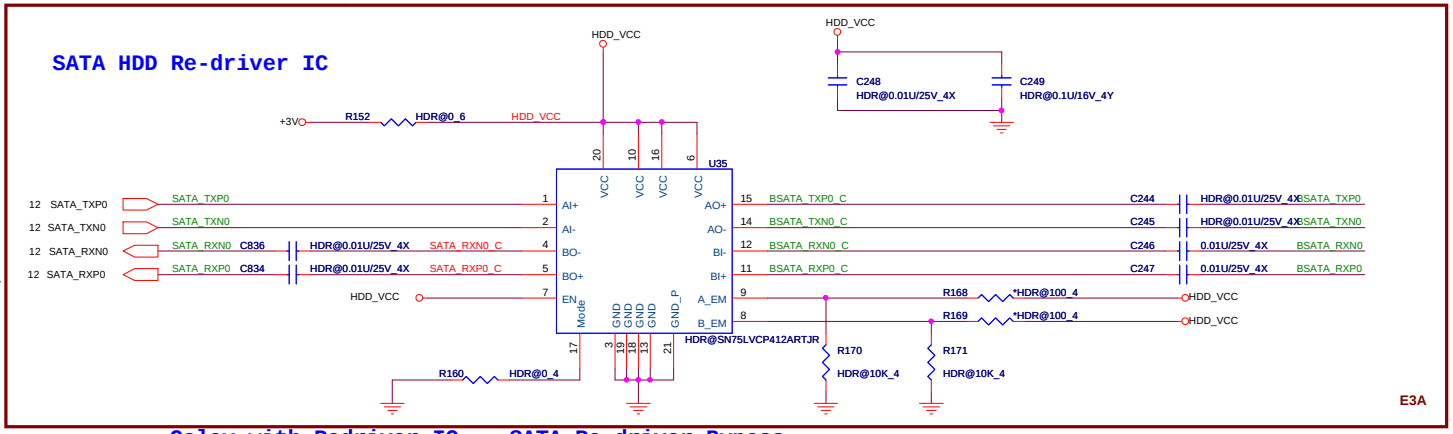


SATA HDD

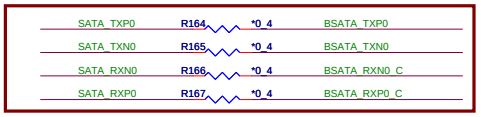
[HDD]



SATA HDD Re-driver IC



Colay with Redriver IC SATA Re-driver Bypass



Quanta Computer Inc.

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Size	Document Number	Rev
	HDD/ODD/MDC	1C

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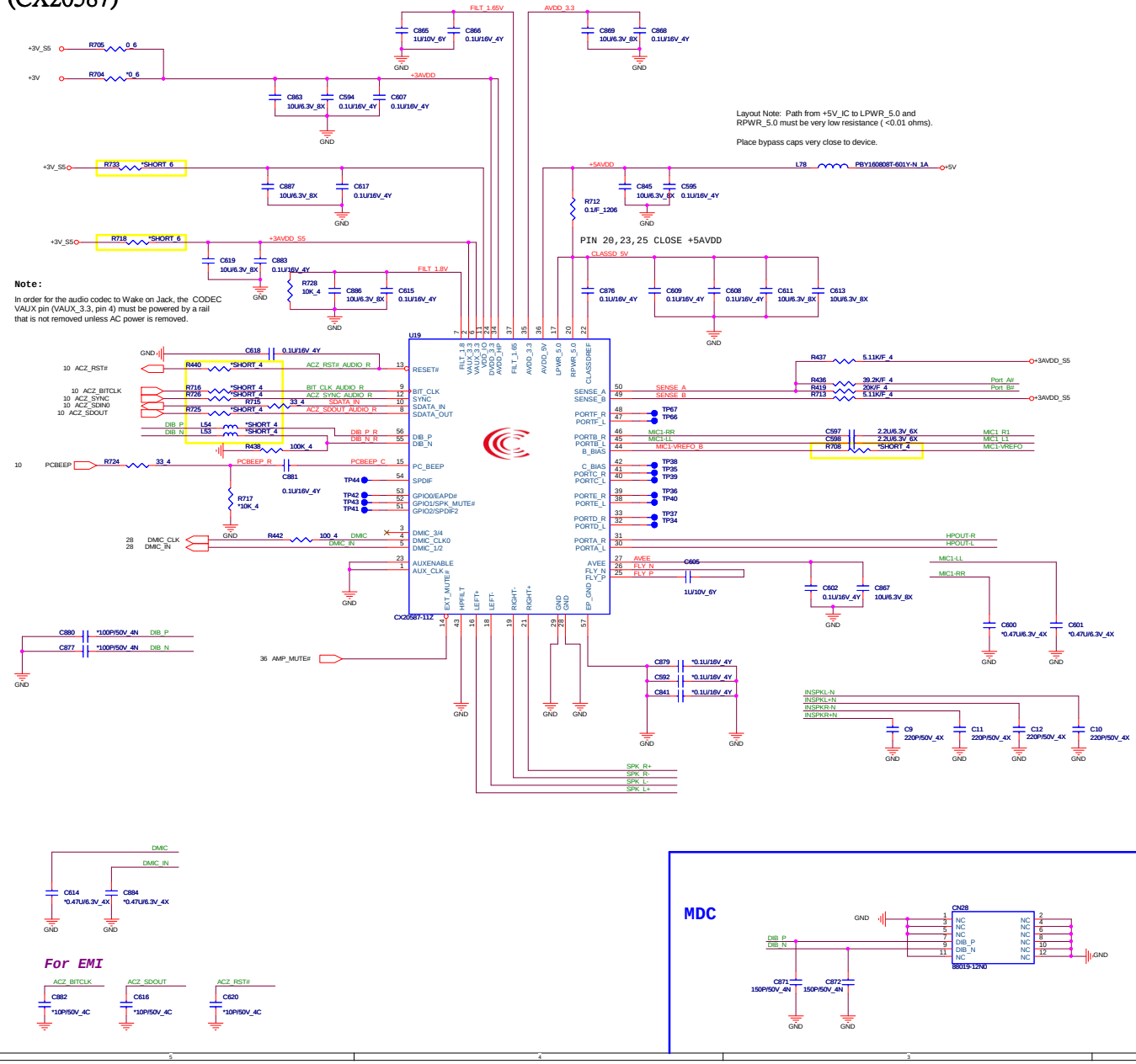
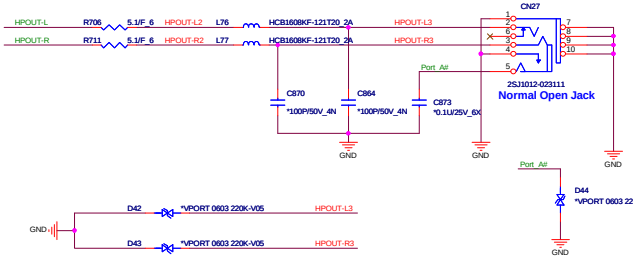
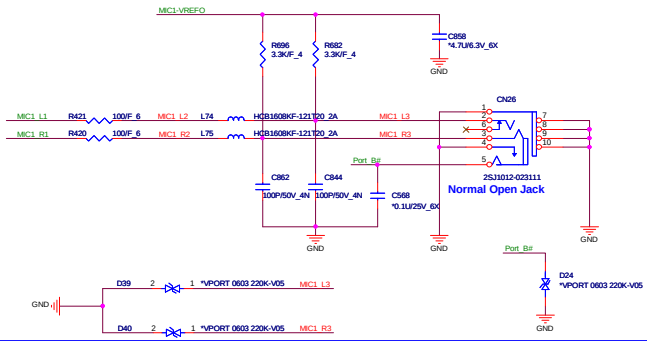
Codec (CX20587)



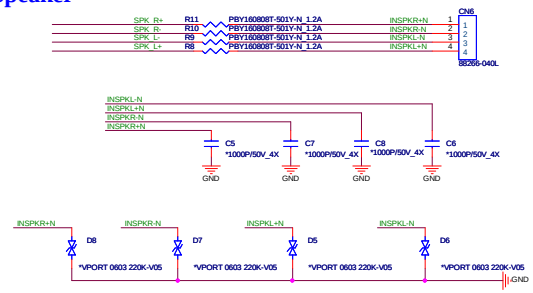
Earphone



External MIC



Internal Speaker



MDC

Quanta Computer Inc.
PROJECT : BLF_BLFD
Size: Document Number: Audio(CX20587)/MDC
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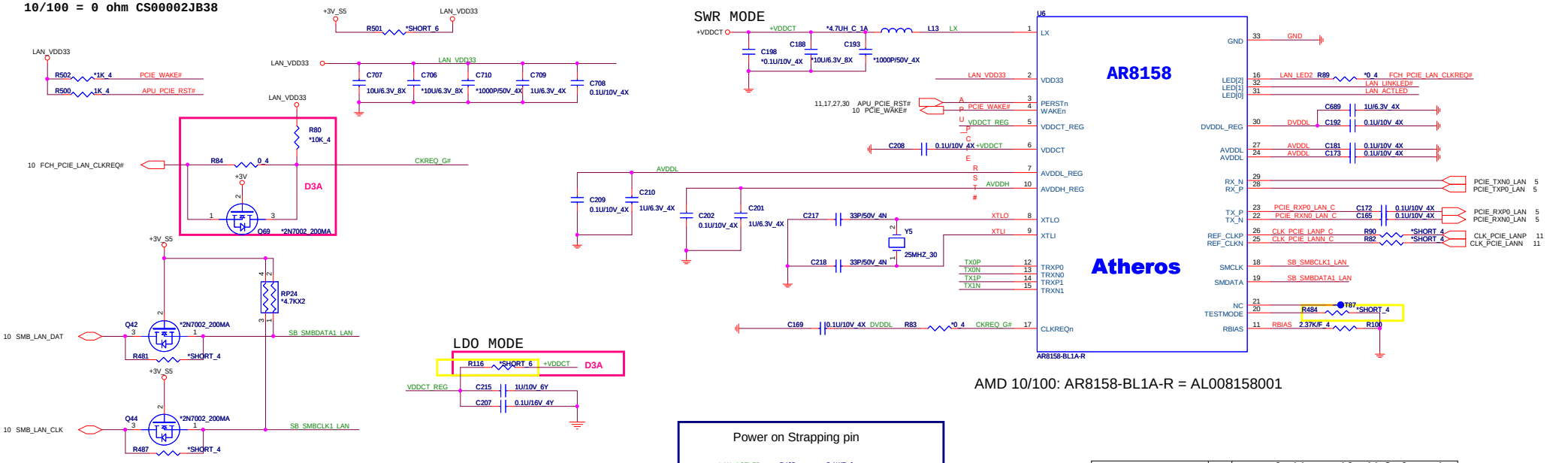
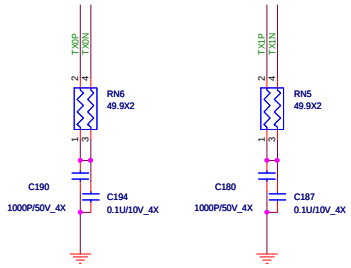
Atheros Lan AR8158

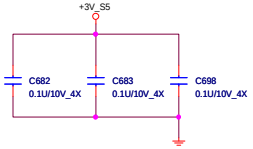
10/100 = 0 ohm CS00002JB38



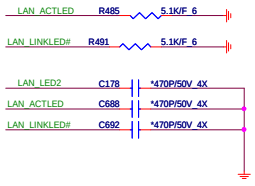
AMD 10/100: AR8158-BL1A-R = AL008158001

PLACE NEAR LAN IC SIDE



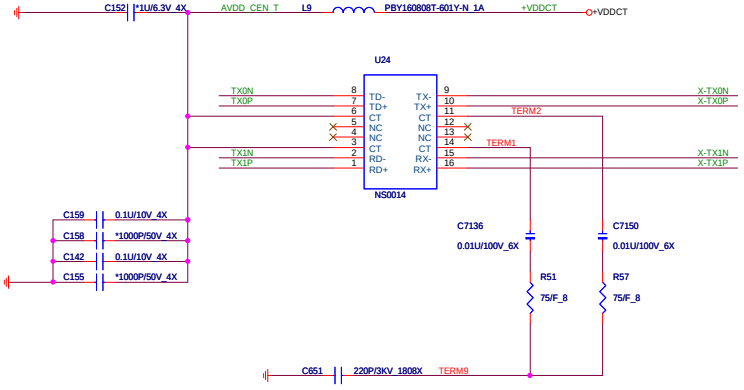


Power on Strapping pin

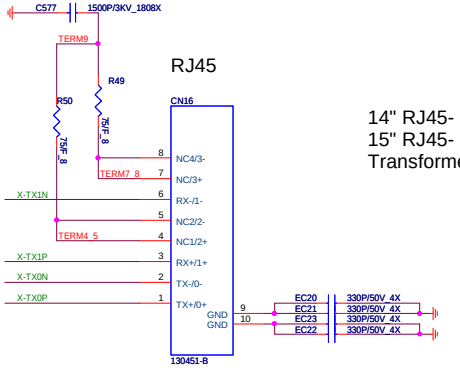


LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low

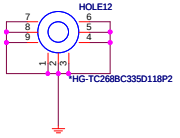
TRANSFORMER



RJ45



14" RJ45- DFTJ08FR164
15" RJ45- DFTJ08FR169
Transformer- DB0EL5LAN02



Quanta Computer Inc.
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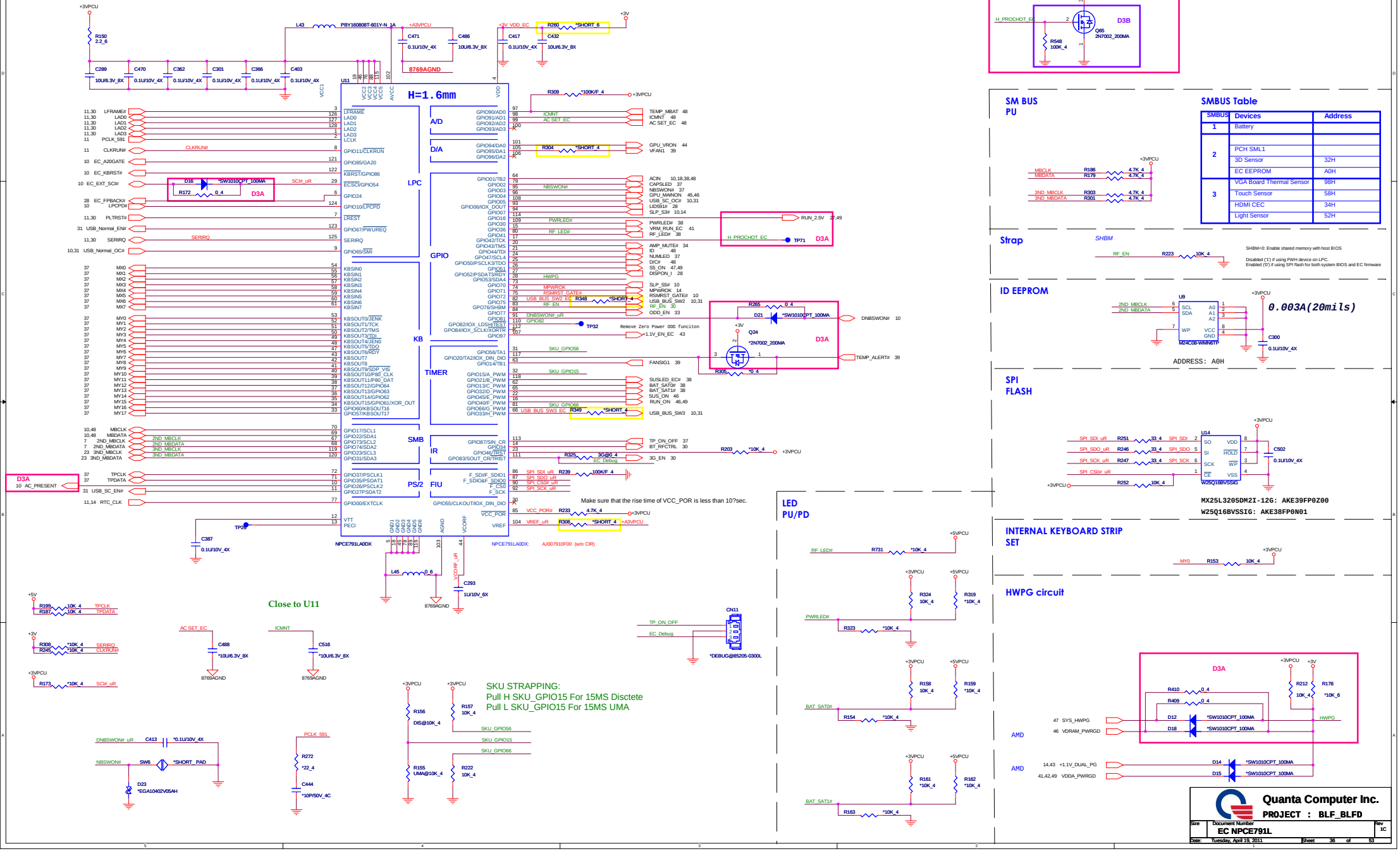
H=1.6mm
LPC
A/D
D/A
GPIO
KB
TIMER
SMB
IR
PS/2
FIU
SM BUS PU
SMBUS Table
SMBUS | Devices | Address
1 | Battery |
2 | PCH SML1 |
2 | 3D Sensor | 32H
2 | EC EEPROM | A0H
3 | VGA Board Thermal Sensor | 98H
3 | Touch Sensor | 58H
3 | HDMI CEC | 34H
3 | Light Sensor | 52H
Strap
SHBM
ID EEPROM
ADDRESS: A0H
SPI FLASH
MX25L3205DM2I-12G: AKE39FP0Z00
W25Q16BVSSIG: AKE38FP0N01
INTERNAL KEYBOARD STRIP SET
HWPG circuit
LED PU/PD
Close to U11
SKU STRAPPING:
Pull H SKU_GPIO15 For 15MS Disctete
Pull L SKU_GPIO15 For 15MS UMA
Make sure that the rise time of VCC_POR is less than 10?sec.
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EC NPCE791L
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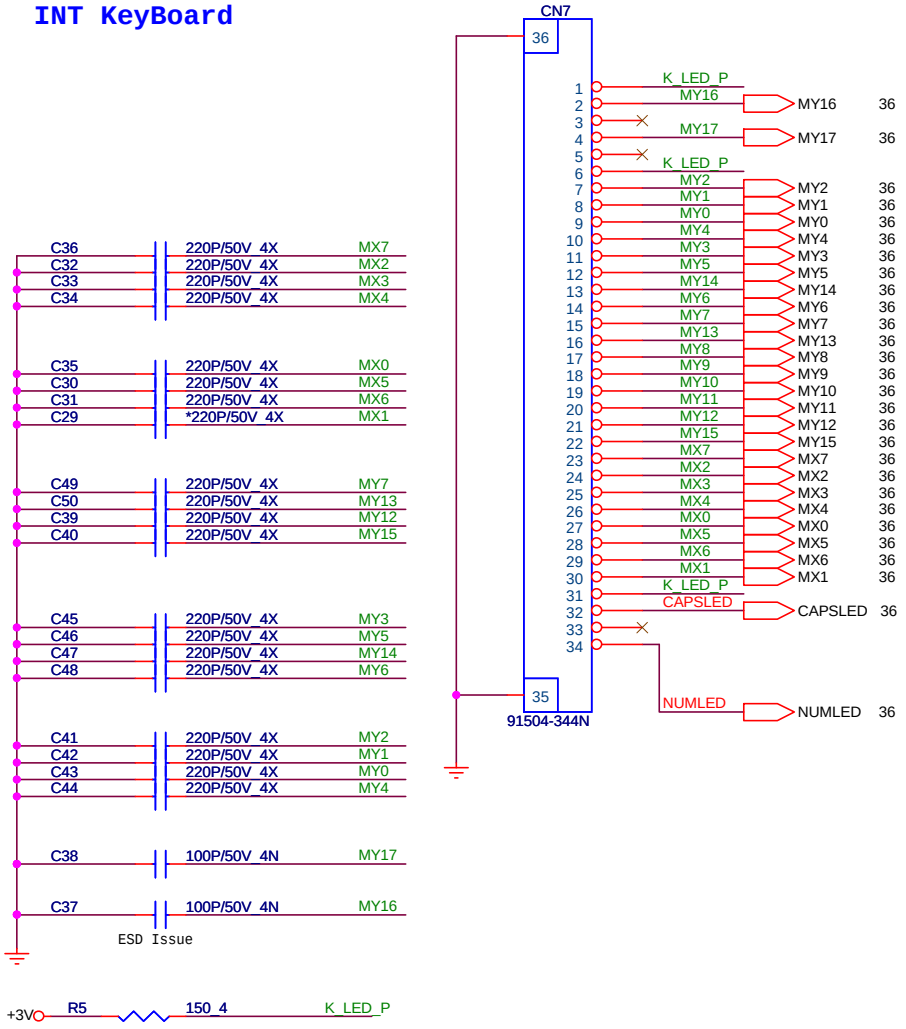
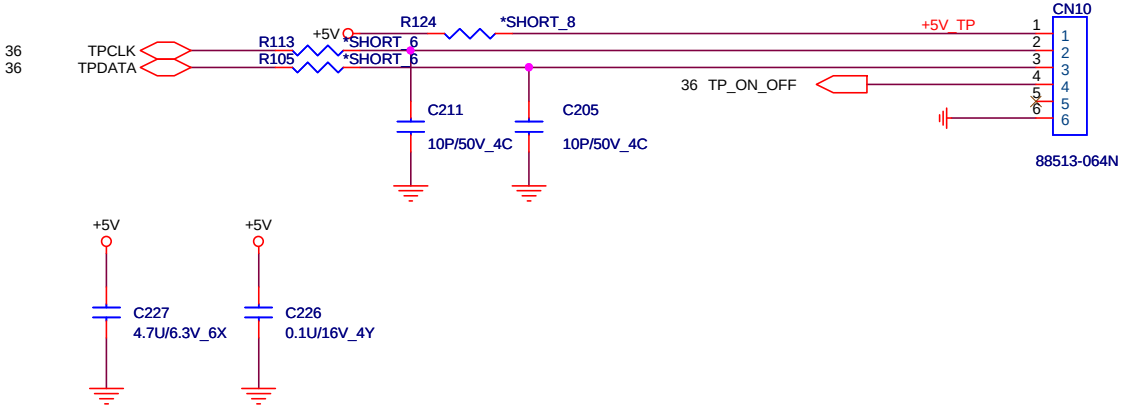
KEY BOARD Connector

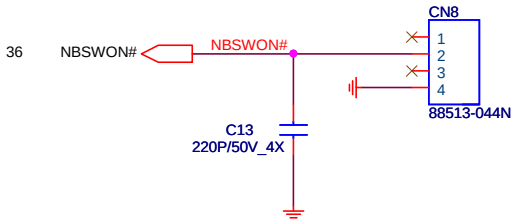
INT KeyBoard



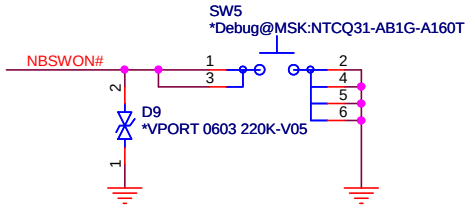
TOUCH PAD BOARD



Power Board (UIF)



Power Switch (debug only)



Quanta Computer Inc.

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	FP/TP/KB Conn	1C
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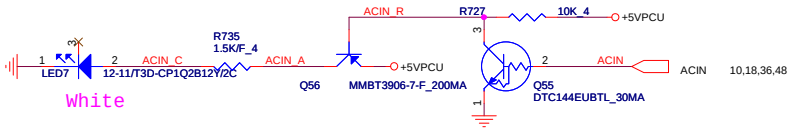
LED

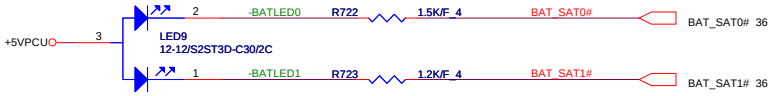
AC-IN



White

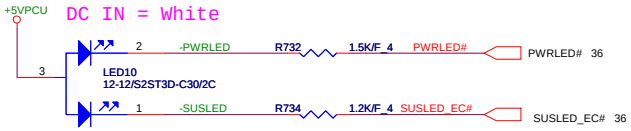
BATERRY

Full Charge = White



Charging = Orange

POWER

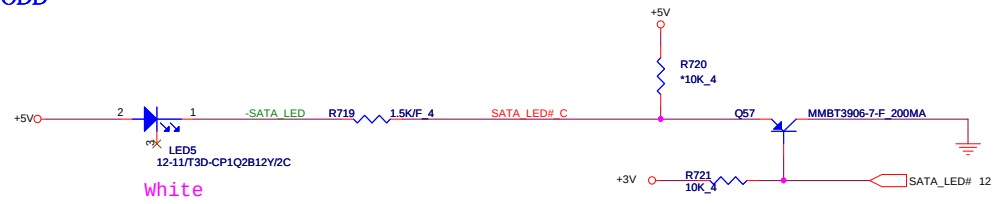


S3 Mode = Orange

CARDREADER

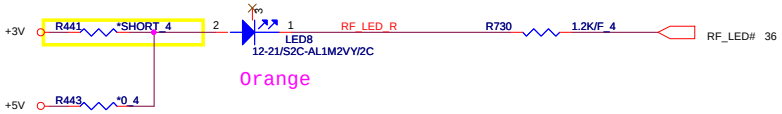
White

HDD/ODD



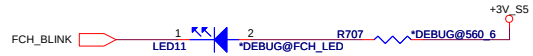
White

RF LED

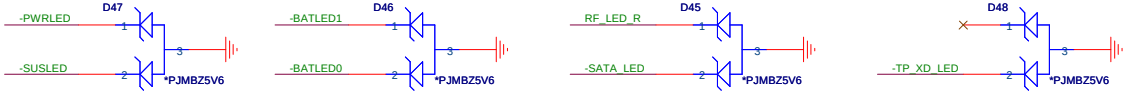


Orange

When ON, means in S0
When BLINK, means in S3
When OFF, means in S5



Orange



Quanta Computer Inc.

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	LED	1C

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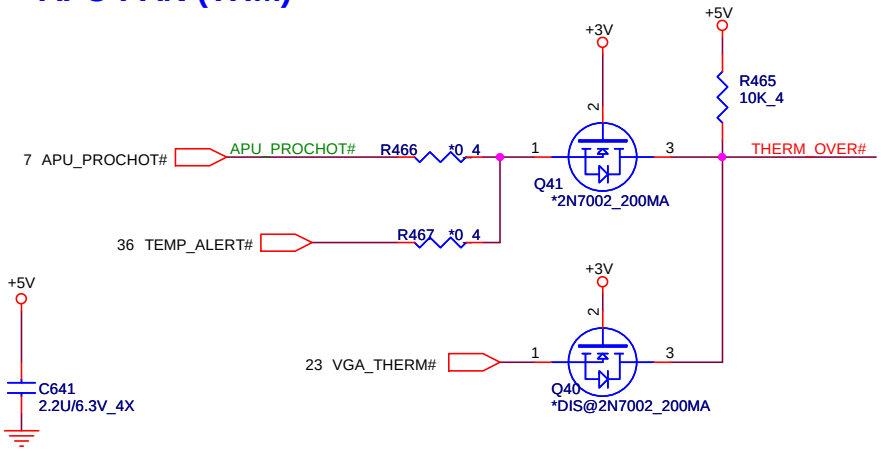
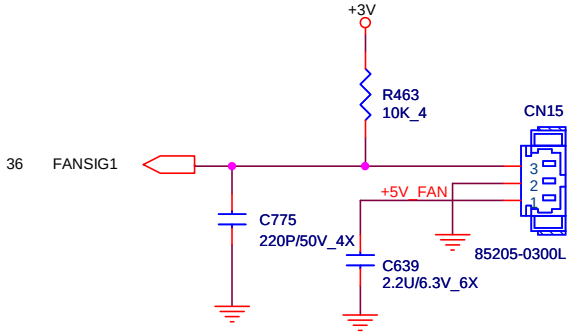
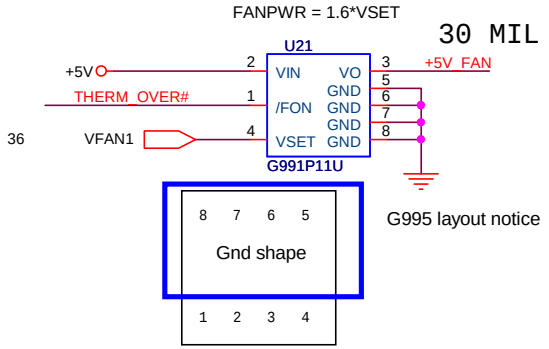
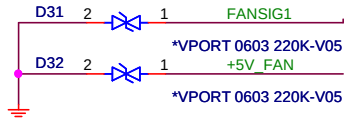
APU FAN (THM)









Quanta Computer Inc.		
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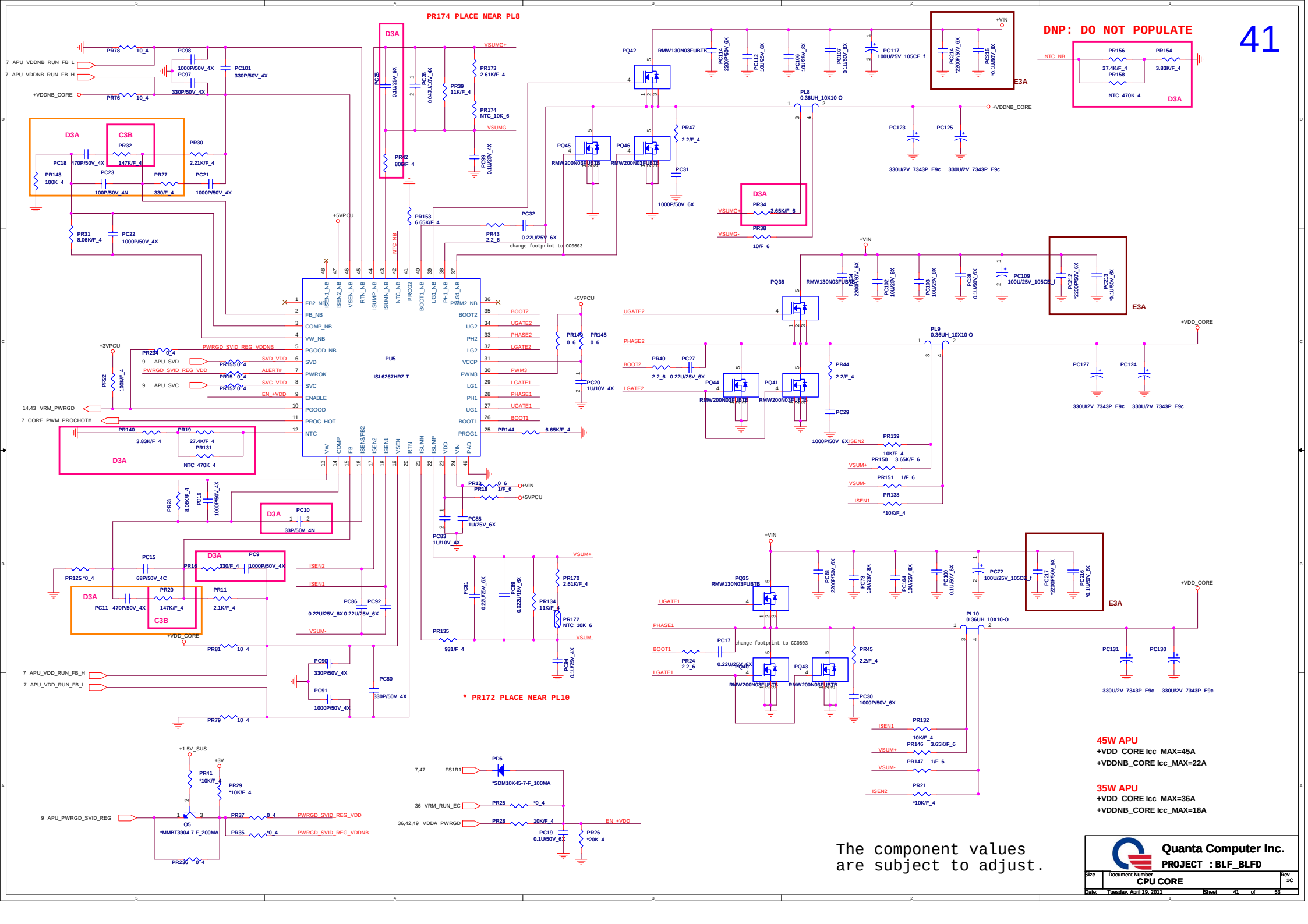
PR174 PLACE NEAR PL8
DNP: DO NOT POPULATE
41
PU5
ISL6267HRZ-T
PQ42
RMW130N03FUBTB
PQ45
PQ46
RMW200N03FUBTB
PQ36
PQ44
PQ41
PQ35
PQ40
PQ43
PL8 0.36UH_10X10-O
PL9 0.36UH_10X10-O
PL10 0.36UH_10X10-O
E3A
D3A
C3B
+VIN
+VDDNB_CORE
+VDD_CORE
+5VPCU
+3VPCU
+1.5V_SUS
+3V
VSUMG+
VSUMG-
VSUM+
VSUM-
UGATE2
PHASE2
BOOT2
LGATE2
UGATE1
PHASE1
BOOT1
LGATE1
ISEN1
ISEN2
PWRGD_SVID_REG_VDDNB
PWRGD_SVID_REG_VDD
PWRGD_SVID_REG_VDDNB
APU_SVD
APU_SVC
SVD_VDD
SVC_VDD
EN +VDD
ALERT#
VRM_PWRGD
CORE_PWM_PROCHOT#
APU_VDDNB_RUN_FB_L
APU_VDDNB_RUN_FB_H
APU_VDD_RUN_FB_H
APU_VDD_RUN_FB_L
APU_PWRGD_SVID_REG
VRM_RUN_EC
VDDA_PWRGD
EN +VDD
FS1R1
NTC_NB
* PR172 PLACE NEAR PL10
45W APU
+VDD_CORE Icc_MAX=45A
+VDDNB_CORE Icc_MAX=22A
35W APU
+VDD_CORE Icc_MAX=36A
+VDDNB_CORE Icc_MAX=18A
The component values are subject to adjust.
Quanta Computer Inc.
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Size
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CPU CORE
Rev 1C
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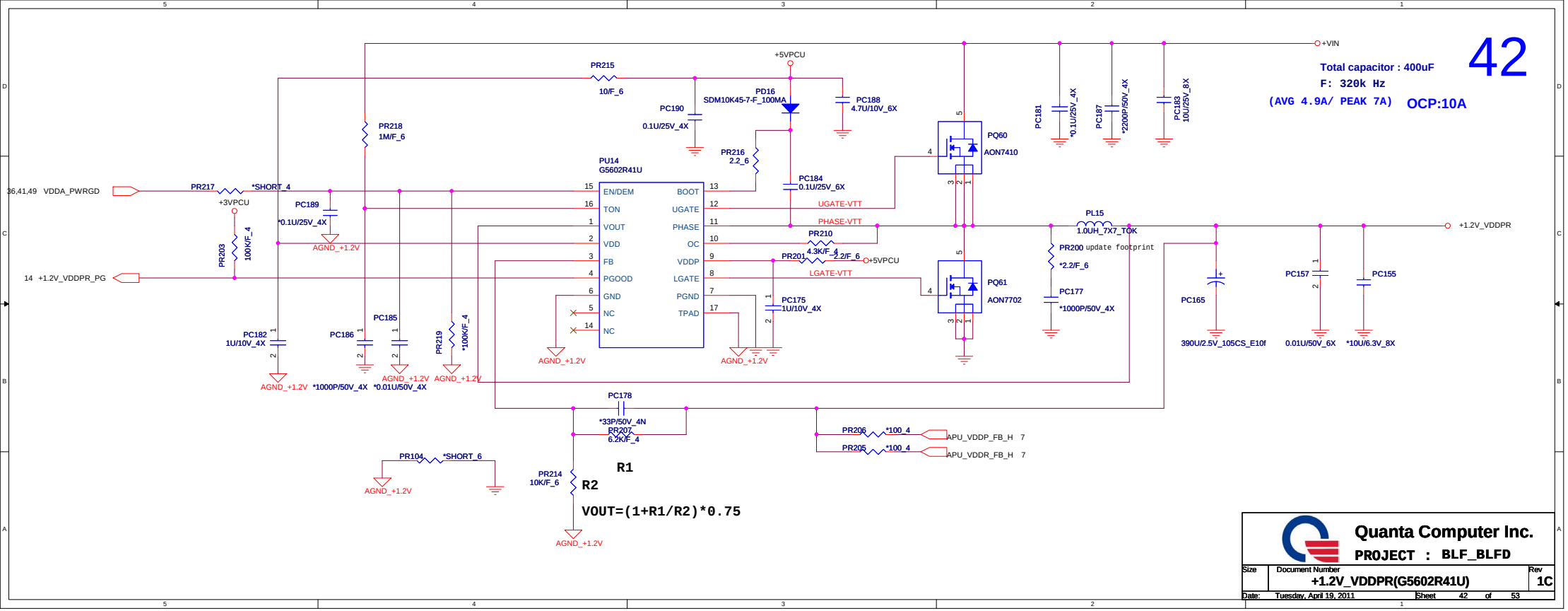
42
Total capacitor : 400uF
F: 320k Hz
(AVG 4.9A/ PEAK 7A) OCP:10A
+VIN
+5VPCU
PR215
10/F_6
PD16
SDM10K45-7-F_100MA
PC190
0.1U/25V_4X
PC188
4.7U/10V_6X
PR218
1M/F_6
PR216
2.2_6
PC184
0.1U/25V_6X
PU14
G5602R41U
EN/DEM
TON
VOUT
VDD
FB
PGOOD
GND
NC
NC
BOOT
UGATE
PHASE
OC
VDDP
LGATE
PGND
TPAD
UGATE-VTT
PHASE-VTT
LGATE-VTT
PQ60
AON7410
PQ61
AON7702
PC181
*0.1U/25V_4X
PC187
*220P/50V_4X
PC183
10U/25V_8X
36,41,49 VDDA_PWRGD
PR217
*SHORT_4
+3VPCU
PC189
*0.1U/25V_4X
AGND_+1.2V
PR203
100K/F_4
14 +1.2V_VDDPR_PG
PR210
4.3K/F_4
PR201
2.2/F_6
+5VPCU
PC175
1U/10V_4X
PL15
1.0UH_7X7_T0K
+1.2V_VDDPR
PR200 update footprint
*2.2/F_6
PC177
*1000P/50V_4X
PC165
390U/2.5V_105CS_E10f
PC157
0.01U/50V_6X
PC155
*10U/6.3V_8X
PC182
1U/10V_4X
PC186
PC185
*0.01U/50V_4X
PR219
*100K/F_4
AGND_+1.2V
*1000P/50V_4X
PC178
*33P/50V_4N
PR207
6.2K/F_4
PR206
*100_4
PR205
*100_4
APU_VDDP_FB_H 7
APU_VDDR_FB_H 7
PR104
*SHORT_6
PR214
10K/F_6
R1
R2
VOUT=(1+R1/R2)*0.75
Quanta Computer Inc.
PROJECT : BLF_BLFD
Size
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+1.2V_VDDPR(G5602R41U)
Rev
1C
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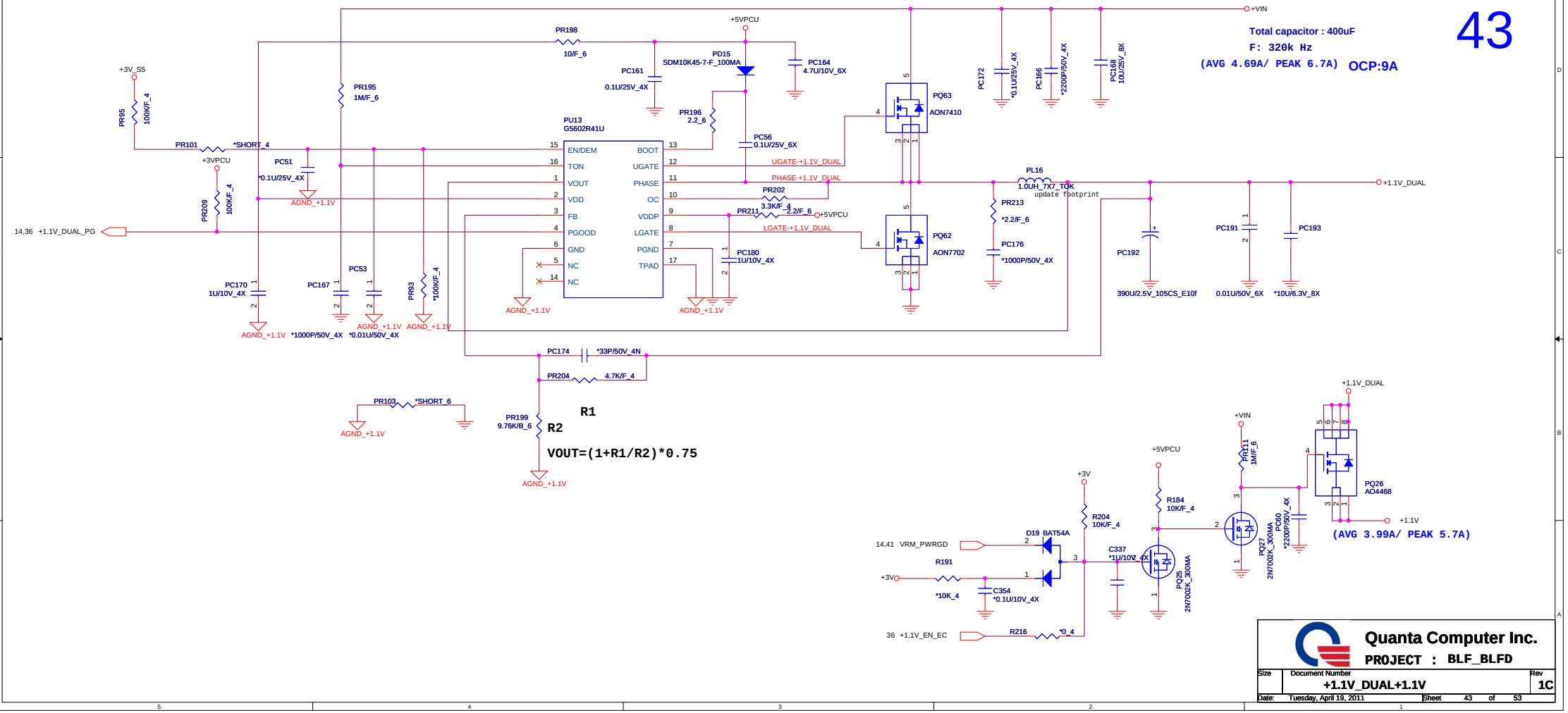

Quanta Computer Inc.		
PROJECT : BLF_BLFD		
Size	Document Number	Rev
	+1.1V_DUAL+1.1V	1C
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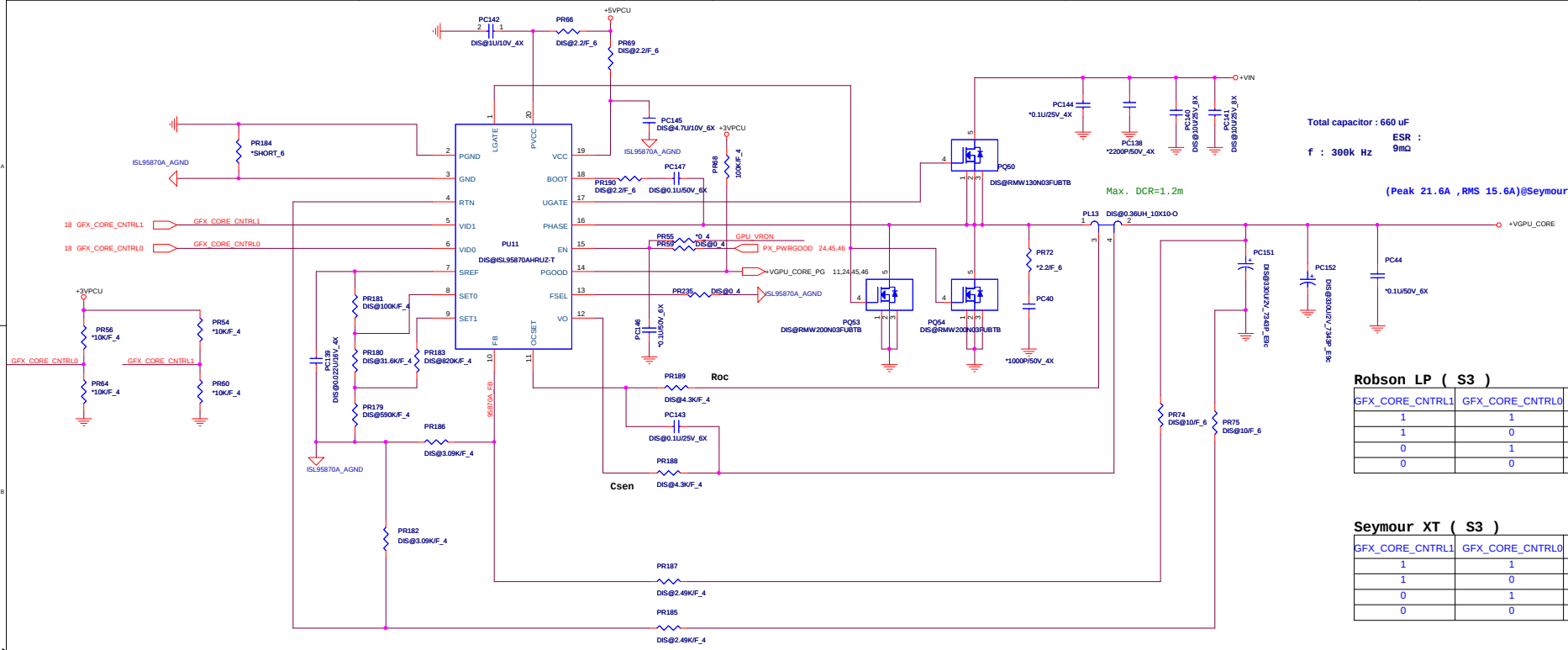

Robson LP (S3)

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.12V

Seymour XT (S3)

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.9V
1	0	1.05V
0	1	1.1V
0	0	1.15V

PCIE_VDDC

Madison,Park-->1.0V

	Madison,Park
R1	25.5K/F_4 (CS32552FB11)
R2	100K/F_4 (CS41002FB28)

Quanta Computer Inc.
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Size	Document Number	Rev
	GPU	1C

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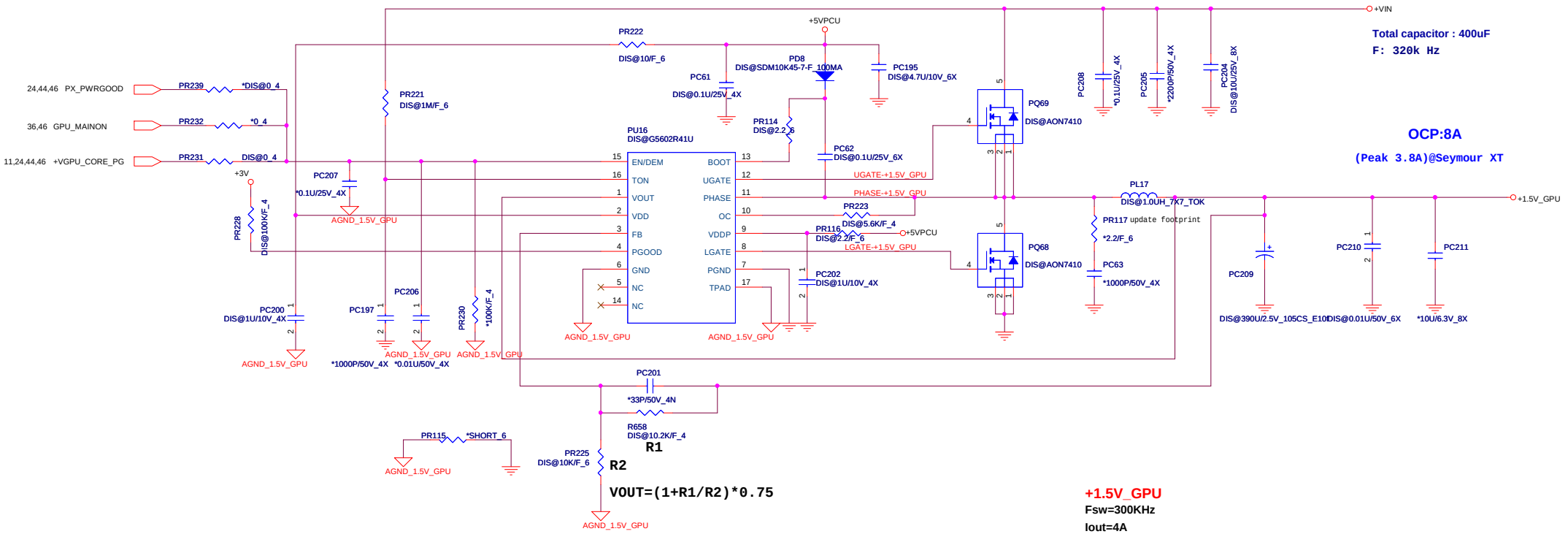

Quanta Computer Inc.		
PROJECT : BLF_BLFD		
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(Peak 0.5A, AVG 0.35A)

(Peak 0.1A, AVG 0.07A)

RT8207LGQW
PU9
FOR DDR III

RDSon=2.3m ohm

OCP:16A
(Peak 13.72A, AVG 10.129A)
ESR : 9mΩ
f : 400k Hz

For RT8207A 400KHZ

Vout = (R1/R2) X 0.75 + 0.75

MEM_P1V5	MEM_P1V35	+1.5VSUS
1	DONT CARE	1.50V
0	1	1.35V
0	0	1.25V

(Peak 2.8A ,RMS 2.3A)
(Peak 6.4A ,RMS 4.4A)

Quanta Computer Inc.	PROJECT : BLF_BLFD
Size	Document Number: DDR1.5V(RT8207LGQW) — Rev: 1C
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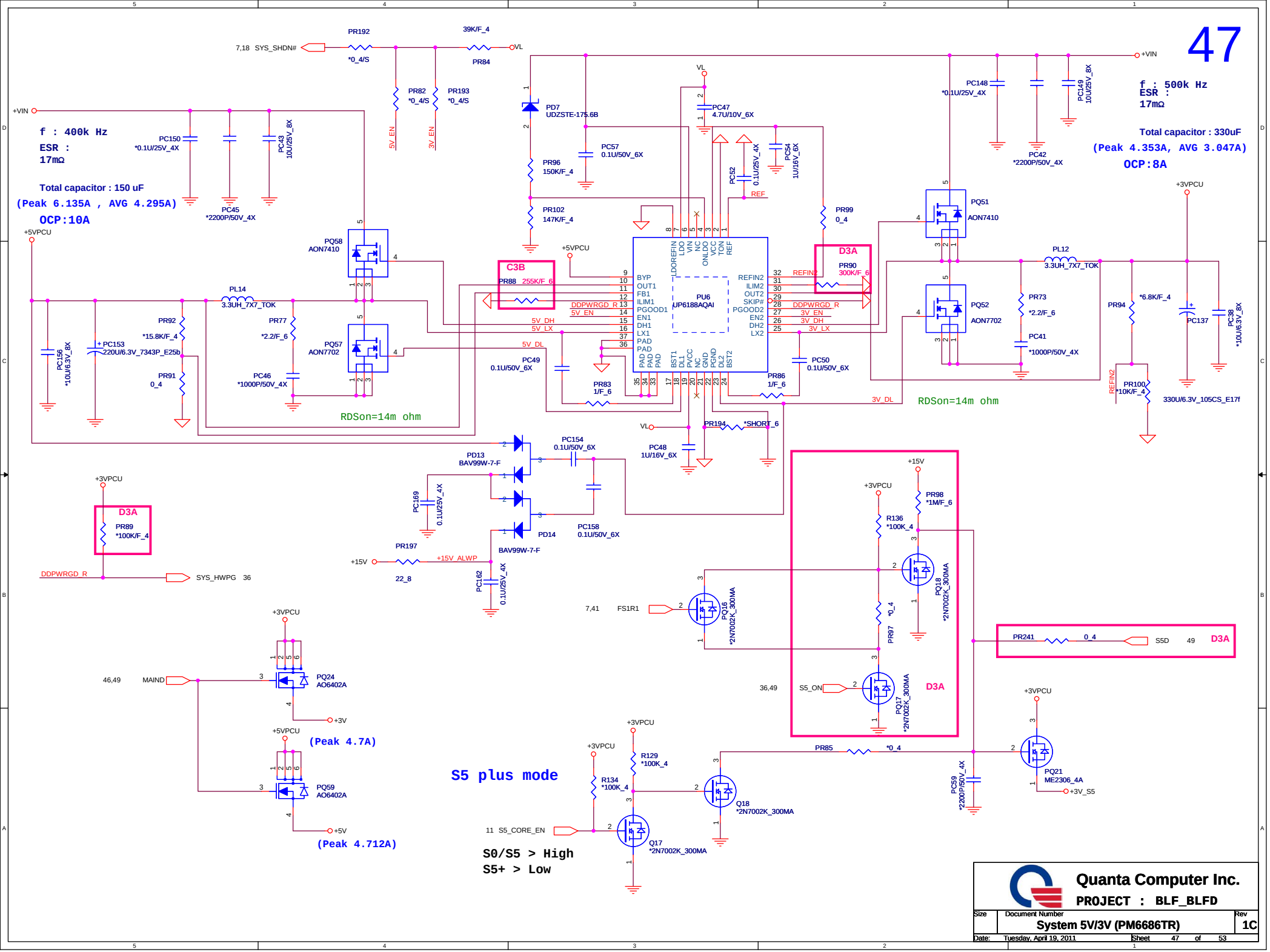
f : 400k Hz
ESR : 17mΩ
Total capacitor : 150 uF
(Peak 6.135A , AVG 4.295A)
OCP:10A
f : 500k Hz
ESR : 17mΩ
Total capacitor : 330uF
(Peak 4.353A, AVG 3.047A)
OCP:8A
RDSon=14m ohm
RDSon=14m ohm
S5 plus mode
S0/S5 > High
S5+ > Low
(Peak 4.7A)
(Peak 4.712A)
UP6188AQAI
PU6
AON7410
AON7702
AO6402A
2N7002K_300MA
ME2306_4A
BAV99W-7-F
UDZSTE-175.6B
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System 5V/3V (PM6686TR)
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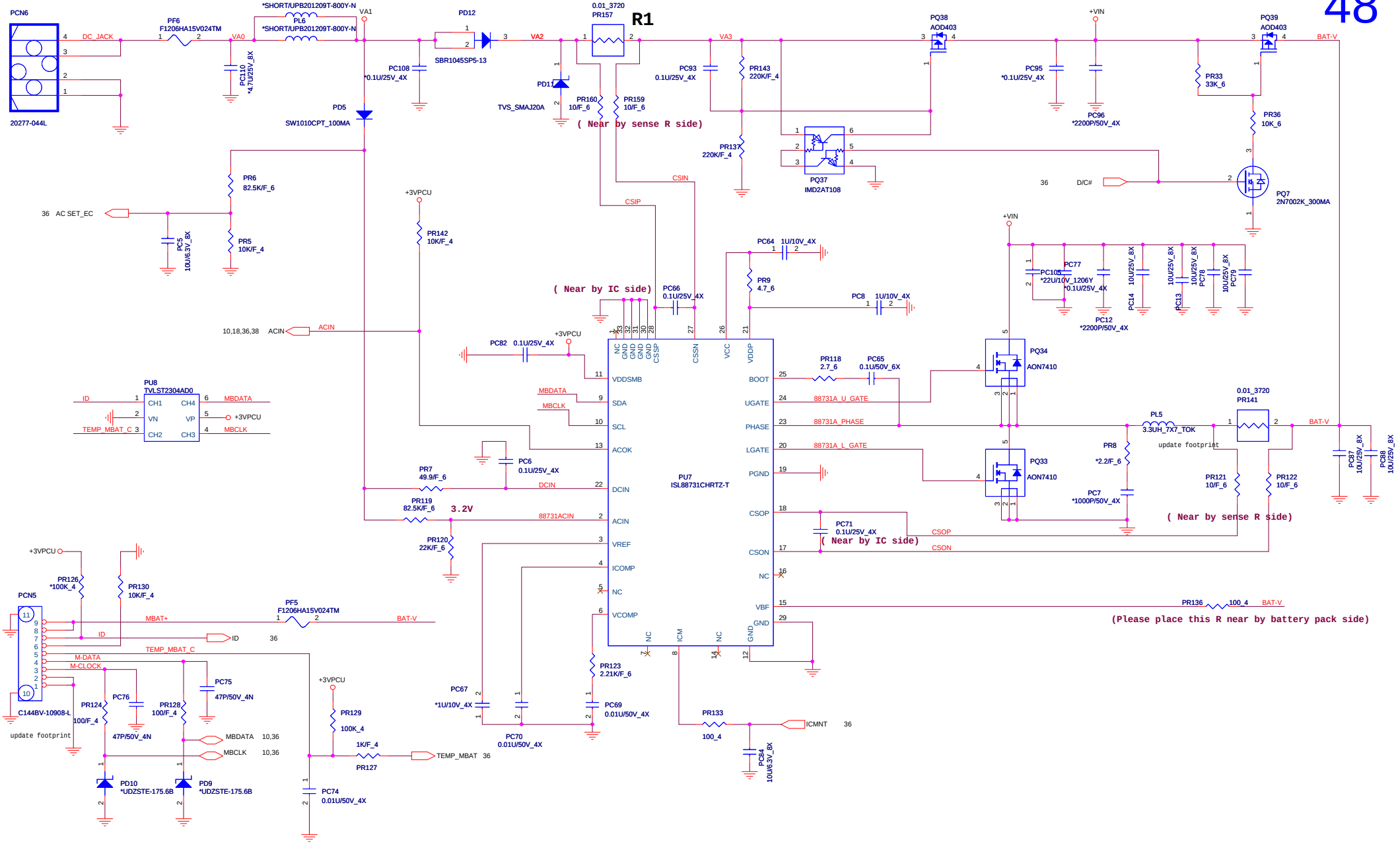

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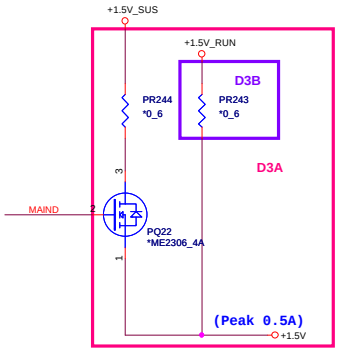
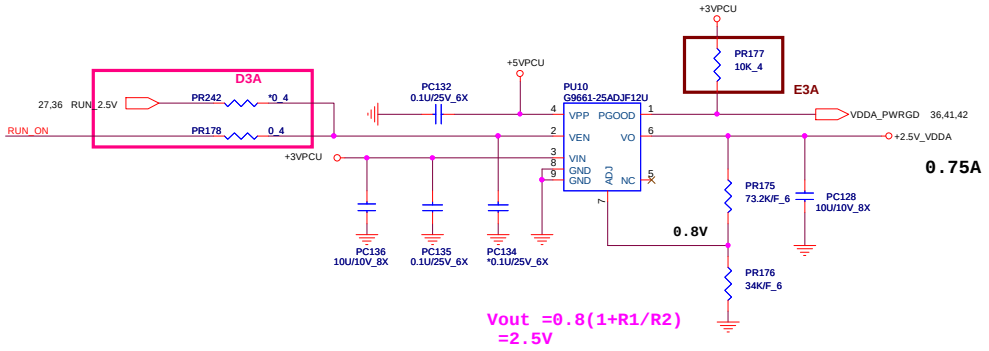
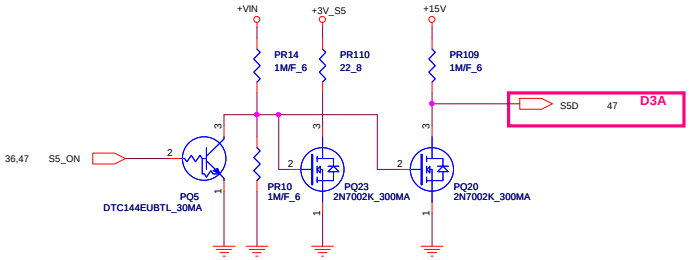
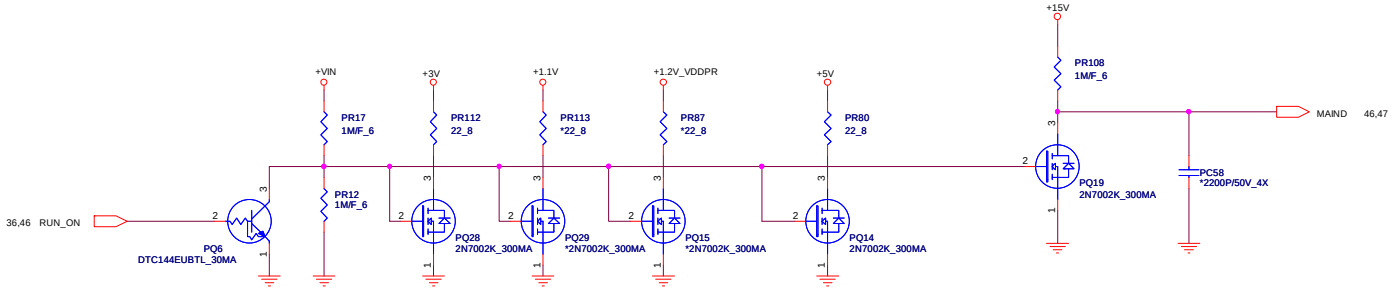


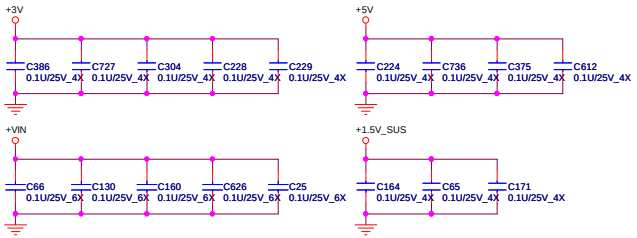


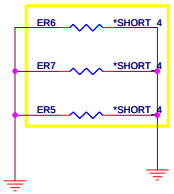


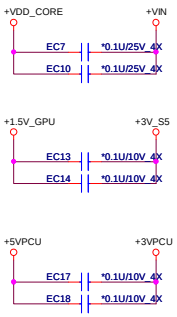


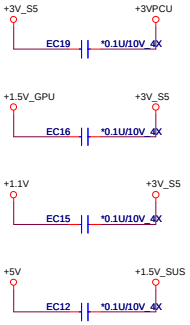
EMI

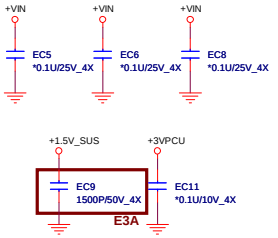
For EMI











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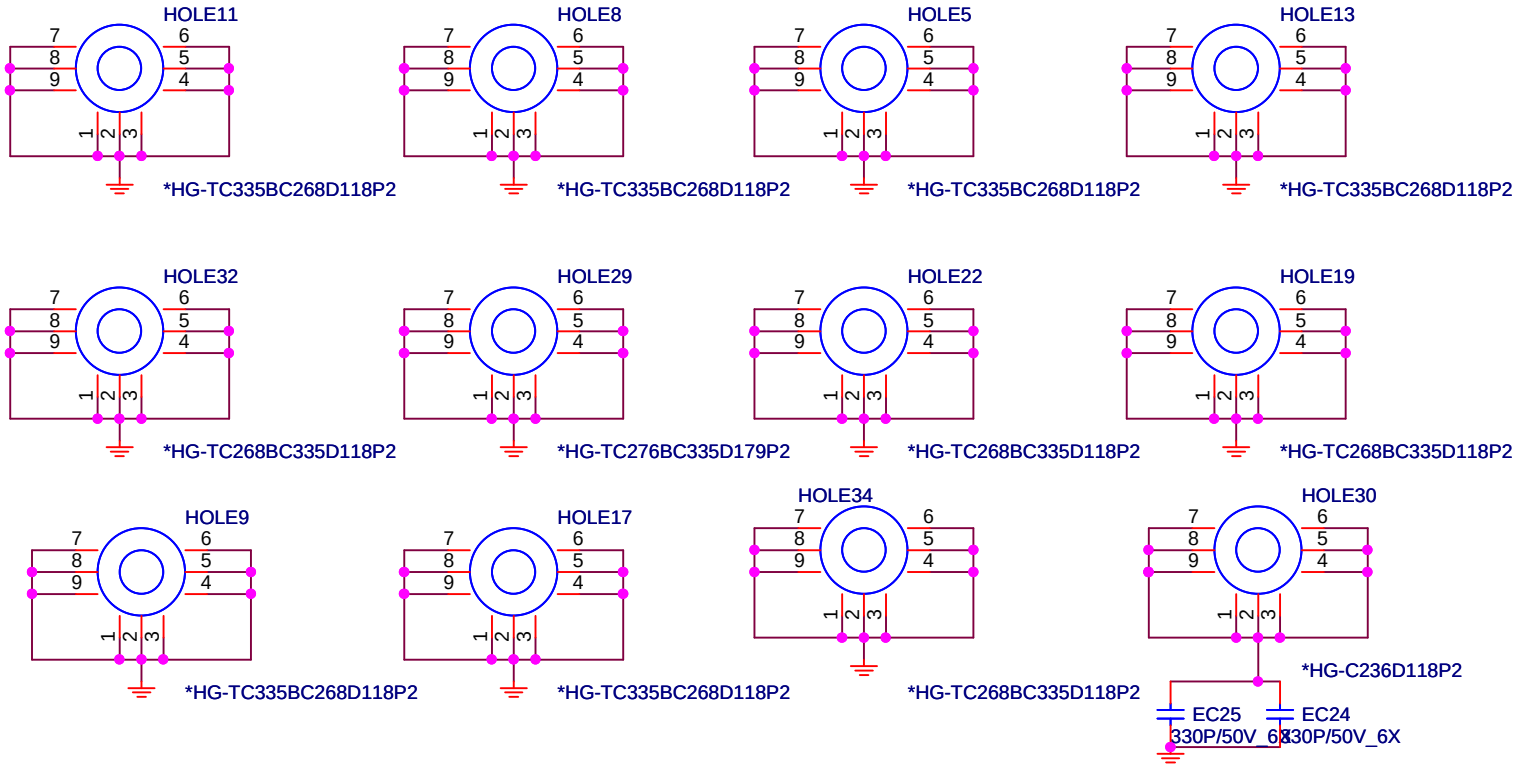

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