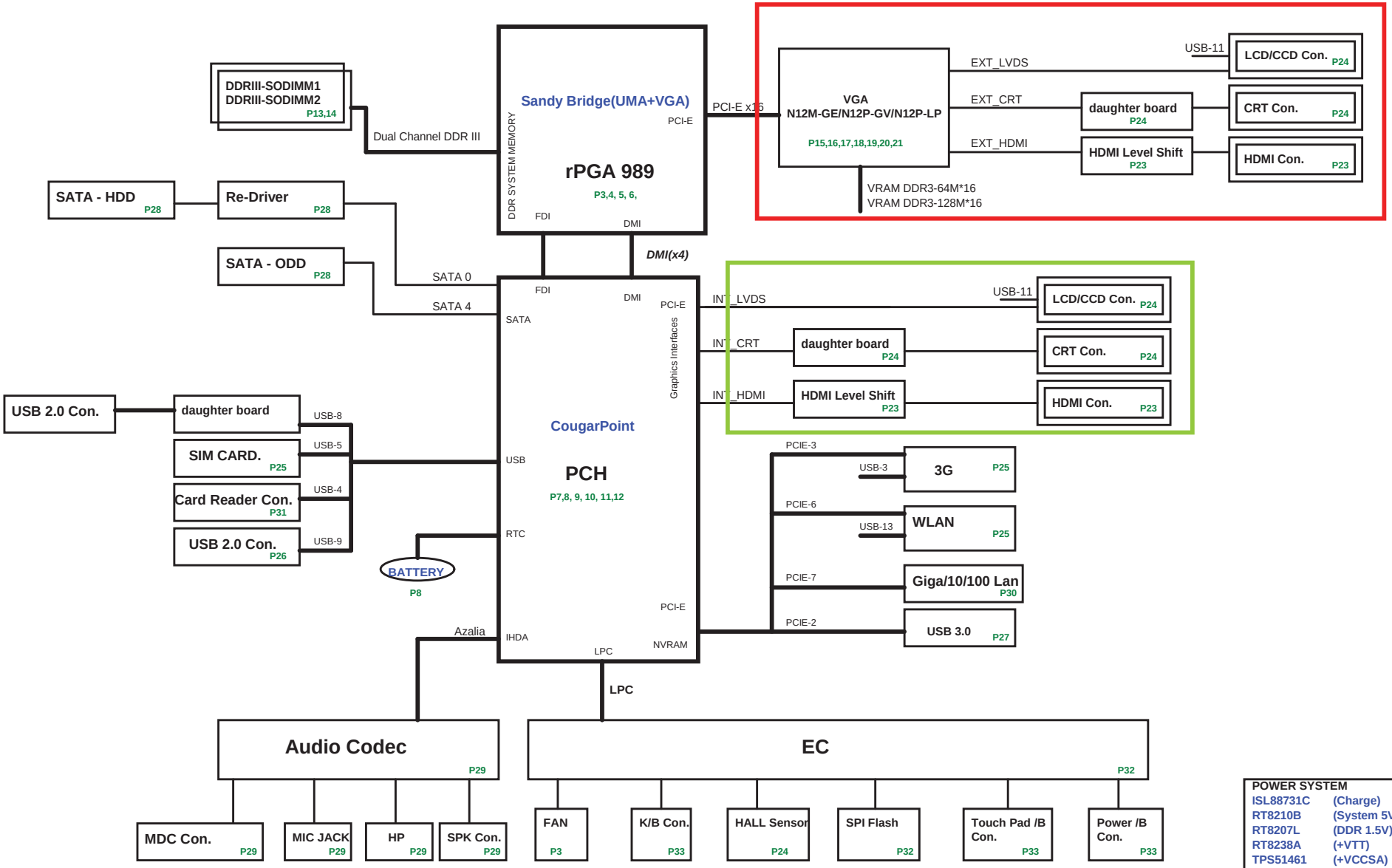
TE5 Block Diagram



POWER SYSTEM		
ISL88731C	(Charge)	P35
RT8210B	(System 5V/3V)	P36
RT8207L	(DDR 1.5V)	P37
RT8238A	(+VTT)	P38
TPS51461	(+VCCSA)	P39
ISL95835	(+VCC_CORE)	P40
G966A	(+1.8V)	P41
ISL95870A	(+GPU_CORE)	P42

Quanta Computer Inc.

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	Block Diagram	1A

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Table of Contents

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		MPWROK	S0

GND PLANE	PAGE
8769AGND	32
Audio_GND	29
Shield_GND	29
GND	ALL
ISL95870A_AGND	29

02

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	POWER STAGE AND BOI-FUNCTION	1A

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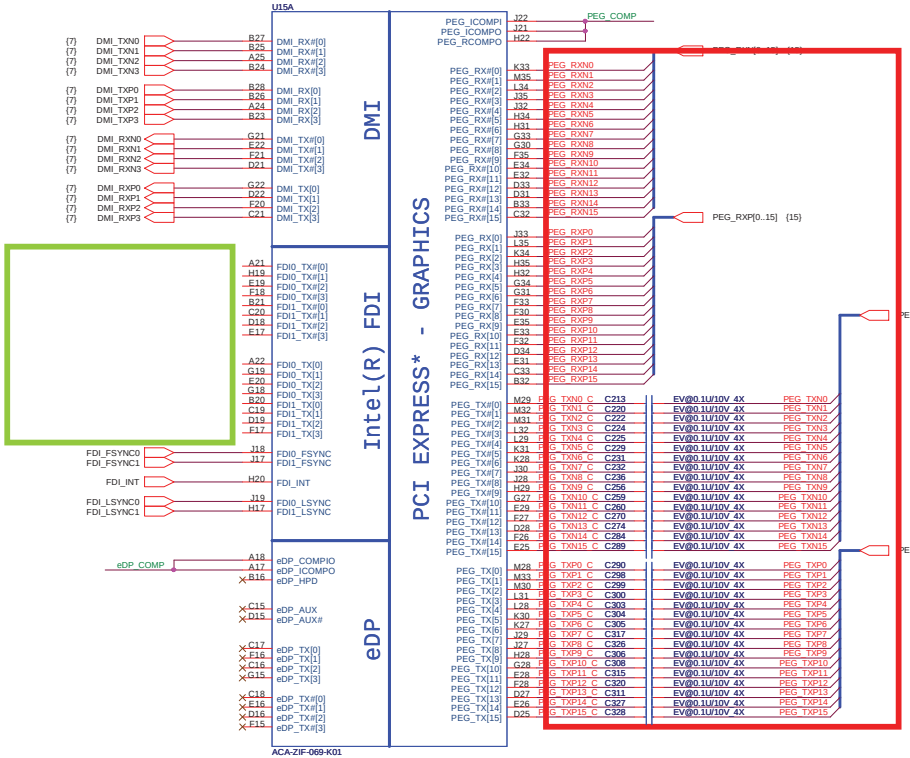
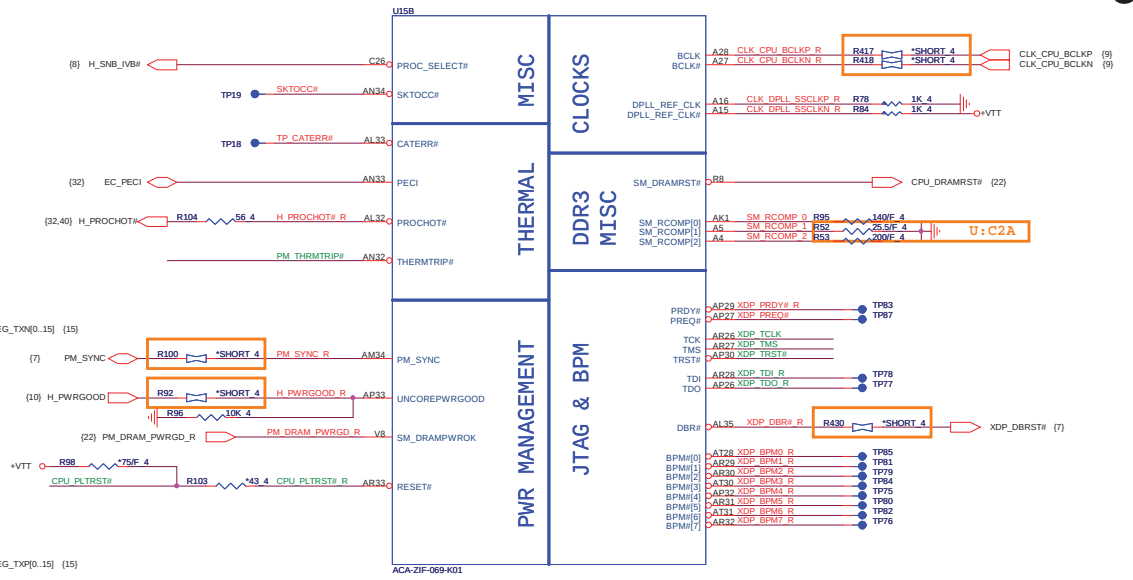
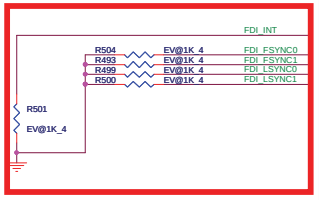
Sandy Bridge Processor (DMI,PEG,FDI) <CPU,VGA>



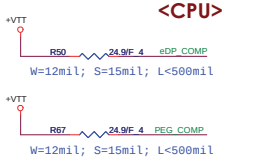
Sandy Bridge Processor (CLK,MISC,JTAG)<CPU>



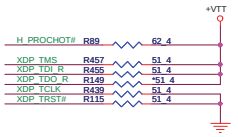
FDI Disabling (Discrete Only) <VGA>



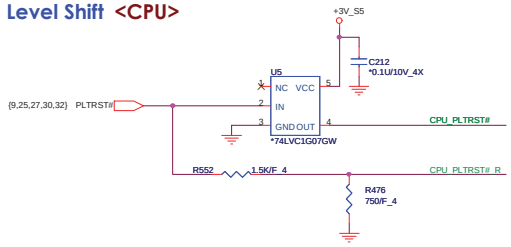
DP & PEG Compensation <CPU>



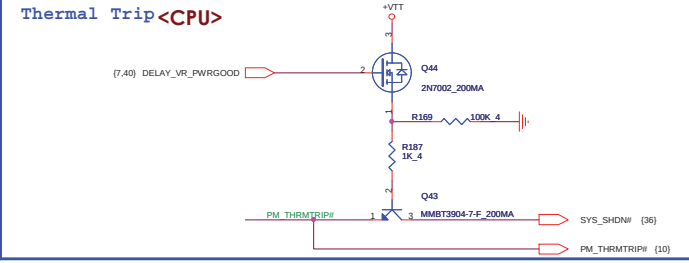
Processor pull-up <CPU>



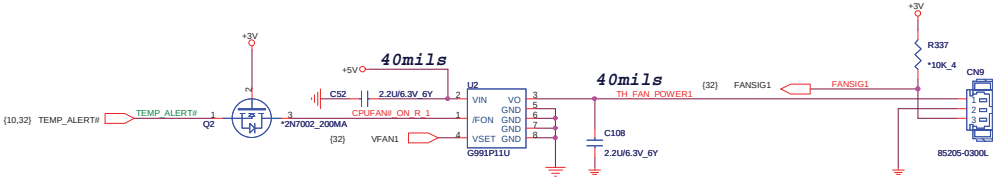
Level Shift <CPU>



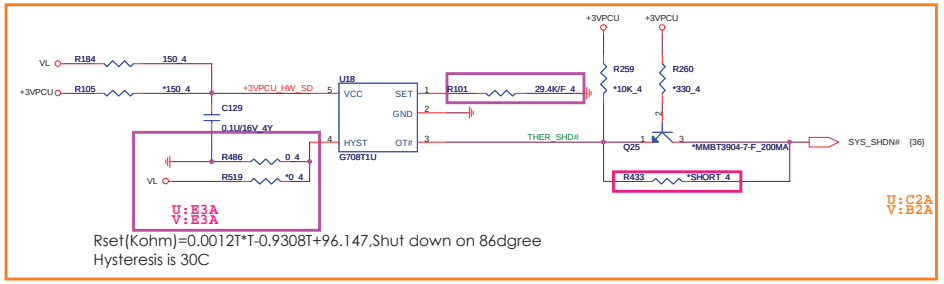
Thermal Trip <CPU>



FAN Control-->For one FAN solution <THC/THV>



CPU Thermal sensor / MB Local TEMP <THC>



Rset(Kohm)=0.0012T*T-0.9308T+96.147,Shut down on 86dgree
Hysteresis is 30C

Quanta Computer Inc.	
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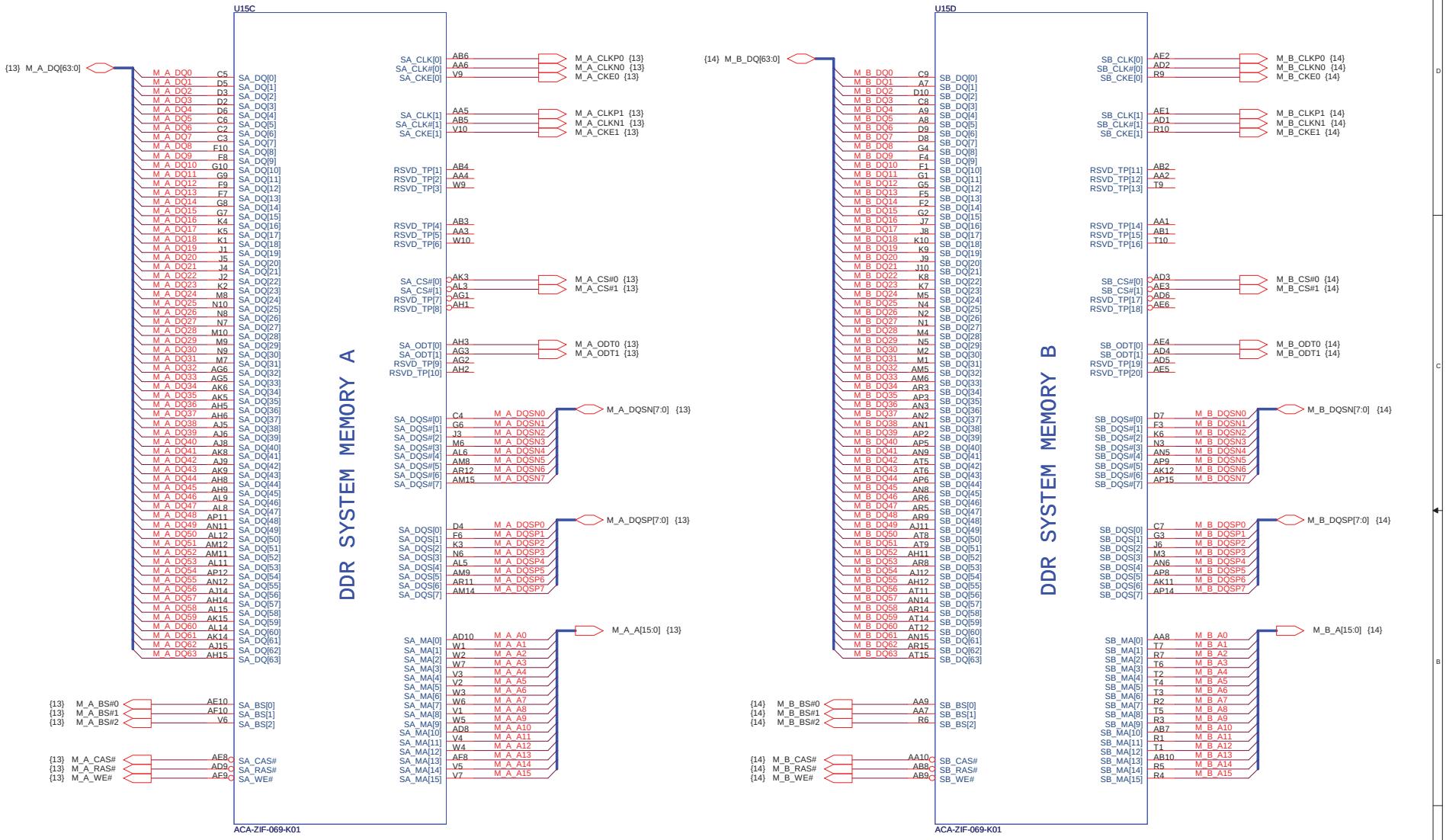
Sandy Bridge Processor (DDR3)



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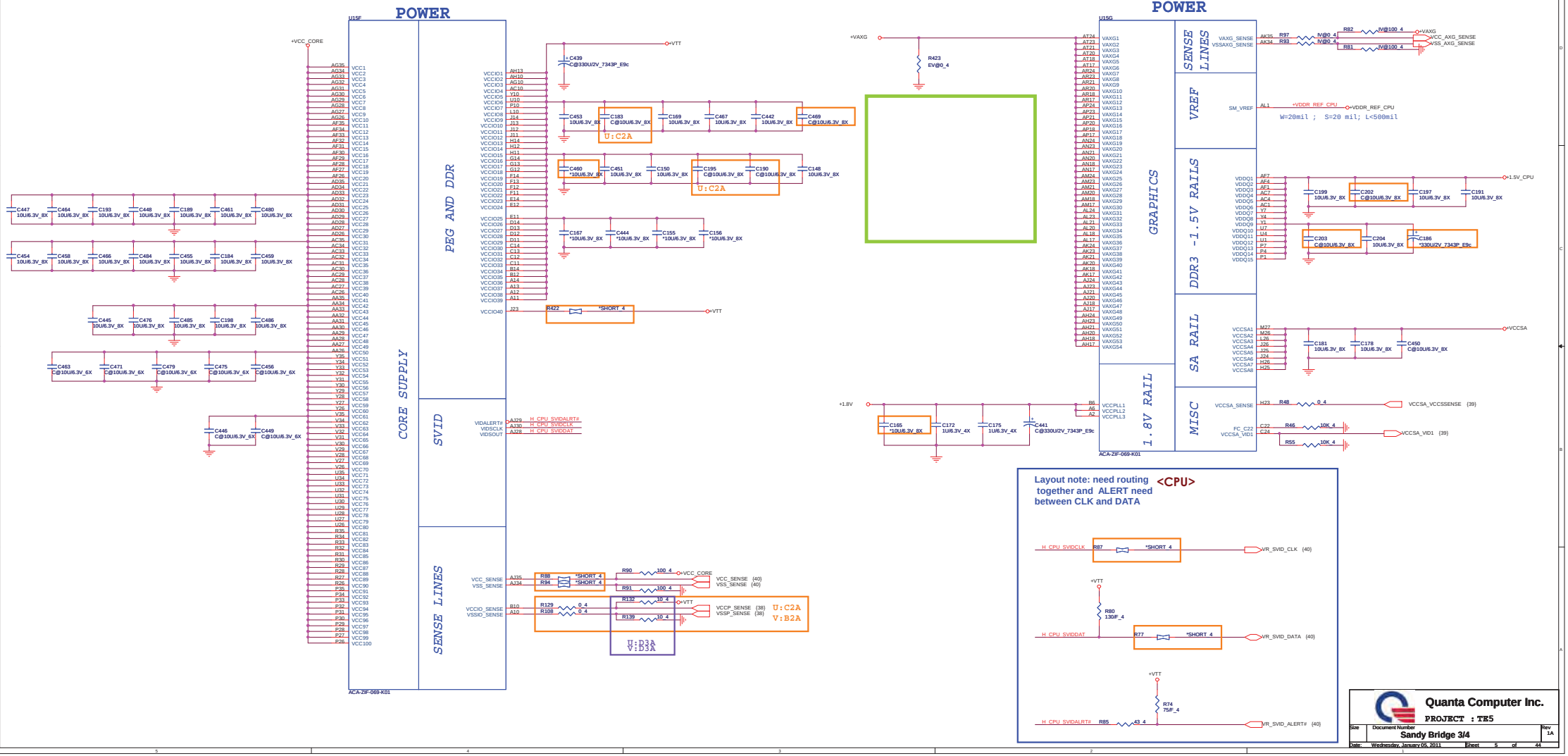
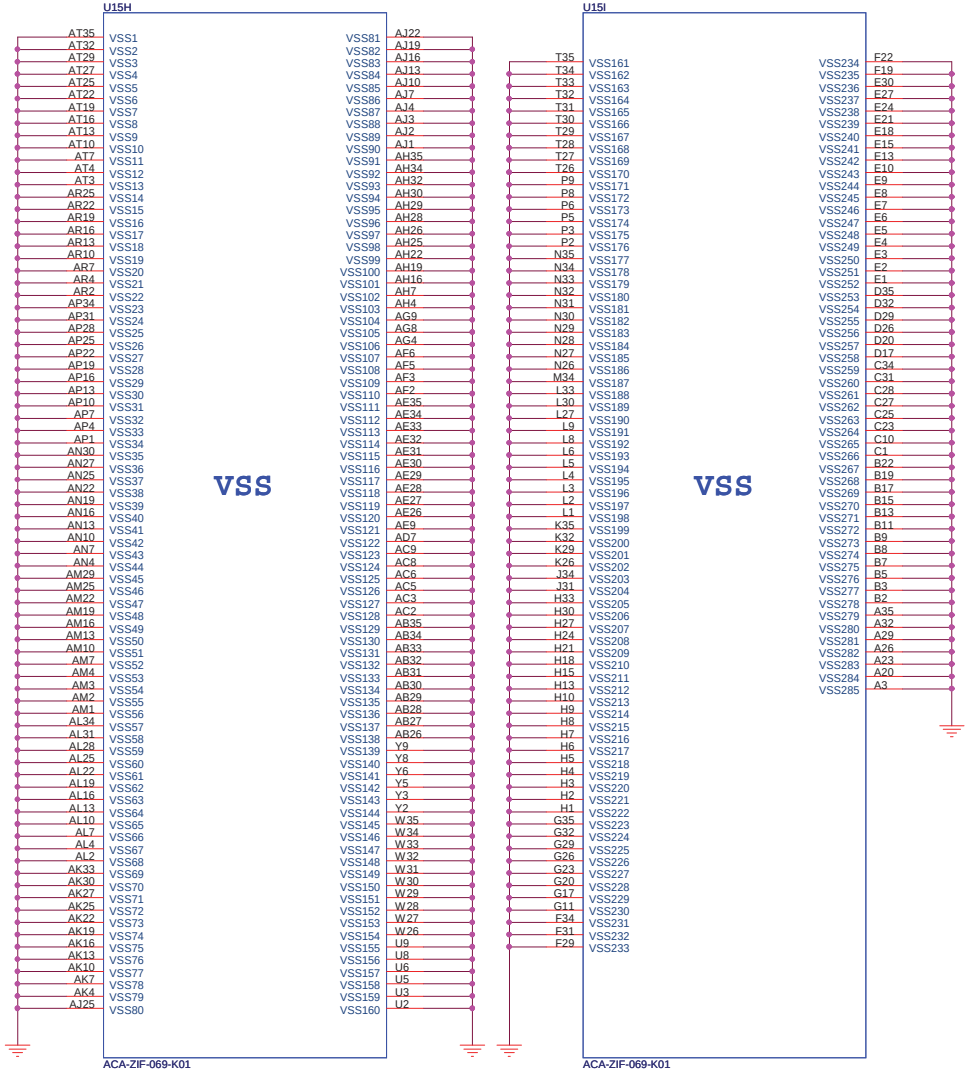
Sandy Bridge Processor (POWER)<CPU>

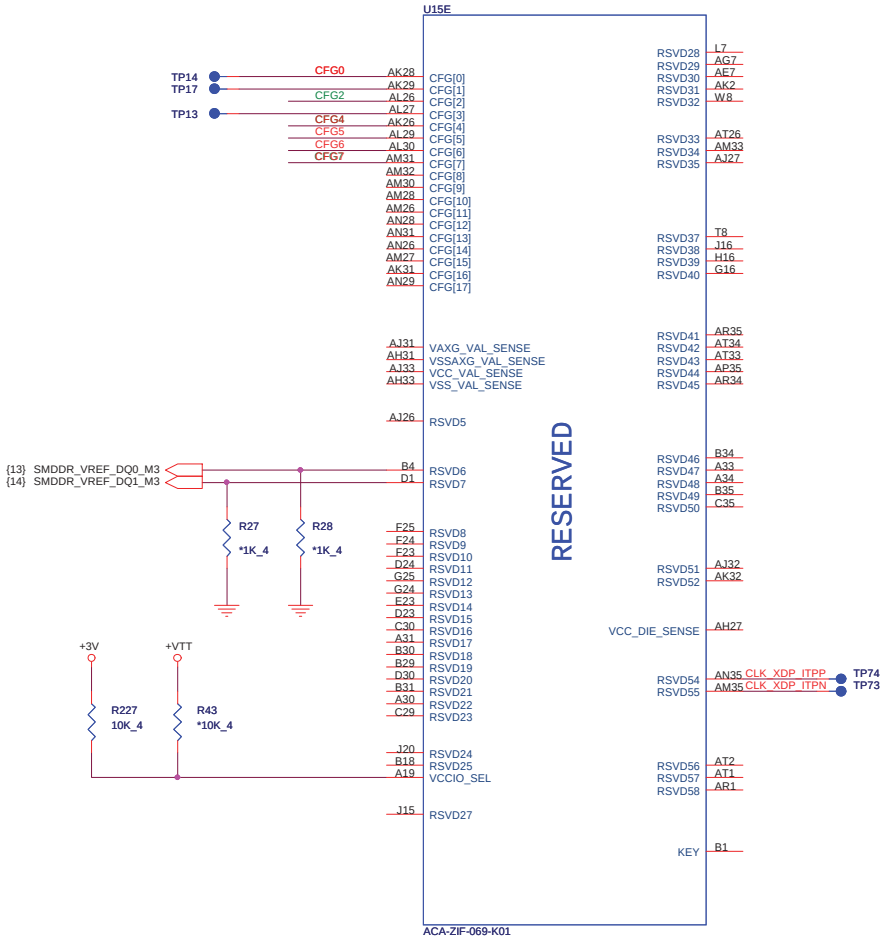
Sandy Bridge Processor (GRAPHIC POWER)<CPU,UGA>



Sandy Bridge Processor (GND)



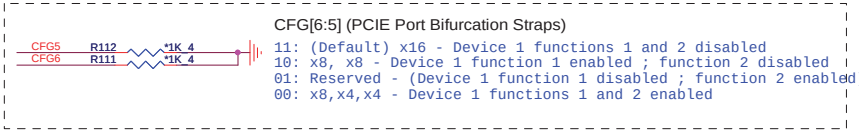
Sandy Bridge Processor (RESERVED, CFG)<CPU>



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



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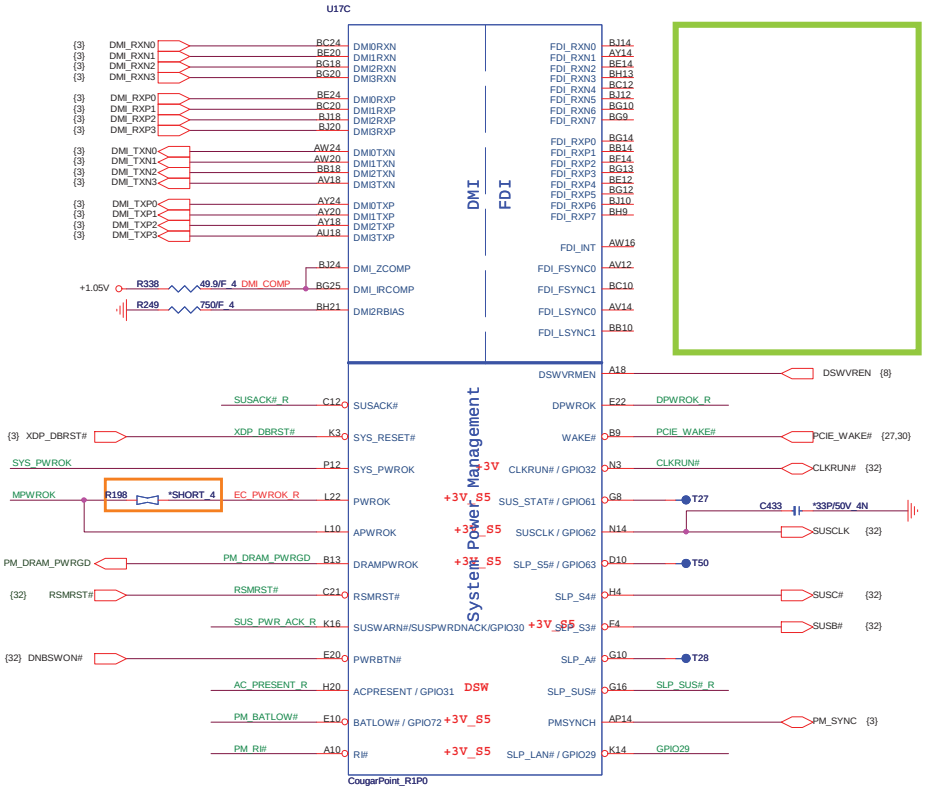
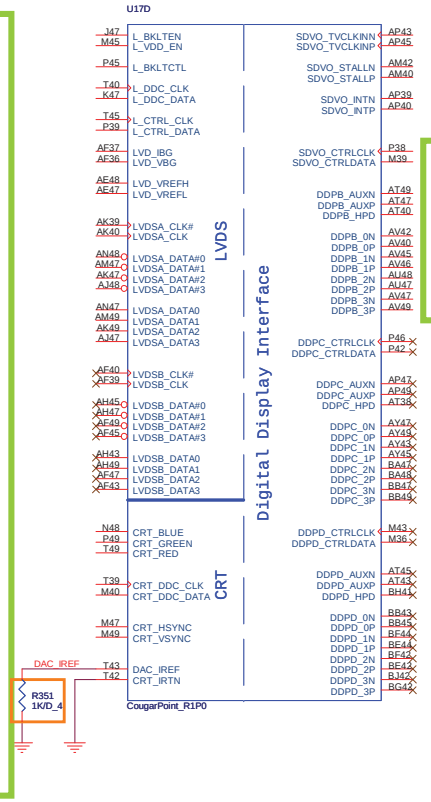
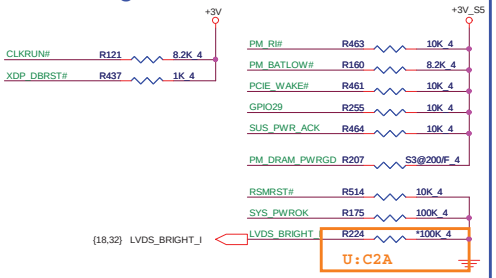
Cougar Point (DMI,FDI,PM)<CLG>



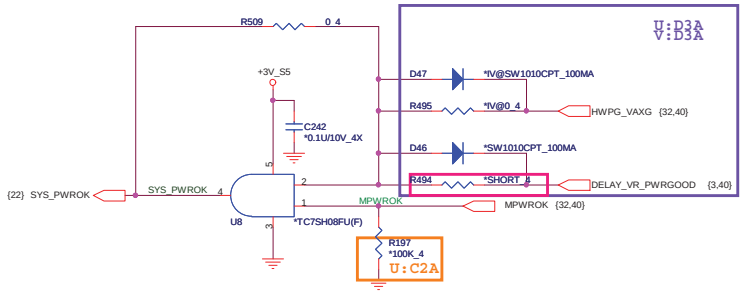
Cougar Point (LVDS,DDI)<CLG/UGA/HMG>



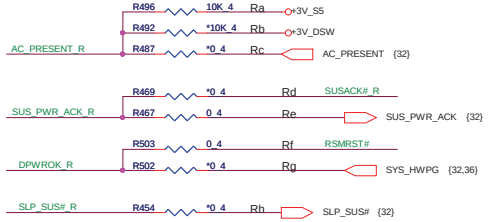
PCH Pull-high/low<CLG>



System PWR_OK <CLG>



Deep Sx <CLG>



Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

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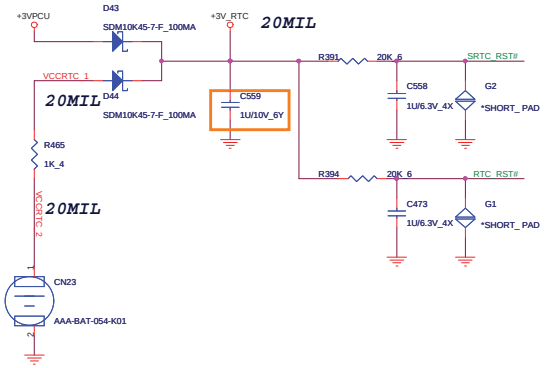
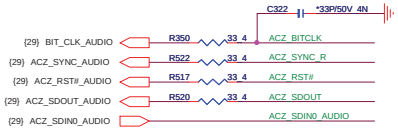
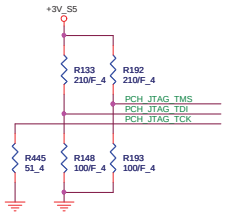
RTC Circuitry(RTC)



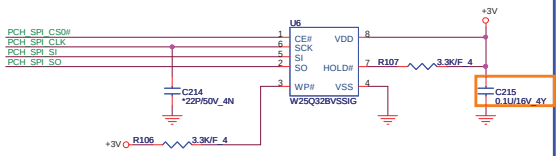
HDA Bus(CLG)



PCH JTAG Debug (CLG)

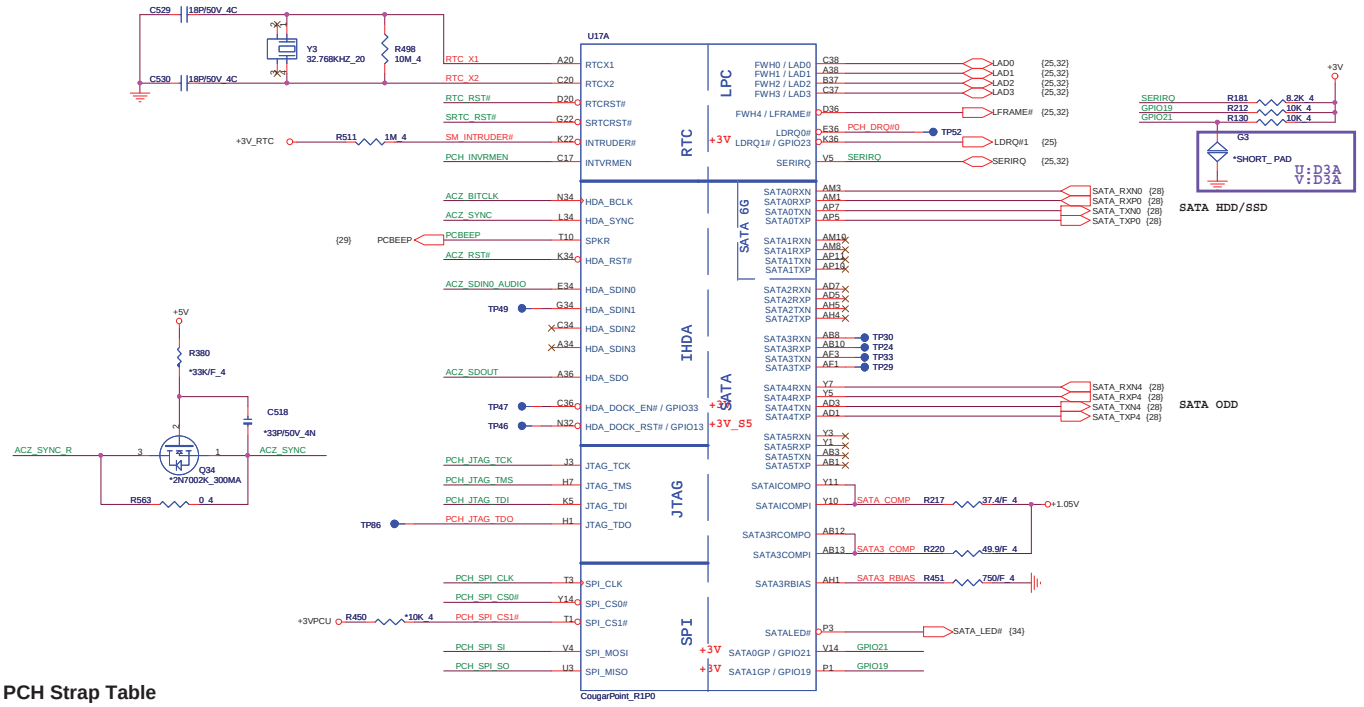


PCH Dual SPI (CLG)



PCH2 (CLG)

Cougar Point (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R116 *1K_4 PCBEEP
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R530 *1K_4 PCI_GNT3# {9}
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R497 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GPIO19 / Boot Location: 1 / 1 / SPI ★; 0 / 0 / LPC	R539 *1K_4 GNT1# {9} R449 *1K_4 GPIO19
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	**RSMRST**	0 = Override 1 = Default (weak pull-up 20K)	+3V R521 *1K_4 ACZ_SDOUT ACZ_SDOUT {32}
DF_TVS	**DMI/FDI Termination voltage**	**PWROK**	**0 = Set to Vss** **1 = Set to Vcc (weak pull-down 20K)**	R453 2.2K_4 +1.8V R452 1K_4 DF_TVS {10} H_SNB_IVB# {3}
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	+3V_S5 R206 *10K_4 R195 *1K_4 PLL_ODVR_EN {10}
HDA_SYNC	**On-Die PLL VR Voltage Select**	**RSMRST**	**0 = Support by 1.8V (weak pull-down)** **1 = Support by 1.5V**	+3V_S5 R525 1K_4 ACZ_SYNC
INIT3_3V#	**Reserved**	PWROK	1 = Default (weak pull-up 20K)	**Should not pull low. leave as No Connect**
GNT2#/ GPIO53	**ESI Strap (Server Only)**	PWROK	1 = Default. Should not be pulled low for desktop and mobile	**Should not pull low for desktop and mobile**
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality	+3V_S5 R313 1K_4 GPIO15 {10}
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
SATA3GP/ GPIO37	**Reserved**	PWROK	0 = Default	**Should not be pulled high when strap is sampled**
SATA2GP/ GPIO36	**Reserved**	PWROK	0 = Default	**Should not be pulled high when strap is sampled**
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	DSWVREN {7} +3V_RTC R489 330K_4 R490 *330K_4

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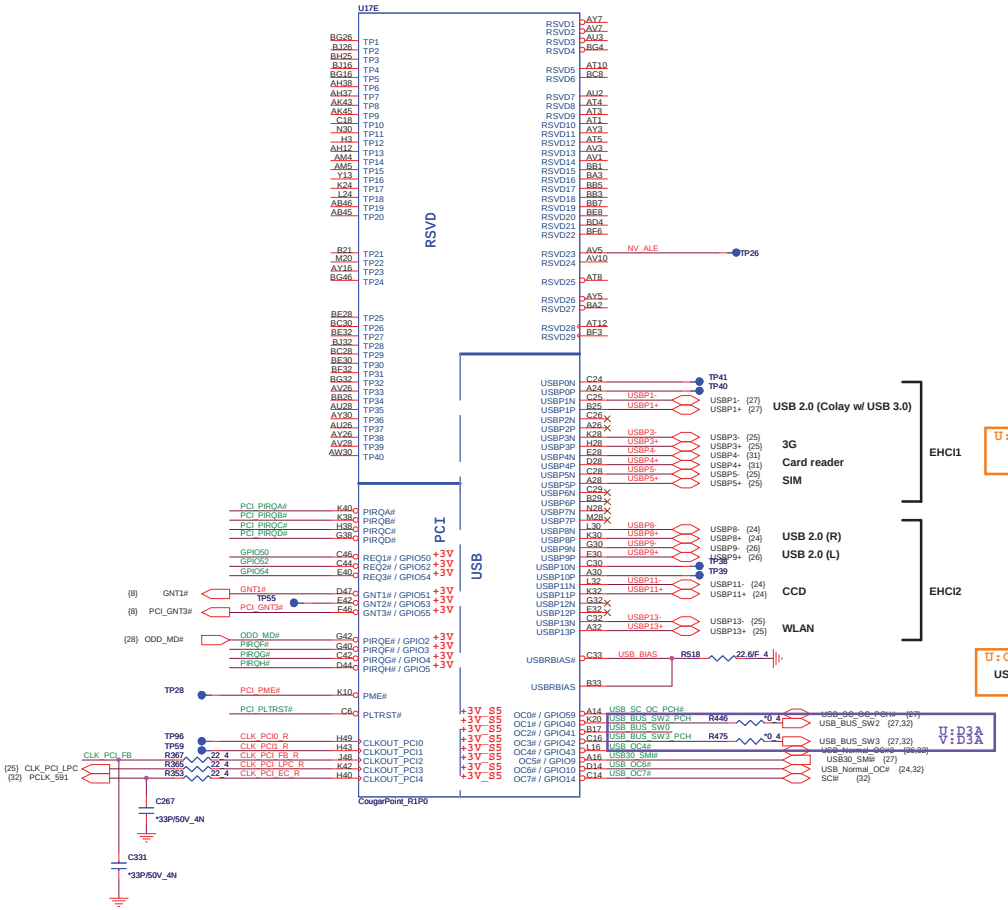
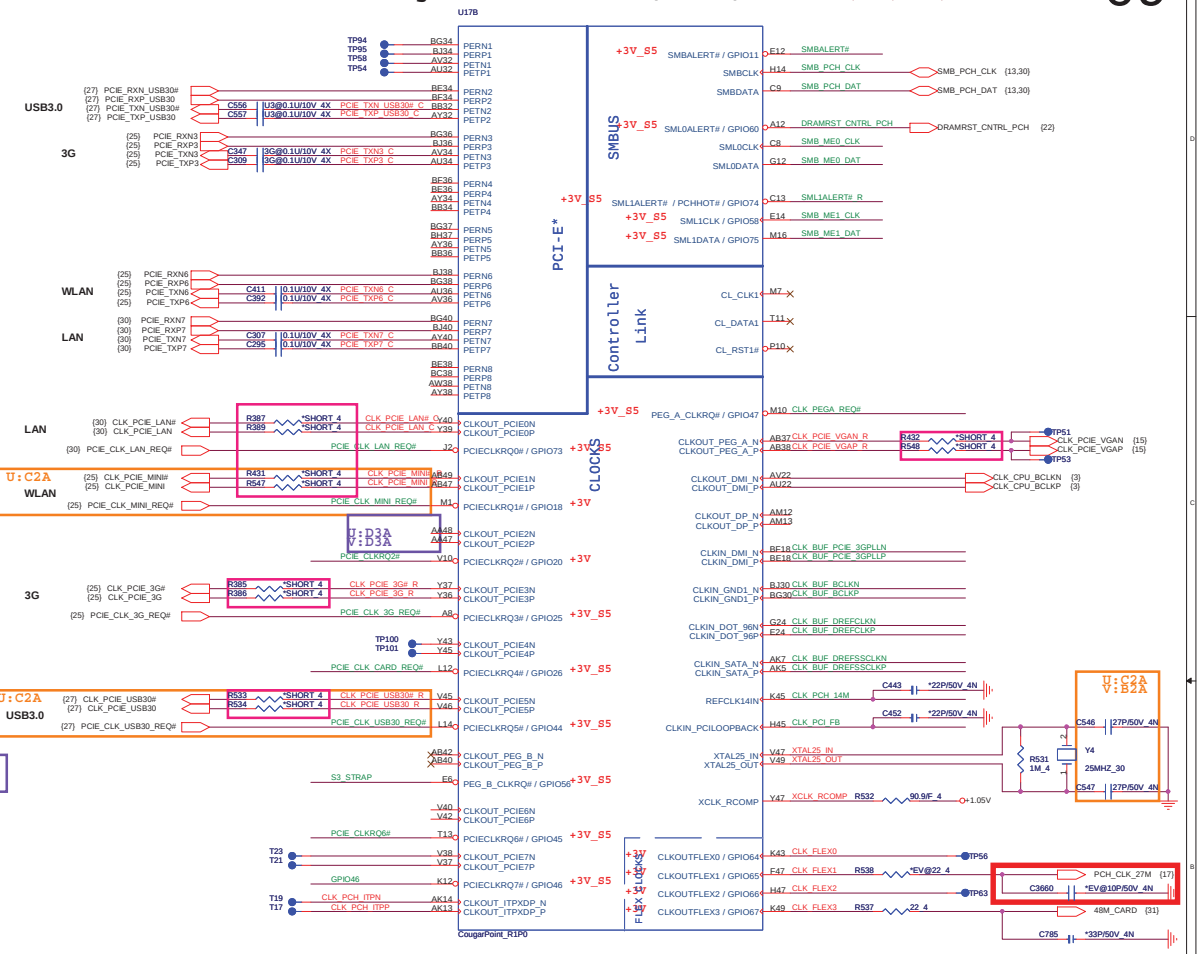
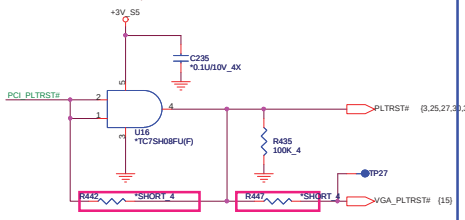
Cougar Point-M (PCI,USB,NVRAM) <CLG>



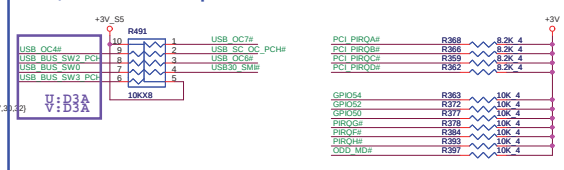
Cougar Point-M (PCI-E,SMBUS,CLK) <CLG,U3B,VGA,MNG>



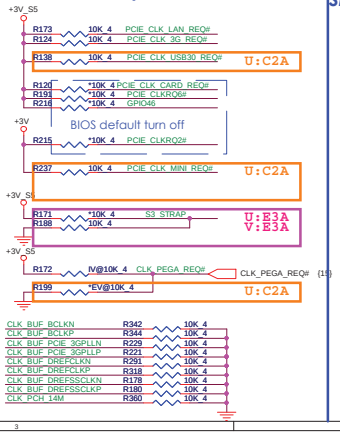
PLTRST# <CLG,VGA>



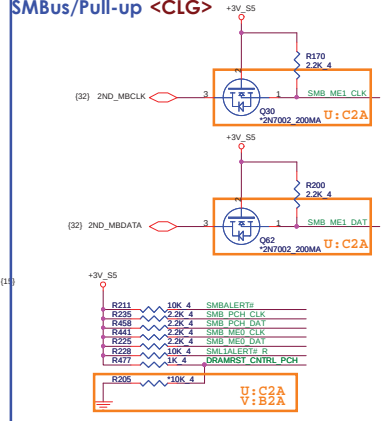
PCI/USBOC# Pull-up <CLG>



CLK_REQ/Strap Pin <CLG>



SMBus/Pull-up <CLG>



	33MHz	27MHz	48/24MHz	14.318MHz	25MHz
CLK_FLEX0	●	●	●	●	
CLK_FLEX1		●	●	●	
CLK_FLEX2	●	●	●	●	●
CLK_FLEX3		●	●	●	

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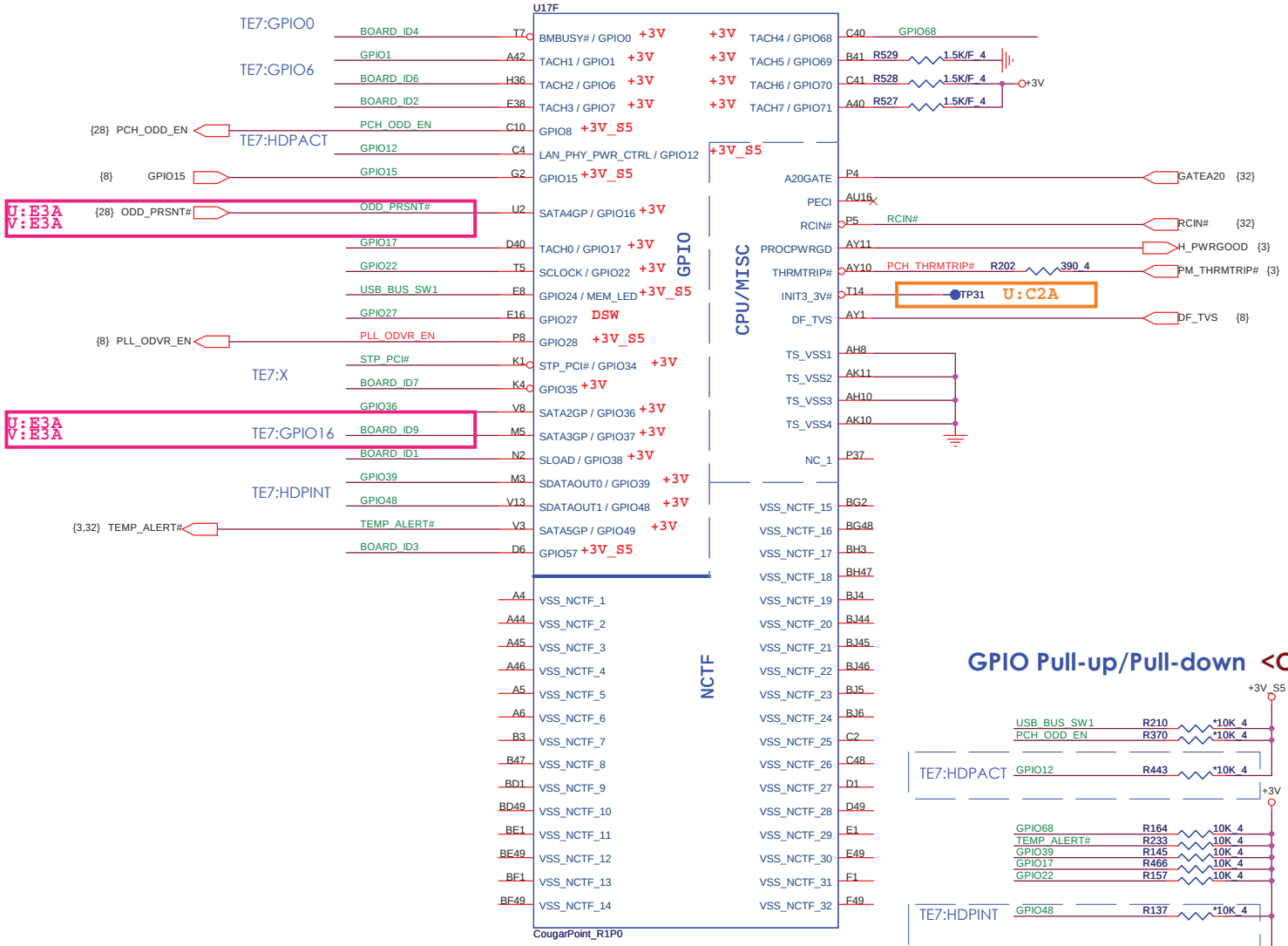
Cougar Point (GPIO,VSS_NCTF,RSVD) <CLG>

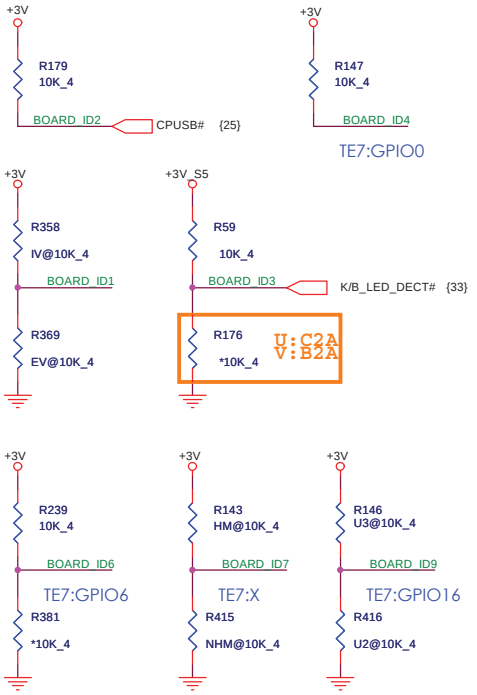


GPIO Pull-up/Pull-down <CLG>

BOARD ID SETTING <CLG>

Board ID	ID1	ID2	ID3	ID4	ID6	ID7	ID9	GPIO1
UMA SKU VGA SKU	H L							
W/O 3G W/ 3G		H L						
W/O LED KB W/ LED KB			H L					
14" 15"				H L				
W/ MDC W/O MDC					H L			
W/ HDMI W/O HDMI						H L		
USB3.0 USB2.0							H L	
W/ G-sensor W/O G-sensor								H L

U:C2A



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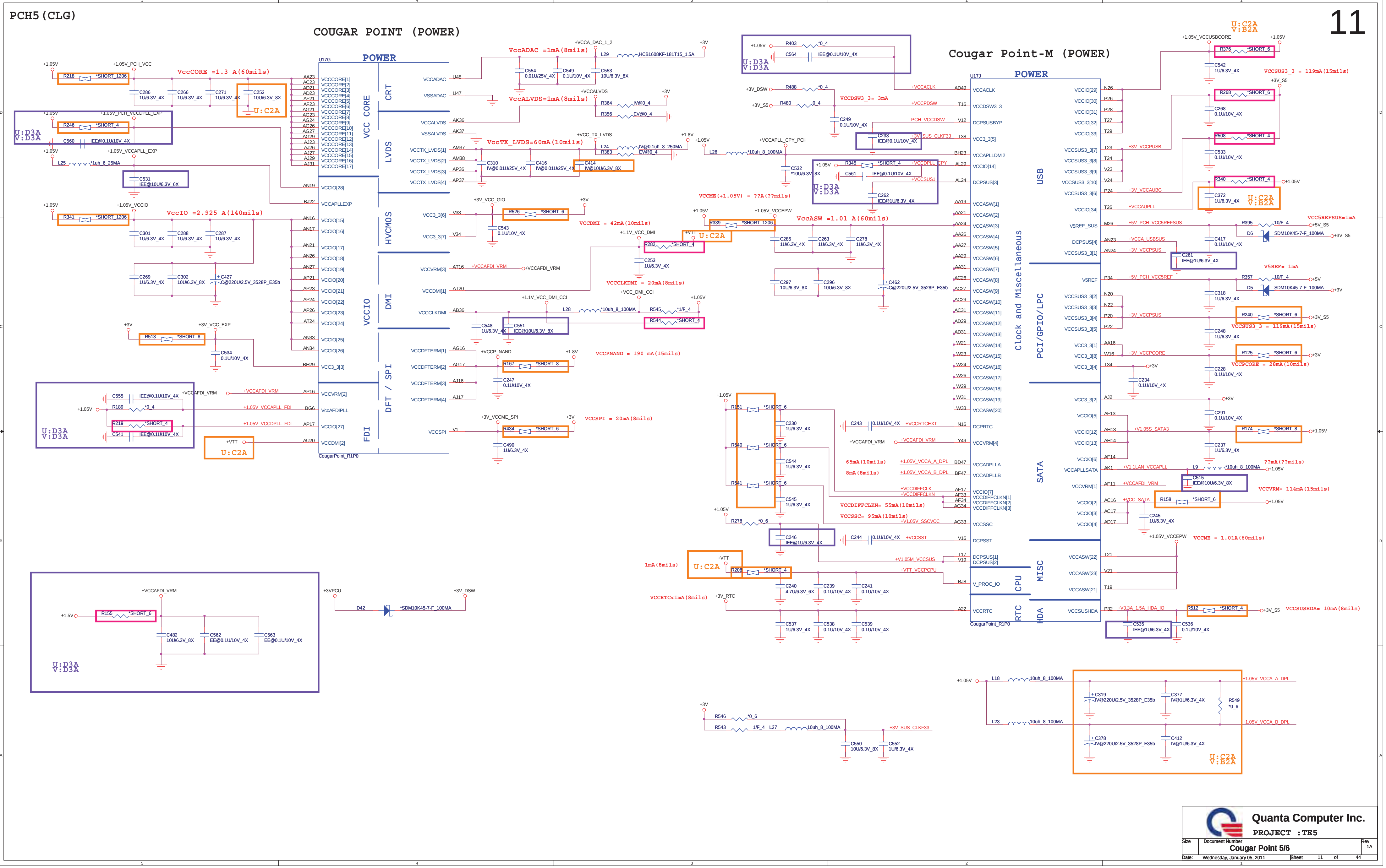

PCH5 (CLG)
COUGAR POINT (POWER)
Cougar Point-M (POWER)
11
POWER
VCC CORE
CRT
LVDS
HVCMOS
VCCIO
DMI
DFT / SPI
FDI
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
MISC
RTC
HDA
VccCORE =1.3 A(60mils)
VccIO =2.925 A(140mils)
VccADAC =1mA(8mils)
VccALVDS=1mA(8mils)
VccTX_LVDS=60mA(10mils)
VCCDMI = 42mA(10mils)
VCCCLKDMI = 20mA(8mils)
VCCPNAND = 190 mA(15mils)
VCCSPI = 20mA(8mils)
VCCDSW3_3= 3mA
VCCME(+1.05V) = ??A(??mils)
VccASW =1.01 A(60mils)
VCCSUS3_3 = 119mA(15mils)
VCC5REFSUS=1mA
V5REF= 1mA
VCCPCORE = 28mA(10mils)
77mA(??mils)
VCCVRM= 114mA(15mils)
VCCME = 1.01A(60mils)
VCCSUSHDA= 10mA(8mils)
VCCDIFFCLKN= 55mA(10mils)
VCCSSC= 95mA(10mils)
65mA(10mils)
8mA(8mils)
1mA(8mils)
VCCRTC<1mA(8mils)
U:C2A
U:D3A V:D3A
U:C2A V:B2A
CougarPoint_R1P0
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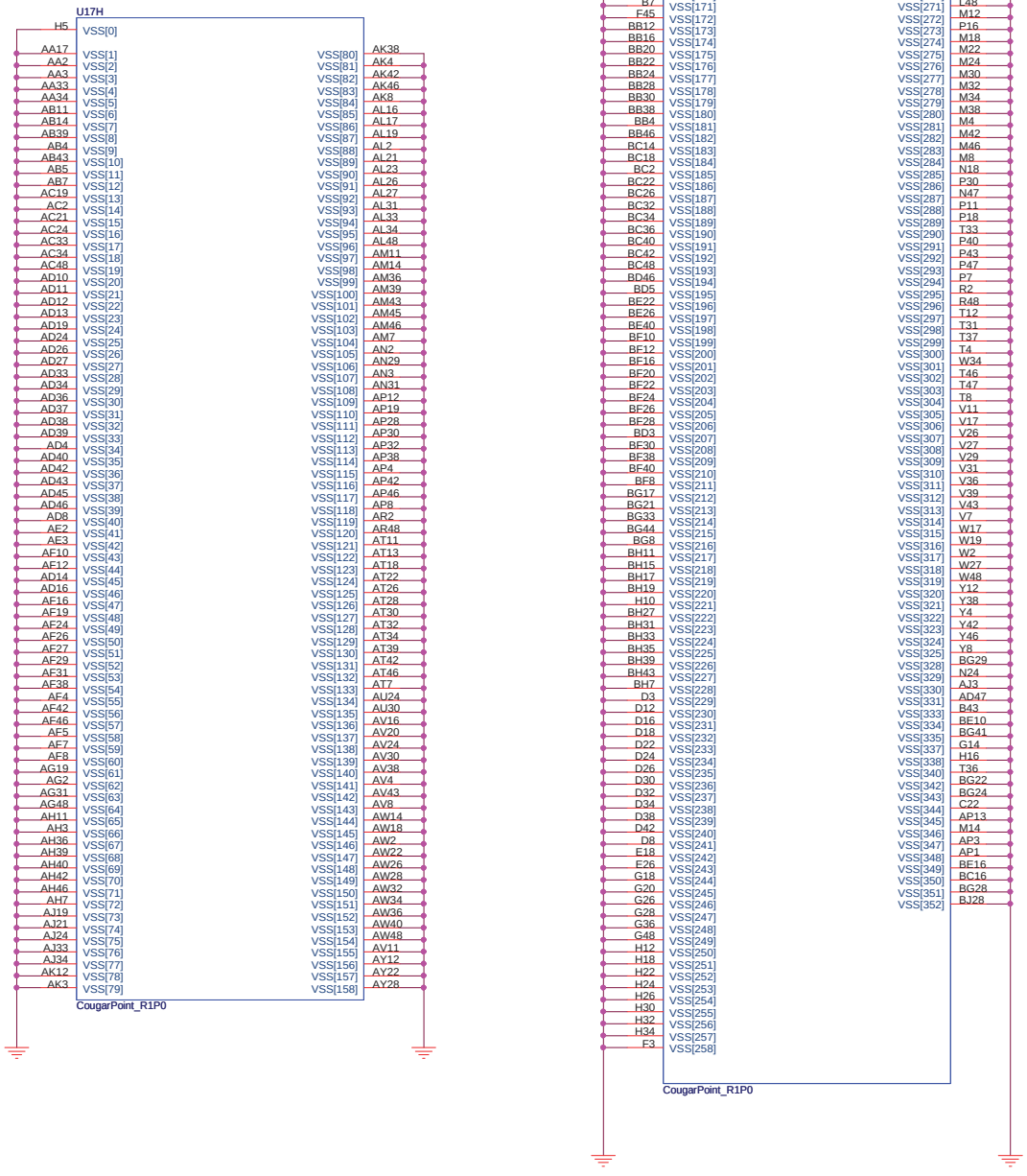
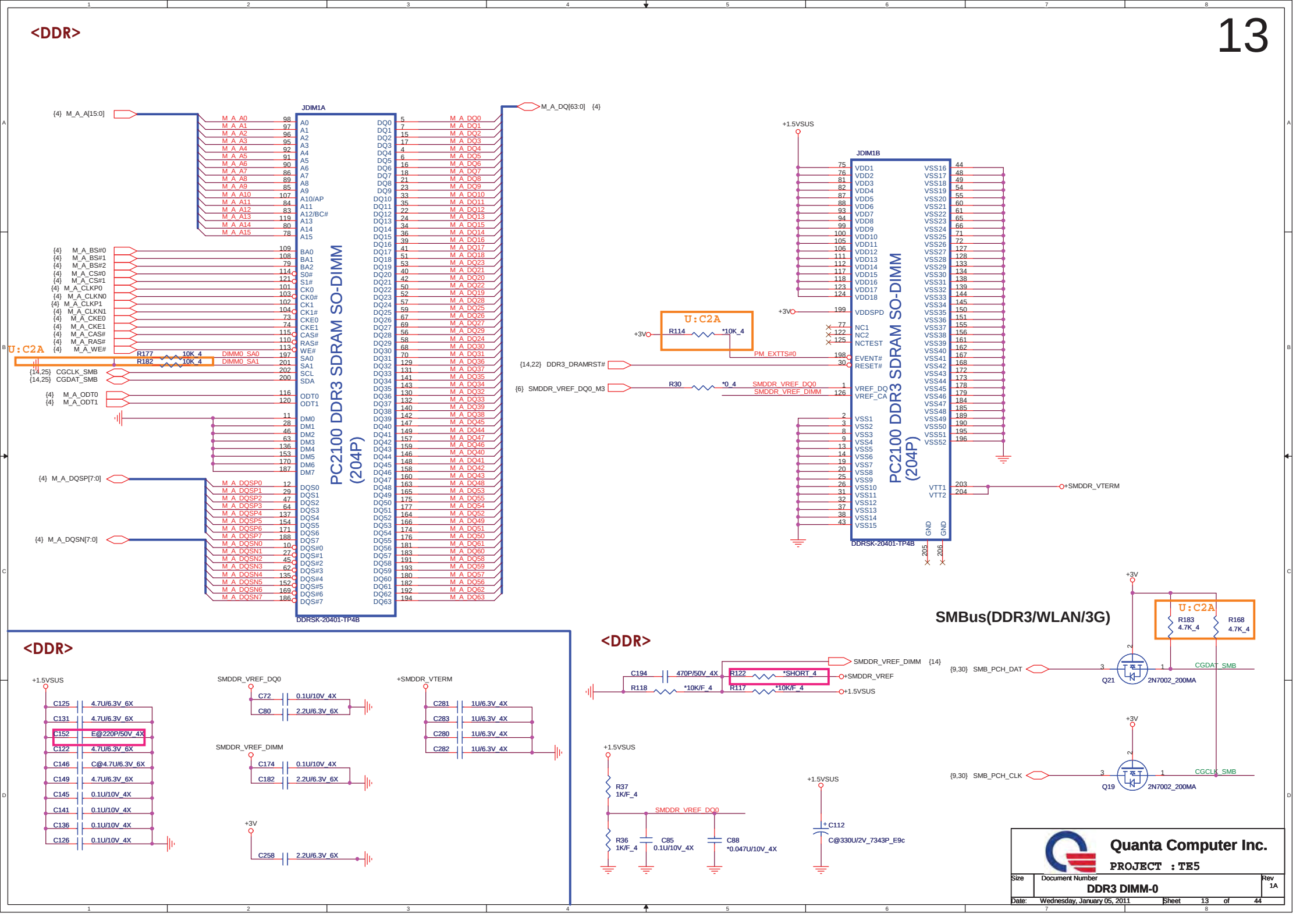
IBEX PEAK-M (GND)

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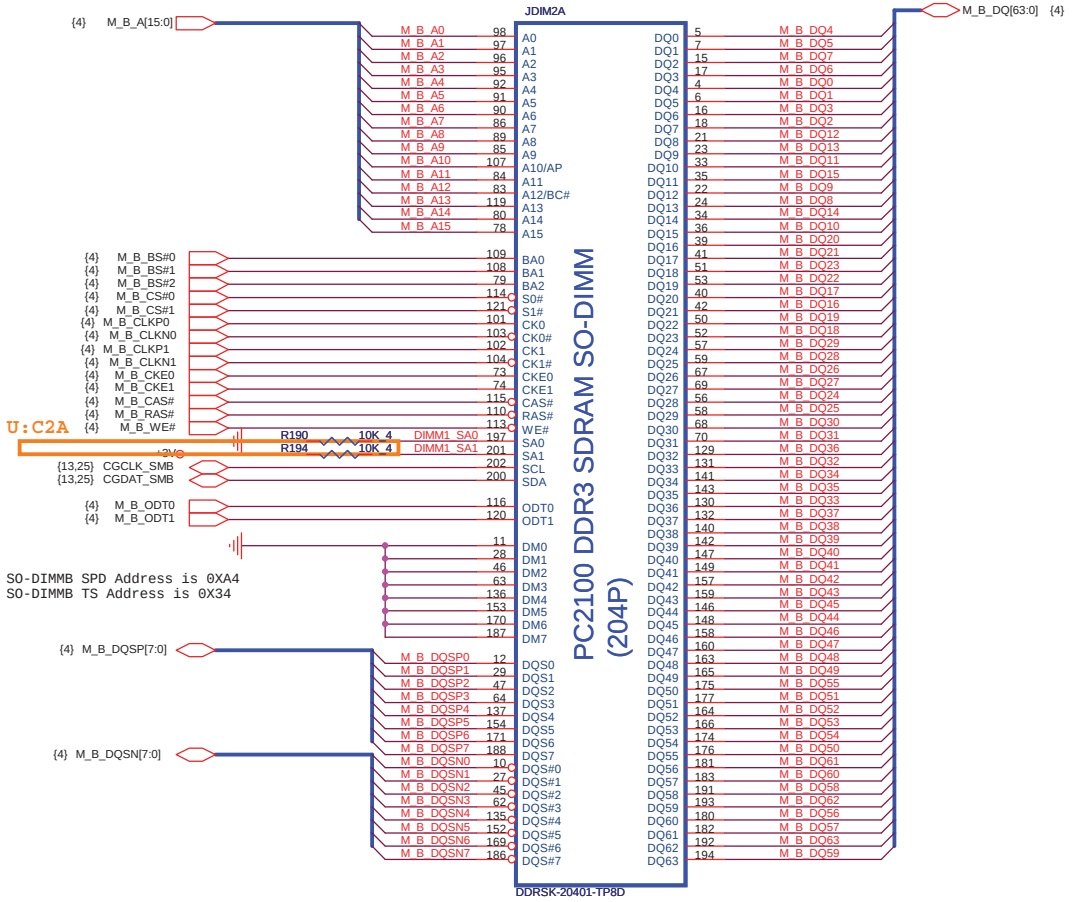
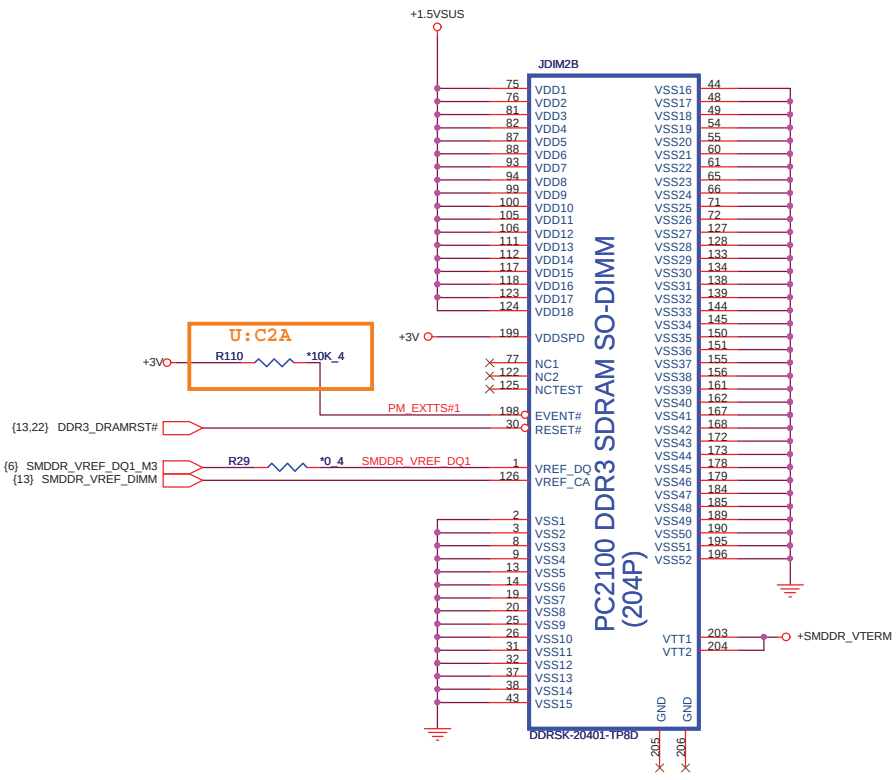
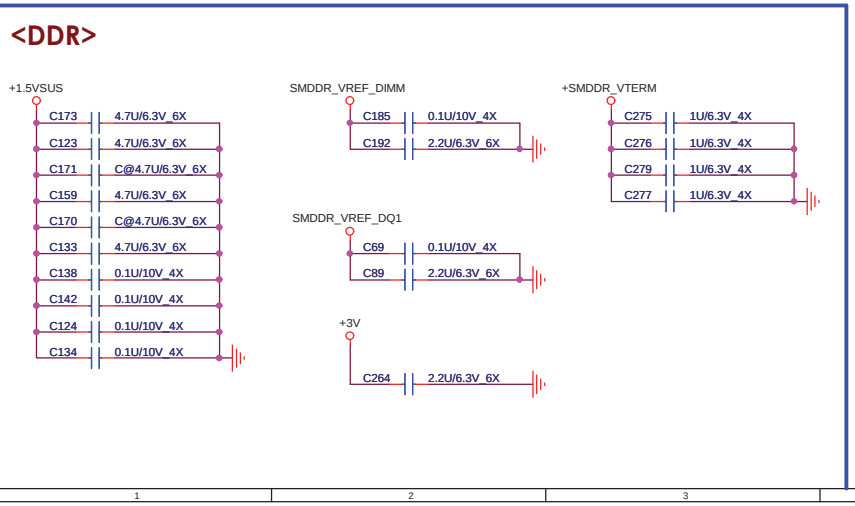
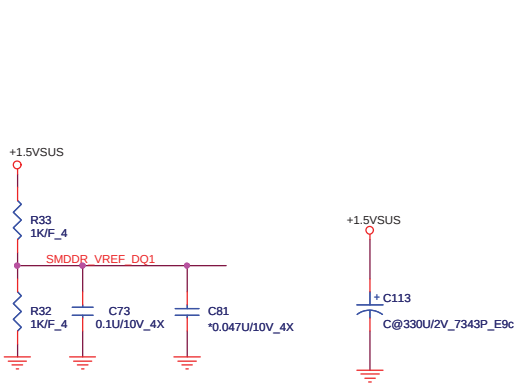
JDIM1A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDRSK-20401-TP4B
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDRSK-20401-TP4B
U:C2A
SMBus(DDR3/WLAN/3G)
Quanta Computer Inc.
PROJECT : TE5
DDR3 DIMM-0
Wednesday, January 05, 2011









Quanta Computer Inc.

PROJECT : TE5

Size	Document Number	Rev
	DDR3 DIMM-1	1A

Date: Wednesday, January 05, 2011 Sheet 14 of 44

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

~ 500mA

1600mA

GPU3500A
fcbga973-nvidia-n11p-es-a1
COMMON

PCI EXPRESS

V:B2A

V:C2A

12~16 mils width
110mA

12~16 mils width

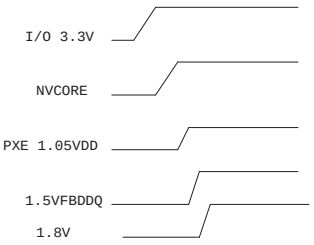
V:D3A

VGA HOLE
HOLE27
HOLE28
HOLE26
*H-C217D142P2
*H-C217D142P2
*H-C217D142P2

Q3503
EV@2N7002_200MA

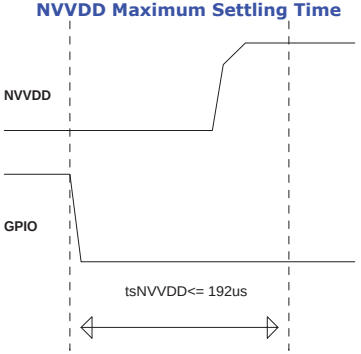
15-V

power up sequence

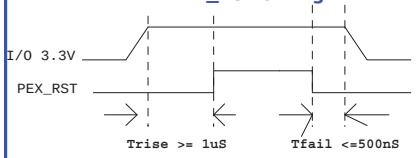


NB9M: VGACORE +0.90V (Normal) , +1.05V

NVVDD Maximum Settling Time



PEX_RST timing



Quanta Computer Inc.
PROJECT : TE5

Size	Document Number	Rev
	N11x-Fermi PCIE	1A
Date: Wednesday, January 05, 2011	Sheet 15 of 44	

GPU3500B
fcbga973-nvidia-n11p-es-a1
COMMON

GPU3500C
fcbga973-nvidia-n11p-es-a1
COMMON

MEMORY I/F A

MEMORY I/F C

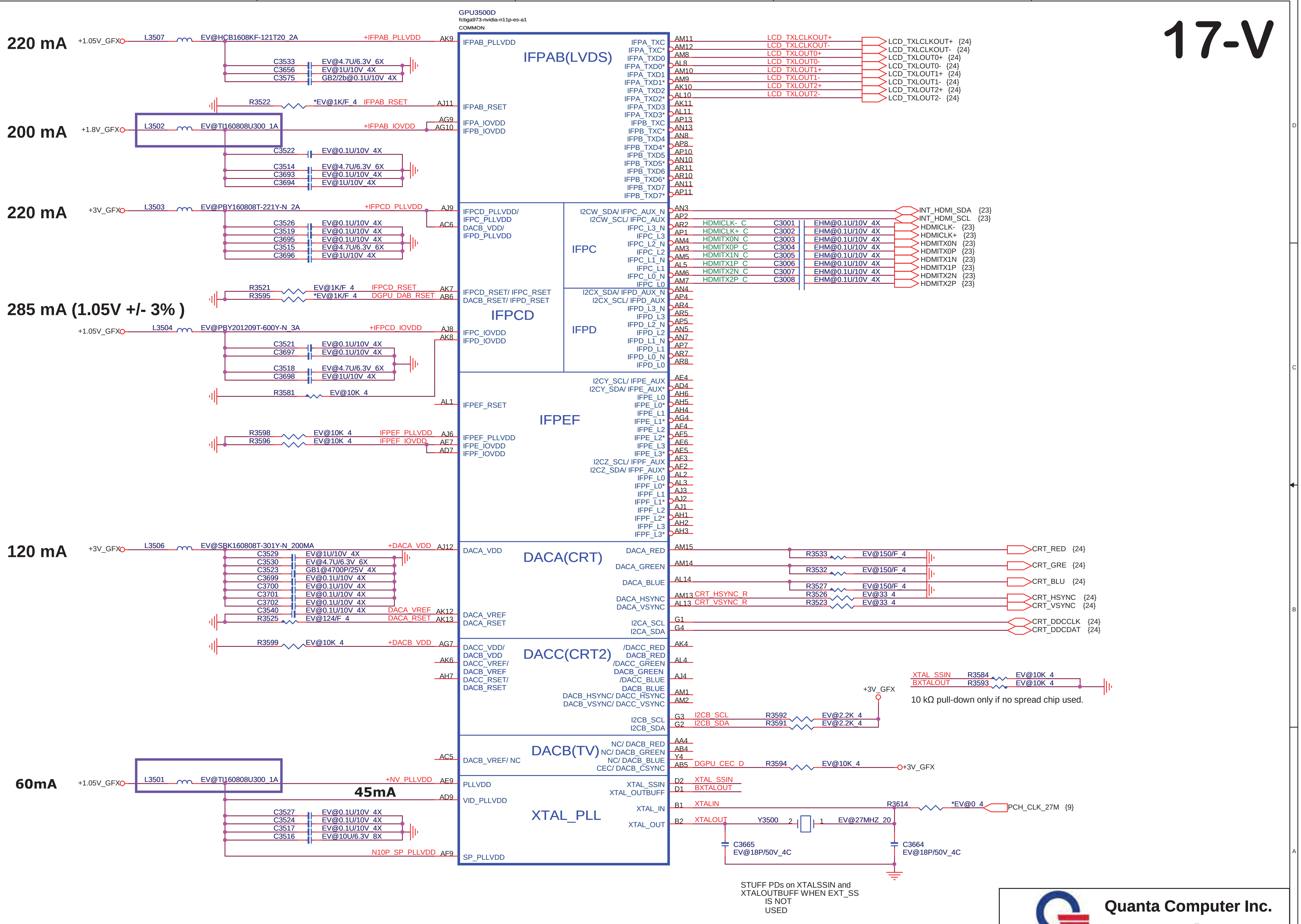
15mils width

15mils width

V:B2A

Quanta Computer Inc.
PROJECT : TE5

Size	Document Number	Rev
	N11x-Fermi (MEM I/F)	1A
Date: Wednesday, January 05, 2011	Sheet 16 of 44	

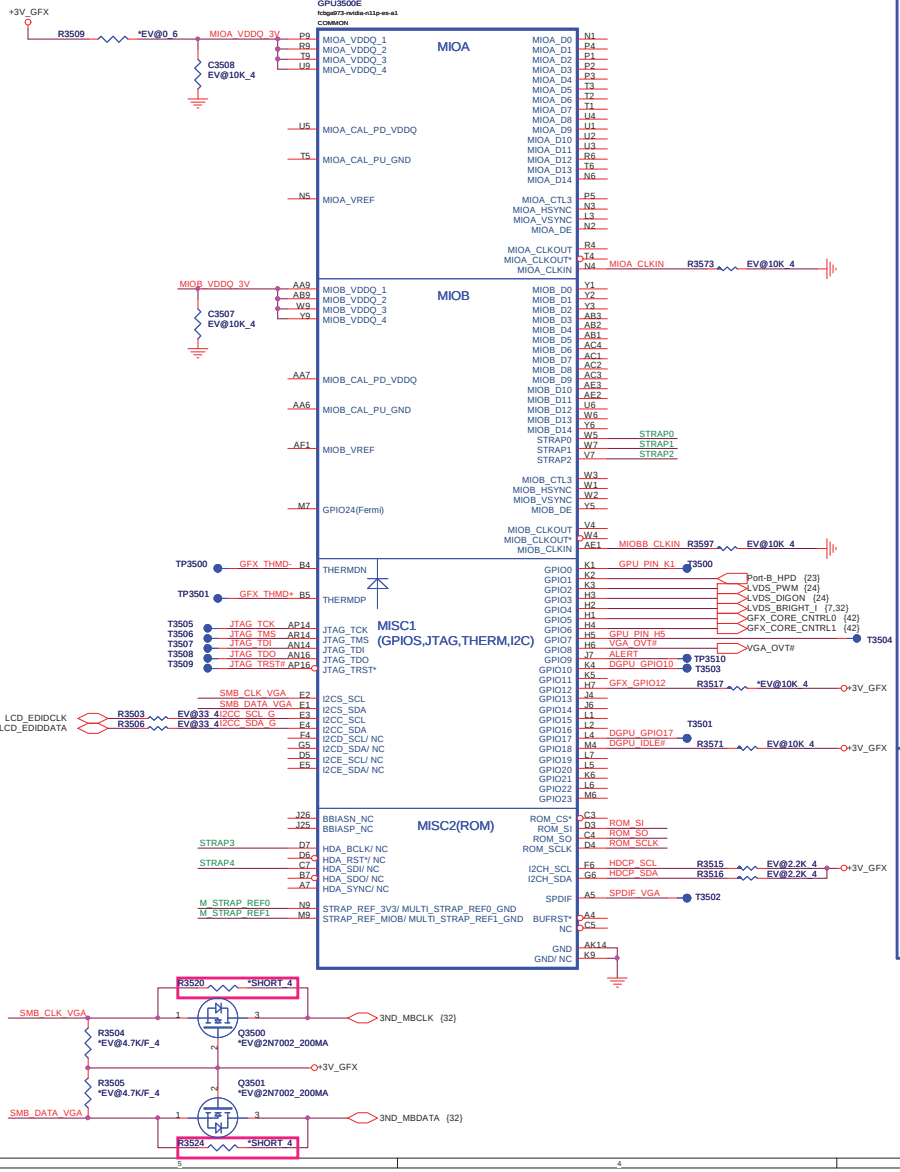


Quanta Computer Inc.

PROJECT :TE5

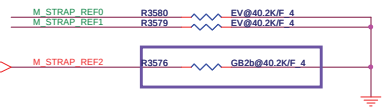
Size	Document Number	Rev
	N11x-Fermi (DISPLAY)	1A

Date: Wednesday, January 05, 2011 | Sheet 17 of 44

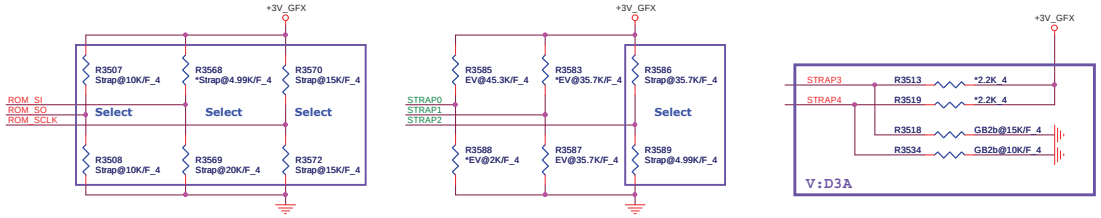


Strappin Model select

MODE	M_STRAP_REF0	M_STRAP_REF1	M_STRAP_REF2
Multi-level	40.2K/F_4 PD	40.2K/F_4 PD	40.2K/F_4 PD



MULTI level strap select



		Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	N12M-GE	N12P-GV	N12P-LP	
ROM_SCLK		PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG PCI_DEVIDE[5]	PEX_PLL_EN_TERM	1010(15KPU)	1001(10KPU)	0010(15KPD)	
ROM_SI		RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	RAMCFG_T	RAMCFG_T	RAMCFG_T	
ROM_SO	GB1/2	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001(10KPD)	1001(10KPU)	0001(10KPD)	Need to Update
	GB2B	FB[1]	FB[0]						
STRAP0		USER[3]	USER[2]	USER[1]	USER[0]	1111(45KPU)	1111(45KPU)	1111(45KPU)	
STRAP1		3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110(35KPD)	0110(35KPD)	0110(35KPD)	Need to Update
STRAP2		PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1010(15KPU)	0000(5KPD)	1100(25KPU)	
STRAP3(Only GB2B)		SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED		0010(15KPD)		Need to Update
STRAP4(Only GB2B)		Reserve	Reserve	PCIE_MAX_SPEED	DP_PLL_VDD33V		0001(10KPD)		

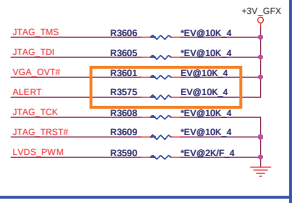
VRAM Configuration Table

RAMCFG [3:0]		DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0x0	0000				
0x1	0001				
0x2	0010	DDR3 64Mx16x8, 128bit, 1GB	Hynix	H5TQ1G63DFR-12C(800MHz) / H5TQ1G63DFR-11C(900MHz)	PD 15K
0x3	0011	DDR3 64Mx16x8, 128bit, 1GB	Samsung	K4W1G1646E-HC12(800MHz) / K4W1G1646E-HC11(900MHz)	PD 20K
0x4	0101				
0x5	0110				
0x6	0110	DDR3 128Mx16x8, 128bit, 2GB	Hynix	H5TQ2G63BFR-12C(800MHz) / H5TQ2G63BFR-11C(900MHz)	PD 35K
0x7	0111	DDR3 128Mx16x8, 128bit, 2GB	Samsung	K4W2G1646C-HC1(800MHz)2 / K4W2G1646C-HC11(900MHz)	PD 45K

N12M-GE(QS)
Device Id=0x0A7A
STRAP2 =15K PU
ROM_SCLK=15K PU

N12P-GV(QS)
Device Id=-x1050
STRAP2 =5K PD
ROM_SCLK=10K PU

N12P-LP(QS)
Device Id=0x0DEC
STRAP2=25K PU
ROM_SCLK=15K PD



GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Quanta Computer Inc.
PROJECT : TE5

Size	Document Number	Rev
	N11x-Fermi (GND&Str&Ther)	1A
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18-V

GPU3500F
fcbga973-nvidia-n11p-es-a1
COMMON

+VCORE_GFX

NVVDD

AB11	VDD_001	P21
AB13	VDD_002	P23
AB15	VDD_003	P25
AB17	VDD_004	R11
AB19	VDD_005	R12
AB21	VDD_006	R13
AB23	VDD_007	R14
AB25	VDD_008	R15
AC11	VDD_009	R16
AC12	VDD_010	R17
AC13	VDD_011	R18
AC14	VDD_012	R19
AC15	VDD_013	R20
AC16	VDD_014	R21
AC17	VDD_015	R22
AC18	VDD_016	R23
AC19	VDD_017	R24
AC20	VDD_018	R25
AC21	VDD_019	T12
AC22	VDD_020	T14
AC23	VDD_021	T16
AC24	VDD_022	T18
AC25	VDD_023	T20
AD12	VDD_024	T22
AD14	VDD_025	T24
AD16	VDD_026	V11
AD18	VDD_027	V13
AD22	VDD_028	V15
AD24	VDD_029	V17
L11	VDD_030	V19
L12	VDD_031	V21
L13	VDD_032	V23
L14	VDD_033	V25
L15	VDD_034	W11
L16	VDD_035	W12
L17	VDD_036	W13
L18	VDD_037	W14
L19	VDD_038	W15
L20	VDD_039	W16
L21	VDD_040	W17
L22	VDD_041	W18
L23	VDD_042	W19
L24	VDD_043	W20
L25	VDD_044	W21
M12	VDD_045	W22
M14	VDD_046	W23
M16	VDD_047	W24
M18	VDD_048	W25
M20	VDD_049	Y12
M22	VDD_050	Y14
M24	VDD_051	Y16
P11	VDD_052	Y18
P13	VDD_053	Y20
P15	VDD_054	Y22
P17	VDD_055	Y24
P19	VDD_056	
	VDD_057	
	VDD_058	
	VDD_059	
	VDD_060	
	VDD_061	
	VDD_062	
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	VDD_103	
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	VDD_105	
	VDD_106	
	VDD_107	
	VDD_108	
	VDD_109	
	VDD_110	
	VDD_111	

+VCORE_GFX

GPU3500G
fcbga973-nvidia-n11p-es-a1
COMMON

GROUND

AA11	GND_1	GND_096 E15
AA12	GND_2	GND_097 E18
AA13	GND_3	GND_098 E24
AA14	GND_4	GND_099 E27
AA15	GND_5	GND_100 E30
AA16	GND_6	GND_101 E6
AA17	GND_7	GND_102 E9
AA18	GND_8	GND_103 F2
AA19	GND_9	GND_104 F31
AA2	GND_10	GND_105 F34
AA20	GND_11	GND_106 F5
AA21	GND_12	GND_107 J2
AA22	GND_13	GND_108 J31
AA23	GND_14	GND_109 J34
AA24	GND_15	GND_110 J5
AA25	GND_16	GND_111 L9
AA34	GND_17	GND_112 M11
AA5	GND_18	GND_113 M13
AB12	GND_19	GND_114 M15
AB14	GND_20	GND_115 M17
AB16	GND_21	GND_116 M19
AB18	GND_22	GND_117 M2
AB20	GND_23	GND_118 M21
AB22	GND_24	GND_119 M23
AB24	GND_25	GND_120 M25
AC9	GND_26	GND_121 M31
AD11	GND_27	GND_122 M34
AD13	GND_28	GND_123 M5
AD15	GND_29	GND_124 N11
AD17	GND_30	GND_125 N12
AD2	GND_31	GND_126 N13
AD21	GND_32	GND_127 N14
AD23	GND_33	GND_128 N15
AD25	GND_34	GND_129 N16
AD31	GND_35	GND_130 N17
AD34	GND_36	GND_131 N18
AD5	GND_37	GND_132 N19
AE11	GND_38	GND_133 N20
AE12	GND_39	GND_134 N21
AE13	GND_40	GND_135 N22
AE14	GND_41	GND_136 N23
AE15	GND_42	GND_137 N24
AE16	GND_43	GND_138 N25
AE17	GND_44	GND_139 P12
AE18	GND_45	GND_140 P14
AE19	GND_46	GND_141 P16
AE20	GND_47	GND_142 P18
AE21	GND_48	GND_143 P20
AE22	GND_49	GND_144 P22
AE23	GND_50	GND_145 P24
AE24	GND_51	GND_146 R2
AE25	GND_52	GND_147 R31
AG2	GND_53	GND_148 R34
AG31	GND_54	GND_149 R5
AG34	GND_55	GND_150 T11
AG5	GND_56	GND_151 T13
AK2	GND_57	GND_152 T15
AK31	GND_58	GND_153 T17
AK34	GND_59	GND_154 T19
AK5	GND_60	GND_155 T21
AL12	GND_61	GND_156 T23
AL15	GND_62	GND_157 T25
AL18	GND_63	GND_158 U11
AL21	GND_64	GND_159 U12
AL24	GND_65	GND_160 U13
AL27	GND_66	GND_161 U14
AL30	GND_67	GND_162 U15
AL6	GND_68	GND_163 U16
AL9	GND_69	GND_164 U17
AN2	GND_70	GND_165 U18
AN34	GND_71	GND_166 U19
AP12	GND_72	GND_167 U20
AP15	GND_73	GND_168 U21
AP18	GND_74	GND_169 U22
AP21	GND_75	GND_170 U23
AP24	GND_76	GND_171 U24
AP27	GND_77	GND_172 U25
AP3	GND_78	GND_173 V12
AP30	GND_79	GND_174 V14
AP33	GND_80	GND_175 V16
AP6	GND_081	GND_176 V18
AP9	GND_082	GND_177 V2
B12	GND_083	GND_178 V20
B15	GND_084	GND_179 V22
B21	GND_085	GND_180 V24
B24	GND_086	GND_181 V31
B27	GND_087	GND_182 V5
B3	GND_088	GND_183 V9
B30	GND_089	GND_184 Y11
B33	GND_090	GND_185 Y13
B6	GND_091	GND_186 Y15
B9	GND_092	GND_187 Y17
C2	GND_093	GND_188 Y19
C34	GND_094	GND_189 Y21
E12	GND_095	GND_190 Y23
		GND_191 Y25

PLACE UNDER BALLS

+VCORE_GFX

C3557	EV@0.01U/25V_4X
C3552	EV@0.01U/25V_4X
C3563	EV@0.01U/25V_4X
C3558	EV@0.01U/25V_4X
C3560	EV@0.01U/25V_4X
C3565	EV@0.01U/25V_4X
C3576	GB2/2b@0.01U/25V_4X
C3692	GB2/2b@0.01U/25V_4X
C3708	GB2/2b@0.022U/16V_4X
C3707	GB2/2b@0.022U/16V_4X
C3705	GB2/2b@0.022U/16V_4X
C3564	EV@0.047U/10V_4X
C3553	EV@0.047U/10V_4X
C3559	EV@0.047U/10V_4X
C3609	EV@0.1U/10V_4X
C3704	GB2/2b@0.1U/10V_4X
C3703	GB2/2b@0.22U/10V_4X
C3709	GB2/2b@0.22U/10V_4X
C3706	GB2/2b@0.22U/10V_4X
C3550	GB2/2b@1U/10V_4X
C3607	*EV@1U/10V_4X
C3614	*EV@1U/10V_4X

PLACE NEAR BALLS

+VCORE_GFX

C3567	EV@4.7U/6.3V_6X
C3589	GB2/2b@10U/6.3V_8X
C3580	GB2/2b@10U/6.3V_8X
C3710	GB2/2b@22U/6.3V_8X
C3711	GB2/2b@47U/6.3V_1206X
C3591	*EV@10U/6.3V_8X
C3606	*EV@10U/6.3V_8X
C3597	*EV@4.7U/6.3V_6X
C3584	*EV@4.7U/6.3V_6X

Quanta Computer Inc.
PROJECT : TE5

Size	Document Number	Rev
	N11x-Fermi (GND/Power)	1A

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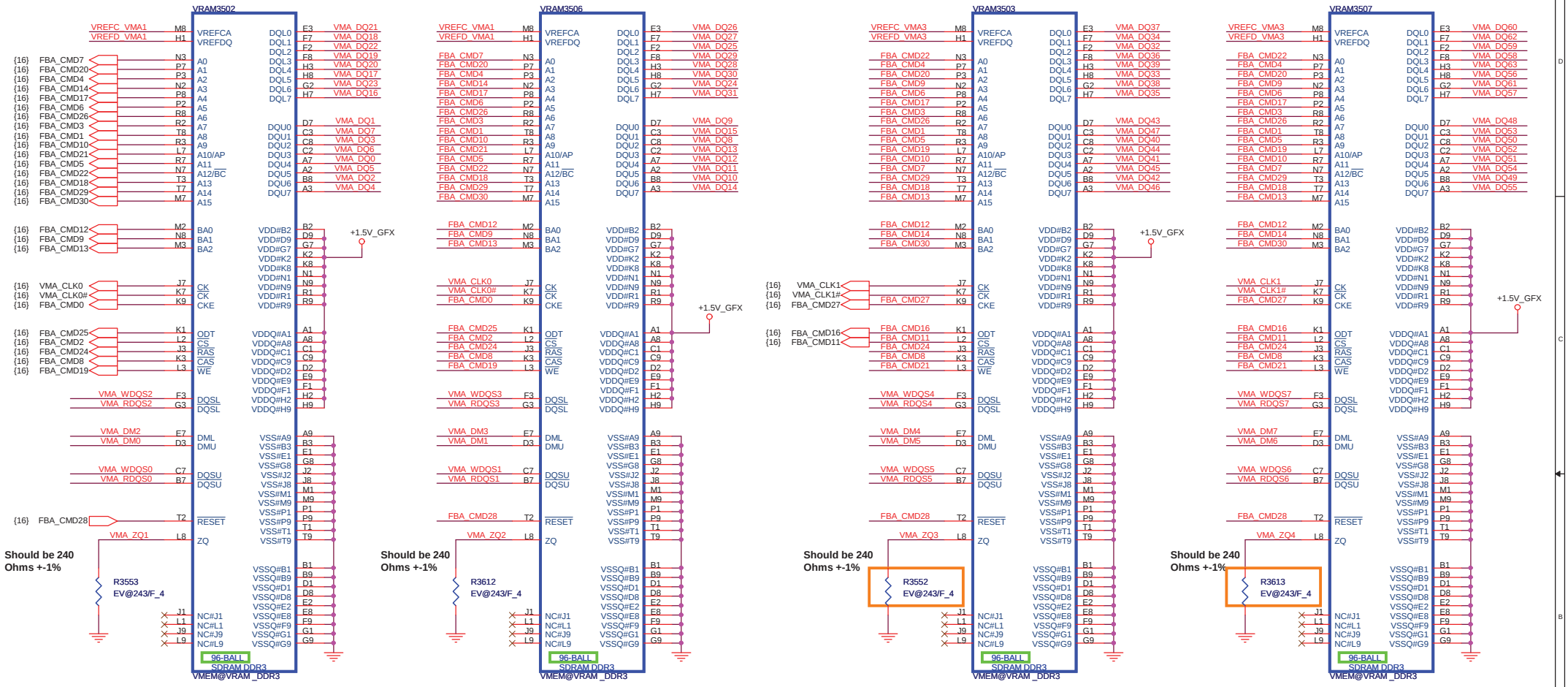
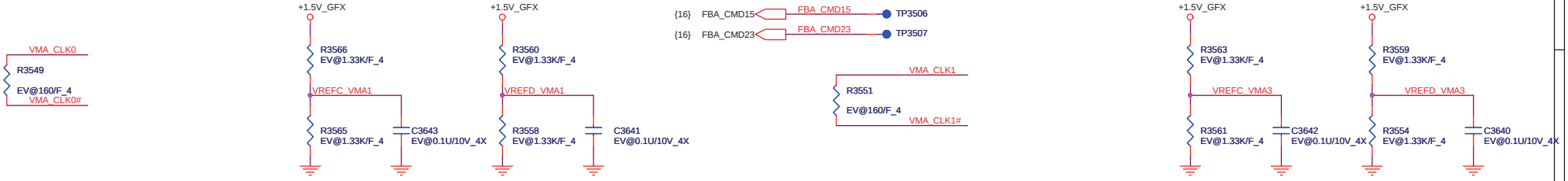
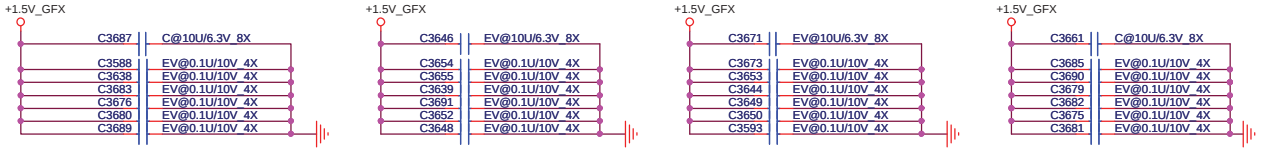
20-V

CHANNEL A: 256MB/512MB DDR3

{16} VMA_DQ[63..0]
{16} VMA_DM[7..0]
{16} VMA_WDQS[7..0]
{16} VMA_RDQS[7..0]







Quanta Computer Inc.

PROJECT : TE5

Size	Document Number	Rev
	N11x-Fermi VRAM A	1A
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21-V

CHANNEL B: 256MB/512MB DDR3

{16} VMC_DQ[63..0]
{16} VMC_DM[7..0]
{16} VMC_WDQS[7..0]
{16} VMC_RDQS[7..0]

VRAM3504 — GB2@VRAM _DDR3

VREFC_VMC1 M8
VREFD_VMC1 H1
{16} FBC_CMD7 N3
{16} FBC_CMD20 P7
{16} FBC_CMD4 P3
{16} FBC_CMD14 N2
{16} FBC_CMD17 P8
{16} FBC_CMD6 P2
{16} FBC_CMD26 R8
{16} FBC_CMD3 R2
{16} FBC_CMD1 T8
{16} FBC_CMD10 R3
{16} FBC_CMD21 L7
{16} FBC_CMD5 R7
{16} FBC_CMD22 N7
{16} FBC_CMD18 T3
{16} FBC_CMD29 T7
{16} FBC_CMD30 M7
{16} FBC_CMD12 M2
{16} FBC_CMD9 N8
{16} FBC_CMD13 M3
{16} VMC_CLK0 J7
{16} VMC_CLK0# K7
{16} FBC_CMD0 K9
{16} FBC_CMD25 K1
{16} FBC_CMD2 L2
{16} FBC_CMD24 J3
{16} FBC_CMD8 K3
{16} FBC_CMD19 L3
VMC_WDQS2 F3
VMC_RDQS2 G3
VMC_DM2 E7
VMC_DM0 D3
VMC_WDQS0 C7
VMC_RDQS0 B7
{16} FBC_CMD28 T2
VMC_ZQ1 L8
VREFA, VREFDQ
A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10/AP, A11, A12/BC, A13, A14, A15
BA0, BA1, BA2
CK, CK, CKE
ODT, CS, RAS, CAS, WE
DQSL, DQSL
DML, DMU
RESET
ZQ
NC#J1, NC#L1, NC#J9, NC#L9
DQL0 E3 VMC_DQ22
DQL1 F7 VMC_DQ21
DQL2 F2 VMC_DQ23
DQL3 F8 VMC_DQ16
DQL4 H3 VMC_DQ20
DQL5 H8 VMC_DQ17
DQL6 G2 VMC_DQ18
DQL7 H7 VMC_DQ19
DQU0 D7 VMC_DQ3
DQU1 C3 VMC_DQ6
DQU2 C8 VMC_DQ0
DQU3 C2 VMC_DQ7
DQU4 A7 VMC_DQ1
DQU5 A2 VMC_DQ5
DQU6 B8 VMC_DQ2
DQU7 A3 VMC_DQ4
VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9
+1.5V_GFX
VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9
VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9
VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9
96-BALL SDRAM DDR3

Should be 240 Ohms +-1%
R3574 GB2@243/F_4

VRAM3500 — GB2@VRAM _DDR3

VREFC_VMC1 M8
VREFD_VMC1 H1
FBC_CMD7 N3
FBC_CMD20 P7
FBC_CMD4 P3
FBC_CMD14 N2
FBC_CMD17 P8
FBC_CMD6 P2
FBC_CMD26 R8
FBC_CMD3 R2
FBC_CMD1 T8
FBC_CMD10 R3
FBC_CMD21 L7
FBC_CMD5 R7
FBC_CMD22 N7
FBC_CMD18 T3
FBC_CMD29 T7
FBC_CMD30 M7
FBC_CMD12 M2
FBC_CMD9 N8
FBC_CMD13 M3
VMC_CLK0 J7
VMC_CLK0# K7
FBC_CMD0 K9
FBC_CMD25 K1
FBC_CMD2 L2
FBC_CMD24 J3
FBC_CMD8 K3
FBC_CMD19 L3
VMC_WDQS3 F3
VMC_RDQS3 G3
VMC_DM3 E7
VMC_DM1 D3
VMC_WDQS1 C7
VMC_RDQS1 B7
FBC_CMD28 T2
VMC_ZQ2 L8
VREFA, VREFDQ
A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10/AP, A11, A12/BC, A13, A14, A15
BA0, BA1, BA2
CK, CK, CKE
ODT, CS, RAS, CAS, WE
DQSL, DQSL
DML, DMU
RESET
ZQ
NC#J1, NC#L1, NC#J9, NC#L9
DQL0 E3 VMC_DQ24
DQL1 F7 VMC_DQ30
DQL2 F2 VMC_DQ26
DQL3 F8 VMC_DQ28
DQL4 H3 VMC_DQ25
DQL5 H8 VMC_DQ31
DQL6 G2 VMC_DQ27
DQL7 H7 VMC_DQ29
DQU0 D7 VMC_DQ8
DQU1 C3 VMC_DQ14
DQU2 C8 VMC_DQ9
DQU3 C2 VMC_DQ12
DQU4 A7 VMC_DQ11
DQU5 A2 VMC_DQ13
DQU6 B8 VMC_DQ10
DQU7 A3 VMC_DQ15
VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9
+1.5V_GFX
VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9
VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9
VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9
96-BALL SDRAM DDR3

Should be 240 Ohms +-1%
R3530 GB2@243/F_4

VRAM3501 — GB2@VRAM _DDR3

VREFC_VMC3 M8
VREFD_VMC3 H1
FBC_CMD22 N3
FBC_CMD4 P7
FBC_CMD20 P3
FBC_CMD9 N2
FBC_CMD6 P8
FBC_CMD17 P2
FBC_CMD3 R8
FBC_CMD26 R2
FBC_CMD1 T8
FBC_CMD5 R3
FBC_CMD19 L7
FBC_CMD10 R7
FBC_CMD7 N7
FBC_CMD29 T3
FBC_CMD18 T7
FBC_CMD13 M7
FBC_CMD12 M2
FBC_CMD14 N8
FBC_CMD30 M3
{16} VMC_CLK1 J7
{16} VMC_CLK1# K7
{16} FBC_CMD27 K9
{16} FBC_CMD16 K1
{16} FBC_CMD11 L2
FBC_CMD24 J3
FBC_CMD8 K3
FBC_CMD21 L3
VMC_WDQS4 F3
VMC_RDQS4 G3
VMC_DM4 E7
VMC_DM5 D3
VMC_WDQS5 C7
VMC_RDQS5 B7
FBC_CMD28 T2
VMC_ZQ3 L8
VREFA, VREFDQ
A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10/AP, A11, A12/BC, A13, A14, A15
BA0, BA1, BA2
CK, CK, CKE
ODT, CS, RAS, CAS, WE
DQSL, DQSL
DML, DMU
RESET
ZQ
NC#J1, NC#L1, NC#J9, NC#L9
DQL0 E3 VMC_DQ36
DQL1 F7 VMC_DQ34
DQL2 F2 VMC_DQ39
DQL3 F8 VMC_DQ32
DQL4 H3 VMC_DQ37
DQL5 H8 VMC_DQ35
DQL6 G2 VMC_DQ38
DQL7 H7 VMC_DQ33
DQU0 D7 VMC_DQ42
DQU1 C3 VMC_DQ47
DQU2 C8 VMC_DQ45
DQU3 C2 VMC_DQ41
DQU4 A7 VMC_DQ44
DQU5 A2 VMC_DQ43
DQU6 B8 VMC_DQ40
DQU7 A3 VMC_DQ46
VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9
+1.5V_GFX
VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9
VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9
VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9
96-BALL SDRAM DDR3

Should be 240 Ohms +-1%
R3543 GB2@243/F_4

VRAM3505 — GB2@VRAM _DDR3

VREFC_VMC3 M8
VREFD_VMC3 H1
FBC_CMD22 N3
FBC_CMD4 P7
FBC_CMD20 P3
FBC_CMD9 N2
FBC_CMD6 P8
FBC_CMD17 P2
FBC_CMD3 R8
FBC_CMD26 R2
FBC_CMD1 T8
FBC_CMD5 R3
FBC_CMD19 L7
FBC_CMD10 R7
FBC_CMD7 N7
FBC_CMD29 T3
FBC_CMD18 T7
FBC_CMD13 M7
FBC_CMD12 M2
FBC_CMD14 N8
FBC_CMD30 M3
VMC_CLK1 J7
VMC_CLK1# K7
FBC_CMD27 K9
FBC_CMD16 K1
FBC_CMD11 L2
FBC_CMD24 J3
FBC_CMD8 K3
FBC_CMD21 L3
VMC_WDQS6 F3
VMC_RDQS6 G3
VMC_DM6 E7
VMC_DM7 D3
VMC_WDQS7 C7
VMC_RDQS7 B7
FBC_CMD28 T2
VMC_ZQ4 L8
VREFA, VREFDQ
A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10/AP, A11, A12/BC, A13, A14, A15
BA0, BA1, BA2
CK, CK, CKE
ODT, CS, RAS, CAS, WE
DQSL, DQSL
DML, DMU
RESET
ZQ
NC#J1, NC#L1, NC#J9, NC#L9
DQL0 E3 VMC_DQ54
DQL1 F7 VMC_DQ50
DQL2 F2 VMC_DQ52
DQL3 F8 VMC_DQ53
DQL4 H3 VMC_DQ49
DQL5 H8 VMC_DQ51
DQL6 G2 VMC_DQ55
DQL7 H7 VMC_DQ48
DQU0 D7 VMC_DQ61
DQU1 C3 VMC_DQ58
DQU2 C8 VMC_DQ62
DQU3 C2 VMC_DQ59
DQU4 A7 VMC_DQ60
DQU5 A2 VMC_DQ56
DQU6 B8 VMC_DQ63
DQU7 A3 VMC_DQ57
VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9
+1.5V_GFX
VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9
VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9
VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9
96-BALL SDRAM DDR3

Should be 240 Ohms +-1%
R3610 GB2@243/F_4

+1.5V_GFX
VMC_CLK0
R3510 GB2@160/F_4
VMC_CLK0#

+1.5V_GFX
R3578 GB2@1.33K/F_4
VREFC_VMC1
R3577 GB2@1.33K/F_4
C3658 GB2@0.1U/10V_4X

+1.5V_GFX
R3529 GB2@1.33K/F_4
VREFD_VMC1
R3531 GB2@1.33K/F_4
C3547 GB2@0.1U/10V_4X

VMC_CLK1
R3541 GB2@160/F_4
VMC_CLK1#

{16} FBC_CMD15 FBC_CMD15 TP3504
{16} FBC_CMD23 FBC_CMD23 TP3503

+1.5V_GFX
R3545 GB2@1.33K/F_4
VREFC_VMC3
R3544 GB2@1.33K/F_4
C3637 GB2@0.1U/10V_4X

+1.5V_GFX
R3537 GB2@1.33K/F_4
VREFD_VMC3
R3536 GB2@1.33K/F_4
C3566 GB2@0.1U/10V_4X

+1.5V_GFX
C3651 C@10U/6.3V_8X
C3678 GB2@0.1U/10V_4X
C3538 GB2@0.1U/10V_4X
C3670 GB2@0.1U/10V_4X
C3659 GB2@0.1U/10V_4X
C3666 GB2@0.1U/10V_4X
C3684 GB2@0.1U/10V_4X

+1.5V_GFX
C3548 GB2@10U/6.3V_8X
C3594 GB2@0.1U/10V_4X
C3542 GB2@0.1U/10V_4X
C3662 GB2@0.1U/10V_4X
C3657 GB2@0.1U/10V_4X
C3663 GB2@0.1U/10V_4X
C3667 GB2@0.1U/10V_4X

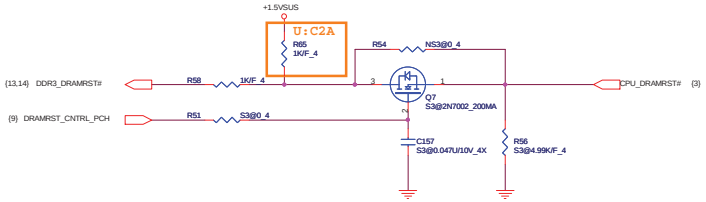
+1.5V_GFX
C3669 GB2@10U/6.3V_8X
C3577 GB2@0.1U/10V_4X
C3686 GB2@0.1U/10V_4X
C3688 GB2@0.1U/10V_4X
C3578 GB2@0.1U/10V_4X
C3549 GB2@0.1U/10V_4X
C3528 GB2@0.1U/10V_4X

+1.5V_GFX
C3573 C@10U/6.3V_8X
C3579 GB2@0.1U/10V_4X
C3635 GB2@0.1U/10V_4X
C3633 GB2@0.1U/10V_4X
C3634 GB2@0.1U/10V_4X
C3636 GB2@0.1U/10V_4X
C3537 GB2@0.1U/10V_4X

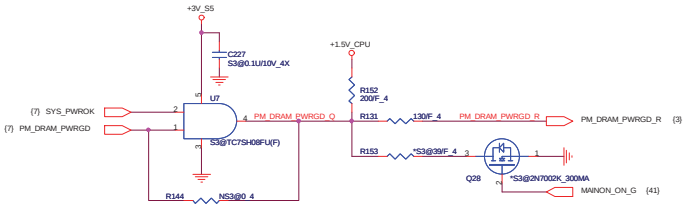
Quanta Computer Inc.
PROJECT : TE5

Size	Document Number	Rev
	N11x-Fermi VRAM B	1A
Date: Wednesday, January 05, 2011	Sheet 21 of 44	

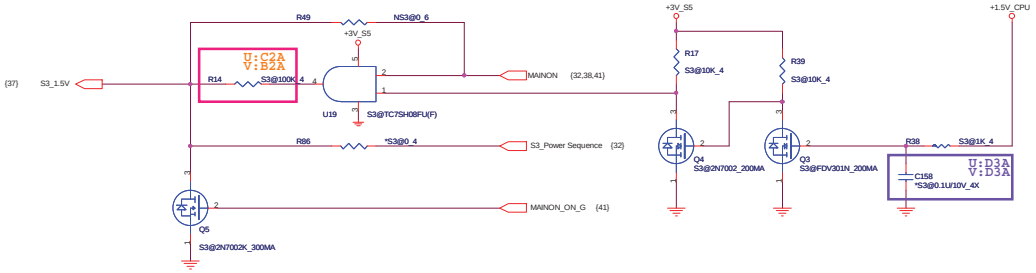
S3 power Reduction (SM_DRAMRST#) <S3P> <4>



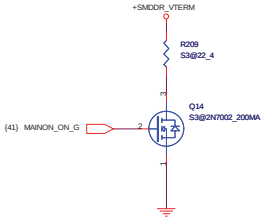
S3 power Reduction (SM_DRAMPWROK) <S3P> <3>



For S3 power Reduction Sequence <S3P> <3>

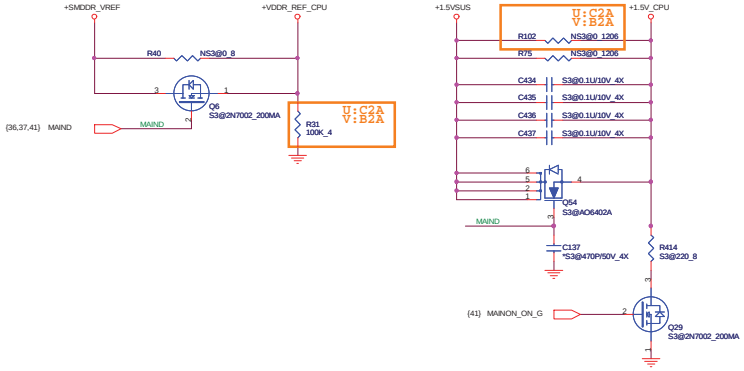


For S3 power Reduction VTT discharge <S3P> <13>



S3 power Reduction (CPU Power) <S3P> <5>

4.5A



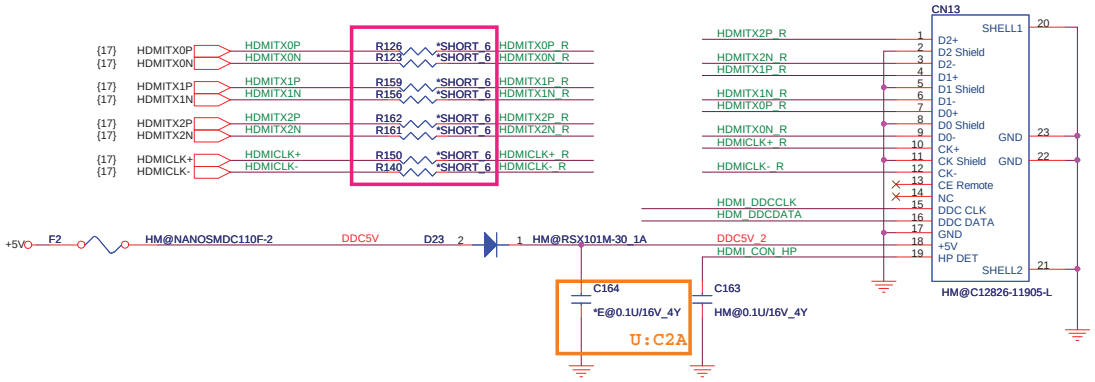
Quanta Computer Inc.

PROJECT : TE5

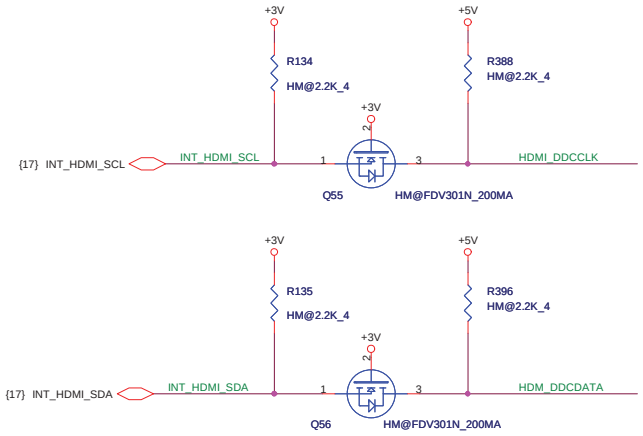
Size	Document Number	Rev
	S3 power Reduction	1A
Date: Wednesday, January 05, 2011	Sheet 22 of 44	

HDMI Conn [HDM]

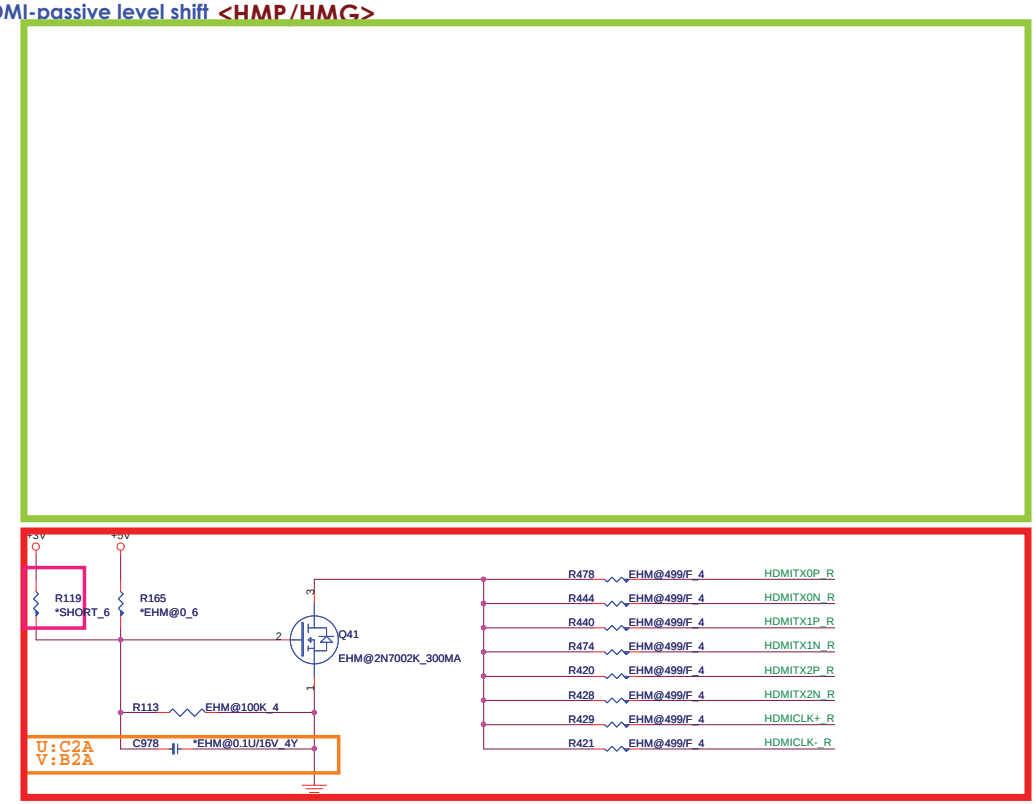
HDMI-CONN <HDM>



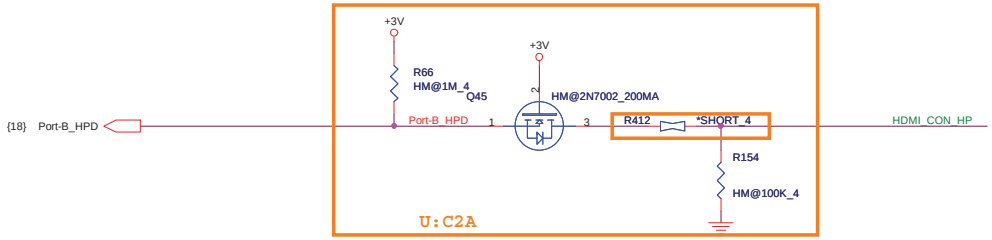
HDMI-SMBus <HDM>



HDMI-passive level shift <HMP/HMG>



HDMI-HPD <HMP/HMG>



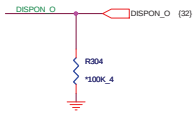
Quanta Computer Inc.

PROJECT : TE5

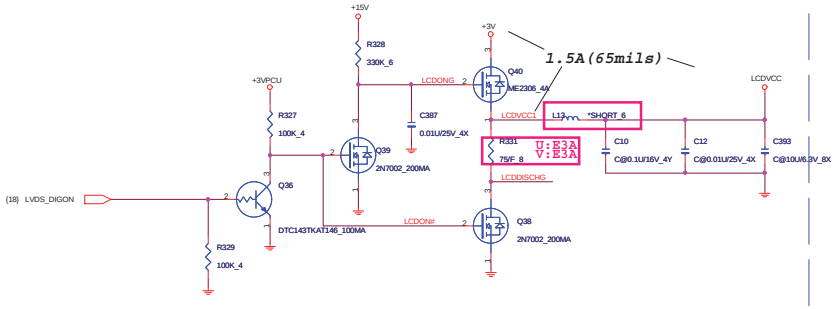
Size	Document Number	Rev
	HDMI CONN	1A

Date: Wednesday, January 05, 2011 Sheet 23 of 44

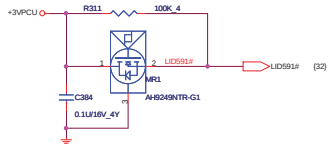
Panel backlight control <LDS>



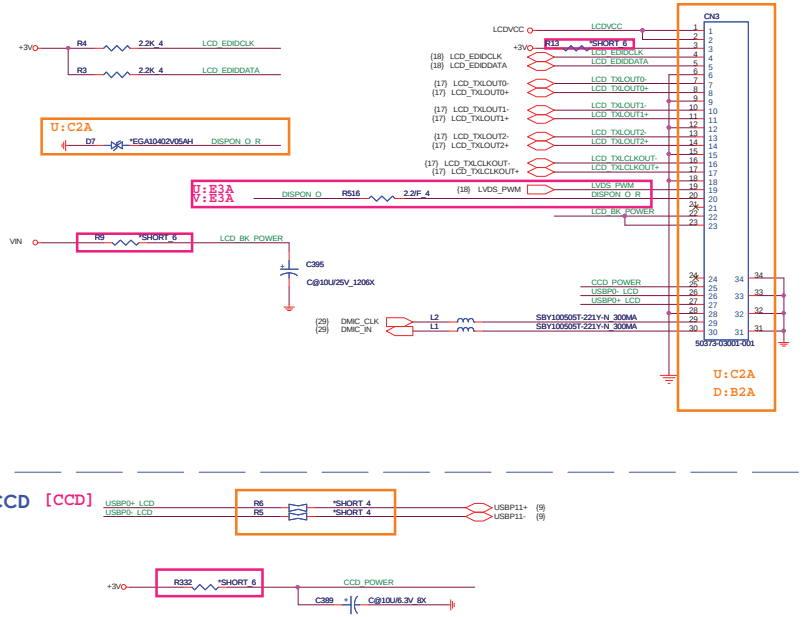
LCD POWER SWITCH <LDS>



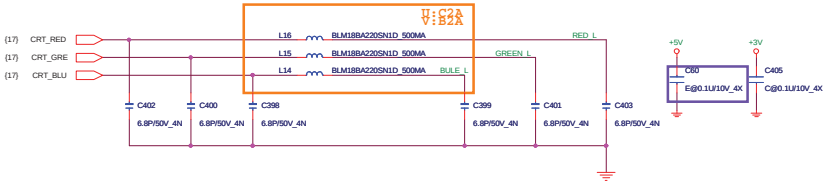
HALL Sensor<HSR>



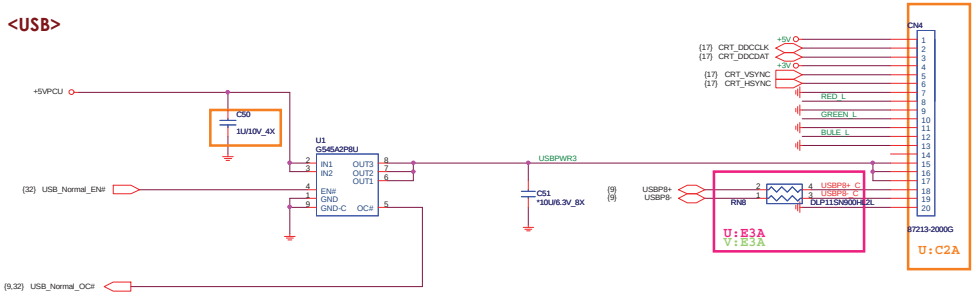
LCD Panel Module [LDS]



CRT <CRT>



USB for CRT BOARD (Right) <USB>

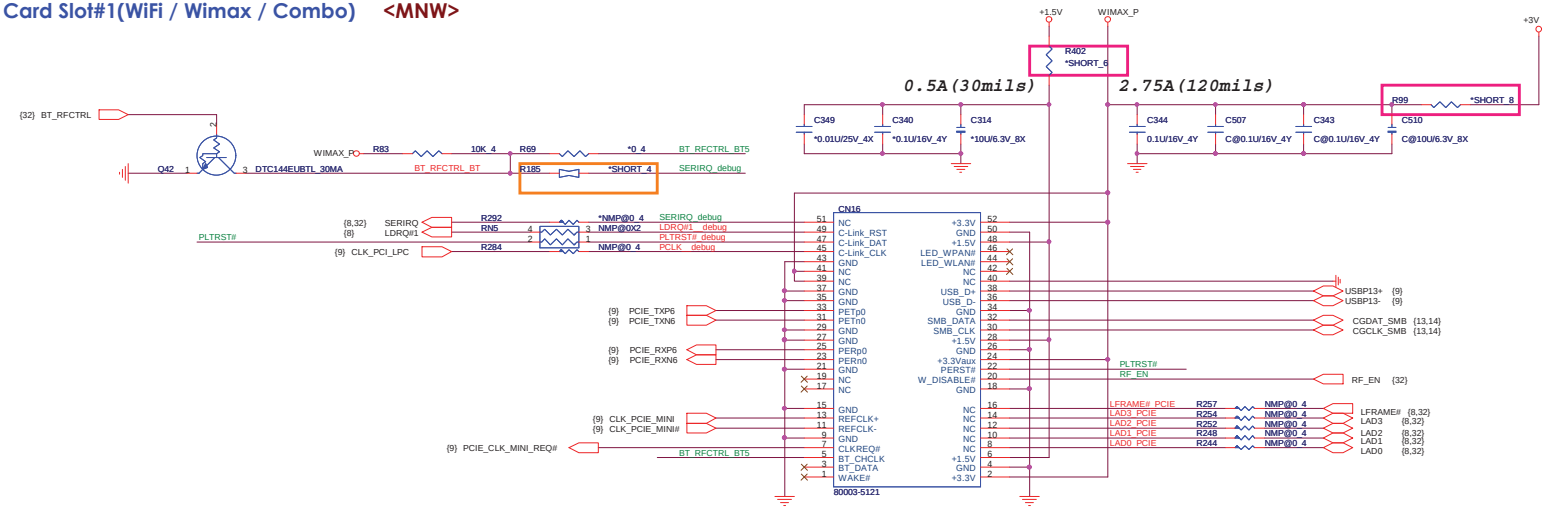


CCD [CCD]

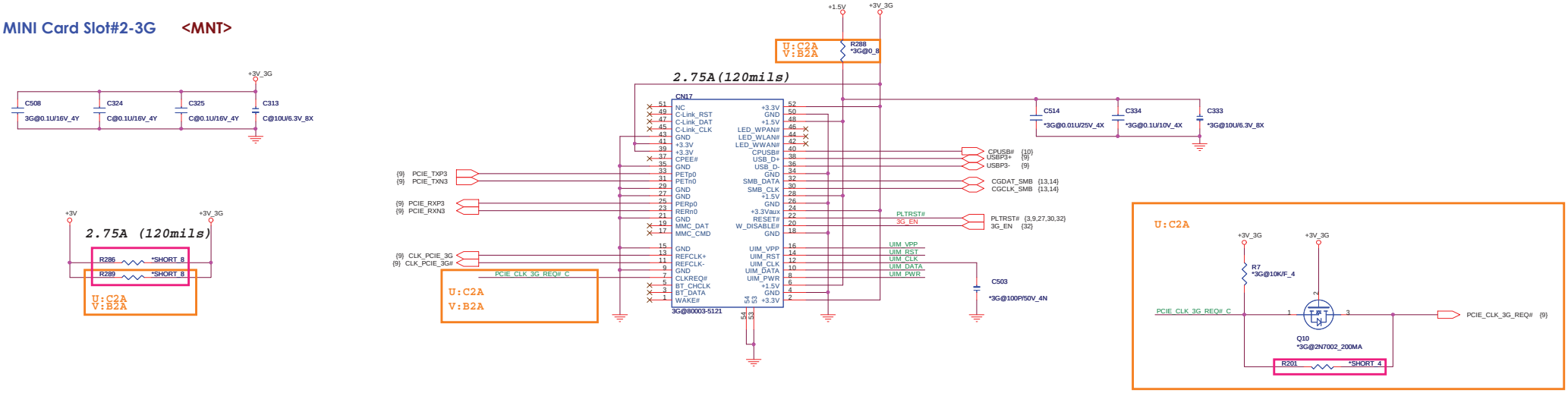
Quanta Computer Inc.
PROJECT : TE5

Size	Document Number	Rev
	LCD/LED Panel/CCD	1A
Date: Wednesday, January 05, 2011	Sheet 24 of 44	

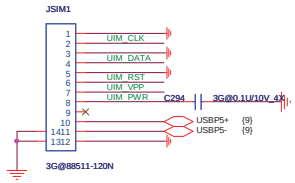
MINI Card Slot#1(WiFi / Wimax / Combo) <MNW>



MINI Card Slot#2-3G <MNT>



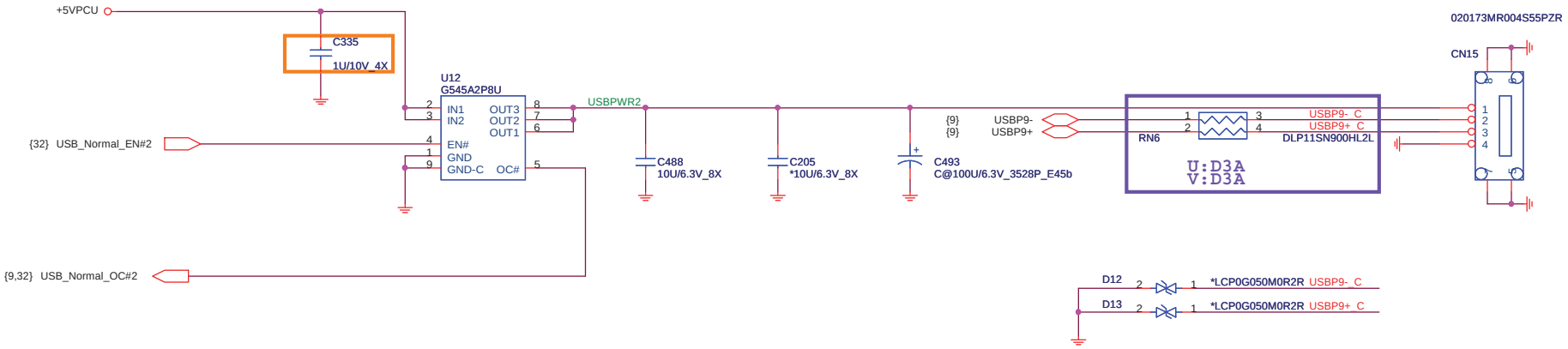
SIM CARD



Quanta Computer Inc.
PROJECT : TE5

Size	Document Number	Rev
	MINI CARD(WLAN/3G/SIM Card)	1A
Date: Wednesday, January 05, 2011	Sheet 25 of 44	

USB2.0 MB SIDE (Left) <USB>



Quanta Computer Inc.

PROJECT : TE5

Size	Document Number	Rev
	TP/SW/ESATA/USB+Audio/LED	1A

Date: Wednesday, January 05, 2011 Sheet 26 of 44

USB 3.0 Controller <U3B>

U:C2A

U6000

U3@UPD720200AF1-DAP-A

USB 3.0 Power switch <SLC>

U:C2A
V:B2A

U6002 G547E2P81U

EEPROM

U6001 U3@EN25F40-100HIP

USB 3.0 CONN

CN6000

USB 2.0 Colay <U3B>

U:B3A
V:B3A

RN7 U2@DLP11SN900HL2L

USB w S&C MAXIM solution <SLC>

U6006 MAX14566BEETA+T

CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

Quanta Computer Inc.

PROJECT : TE5

Size	Document Number	Rev
	MINI CARD(WLAN/3G/SIM Card)	1A

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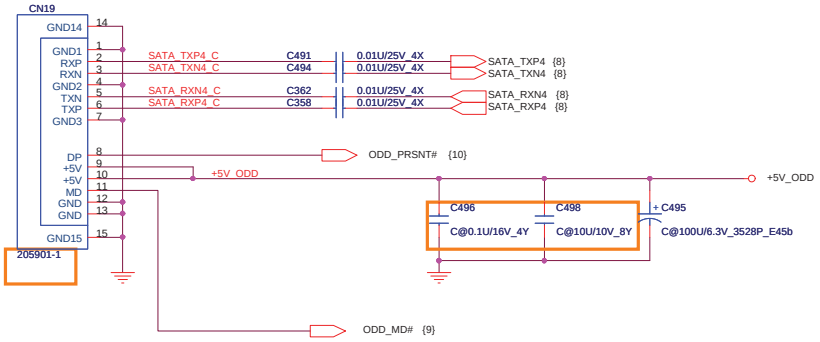
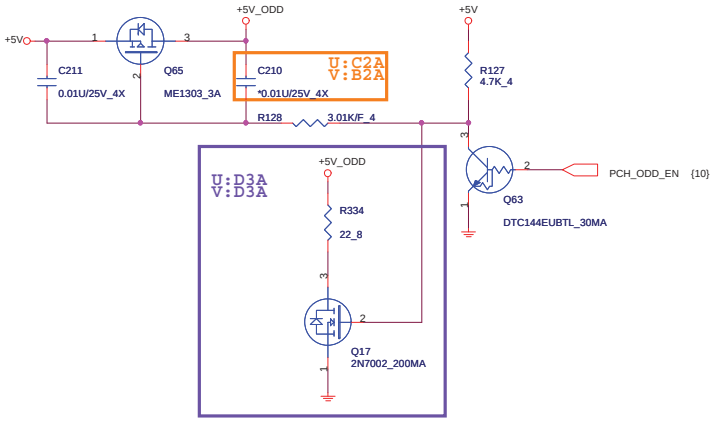
SATA ODD

[ODD]

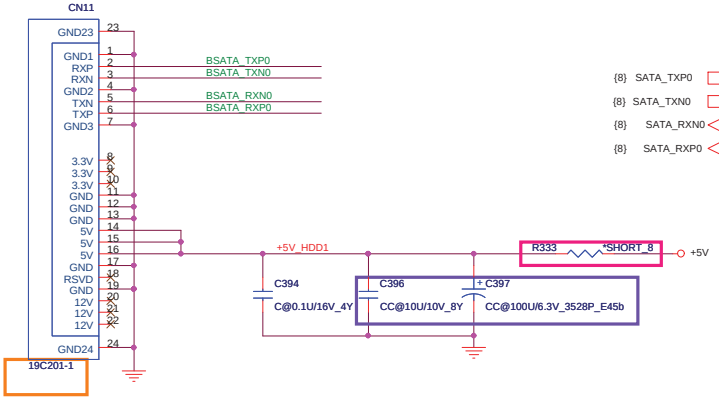


ODD Zero power . (Only for Intel) <OZP>

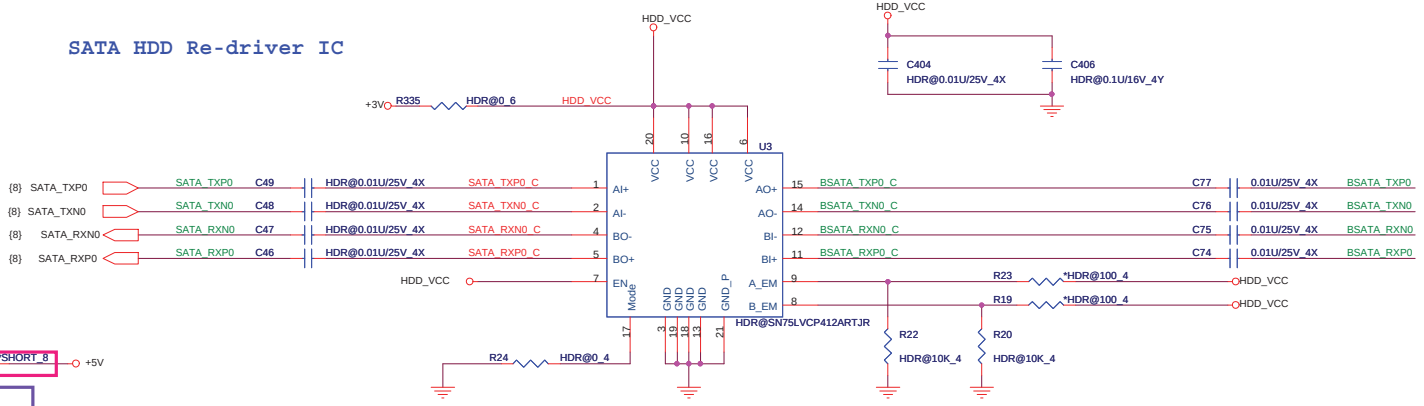


SATA HDD

[HDD]

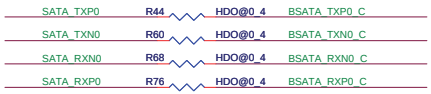


SATA HDD Re-driver IC



SATA Re-driver Bypass

Colay with Redriver IC



Quanta Computer Inc.

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Size	Document Number	Rev
	HDD/ODD/MDC	1A

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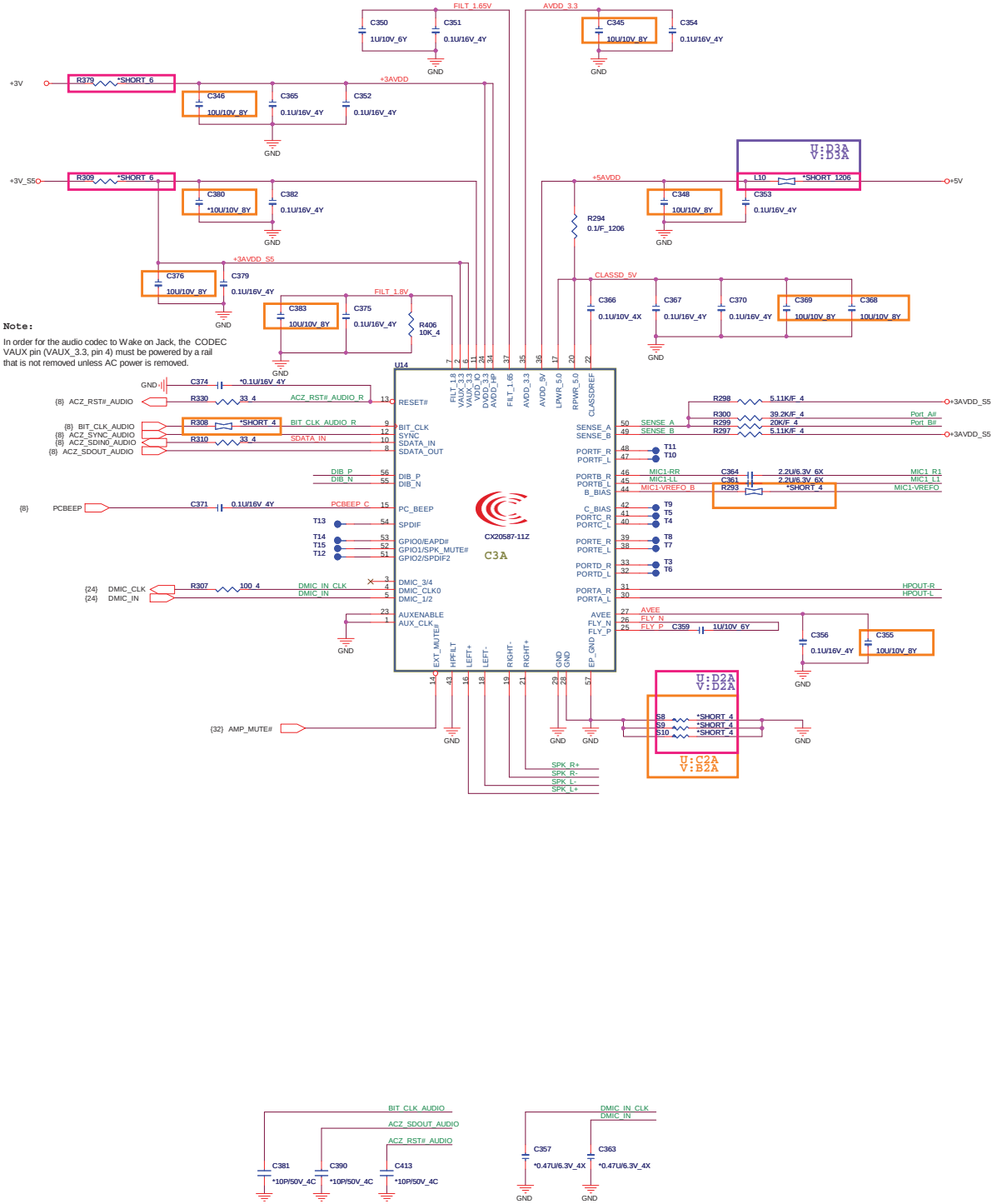
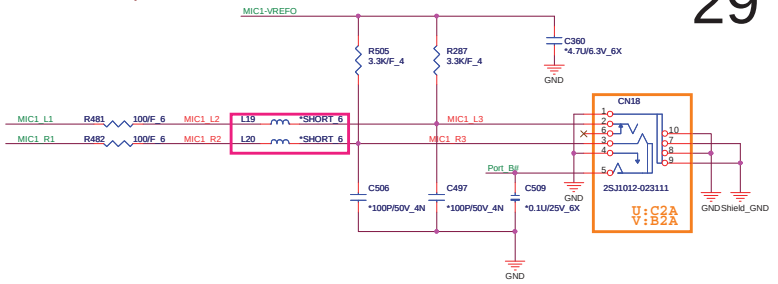
Codec(CX20587-11Z) <ADO/MDC/SLM>



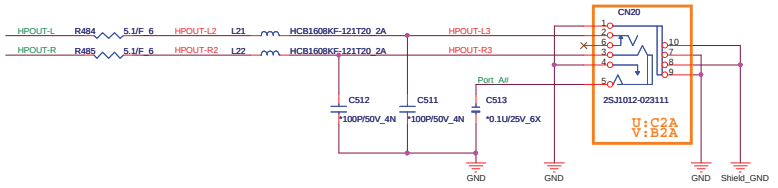
Note:

In order for the audio codec to Wake on Jack, the CODEC VAUX pin (VAUX_3.3, pin 4) must be powered by a rail that is not removed unless AC power is removed.

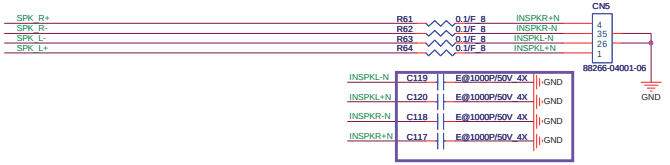
EXT MIC <ADO/SLM>



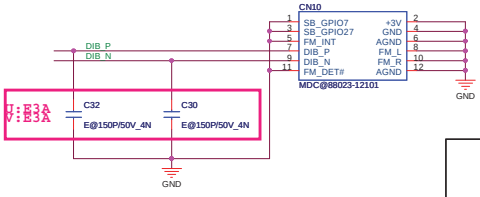
EXT H.P / Beats <ADO/AMP>



INT SPK <ADO>



MDC <MDC>



Quanta Computer Inc.			
PROJECT : TE5			
Size	Document Number		Rev
	Codec (CX20587)		1A
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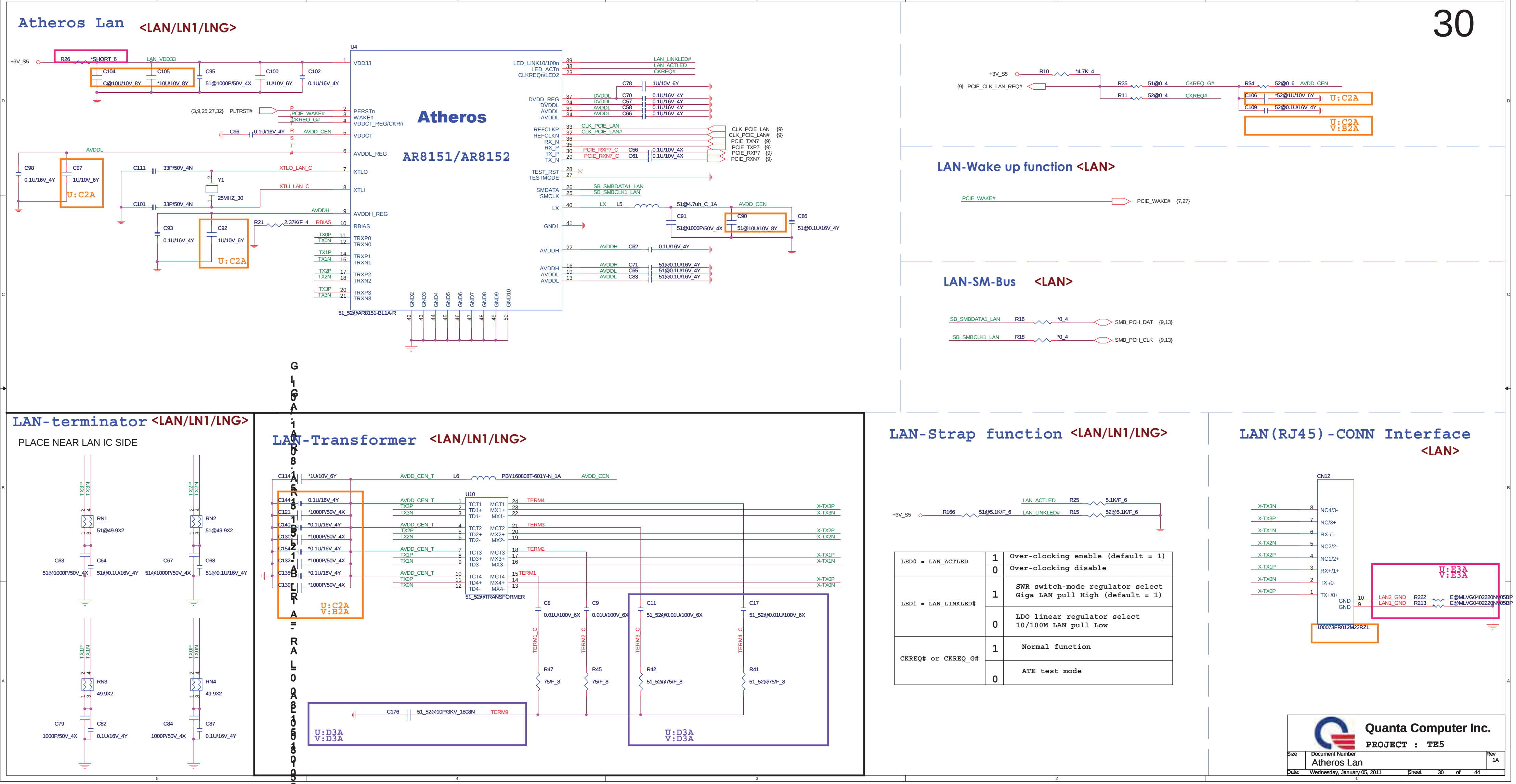
Atheros Lan <LAN/LN1/LNG>



LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

Quanta Computer Inc.

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	Atheros Lan	1A

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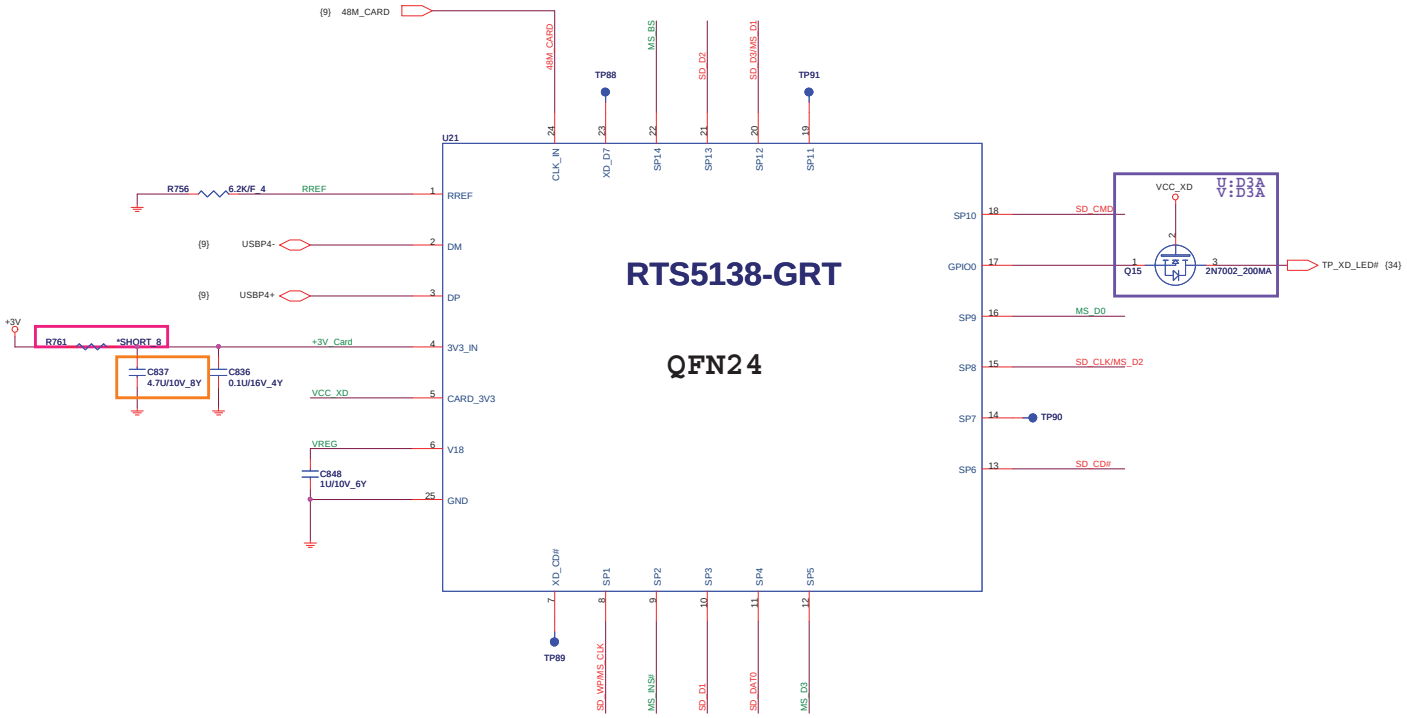
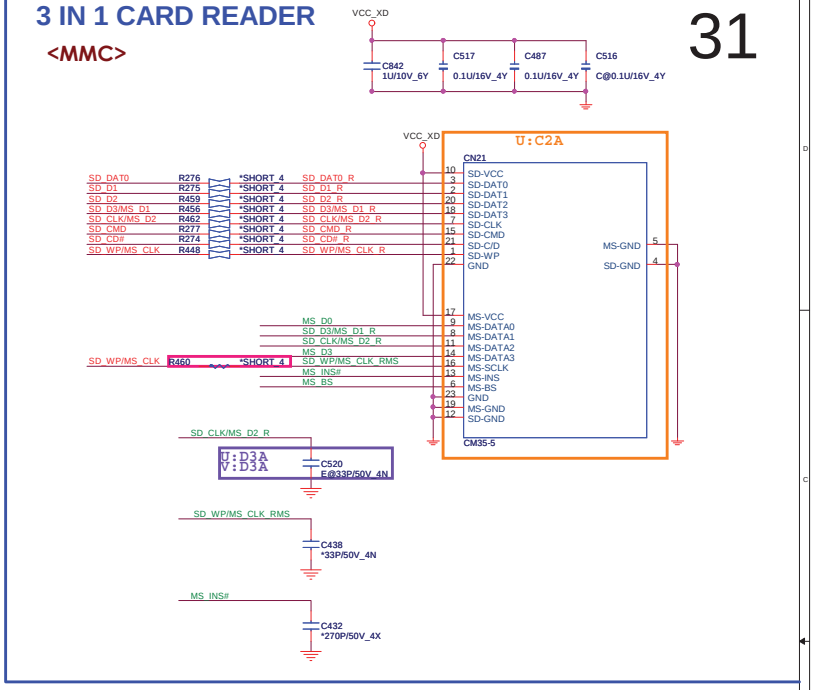
3 IN 1 CARD READER

Card reader controller <MMC>



3 IN 1 CARD READER

<MMC>



Quanta Computer Inc.

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Size	Document Number	Rev
	RTS5138 (Card Reader)	1A

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Intel Turbo mode only<CPU>

H_PROCHOT# {3,40}

H_PROCHOT_EC

R506 100K_4

Q64 2N7002_200MA

SM BUS PU/Address <KBC>

+3VPCU

MBCLK R236 4.7K_4
MBDATA R234 4.7K_4
2ND_MBCLK R468 4.7K_4
2ND_MBDATA R472 4.7K_4

3ND_MBCLK R269 4.7K_4
3ND_MBDATA R270 4.7K_4

+3V U:C2A

3Cell Battery protect & K/B LED Control <KBC>

SKU_Strap — KB_LED {33}

TP <KBC>

+5V

TPCLK R273 4.7K_4
TPDATA R279 4.7K_4

Strap <KBC>

SHBM — RF_EN — R247 10K_4

SHBM=0: Enable shared memory with host BIOS

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID EEPROM <KBC>

U20 M24C08-WMN6TP

2ND_MBCLK — SCL
2ND_MBDATA — SDA
WP
A0 A1 A2 VCC GND

+3VPCU

C477 0.1U/16V_4Y

ADDRESS: A0H

SPI FLASH <KBC>

U13 W25X40BVSSIG

SPI_SDI_uR R283 33_4 — SPI_SDI
SPI_SDO_uR R261 33_4 — SPI_SDO
SPI_SCK_uR R262 33_4 — SPI_SCK
SPI_CS0#_uR

SO SI SCK CE VDD HOLD WP VSS

+3VPCU R285 10K_4

C342 0.1U/16V_4Y

Intel	512KB	W25X40BVSSIG
AMD	2MB	W25Q16BVSSIG

INTERNAL KEYBOARD STRIP SET <KBC>

MY0 R214 10K_4 +3VPCU

HWPG circuit <KBC>

+3VPCU +3V

R186 10K_4 R196 *10K_4

{42} GFX_PG — D45 *EV@SW1010CPT_100MA — R267 EV@0_4
{39} HWPG_VCCSA — D40 *SW1010CPT_100MA — R245 *SHORT_4
{41} HWPG_1.8V — D41 *SW1010CPT_100MA — R256 *SHORT_4
{7,36} SYS_HWPG — D32 *SW1010CPT_100MA — R265 *SHORT_4
{37} HWPG_1.5V — D29 *SW1010CPT_100MA — R266 *SHORT_4
{7,40} HWPG_VAXG — D30 *IV@SW1010CPT_100MA — R280 *IV@0_4

HWPG

U:C2A

13MS,14MS,15MS Strap

+3VPCU — R371 *10K_4 — SKU_STRAP_1 — R382 10K_4
+3VPCU — R398 10K_4 — SKU_STRAP_2 — R399 *10K_4
+3VPCU — R400 EV@10K_4 — SKU_STRAP_3 — R401 IV@10K_4

U:D3A V:C2A

U:C2A

MS Strap	SKU_STRAP_1	SKU_STRAP_2	SKU_STRAP_3
13" UMA	0	0	0
13" DIS	0	0	1
14" UMA	0	1	0
14" DIS	0	1	1
15" UMA	1	0	0
15" DIS	1	0	1

Power Button<KBC>

DNBSWON# uR — C330 *0.1U/10V_4X
NBSWON# — SW1 *SHORT_PAD
D15 *LCP0G050M0R2R

LED PU/PD <LED>

+5VPCU

SUSLED_EC# R231 10K_4
BAT_SAT0# R242 10K_4
BAT_SAT1# R241 10K_4
PWRLED# R230 10K_4

+5V

RF_LED# R413 10K_4

D3A : R487 from 4.7K change to 10k.

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	EC-NPCE791LA0DX	1A

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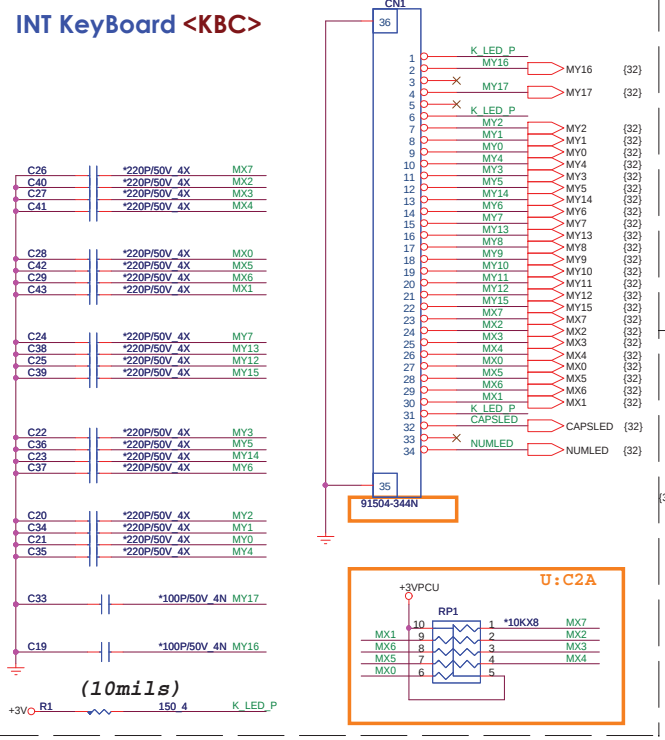
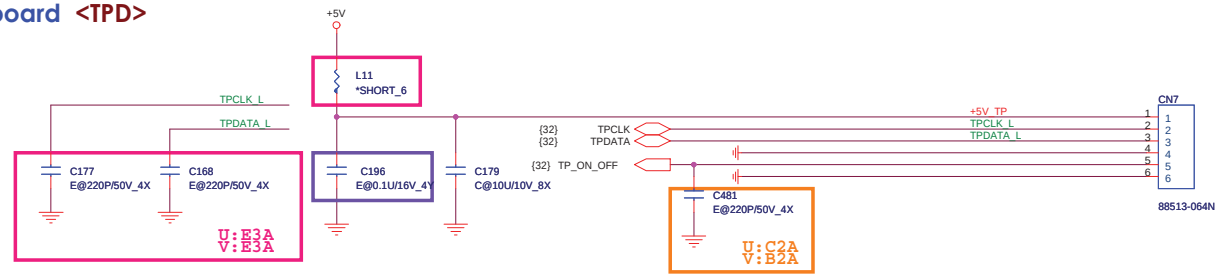
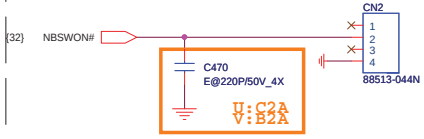
INT KeyBoard <KBC>



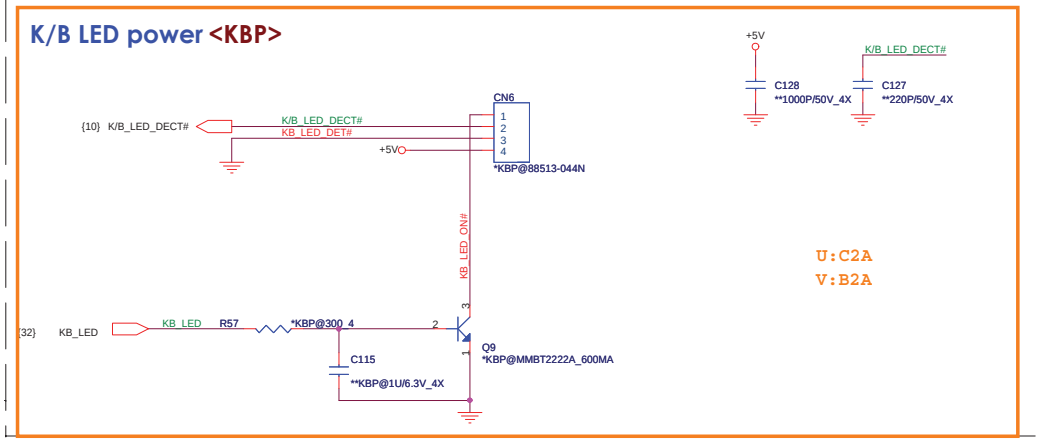
TP board <TPD>



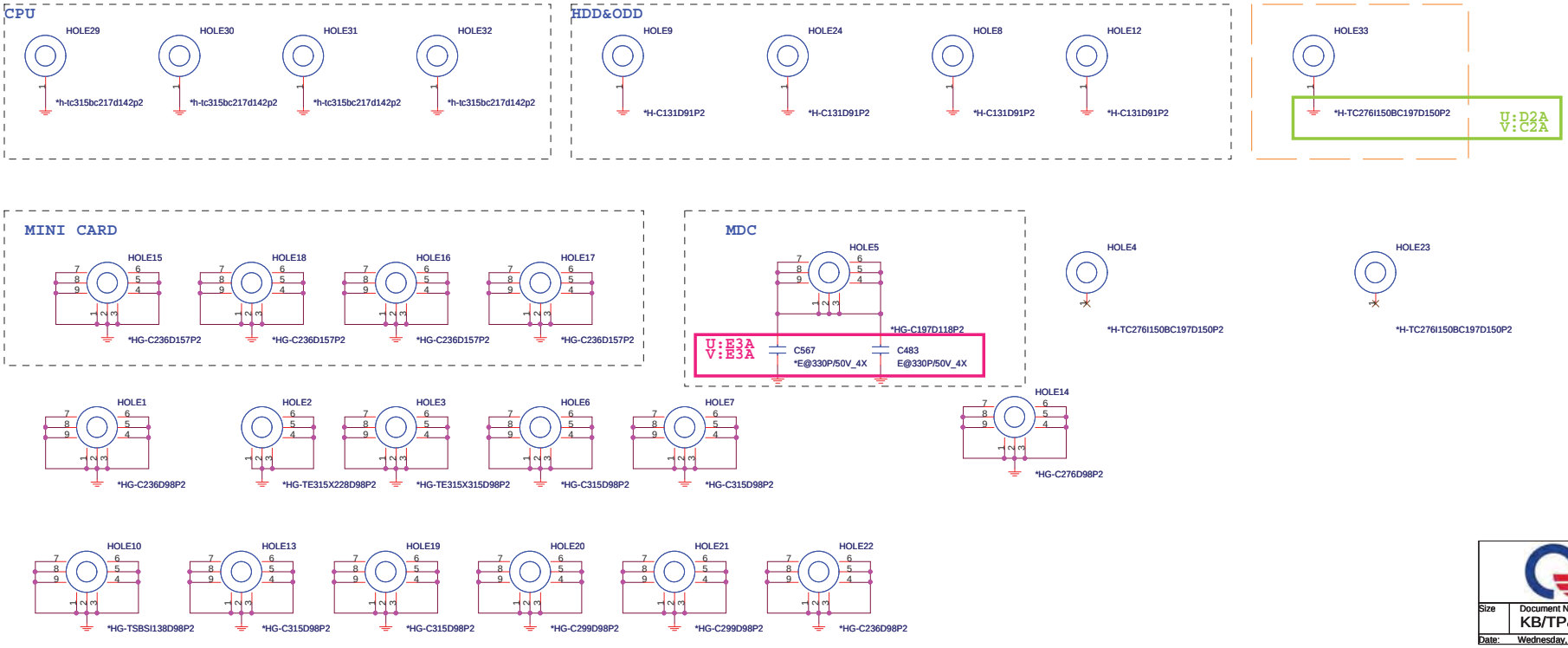
Power board <PSW>



K/B LED power <KBP>



HOLE



Quanta Computer Inc.

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Size	Document Number	Rev
	KB/TP&TP/PB/FL/LEB/MMB/B-CAS	1A

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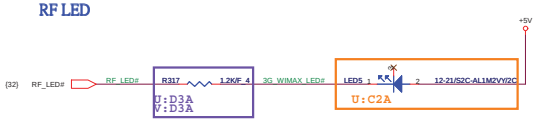
LED <LED>

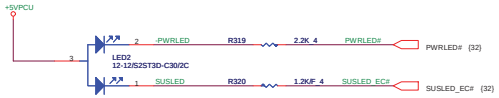
AC-IN

BATERRY

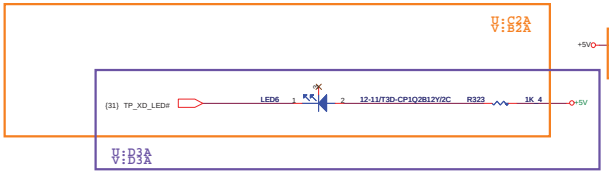
RF LED



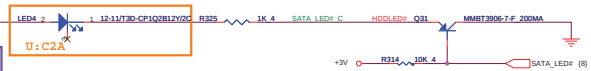
POWER



CARDREADER

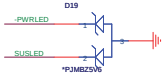


HDD/ODD

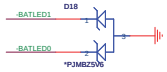


ESD Protect

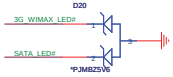
FOR POWER LED



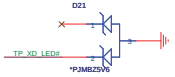
FOR BATTERY LED



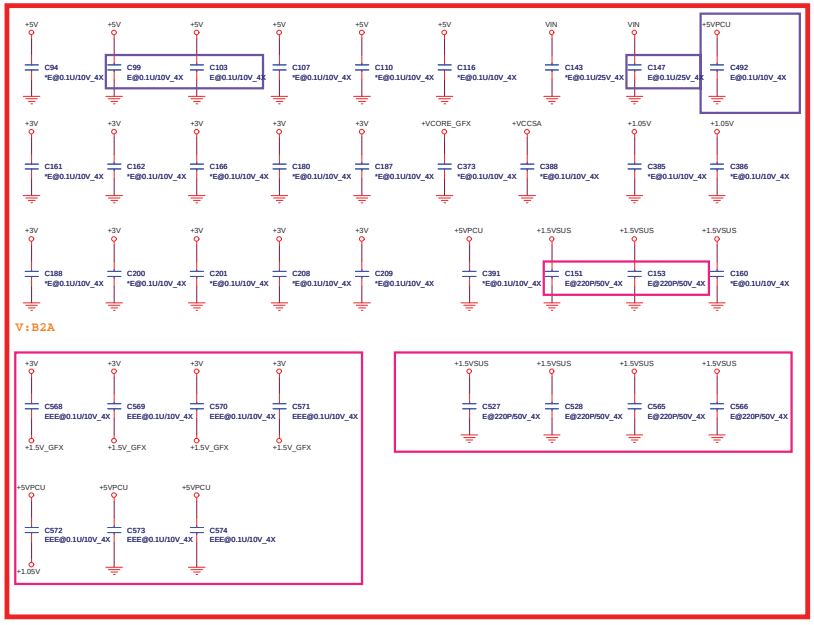
FOR HDD/W-LAN LED



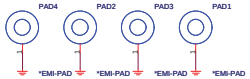
FOR 3G/CARDREADER LED

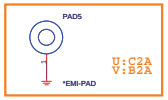


EMI



EMI PAD





Quanta Computer Inc.

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	LED/HOLE	1A

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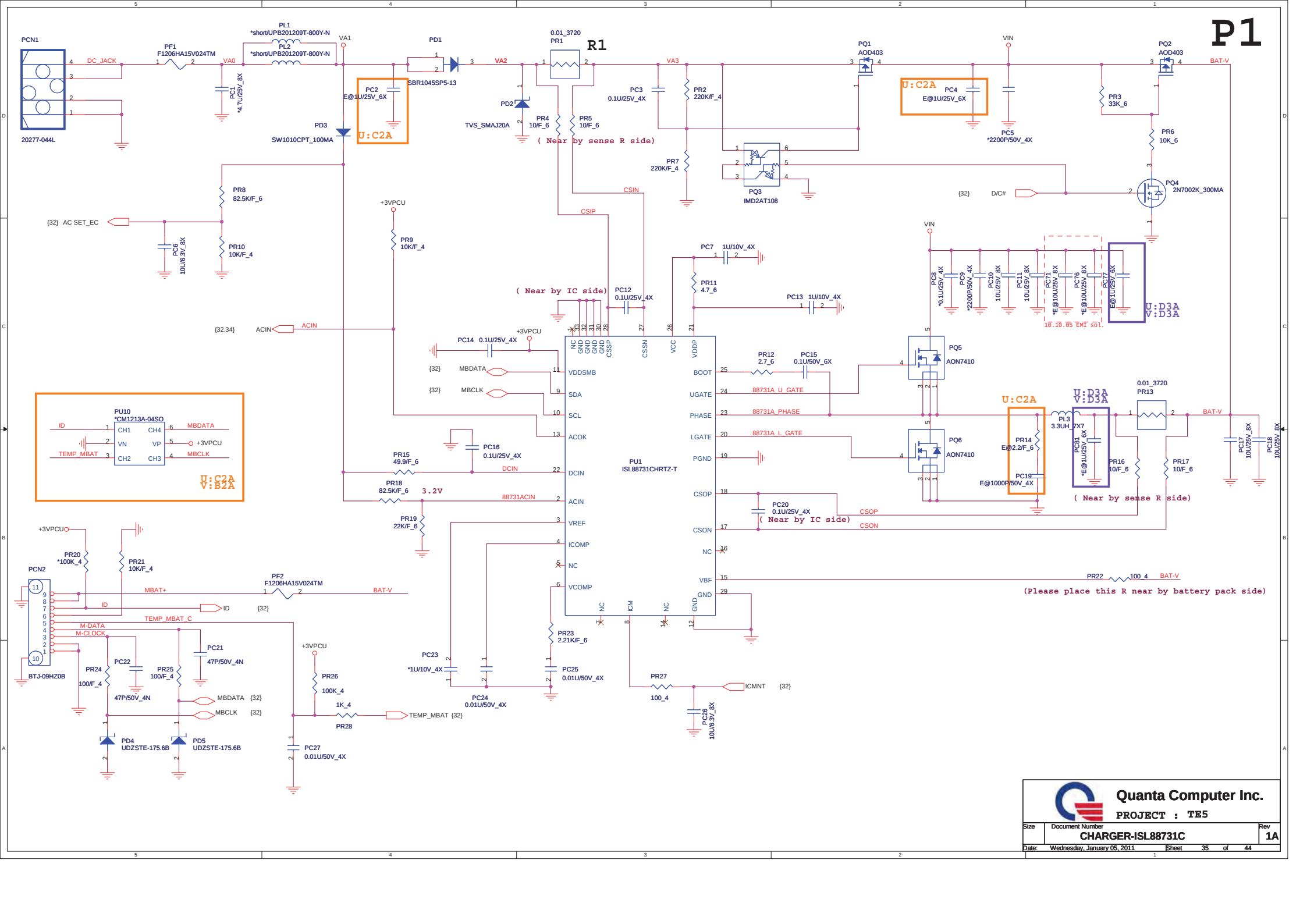
P1
PCN1
20277-044L
DC_JACK
PF1
F1206HA15V024TM
VA0
PC1
*4.7U/25V_8X
PL1
*short/UPB201209T-800Y-N
PL2
*short/UPB201209T-800Y-N
VA1
PD1
SBR1045SP5-13
VA2
PD2
TVS_SMAJ20A
PD3
SW1010CPT_100MA
U:C2A
PC2
E@1U/25V_6X
0.01_3720
PR1
R1
PR4
10/F_6
PR5
10/F_6
(Near by sense R side)
VA3
PC3
0.1U/25V_4X
PR2
220K/F_4
PR7
220K/F_4
PQ1
AOD403
PQ3
IMD2AT108
VIN
U:C2A
PC4
E@1U/25V_6X
PC5
*2200P/50V_4X
PQ2
AOD403
BAT-V
PR3
33K_6
PR6
10K_6
PQ4
2N7002K_300MA
{32} D/C#
CSIN
CSIP
PR8
82.5K/F_6
{32} AC SET_EC
PC6
10U/6.3V_8X
PR10
10K/F_4
+3VPCU
PR9
10K/F_4
PC7 1U/10V_4X
PR11
4.7_6
PC13 1U/10V_4X
(Near by IC side)
PC12
0.1U/25V_4X
VIN
PC8
*0.1U/25V_4X
PC9
*2200P/50V_4X
PC10
10U/25V_8X
PC11
10U/25V_8X
PC71
*E@10U/25V_8X
PC76
*E@10U/25V_8X
PC77
E@1U/25V_6X
10.10.05 EMI sol.
U:D3A
V:D3A
{32,34} ACIN
ACIN
PC14 0.1U/25V_4X
+3VPCU
{32} MBDATA
{32} MBCLK
PU1
ISL88731CHRTZ-T
NC
GND
GND
GND
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
NC
ICM
NC
GND
PR12
2.7_6
PC15
0.1U/50V_6X
88731A_U_GATE
88731A_PHASE
88731A_L_GATE
PQ5
AON7410
PQ6
AON7410
U:C2A
U:D3A
V:D3A
0.01_3720
PR13
PL3
3.3UH_7X7
PR14
E@2.2/F_6
PC81
*E@1U/25V_6X
PC19
E@1000P/50V_4X
PR16
10/F_6
PR17
10/F_6
PC17
10U/25V_8X
PC18
10U/25V_8X
(Near by sense R side)
PU10
*CM1213A-04SO
ID
TEMP_MBAT
CH1
VN
CH2
CH4
VP
CH3
MBDATA
+3VPCU
MBCLK
U:C2A
V:B2A
PR15
49.9/F_6
DCIN
PC16
0.1U/25V_4X
PR18
82.5K/F_6
3.2V
88731ACIN
PR19
22K/F_6
PC20
0.1U/25V_4X
(Near by IC side)
CSOP
CSON
PR22 100_4 BAT-V
(Please place this R near by battery pack side)
+3VPCU
PR20
*100K_4
PR21
10K/F_4
PCN2
BTJ-09HZ0B
MBAT+
PF2
F1206HA15V024TM
BAT-V
ID
{32}
TEMP_MBAT_C
M-DATA
M-CLOCK
PC21
47P/50V_4N
PR24
100/F_4
PC22
47P/50V_4N
PR25
100/F_4
MBDATA {32}
MBCLK {32}
PD4
UDZSTE-175.6B
PD5
UDZSTE-175.6B
+3VPCU
PR26
100K_4
1K_4
PR28
TEMP_MBAT {32}
PC27
0.01U/50V_4X
PC23
*1U/10V_4X
PC24
0.01U/50V_4X
PC25
0.01U/50V_4X
PR23
2.21K/F_6
PR27
100_4
ICMNT {32}
PC26
10U/6.3V_8X
Quanta Computer Inc.
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Document Number
CHARGER-ISL88731C
Rev
1A
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P2

MAIND {22,37,41}
S5D {41}
{3} SYS_SHDN#
PR29 *0_4/S
39K/F_4 PR30
VL
VIN
PR31 *0_4/S
PR32 *0_4/S
5V_EN
3V_EN

PC28 *0.1U/25V_4X
PC29 *2200P/50V_4X
PC30 10U/25V_8X

f : 400k Hz
ESR : 17mΩ
Total capacitor : 370 uF
(Peak 9.479A ,AVG 6.635A)
OCP:10.25A

+5VPCU
10.10.05 delete JP
PC40 *10U/6.3V_8X
PC41 330U/6.3V_105CS_E17f
10.10.20 change Value U:C2A
PL5 1.5UH_7X7
PR38 *15.8K/F_4
PR39 *2.2/F_6
PR40 0_4
PC44 *1000P/50V_4X
10.10.13 U:C2A

PQ8 AON7410
PQ10 AON7702
RDSon=14m ohm

10.10.11 add
PD12 UDZSTE-175.6B
U:C2A V:B2A
PR33 150K/F_4
PC35 0.1U/50V_6X
PR142 147K/F_4
U:C2A V:B2A

PC34 4.7U/10V_6X
PC37 0.1U/25V_4X
PC36 1U/16V_6X
REF
10.10.11 add
PR139 0_4
U:C2A V:B2A

10.10.14 change net Name
PU2 PM6686TR
LDOREFIN LDO VIN NC ONLDO VCC TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DL1 PVCC NC GND PGND TON BST2

+5VPCU
PR35 255K/F_6
DDPWRGD_R
5V_EN
5V_DH
5V_LX
5V_DL
PC45 0.1U/50V_6X
PR43 1/F_6
PR41 1/F_6
PC43 0.1U/50V_6X
10.10.20 change Value
3V_DL

VL
PC46 1U/16V_6X
PR44 0_6/S U:E3A

PD6 BAV99W-7-F
PC47 0.1U/50V_6X
PC48 0.1U/25V_4X
PD7 BAV99W-7-F
PC49 0.1U/50V_6X
PR46 22_8
+15V
+15V_ALWP
PC50 0.1U/25V_4X

PC31 *0.1U/25V_4X
PC32 E@0.1U/25V_4X
PC33 10U/25V_8X
VIN

f : 500k Hz
ESR : 17mΩ
Total capacitor : 342uF
(Peak 11.921A, AVG 8.345A)
OCP:12.52~12.23A

PQ7 AON7410
PQ9 AON7702
PR34 300K/F_6
REFIN2
SKIP
DDPWRGD_R
3V_EN
3V_DH
3V_LX
10.10.19 change Value U:C2A
RDSon=14m ohm

10.10.20 change Value U:C2A
PL4 1.5UH_7X7
PR36 *2.2/F_6
PC42 *1000P/50V_4X
+3VPCU
10.10.05 delete JP
PR37 *6.8K/F_4
PC38 330U/6.3V_105CS_E17f
PC39 *10U/6.3V_6X
PR42 *10K/F_4
10.10.13 U:C2A

+3VPCU
U:C2A
PR45 *100K_4
DDPWRGD_R
SYS_HWPG {7,32}

+5VPCU
S5D
PQ12 AO6402A
+5V_S5
(Peak 1A, AVG 0.7A)

+5VPCU
MAIND
PQ13 AO6402A
+5V
(Peak 3.5A, AVG 2.4A)

+3VPCU
S5D
PQ11 AO6402A
+3V_S5
(Peak 0.35A, AVG 0.25A)

+3VPCU
MAIND
PQ14 AO6402A
+3V
(Peak 6A, AVG 4.2A)

Quanta Computer Inc.
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Size	Document Number	Rev
	System 3V/5V(RT8210B)	1A
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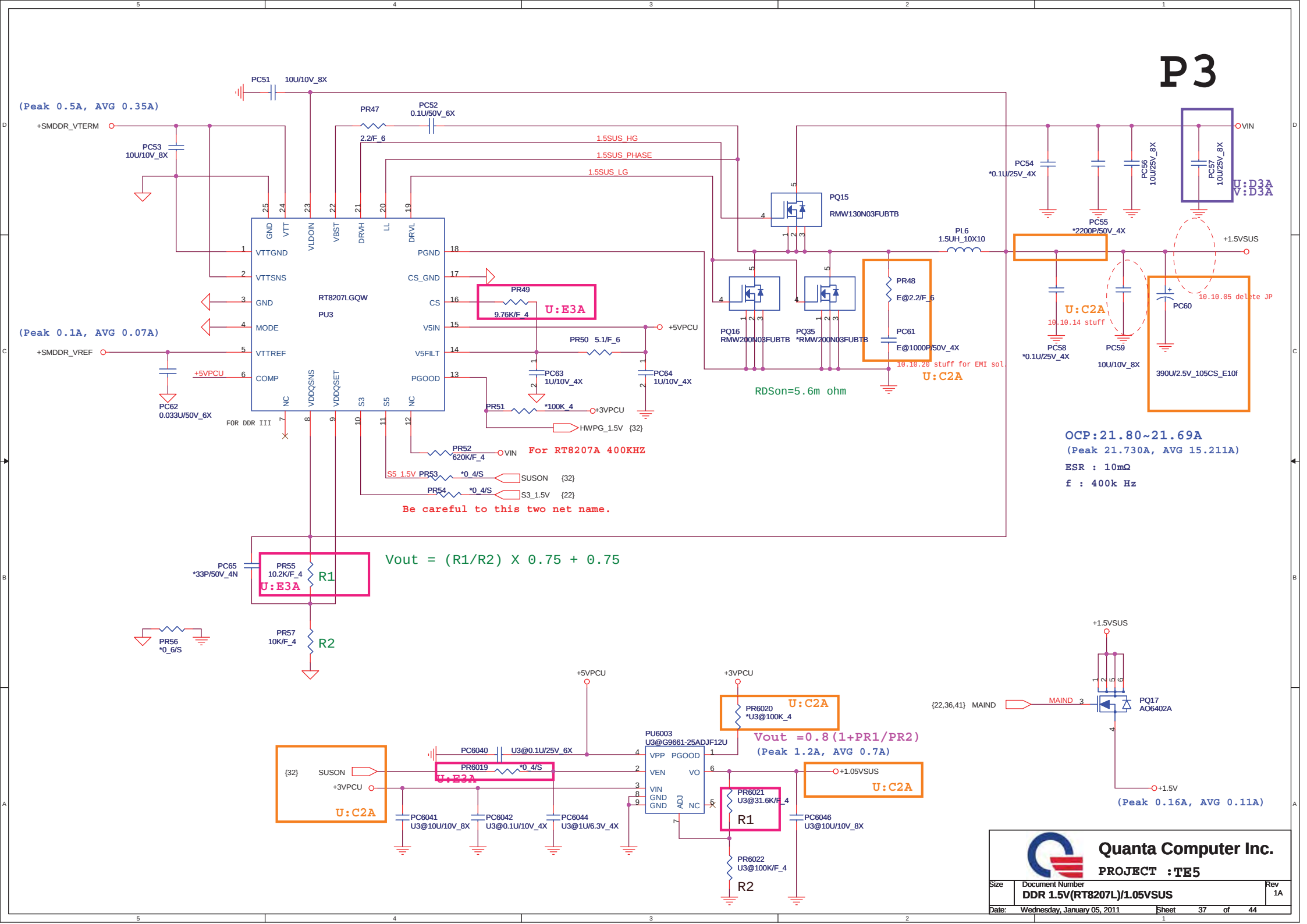
P3



Quanta Computer Inc.		
PROJECT : TE5		
Size	Document Number: DDR 1.5V(RT8207L)/1.05VSUS	Rev: 1A
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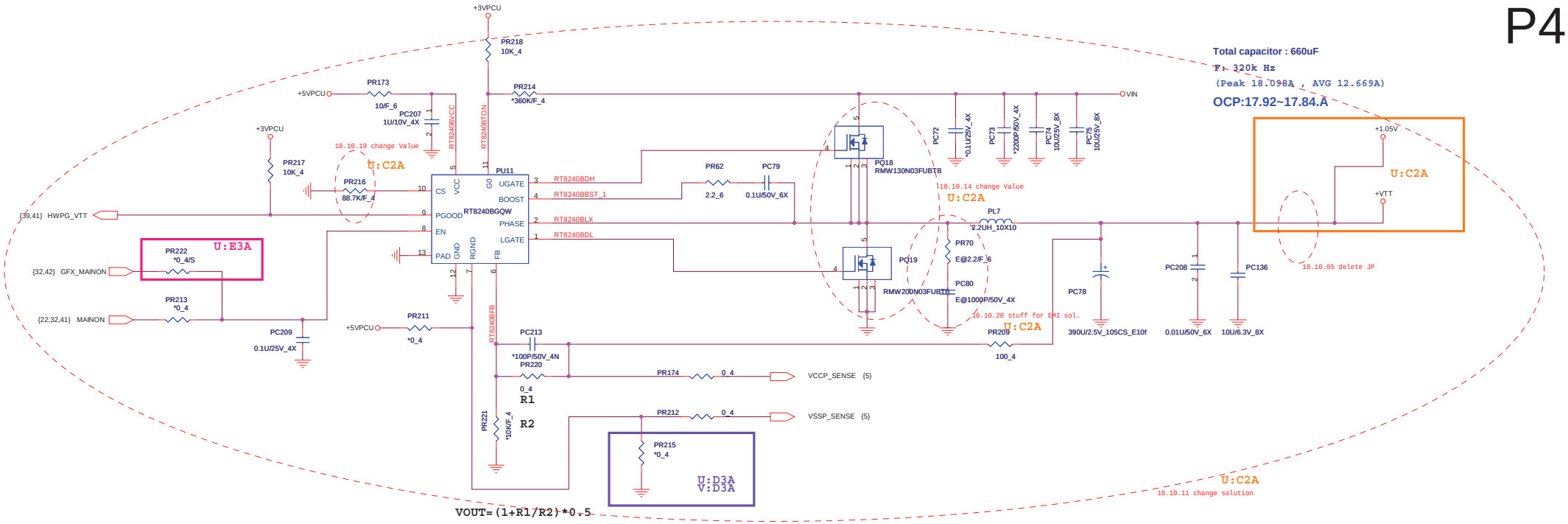
P4
Total capacitor : 660uF
F: 320k Hz
(Peak 18.098A , AVG 12.669A)
OCP:17.92~17.84A
+3VPCU
PR218 10K_4
+5VPCU
PR173 10/F_6
PC207 1U/10V_4X
PR214 *360K/F_4
VIN
PR217 10K_4
PR216 88.7K/F_4
10.10.19 change Value
U:C2A
RT8240BVCC
RT8240BTON
PU11
RT8240BGQW
CS
VCC
G0
UGATE
BOOST
PHASE
LGATE
PGOOD
EN
PAD
GND
RGND
FB
RT8240BDH
RT8240BBST_1
RT8240BLX
RT8240BDL
PR62 2.2_6
PC79 0.1U/50V_6X
PQ18 RMW130N03FUBTB
PC72 *0.1U/25V_4X
PC73 *2200P/50V_4X
PC74 10U/25V_8X
PC75 10U/25V_8X
10.10.14 change Value
U:C2A
PL7 2.2UH_10X10
PQ19 RMW200N03FUBTB
PR70 E@2.2/F_6
PC80 E@1000P/50V_4X
10.10.20 stuff for EMI sol.
U:C2A
PC78 390U/2.5V_105CS_E10f
PC208 0.01U/50V_6X
PC136 10U/6.3V_8X
+1.05V
+VTT
U:C2A
10.10.05 delete JP
{39,41} HWPG_VTT
PR222 *0_4/S
U:E3A
{32,42} GFX_MAINON
PR213 *0_4
{22,32,41} MAINON
PC209 0.1U/25V_4X
PR211 *0_4
PC213 *100P/50V_4N
PR220 0_4
R1
R2
PR221 *10K/F_4
PR174 0_4
VCCP_SENSE {5}
PR212 0_4
VSSP_SENSE {5}
PR215 *0_4
U:D3A
V:D3A
PR209 100_4
U:C2A
10.10.11 change solution
VOUT=(1+R1/R2)*0.5
Quanta Computer Inc.
PROJECT : TE5
Size
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+VTT /+1.05V(RT8238A)
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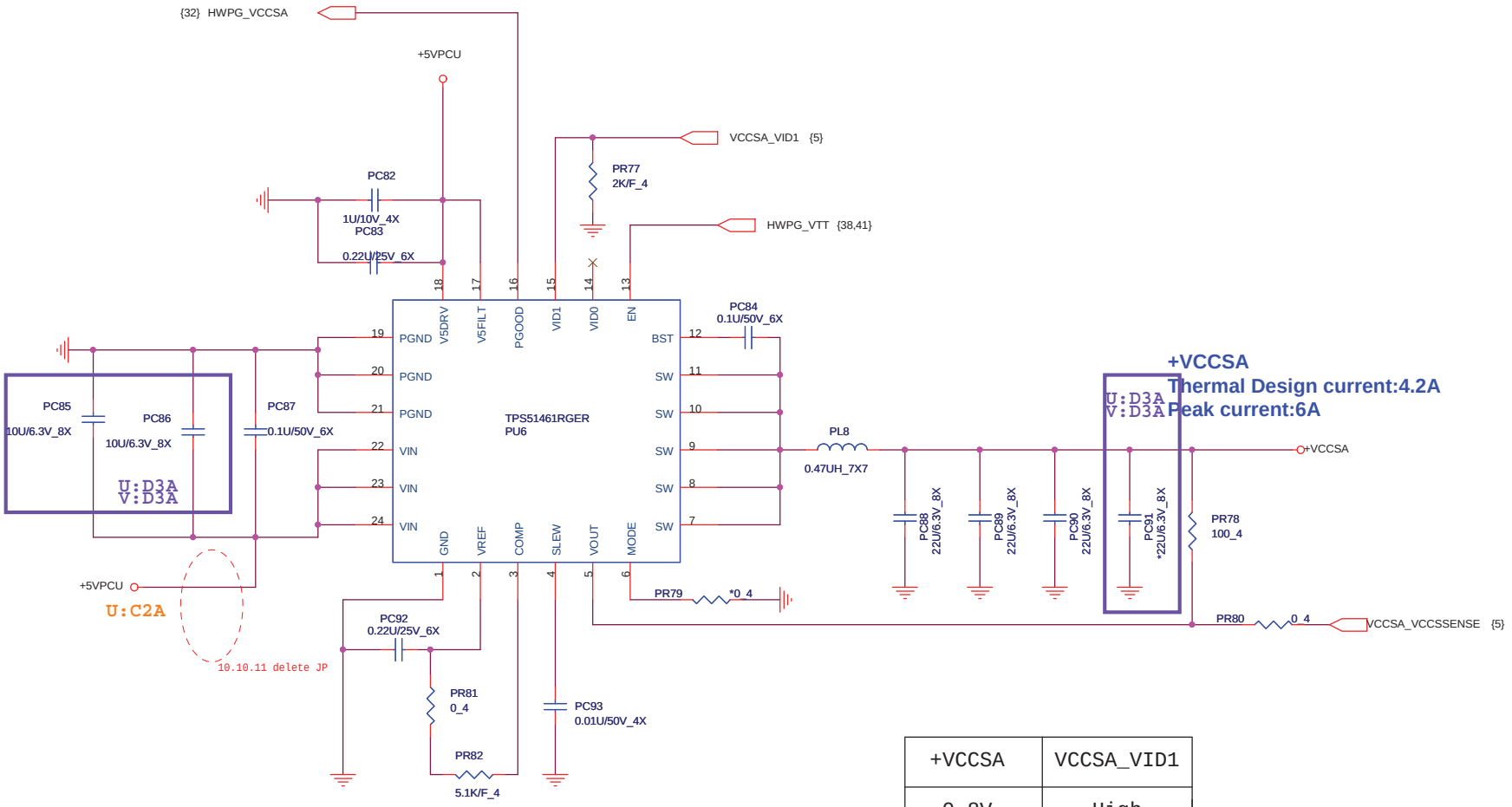

+VCCSA	VCCSA_VID1
0.8V	High
0.9V	Low

U:C2A

Quanta Computer Inc.

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	+VCCSA ISL95870A)	1A

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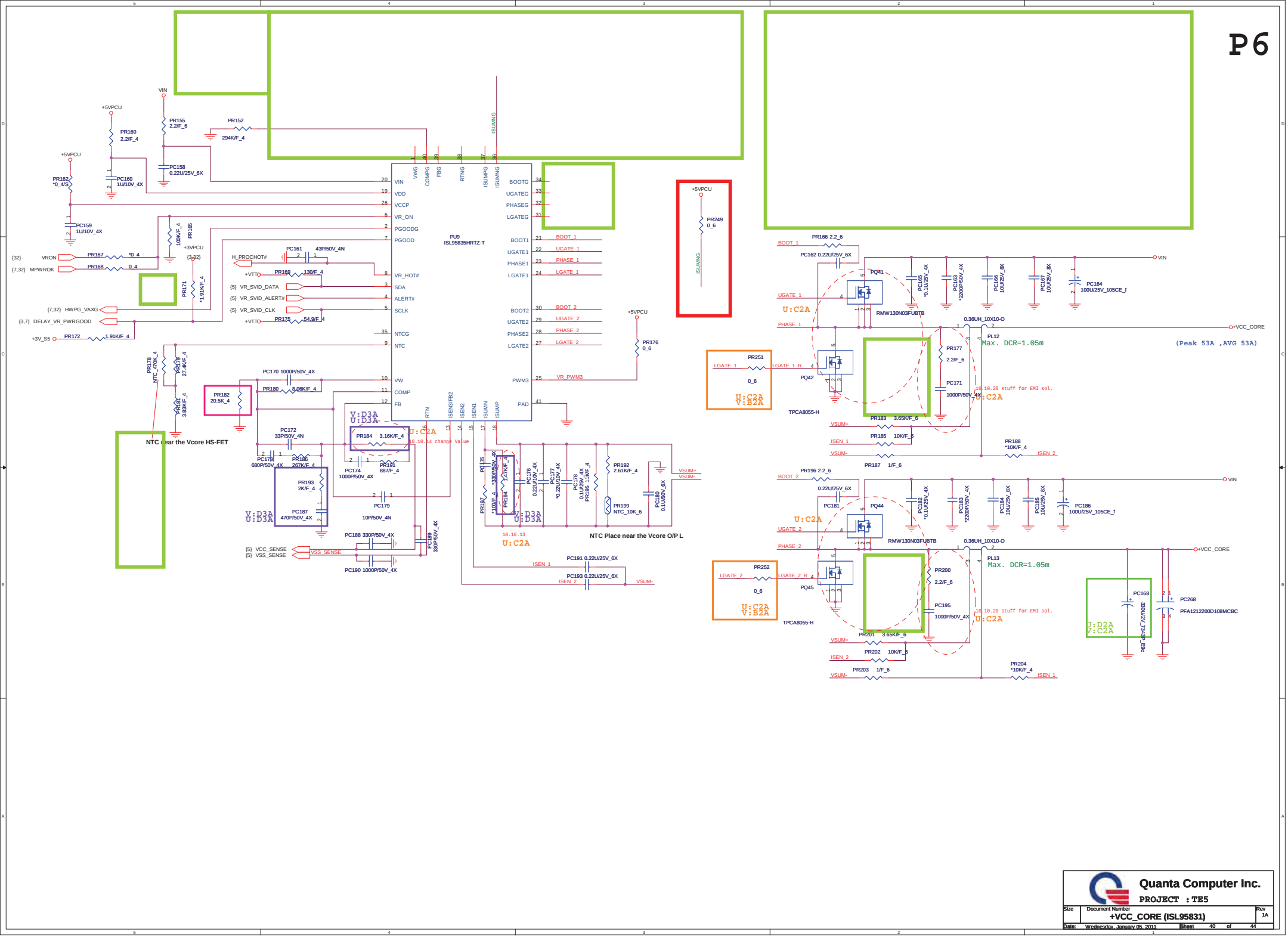
P6
PU9
ISL95835HRTZ-T
NTC near the Vcore HS-FET
NTC Place near the Vcore O/P L
TPCA8055-H
RMW130N03FUBTB
+VCC_CORE
Max. DCR=1.05m
(Peak 53A ,AVG 53A)
Quanta Computer Inc.
PROJECT : TE5
+VCC_CORE (ISL95831)
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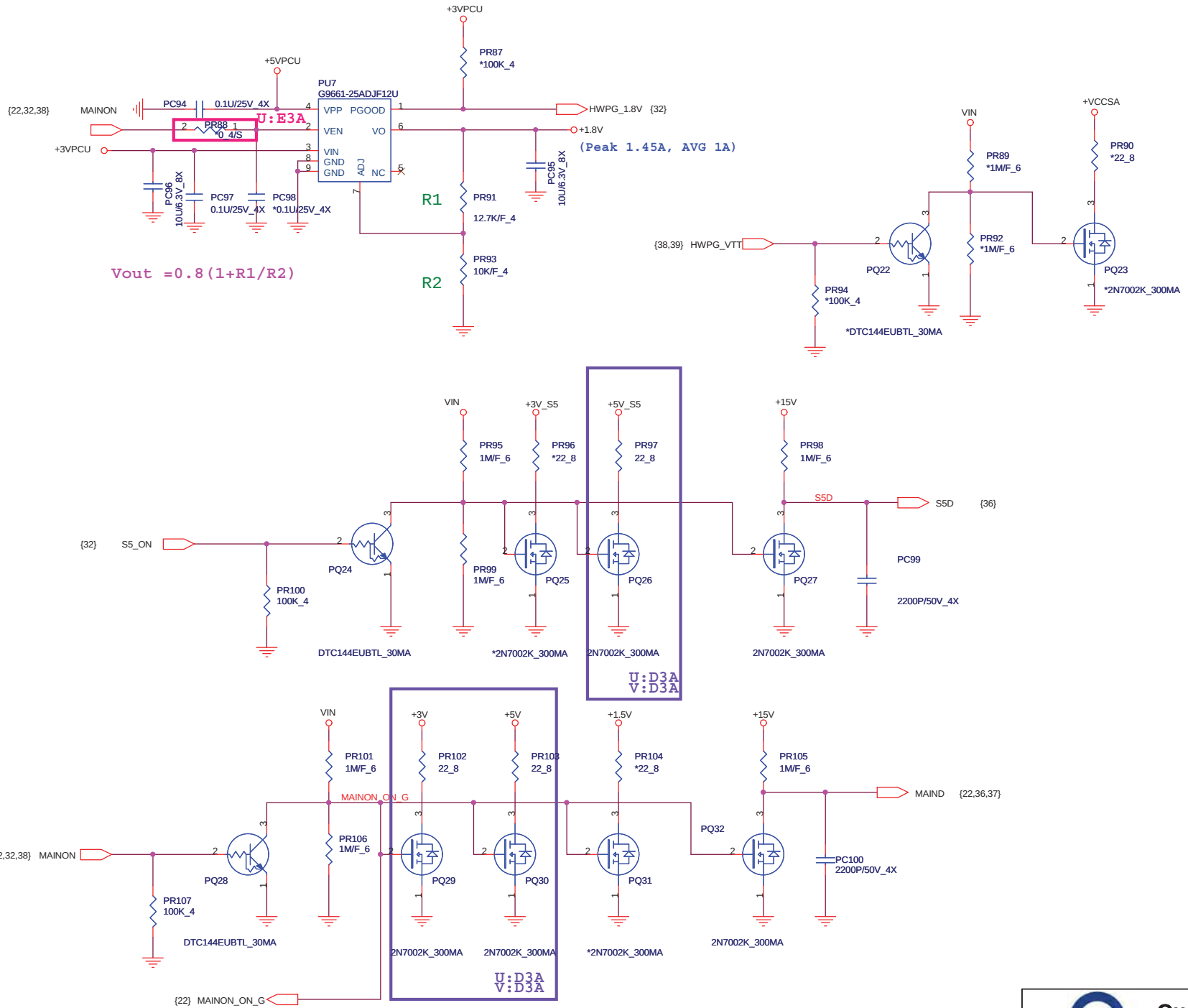

Quanta Computer Inc.		
PROJECT :TE5		
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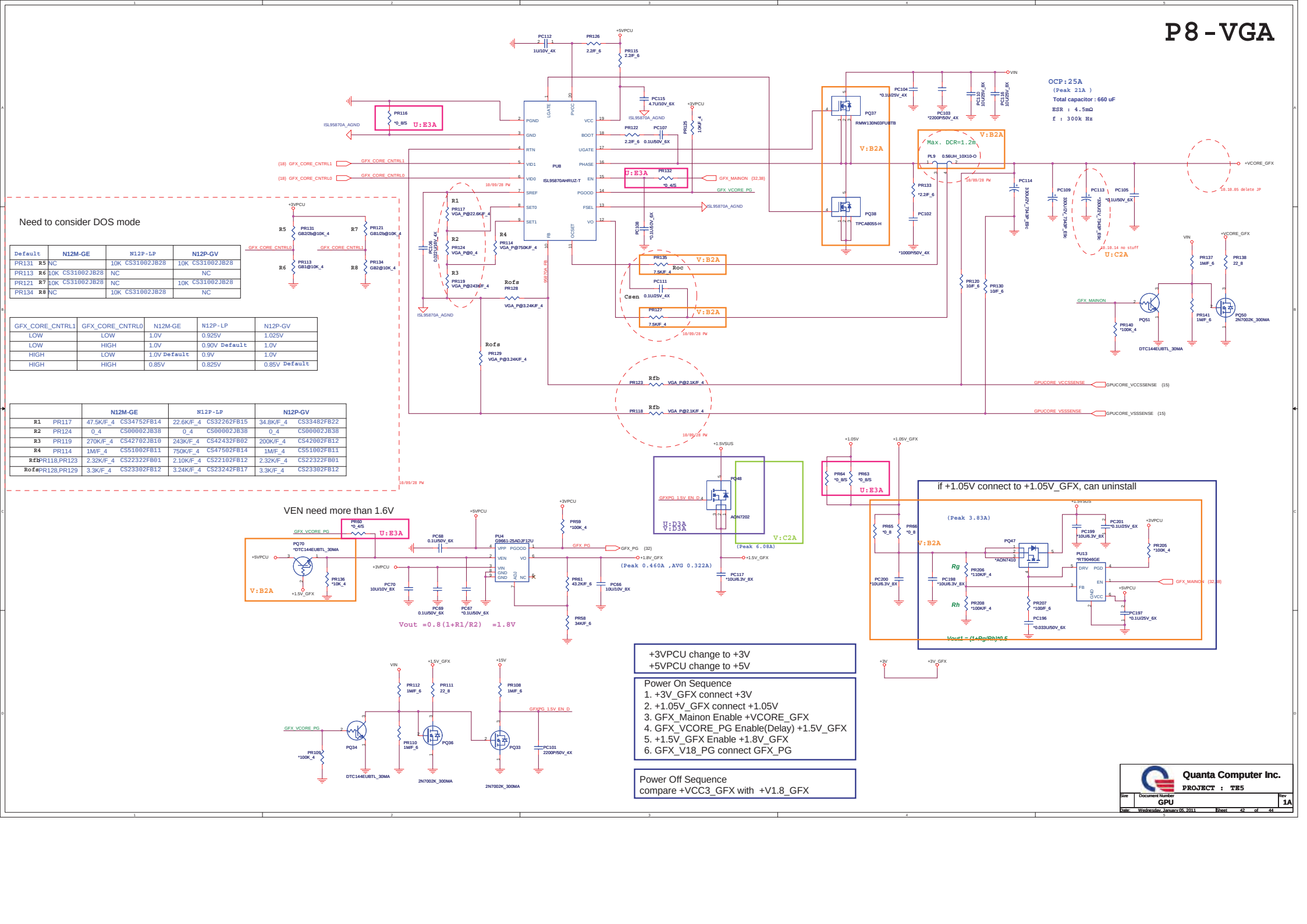
P8-VGA



Default	N12M-GE	N12P-LP	N12P-GV
PR131 R5	NC	10K CS31002JB28	10K CS31002JB28
PR113 R6	10K CS31002JB28	NC	NC
PR121 R7	10K CS31002JB28	NC	10K CS31002JB28
PR134 R8	NC	10K CS31002JB28	NC

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	N12M-GE	N12P-LP	N12P-GV
LOW	LOW	1.0V	0.925V	1.025V
LOW	HIGH	1.0V	0.90V Default	1.0V
HIGH	LOW	1.0V Default	0.9V	1.0V
HIGH	HIGH	0.85V	0.825V	0.85V Default

		N12M-GE	N12P-LP	N12P-GV
R1	PR117	47.5K/F_4 CS34752FB14	22.6K/F_4 CS32262FB15	34.8K/F_4 CS33482FB22
R2	PR124	0_4 CS00002JB38	0_4 CS00002JB38	0_4 CS00002JB38
R3	PR119	270K/F_4 CS42702JB10	243K/F_4 CS42432FB02	200K/F_4 CS42002FB12
R4	PR114	1M/F_4 CS51002FB11	750K/F_4 CS47502FB14	1M/F_4 CS51002FB11
Rfb	PR118,PR123	2.32K/F_4 CS22322FB01	2.10K/F_4 CS22102FB12	2.32K/F_4 CS22322FB01
Rofs	PR128,PR129	3.3K/F_4 CS23302FB12	3.24K/F_4 CS23242FB17	3.3K/F_4 CS23302FB12

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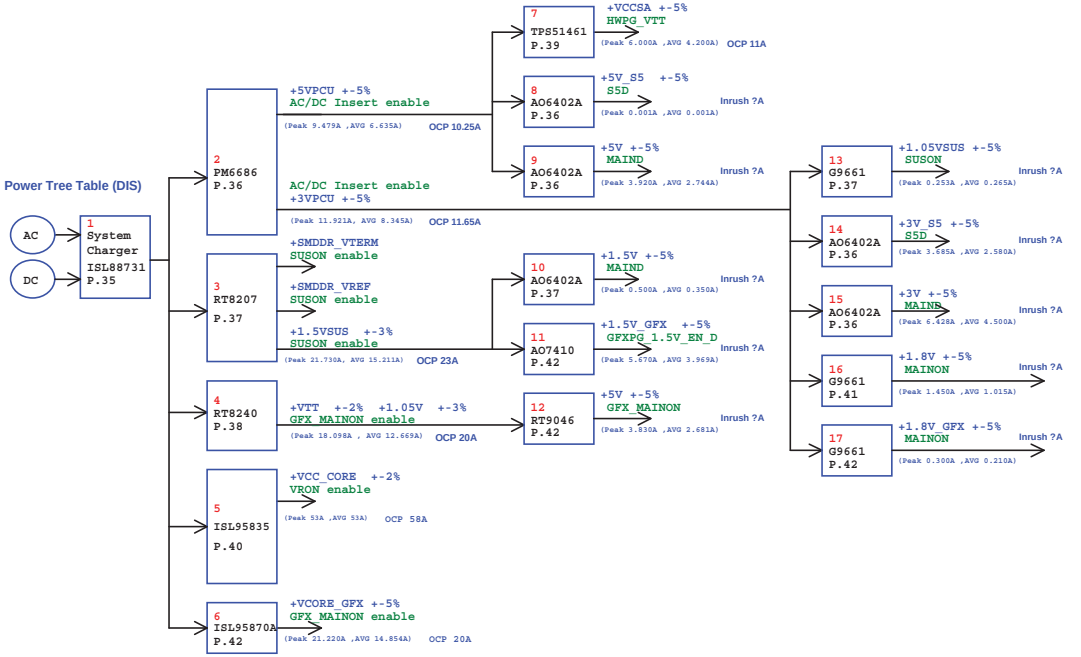
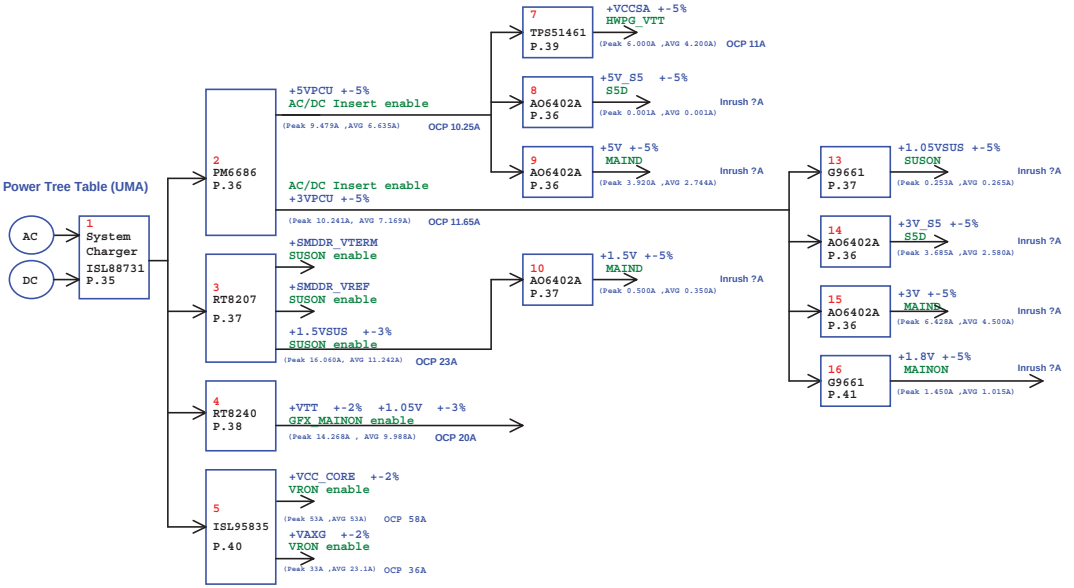
Power Tree Table (DIS)



Power Tree Table (UMA)



Power Distribution List

Power	Distribution

Quanta Computer Inc.
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Model	REV	CHANGE LIST
TE5 MB	1A	PAGE 3: (UMA)--R52 change to 25.5/F_4
		PAGE 5: (UMA)--C183,C190,C195 change to 10U/6.3V_8X
		PAGE 7: (UMA)--R224,R197 change to NC
		PAGE 9: (UMA)--PCIE_CLK_USB30_REQ#, R138 pull up to +3V_S5
		PAGE 9: (UMA)--PCIE_CLK_MINI_REQ#, R237 pull up to +3V
		PAGE 9: (UMA)--R199 NC
		PAGE 9: (UMA)--Q30, Q62 NC
		PAGE 10: (UMA)--add TP31
		PAGE 10: (UMA)--change Board ID9 strap Function name
		PAGE 11: (UMA)--C252 change to 10U/6.3V_8X
		PAGE 11: (UMA)--Net +1.05V change to +VTT
		PAGE 11: (UMA)--R117,R182,R114 change to 10K_4
		PAGE 12: (UMA)--R190,R194,R110 change to 10K_4
		PAGE 23: (UMA)--C978 NC
		PAGE 23: (UMA)--R66,R412,R154,Q45 change Function code to HM@ and delete discrete HDMI-HPD reference
		PAGE 24: (UMA)--add D7
		PAGE 25: (UMA)--add R201,R7,Q10
		PAGE 27: (UMA)--USB3.0 change to NEC solution
		PAGE 30: (UMA)--C97,C92,C106 change to 1U/10V_6Y
		PAGE 31: (UMA)--CN21 Foot-print change to 3in1-cm35-5-21p
		PAGE 32: (UMA)--3ND_MBCLK,3ND_MBDATA R269,R270 pull up to +3V
		PAGE 32: (UMA)--add 13MS,14MS,15MS Strap pin SKU_STRAP_1,SKU_STRAP_2,SKU_STRAP_3
		PAGE 33: (UMA)--add PR1
		PAGE 34: (UMA)--LED1,LED4,LED5,LED6 change symbol and Foot-print
		PAGE 16: (VGA)--add R3712
		PAGE 19: (VGA)--R3711 change to 47U/6.3V_1206X
		PAGE 25: (ALL)--Net name PCIE_CLK_3G_REQ# change to PCIE_CLK_3G_REQ#_C
		PAGE 22: (ALL)--add R65
		PAGE 37: (ALL)--PC60 change to CC7390JMZ02
		PAGE 18: (VGA)--add R3601, R3575
		PAGE 24: (UMA)--CN4 Value change to 87213-2000G
		PAGE 22: (ALL)--add R102
		PAGE 33: (ALL)--Remove K/B LED power circuit
	2A	PAGE 15: (VGA)--delete R3535,R3547
		PAGE 22: (ALL)--add R31
		PAGE 22: (ALL)--add R102
		PAGE 40: (ALL)--add PC168
		PAGE 32: (ALL)--13MS,14MS,15MS Strap pull up voltage change to +3VPCU
		PAGE 34: (ALL)--add R213
		PAGE 42: (VGA)--add PQ49

MODEL TE5

PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
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14	1A	
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24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	

DOC NO. 204					
PROJECT MODEL :	TE5	APPROVED BY:	Andy Wang	DATE:	2010/10/01
PART NUMBER:		DRAWING BY:	Andy Wang	REVISON:	1A

Quanta Computer Inc.
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CHANGE LIST

Model	REV	
TE5 MB	1A	PAGE 35: (COM)--add PC76 and PC77 for EMI Sol. (101005) PAGE 35~42: (COM)--delete PJP1 , PJP2 , PJP3 , PJP14 , PJP6 , PJP9 (101005) PAGE 38: (COM)--PC212 change to 0.1U/25V_6X (101005) PAGE 38: (COM)--PC216 change to 1.74K/F_4 (101005) PAGE 40: (COM)--PC153 and PC154 change to 330U/2V_7343P_E9C (101005) PAGE 36: (COM)--add PD12 , PR142 , PR139 (101011) PAGE 38: (COM)--Change VTT/1.05V solution (101011) PAGE 37: (COM)--PC59 stuff (101014) PAGE 38: (COM)--Change PQ18 and PQ19 Value (101014) PAGE 40: (COM)--Change PR184 Value ; PC151 stuff (101014) PAGE 42: (COM)--PC113 no stuff (101014) PAGE 35 , 37 , 38 , 40: (COM)--PR14 , PC19 , PR48 , PC61 , PR70 , PC80 , PR159 , PC157 , PR177 , PC171 , PR200 , PC195 stuff (101020) PAGE 36: (COM)--PU2 , PL4 , PL5 change Value (101020)	

MODEL TE5

PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
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30	1A	

DOC NO. 204					
PROJECT MODEL :	TE5	APPROVED BY:	Andy Wang	DATE:	2010/10/01
PART NUMBER:		DRAWING BY:	Andy Wang	REVISON:	1A

Quanta Computer Inc.
PROJECT : TE5
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