EW6

CPU CORE Page:26 — VCC_CORE

+3VPCU / +3V_S5/+3VSUS / +3V / +5VSUS/+5V / +12V Page:24 — +3VPCU, +3V_S5, +3VSUS, +3V, +5VSUS, +5V, +12V

+1.8VSUS/+1.8V / +1.2V / SMDDR_VTERM Page:27 — +1.8VSUS, +1.8V, +1.2V, SMDDR_VTERM

+1.8V_S5 / +1.5V / VTT Page:23 — +1.8V_S5, +1.5V, VTT

BATTERY CHARGER Page:25

Power State Table

Power Name	Control Signal	Power State
VCC_CORE	VRON	S0
+3VPCU	N/A	ALWAYS
+3V_S5	S5_ON	S0-S5
+3VSUS	SUSON	S0-S3
+3V	MAINON	S0
+5VSUS	SUSON	S0-S3
+5V	MAINON	S0
+12V	MAINON	S0
+1.2V	MAINON	S0
VTT	MAINON	S0
SMDDR_VTERM	MAINON	S0
+1.8V_S5	S5_ON	S0-S5
+1.8VSUS	SUSON	S0-S3
+1.8V	MAINON	S0
+1.5V	MAINON	S0

CLOCK GEN ICS951413CGLFT Page:4

CELERON-M/PENTIUM-M INTEL Mobile_479 CPU Page:2, 3

HOST BUS 400MHZ

NB ATi RC410MB/RC410MD Page: 5, 6 , 7, 8

- RGB → **CRT** Page: 15
- LVDS → **LVDS** Page: 15
- S-VIDEO → **TV-OUT** Page: 15
- DDR-II → **DDR-II SODIMM1** Page: 13, **DDR-II SODIMM2** Page: 13

2X PCIE

SB ATi SB400 Page: 9, 10, 11, 12

Manufacturing Option

- SATA → **SATA HDD** Page: 16
- ATA 66/100 → **PATA HDD** Page: 16
- ATA 66/100 → **IDE-ODD** Page: 16
- AC97 → **AUDIO CODEC** CONEXANT 20468-31 Page: 18
  - **AMP** MAX9750 Page: 19
  - **MODEM** CONEXANT 20493-21 Page: 18
  - **MIC IN** Page: 18
  - **SPEAKER** Page: 19
  - **LINE OUT** Page: 19
  - **RJ11** Page: 14

PCI BUS 33MHZ

- **TI PCMCIA** PCI1510A — AD17, REQ3# / GNT3#, INTE# Page: 17 → **TYPE II SLOT** Page: 17
- **MINI-PCI** Wireless LAN — AD20, REQ1# / GNT1#, INTB# , INTC# Page: 22
- **REALTEK** RTL8100CL Page: 14 → **BOTHHAND** TRANSFORMER NS0013 Page: 14 → **RJ45** Page: 14

USB 2.0

- **SYSTEM USB PORT *3** Page: 20 — USB2,3,5

LPC 33MHZ

KBC NS PC97551 Page: 21

- **Touchpad** Page: 22
- **Keyboard** Page: 22
- **FLASH** Page: 21
- **FAN** Page: 22

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Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

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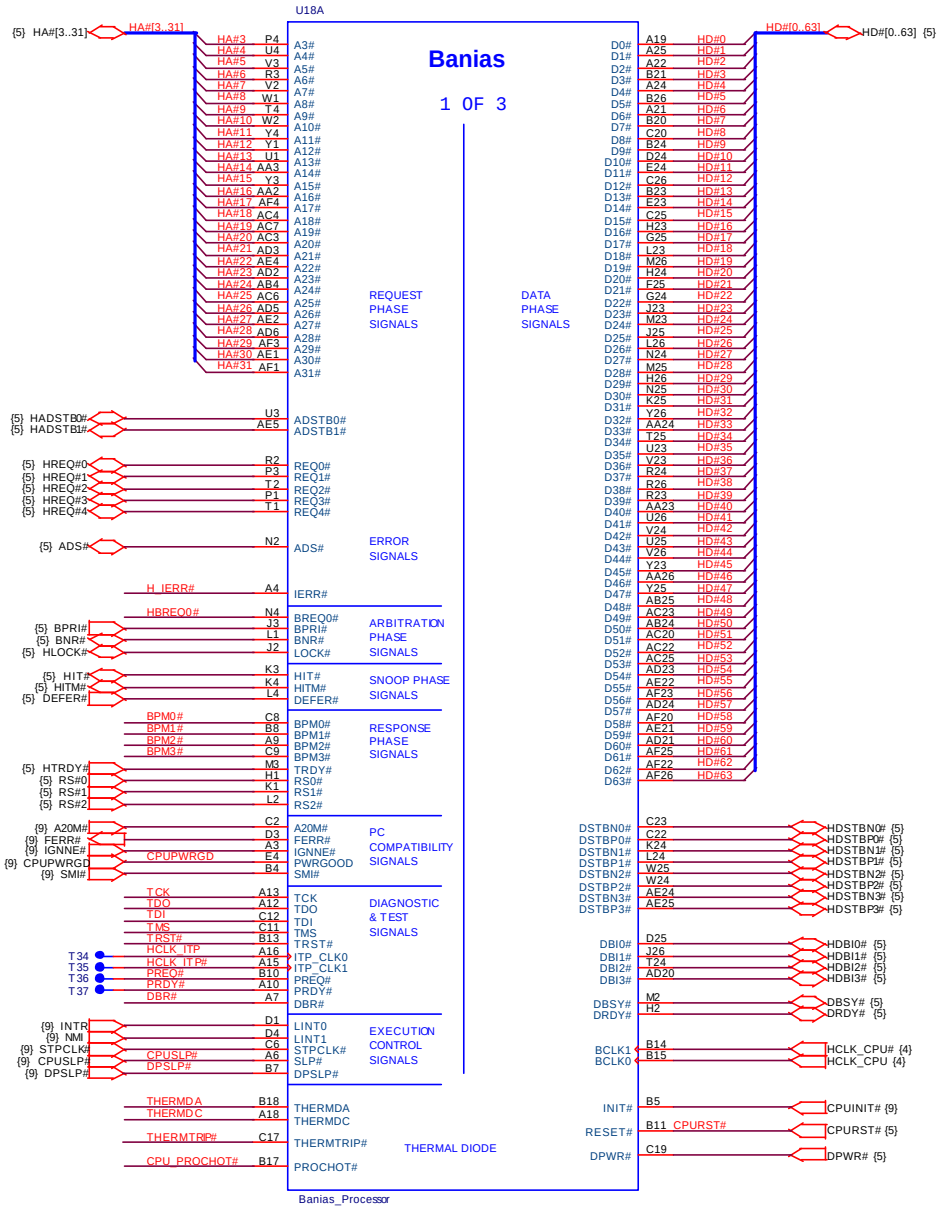
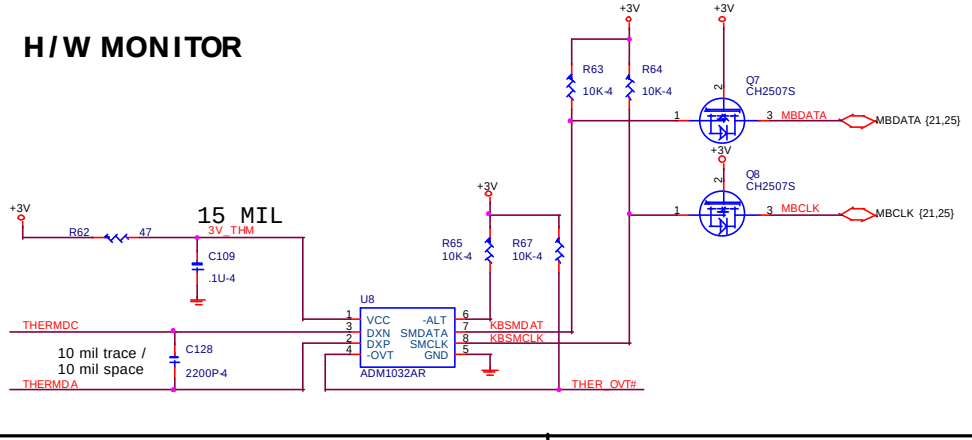
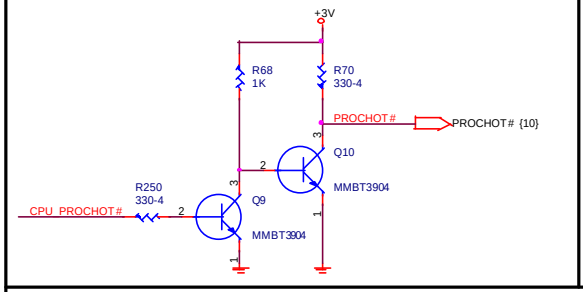
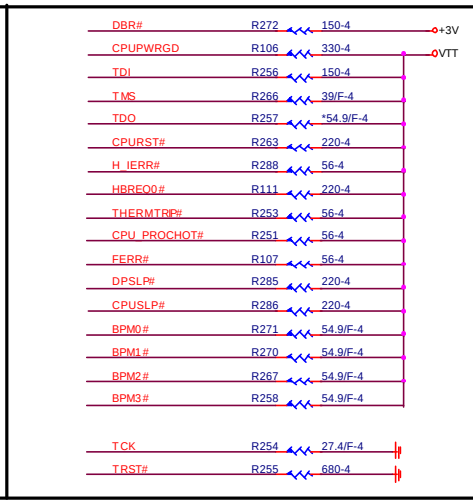
CPU

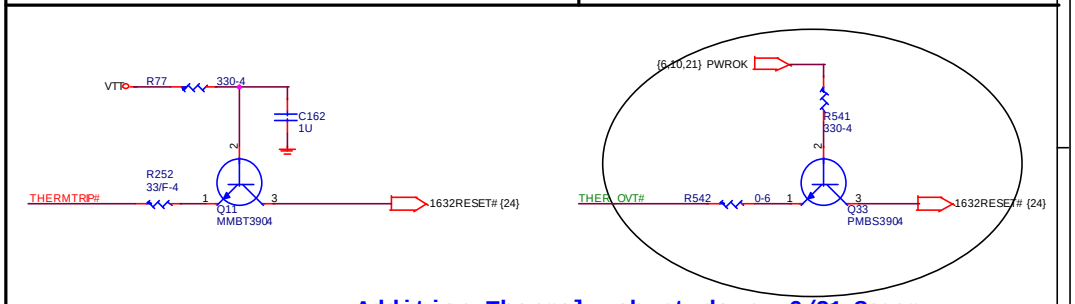


H/W MONITOR



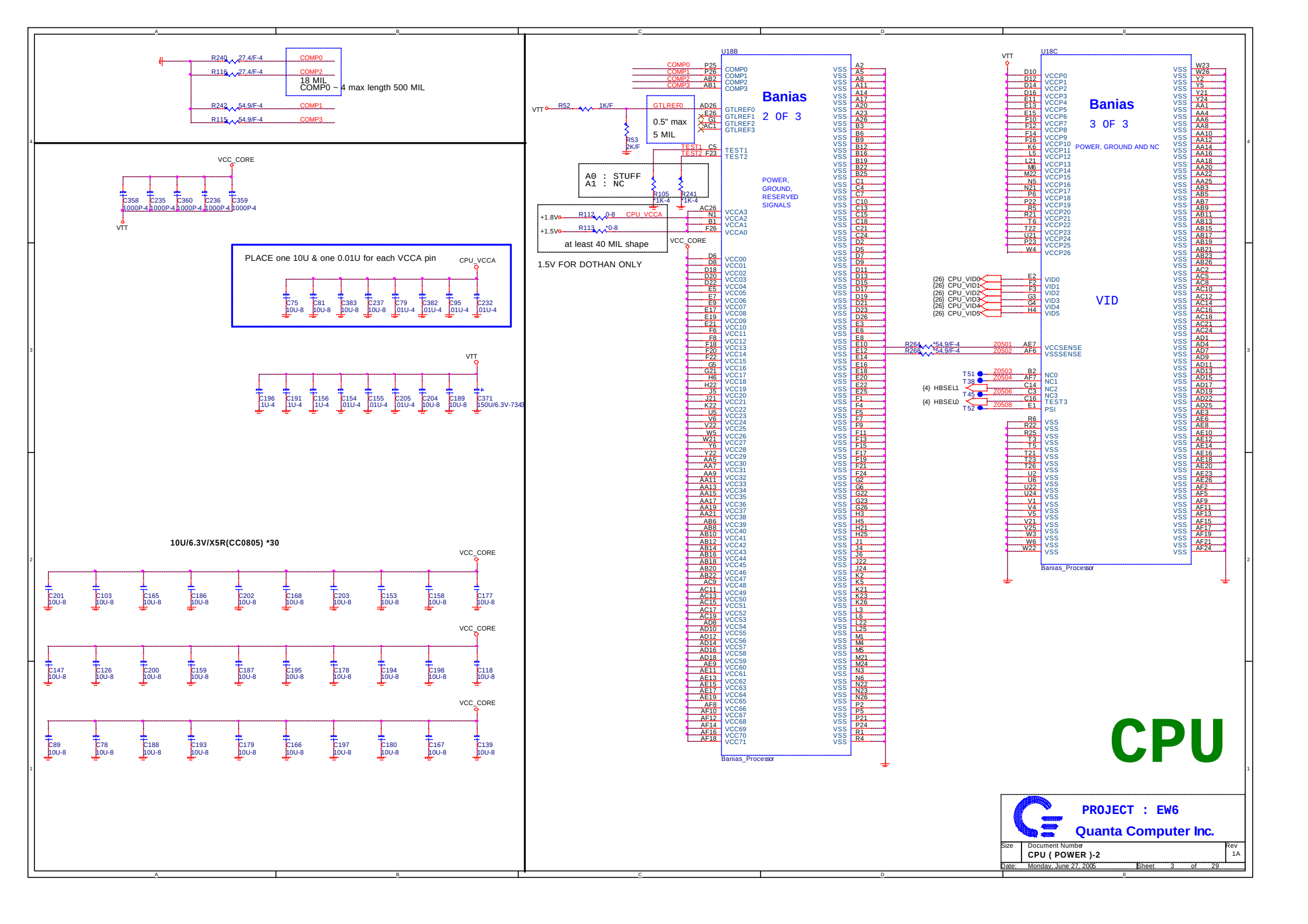






Addition Thermal shunt down 6/21 Sagem

PROJECT : EW6		
Quanta Computer Inc.		
Size	Document Number: CPU (HOST BUS)-1	Rev: 3A
Date: Monday, June 27, 2005	Sheet 2 of 29	


R240 27.4/F-4 COMP0
R116 27.4/F-4 COMP2
18 MIL
COMP0 ~ 4 max length 500 MIL
R242 54.9/F-4 COMP1
R115 54.9/F-4 COMP3
VCC_CORE
C358 1000P-4
C235 1000P-4
C360 1000P-4
C236 1000P-4
C359 1000P-4
VTT
PLACE one 10U & one 0.01U for each VCCA pin
CPU_VCCA
C75 10U-8
C81 10U-8
C383 10U-8
C237 10U-8
C79 01U-4
C382 01U-4
C95 01U-4
C232 01U-4
VTT
C196 1U-4
C191 1U-4
C156 1U-4
C154 01U-4
C155 01U-4
C205 01U-4
C204 10U-8
C189 10U-8
C371 150U/6.3V-7343
10U/6.3V/X5R(CC0805) *30
VCC_CORE
C201 10U-8
C103 10U-8
C165 10U-8
C186 10U-8
C202 10U-8
C168 10U-8
C203 10U-8
C153 10U-8
C158 10U-8
C177 10U-8
VCC_CORE
C147 10U-8
C126 10U-8
C200 10U-8
C159 10U-8
C187 10U-8
C195 10U-8
C178 10U-8
C194 10U-8
C198 10U-8
C118 10U-8
VCC_CORE
C89 10U-8
C78 10U-8
C188 10U-8
C193 10U-8
C179 10U-8
C166 10U-8
C197 10U-8
C180 10U-8
C167 10U-8
C139 10U-8
U18B
Banias
2 OF 3
COMP0 P25
COMP1 P26
COMP2 AB2
COMP3 AB1
VTT
R52 1K/F
GTLREF0 AD26
0.5" max
5 MIL
R53 2K/F
TEST1 C5
TEST2 F23
A0 : STUFF
A1 : NC
R105 1K-4
R241 1K-4
+1.8V
R112 0-8 CPU_VCCA
+1.5V
R113 *0-8
at least 40 MIL shape
VCC_CORE
1.5V FOR DOTHAN ONLY
POWER, GROUND, RESERVED SIGNALS
Banias_Processor
U18C
Banias
3 OF 3
POWER, GROUND AND NC
VID
VCCSENSE
VSSSENSE
NC0
NC1
NC2
NC3
TEST3
PSI
Banias_Processor
CPU
PROJECT : EW6
Quanta Computer Inc.
Size
Document Number
CPU (POWER)-2
Rev
1A
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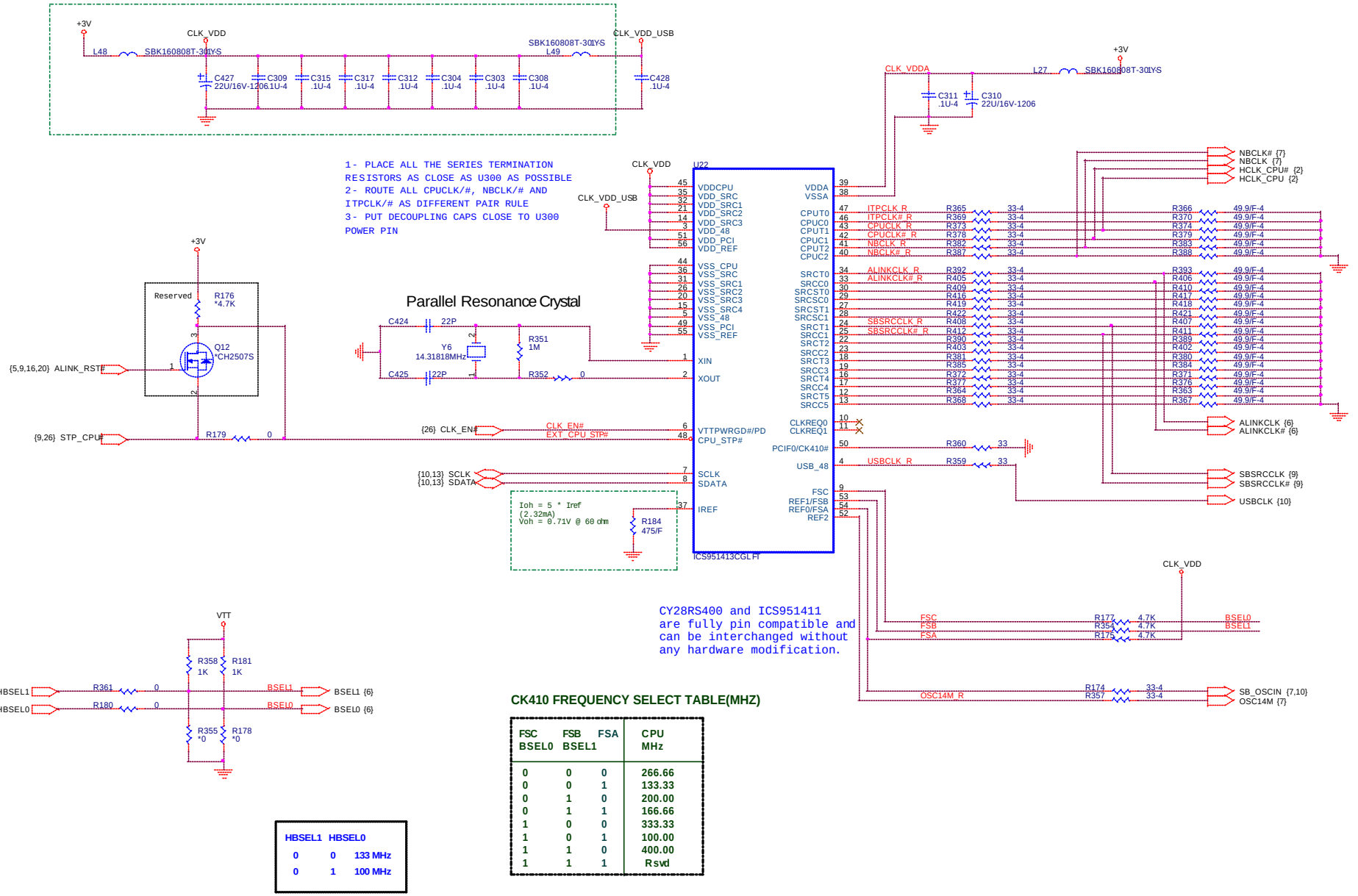
Sheet 3 of 29



CK410 FREQUENCY SELECT TABLE(MHZ)

FSC BSEL0	FSB BSEL1	FSA	CPU MHz
0	0	0	266.66
0	0	1	133.33
0	1	0	200.00
0	1	1	166.66
1	0	0	333.33
1	0	1	100.00
1	1	0	400.00
1	1	1	Rsvd

HBSEL1	HBSEL0	
0	0	133 MHz
0	1	100 MHz

CLK

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	EXTERNAL CLKGEN	1B

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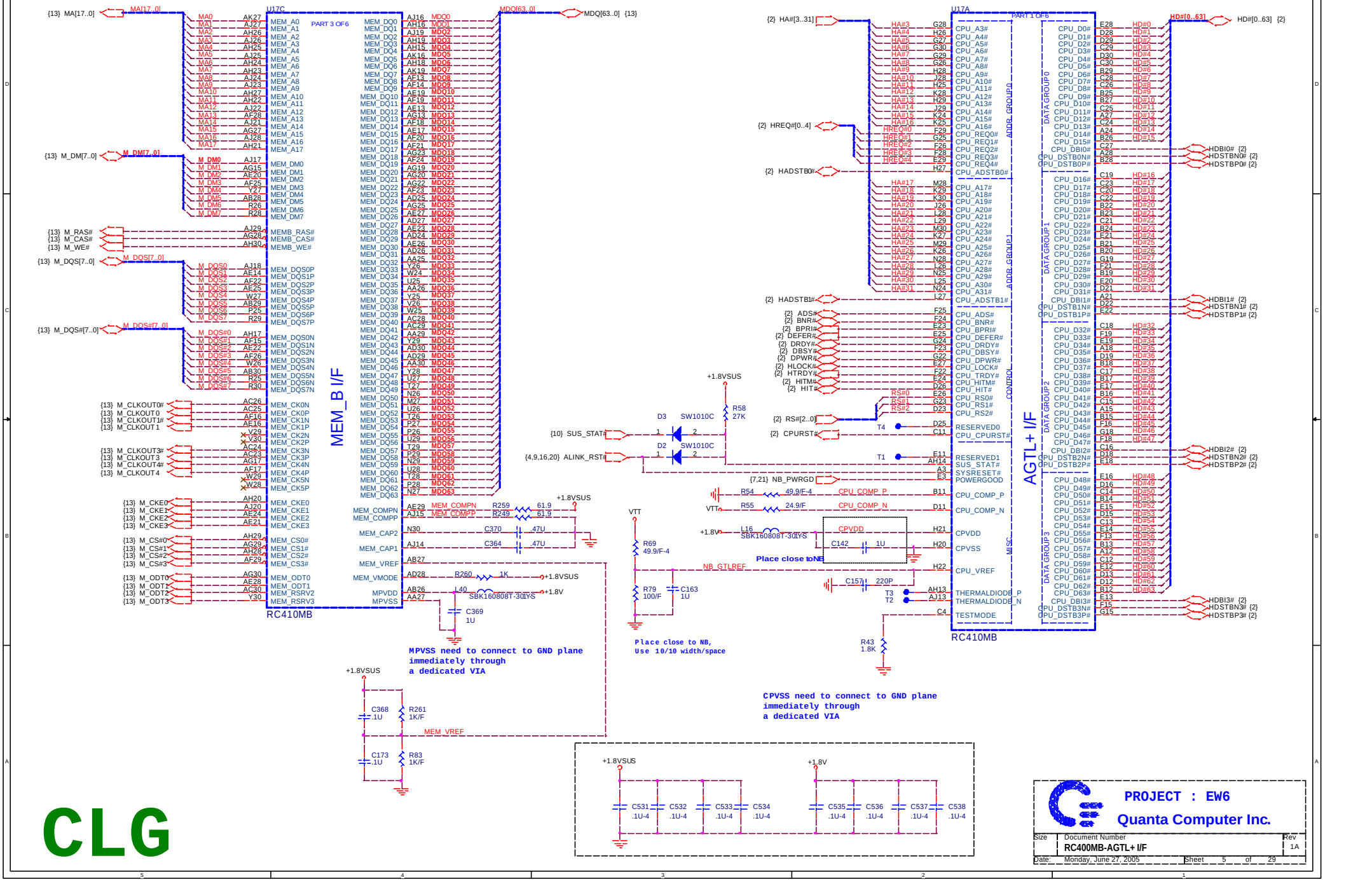
U17C
PART 3 OF6
MEM_B I/F
RC410MB
U17A
PART 1 OF 6
AGTL+ I/F
RC410MB
MA[17..0]
M_DM[7..0]
M_DQS[7..0]
M_DQS#[7..0]
MDQ[63..0]
HA#[3..31]
HREQ#[0..4]
HD#[0..63]
M_CLKOUT0#
M_CLKOUT0
M_CLKOUT1#
M_CLKOUT1
M_CLKOUT3#
M_CLKOUT3
M_CLKOUT4#
M_CLKOUT4
M_CKE0
M_CKE1
M_CKE2
M_CKE3
M_CS#0
M_CS#1
M_CS#2
M_CS#3
M_ODT0
M_ODT1
M_ODT2
M_ODT3
M_RAS#
M_CAS#
M_WE#
MEM_VREF
MEM_VMODE
MPVDD
MPVSS
+1.8VSUS
+1.8V
SUS_STAT#
ALINK_RST#
NB_PWRGD
VTT
NB_GTLREF
CPU_COMP_P
CPU_COMP_N
CPVDD
CPVSS
CPU_VREF
THERMALDIODE_P
THERMALDIODE_N
TESTMODE
HADSTB0#
HADSTB1#
ADS#
BNR#
BPRI#
DEFER#
DRDY#
DBSY#
DPWR#
HLOCK#
HTRDY#
HIT#
HITM#
RS#[2..0]
CPURST#
RESERVED0
RESERVED1
SUS_STAT#
SYSRESET#
POWERGOOD
HDBI0#
HDBI1#
HDBI2#
HDBI3#
HDSTBN0#
HDSTBP0#
HDSTBN1#
HDSTBP1#
HDSTBN2#
HDSTBP2#
HDSTBN3#
HDSTBP3#
Place close to NB
Place close to NB, Use 10/10 width/space
MPVSS need to connect to GND plane immediately through a dedicated VIA
CPVSS need to connect to GND plane immediately through a dedicated VIA
PROJECT : EW6
Quanta Computer Inc.
RC400MB-AGTL+ I/F
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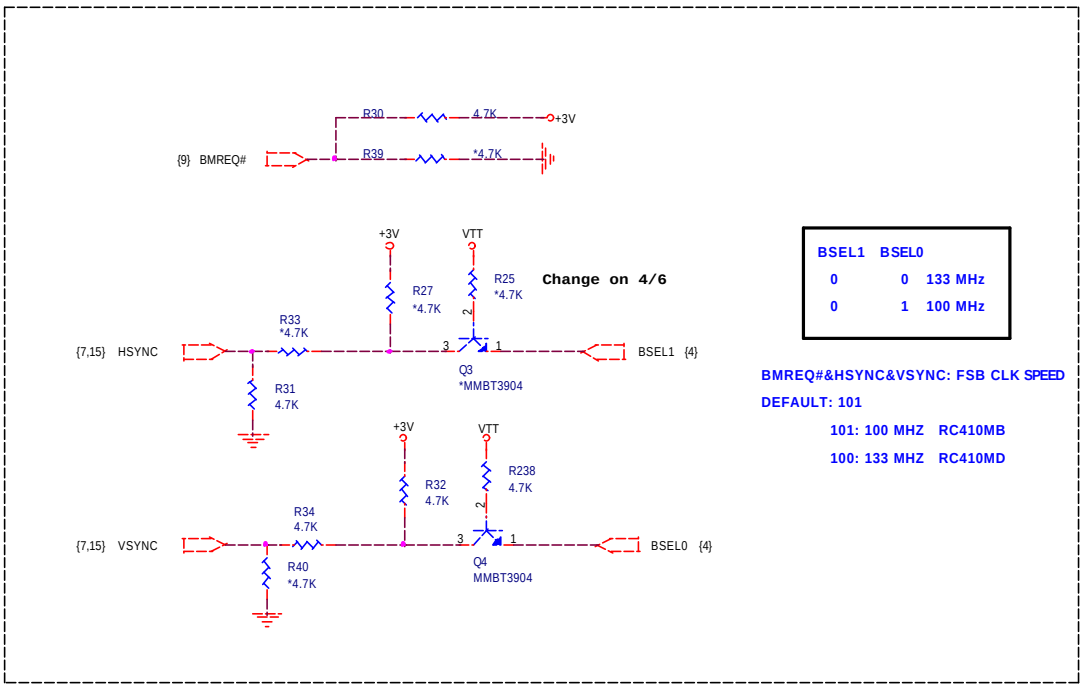
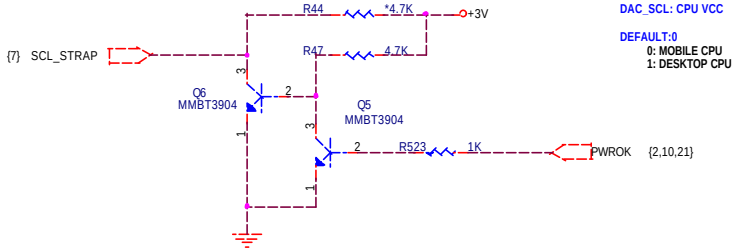
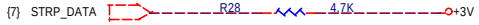
1A





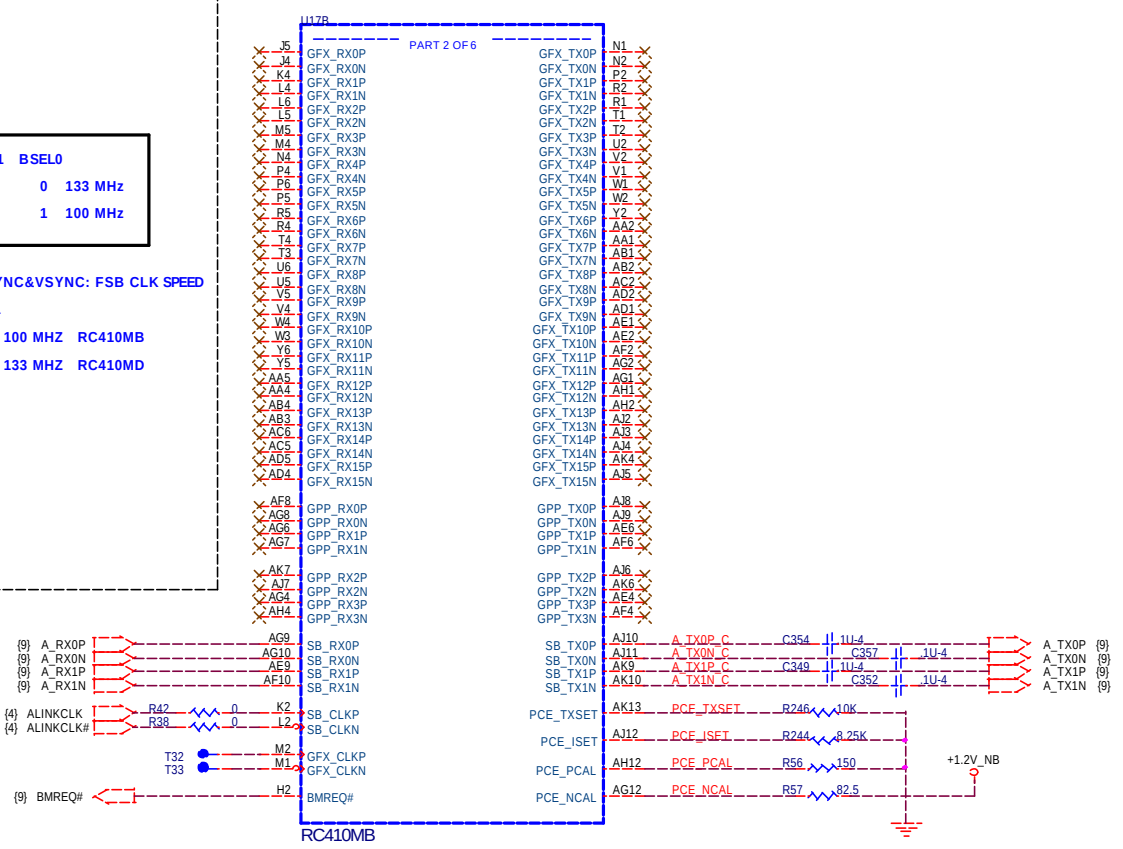
DAC_SCL: CPU VCC

DEFAULT:0
0: MOBILE CPU
1: DESKTOP CPU



STRP_DATA:Debug strap

DEFAULT:1
0: MEMORY CHANNEL STRAPING
1: E2PROM STRAPING



CLG

PROJECT : EW6

Quanta Computer Inc.

Size	Document Number	Rev
	RC400MB-PCIE LINK I/F	2A

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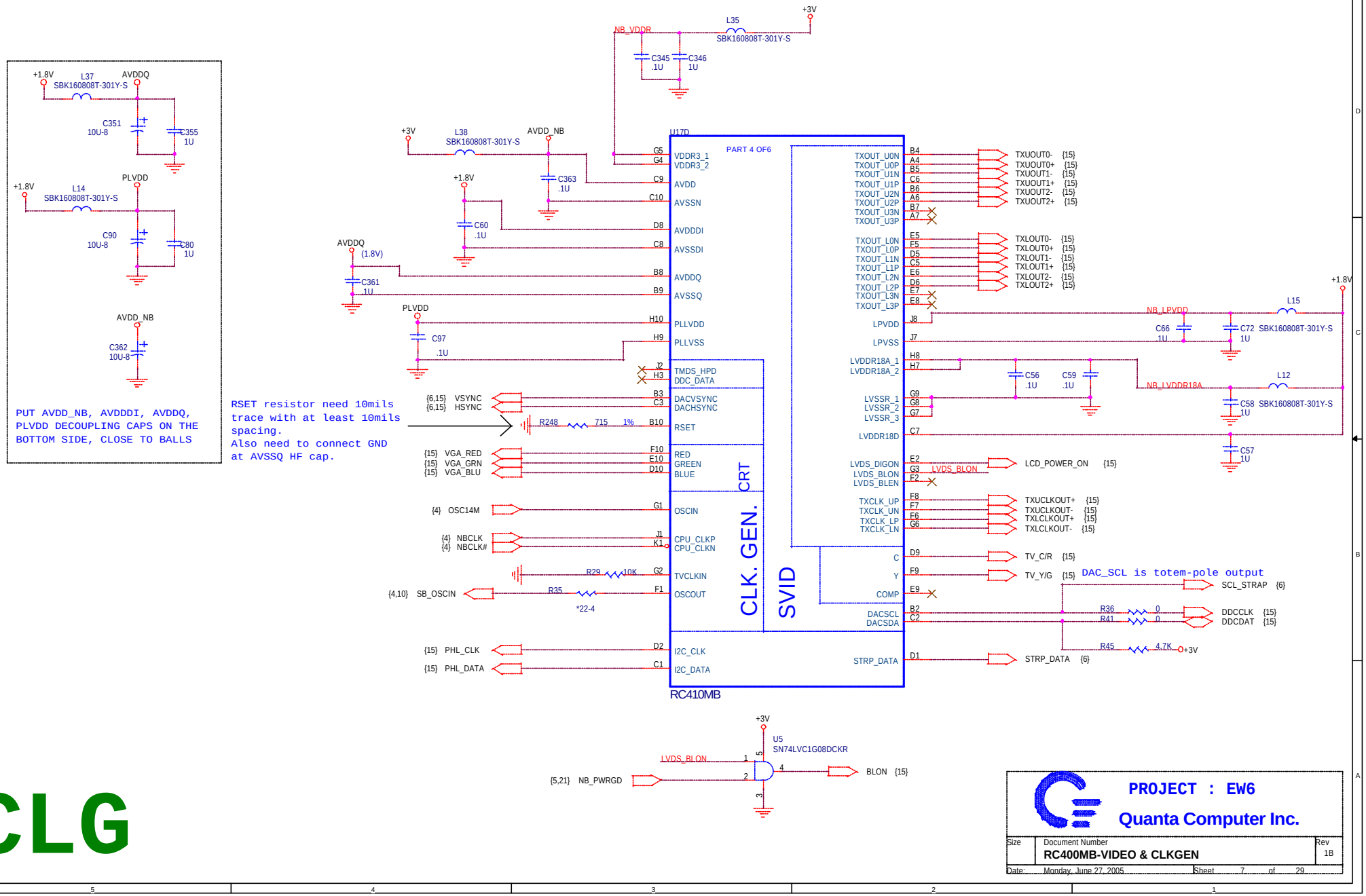
+1.8V
L37
SBK160808T-301Y-S
AVDDQ
C351
10U-8
C355
1U
PLVDD
+1.8V
L14
SBK160808T-301Y-S
C90
10U-8
C80
1U
AVDD_NB
C362
10U-8
PUT AVDD_NB, AVDDDI, AVDDQ, PLVDD DECOUPLING CAPS ON THE BOTTOM SIDE, CLOSE TO BALLS
RSET resistor need 10mils trace with at least 10mils spacing.
Also need to connect GND at AVSSQ HF cap.
+3V
L35
SBK160808T-301Y-S
NB_VDDR
C345
.1U
C346
1U
+3V
L38
SBK160808T-301Y-S
AVDD_NB
+1.8V
C363
.1U
C60
.1U
AVDDQ
(1.8V)
C361
1U
PLVDD
C97
.1U
U17D
PART 4 OF6
G5 VDDR3_1
G4 VDDR3_2
C9 AVDD
C10 AVSSN
D8 AVDDDI
C8 AVSSDI
B8 AVDDQ
B9 AVSSQ
H10 PLLVDD
H9 PLLVSS
J2 TMDS_HPD
H3 DDC_DATA
{6,15} VSYNC
{6,15} HSYNC
B3 DACVSYNC
C3 DACHSYNC
R248 715 1%
B10 RSET
{15} VGA_RED
{15} VGA_GRN
{15} VGA_BLU
F10 RED
E10 GREEN
D10 BLUE
CRT
{4} OSC14M
G1 OSCIN
{4} NBCLK
{4} NBCLK#
J1
K1
CPU_CLKP
CPU_CLKN
CLK. GEN.
R29 10K
G2 TVCLKIN
{4,10} SB_OSCIN
R35
*22-4
F1 OSCOUT
{15} PHL_CLK
{15} PHL_DATA
D2 I2C_CLK
C1 I2C_DATA
TXOUT_U0N B4
TXOUT_U0P A4
TXOUT_U1N B5
TXOUT_U1P C6
TXOUT_U2N B6
TXOUT_U2P A6
TXOUT_U3N B7
TXOUT_U3P A7
TXUOUT0- {15}
TXUOUT0+ {15}
TXUOUT1- {15}
TXUOUT1+ {15}
TXUOUT2- {15}
TXUOUT2+ {15}
TXOUT_L0N E5
TXOUT_L0P F5
TXOUT_L1N D5
TXOUT_L1P C5
TXOUT_L2N E6
TXOUT_L2P D6
TXOUT_L3N E7
TXOUT_L3P E8
TXLOUT0- {15}
TXLOUT0+ {15}
TXLOUT1- {15}
TXLOUT1+ {15}
TXLOUT2- {15}
TXLOUT2+ {15}
LPVDD J8
LPVSS J7
NB_LPVDD
L15
C66 .1U
C72 SBK160808T-301Y-S 1U
LVDDR18A_1 H8
LVDDR18A_2 H7
C56 .1U
C59 .1U
NB_LVDDR18A
L12
C58 SBK160808T-301Y-S 1U
LVSSR_1 G9
LVSSR_2 G8
LVSSR_3 G7
LVDDR18D C7
C57 1U
+1.8V
LVDS_DIGON E2
LVDS_BLON G3
LVDS_BLEN F2
LVDS_BLON
LCD_POWER_ON {15}
TXCLK_UP F8
TXCLK_UN F7
TXCLK_LP F6
TXCLK_LN G6
TXUCLKOUT+ {15}
TXUCLKOUT- {15}
TXLCLKOUT+ {15}
TXLCLKOUT- {15}
C D9
Y F9
COMP E9
TV_C/R {15}
TV_Y/G {15}
DAC_SCL is totem-pole output
SVID
DACSCL B2
DACSDA C2
R36 0
R41 0
SCL_STRAP {6}
DDCCLK {15}
DDCDAT {15}
R45 4.7K
+3V
STRP_DATA D1
STRP_DATA {6}
RC410MB
+3V
U5
SN74LVC1G08DCKR
LVDS_BLON
{5,21} NB_PWRGD
BLON {15}
CLG
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Quanta Computer Inc.
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RC400MB-VIDEO & CLKGEN
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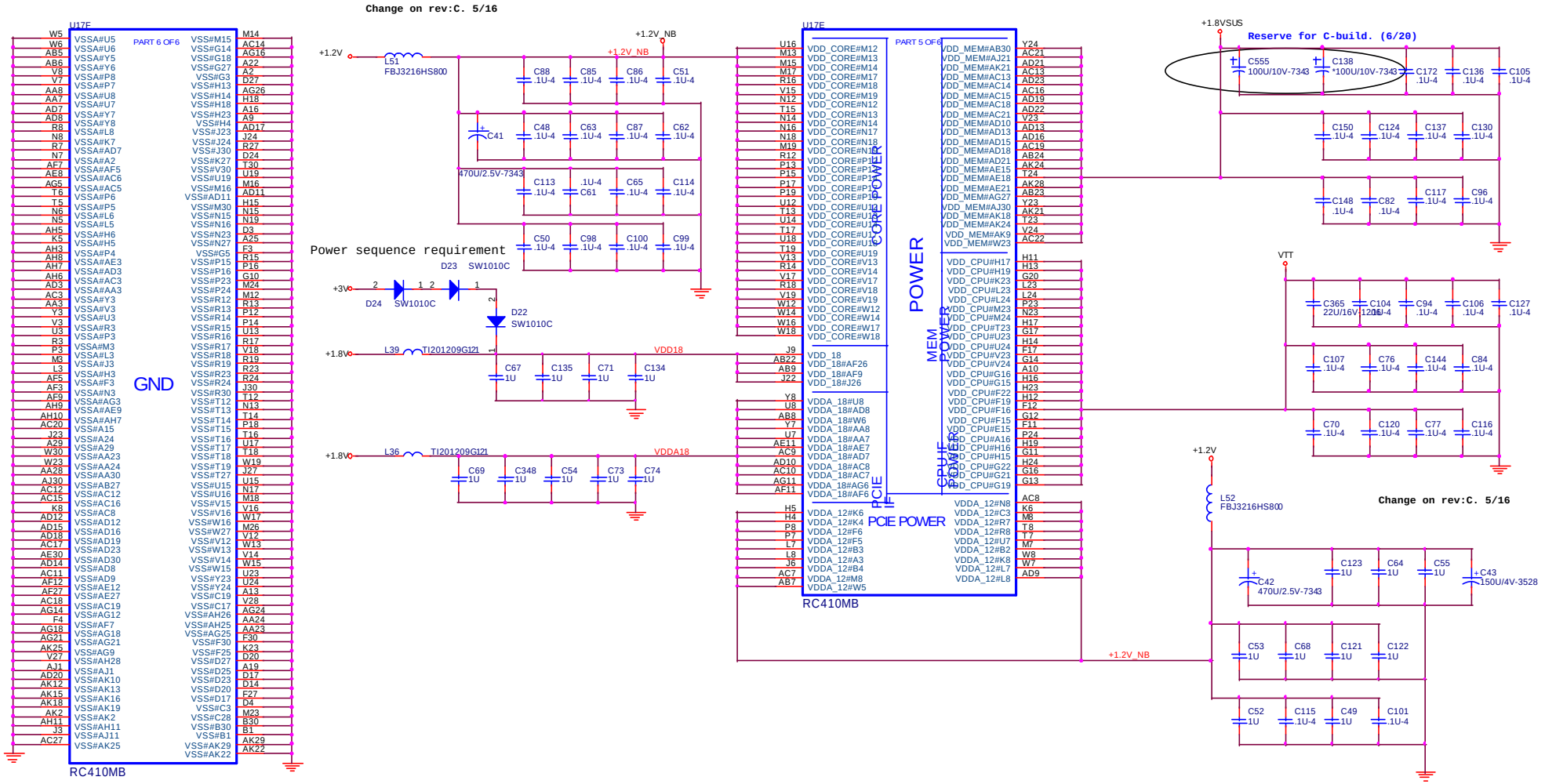
CLG



PROJECT : EW6

Quanta Computer Inc.

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	RC400MB-POWER	3A
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CLG

U9 *7SH08 — +3V_S5 — C207 .1U-4 — {4,5,16,20} ALINK_RST# — R85 0 — R86 8.2K-4

ATi Recommend
Vendor: NSK
Part Number: NXG 32.768KAE12FUD 16 PPM.

Y4 32.768KHZ — 32K_X1 — 32K_X2 — R348 20M-4 — R338 20M-4 — C420 18P-4 — C407 18P-4

SB400 SB Part 1 of 4 — U20A

PCI CLKS: PCICLK0 L4 — PCICLK1 L3 — PCICLK2 L2 PCI_MINI R305 33-4 PCLK_MINI — PCICLK3 L1 PCI_591 R306 33-4 PCLK_591 — PCICLK4 M4 PCI_PCM R301 33-4 PCLK_PCM — PCICLK5 M3 PCI_SIO R123 33-4 PCLK_SIO — PCICLK6 M2 SRC_CLK6 R125 22-4 PCICLK6 — PCICLK7 M1 PCI_LAN R304 33-4 PCLK_LAN — PCICLK8 N4 PCI_CLK8 R299 22-4 PCICLK8 — PCICLK9 N3 PCICLK9 R300 22-4 — PCICLK_FB N2 PCI_CLK9_FB

Change for EMI. 06/24
Add PCLK_SIO for debug card. 06/16

PCLK_MINI {12,20} — PCLK_591 {12,21} — PCLK_PCM {12,17} — PCLK_SIO {12,20} — PCICLK6 {12} — PCLK_LAN {12,14} — PCICLK8 {12}

T8 — T7

Item 52 REV.A2
BIOS 1A15_T0 adjust PCI drive strength will cause Error code hang up 81h,Must move C387.But before 1A14 BIOS use C387 is ok

C387 *100P-4

Change on B version.

PCI EXPRESS INTERFACE:
- {6} A_RX0P — C396 .01U-4 A_RX0P_C — A_RX0N — C394 .01U-4 A_RX0N_C — A_RX1P — C399 .01U-4 A_RX1P_C — A_RX1N — C398 .01U-4 A_RX1N_C
- {6} A_TX0P — A_TX0N — A_TX1P — A_TX1N
- PCIE_VDDR — R320 150/F PCIE_CALRP — R311 150/F PCIE_CALRN — R316 4.12K/F PCIE_CALI — PCIE_PVDD

PCIE Power: +1.8V — L42 SBK160808T-301YS — C385 22U/16V-1206 — C384 1U — C256 .1U-4 — PCIE_VDDR — L43 TI201209G121 — C390 22U/16V-1206 — C286 1U-4 — C277 .1U-4 — C271 .1U-4 — C263 .1U-4 — C254 .1U-4 — C265 .1U-4 — C266 .1U-4 — C274 .1U-4 — C255 .1U-4

PCI INTERFACE:
- PCIRST# — AD[0..31] — AD[0..31] {12,14,17,20}
- CBE0#/ROMA10 — CBE0# {14,17,20}
- CBE1#/ROMA1 — CBE1# {14,17,20}
- CBE2#/ROMWE# — CBE2# {14,17,20}
- CBE3# — CBE3# {14,17,20}
- FRAME# — FRAME# {14,17,20}
- DEVSEL#/ROMA0 — DEVSEL# {14,17,20}
- IRDY# — IRDY# {14,17,20}
- TRDY#/ROMOE# — TRDY# {14,17,20}
- PAR/ROMA19 — PAR {14,17,20}
- STOP# — STOP# {14,17,20}
- PERR# — PERR# {14,17,20}
- SERR# — SERR# {14,17,20}
- REQ0# — REQ0# {14}
- REQ1# — REQ1# {20}
- REQ3#/PDMA_REQ0# — REQ3# {17}
- REQ4#/PLL_BP33/PDMA_REQ1#
- REQ5#/GPIO13
- REQ6#/GPIO31
- GNT0# — GNT0# {14}
- GNT1# — GNT1# {20}
- GNT2#
- GNT3#/PLL_BP66/PDMA_GNT0# — GNT3# {17}
- GNT4#/PLL_BP50/PDMA_GNT1#
- GNT5#/GPIO14
- GNT6#/GPIO32
- CLKRUN# — CLKRUN# {14,17,20,21}
- LOCK# — PCI_LOCK# {14,17,20}

LCDID1 {15} — LCDID0 {15} — LCDID2 {15}

U19 *7SH08 — C375 *.1U-4 — C372 *82P-4 — R262 8.2K-4 — R265 0 — C374 82P-4 — PCIRST# — PCIRST# {14,17,20,21}

Reserved For EMI
PCLK_MINI C395 *33P-4 — PCLK_591 C397 *33P-4 — PCLK_PCM C388 *33P-4 — PCLK_SIO C391 *33P-4 — PCICLK6 C392 *33P-4 — PCLK_LAN C393 *33P-4 — PCICLK8 C386 *33P-4

+3V — PCI_LOCK# R298 8.2K-4 — INTA# R277 8.2K-4 — INTB# R279 8.2K-4 — INTC# R278 8.2K-4 — INTD# R275 8.2K-4 — INTE# R276 8.2K-4 — INTF# R87 8.2K-4 — INTG# R91 8.2K-4 — INTH# R89 8.2K-4

+3V — CLKRUN# R293 8.2K-4

RN3 8.2KX4-4: PERR# FRAME# TRDY# STOP# REQ3# REQ0# REQ2# REQ1#

RN1 8.2KX4-4: GNT0# GNT1# GNT2# GNT3# PAR SERR# DEVSEL# IRDY#

RN6 8.2KX4-4

RN2 8.2KX4-4: GNT4# R291 8.2K-4 — REQ4# R289 8.2K-4 — LAD3 R283 100K-4 — LAD2 R280 100K-4 — LAD1 R281 100K-4 — LAD0 R282 100K-4 — REQ5# R287 8.2K-4

RN5 8.2KX4-4: SERIRQ — LDRQ#0 — LDRQ#1 — LFRAME#

Add for debug. 06/16 (C state)

LPC:
- LAD0 — LAD0/FWH0 {20,21}
- LAD1 — LAD1/FWH1 {20,21}
- LAD2 — LAD2/FWH2 {20,21}
- LAD3 — LAD3/FWH3 {20,21}
- LFRAME# — LFRAME#/FWH4 {20,21}
- LDRQ0# — LDRQ#0 {20}
- LDRQ1#
- SERIRQ — SERIRQ {17,20,21}

RTC:
- RTCCLK — RTC_CLK {12}
- RTC_IRQ#/ACPWR_STRAP — AUTO_ON# {12}
- VBAT — VCCRTC
- RTC_GND — C410 1U

XTAL:
- VTT — 32K_X1 — X1 — R324 *1K-4 — 32K_X2 — X2

CPU:
- {2} CPUPWRGD — CPU_PG/LDT_PG
- {2} INTR — INTR/LINT0
- {2} NMI — NMI/LINT1
- {2} CPUINIT# — INIT#
- {2} SMI# — SMI#
- {2} CPUSLP# — SLP#/LDT_STP#
- {2} IGNNE# — IGNNE#
- {2} A20M# — A20M#
- {2} FERR# — FERR#
- {2} STPCLK# — STPCLK#/ALLOW_LDTSTP
- T11 — SSMUXSEL/GPIO0
- {26} DPRSLPVR — DPRSLPVR
- {6} BMREQ# — BMREQ#
- T16 — LDT_RST#

SB400

{4,26} STP_CPU# — STP_CPU# — CPU_STP#/DPSLP_3V#
{2} DPSLP# — DPSLP# — DPSLP_OD#/GPIO37

INTA# AJ8 — INTB# AK7 — INTC# AG5 — INTD# AH5
{17} INTE# — {14} INTF# — {20} INTG# — {20} INTH#
INTE# AJ5 — INTF# AH6 — INTG# AK6 — INTH# AG7
INTA# — INTB# — INTC# — INTD# — INTE#/GPIO33 — INTF#/GPIO34 — INTG#/GPIO35 — INTH#/GPIO36

PCIE_VDDR — PCIE_VDDR_1 F26 — PCIE_VDDR_2 R29 — PCIE_VDDR_3 G26 — PCIE_VDDR_4 P26 — PCIE_VDDR_5 K26 — PCIE_VDDR_6 L26 — PCIE_VDDR_7 P28 — PCIE_VDDR_8 N26 — PCIE_VDDR_9 P27

PCIE_VSS_1 H28 — PCIE_VSS_2 F29 — PCIE_VSS_3 H29 — PCIE_VSS_4 H26 — PCIE_VSS_5 F27 — PCIE_VSS_6 G29 — PCIE_VSS_7 L29 — PCIE_VSS_8 J26 — PCIE_VSS_9 L28 — PCIE_VSS_10 J27 — PCIE_VSS_11 N27 — PCIE_VSS_12 M26 — PCIE_VSS_13 K27 — PCIE_VSS_14 P29 — PCIE_VSS_15 P30

RTC

D25 RB751 — +3VPCU — VCCRTC — R196 1K-4 — RTC_N02 — D26 RB751 — C467 1U — C468 .1U-4 — JP1 Clear PAD — R425 100/F

Q14 MMBT3904 — 3VRTC — RTC_N01 — R192 3K — +5VSUS — R191 4.7K/F — RTC_N03 — R190 15K/F — C324 .1U-4 — CN23 RTC CONN

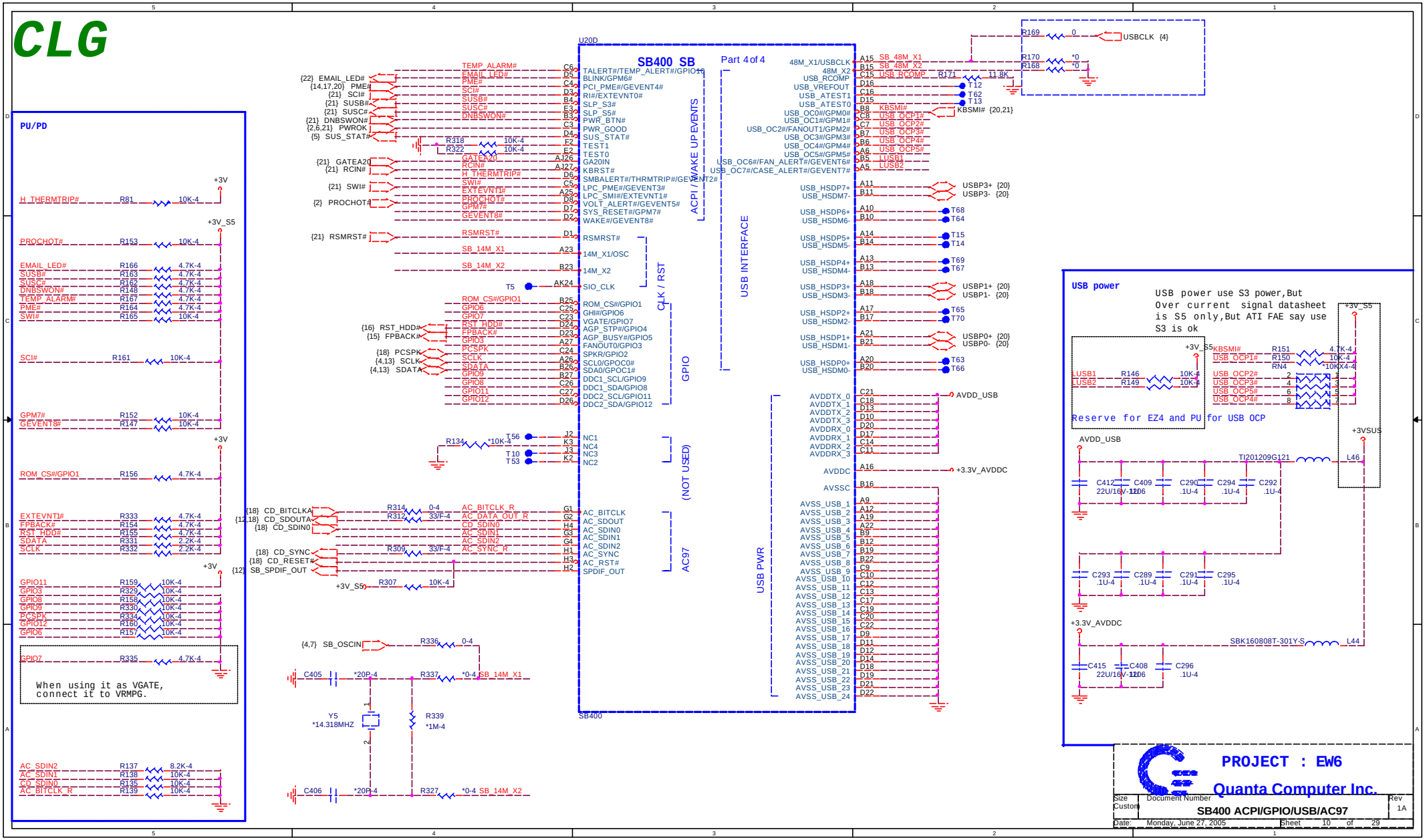
+3V — C539 .1U-4 — C540 .1U-4 — C541 .1U-4 — C542 .1U-4 — C543 .1U-4 — C544 .1U-4 — C545 .1U-4 — C546 .1U-4

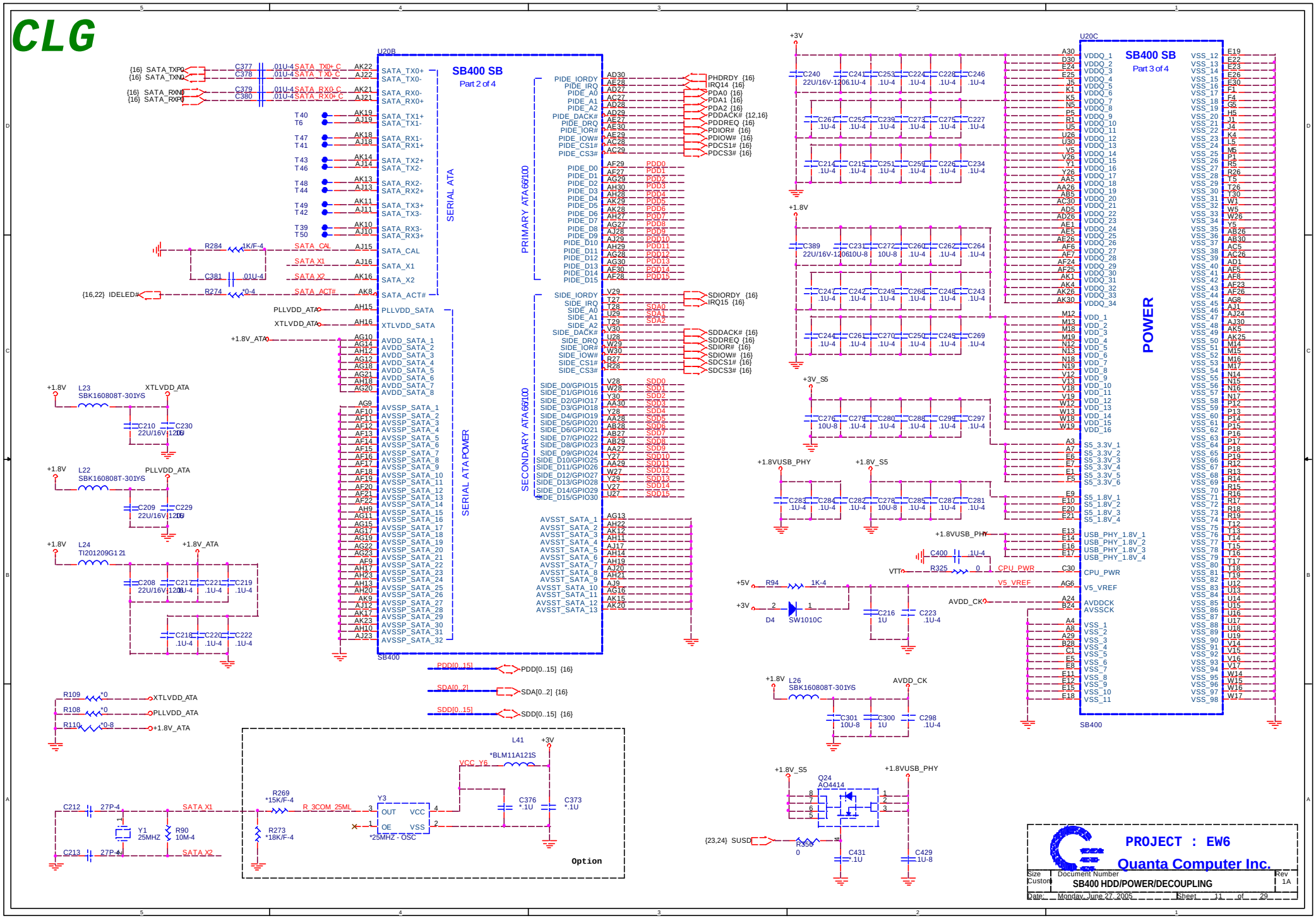
PROJECT : EW6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB400 PCIE/PCI/CPU/LPC I/F	3A

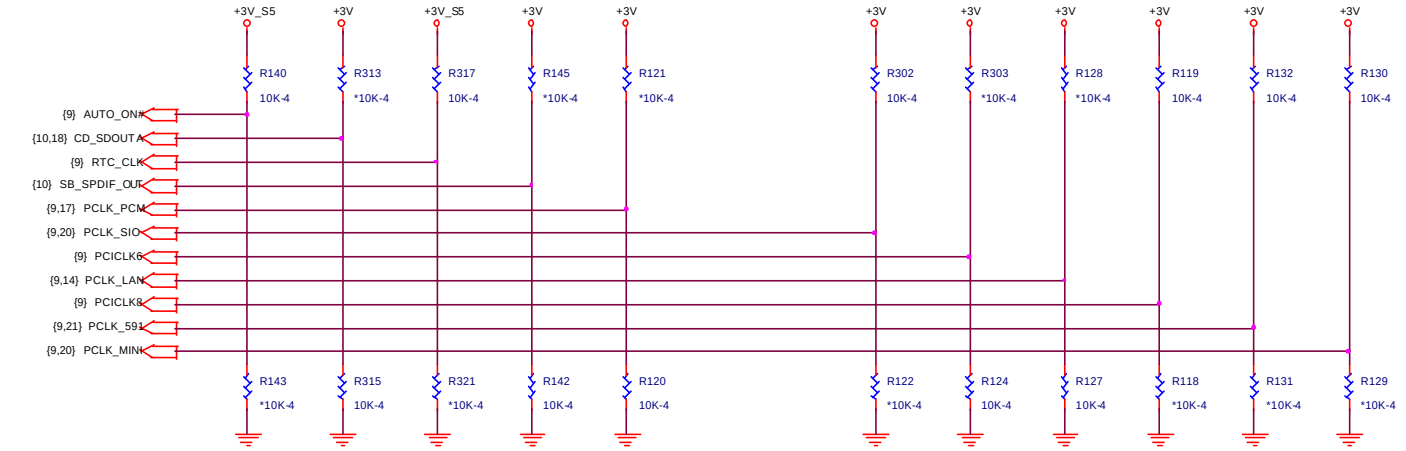
Date: Monday, June 27, 2005 — Sheet 9 of 29

CLG


PU/PD
When using it as VGATE, connect it to VRMPG.
U20D
SB400 SB
Part 4 of 4
SB400
ACPI / WAKE UP EVENTS
USB INTERFACE
CLK / RST
GPIO
(NOT USED)
AC97
USB PWR
USB power
USB power use S3 power,But Over current signal datasheet is S5 only,But ATI FAE say use S3 is ok
Reserve for EZ4 and PU for USB OCP
PROJECT : EW6
Quanta Computer Inc.
SB400 ACPI/GPIO/USB/AC97
Size: Custom
Document Number
Rev: 1A
Date: Monday, June 27, 2005
Sheet 10 of 29


CLG
U20B
SB400 SB
Part 2 of 4
SERIAL ATA
PRIMARY ATA66/100
SECONDARY ATA66/100
SERIAL ATA POWER
SB400
U20C
SB400 SB
Part 3 of 4
POWER
SB400
PROJECT : EW6
Quanta Computer Inc.
SB400 HDD/POWER/DECOUPLING
Size: Custom
Document Number
Rev: 1A
Date: Monday, June 27, 2005
Sheet 11 of 29
Option

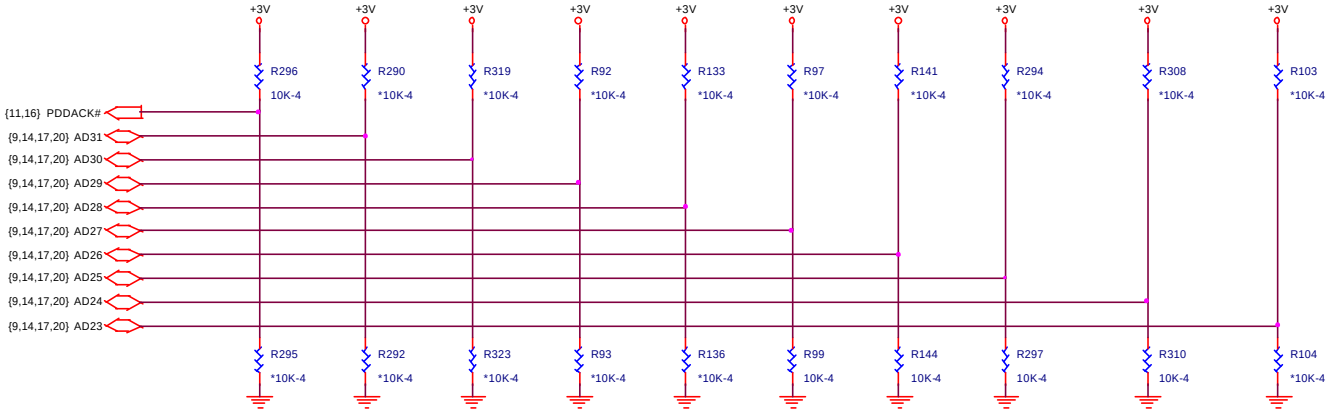
CLG



REQUIRED STRAPS

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK4 PCLK_PCM	PCI_CLK5 PCLK_SIO	PCI_CLK6 PCI_CLK6	PCI_CLK7 PCLK_LAN	PCI_CLK8 PCI_CLK8	PCI_CLK3 PCLK_591	PCI_CLK2 PCLK_MINI*
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz use Internal PLL	14MHz OSC MODE DEFAULT	CPU I/F = K8	H,H = PCI(X BUS) ROM H,L = LPC ROM I (LPC addresses are translated to the top of the 4G address space)		USB PHY PWRDOWN DISABLE DEFAULT	48MHz OSC/Clock Buffer
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	48MHz use External Clock DEFAULT	14MHz XTAL MODE	CPU I/F = P4 DEFAULT	L,H = LPC ROM II DEFAULT (addresses mapped to below 1M) L,L = FWH ROM		USB PHY PWRDOWN ENABLE	48MHz Crystal Pad DEFAULT

*This strap is only required if the strap on PCICLK4 is configured for External Clock.



DEBUG STRAPS

	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

PROJECT : EW6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB400 STRAPS	1A
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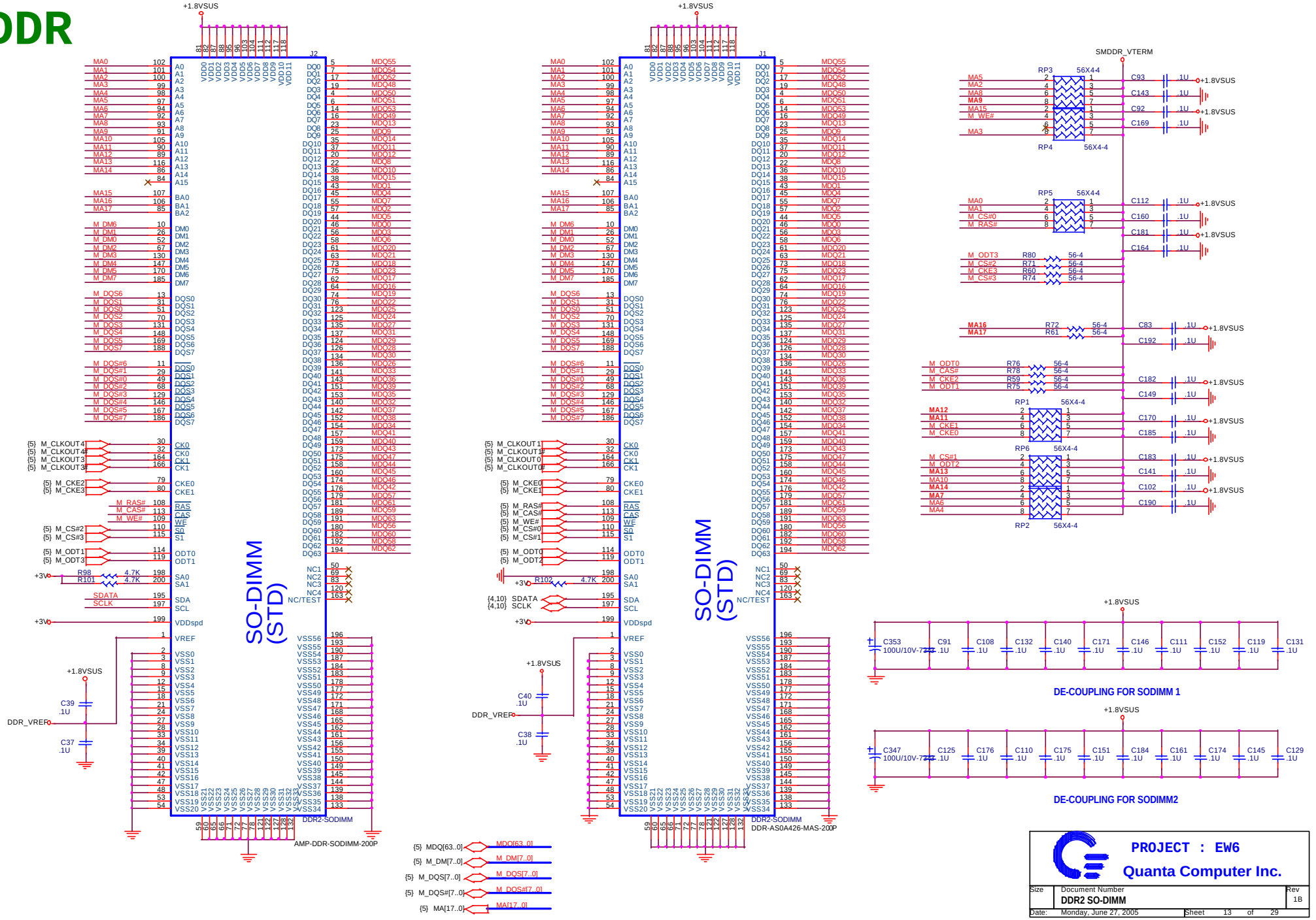
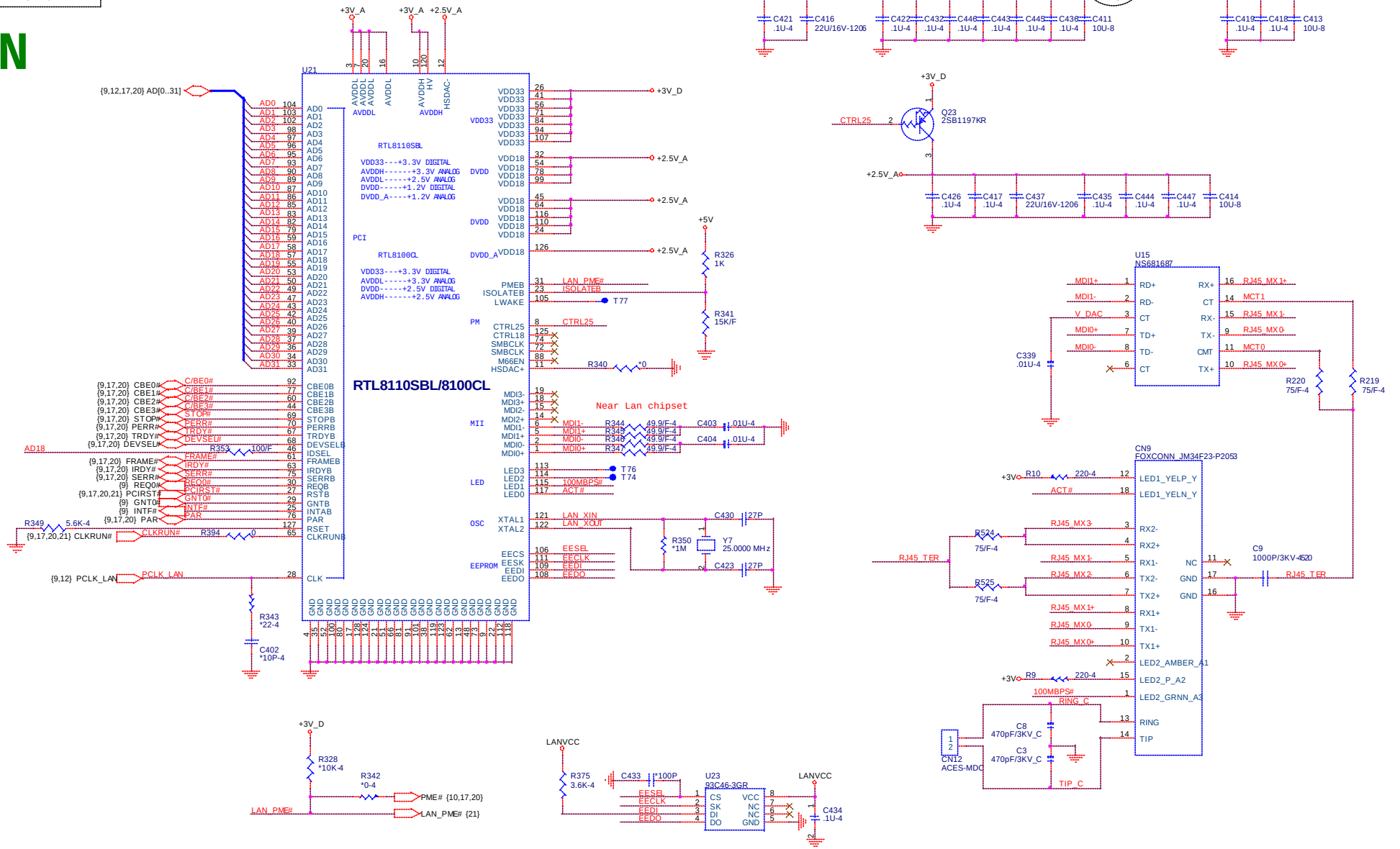
DDR

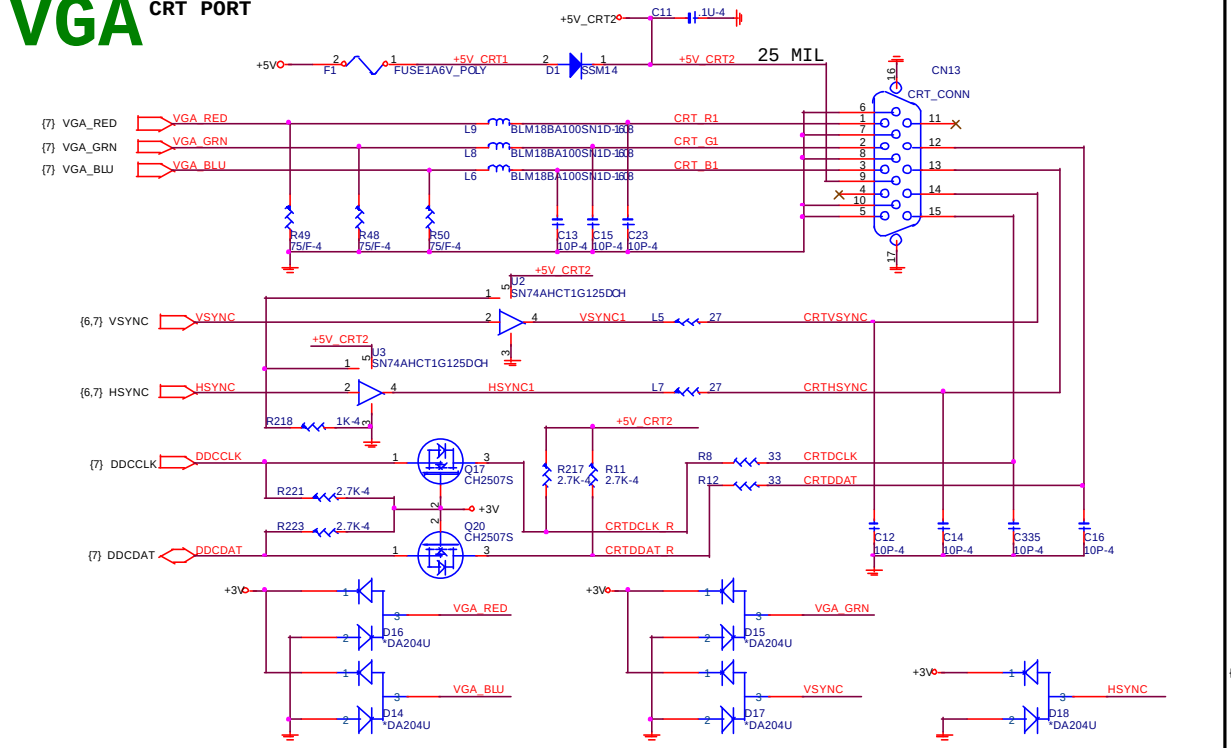

+1.8VSUS
J2
SO-DIMM (STD)
DDR2-SODIMM
AMP-DDR-SODIMM-200P
J1
SO-DIMM (STD)
DDR2-SODIMM
DDR-AS0A426-MAS-200P
SMDDR_VTERM
RP3 56X4-4
RP4 56X4-4
RP5 56X4-4
RP1 56X4-4
RP6 56X4-4
RP2 56X4-4
DE-COUPLING FOR SODIMM 1
DE-COUPLING FOR SODIMM2
PROJECT : EW6
Quanta Computer Inc.
DDR2 SO-DIMM
Monday, June 27, 2005
Sheet 13 of 29

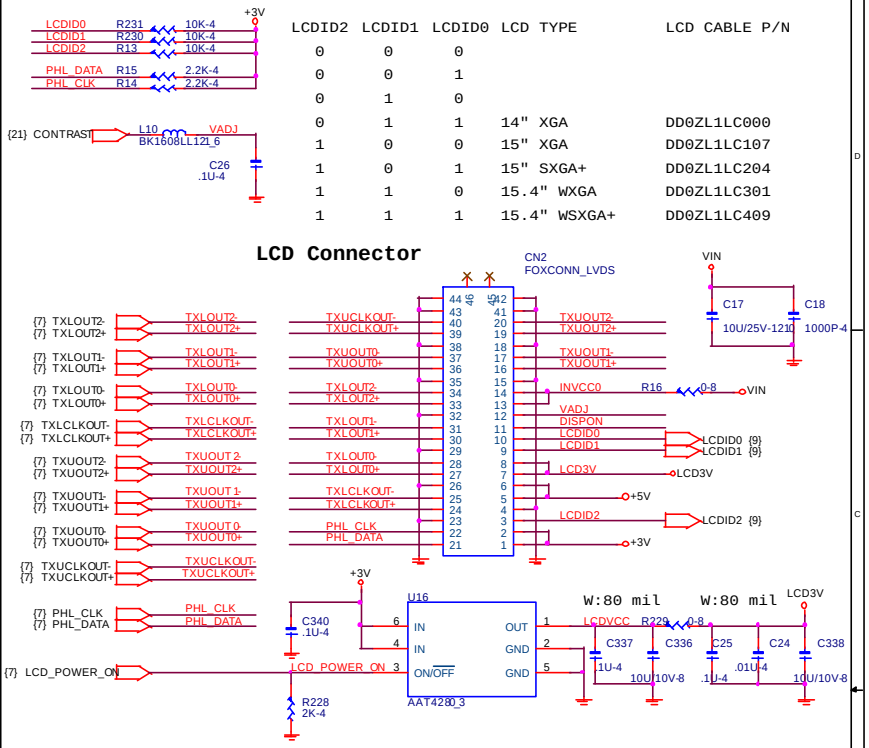
ID Select : AD18
Interrupt Pin : INTD#
Request Indicate : REQ0#
Grant Indicate : GNT0#

LAN

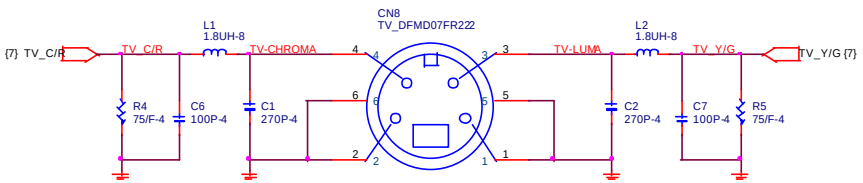


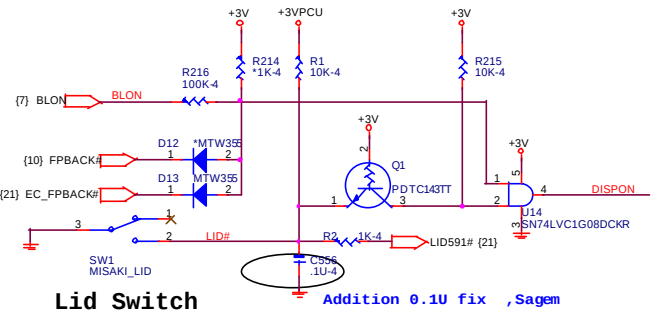
VGA CRT PORT





S-VIDEO



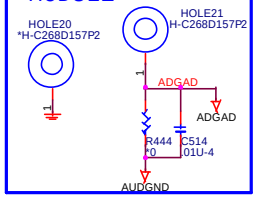


Lid Switch

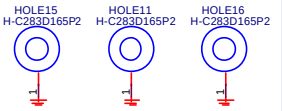
Addition 0.1U fix ,Sagem

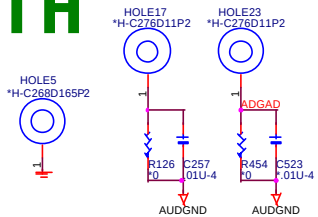
OTH

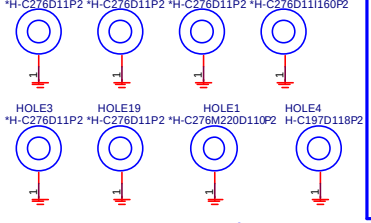
FOR MODEM MODULE



FOR CPU HEATSINK

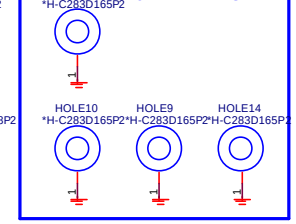


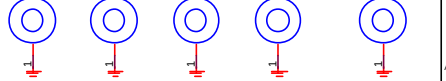




FOR M/B HOLE

FOR NB HEATSINK

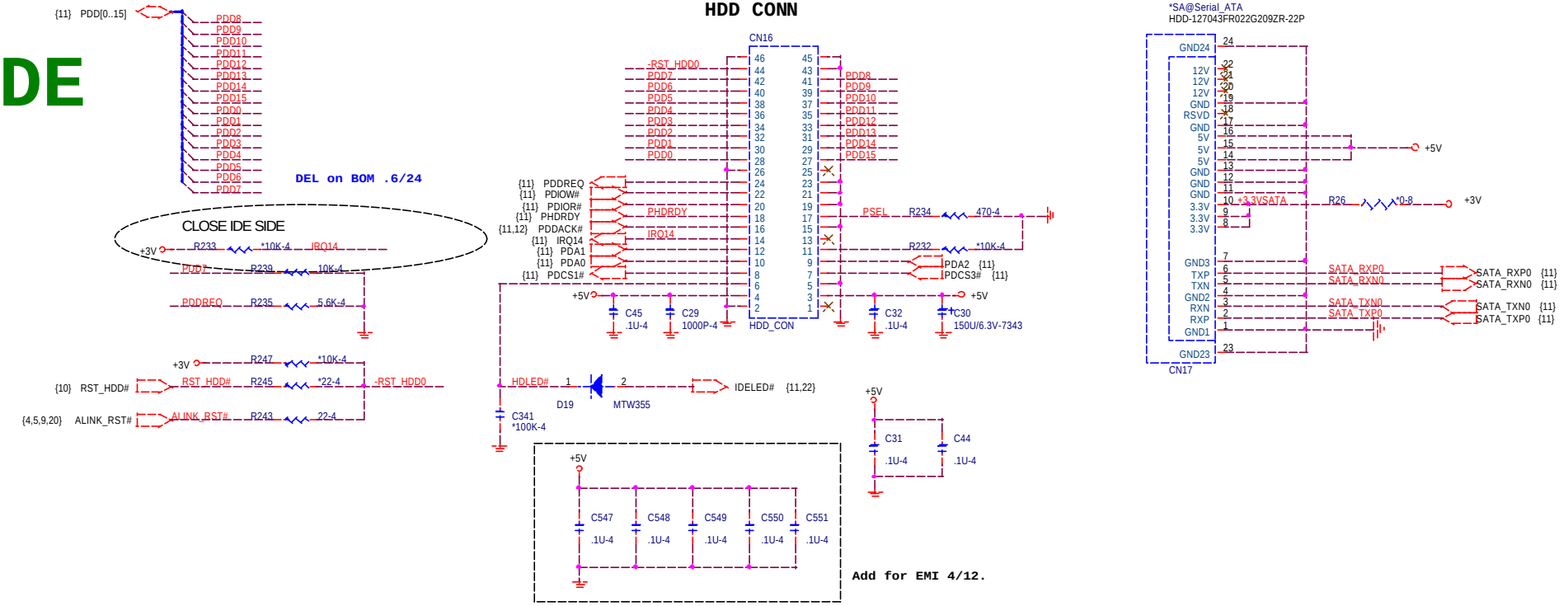




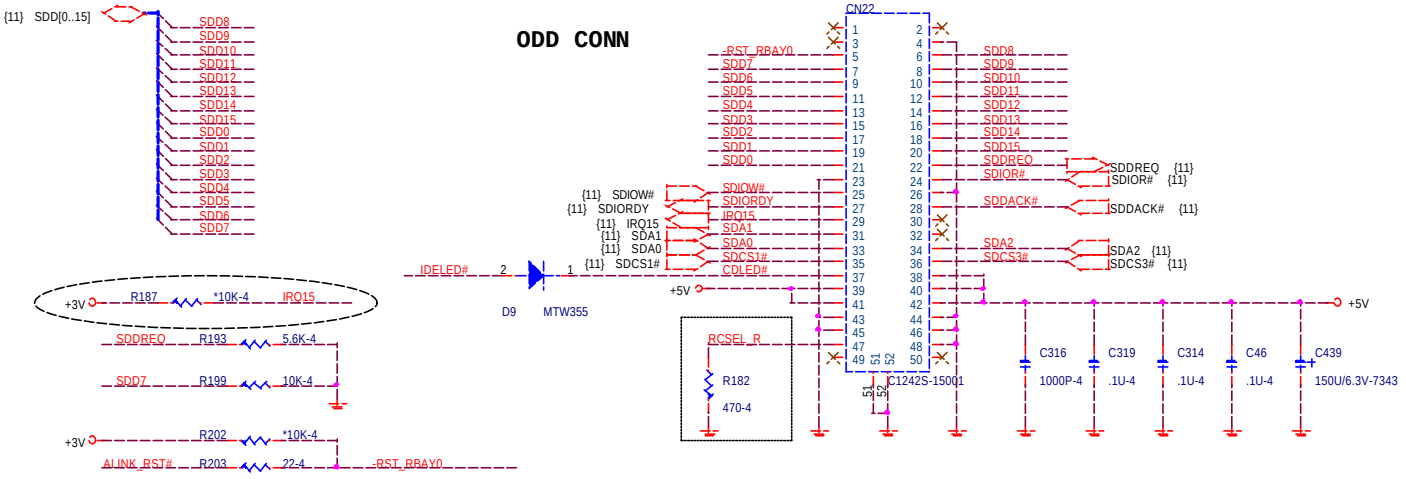
Size	Document Number	Rev
	VGA Ports, LID, & HOLES	3A
Date: Monday, June 27, 2005	Sheet 15 of 29	

IDE

HDD CONN



ODD CONN



PROJECT : EW6

Quanta Computer Inc.

Size	Document Number	Rev
	HDD & CDROM	3A

Date: Monday, June 27, 2005 Sheet 16 of 29

ID Select : AD17
Interrupt Pin : INTE#
Request Indicate : REQ3#
Grant Indicate : GNT3#

CBS

CARDBUS SLOT

U30-1 PCI1510PGE

U30-2 PCI1510PGE

U30-4 PCI1510PGE

U27 TPS2211ADBR

CN5 CARDBUS-SANTA

Near TPS2211A

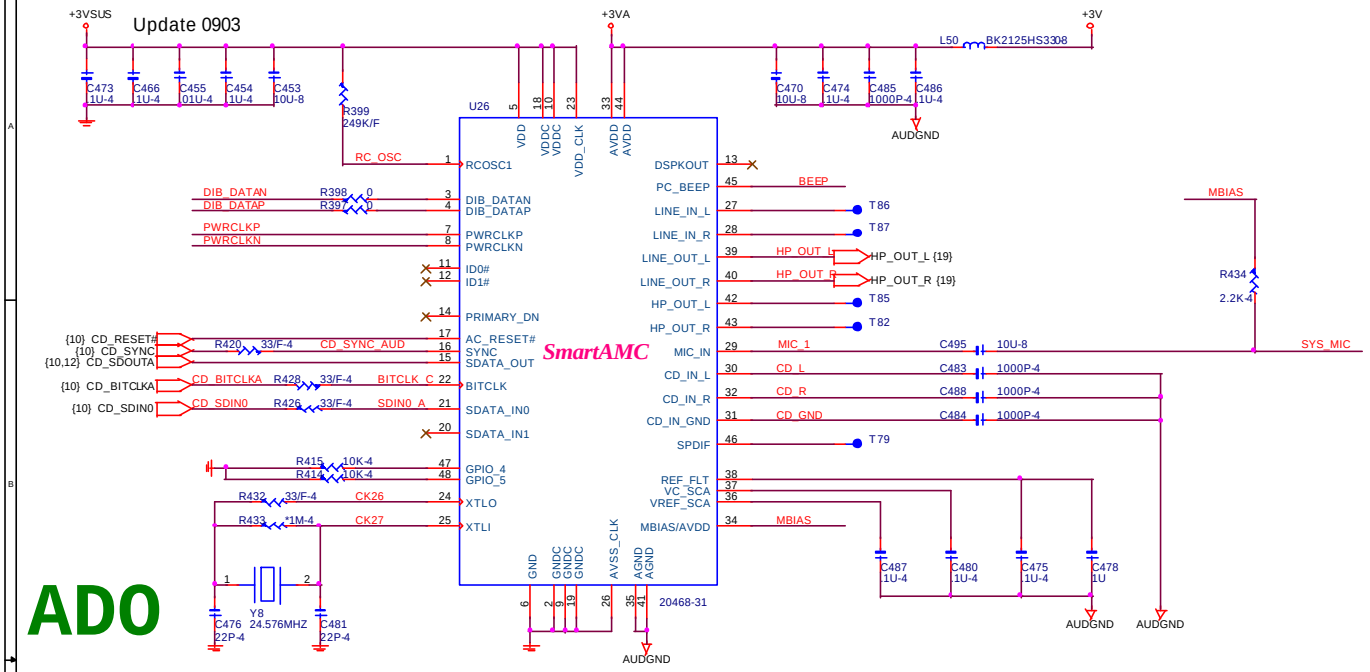
Near Slot

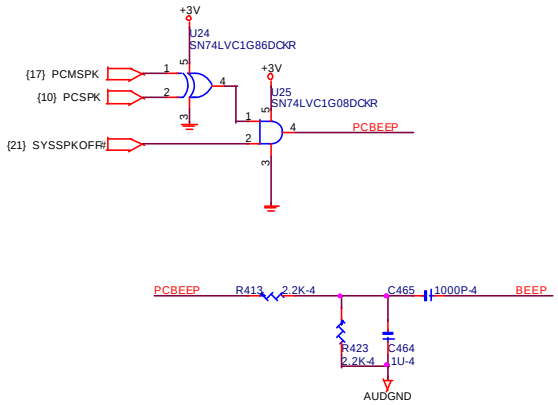
Near Chipset

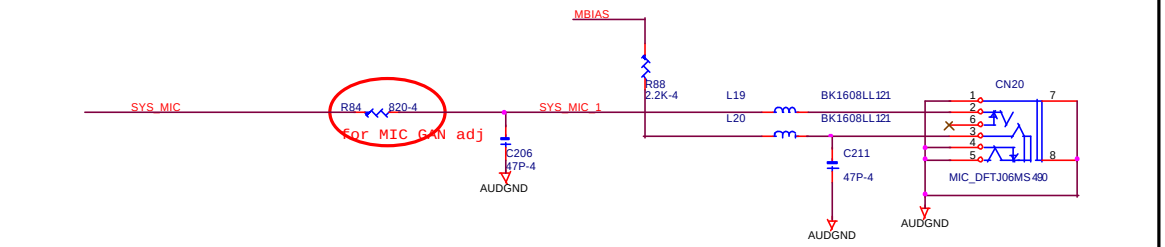
+3V Plane

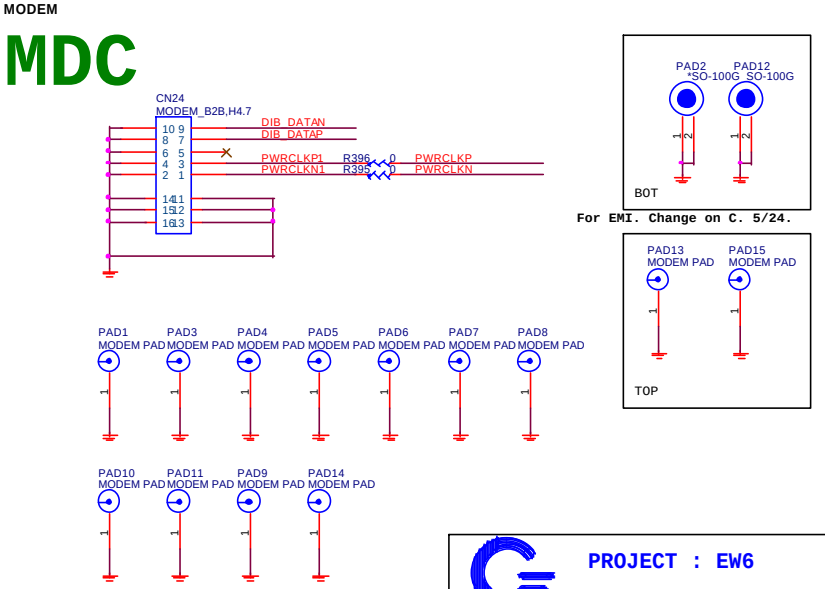
Near Chipset

Project	EW6
Quanta Computer Inc.	
Size	Document Number: PCMCIA CONTROLLER
Rev	1B
Date:	Monday, June 27, 2005
Sheet	17 of 29









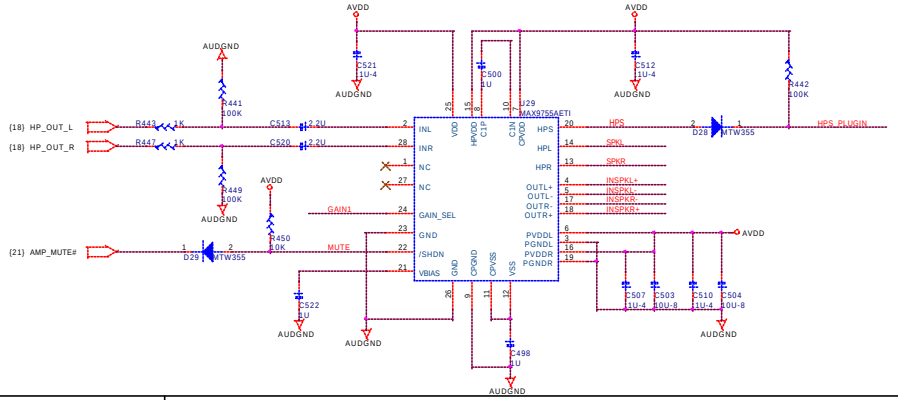
PROJECT : EW6

Quanta Computer Inc.

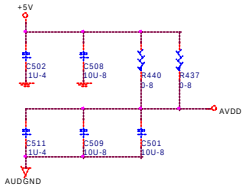
Size	Document Number	Rev
	CODEC & LINE IN & MIC	2A
Date: Monday, June 27, 2005	Sheet 18 of 29	

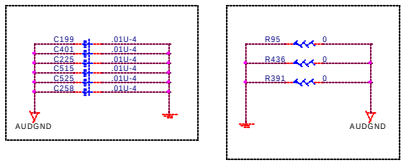
ADO

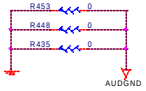
GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0



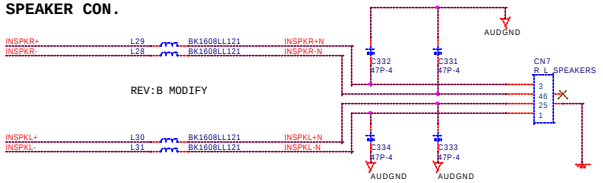
AMP POWER



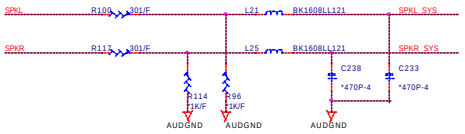




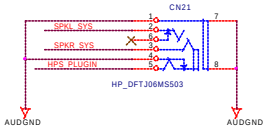
SPEAKER CON.



LINE-OUT



LINE OUT



PROJECT : EW6
Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO AMP	2A
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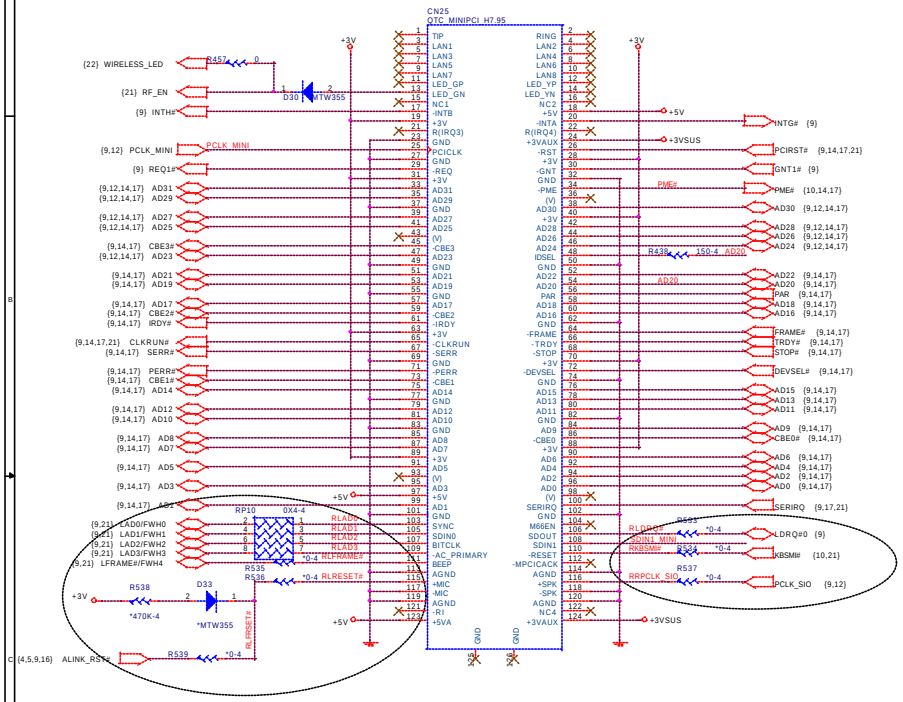
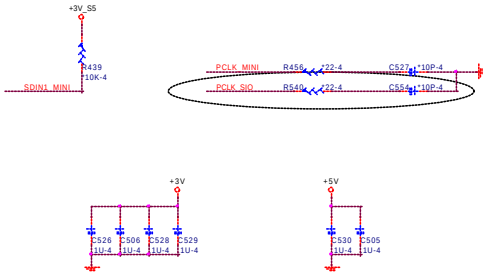
MPC

ID Select : AD20
Interrupt Pin : INTB# , INTC#
Request Indicate : REQ1#
Grant Indicate : GNT1#

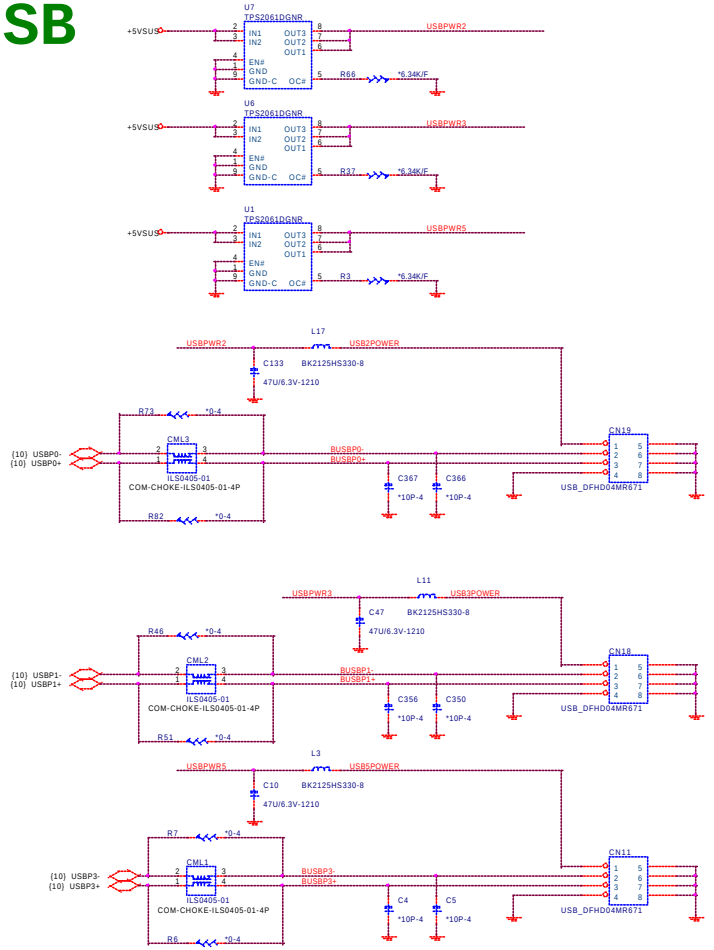
MINI-PCI



Add for debug. 06/16 (C state)



USB



PROJECT : EW6
Quanta Computer Inc.

Size	Document Number	Rev
	MINI PCI,USB	3A
Date: Monday, June 27, 2005	Sheet 20 of 29	

KBC

REV:B
MODIFY
FOR
EMI

LDRQ#(pin 8) internal is no use

Reserve on C build. 6/27

Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

SHBM=1: Enable shared memory with host BIOS

BADDR1-0	I/O Address	
	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)(HCFGBAH, HCFGBAL)+1	
1 1	Reserved	

BIU configuration should match flash speed used

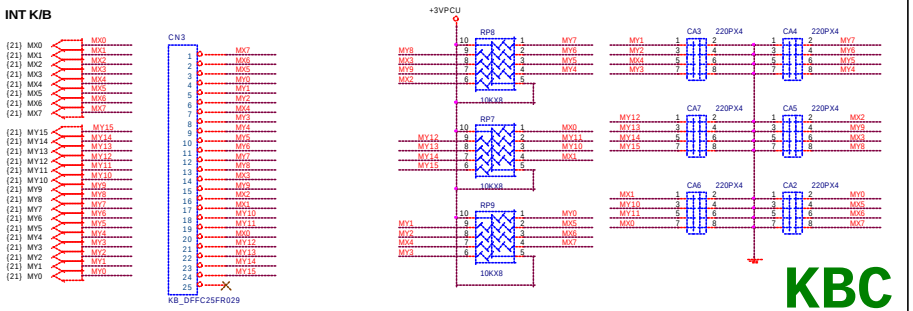
FOR 97551 ONLY

FWH

PROJECT : EW6
Quanta Computer Inc.

Size	Document Number	Rev
	PC97551 & FLASH	2A
Date: Monday, June 27, 2005	Sheet 21 of 29	

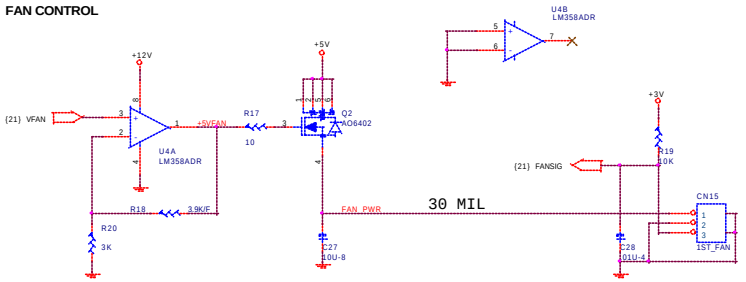
INT K/B



KBC

THM

FAN CONTROL

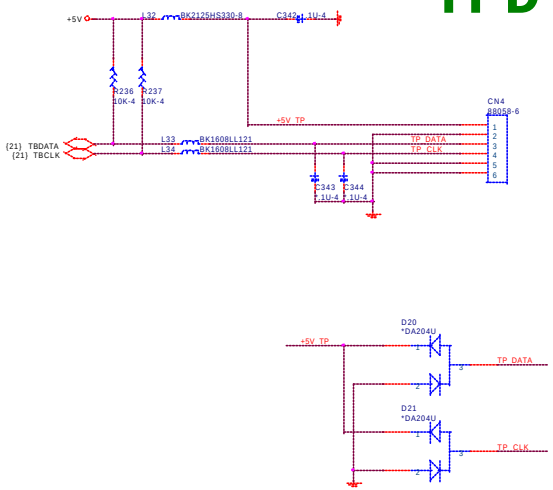


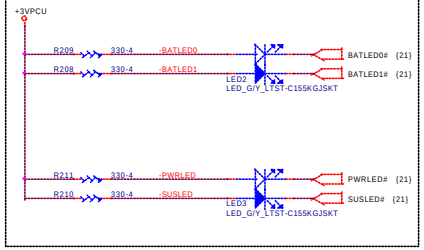
TOUCH PAD

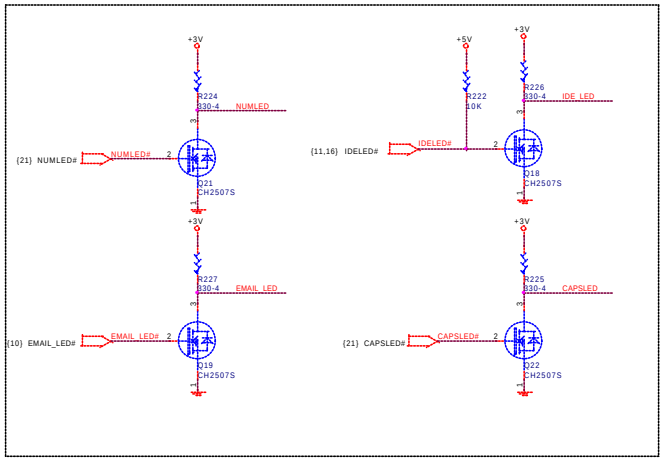
20 MIL

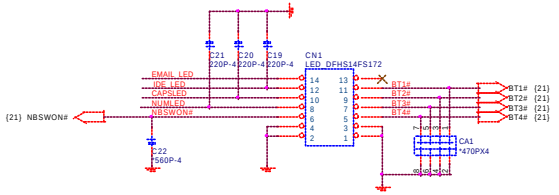
TPD

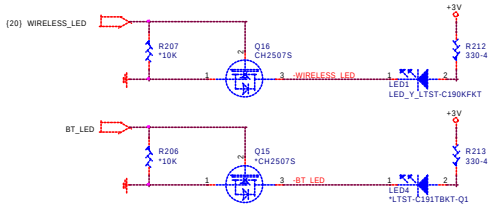
UIF





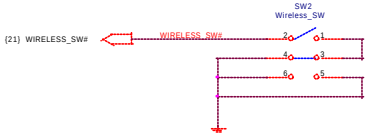






SWITCH

UIF



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Quanta Computer Inc.

Size	Document Number	Rev
	T/P,FAN,SWITCH,LED,K/B	1B
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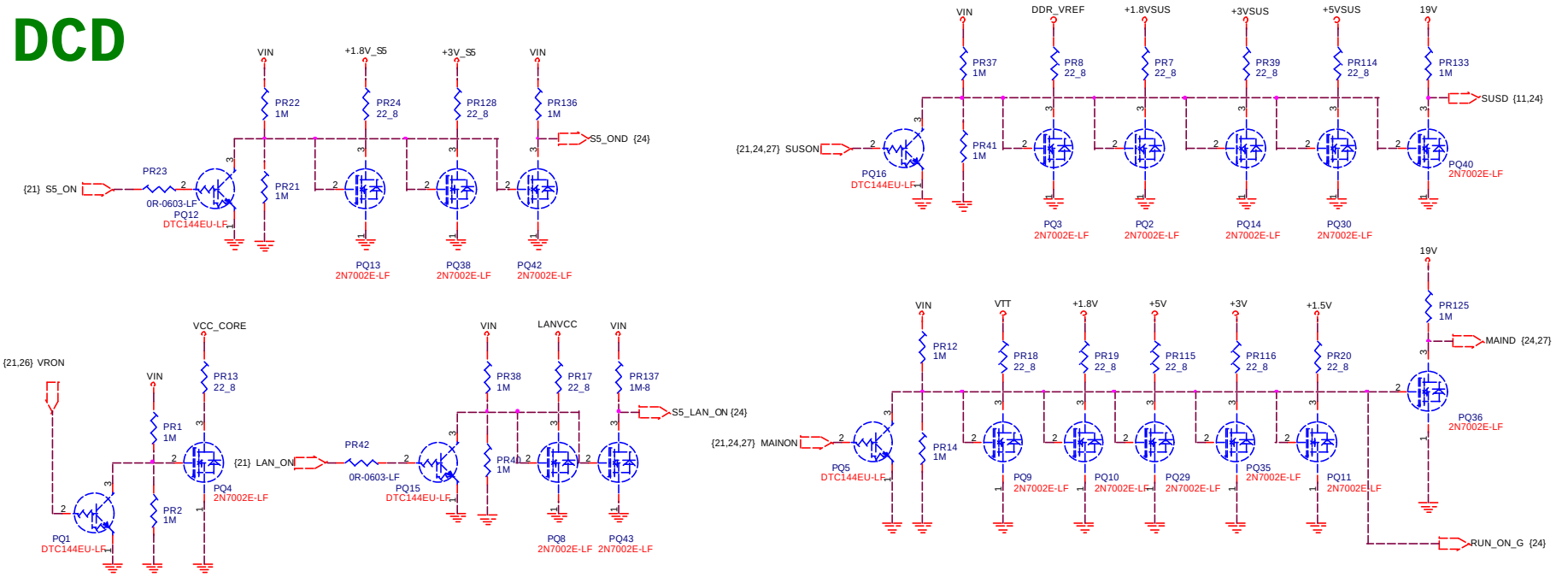
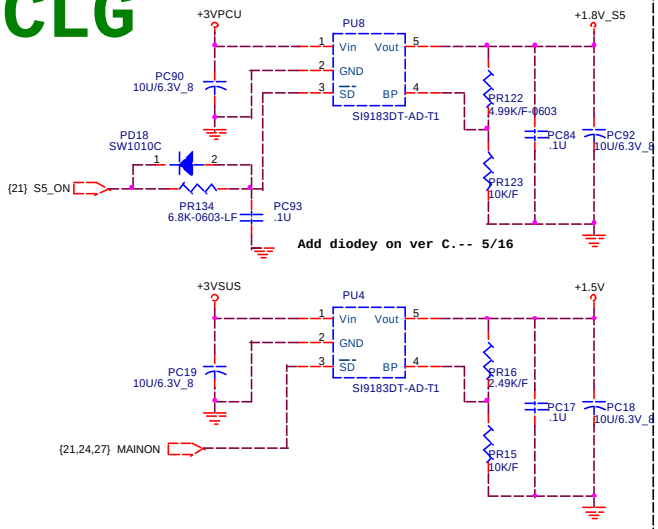
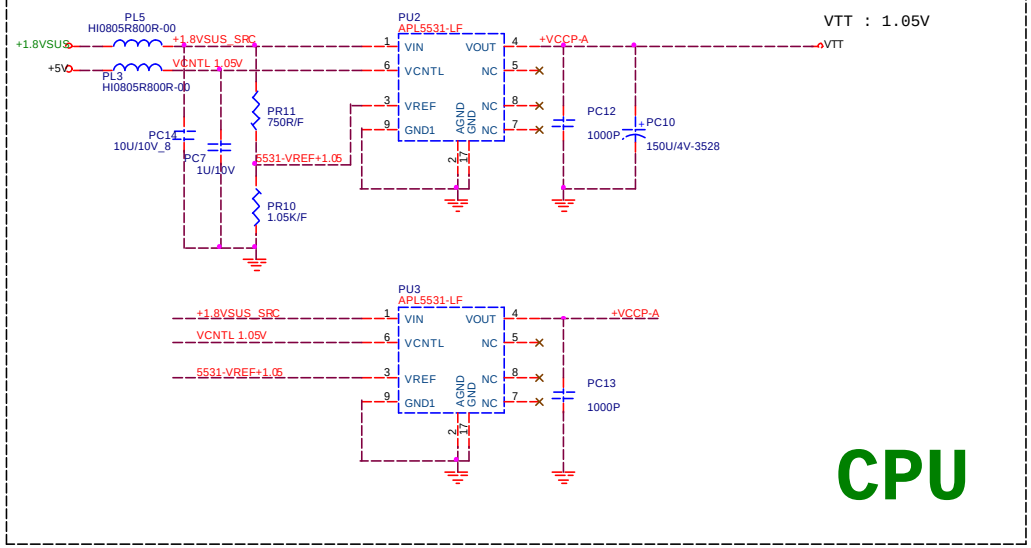
DCD



CLG





CPU

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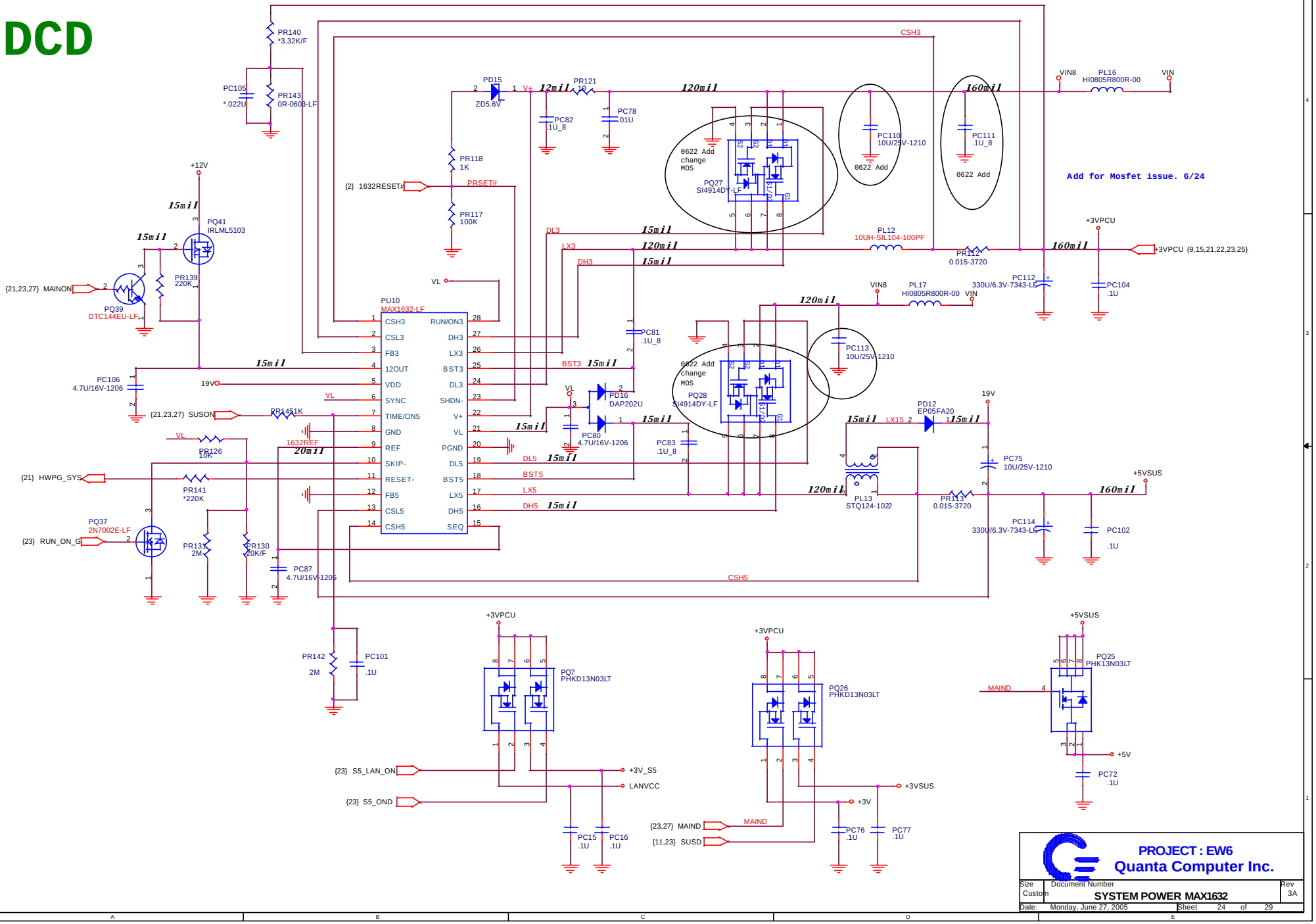
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHAGE&+1.8V	2A
Date: Monday, June 27, 2005	Sheet 23 of 29	

DCD



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	SYSTEM POWER MAX1632	3A
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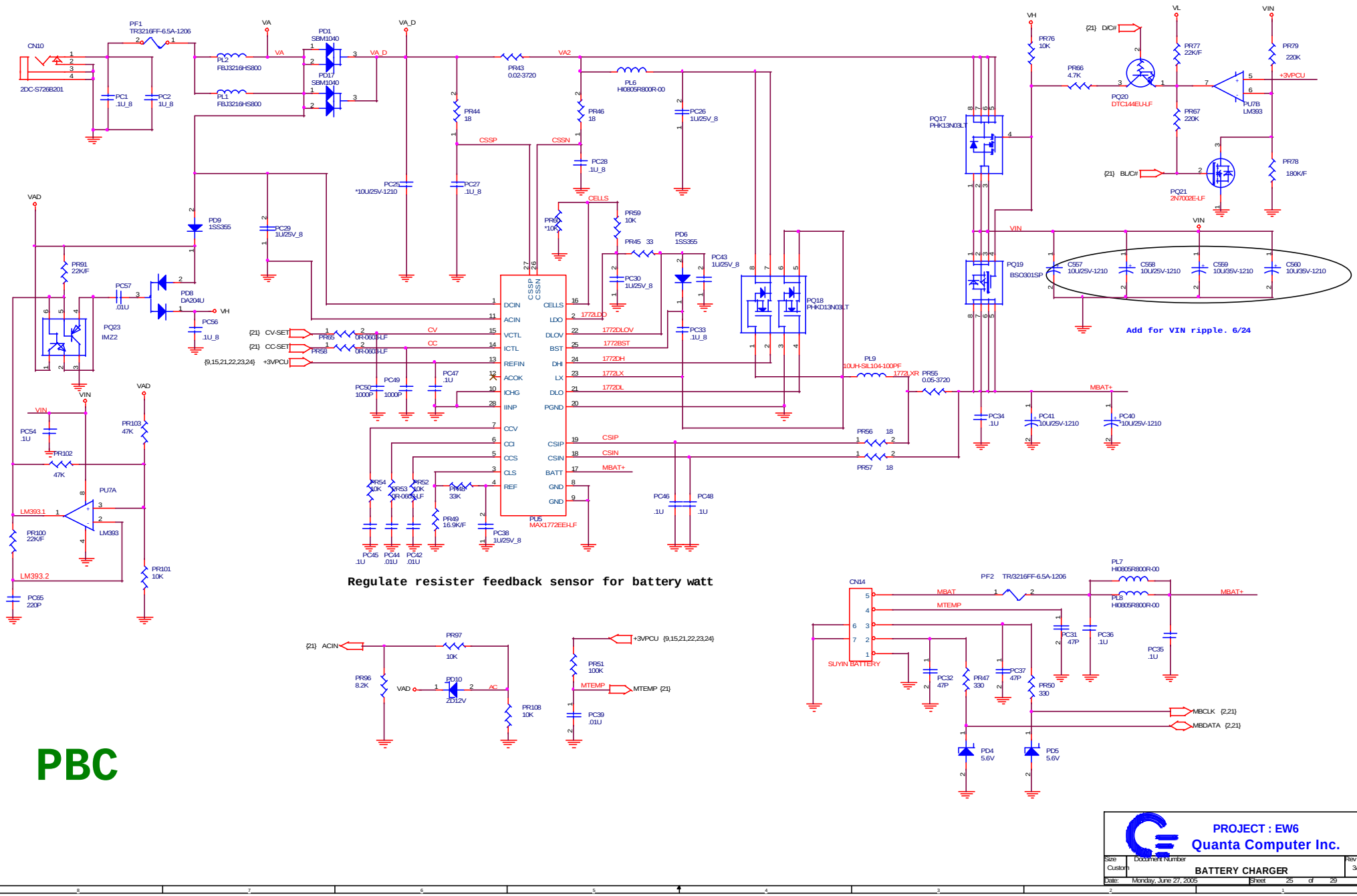

PBC

PROJECT : EW6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BATTERY CHARGER	3A
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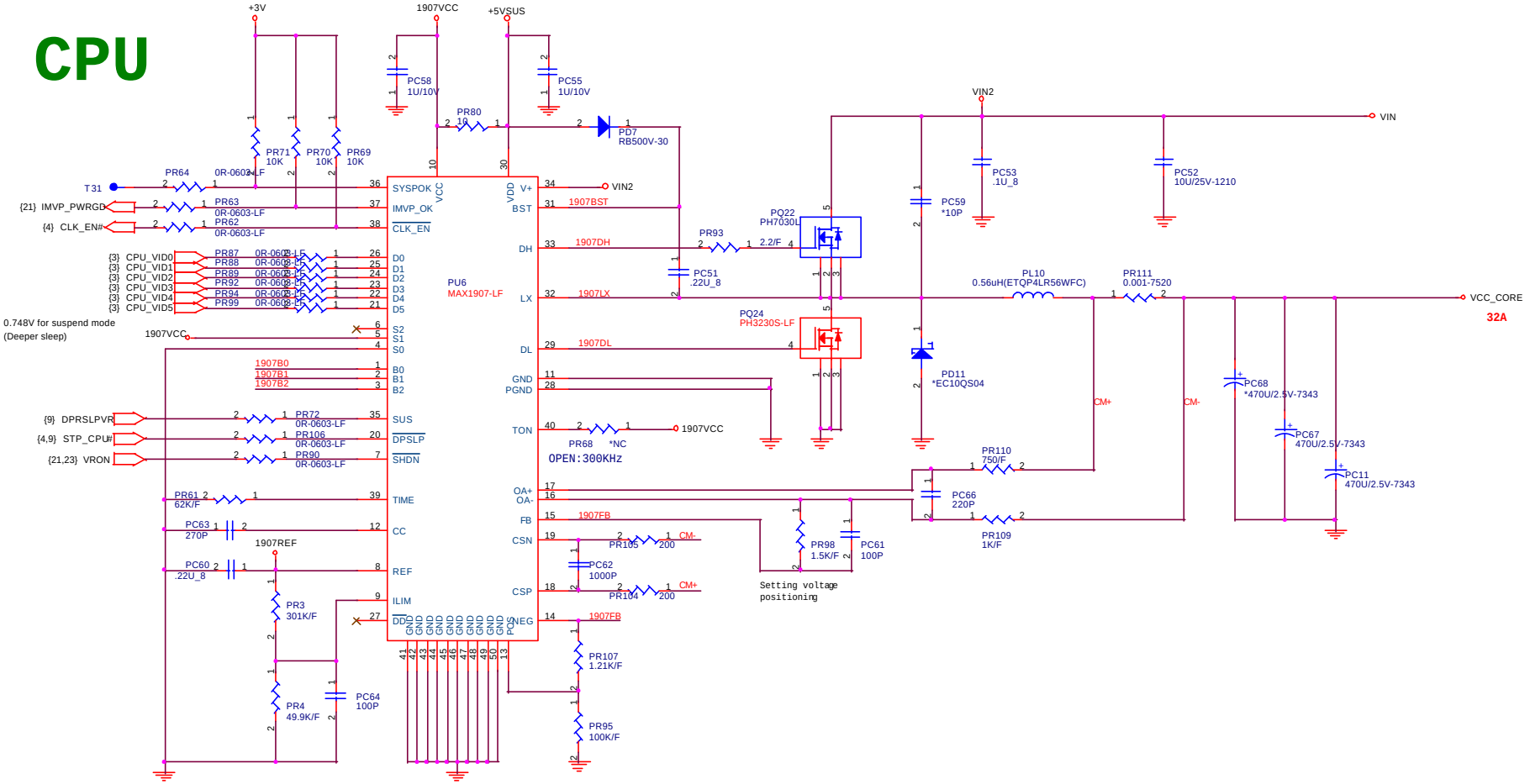
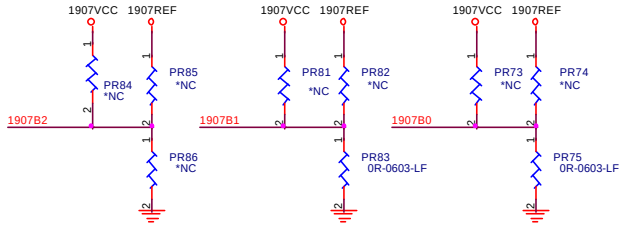
CPU





Setting boot voltage=1.2V

SUSPEND MODE (SUS=HIGH)

S2	S1	S0	Output
OPEN	VCC	GND	0.748V

VCC_BOOT

B2	B1	B0	Output
OPEN	GND	GND	1.708V
REF	REF	REF	1.372V
OPEN	OPEN	OPEN	1.036V
VCC	VCC	VCC	0.700V
REF	VCC	VCC	1.212V

D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V
1	0	0	0	0	1	1.180V
1	0	0	0	1	0	1.164V
1	0	0	0	1	1	1.148V
1	0	0	1	0	0	1.132V
1	0	0	1	0	1	1.116V
1	0	0	1	1	0	1.100V
1	0	0	1	1	1	1.084V
1	0	1	0	0	0	1.068V
1	0	1	0	0	1	1.052V
1	0	1	0	1	0	1.036V
1	0	1	0	1	1	1.020V
1	0	1	1	0	0	1.004V
1	0	1	1	0	1	0.988V
1	0	1	1	1	0	0.972V
1	0	1	1	1	1	0.956V
1	1	0	0	0	0	0.940V
1	1	0	0	0	1	0.924V
1	1	0	0	1	0	0.908V
1	1	0	0	1	1	0.892V
1	1	0	1	0	0	0.876V
1	1	0	1	0	1	0.860V
1	1	0	1	1	0	0.844V
1	1	0	1	1	1	0.828V
1	1	1	0	0	0	0.812V
1	1	1	0	0	1	0.796V
1	1	1	0	1	0	0.780V
1	1	1	0	1	1	0.764V
1	1	1	1	0	0	0.748V
1	1	1	1	0	1	0.732V
1	1	1	1	1	0	0.716V
1	1	1	1	1	1	0.700V

D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.708V
0	0	0	0	0	1	1.692V
0	0	0	0	1	0	1.676V
0	0	0	0	1	1	1.660V
0	0	0	1	0	0	1.644V
0	0	0	1	0	1	1.628V
0	0	0	1	1	0	1.612V
0	0	0	1	1	1	1.596V
0	0	1	0	0	0	1.580V
0	0	1	0	0	1	1.564V
0	0	1	0	1	0	1.548V
0	0	1	0	1	1	1.532V
0	0	1	1	0	0	1.516V
0	0	1	1	0	1	1.500V
0	0	1	1	1	0	1.484V
0	0	1	1	1	1	1.468V
0	1	0	0	0	0	1.452V
0	1	0	0	0	1	1.436V
0	1	0	0	1	0	1.420V
0	1	0	0	1	1	1.404V
0	1	0	1	0	0	1.388V
0	1	0	1	0	1	1.372V
0	1	0	1	1	0	1.356V
0	1	0	1	1	1	1.340V
0	1	1	0	0	0	1.324V
0	1	1	0	0	1	1.308V
0	1	1	0	1	0	1.292V
0	1	1	0	1	1	1.276V
0	1	1	1	0	0	1.260V
0	1	1	1	0	1	1.244V
0	1	1	1	1	0	1.228V
0	1	1	1	1	1	1.212V

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Custom	CPU CORE	1A
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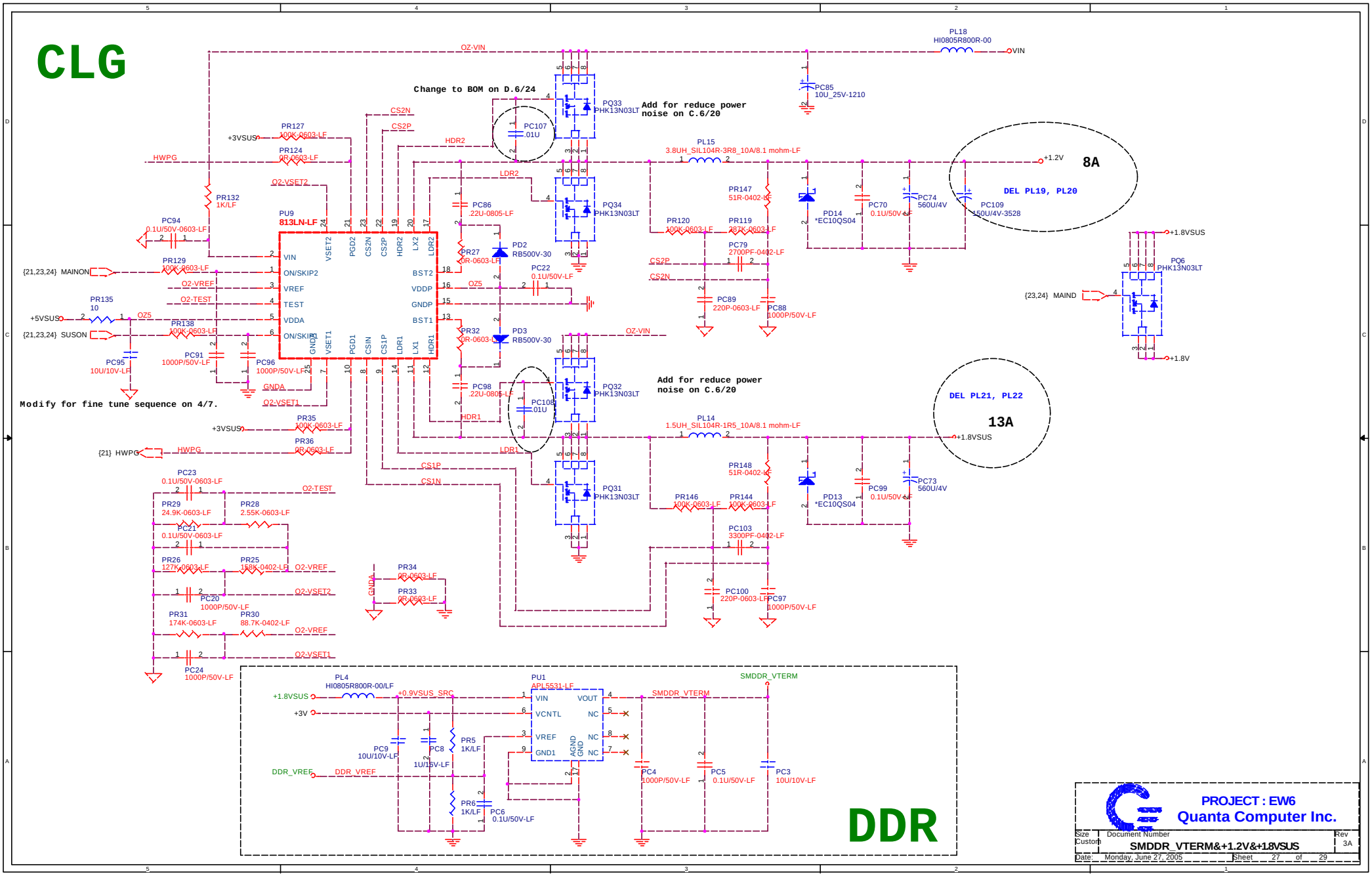
CLG
Change to BOM on D.6/24
Add for reduce power noise on C.6/20
Add for reduce power noise on C.6/20
Modify for fine tune sequence on 4/7.
DEL PL19, PL20
8A
DEL PL21, PL22
13A
DDR
PROJECT : EW6
Quanta Computer Inc.
SMDDR_VTERM&+1.2V&+1.8VSUS
Monday, June 27, 2005