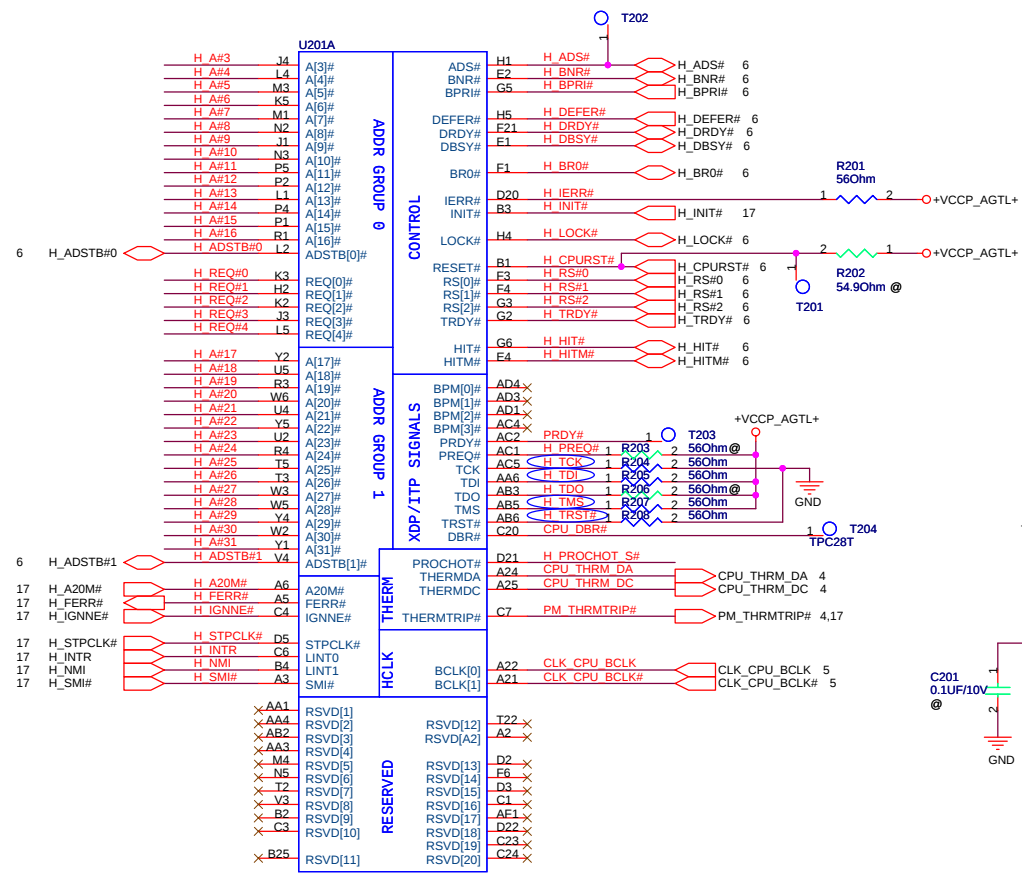


FAN + SENSOR ADM1032ARMZ	PAGE 4
CLOCK GEN ICS954310	PAGE 5
DISCHARGER CIRCUIT	PAGE 37
Power On Sequence	PAGE 40
DC/BATT IN	PAGE 41
CPU VCORE	PAGE 50
SYSTEM PWR	PAGE 51
BAT & CHARGER	PAGE 57



6 H_A#16..3]
6 H_REQ#4..0]
6 H_A#31..17]



(070122)Change CPU Socket into PN=12G011204796

68 ± 5% pull-up to Vcc1_05
If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
If PROCHOT# is routed between CPU, IMVP and MCH, pull-up resistor has to be 75 Ohm ± 5%

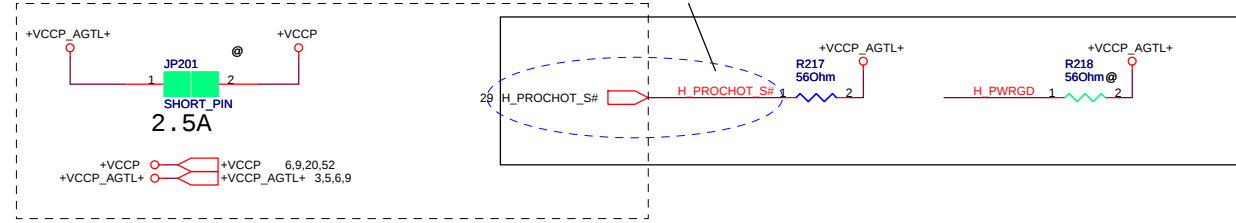
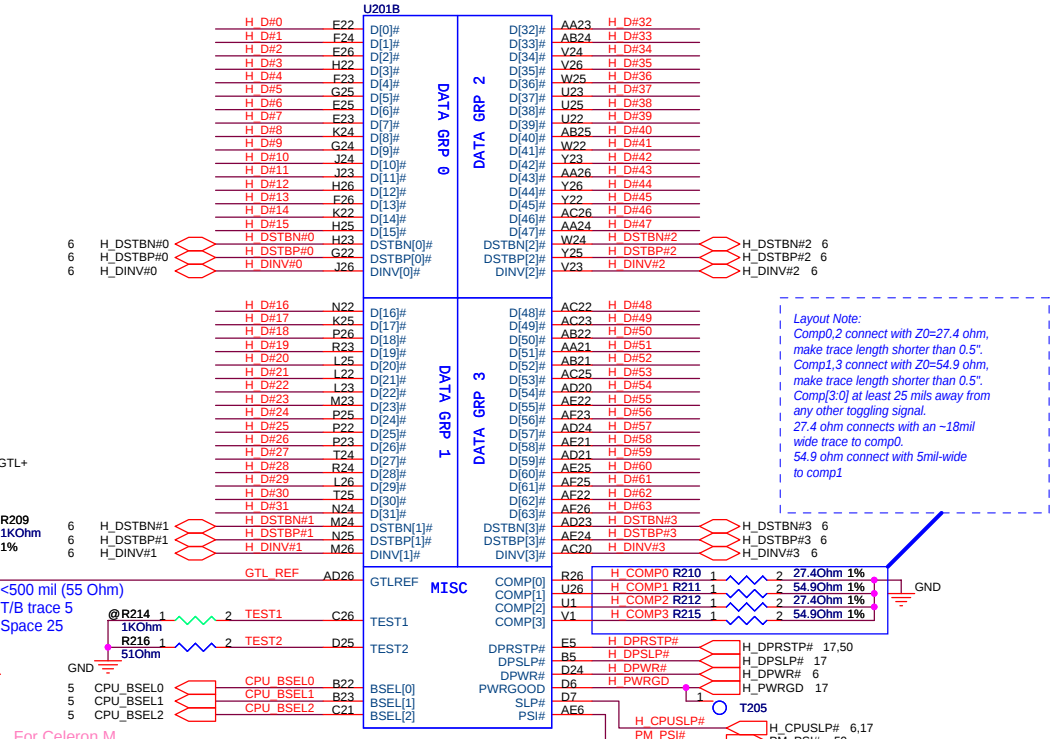


Table with 4 columns: BCLK, FSB, BSEL2, BSEL1, BSEL0. Values: 133MHz, 533MHz, L, L, H.

For Celeron M

(070122)Change CPU Socket into PN=12G011204796



Layout Note:
Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
Comp1,3 connect with Z0=54.9 ohm, make trace length shorter than 0.5".
Comp3,0 at least 25 mils away from any other toggling signal.
27.4 ohm connects with an ~18mil wide trace to comp0.
54.9 ohm connect with 5mil-wide to comp1

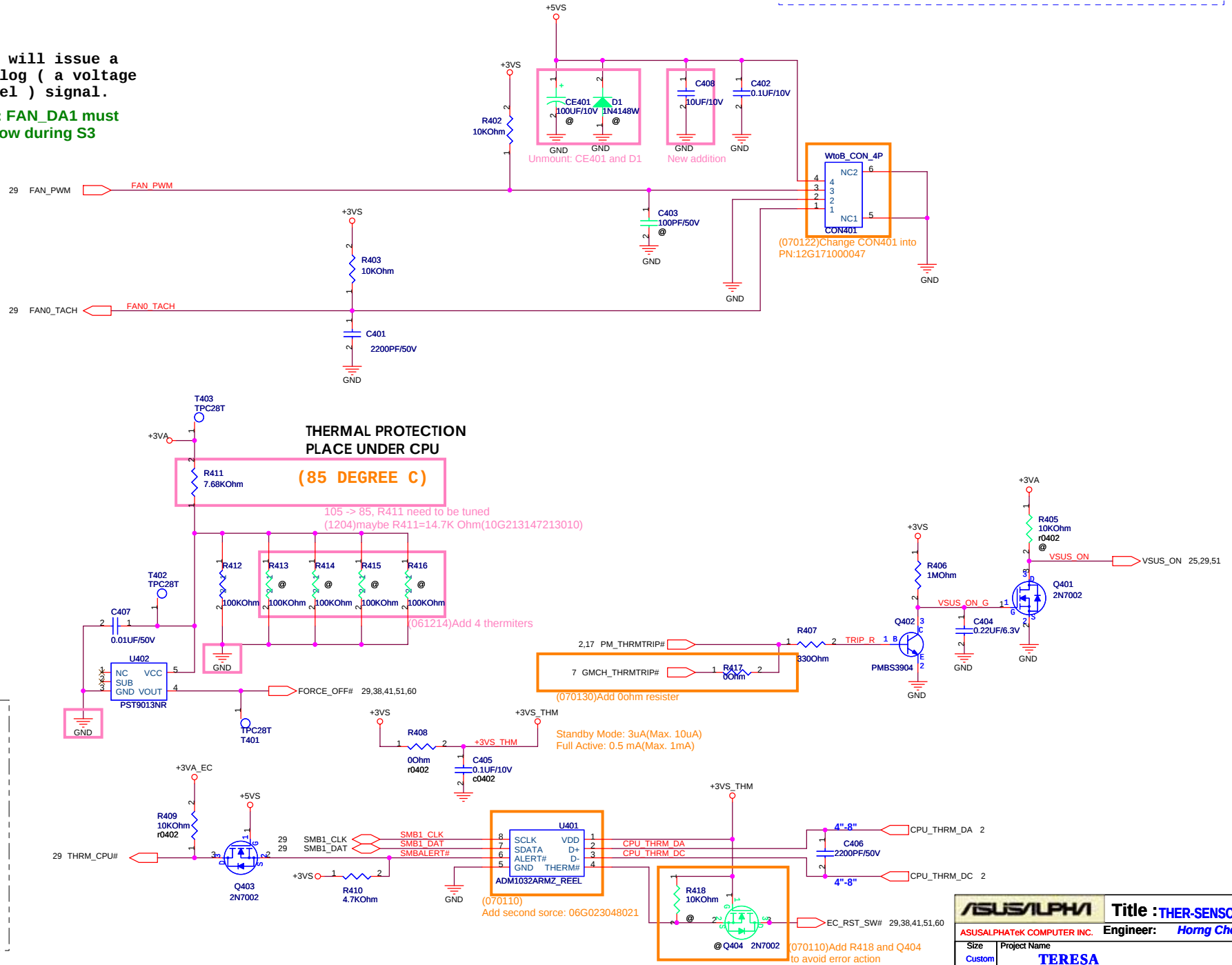
Celeron M FSB:533MHz	MIN	TYP	MAX
VCCP	0.997V	1.05V	1.102V
	MIN	TYP	MAX
ICCP			2.5A

ASUS/ALPHA		Title : <i>Yonah CPU (2)</i>	
ASUSALPHATeK COMPUTER INC.		Engineer: <i>Hornig Chou</i>	
Size <i>Custom</i>	Project Name TERESA	Rev <i>1.1</i>	
Date: <i>Monday, February 05, 2007</i>	Sheet	<i>3</i>	of <i>57</i>

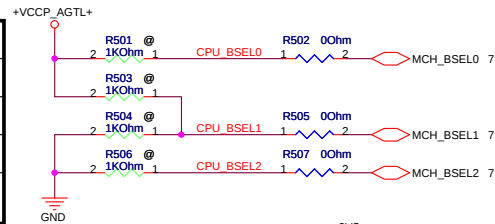
Fan Speed Control

KBC will issue a
analog (a voltage
level) signal.

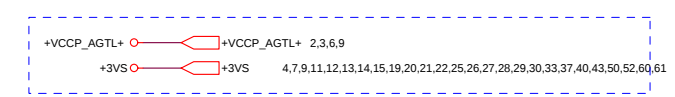
SW: FAN_DA1 must
be low during S3



Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#), PCIE7(#)	CLK_MCH_3GPLL(#)



Bclk	FSB	FSLC	FSLB	FSLA
133	533	L	L	H
166	667	L	H	H



Layout Note:
Place termination close to source IC

(070130)Change C516 from 27PF to 33PF

Delete CLK_I7MPC1(connect to pins)

SELPICIE0_LCD#:
0-->pin17, pin18=LCDCLK(96MHz) or 27M/27M_SS

SELLCD_27#/PCICLK_F1:
1-->pin17, pin18=LCDCLK(96MHz)

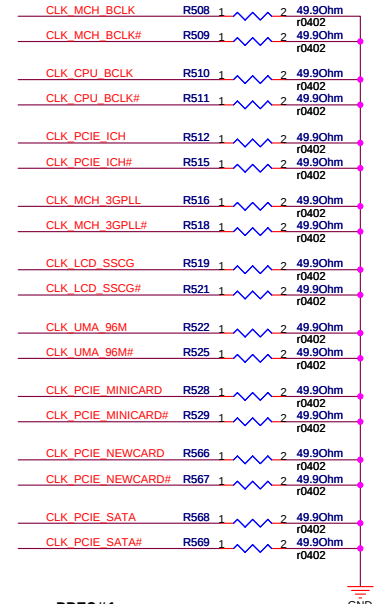
PCICLK2/REQ_SEL:
1-->pin40, pin41=PREQ1#, PREQ2#

ITP_EN/PCICLK_F0:
1-->CPU_ITP pair

Realtek:Mount R519, Remove R550 R534

Internal Pull-Up Resistor

Internal Pull-Down Resistor



PREQ#1
0=PCIE X 6/0 Not Controlled
1=PCIE X 6/0 Controlled

PREQ#2
0=PCIE X 8/1 Not Controlled
1=PCIE X 8/1 Controlled

PREQ#3
0=PCIE X 4/2 Not Controlled
1=PCIE X 4/2 Controlled

PREQ#4
0=PCIE X 7/5/3 Not Controlled
1=PCIE X 7/5/3 Controlled

U601A

H_D#0 F1 H_D#_0
H_D#1 J1 H_D#_1
H_D#2 H1 H_D#_2
H_D#3 J6 H_D#_3
H_D#4 H3 H_D#_4
H_D#5 K2 H_D#_5
H_D#6 G1 H_D#_6
H_D#7 G2 H_D#_7
H_D#8 K9 H_D#_8
H_D#9 K1 H_D#_9
H_D#10 K7 H_D#_10
H_D#11 J8 H_D#_11
H_D#12 H4 H_D#_12
H_D#13 J3 H_D#_13
H_D#14 K11 H_D#_14
H_D#15 G4 H_D#_15
H_D#16 T10 H_D#_16
H_D#17 W11 H_D#_17
H_D#18 T3 H_D#_18
H_D#19 U7 H_D#_19
H_D#20 U9 H_D#_20
H_D#21 U11 H_D#_21
H_D#22 T11 H_D#_22
H_D#23 W9 H_D#_23
H_D#24 T1 H_D#_24
H_D#25 T8 H_D#_25
H_D#26 T4 H_D#_26
H_D#27 W7 H_D#_27
H_D#28 U5 H_D#_28
H_D#29 T9 H_D#_29
H_D#30 W6 H_D#_30
H_D#31 T5 H_D#_31
H_D#32 AB7 H_D#_32
H_D#33 AA9 H_D#_33
H_D#34 W4 H_D#_34
H_D#35 W3 H_D#_35
H_D#36 Y3 H_D#_36
H_D#37 Y7 H_D#_37
H_D#38 W5 H_D#_38
H_D#39 Y10 H_D#_39
H_D#40 AB8 H_D#_40
H_D#41 W2 H_D#_41
H_D#42 AA4 H_D#_42
H_D#43 AA7 H_D#_43
H_D#44 AA2 H_D#_44
H_D#45 AA6 H_D#_45
H_D#46 AA10 H_D#_46
H_D#47 Y8 H_D#_47
H_D#48 AA1 H_D#_48
H_D#49 AB4 H_D#_49
H_D#50 AC9 H_D#_50
H_D#51 AB11 H_D#_51
H_D#52 AC11 H_D#_52
H_D#53 AB3 H_D#_53
H_D#54 AC2 H_D#_54
H_D#55 AD1 H_D#_55
H_D#56 AD9 H_D#_56
H_D#57 AC1 H_D#_57
H_D#58 AD7 H_D#_58
H_D#59 AC6 H_D#_59
H_D#60 AB5 H_D#_60
H_D#61 AD10 H_D#_61
H_D#62 AD4 H_D#_62
H_D#63 AC8 H_D#_63

H_XRCOMP E1 H_XRCOMP
H_XSCOMP E2 H_XSCOMP
H_XSWING E4 H_XSWING
H_YRCOMP Y1 H_YRCOMP
H_YSCOMP U1 H_YSCOMP
H_YSWING W1 H_YSWING

5 CLK_MCH_BCLK AG2
5 CLK_MCH_BCLK# AG1

CALISTOGA_Q137

HOST

H_A#_3 H9 H_A#3
H_A#_4 C9 H_A#4
H_A#_5 E11 H_A#5
H_A#_6 G11 H_A#6
H_A#_7 F11 H_A#7
H_A#_8 G12 H_A#8
H_A#_9 E9 H_A#9
H_A#_10 H11 H_A#10
H_A#_11 J12 H_A#11
H_A#_12 G14 H_A#12
H_A#_13 D9 H_A#13
H_A#_14 J14 H_A#14
H_A#_15 H13 H_A#15
H_A#_16 J15 H_A#16
H_A#_17 F14 H_A#17
H_A#_18 D12 H_A#18
H_A#_19 A11 H_A#19
H_A#_20 C11 H_A#20
H_A#_21 A12 H_A#21
H_A#_22 A13 H_A#22
H_A#_23 E13 H_A#23
H_A#_24 G13 H_A#24
H_A#_25 F12 H_A#25
H_A#_26 B12 H_A#26
H_A#_27 C12 H_A#27
H_A#_28 A14 H_A#28
H_A#_29 C14 H_A#29
H_A#_30 D14 H_A#30
H_A#_31

H_ADS# E8 H_ADS# 2
H_ADSTB#0 B9 H_ADSTB#0 2
H_ADSTB#1 C13 H_ADSTB#1 2
H_AVREF J13 H_VREF
H_BNR# C6 H_BNR# 2
H_BPRI# F6 H_BPRI# 2
H_BR0# C7 H_BR0# 2
H_CPURST# B7 H_CPURST# 2
H_DBSY# C3 H_DBSY# 2
H_DEFER# J9 H_DEFER# 2
H_DPWR# H8 H_DPWR# 2
H_DRDY# K13 H_DRDY# 2
H_DVREF

H_DINV#0 J7 H_DINV#0 2
H_DINV#1 W8 H_DINV#1 2
H_DINV#2 U3 H_DINV#2 2
H_DINV#3 AB10 H_DINV#3 2

H_DSTBN#0 K4 H_DSTBN#0 2
H_DSTBN#1 I7 H_DSTBN#1 2
H_DSTBN#2 Y5 H_DSTBN#2 2
H_DSTBN#3 AC4 H_DSTBN#3 2

H_DSTBP#0 K3 H_DSTBP#0 2
H_DSTBP#1 T6 H_DSTBP#1 2
H_DSTBP#2 AA5 H_DSTBP#2 2
H_DSTBP#3 AC5 H_DSTBP#3 2

H_HIT# D3 H_HIT# 2
H_HITM# D4 H_HITM# 2
H_LOCK# B3 H_LOCK# 2

H_REQ#0 D8 H_REQ#0 2
H_REQ#1 G8 H_REQ#1 2
H_REQ#2 B8 H_REQ#2 2
H_REQ#3 E8 H_REQ#3 2
H_REQ#4 A8 H_REQ#4 2

H_RS#0 B4 H_RS#0 2
H_RS#1 E6 H_RS#1 2
H_RS#2 D6 H_RS#2 2

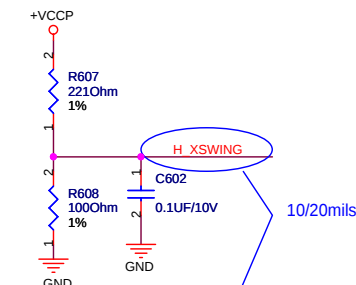
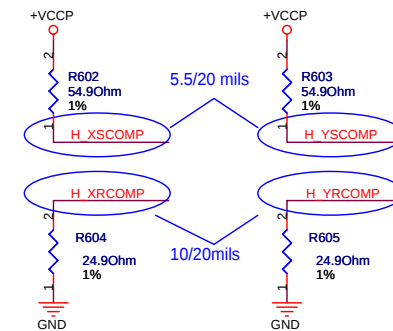
H_SLPCPU# E3 H_SLPCPU# 2
H_TRDY# E7 H_TRDY# 2

+VCCP AGTL+
R601 100Ohm 1%
R606 200Ohm 1%
C601 0.1UF/10V

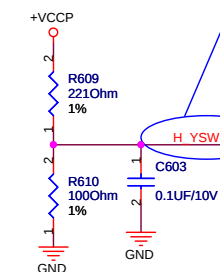
Layout Note:
0.1uF should be placed 100mils or less from GMCH pin.

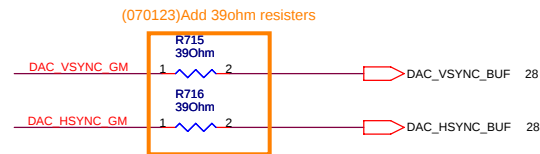
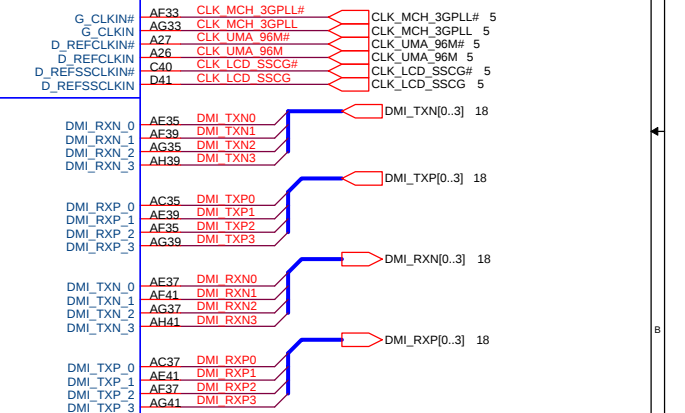
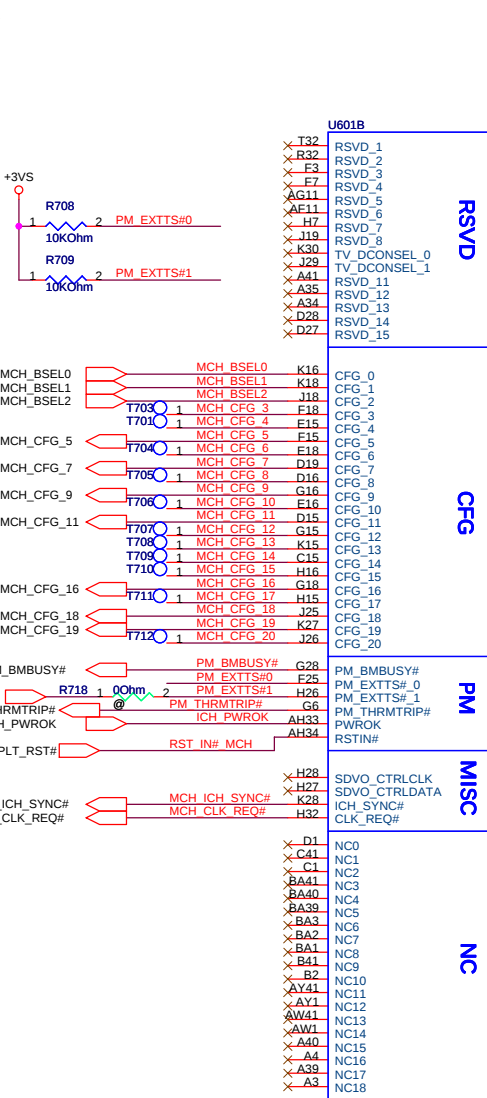
R611 00hm

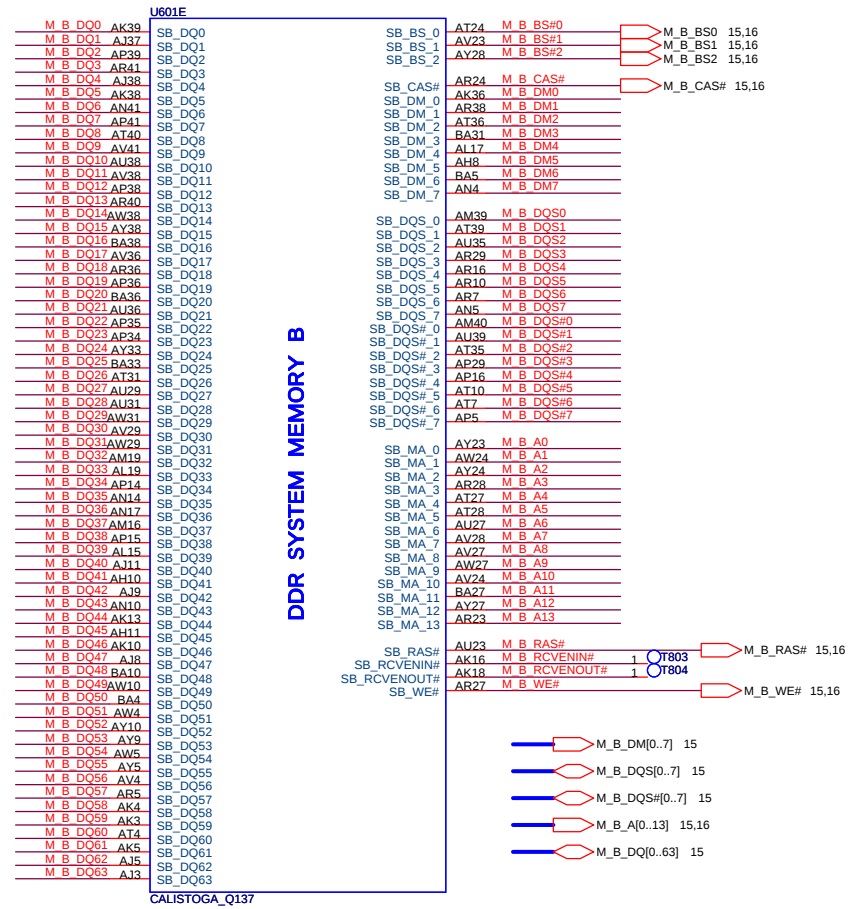
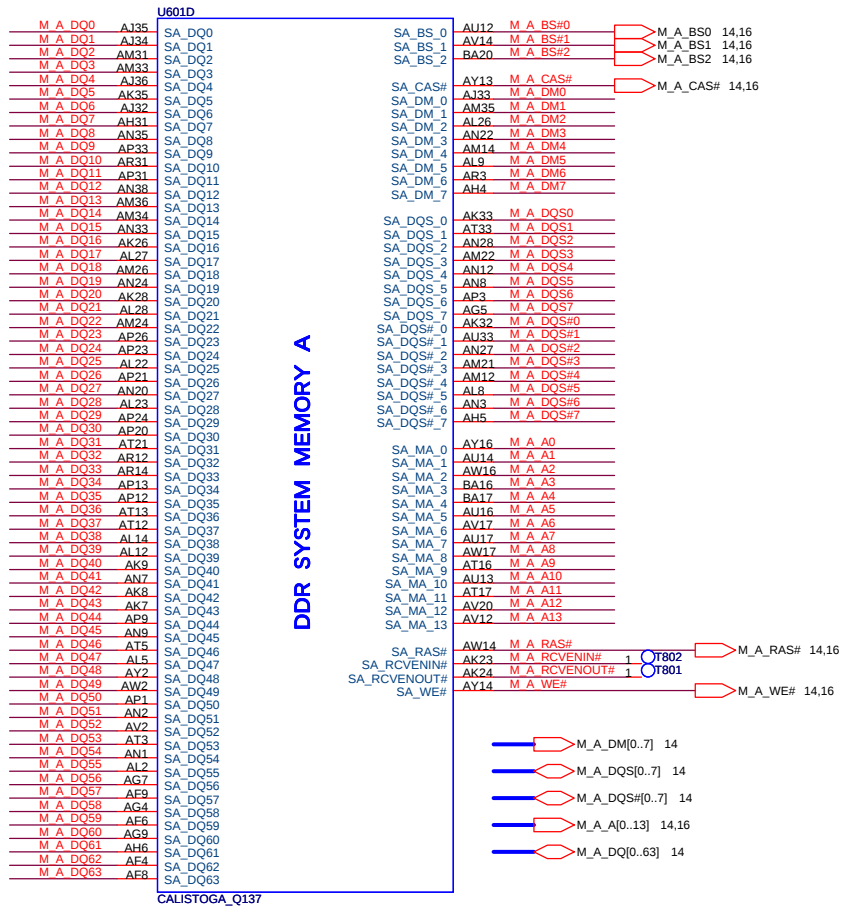
+VCCP +VCCP 2,9,20,52
+VCCP_AGTL+ +VCCP_AGTL+ 2,3,5,9



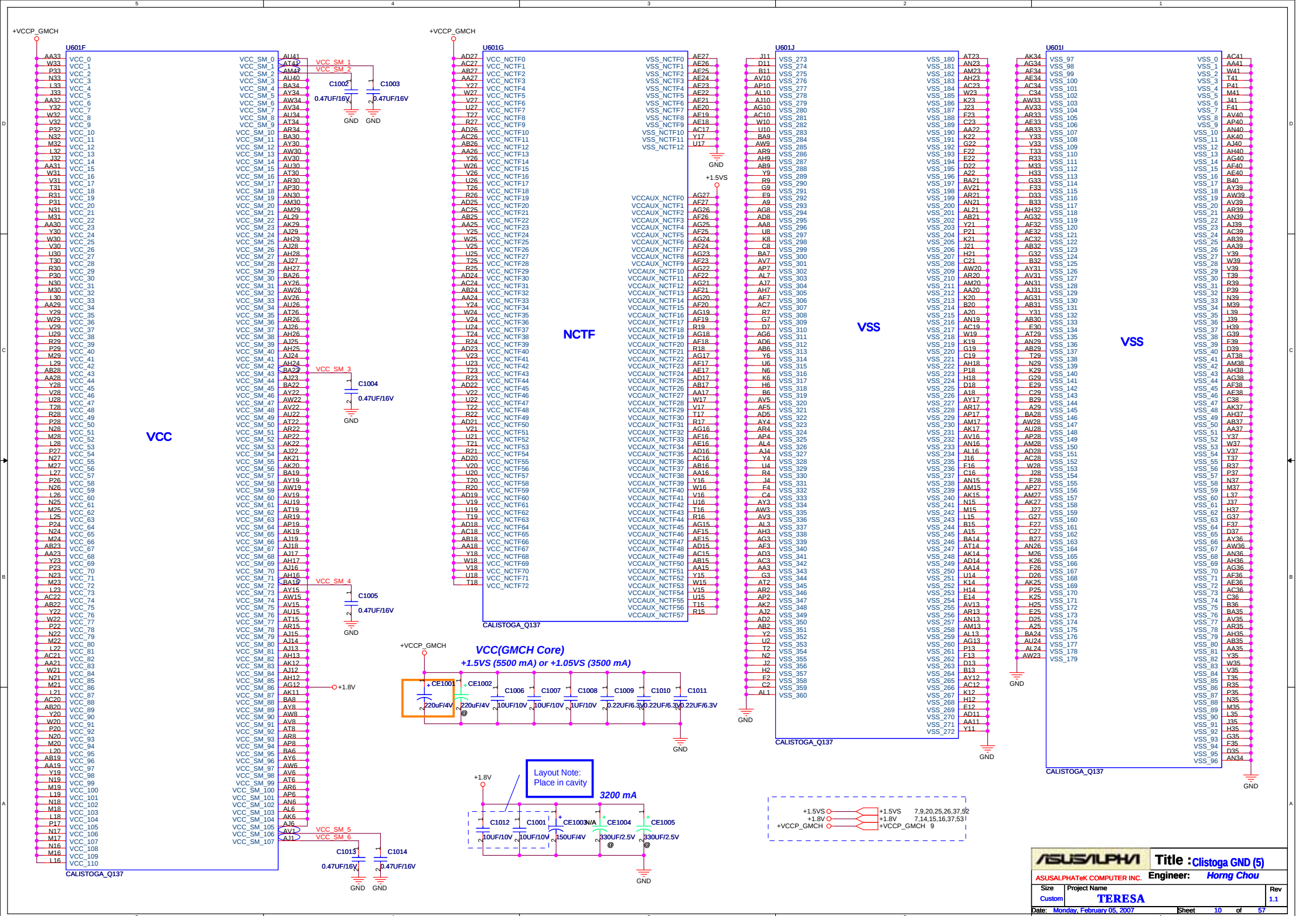
Signal voltage level =
0.3125*VCCP
Trace should be 10 mil wide
with 20 mil spacing

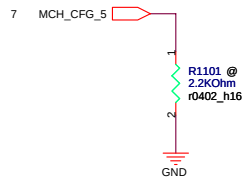




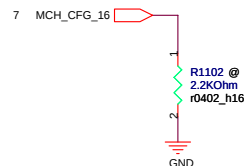




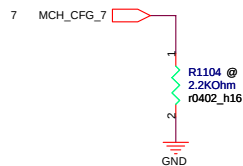




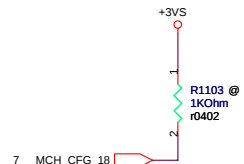
CFG5 : DMI X2 Select
 LOW = DMI X 2
HIGH = DMI X 4 (Default)



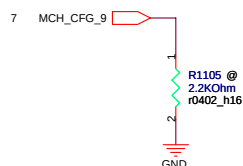
CFG16 : FSB DYNAMIC ODT
 LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



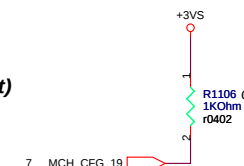
CFG7 : CPU STRAP
 LOW = Reserved
HIGH = Mobility CPU (Default)



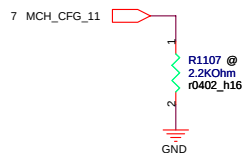
CFG18 : GMCH Core Voltage Level
 LOW = 1.05V
HIGH = 1.5V (default)



CFG9 : PCIE GRAPHIC LANE
 LOW = REVERSE LANES
HIGH = NORMAL OPERATION (Default)



CFG19 : DMI LANE REVERSAL
 LOW = NORMAL
 HIGH = LANES REVERSED



CFG11 : Reserved but need to be pull low

(061215)Remove +2.5VS power supply

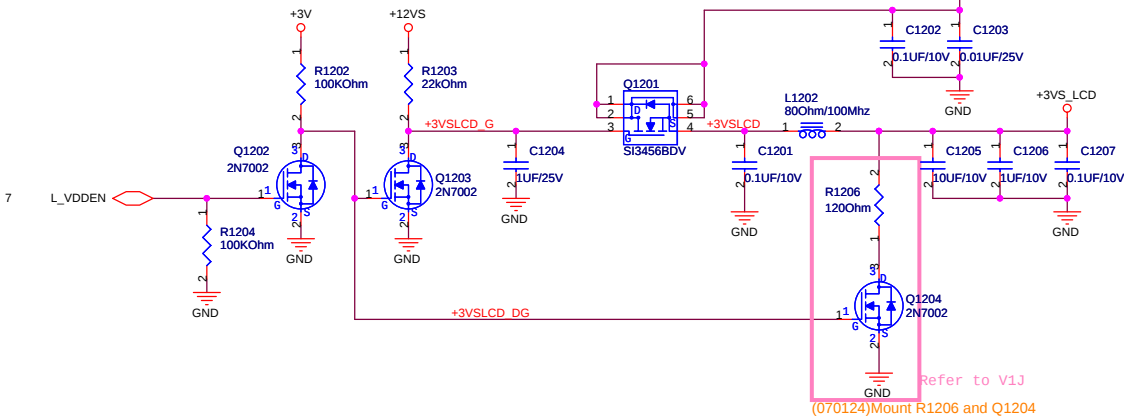
CFG[17..3] have internal pullup resistors.
 CFG[19..18] have internal pulldown resistors.
 SDVOCRTL_DATA has internal pulldown resistors.

CFG		All are sampled with respect to the leading edge of the GMCH PWROK
2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4 (Default)
6		
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal (Default)
11:10		
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_C TRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

LCD Panel Power

3~3.6V
Full Active: 410 mA(Max. 500 mA)
3~3.6V
S0-S1 M: 410 mA(Max. 500 mA)

Remove CMOS Camera(USB4)

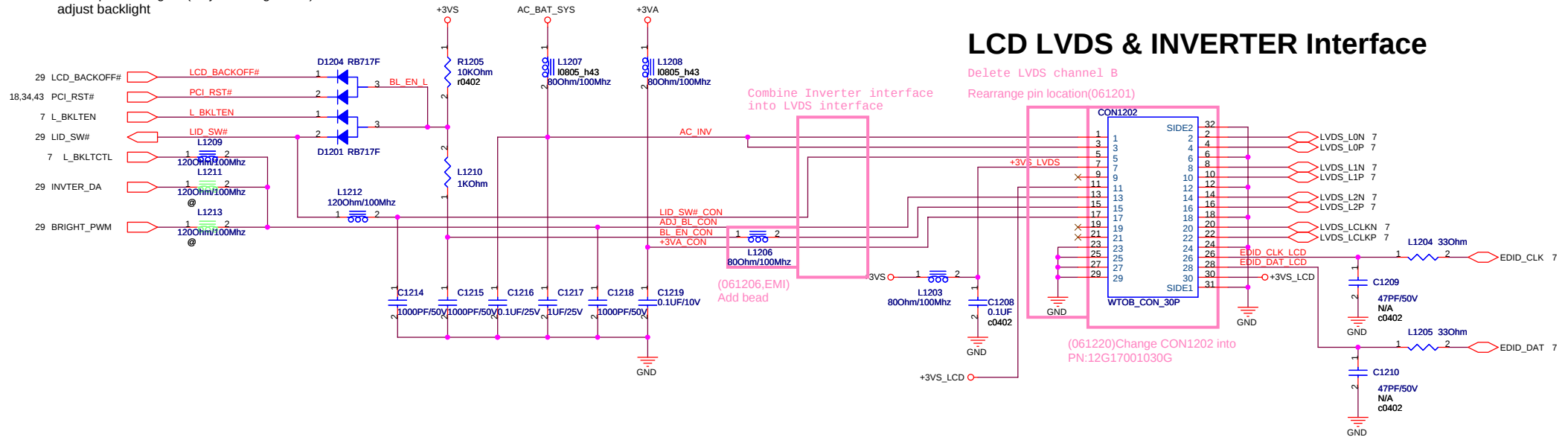


LCD Backlight Control

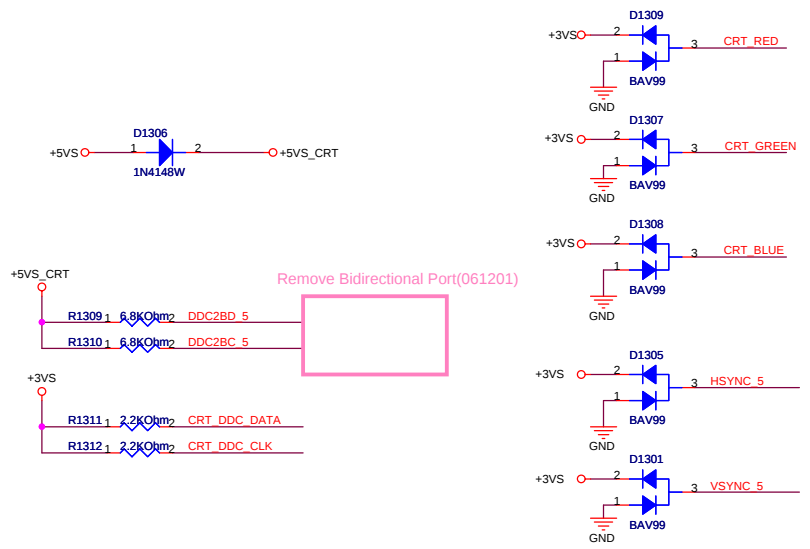
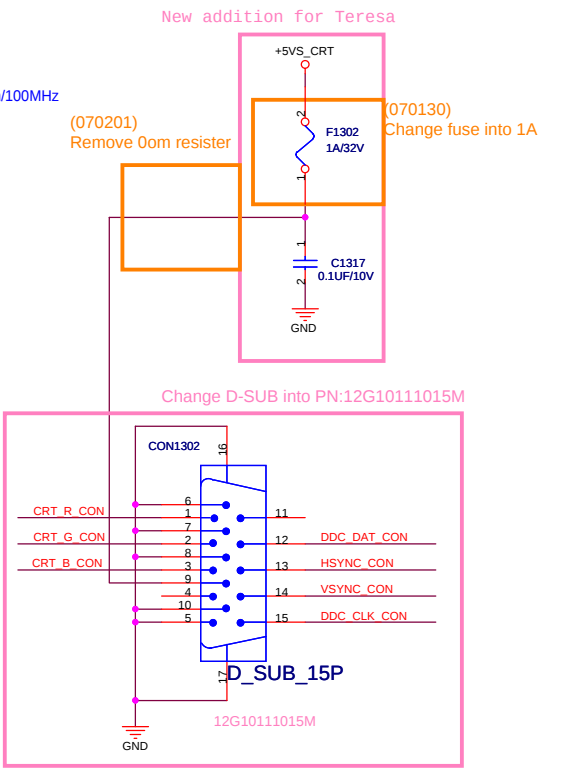
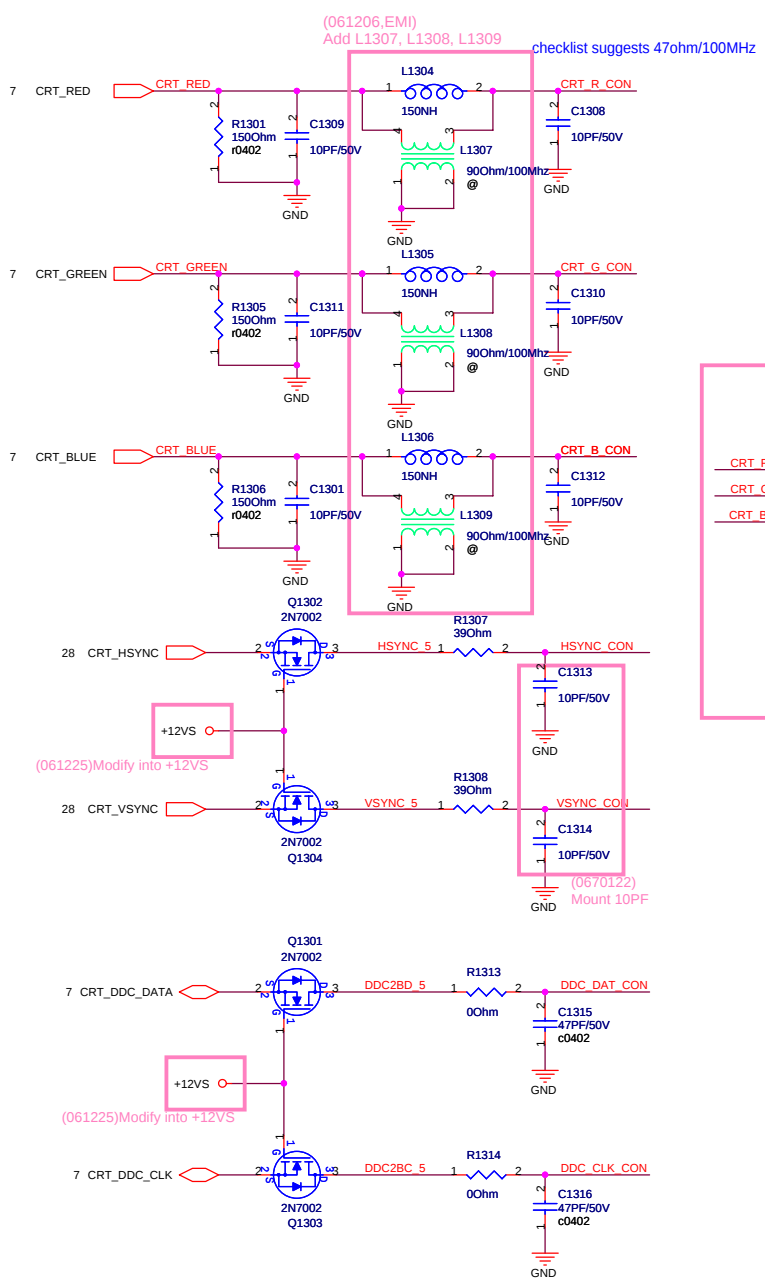
BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

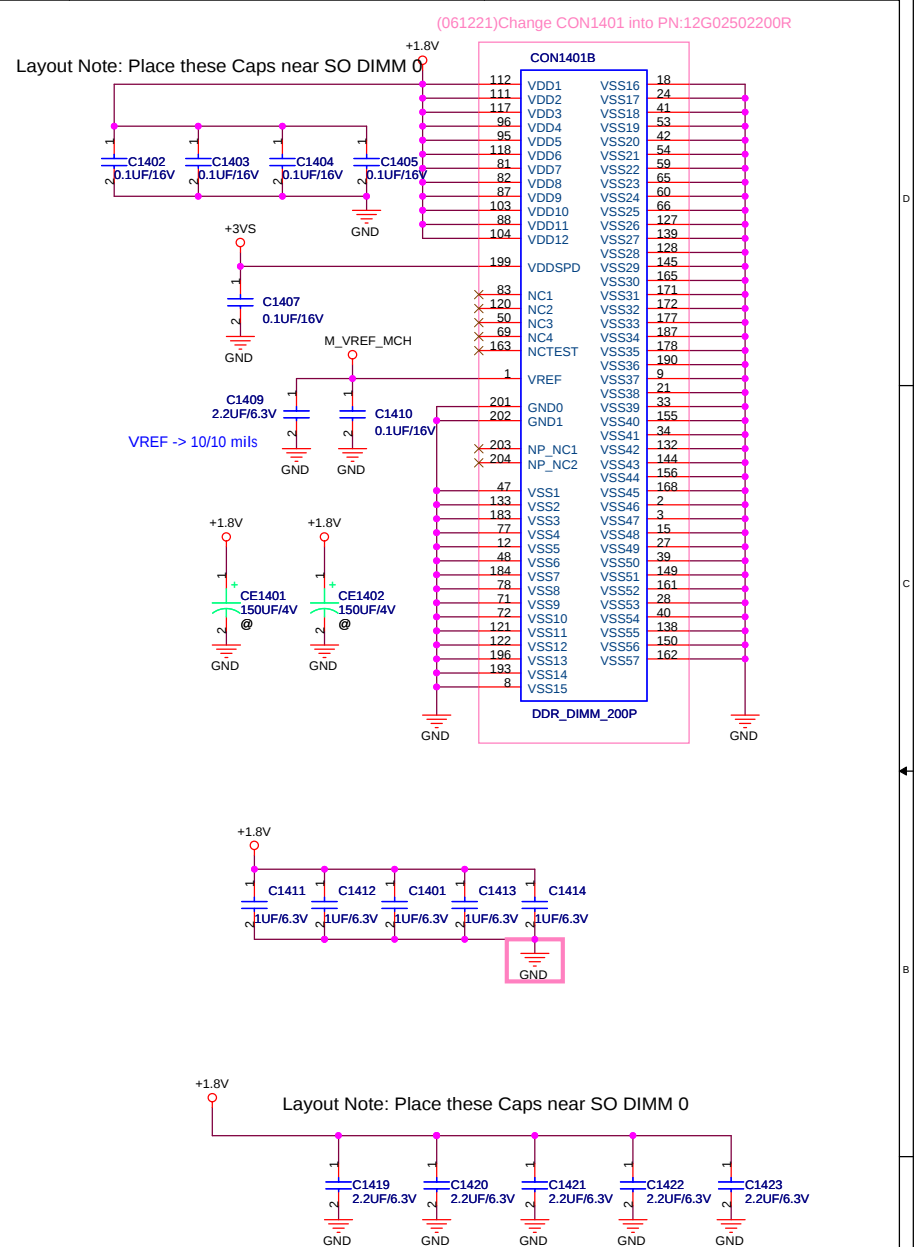
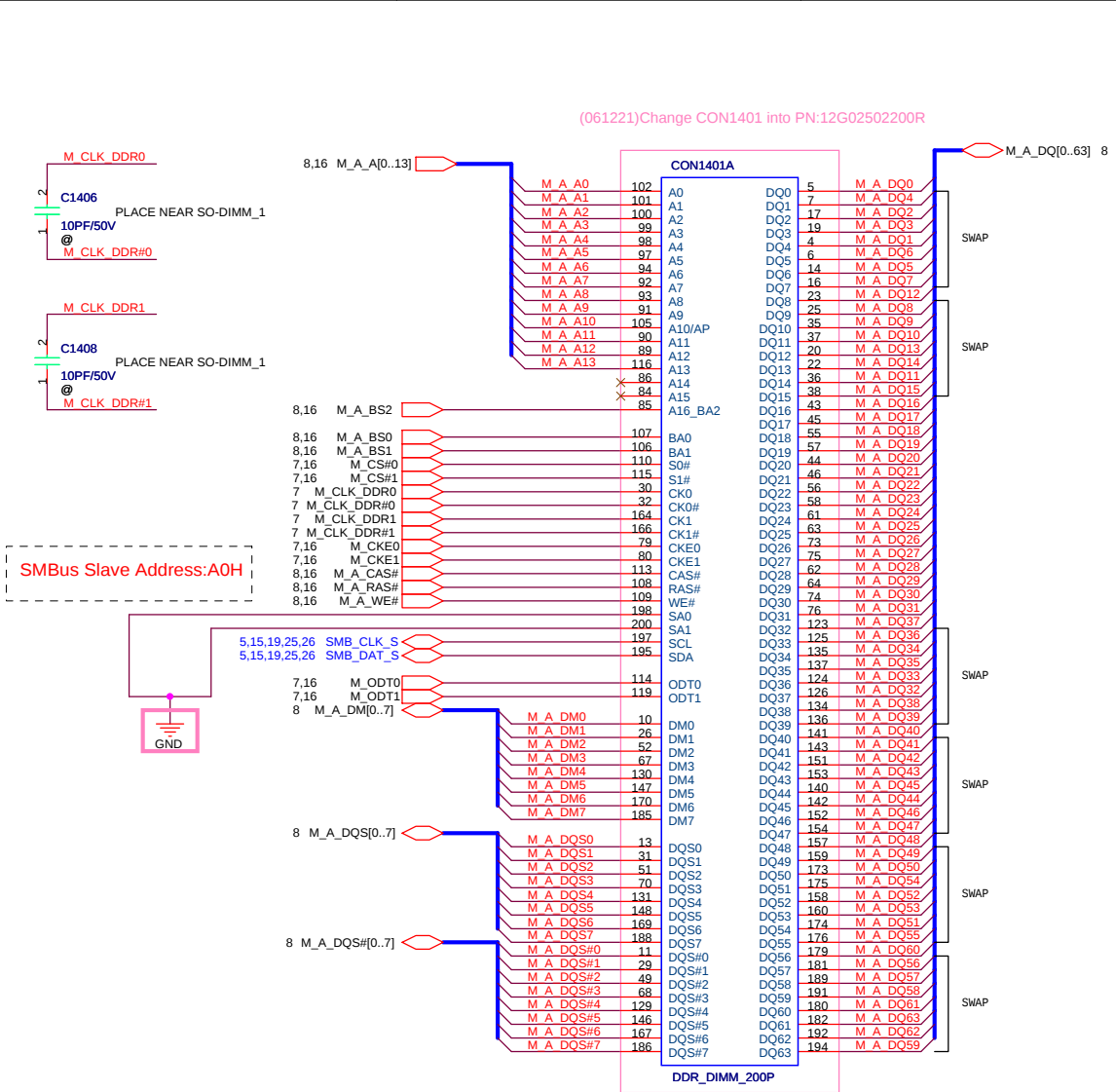
EC
INVTER_DA:
EC output D/A signal (adjust voltage level) to
adjust backlight

**Inverter Board
built in 15.4W
LCD Panel**



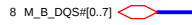
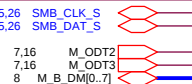
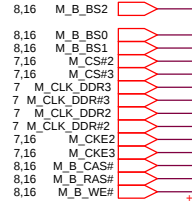
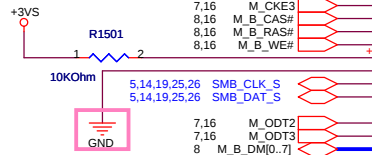
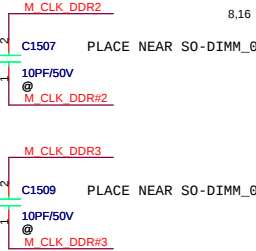
CRT OUT



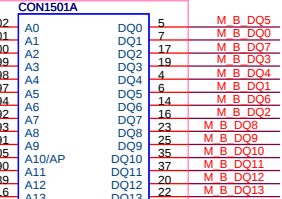


SO-DIMM 0 is placed farther from the GMCH than SO-DIMM 1

SMBus Slave Address:A4H

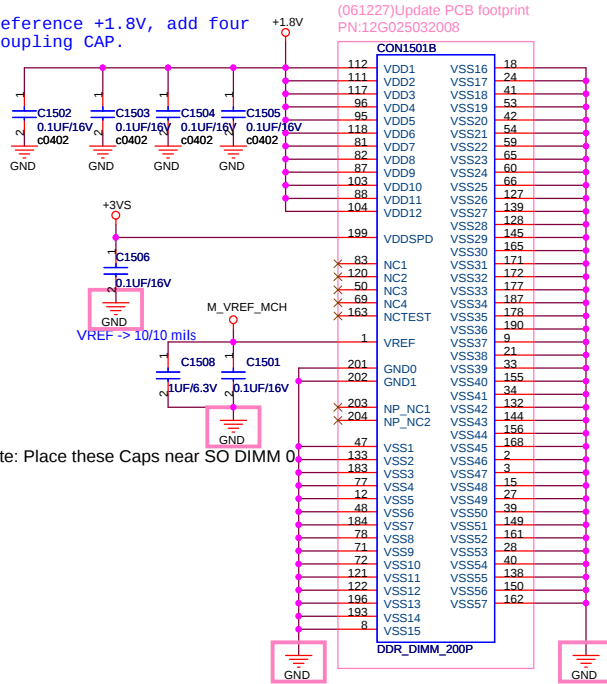


(061227)Update PCB footprint
PN:12G025032008



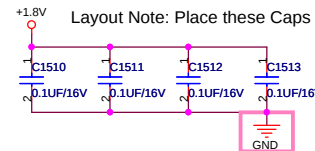
DDR_DIMM_200P

Address reference +1.8V, add four
0.1uF decoupling CAP.

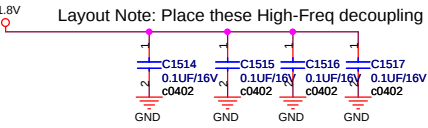


Layout Note: Place these Caps near SO DIMM 0

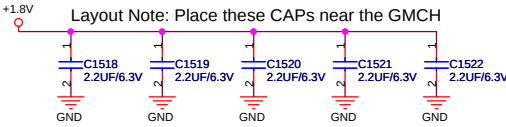
Layout Note: Place these Caps near SO DIMM 0

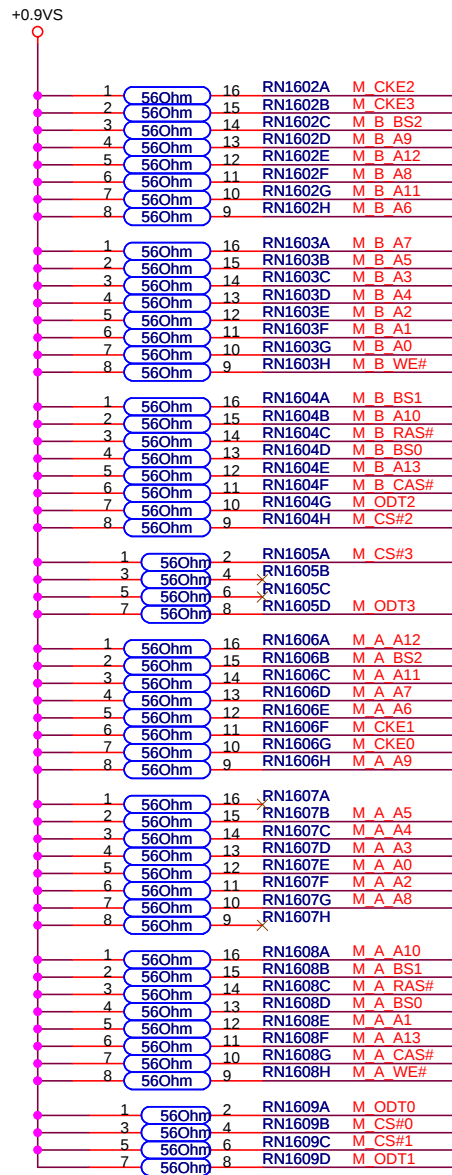


Layout Note: Place these High-Freq decoupling Caps near the GMCH



Layout Note: Place these CAPS near the GMCH





M_A_A[0..13] 8,14
M_A_BS[0..2] 8,14

M_A_CAS# 8,14
M_A_RAS# 8,14
M_A_WE# 8,14

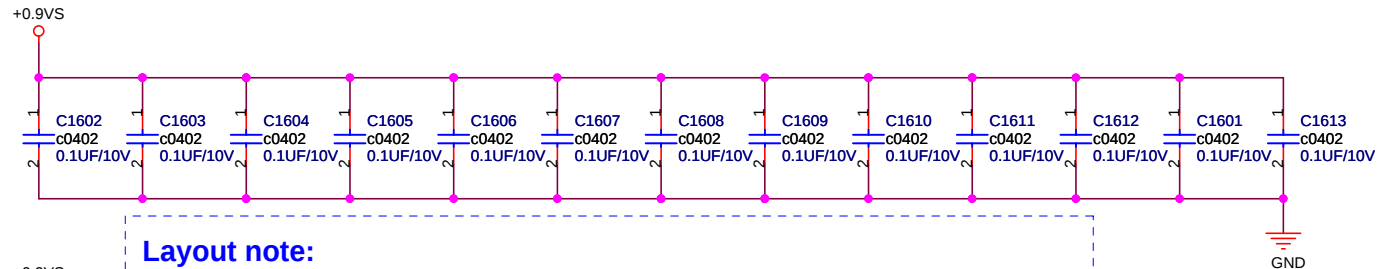
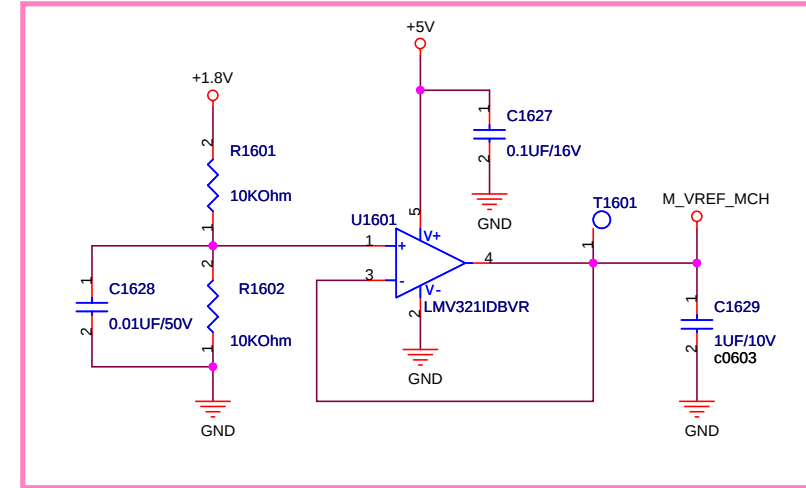
M_B_A[0..13] 8,15
M_B_BS[0..2] 8,15

M_B_CAS# 8,15
M_B_RAS# 8,15
M_B_WE# 8,15

M_CS#[0..3] 7,14,15
M_ODT[0..3] 7,14,15
M_CKE[0..3] 7,14,15

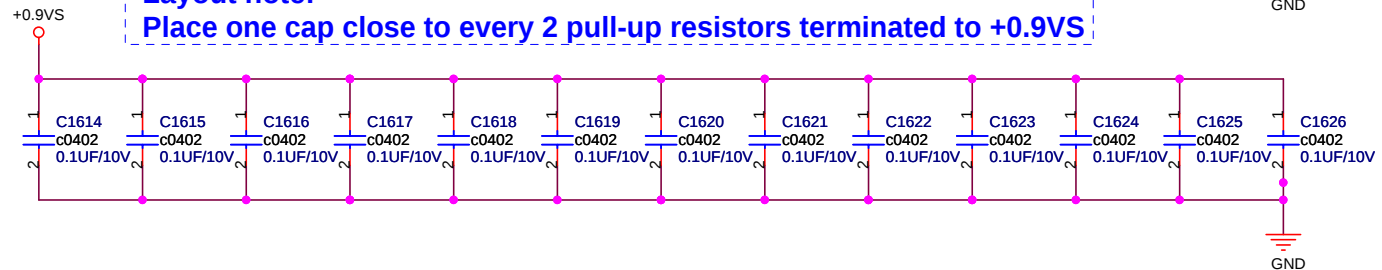
M_VREF_MCH
+0.9VS
M_VREF_MCH 7,14,15
+0.9VS 37,53

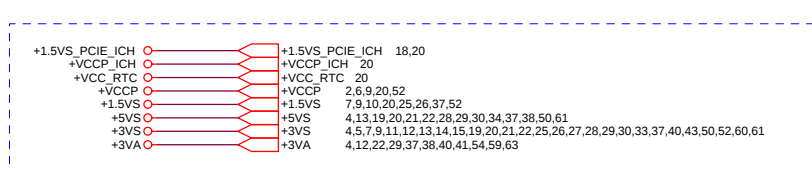
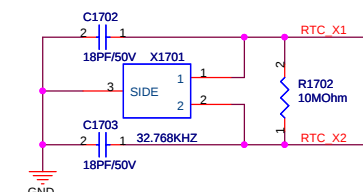
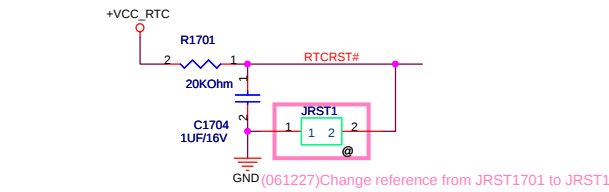
Add Voltage Follower



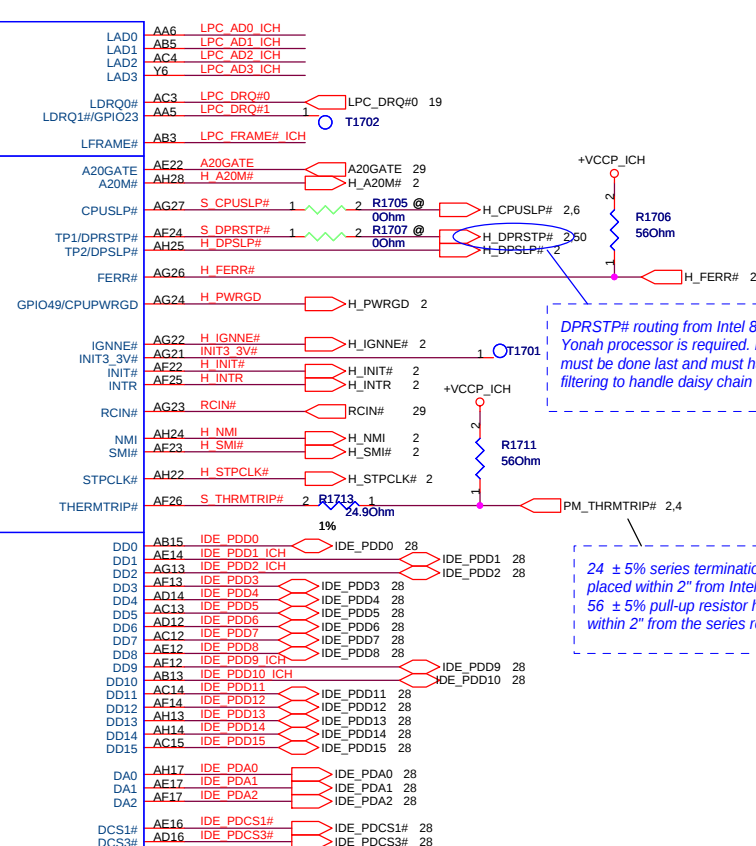
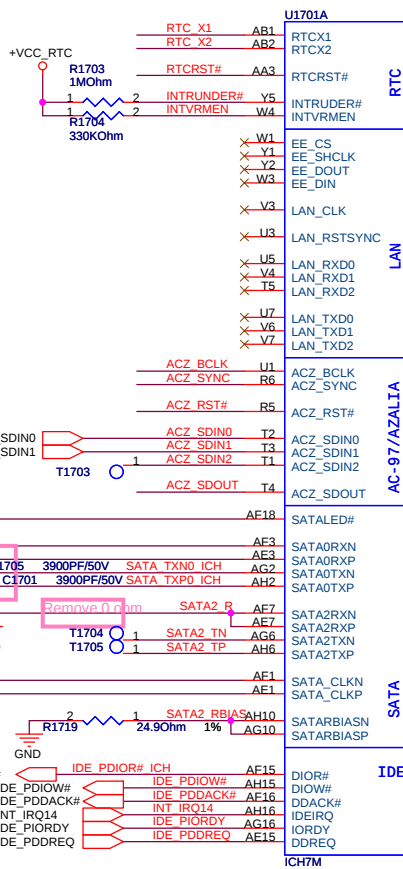
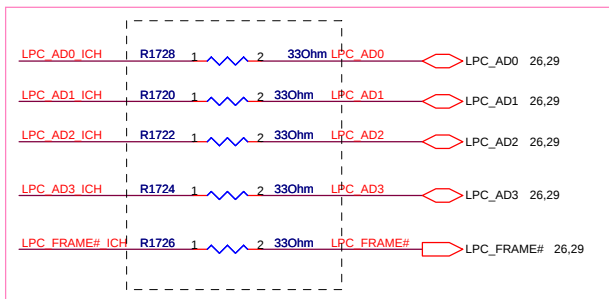
Layout note:

Place one cap close to every 2 pull-up resistors terminated to +0.9VS



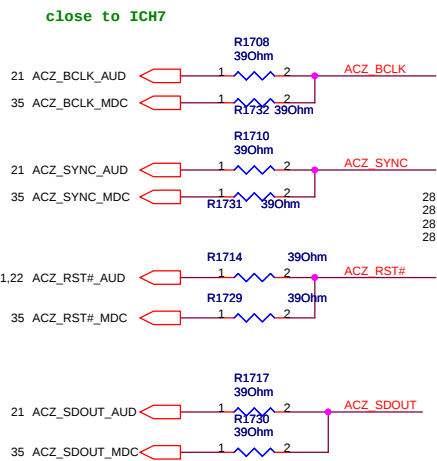


Delete LPC interface of TPM



DPRSTP# routing from Intel 82801GBM to Yonah processor is required. Routing to VR must be done last and must have de-bounce filtering to handle daisy chain topology.

24 ± 5% series termination resistor placed within 2" from Intel 82801GBM, 56 ± 5% pull-up resistor has to be within 2" from the series resistor



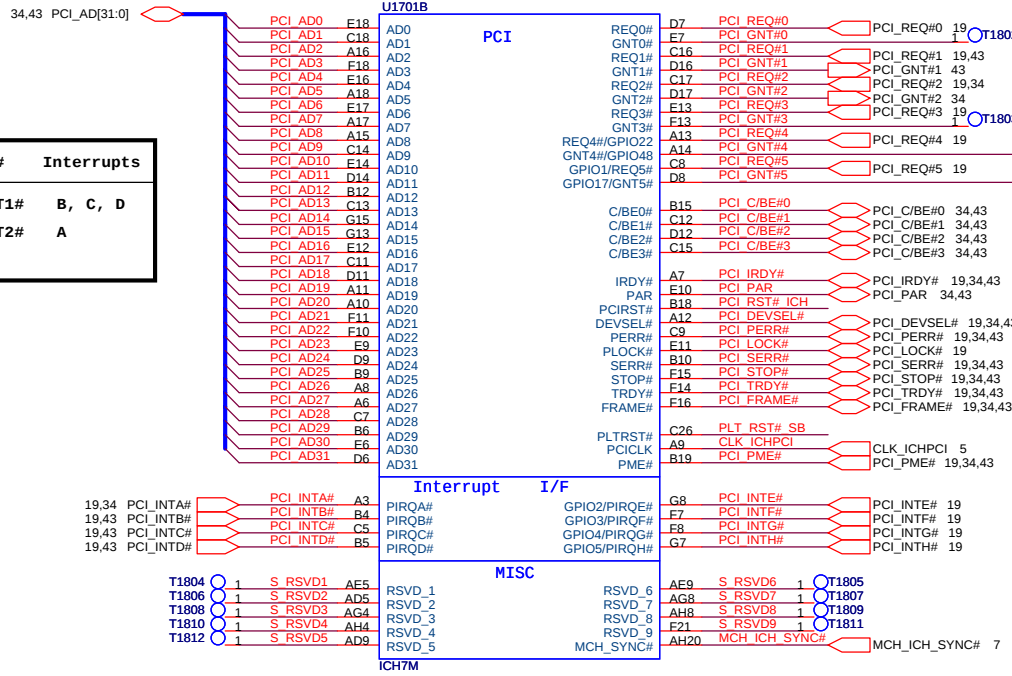
Check with EMI: remove 0 ohm
=>IDE_PDIO#_ICH
IDE_PDD1_ICH
IDE_PDD2_ICH
IDE_PDD9_ICH
IDE_PDD10_ICH

ACZ_SDOUT	PWROK rising	TP3 pull low: allow entrance to XOR Chain testing TP3 not pull low: sets bit 1 of RPC.PC	PD
ACZ_SYNC	PWROK rising	sets bit 0 of RPC.PC	PD
EE_CS		should not be pulled high	PD
EE_DOUT		should not be pulled low	PU
GNT2#		should not be pulled low	PU
GNT3#	PWROK rising	low: "top-block swap" mode	PU
GNT5#/GPIO17# GNT4#/GPIO48	PWROK rising	GNT5# GNT4# 0 1 SPI 1 0 PCI 1 1 LPC	PU

GPIO16 /DPRSLPVR		should not be pulled high	PD
GPIO25	RSRST# rising	should not be pulled low	PU
INTRVREN	ALWAYS	high: Enable integrated VccSus1_05 VRM	
LINKALERT#		REQUIRE an external pull-up R	Need PU
REQ[4:]#	PWROK rising		
SATALED#		should not be pulled low	Conditional PU
SPKR	PWROK rising	high: "No reboot" mode	PD
TP3	PWROK rising	should not be pulled low unless using XOR Chain testing	PU

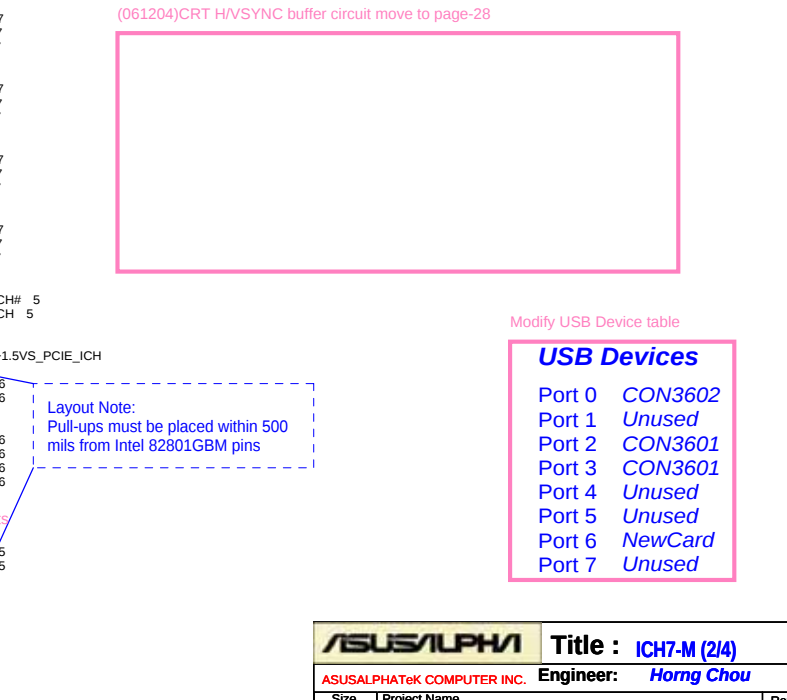
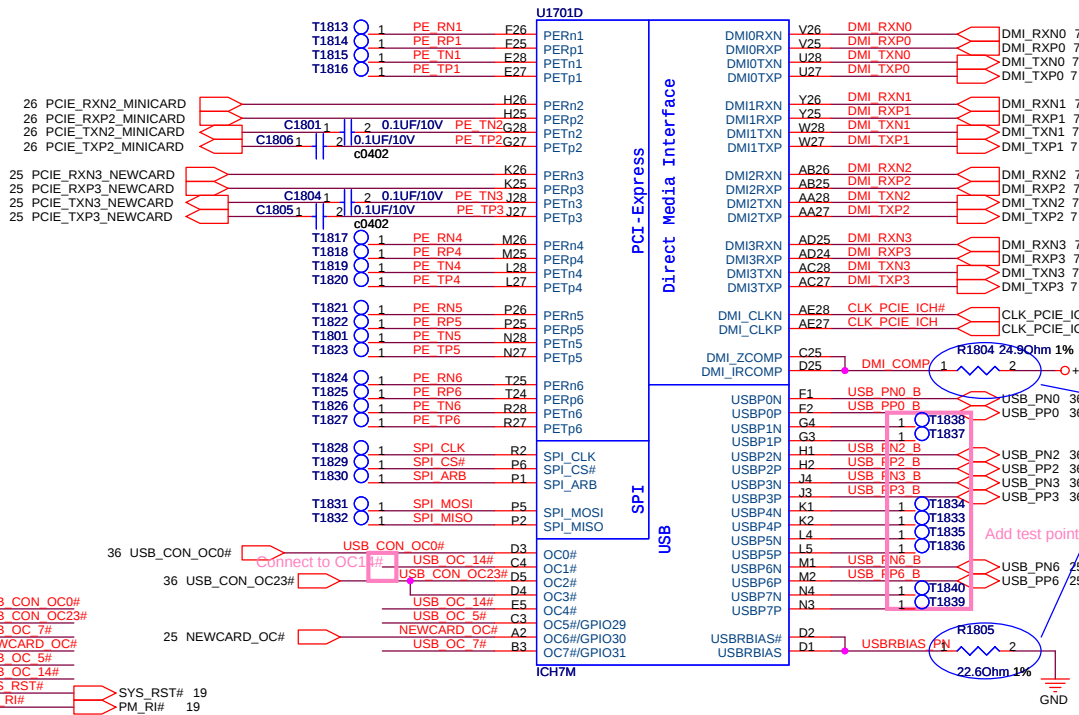
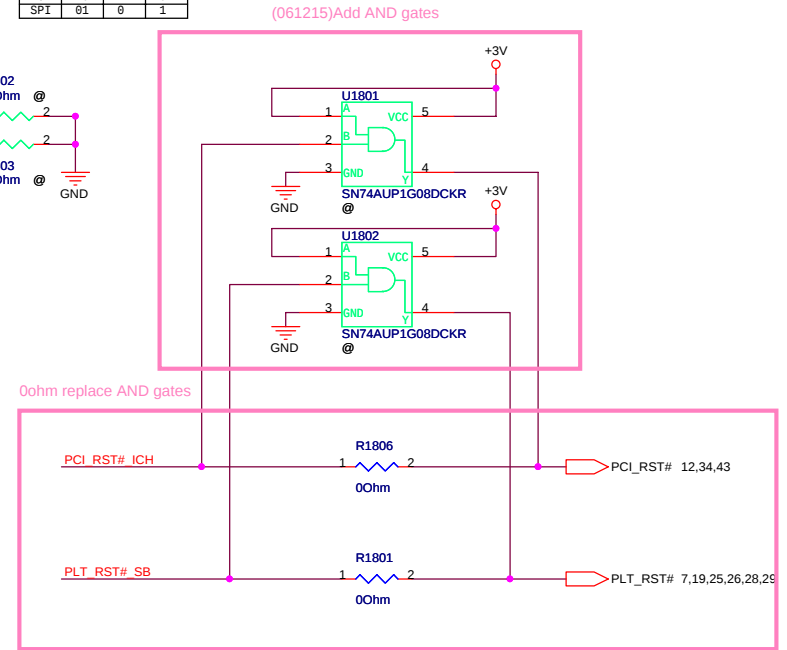
PCI Device

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD17	REQ1#/GNT1#	B, C, D
LAN	AD23	REQ2#/GNT2#	A



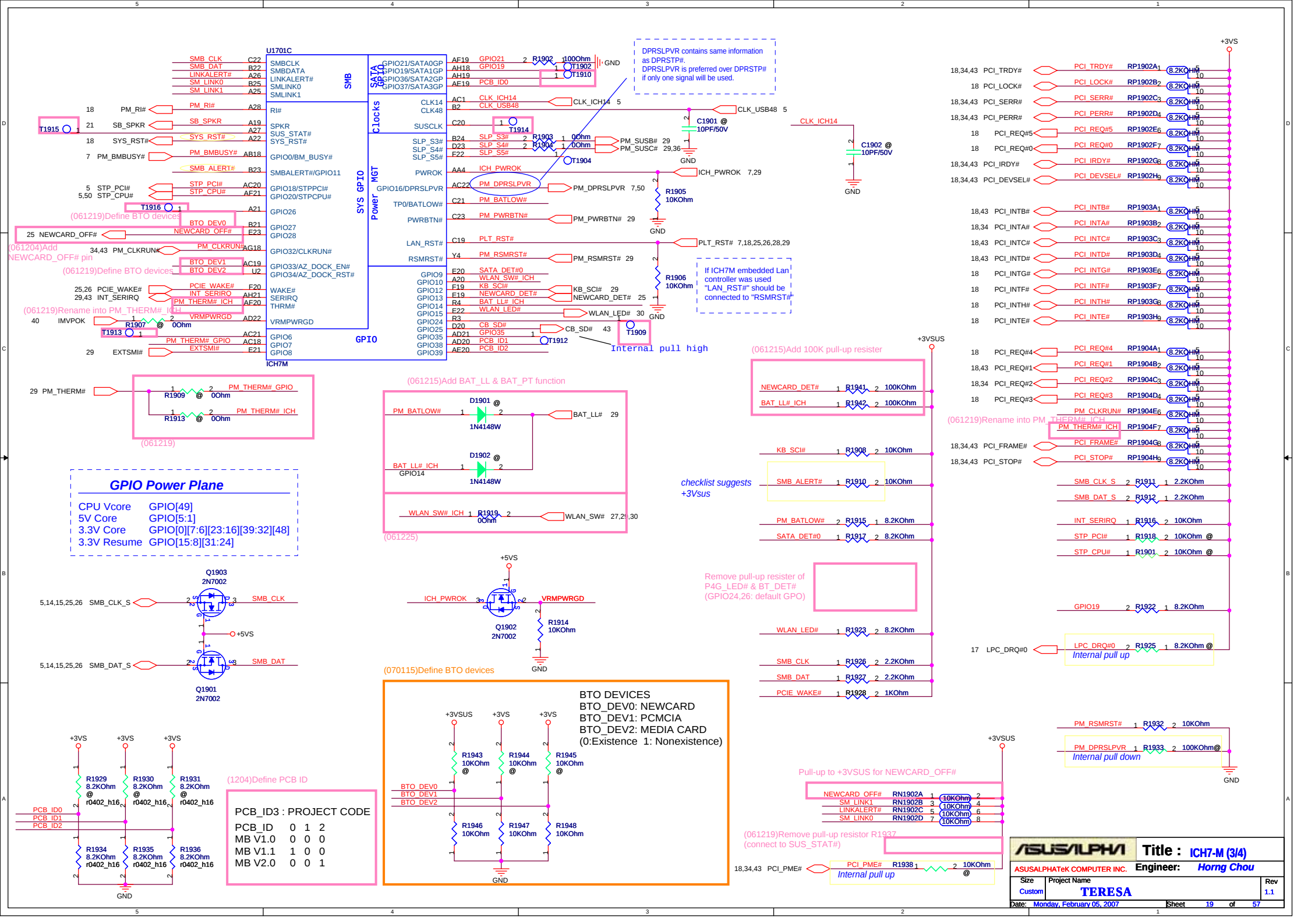
	GNT#5	GNT#4
LPC	11	1
PCI	10	1
SPI	01	0

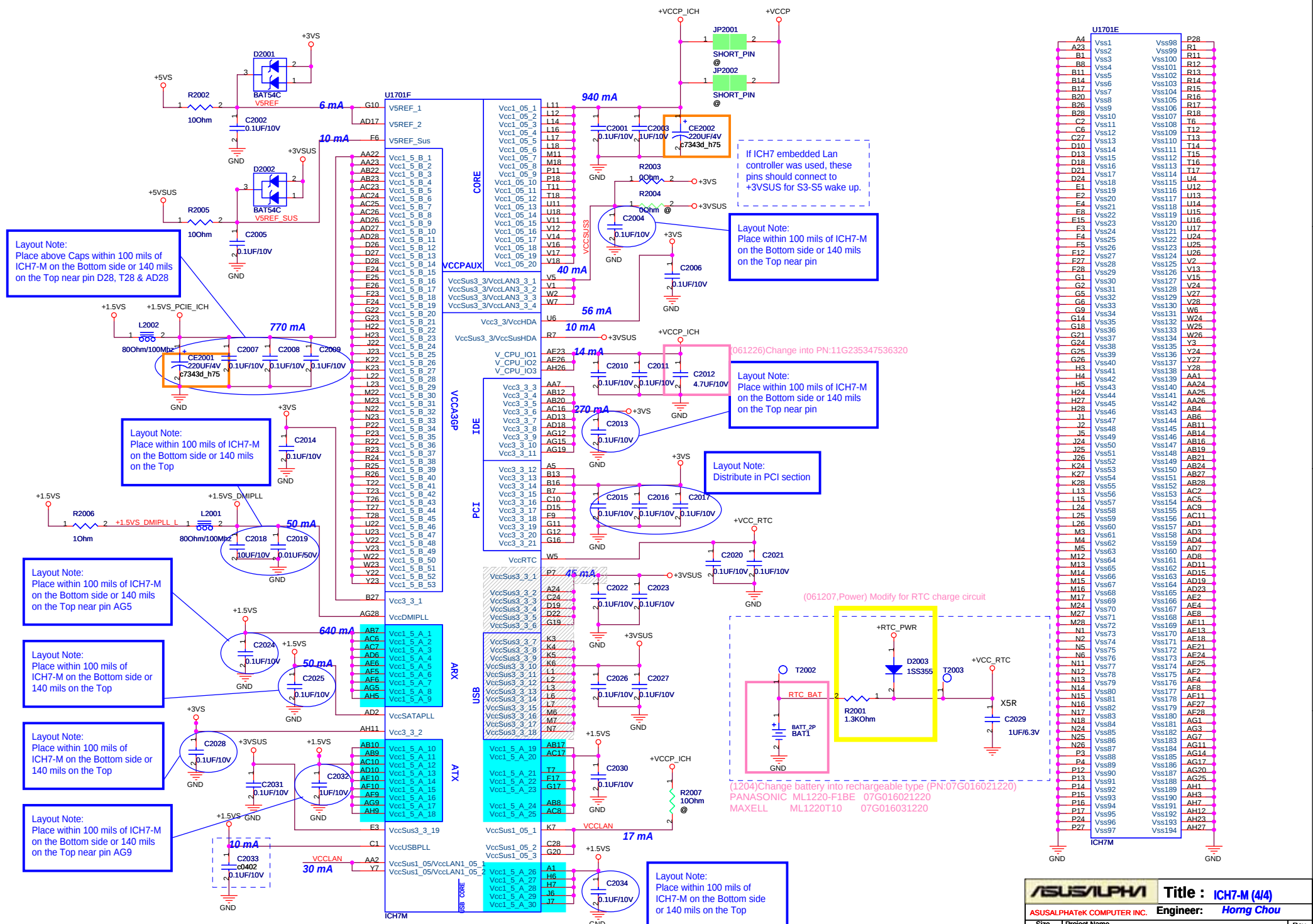
(default)

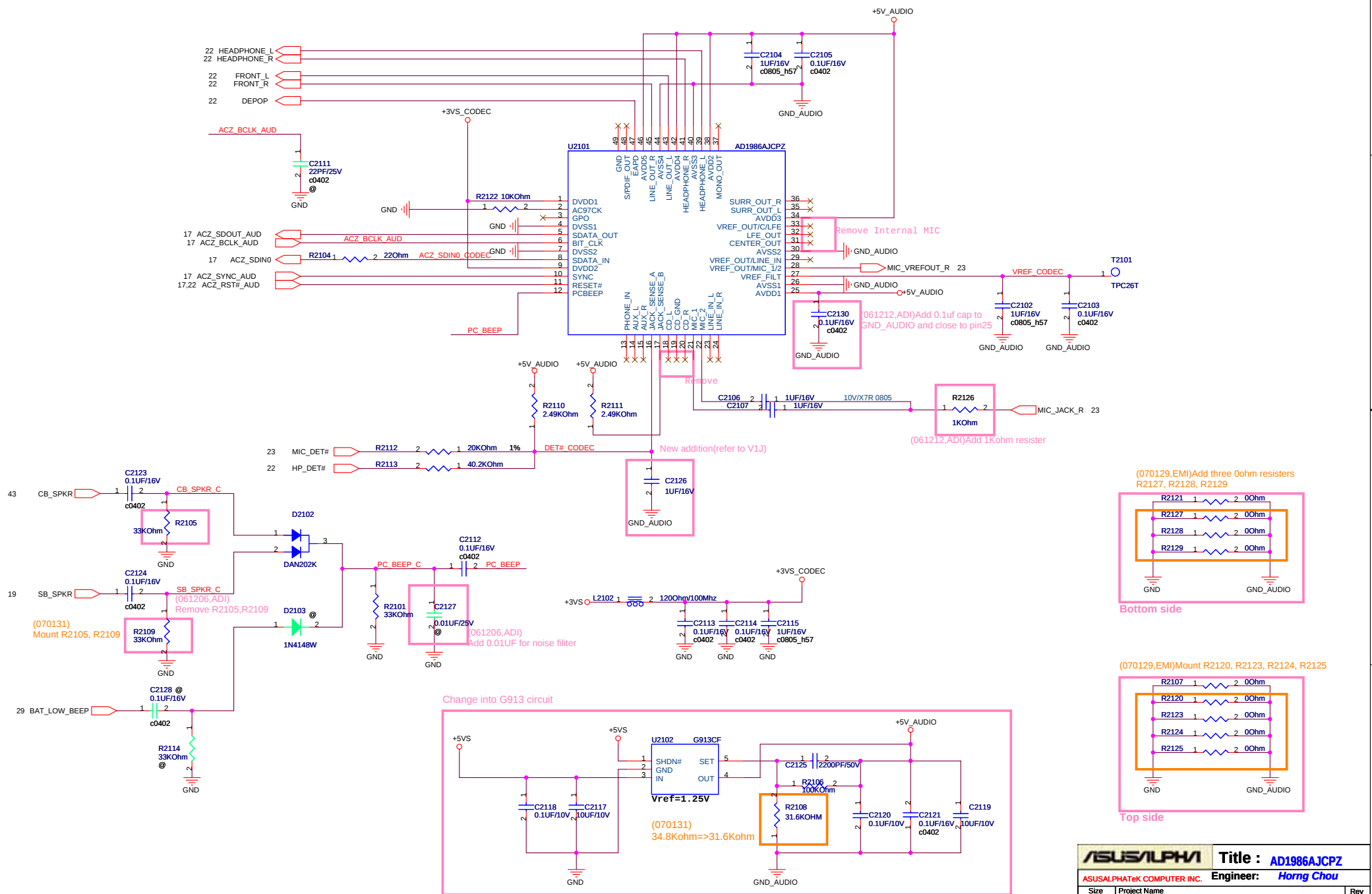


USB Devices

Port 0	CON3602
Port 1	Unused
Port 2	CON3601
Port 3	CON3601
Port 4	Unused
Port 5	Unused
Port 6	NewCard
Port 7	Unused

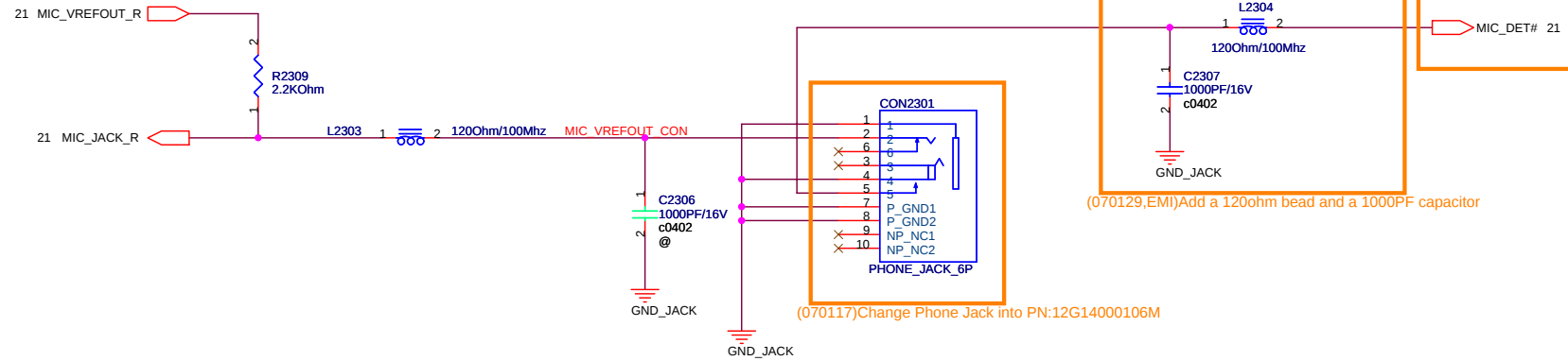






Remove Internal MIC pre-Amplifier

MICROPHONE IN

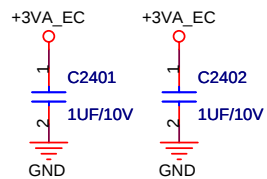


(070110)modify MIC_DET# circuit

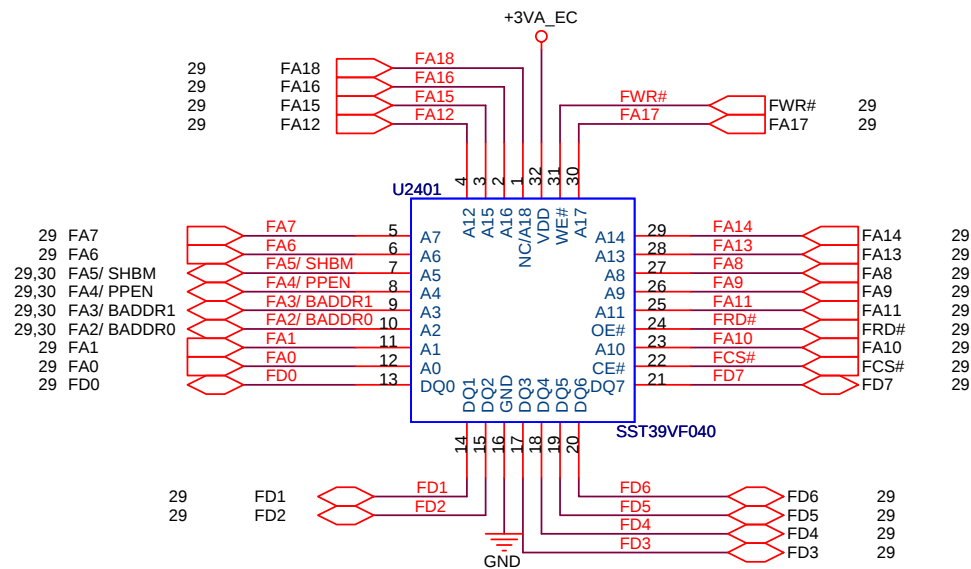
(070129,EMI)Add a 120ohm bead and a 1000PF capacitor

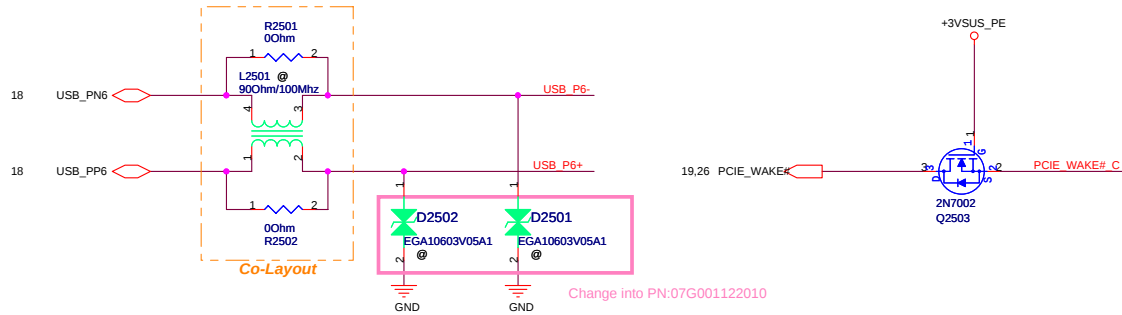
(070117)Change Phone Jack into PN:12G14000106M

ASUS/ALPHA		Title : MIC JACK	
ASUSALPHATeK COMPUTER INC.		Engineer: Horng Chou	
Size Custom	Project Name TERESA		Rev 1.1
Date: Monday, February 05, 2007		Sheet 23 of 57	

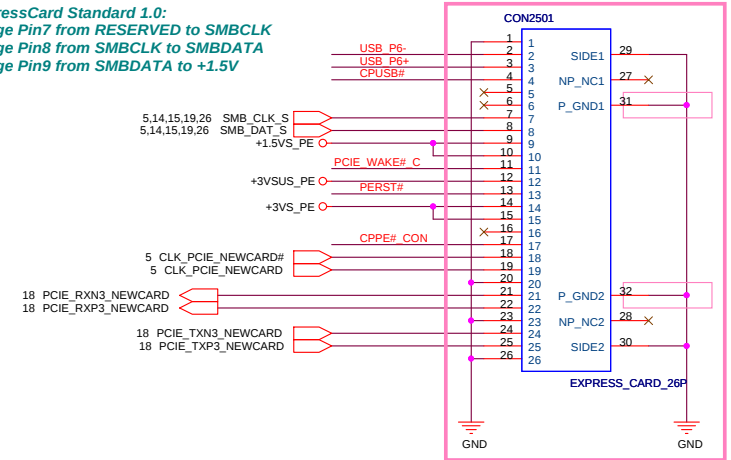


ISA ROM





!! ExpressCard Standard 1.0:
 Change Pin7 from RESERVED to SMBCLK
 Change Pin8 from SMBCLK to SMBDATA
 Change Pin9 from SMBDATA to +1.5V

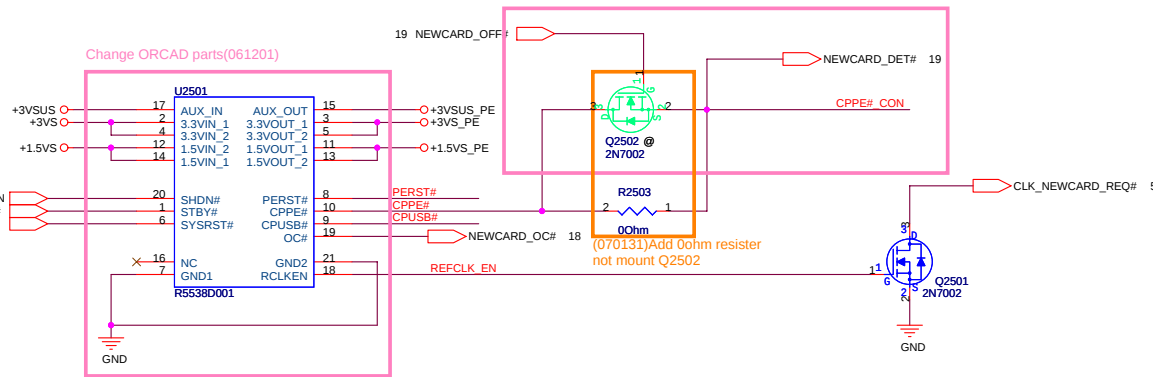


(061214)NewCard Ejector was combined into Header

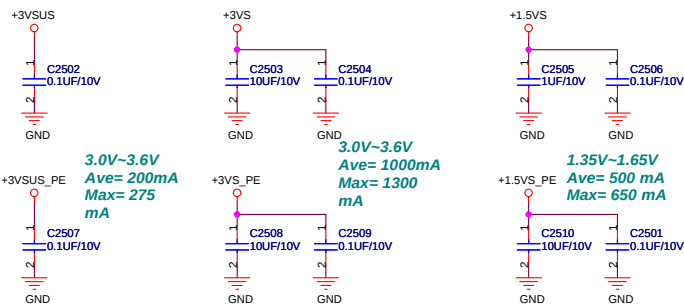
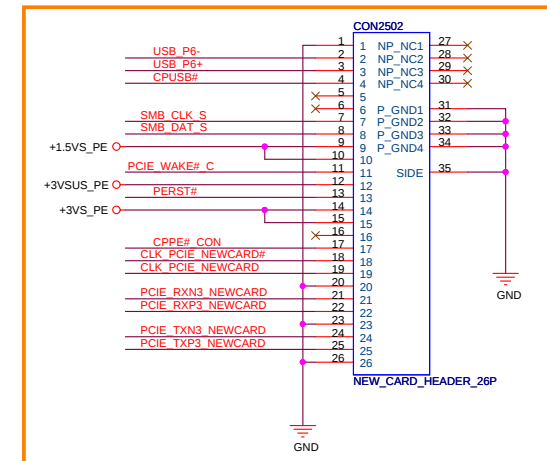


Change ORCAD parts(061201)

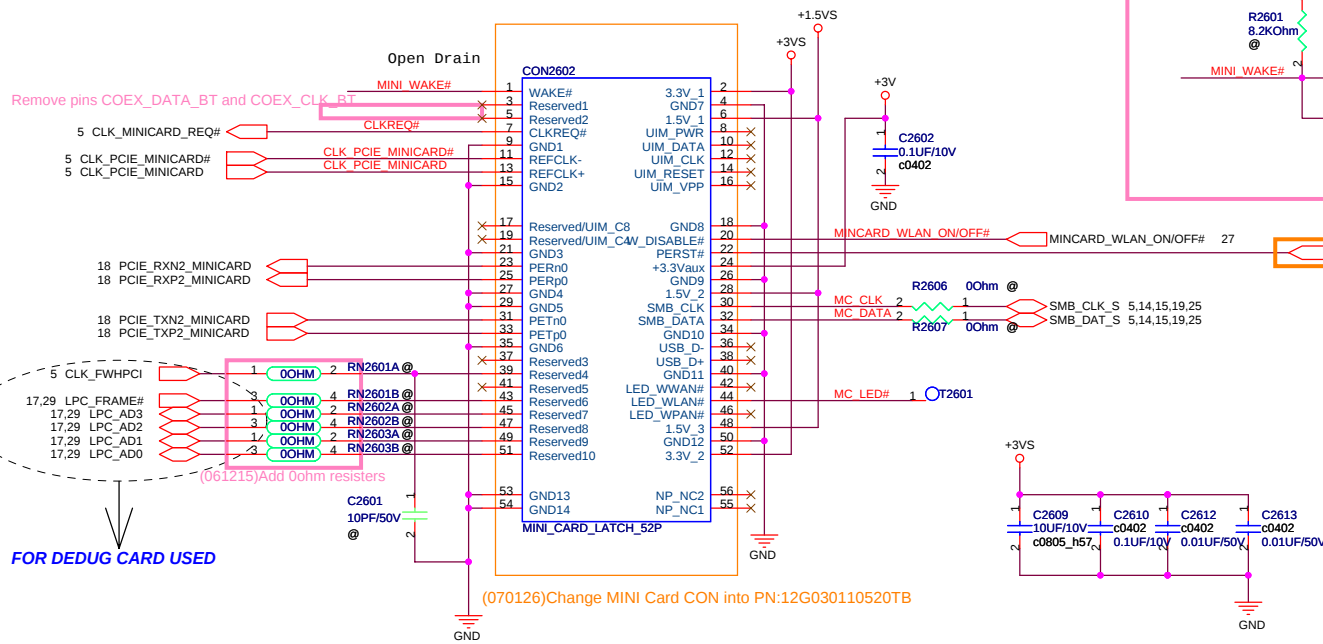
Refer to V1J(061201)



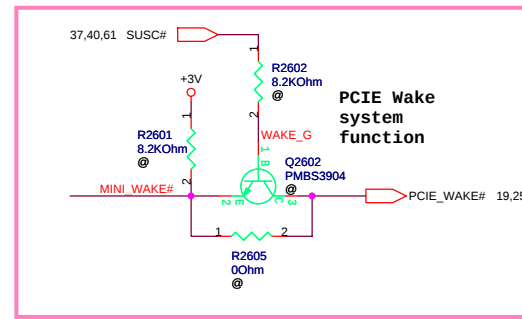
(070201)Add CON2502 in other to colayout with CON2501



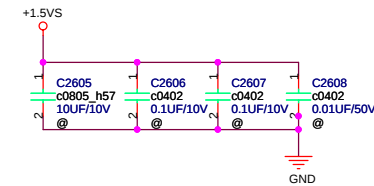
MINI CARD CONNECTOR



(061212) Not mount (Not support wake on WLAN)

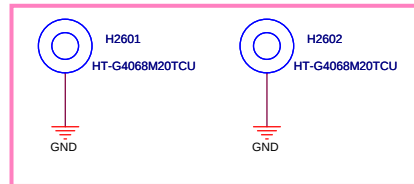


(070129) Change pin connection from PCI_RST# to PLT_RST#



Check O/D output or push pull

Instead of Mini-PCIE latch connector. For cost down.



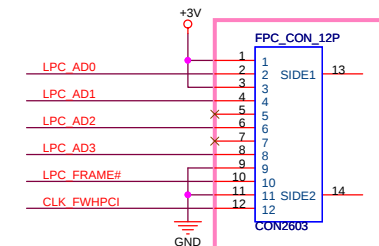
(070201) Change MINI Card NUT into PN:13G021056061TB

WLAN SPEC:

		WLL3140	WLL4080
Transmit Mode Current	11.a		550mA
	11.b	525mA	560mA
	11.g	560mA	550mA
	11.n		
Receive Mode Current	11.a		280mA
	11.b	430mA	270mA
	11.g	460mA	280mA
	11.n		
Sleep Mode Current		220mA	20mA
Supplied Voltage(VCC)	MIN	3.0V	3.0V
	TYP	3.3V	3.3V
	MAX	3.6V	3.6V

Debug Card CON

(061206) Change Debug CON into PN:12G18340120E

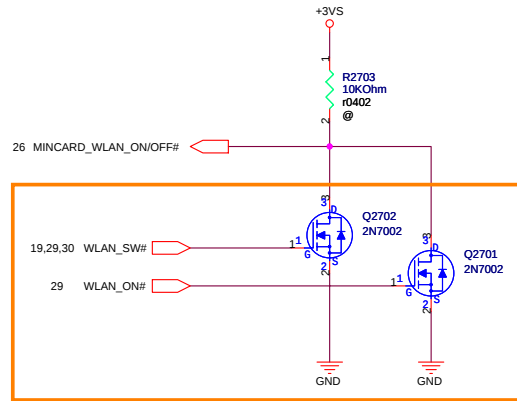


For Bluetooth

For Side SW

Deltete Bluetooth CON

WLAN ON/OFF Control

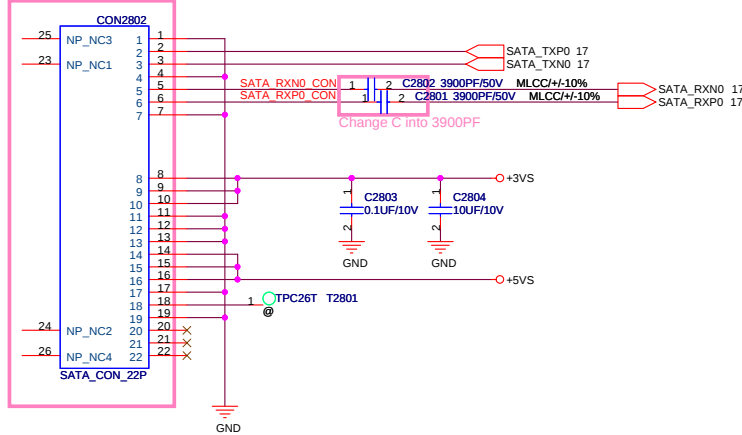


(070202)Modify WLAN on/off circuit

Deltete BT ON/OFF Control

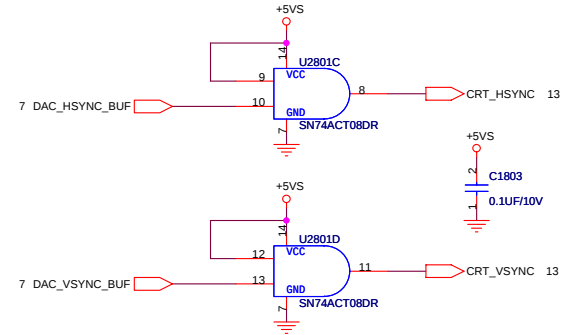
Deltete FR Switch

(061208)Change SATA CON into PN:12G15101022A

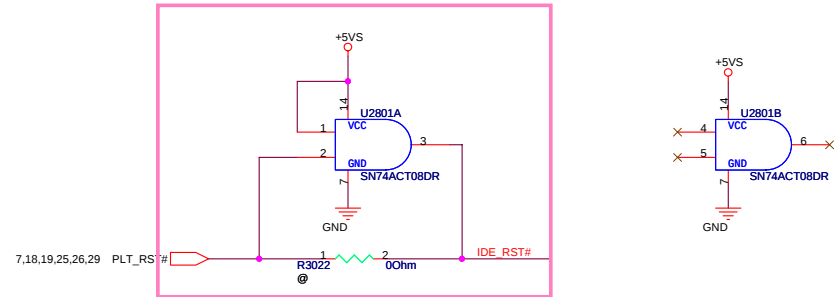


SATA HDD

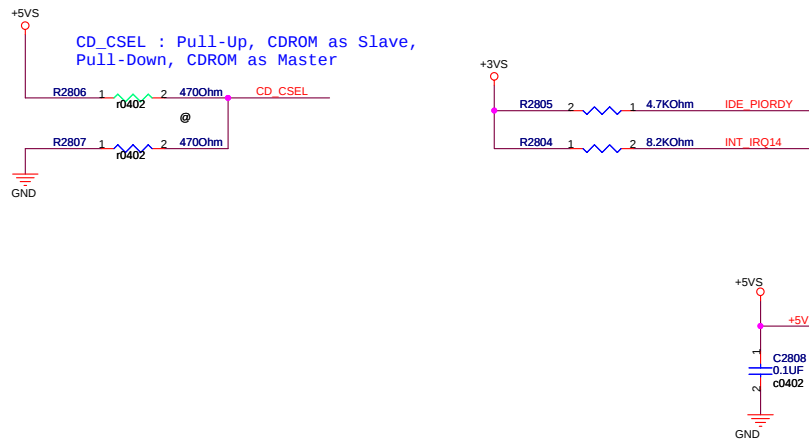
Change AND gate into 5V Vcc



Modify

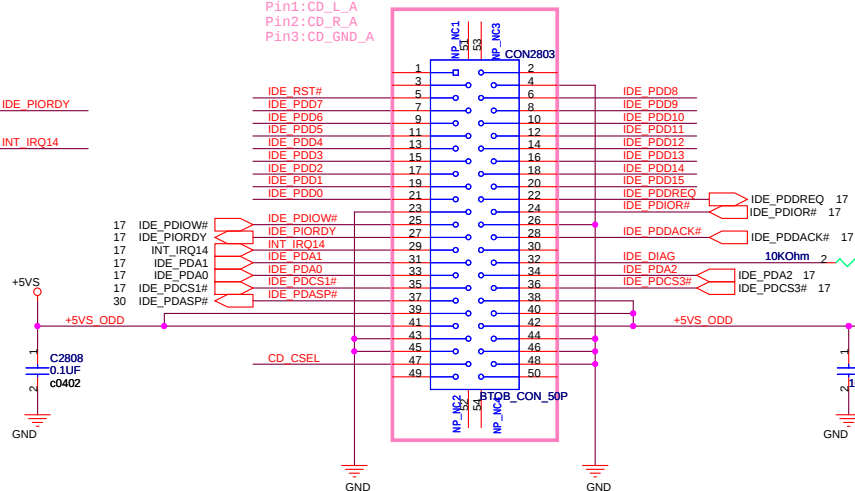


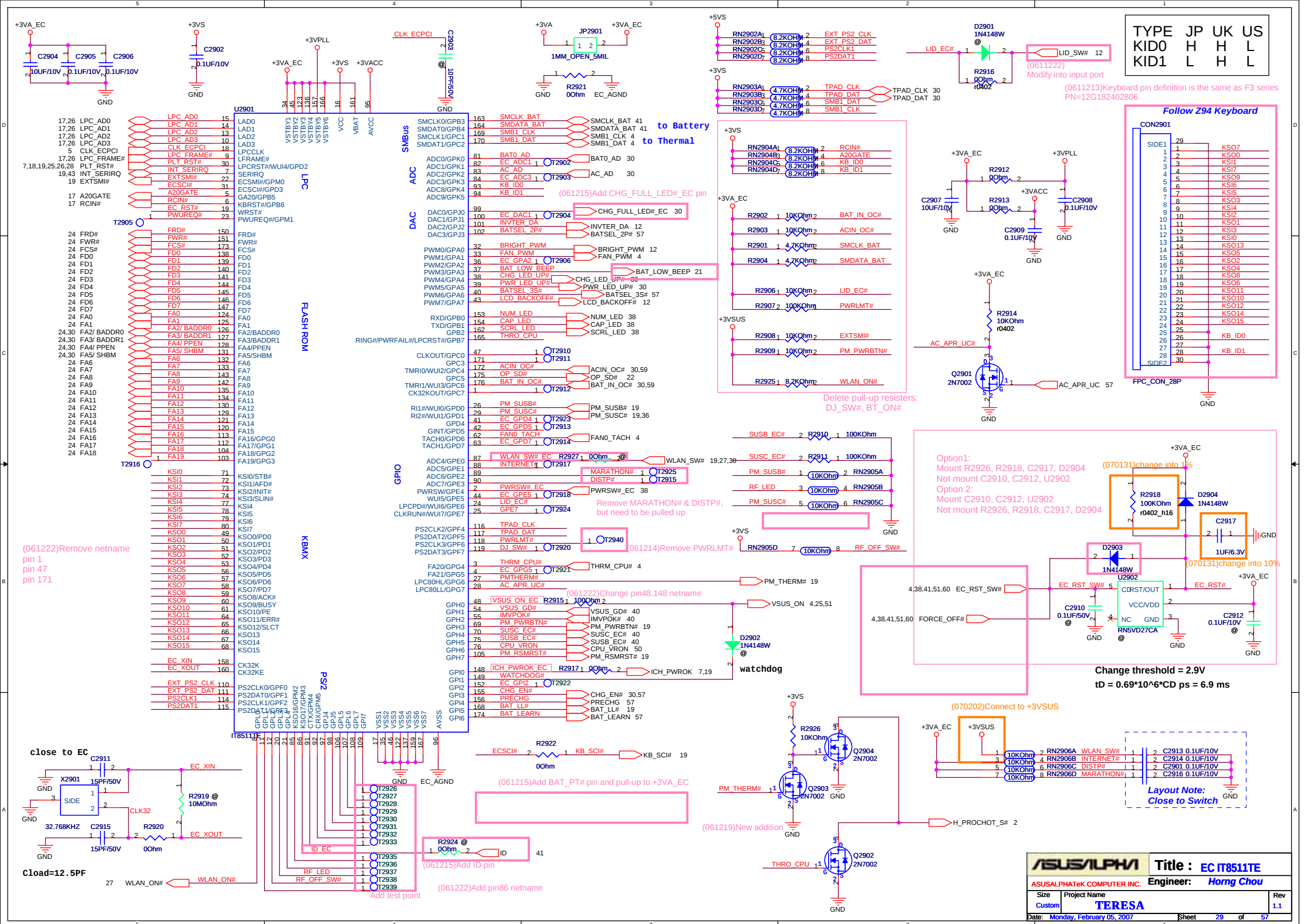
CD-ROM



Delete
Pin1:CD_L_A
Pin2:CD_R_A
Pin3:CD_GND_A

(061208)Change ODD CON into PN:12G161220509

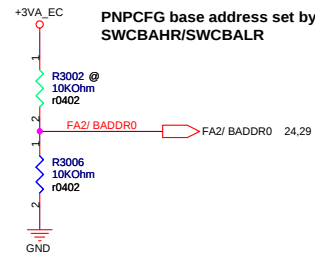




EC Hardware Strap

Strap value sampled after
VSTBY power up reset

PNPCFG base address set by SWCBAHR/SWCBALR



BADDR[1:0]

No pull up:

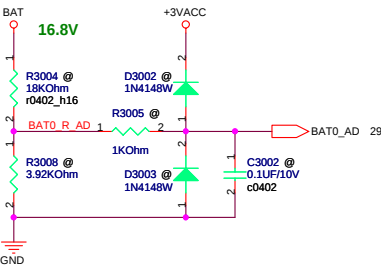
Ext 10K up on BADDR0:

Ext 10K up on BADDR1:

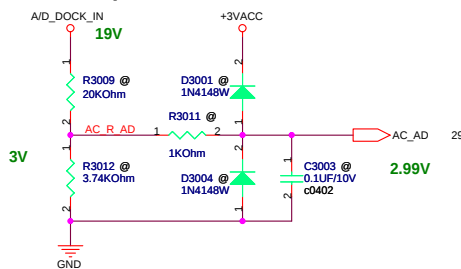
The register pair to access PNPCFG is 002Eh and 002Fh.
The register pair to access PNPCFG is 004Eh and 004Fh.
The register pair to access PNPCFG is determined by EC domain registers SWCBAHR and SWCBALR.

EC ADC

Battery



Adaptor



Share Memory



SHBM

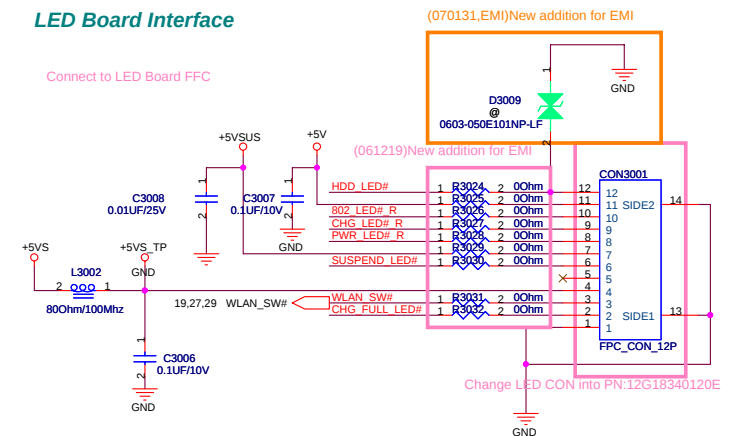
No pull up: Disable shared memory with host BIOS
Ext 10K up: Enable shared memory with host BIOS

PPEN

No pull up: Normal
Ext 10K up: KBS interface pins are switched to parallel port interface for in-system programming.

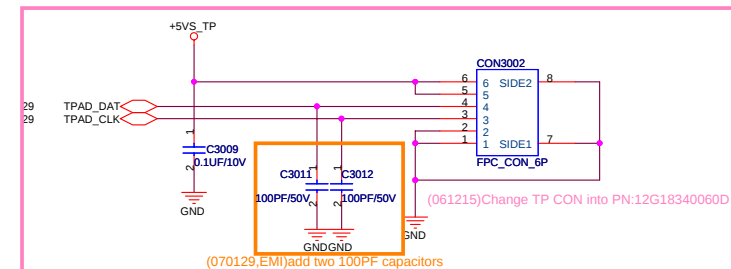
LED Board Interface

Connect to LED Board FFC

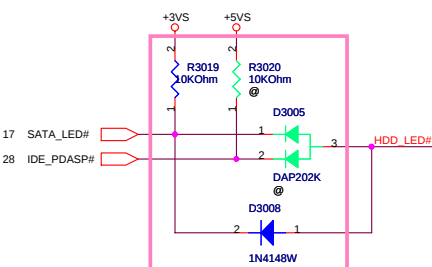


Touchpad Board Interface

Connect to Touchpad Board FFC



HDD LED

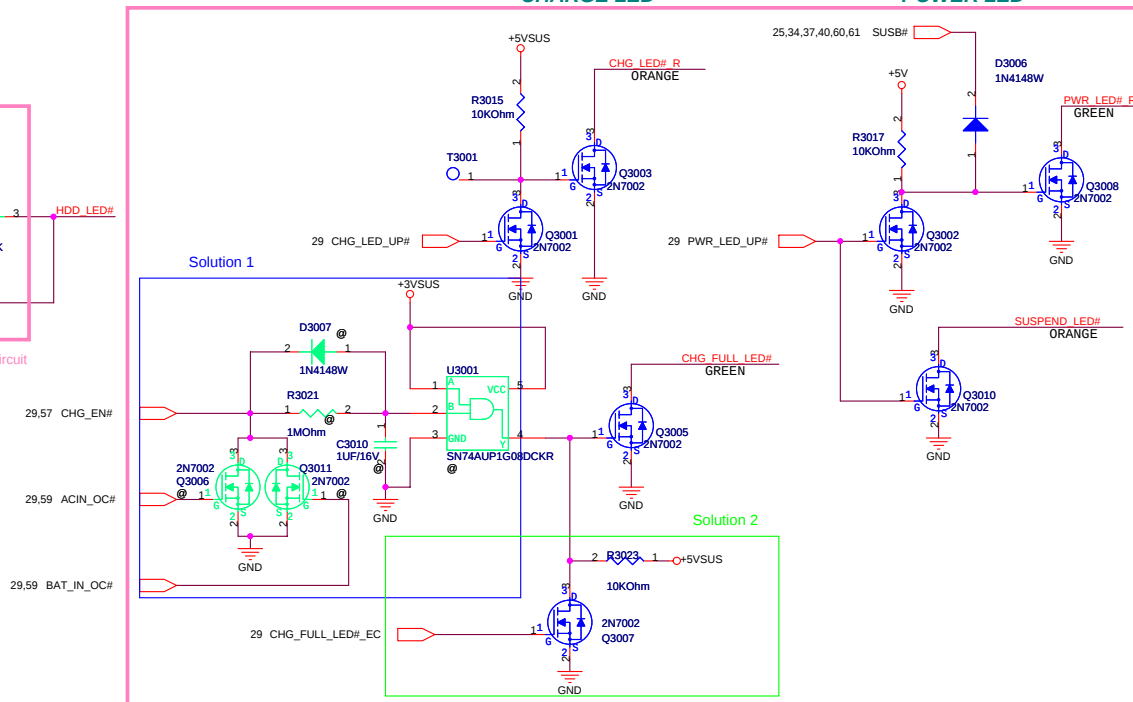


(061212)Modify HDD LED circuit

(061201)Modify Charge & Power circuit

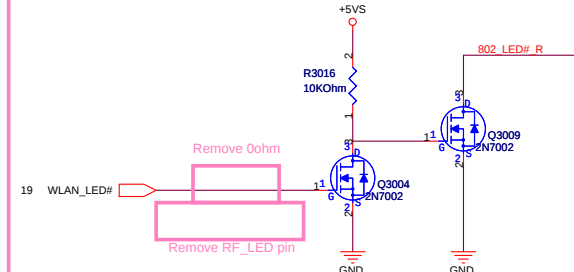
CHARGE LED

POWER LED



(061212)Modify charge full circuit : solution1 & solution2

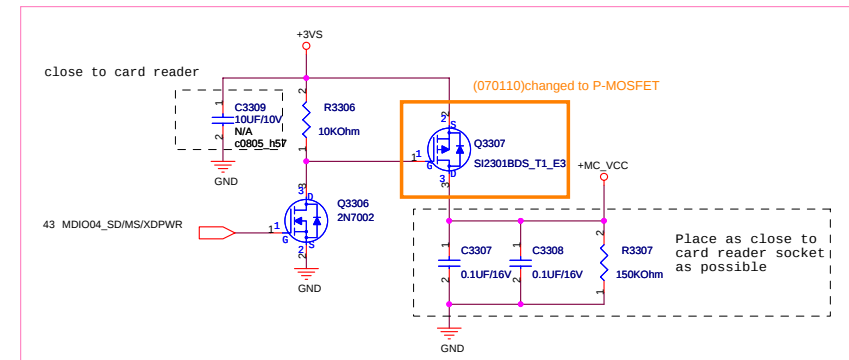
WLAN LED



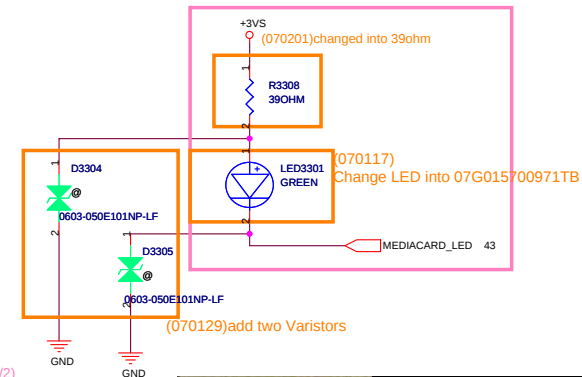
(070124)Add Media Card CON for colayout **MEDIA CARD SLOT** (070130)Add RN3301, RN3302, RN3303

[illegible][illegible]

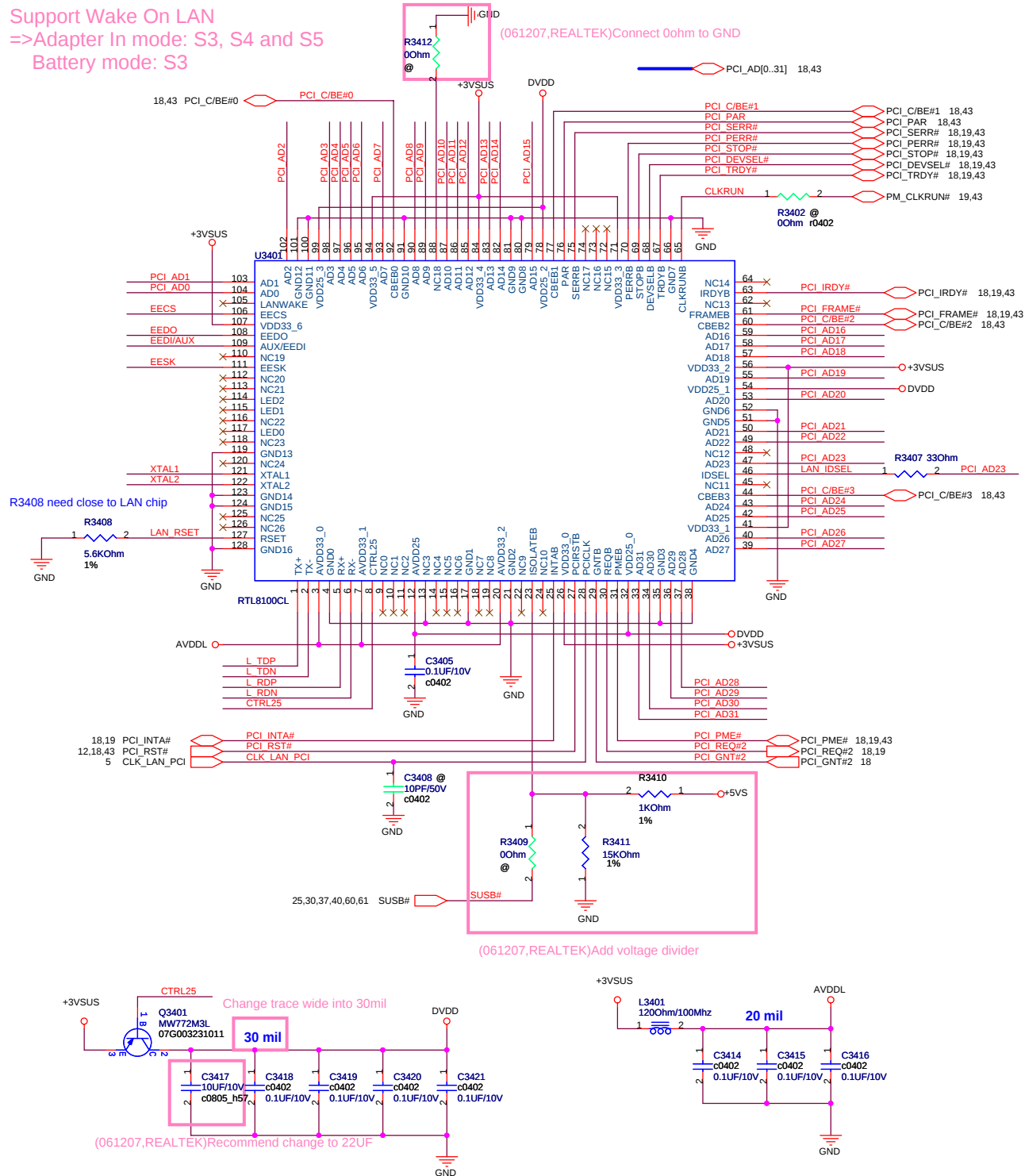
Change circuit from AAT4610A to SI2301



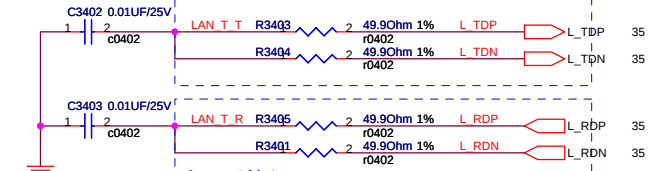
A circuit diagram showing a D3303 OR gate. The gate has two inputs: SDCD# (pin 2) and MSCD# (pin 1). The output is XD_CD# (pin 3). The gate is labeled D3303 and DAN202K.



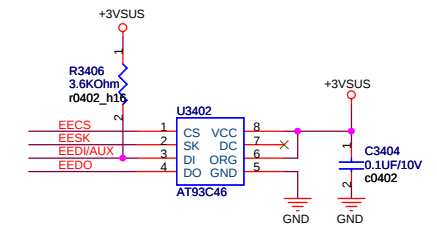
Support Wake On LAN
=>Adapter In mode: S3, S4 and S5
Battery mode: S3



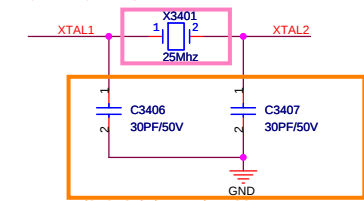
- | Layout Note:
- | L_TDP, L_TDN termination resistors
- | should be near chip



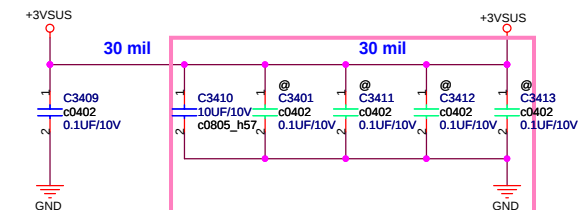
Layout Note:
L_RDP, L_RDN termination resistors
should be near transformer



(061207)Change to PN:07G010Q12500



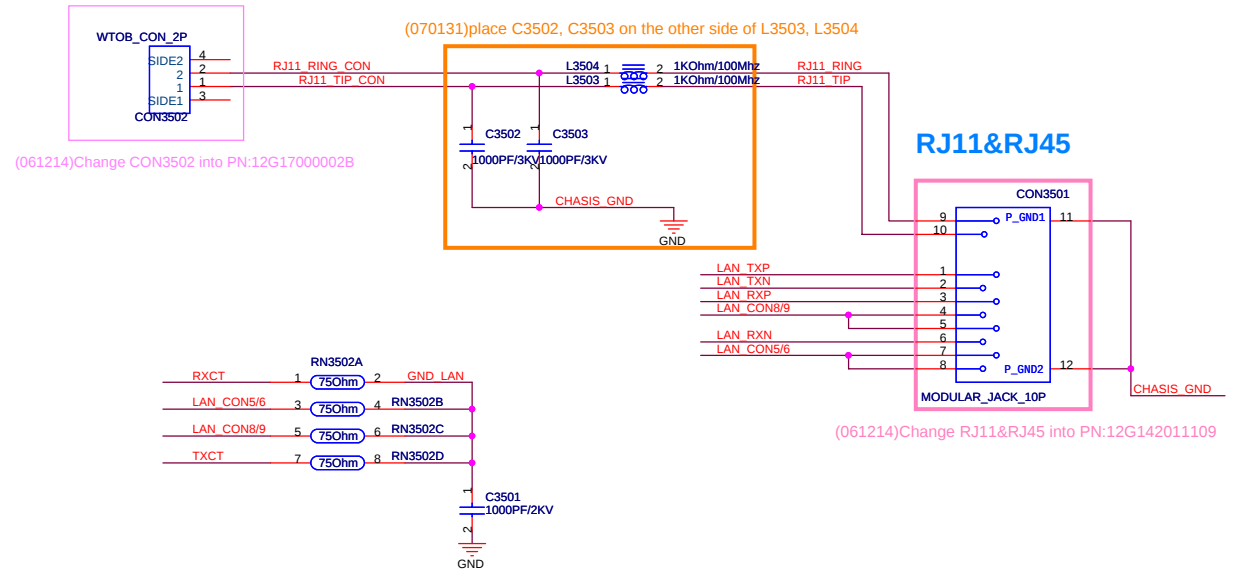
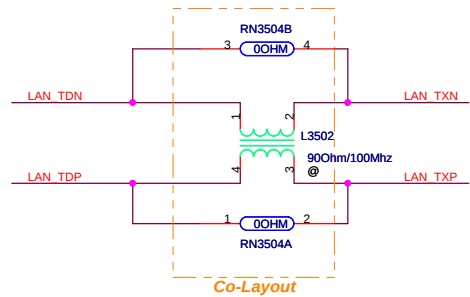
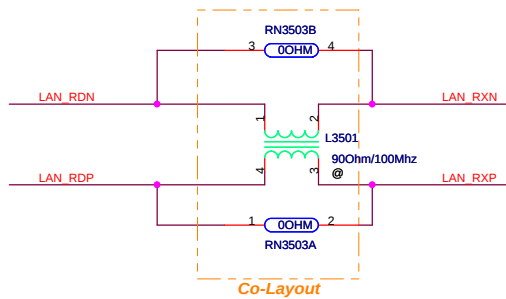
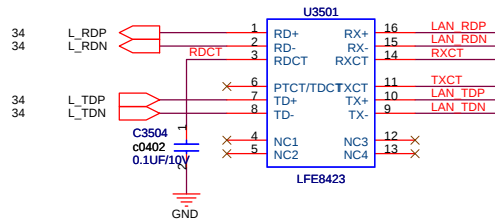
(070131)change into 30PF



(061207,REALTEK)Remove capacitors

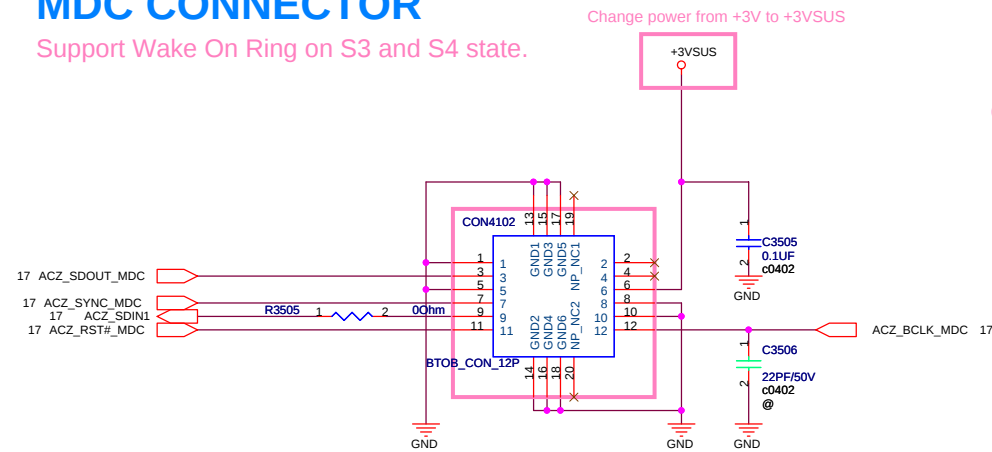
LAN PORT

TRANSFORMER 10/100MB



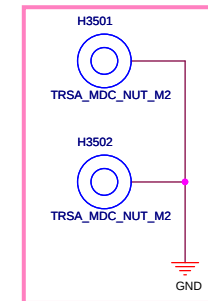
MDC CONNECTOR

Support Wake On Ring on S3 and S4 state.

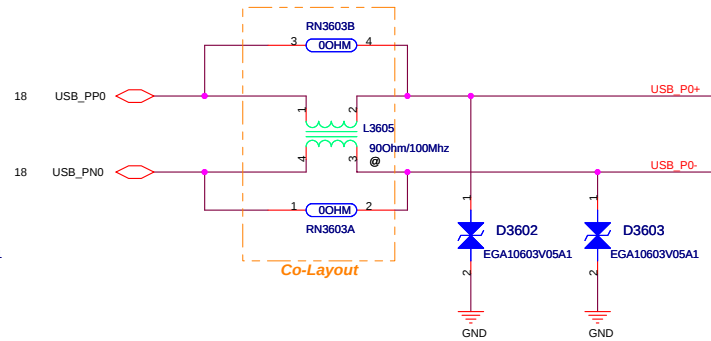
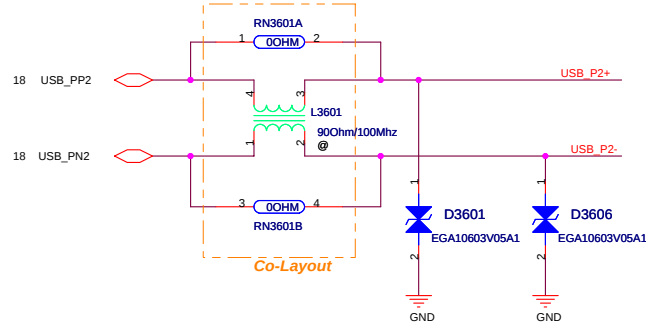
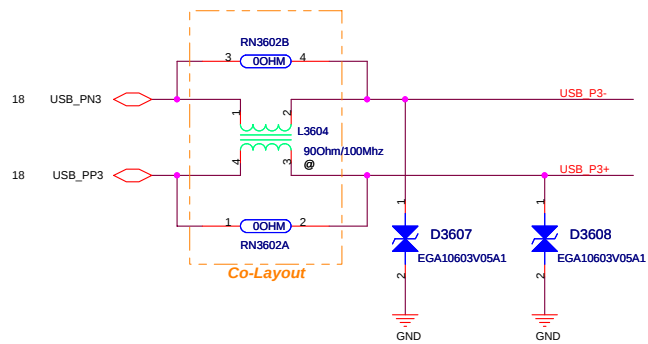


B:MDC NUT

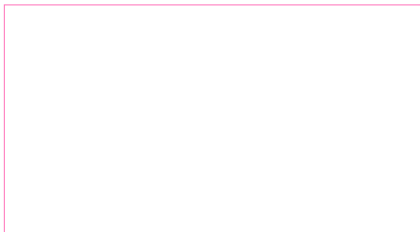
(061219)Change MDC NUT into PN:13G021054000



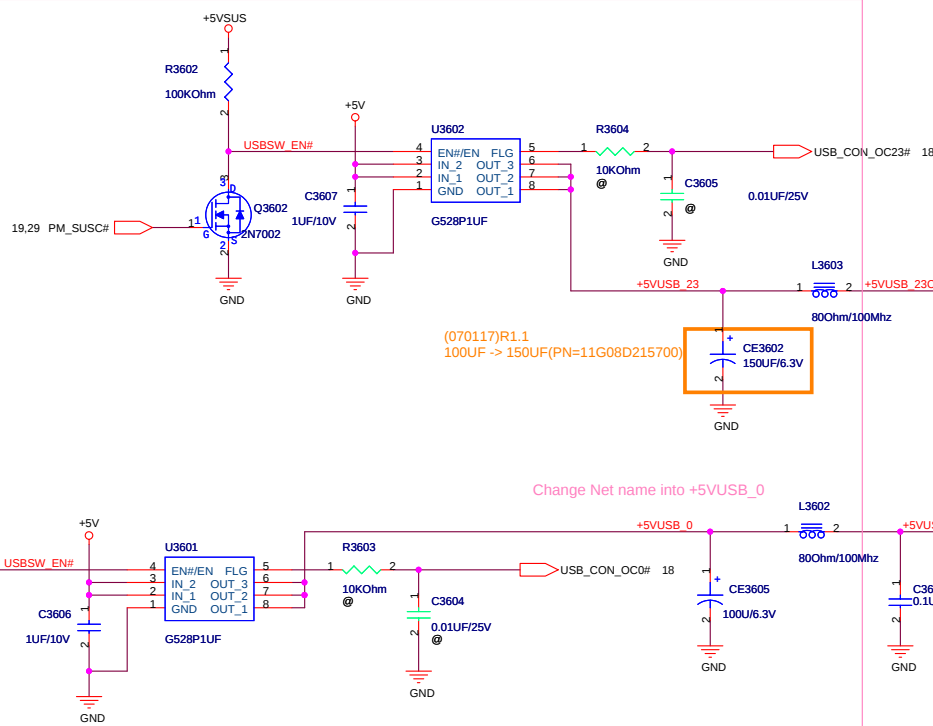
ASUS/ALPHA		Title : RJ45/RJ11/MDC	
ASUSALPHATEK COMPUTER INC.		Engineer: Homg Chou	
Size	Project Name	Rev	
Custom	TERESA	1.1	
Date: Monday, February 05, 2007	Sheet 35 of 57		



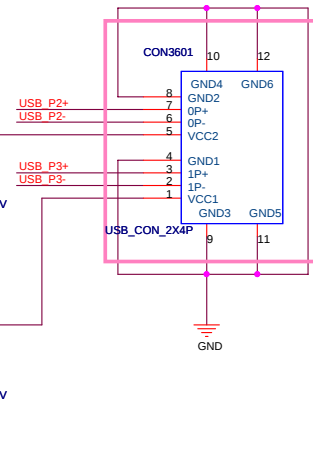
Delete N-MOSFET PMN45EN



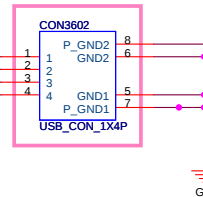
Add USB Switch



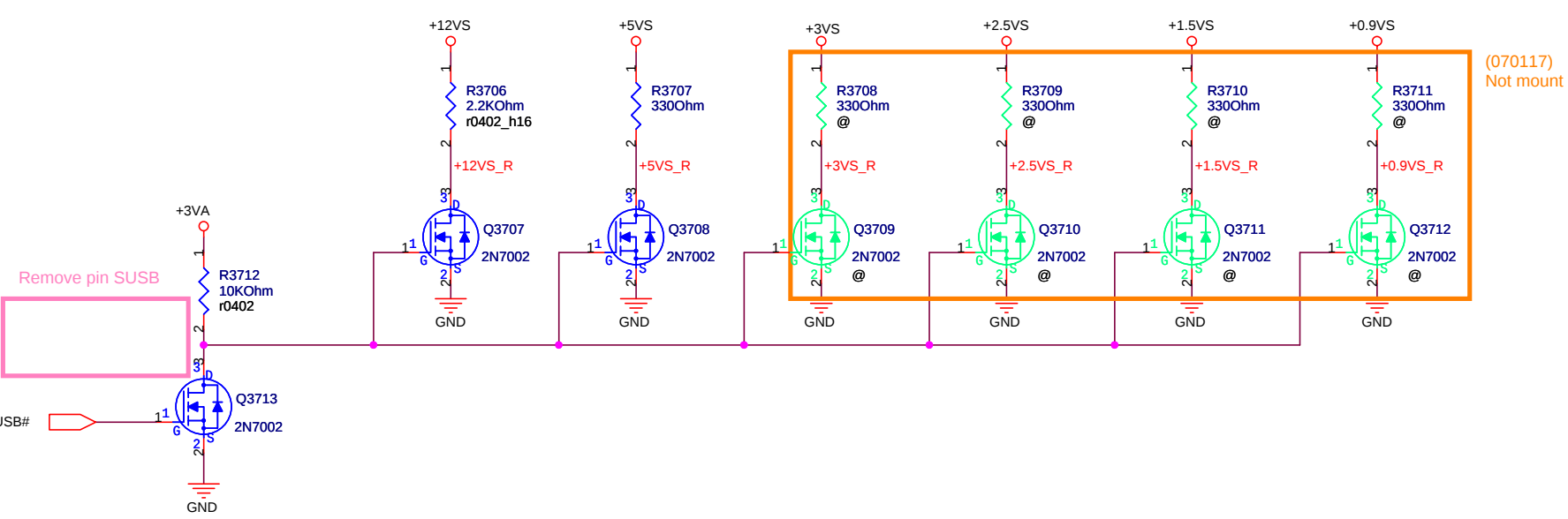
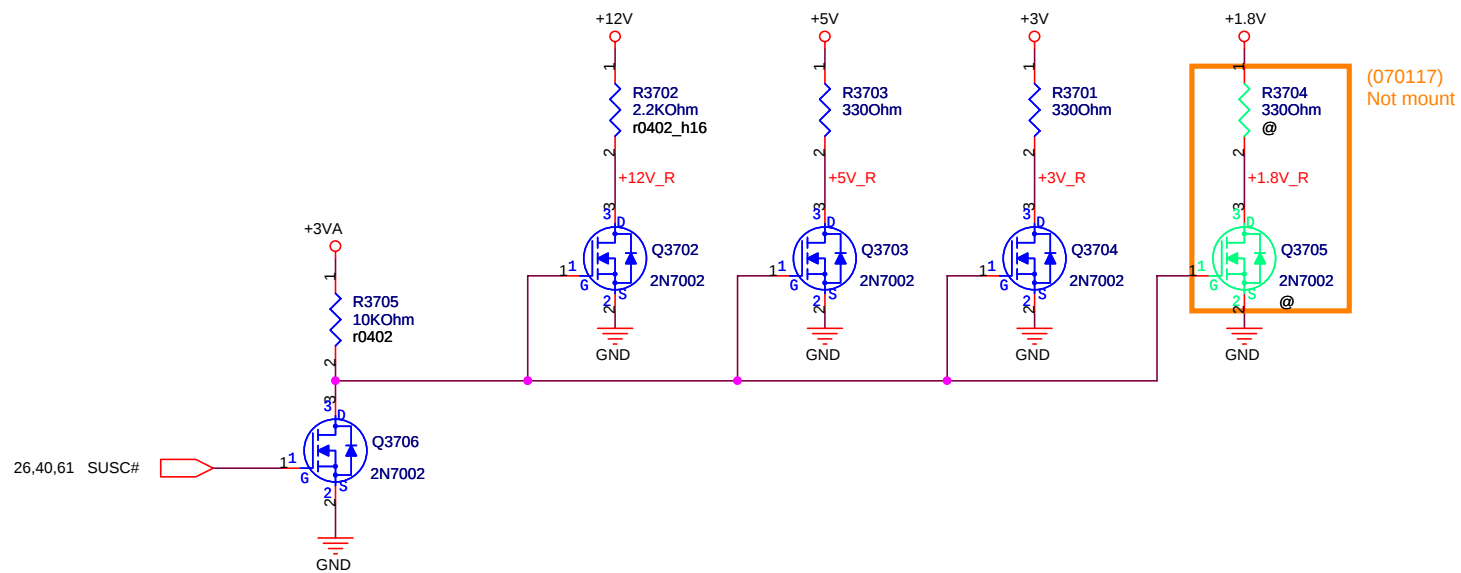
(061211)Change USB CON into PN:12G13111108F



(061206)Change USB CON into PN:12G131030043

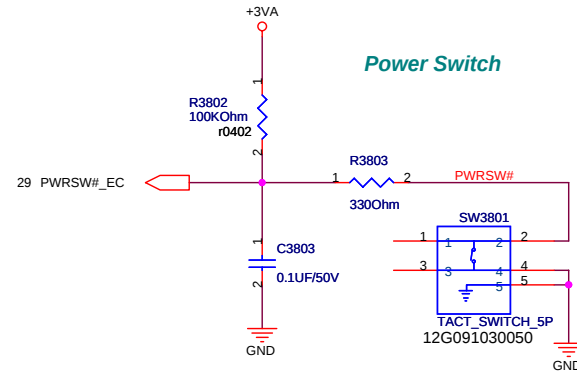


ASUS/ALPHA		Title : USB CONN x3	
ASUSALPHATEK COMPUTER INC.		Engineer: Horng Chou	
Size	Project Name	TERESA	Rev 1.1
Custom			
Date: Monday, February 05, 2007		Sheet 36	of 57



Main Board SW & LED

Power LED move to daughter board



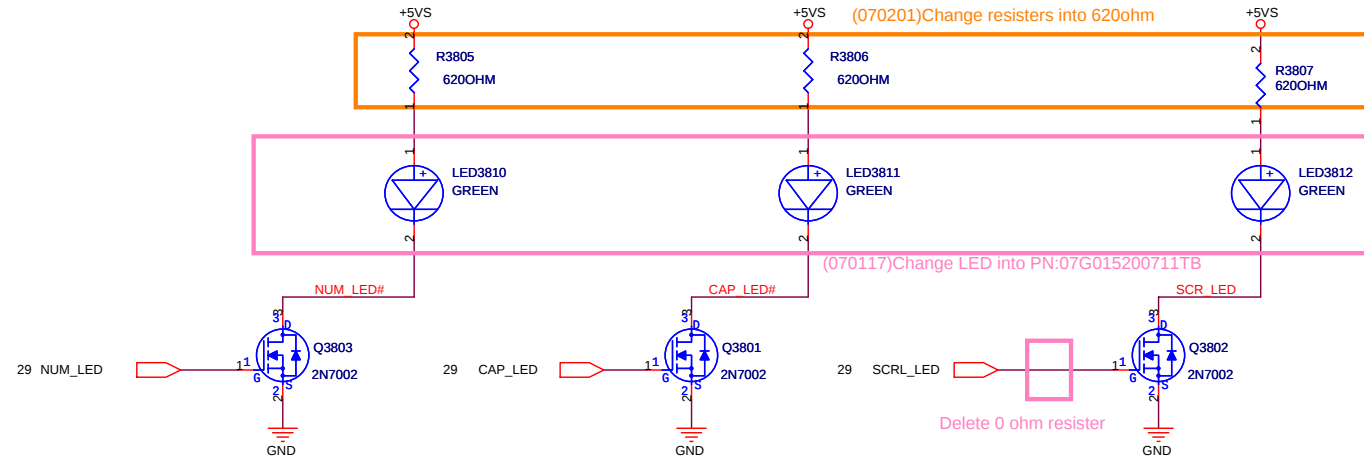
Delete RF LED and Power4 Gear LED

Delete RF/Touchpad and Power4 Gear SWITCH

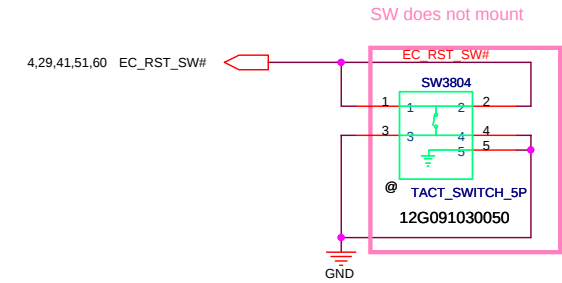
NUMBER LOCK LED

CAPS LOCK LED

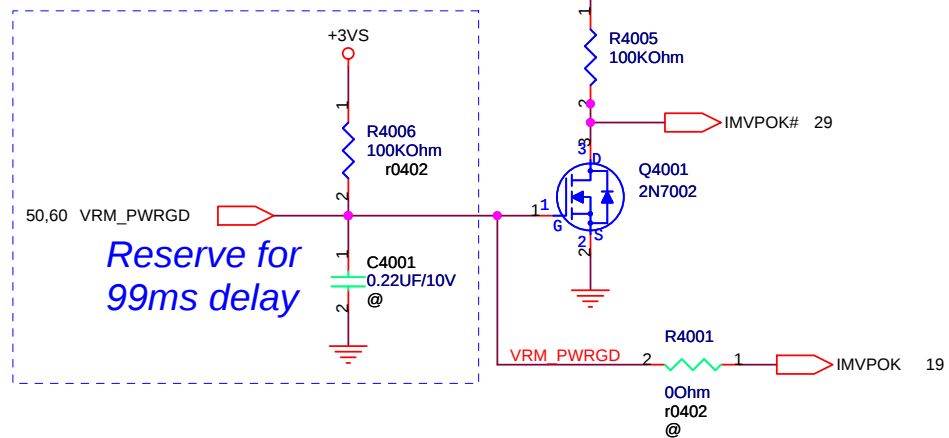
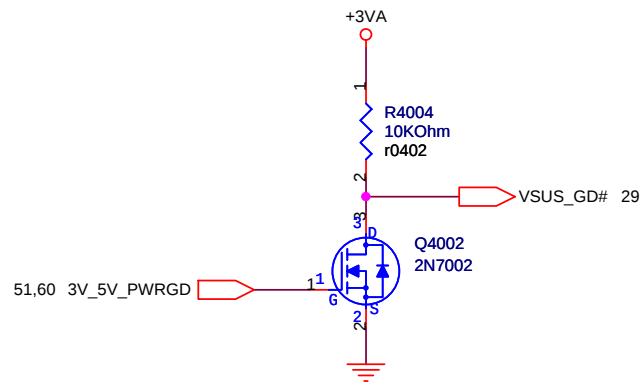
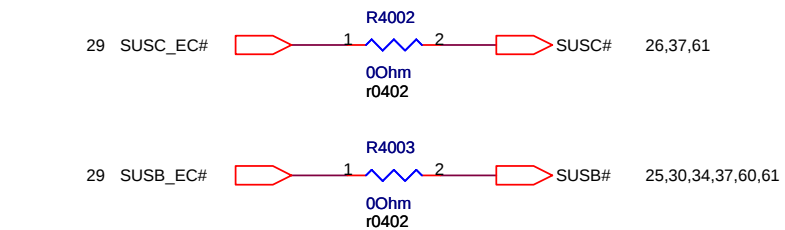
SCROLL LOCK LED



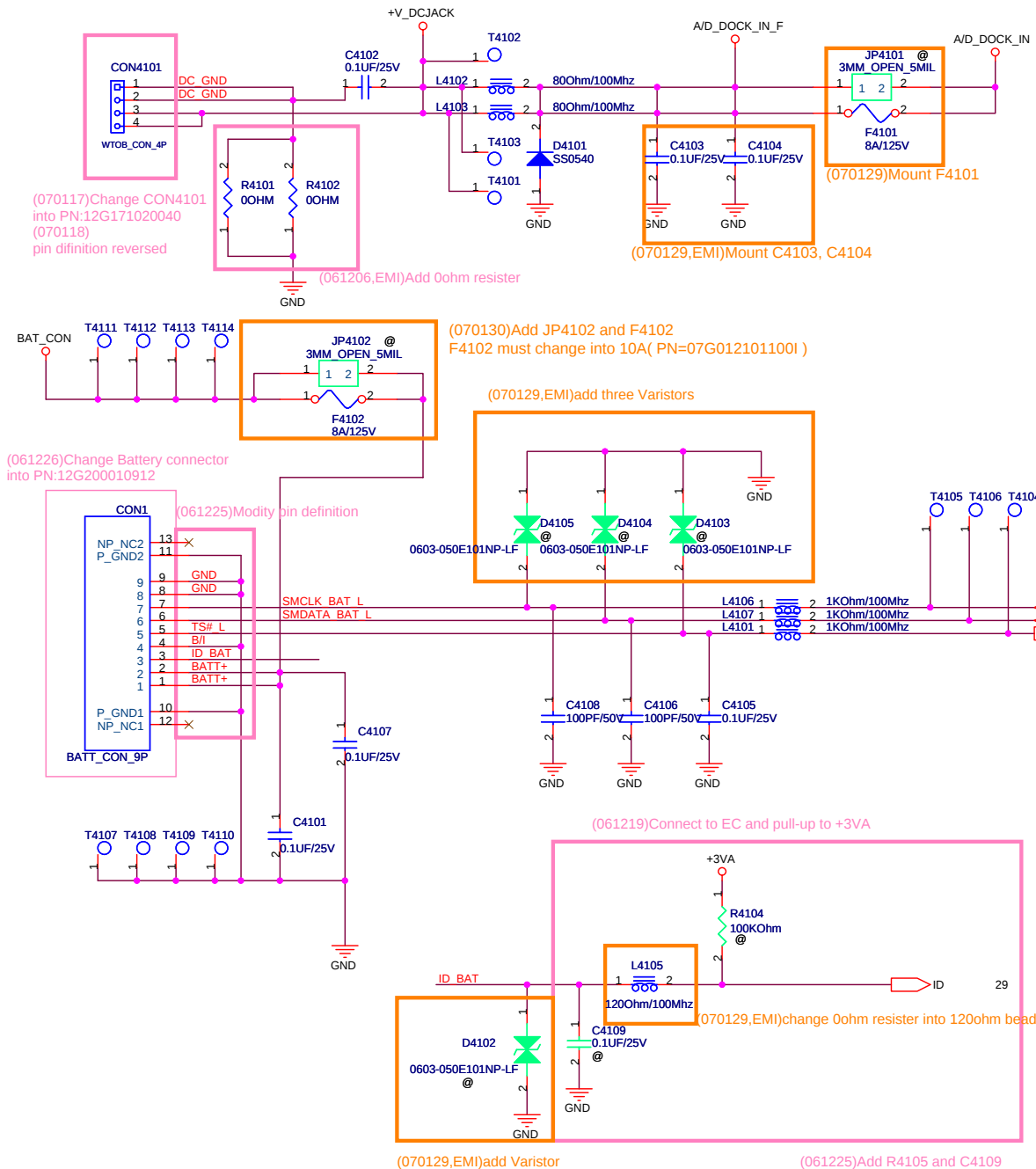
Reset Switch



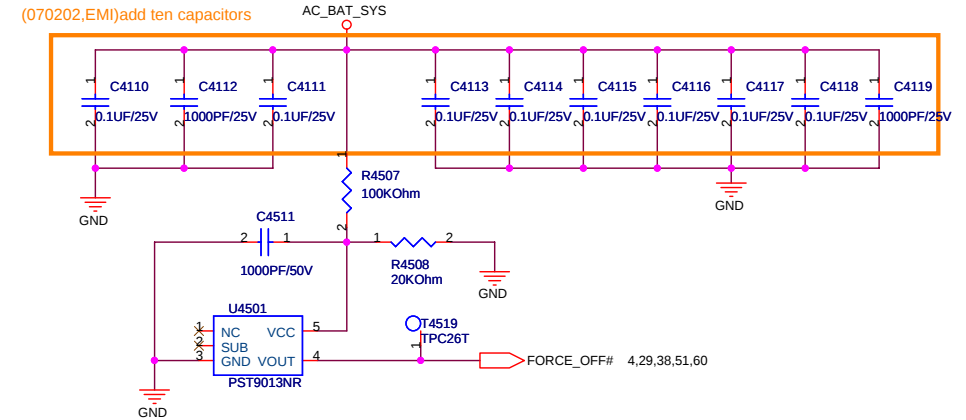
		Title : SW/LED	
ASUSALPHATeK COMPUTER INC.		Engineer: Hong Chou	
Size Custom	Project Name TERESA		Rev 1.1
Date: Monday, February 05, 2007		Sheet	38 of 57

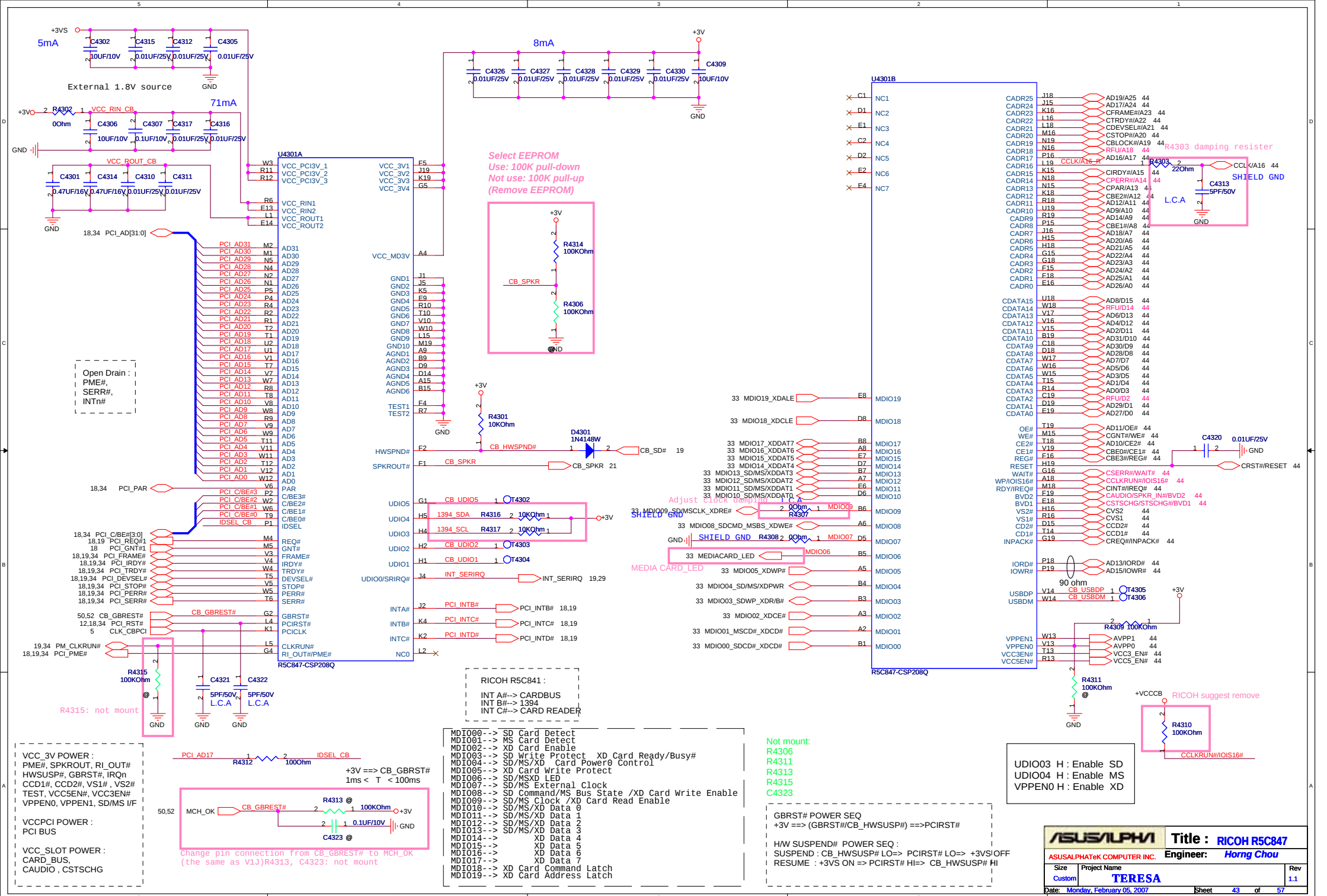


DC Power Jack



Without Battery & Pull out Adapter



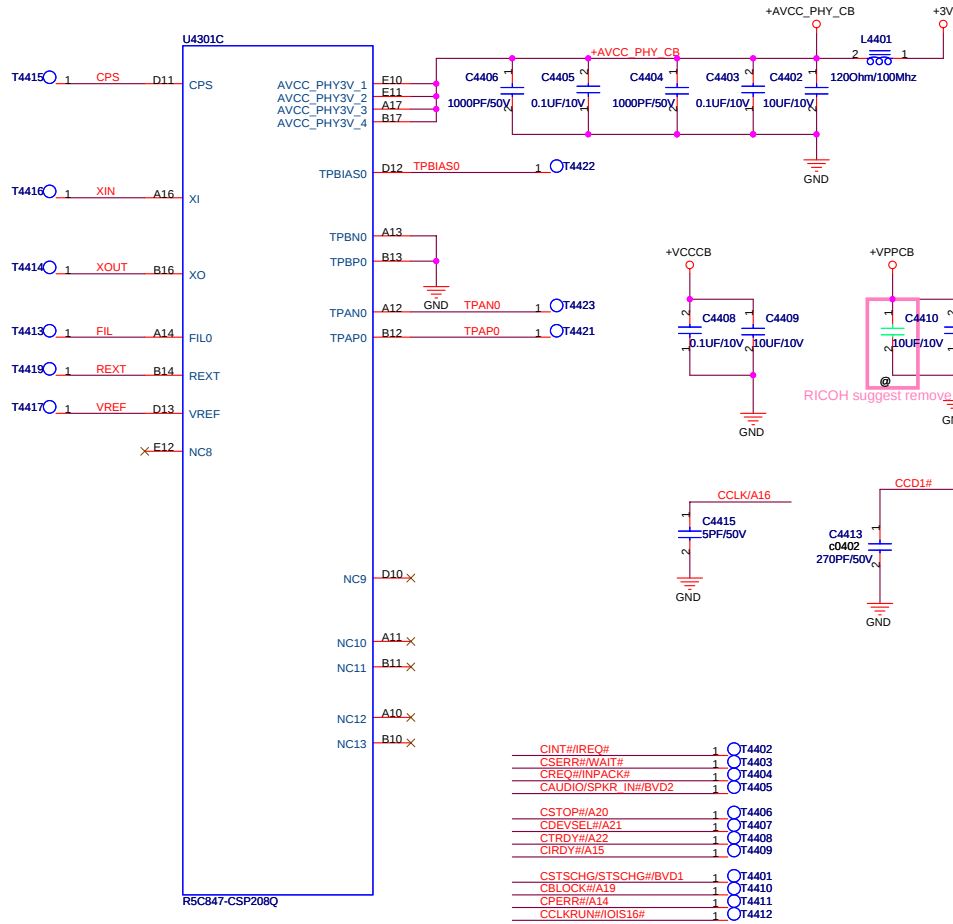


PCMCIA SOCKET

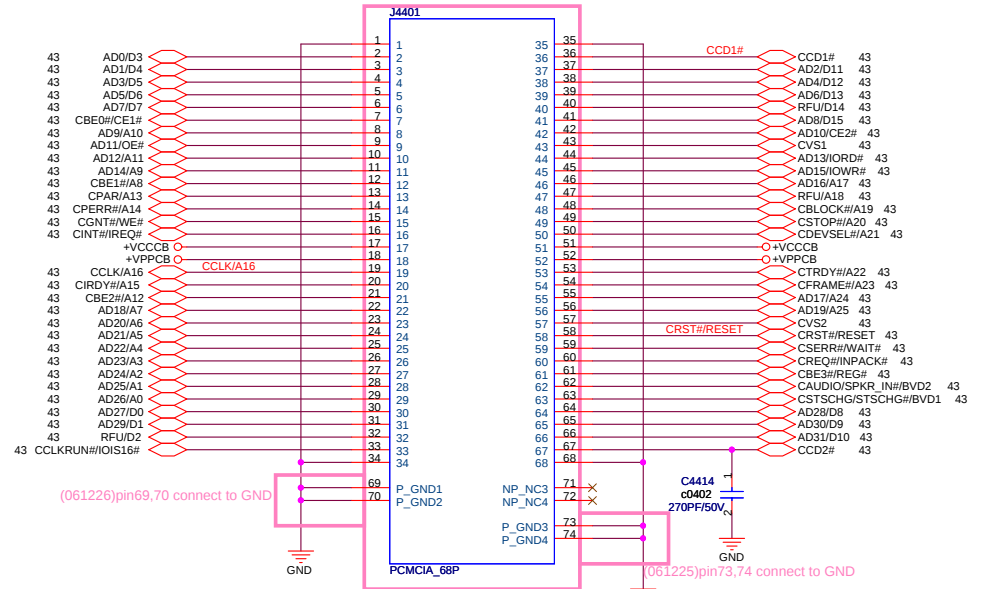
CCD1# CCD2#
L 16bit
OTHER 32bit

Not mount:
C4410

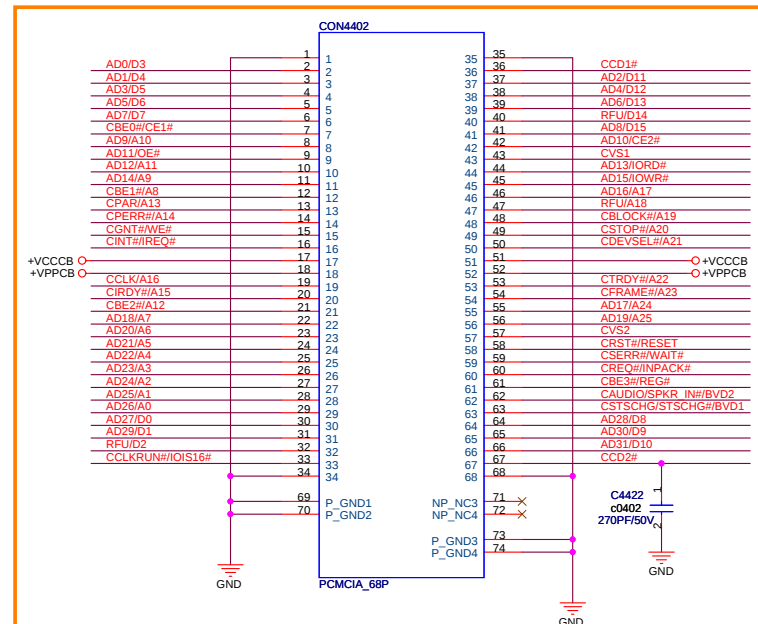
(061227)Change PCB footprint
PN=12G16040068Y



CINT#/#REQ# 1 T4402
CSERR#/#WAIT# 1 T4403
CREQ#/#INPACK# 1 T4404
CAUDIO/#SPKR IN#/#BVD2 1 T4405
CSTOP#/#A20 1 T4406
CDEVSEL#/#A21 1 T4407
CTRDY#/#A22 1 T4408
CIRDY#/#A15 1 T4409
CSTSCHG#/#STSCHG#/#BVD1 1 T4401
CBLOCK#/#A19 1 T4410
CPERR#/#A14 1 T4411
CCLKRUN#/#IOIS16# 1 T4412

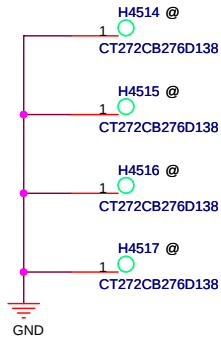


(070131)Add PCMCIA Socket



A:CPU BKT

PN:s01756



B:MDC NUT

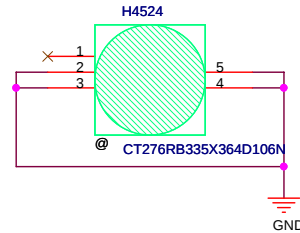
MDC NUT put on page35
(H3501, H3502)

F:MINI CARD NUT

MINI CARD NUT put on
page26(H2601, H2602)

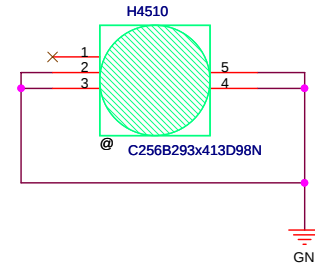
C:TOP TO BTM

PN:S01912



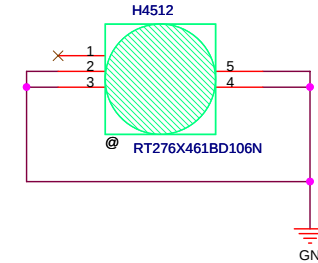
D:FIX MB

PN:s01769



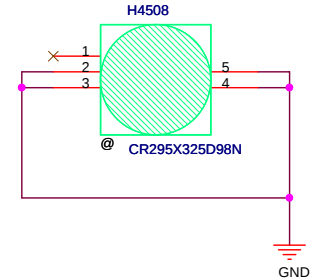
E:TOP TO BTM

PN:S01911



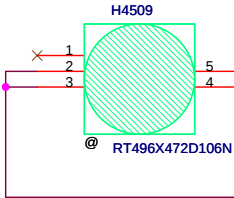
G:FIX MB

PN:s01783



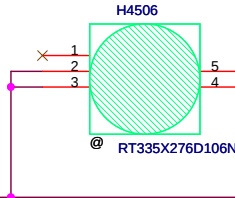
H:SYS BOSS

PN:S01914



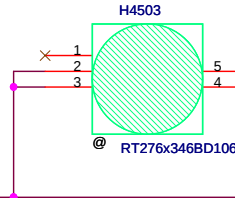
I:MB TO IO BKT

PN:S01913



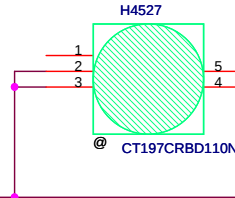
J:SYS BOSS

PN:S01915



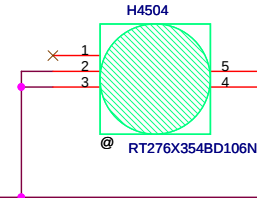
K:MB TO IO BKT

PN:S01705



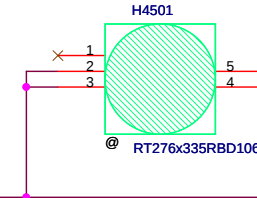
L:TOP TO BTM

PN:S01916



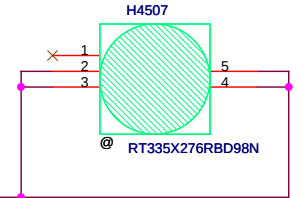
M:SYS BOSS

PN:s01917



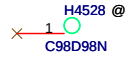
N:TOP TO BTM

PN:S01851

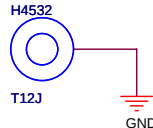


O:ALIGNMENT HOLE T:NB SINK NUT

PN:temp_5262_gh15

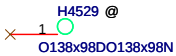


PN:13GNJ510M170-1



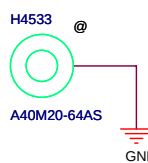
P:ALIGNMENT HOLE

PN:s01724



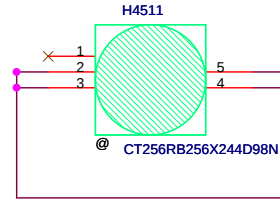
EMI NUT for LVDS cable

PN:13G021029050



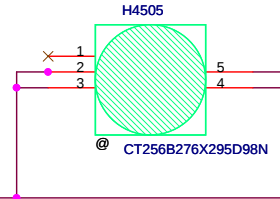
U:TOP TO BTM

PN:S01854



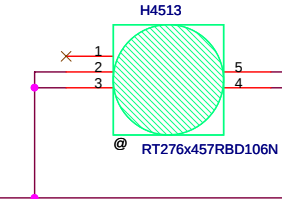
V:TOP TO BTM

PN:S01857



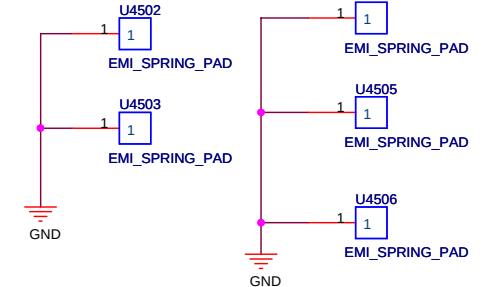
W:TOP TO BTM

PN:S01918



EMI SPRING

PN:13G021034050



R1.0 to R1.1

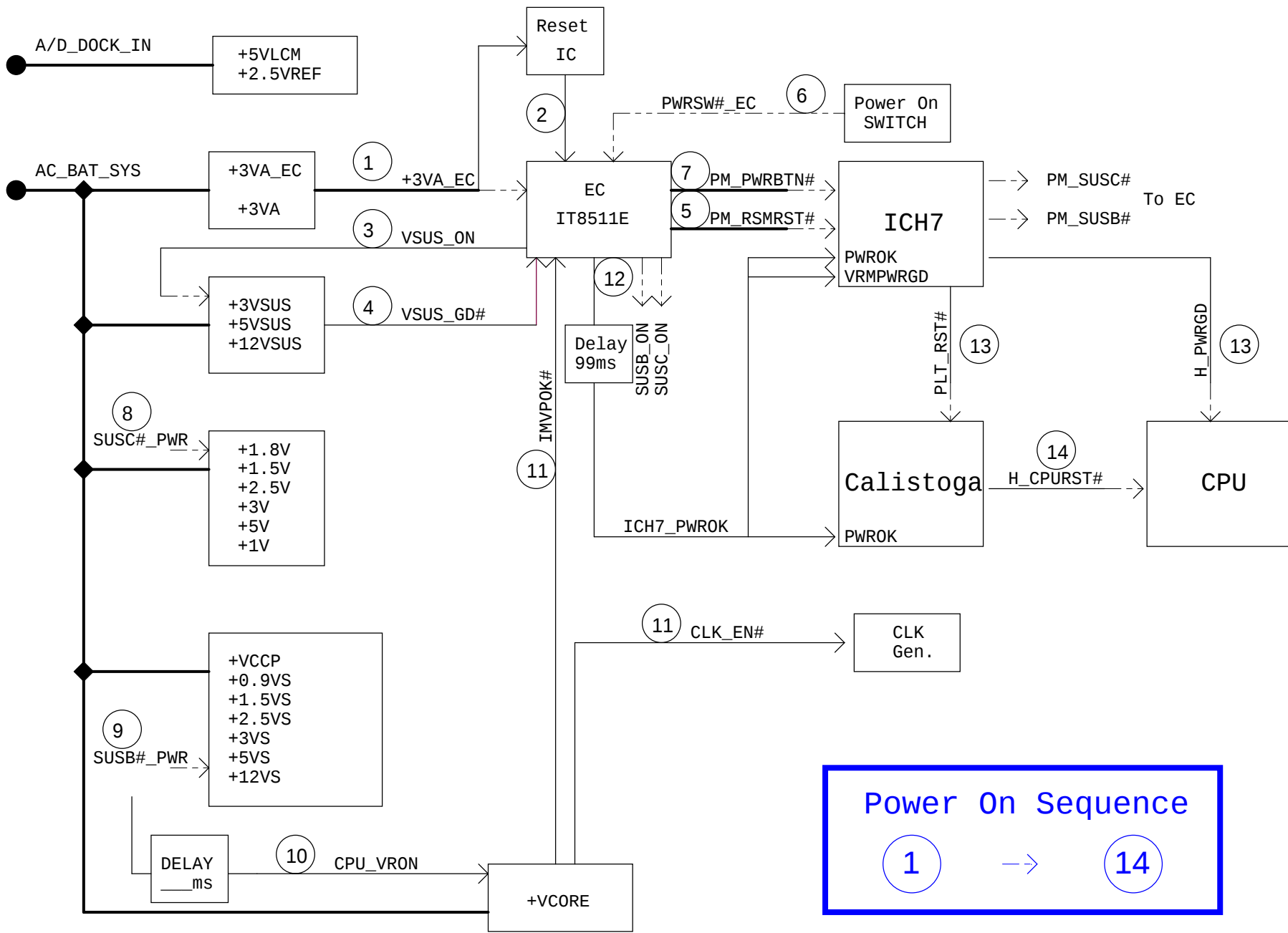
Page	Action
3	Change C304, C305, C306, C307, C308, C310, C312, C313 into 10UF for cost down.
4	Add R418 and Q404 to avoid error action.
7	Add R715 and R716 in other to improve signal quality.
12	Mount R1206 and Q1204 in other to reduce discharge time.
13	Change C1313, C1314 into 22PF in other to improve undershoot.
13	Change the rated current of the fuse(F1302) into 1A for customer's demand.
21	Mount R2105 and R2109, or there is no dialing tone.
21	Modify R2108 into 31.6Kohm in other to tune +5V_AUDIO.
21	Add three 0ohm resisters R2127, R2128, R2129 for EMI.
22	Change R2201~R2204 into 27Kohm for speaker volume.
22	Change 0ohm resisters(R2238, R2239) into beads.
22	Remove a N-MOS and a resistor on JACK_IN side due to change a new HP JACK.
22	Add 4 Varistors(D2202~D2205) for EMI.
23	Remove a N-MOS due to change a new MIC JACK.
23	Add a 120ohm bead L2304 and a 1000PF capacitor C2307 for EMI.
25	Add 0ohm resister R2503 and change Q2502 into unmount.
25	Add CON2502 in other to colayout with CON2501.
26	Connect not PCI_RST# but PLT_RST# to the RESET# signal of PCIE MiniCard for customer's demand.
27	Connect pin20 of MiniCard to the signal of OR conditions of WLAN_SW# and WLAN_ON# for customer's demand.
29	Change tolerance of R2918 into 1% and C2917 into 10% for the timing of EC_RST#.
29	Change WLAN_SW# into pull-up +3VSUS
30	Add 100PF capacitors C3011 and C3012 for EMI.
33	Add CON3302, RN3301, RN3302, RN3303, RN3304, RN3305 in other to colayout with CON3301.
33	Add Varistors D3304 and D3305 for EMI.
33	Change R3308 into 39ohm for the brightness of LED3301.
34	Change C3406, C3407 into 30PF in other to fit 25MHz frequency.
35	Place C3502, C3503 on the other side of L3503, L3504 for layout.
36	Change CE3602 from 100UF to 150UF in other to fit droop SPEC.
37	Change R3704, Q3705, R3708, Q3709, R3709, Q3710, R3710, Q3711, R3711, Q3711 into unmount because they don't affect the discharge circuit.
38	Change resisters R3805, R3806, R3807 into 620ohm in other to tune brightness.
41	Change the fuse F4101 into mount for customer's demand.
41	Add the colayout of JP4102 and F4102 for customer's demand.
41	Change 0ohm resister R4105 into 120ohm bead L4105 for EMI.
41	Add four Varistors D4102, D4103, D4104, D4105 and ten capacitors C4110~C4119 for EMI.
41	Chane C4103, C4104 into mount for EMI.
70	Chane R7002 into 80.6ohm for brightness.

R1.1 to R1.2

Page	Action

R1.2 to R2.0

Page	Action	Reason



Power On Sequence

1 → 14

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM	O	48	GPH0	VSUS_ON_EC	O
33	PWM1/GPA1	FAN_PWM	O	54	GPH1	VSUS_GD#	I
36	PWM2/GPA2	/	O	55	GPH2	IMVPOK#	I
37	PWM3/GPA3	BAT_LOW_BEEP(Reserved)	O	69	GPH3	PM_PWRBTN#	O
38	PWM4/GPA4	CHG_LED_UP#	O	70	GPH4	SUSC_EC#	O
39	PWM5/GPA5	PWR_LED_UP#	O	75	GPH5	SUSB_EC#	O
40	PWM6/GPA6	BATSEL_3S#	O	76	GPH6	CPU_VRON	O
43	PWM7/GPA7	LCD_BACKOFF#	O	105	GPH7	PM_RSMRST#	O
153	RXD/GPB0	NUM_LED	O	148	GP10	ICH_PWROK_EC	O
154	TXD/GPB1	CAP_LED	O	149	GP11	WATCHDOG#	O
162	GPB2	SCRL_LED	O	152	GP12	/	
163	SMCLK0/GPB3	SMCLK_BAT	I/O	155	GP13	CHG_EN#	O
164	SMDAT0/GPB4	SMDATA_BAT	I/O	156	GP14	PRECHG	O
5	GA20/GPB5	A20GATE	O	168	GP15	BAT_LL#	O
6	KBRST#/GPB6	RCIN#	O	174	GP16	BAT_LEARN	O
165	GPB7	THRO_CPU	O	109	GP17	/	
47	CLKOUT/GPC0	/	O	99	DAC0/GPJ0	CHG_FULL_LED#_EC	O
169	SMCLK1/GPC1	SMB1_CLK	I/O	100	DAC1/GPJ1	/	
170	SMDAT1/GPC2	SMB1_DAT	I/O	101	DAC2/GPJ2	INVTER_DA	O
171	GPC3	/	I	102	DAC3/GPJ3	BATSEL_2P#	O
172	TMR10/WUI2/GPC4	ACIN_OC#	I	97	GPJ4	/	
175	GPC5	OP_SD#	O	98	GPJ5	/	
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I			/	
1	CK32KOUT/GPC7	/	O			/	
26	RI1#/WUI0/GPD0	PM_SUSB#	I	81	ADC0/GPK0	BAT0_AD	I
29	RI2#/WUI1/GPD1	PM_SUSCH#	I	82	ADC1/GPK1	/	
30	LPCRST#/WUI4//GPD2	PLT_RST#	I	83	ADC2/GPK2	AC_AD	I
31	ECSCI#//GPD3	ECSCI#	O	84	ADC3/GPK3	/	
41	GPD4	/		93	ADC8/GPK4	KB_ID0	I
42	GINT1/GPD5	/		94	ADC9/GPK5	KB_ID0	I
62	TACH0/GPD6	FAN0_TACH	I				
63	TACH1/GPD7	/	O				
87	ADC4/GPE0	WLAN_SW#_EC(Reserved)	I	8	GPL0	/	O
88	ADC5/GPE1	/	I	11	GPL1	/	O
89	ADC6/GPE2	/	I	12	GPL2	/	I
90	ADC7/GPE3	/	I	20	GPL3	/	O
2	PWRSW/GPE4	PWRSW#_EC	I	21	GPL4	/	
44	WUI5/GPE5	/	I	106	GPL5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I	107	GPL6	/	
25	CLKRUN#/WUI7/GPE7	/	O	108	GPL7	/	
110	PS2CLK0/GPF0	/		22	ECSMH#/GPM0	EXTSM#	O
111	PS2DAT0/GPF1	/		23	PWUREQ#/GPM1	/	
114	PS2CLK1/GPF2	/	I/O	85	KSO16/GPM2	/	
115	PS2DAT1/GPF3	/	I/O	86	KSO17/GPM3	ID_EC (Reserved)	I
116	PS2CLK2/GPF4	TPAD_CLK		91	CTX/GPM4	/	
117	PS2DAT2/GPF5	TPAD_DAT		92	CRX/GPM5	/	
118	PS2CLK3/GPF6	/					
119	PS2DAT3/GPF7	/	I				
113	FA16/GPG0	FA16					
112	FA17/GPG1	FA17					
104	FA18/GPG2	FA18					
103	FA19/GPG3	/					
3	FA20/GPG4	THRM_CPU#	I				
4	FA21/GPG5	/					
27	LPC80HL/GPG6	PMTHERM#	O				
28	LPC80LL/GPG7	AC_APR_UC#	I				

ICH7-M GPIO SETTING

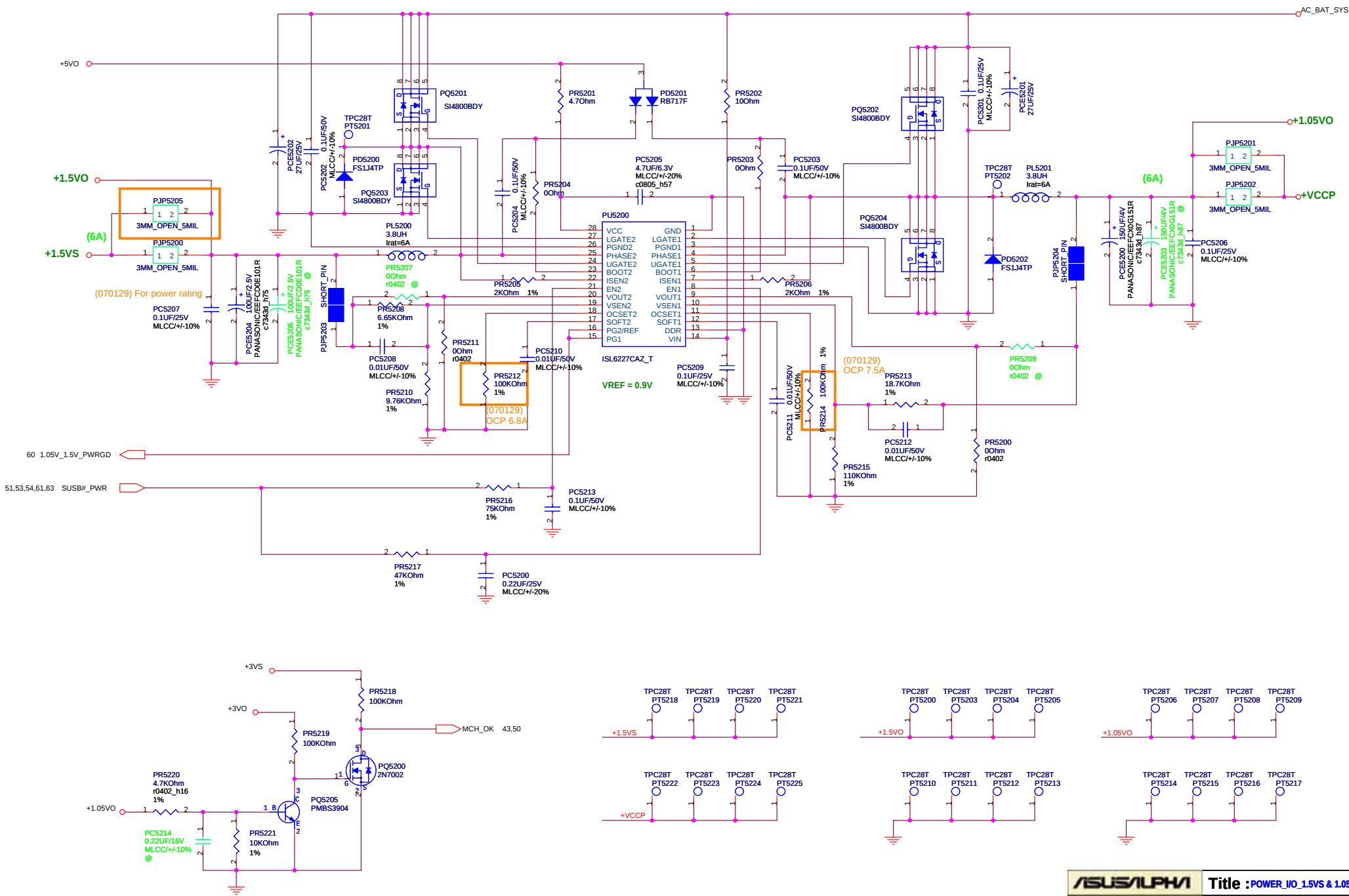
Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	/	I/O
AC18	GPIO07	PM_THERM#_GPIO (Reserved)	I
E21	GPIO08	EXTSM#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	WLAN_SW#_ICH	I
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SC#	I
E19	GPIO13	NEWCARD_DET#	I
R4	GPIO14	BAT_LL#_ICH (Reserved)	I
E22	GPIO15	WLAN_LED#	O
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STPPCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	/	I
AF21	GPIO20/STPCPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	/	I
A13	REQ4#/GPIO22	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	/	
R3	GPIO24	/	
D20	GPIO25	CB_SD#	O
A21	GPIO26	/	
B21	GPIO27	BTO_DEV0	I
E23	GPIO28	NEWCARD_OFF#	O
C3	GPIO29/OC#5	USB_OC_5#	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC_7#	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	I/O
AC19	GPIO33/AZ_DOCK_EN#	BTO_DEV1	I
U2	GPIO34/AZ_DOCK_RST#	BTO_DEV2	I
AD21	GPIO35	/	O
AH19	GPIO36/SATA2GP	/	
AE19	GPIO37/SATA3GP	PCB_ID0	I
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUUPWRGD	H_PWRGD	O

Indigo: the same as T12F
Pink: different from T12F

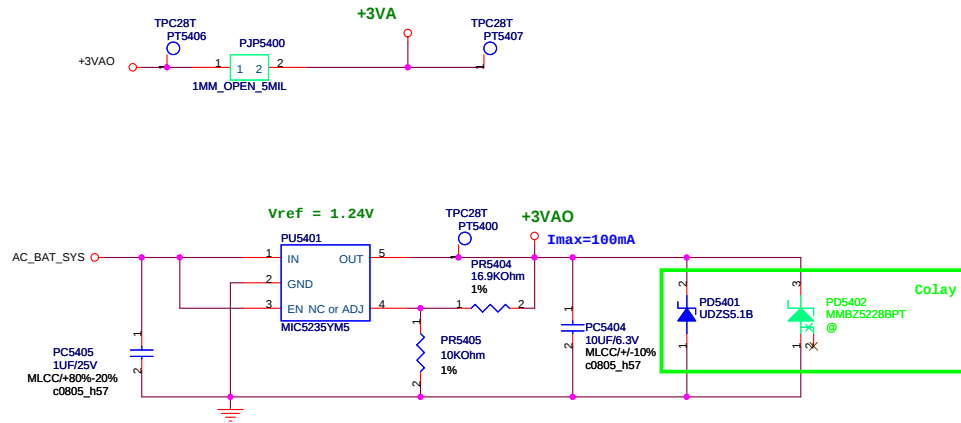
PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

PCIE Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

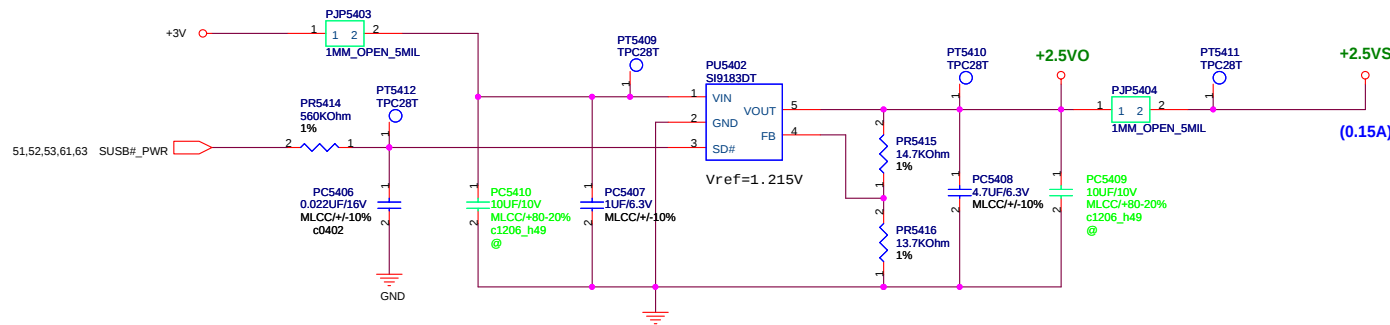
SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)



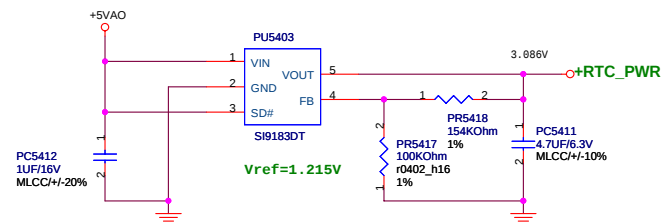
+3VAO



+2.5VS

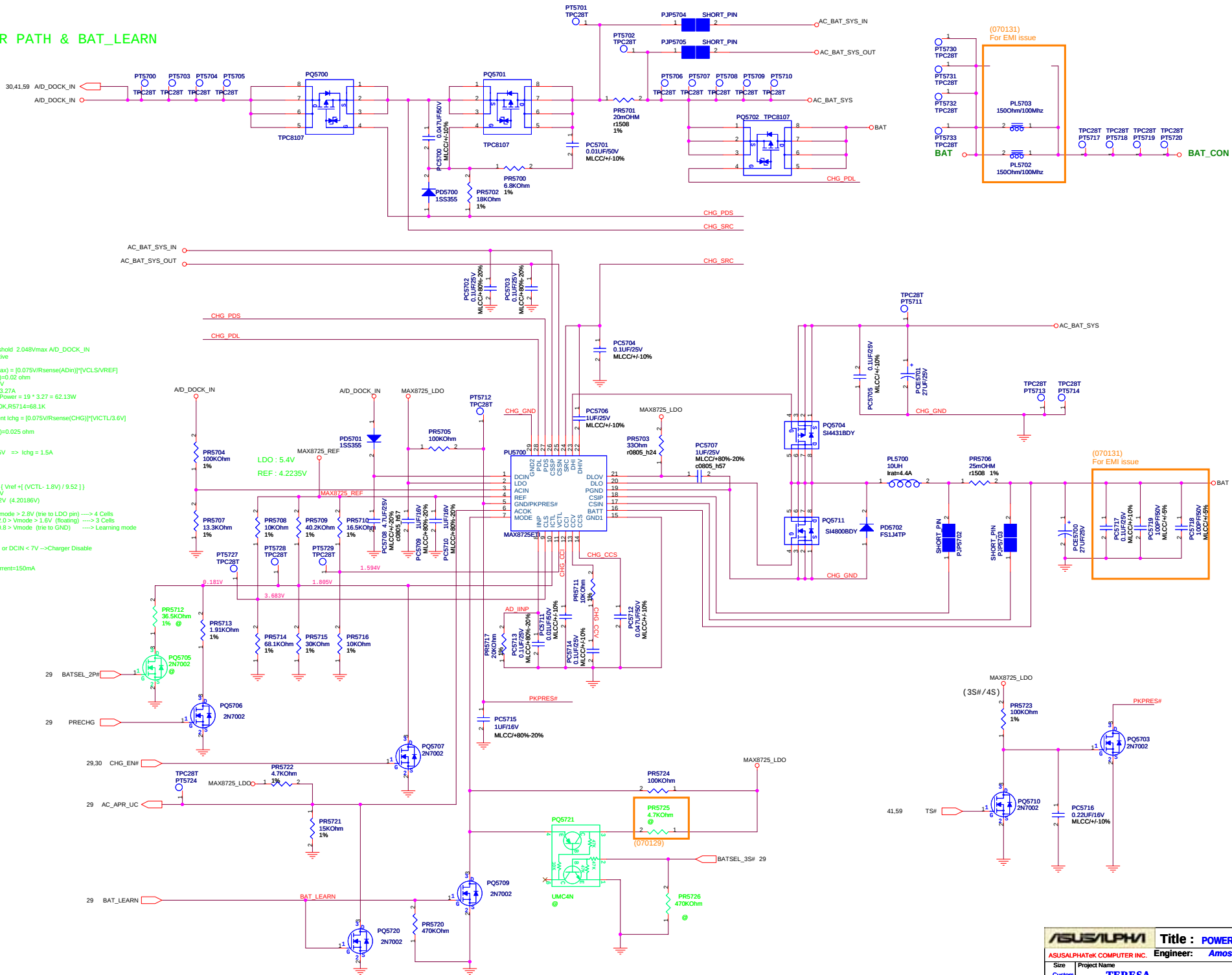


+RTC_PWR

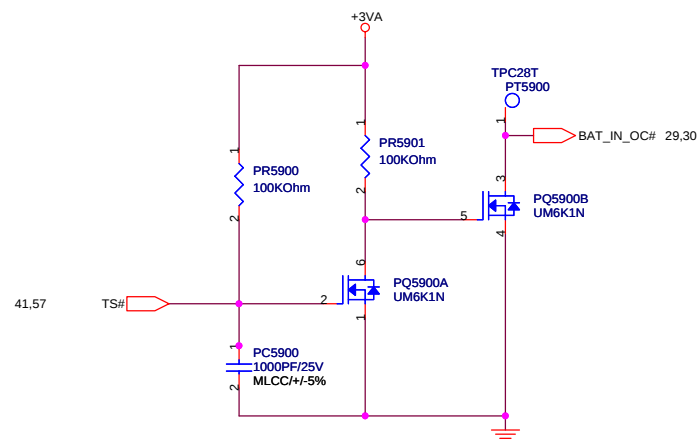


POWER PATH & BAT_LEARN

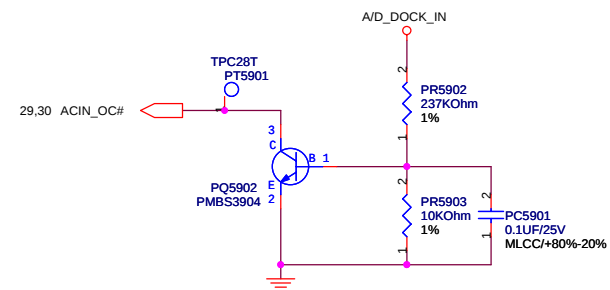
- ⊗ AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active
Adapter Iin(max) = $[0.075V/Rsense(ADin)] \cdot [VCL/S/VREF]$
Rsense(ADin)=0.02 ohm
VCL= 3.663V
⇒ Iin(max)=3.27A
⇒ Constant Power = $19 \cdot 3.27 = 62.13W$
⇒ R5708=10K, R5714=68.1K
- ⊗ Charge Current Ichg = $[0.075V/Rsense(CHG)] \cdot [VICTL/3.6V]$
Rsense(CHG)=0.025 ohm
VICTL= 1.805V ⇒ Ichg = 1.5A
- ⊗ Vbatt = Cell * (Vref + (VCTL - 1.8V) / 9.52)
VCTL= 1.594V
⇒ Vbatt = 4.2V (4.20186V)
- ⊗ Mode pin : Vmode > 2.8V (tie to LDO pin) → 4 Cells
2.0 > Vmode > 1.6V (floating) → 3 Cells
0.8 > Vmode (tie to GND) → Learning mode
- ⊗ VICTL< 0.8V or DCIN < 7V → Charger Disable
- ⊗ Precharge current=150mA



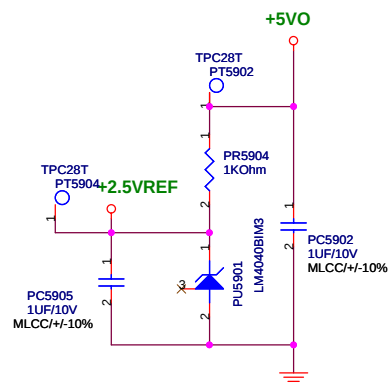
BATTERY IN DETECT



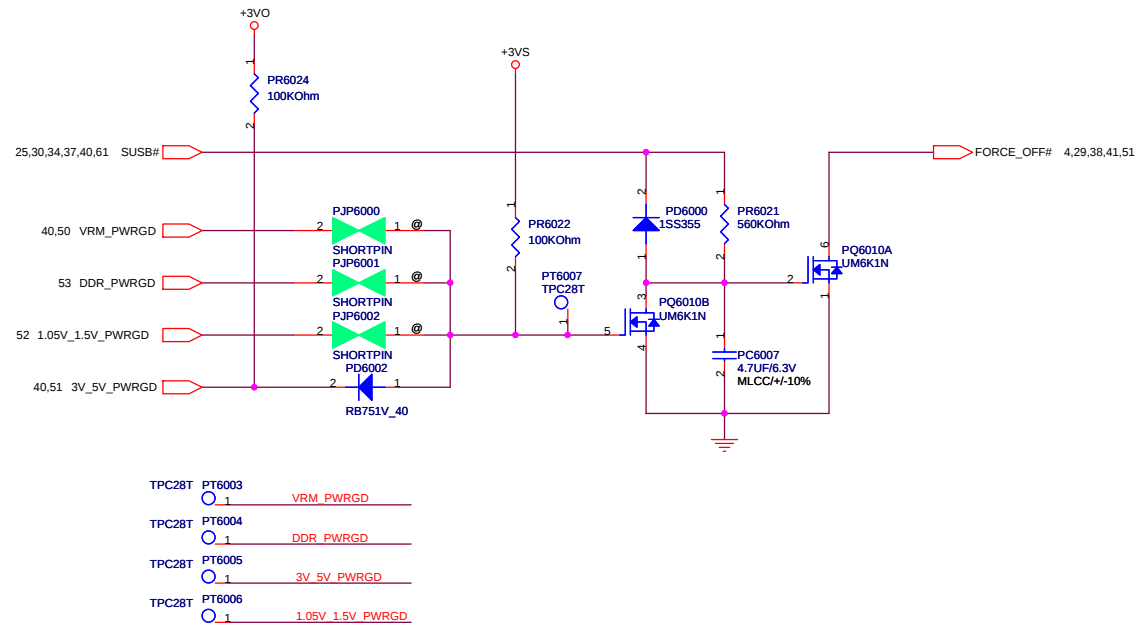
ADAPTER IN DETECT



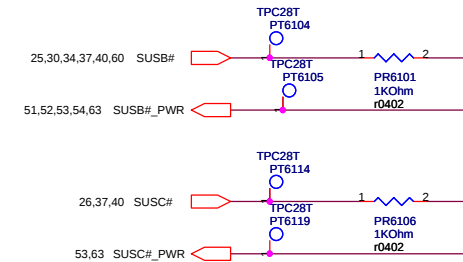
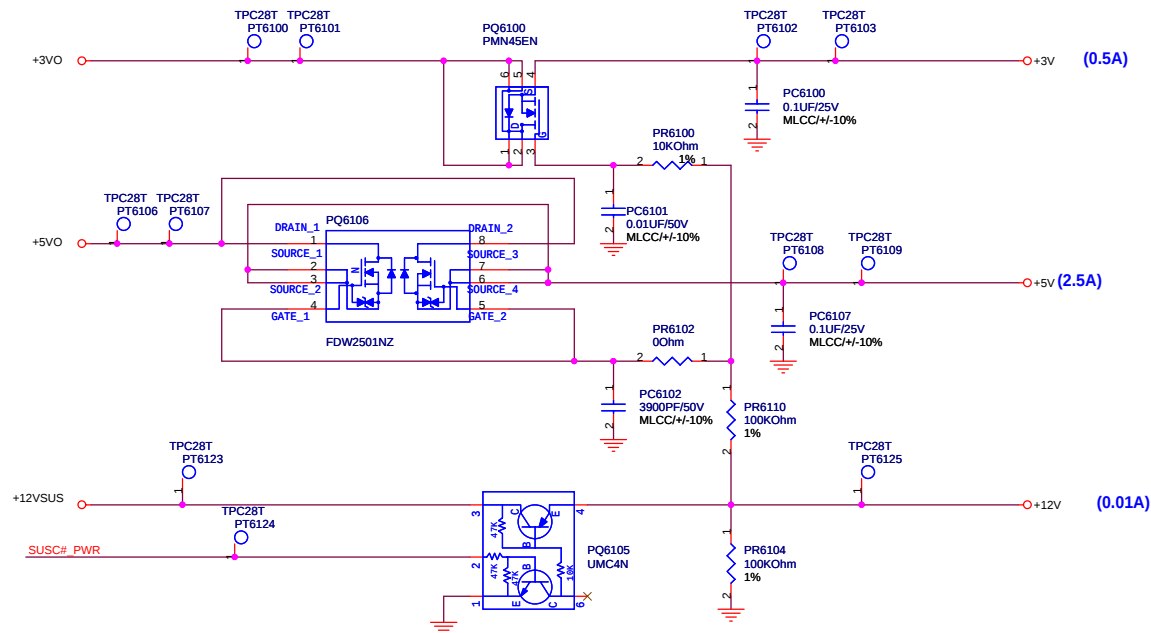
+2.5VREF



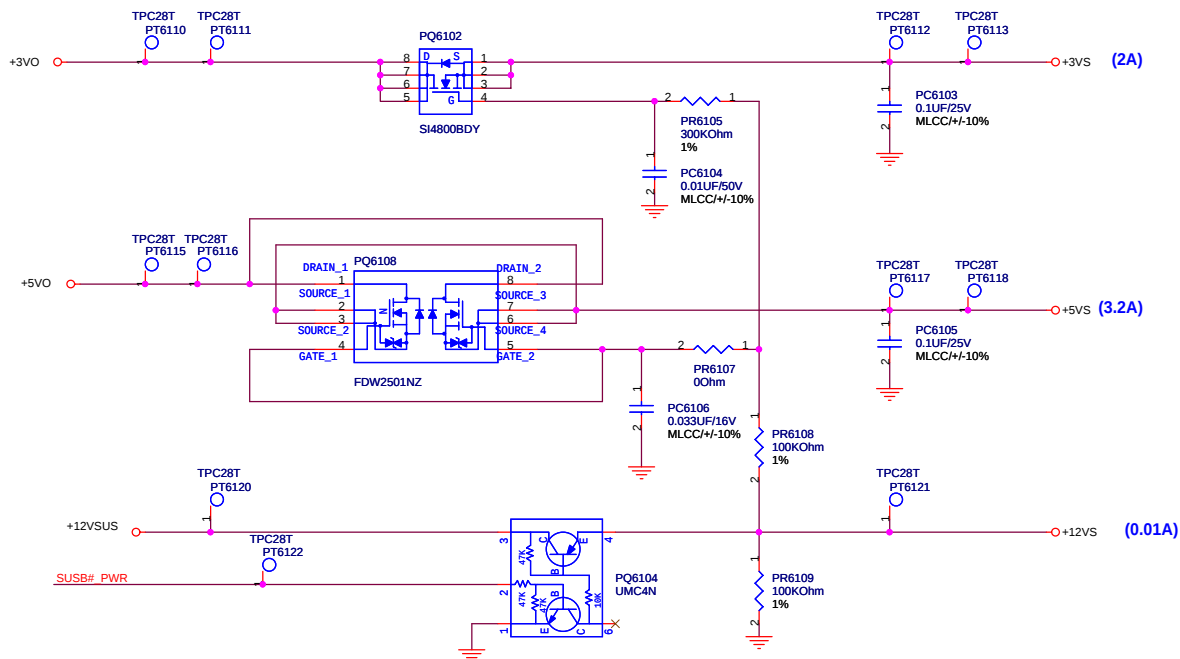
POWER GOOD DETECTOR



SUSC#_PWR POWER

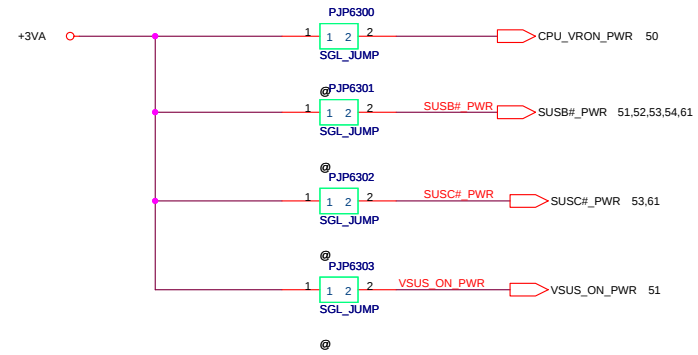


SUSB#_PWR POWER



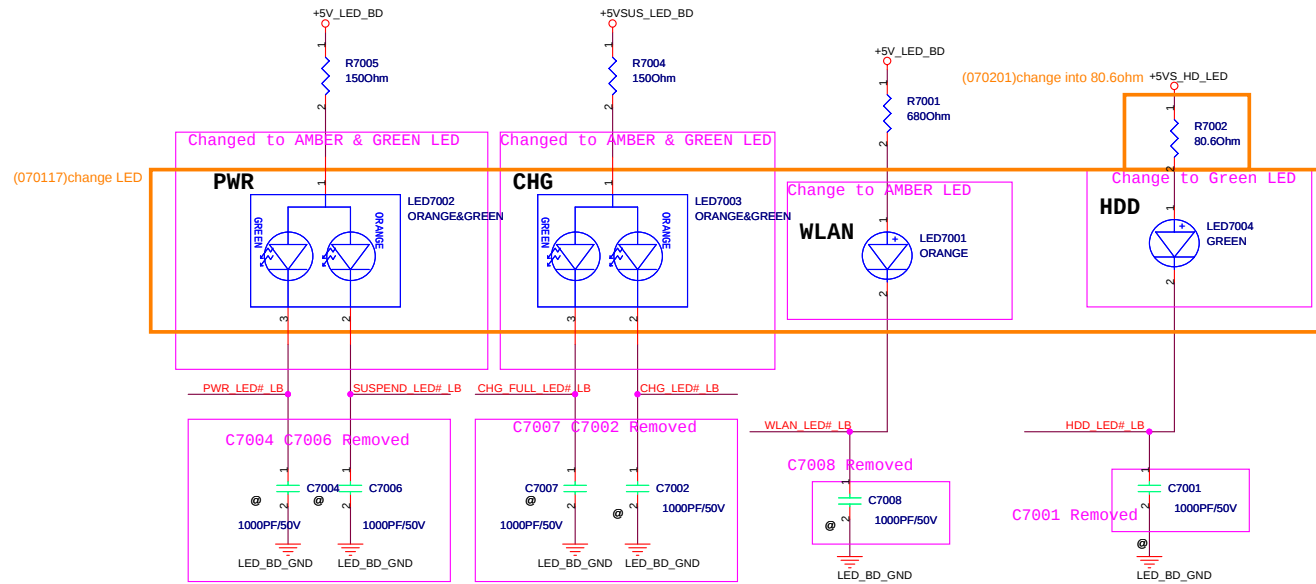
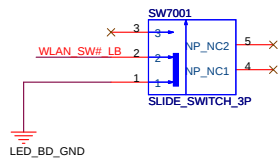


FOR POWER TEST

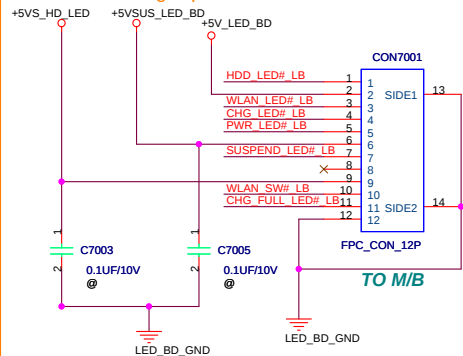


LEFT & RIGHT Button remove to TP BOARD

New added SW for Teresa

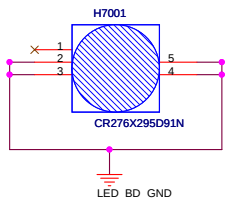


070115 Change pin define

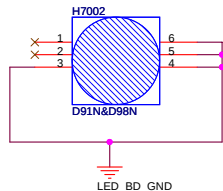


CON to T/P remove to TP BOARD

IR receive module removed



DETAIL: Q



DETAIL: S

