

CLK-GEN
ICS954226

HOST 133/166MHz
PCIE 100MHz
VGA 96MHz
USB 48MHz
PCI 33MHz
REF 14MHz

Page 2

3V / 5V

+3VPCU
+3V_S5
+3VSUS
+5VSUS
+3V
+5V
+12V

Page 22

1.8V / 1.05V

+1.8VSUS
SMDDR_VTERM
+1.05V

Page 24

1.5V / 2.5V

+1.5V
+2.5V

Page 25

CPU CORE

+VCC_CORE

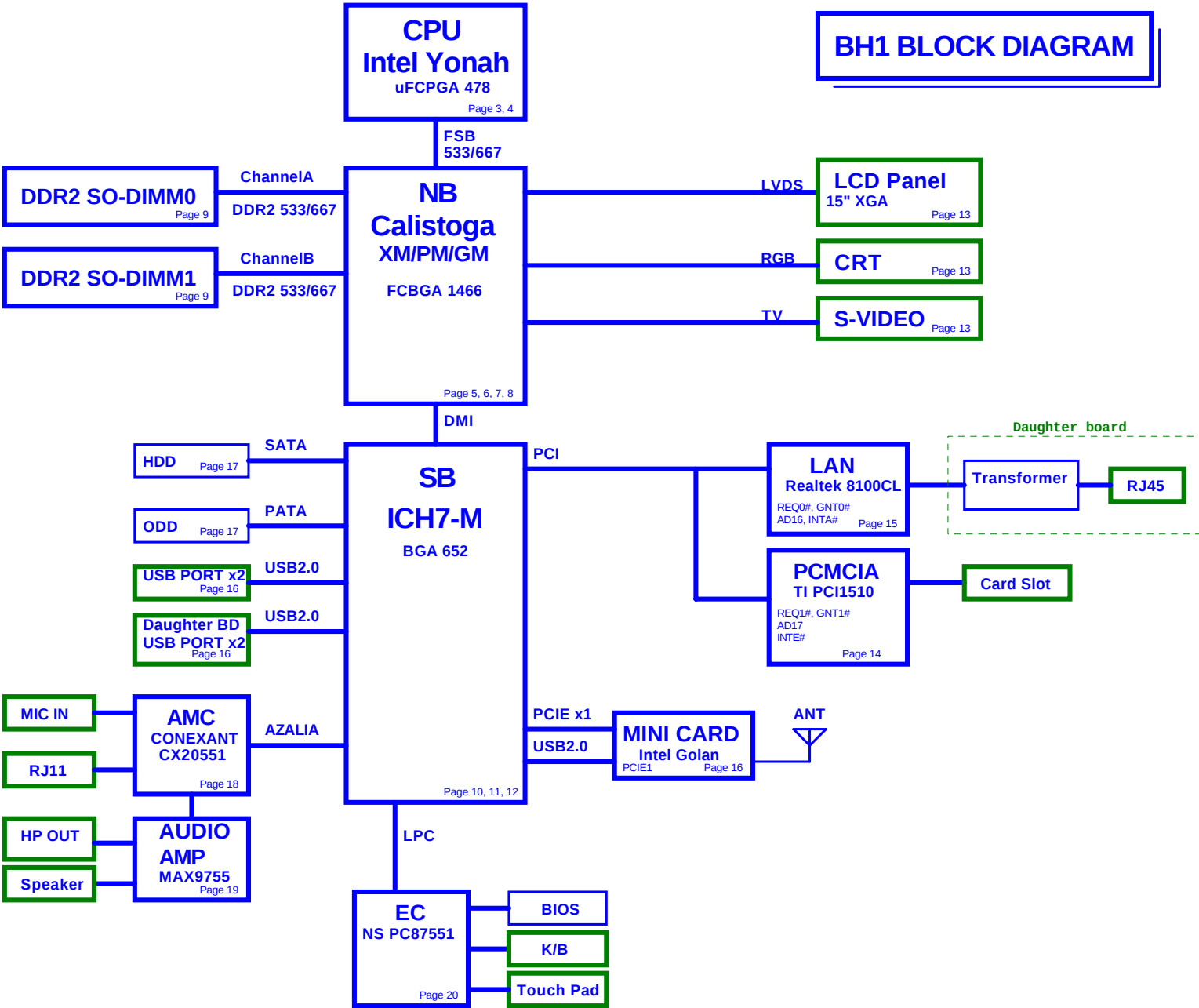
Page 23

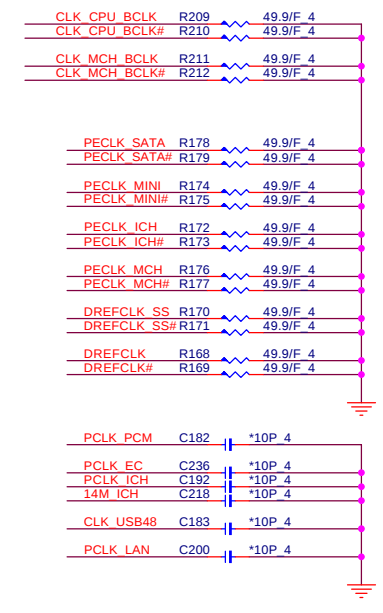
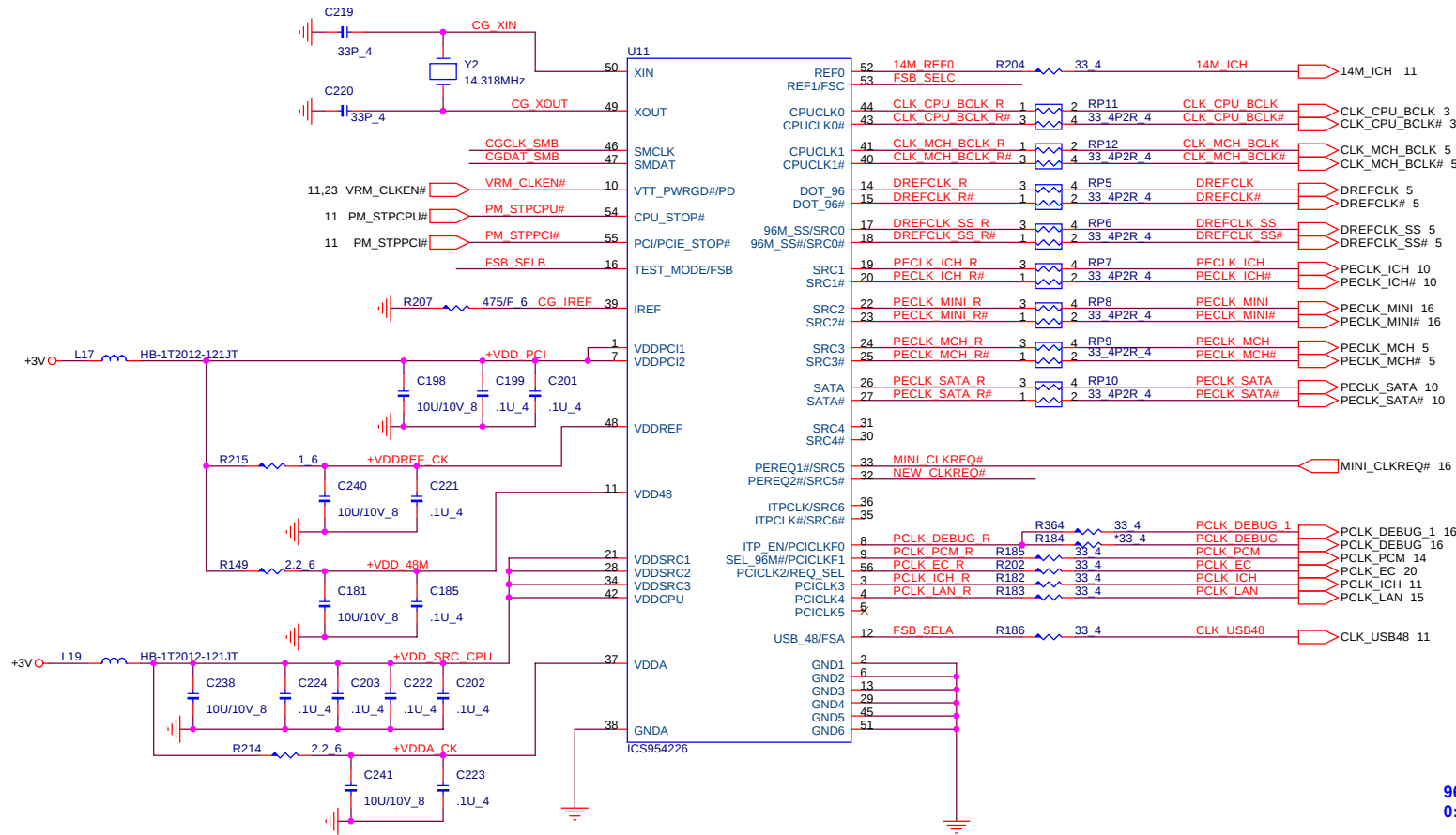
BATTERY CHARGER

VIN

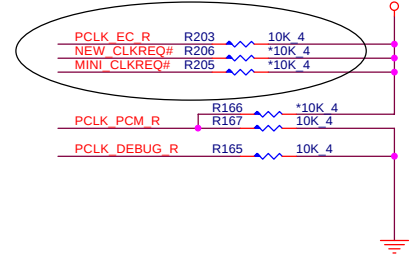
Page 26

Power State Table		
Power Name	Control Signal	Power State
+3VPCU	N/A	ALWAYS
+3V_S5	S5_ON	S0 - S5
+3VSUS	SUSON	S0 - S3
+3V	MAINON	S0
+5VSUS	SUSON	S0 - S3
+5V	MAINON	S0
+12V	MAINON	S0
+1.8VSUS	SUSON	S0 - S3
+SMDDR_VTERM	MAINON	S0
+1.05V	MAINON	S0
+1.5V	MAINON	S0
+2.5V	MAINON	S0
+VCC_CORE	VRON	S0



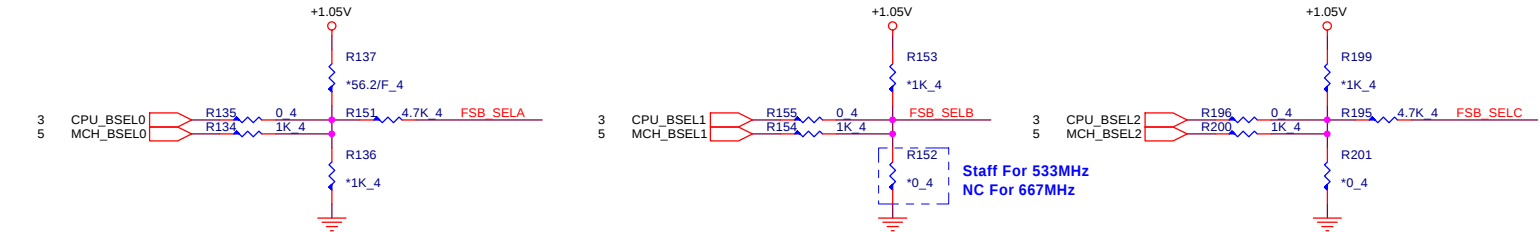
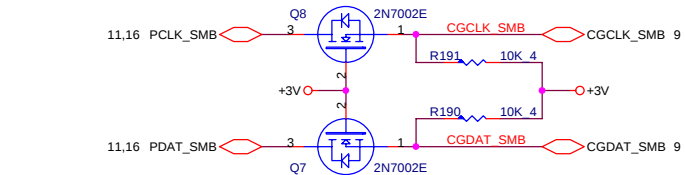


96M/SRC0 SELECT
0: 96M 1: SRC0



PEREQ Control Pair	
PEREQ1	SATA,PCIEX0, 2
PEREQ2	PCIEX1, 3, 4

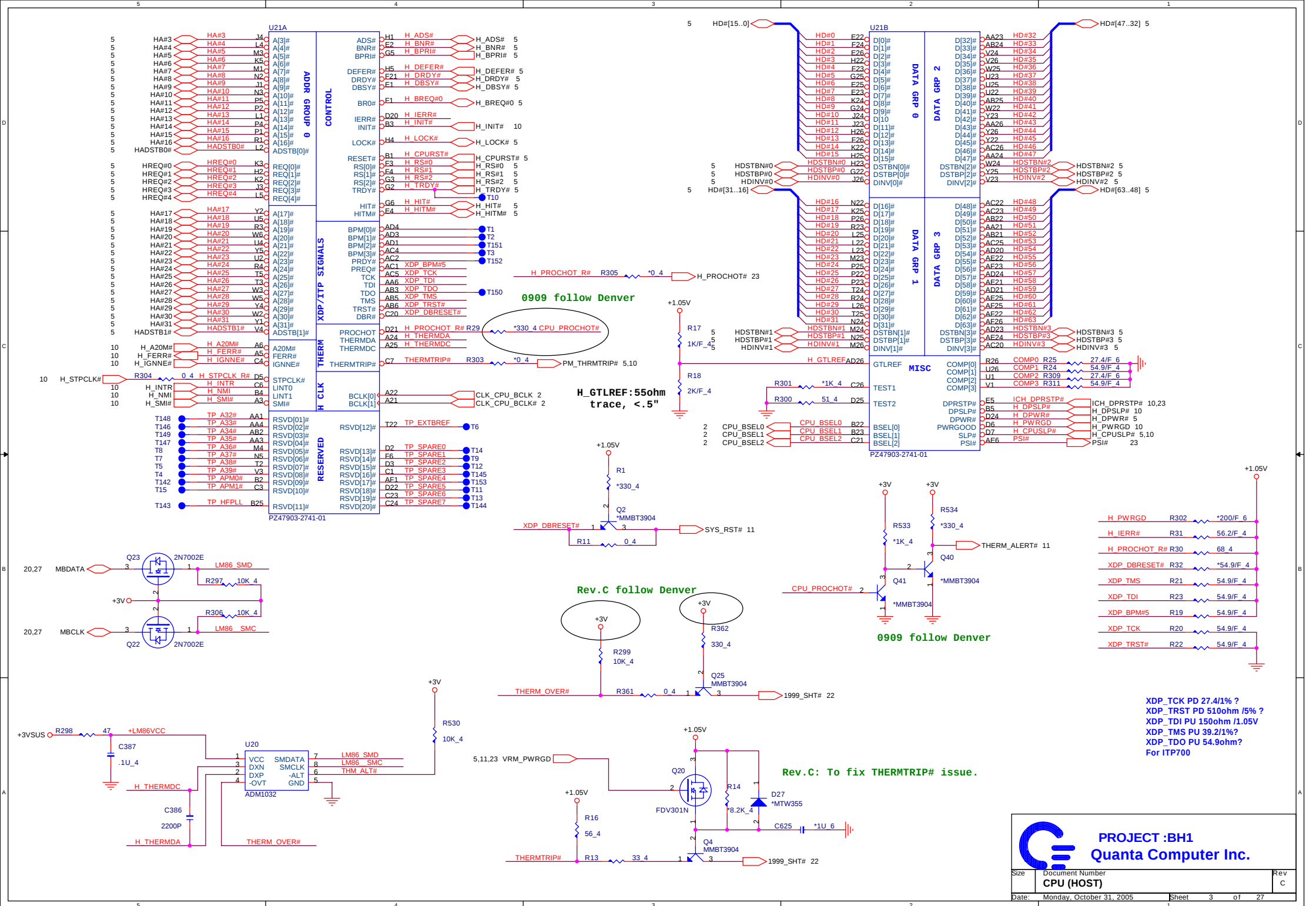
FSC	FSB	FSA	CPU	SRC	PCI	FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33	0	1	0	200	100	33
0	0	1	133	100	33	0	0	0	266	100	33
0	1	1	166	100	33	1	0	0	333	100	33
1	1	1	200	100	33	1	1	0	400	100	33

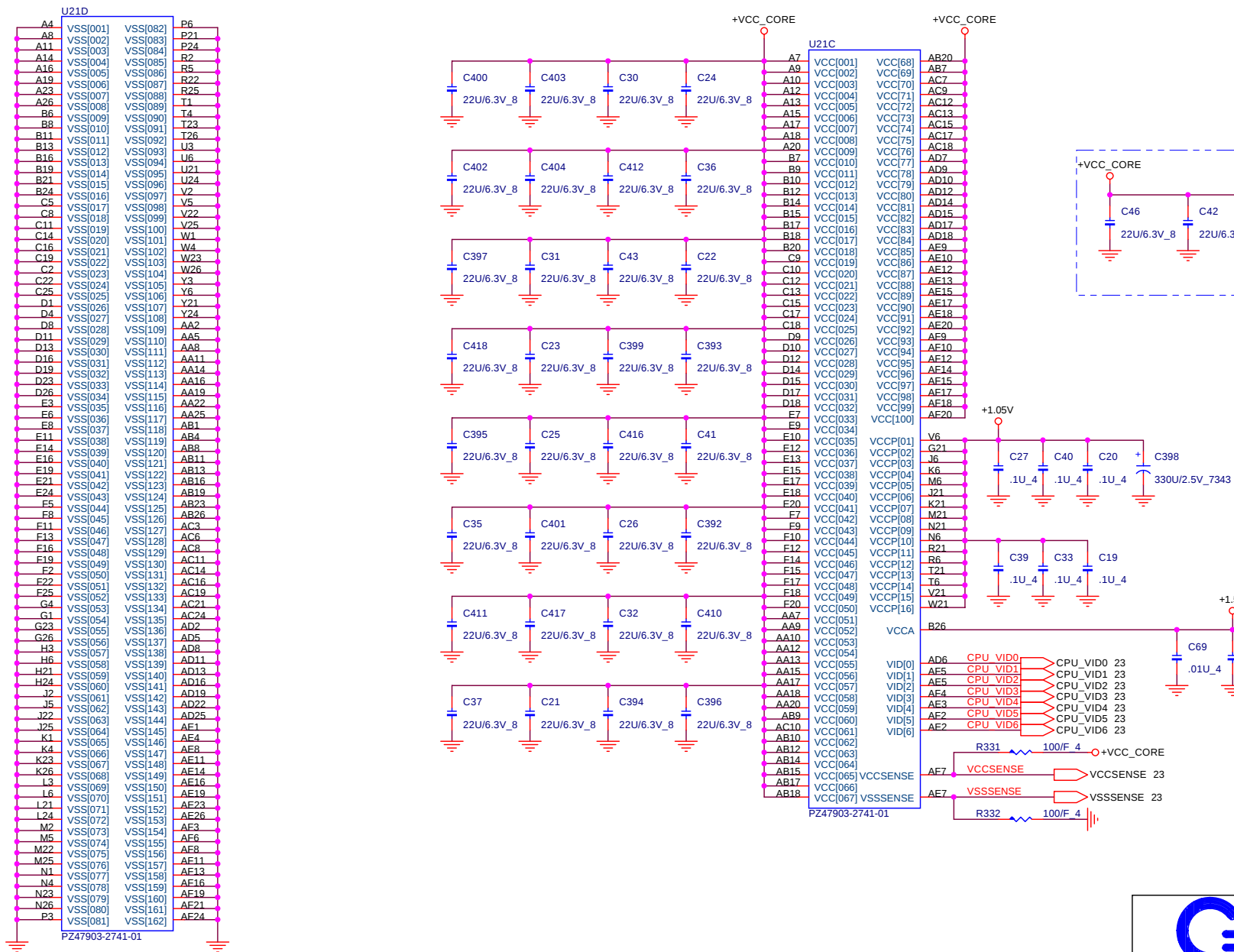


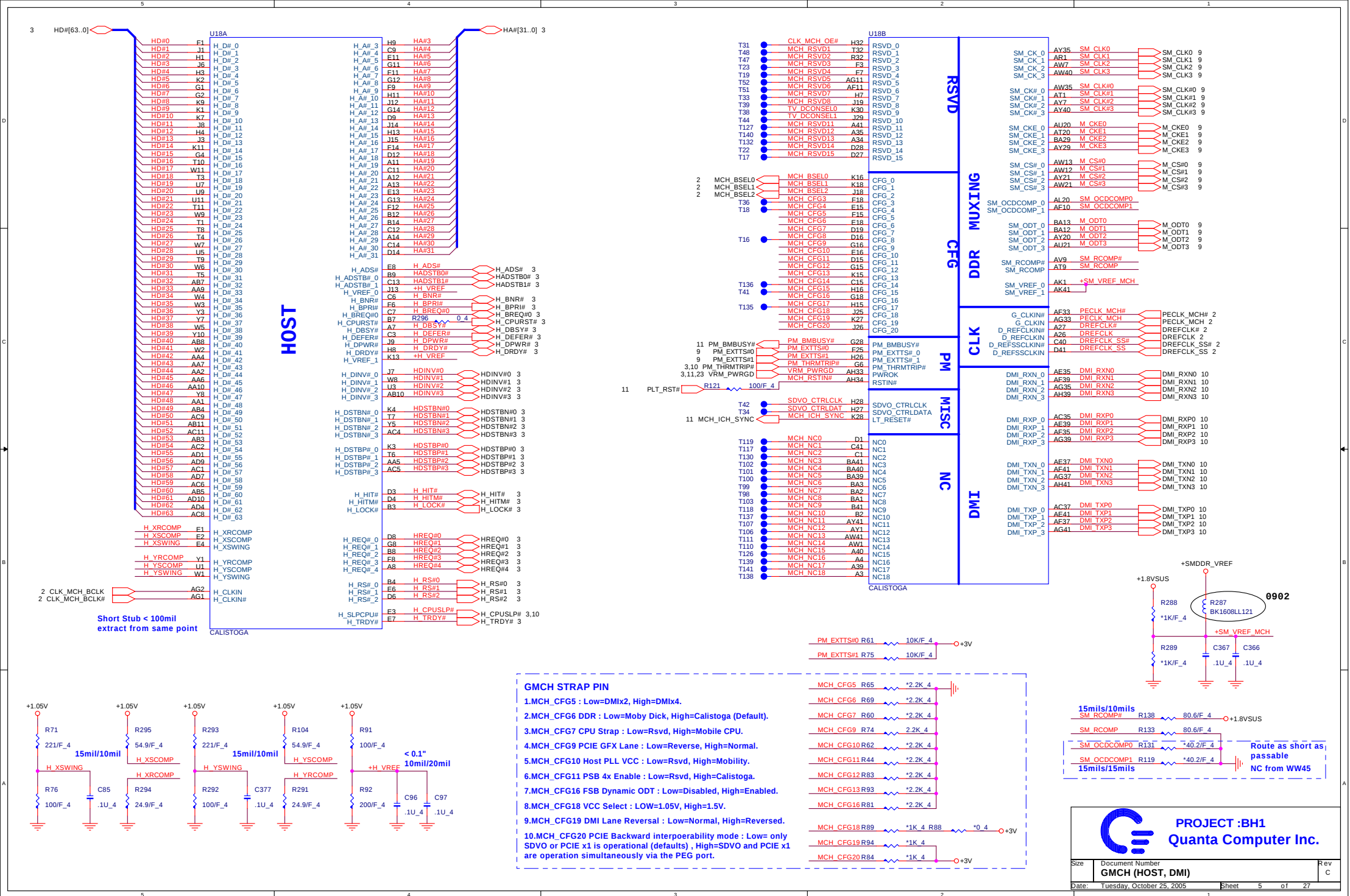
PROJECT :BH1
Quanta Computer Inc.

Size: Document Number: **CLOCK GENERATOR** Rev: C

Date: Tuesday, October 25, 2005 Sheet: 2 of 27







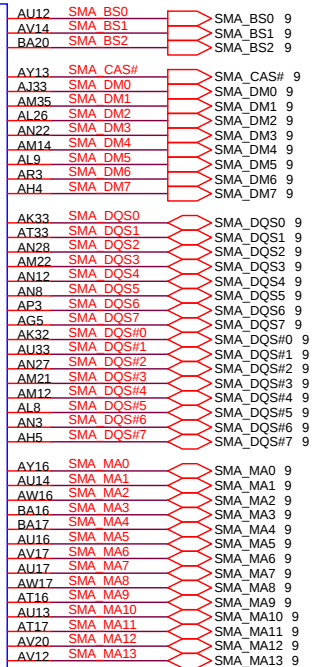
9 SMA_DQ[63..0]



U18D

DDR SYSTEM MEMORY A

CALISTOGA



9 SMB_DQ[63..0]



U18E

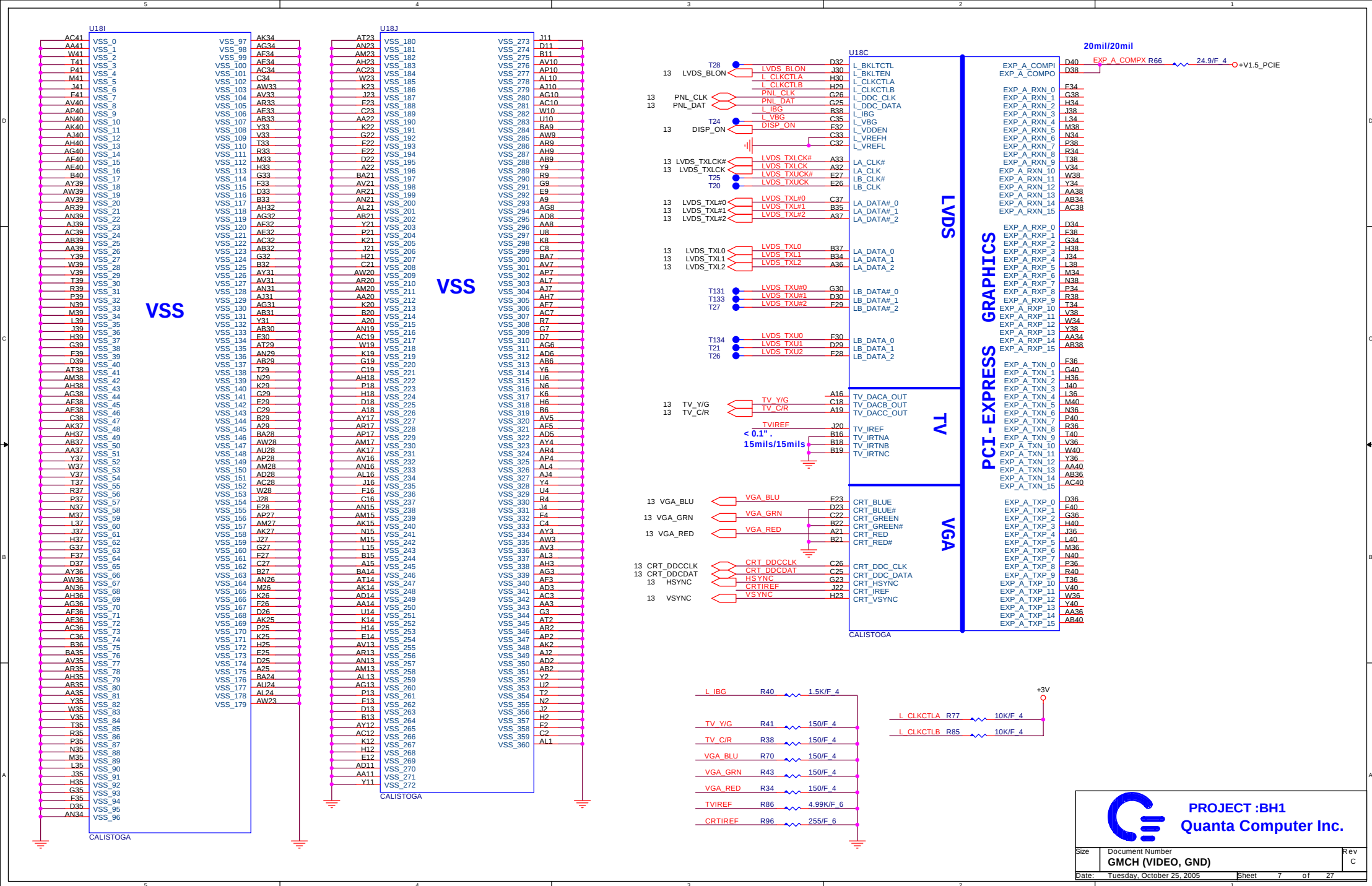
DDR SYSTEM MEMORY B

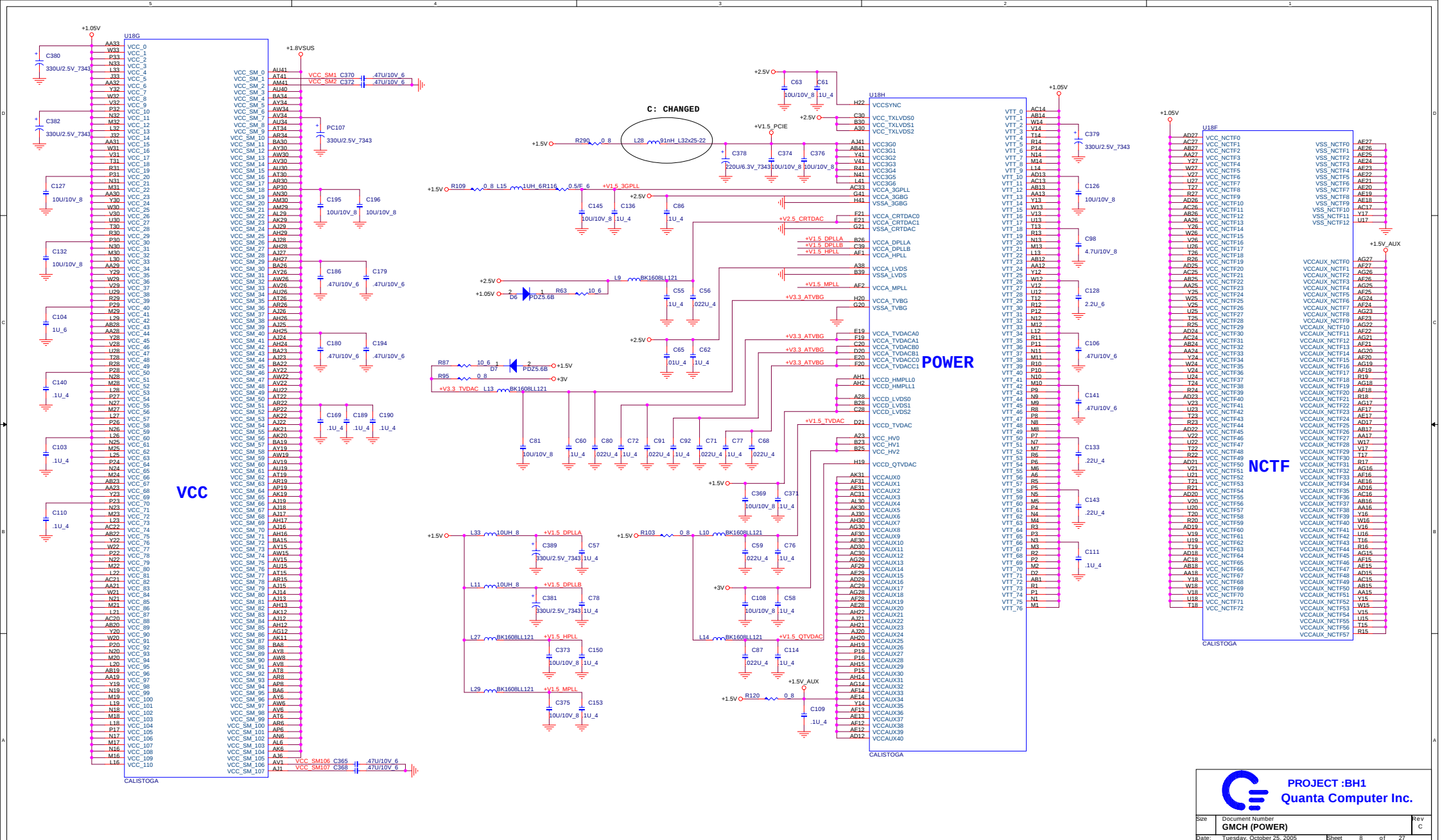
CALISTOGA

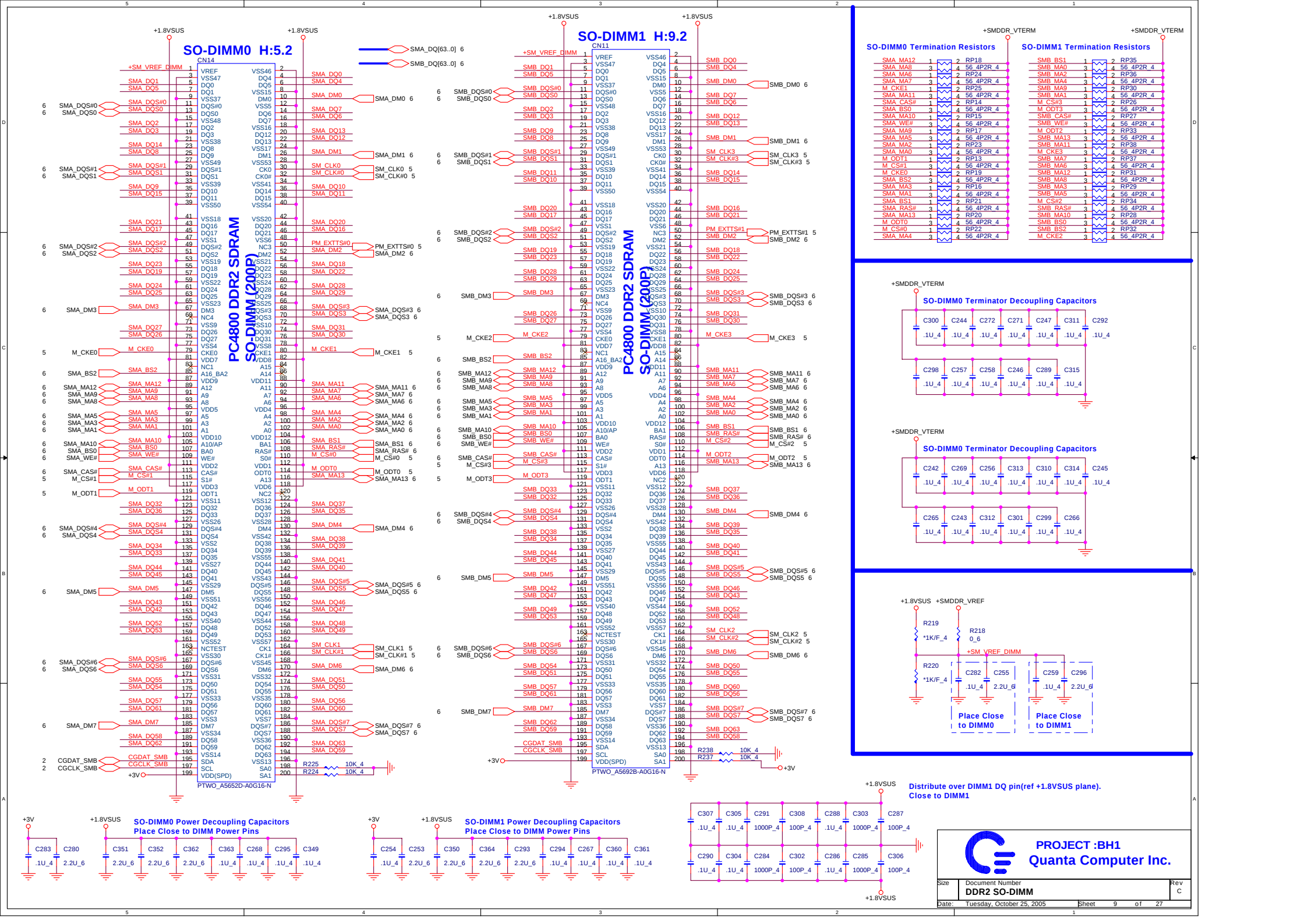


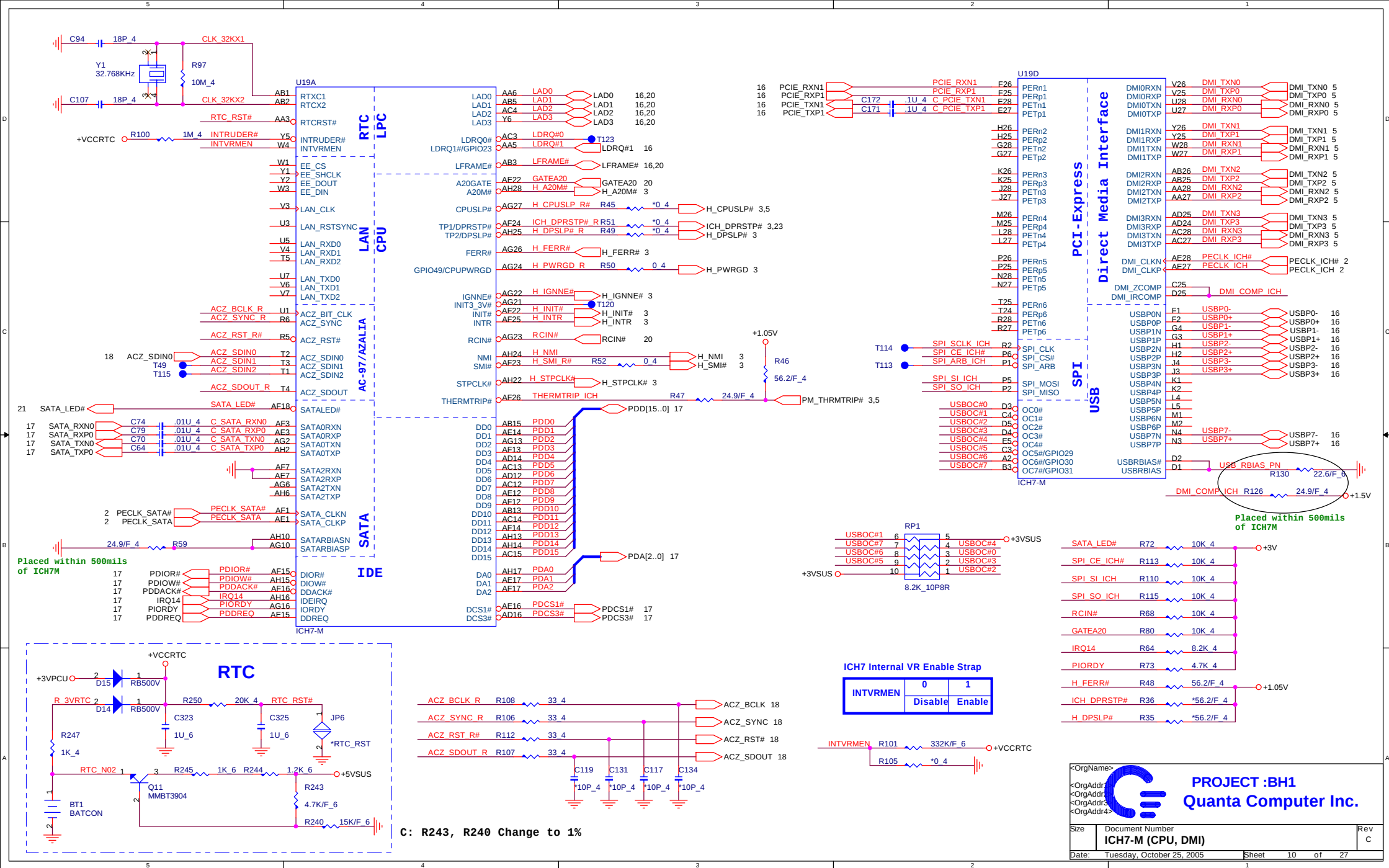
PROJECT :BH1
Quanta Computer Inc.

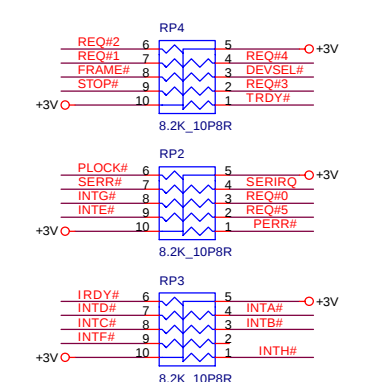
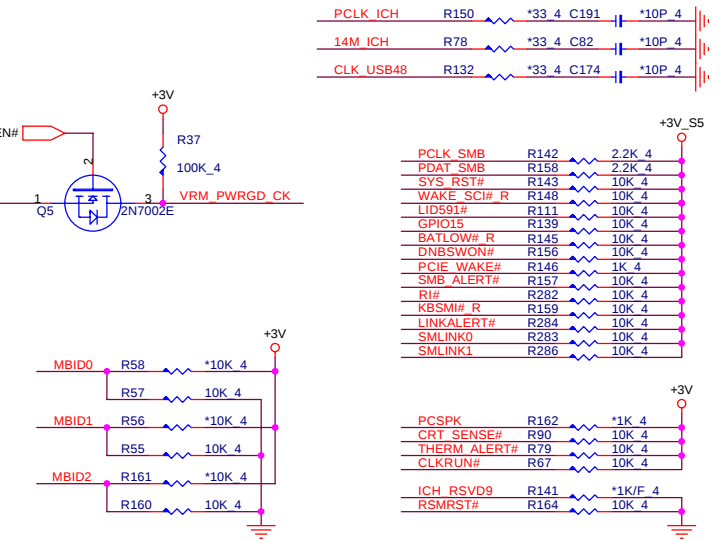
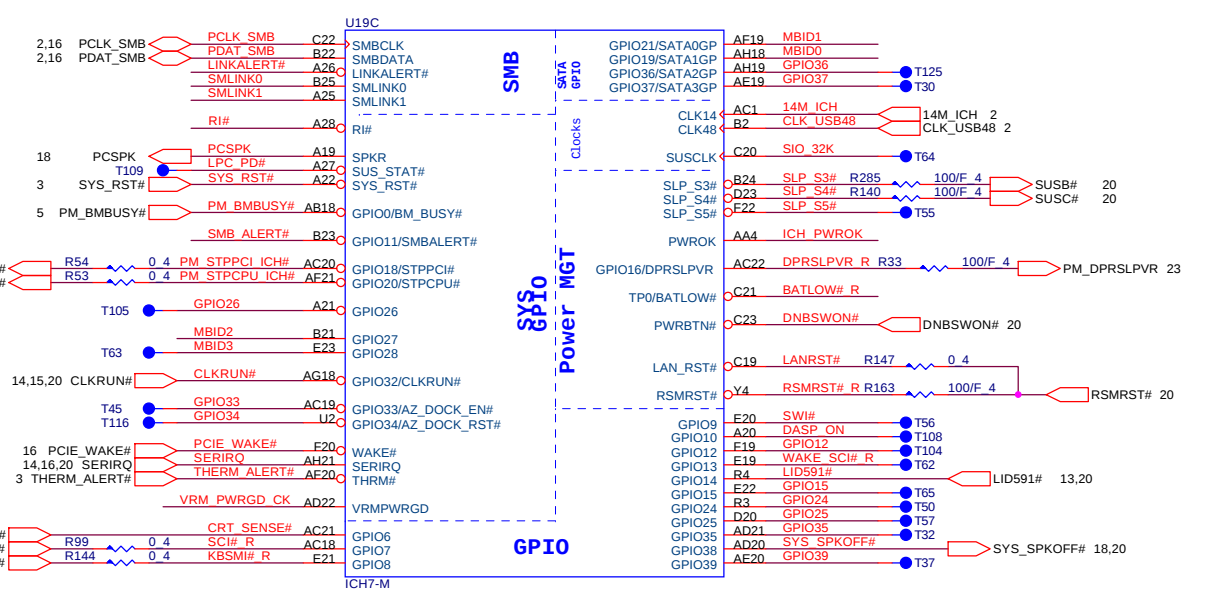
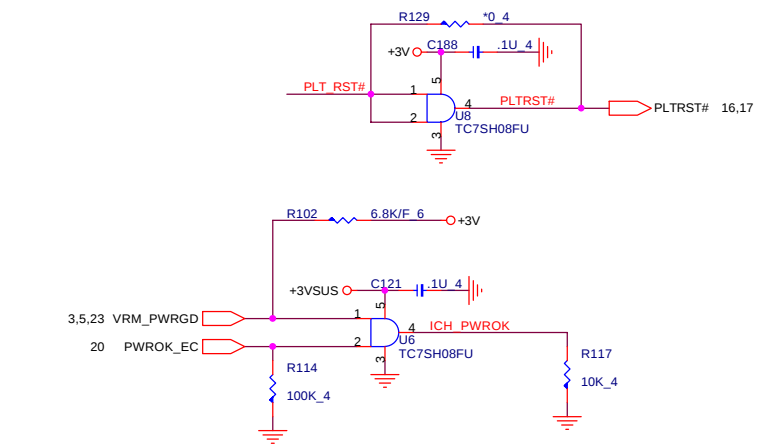
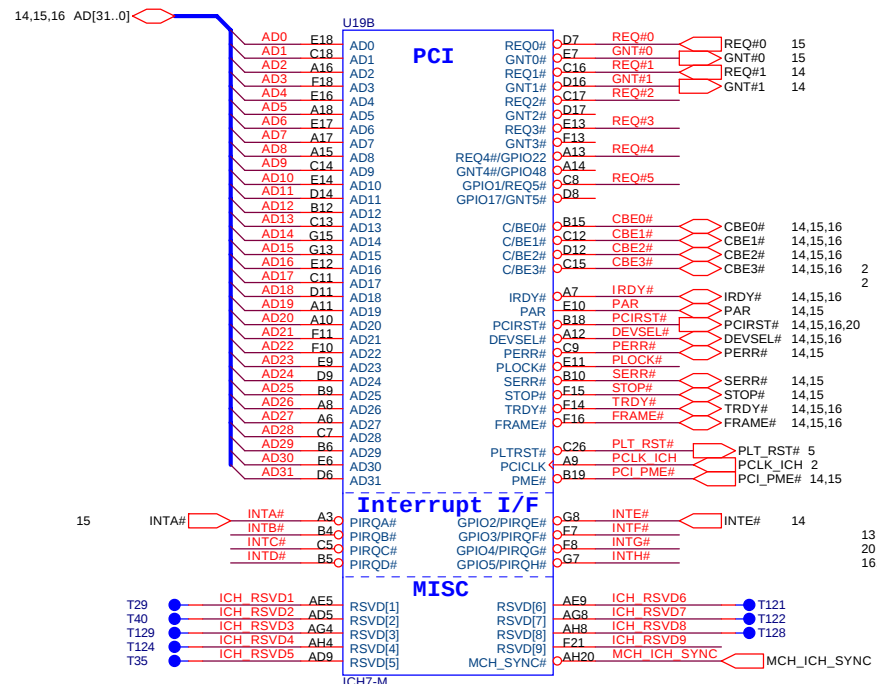
Size	Document Number	Rev
	GMCH (MEMORY)	C
Date:	Tuesday, October 25, 2005	Sheet 6 of 27







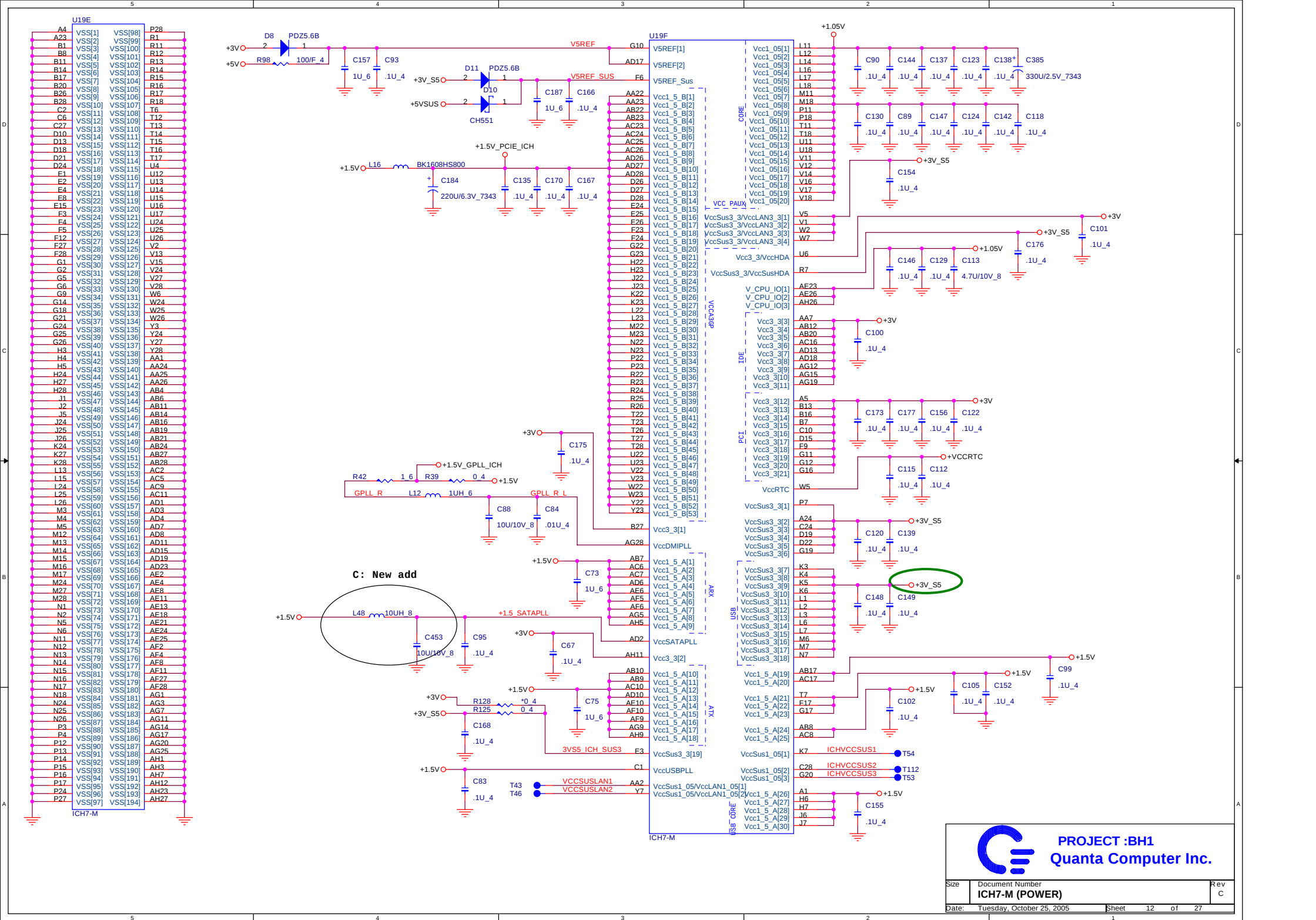




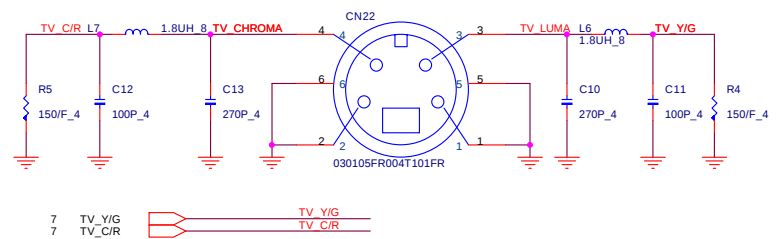
PROJECT :BH1

Quanta Computer Inc.

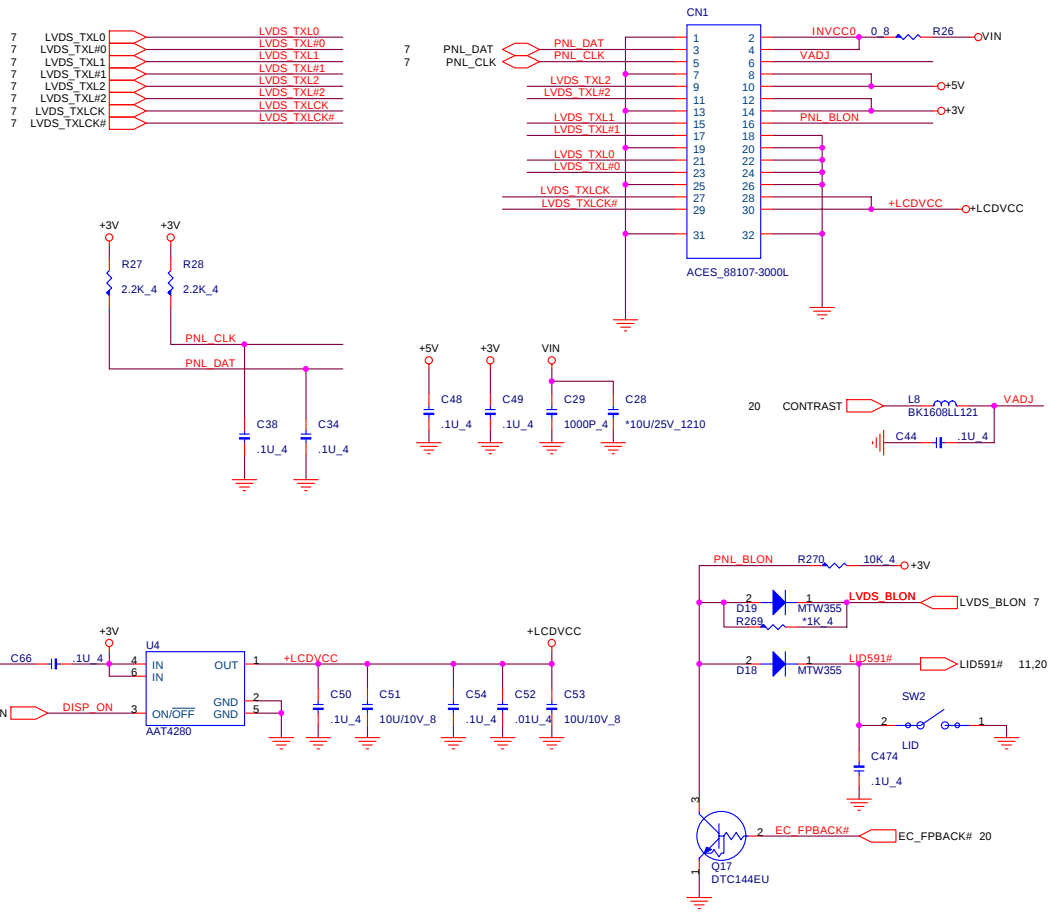
Size	Document Number	Rev
	ICH7-M (PCI, GPIO)	C
Date:	Tuesday, October 25, 2005	Sheet 11 of 27



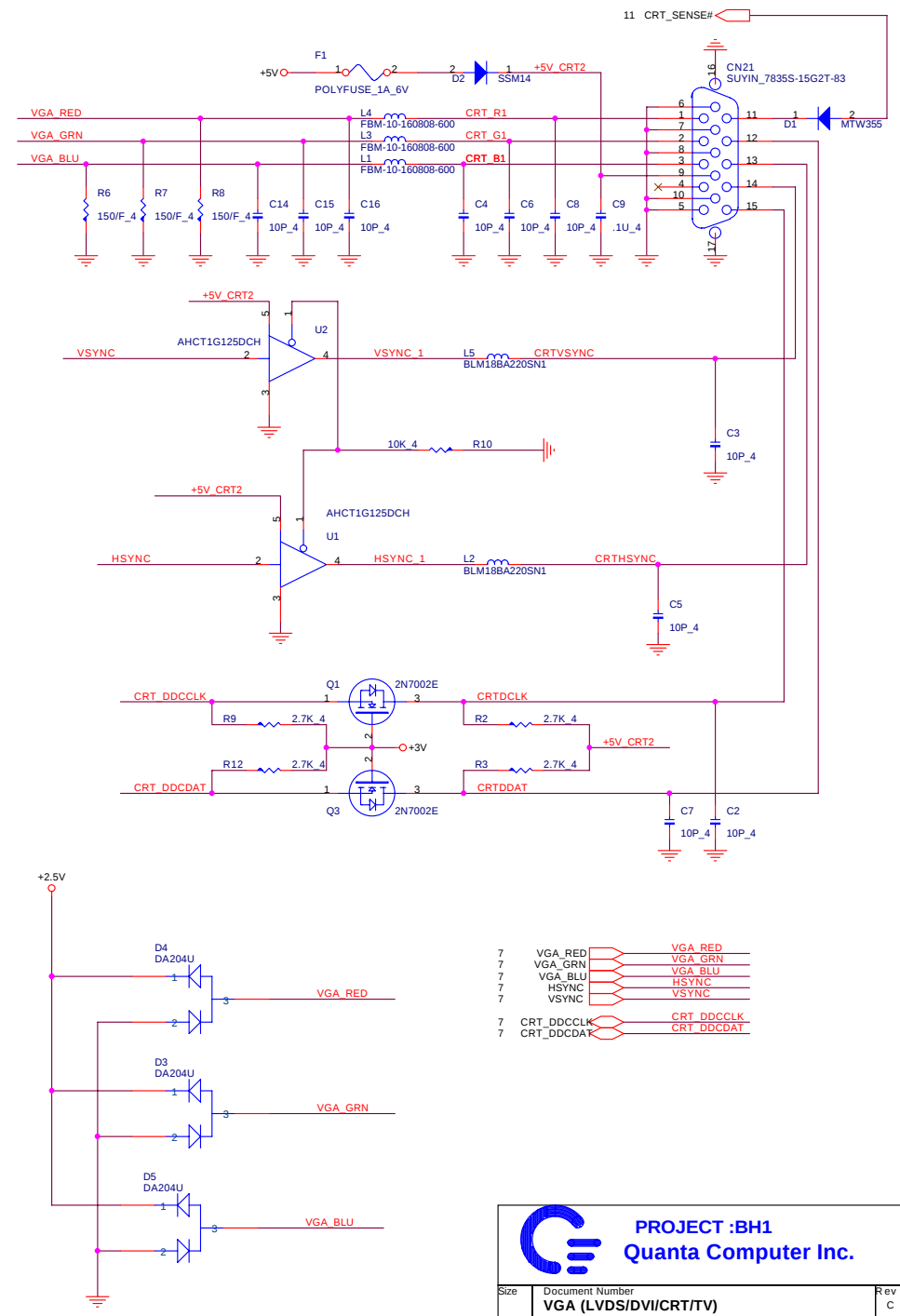
S-VIDEO



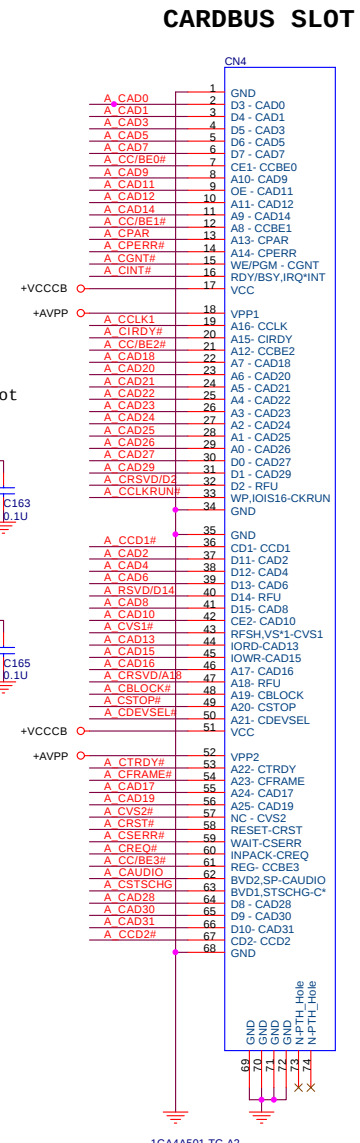
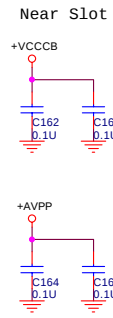
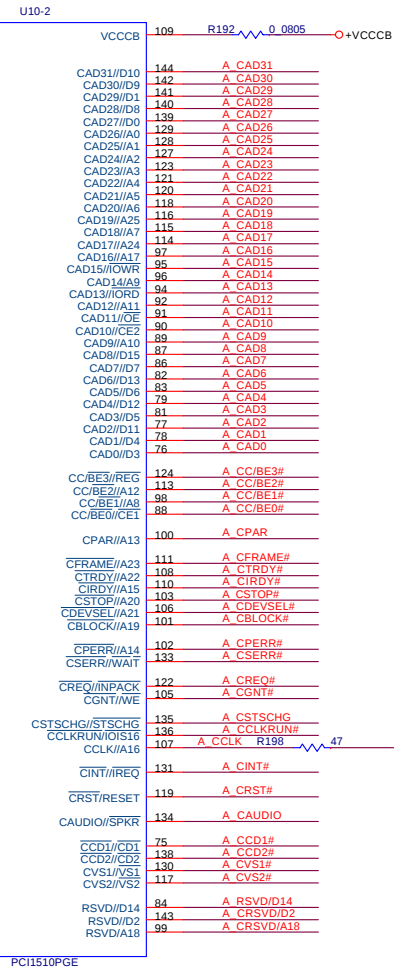
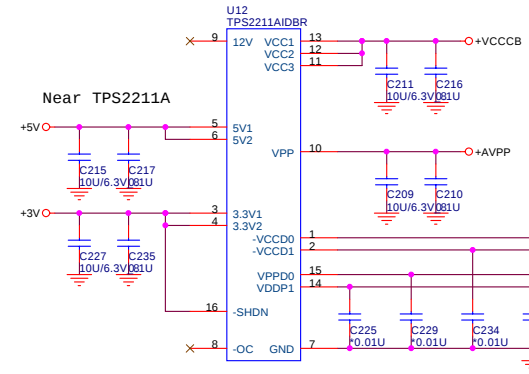
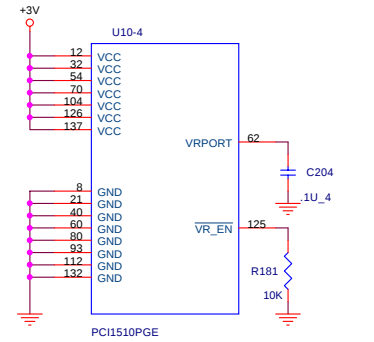
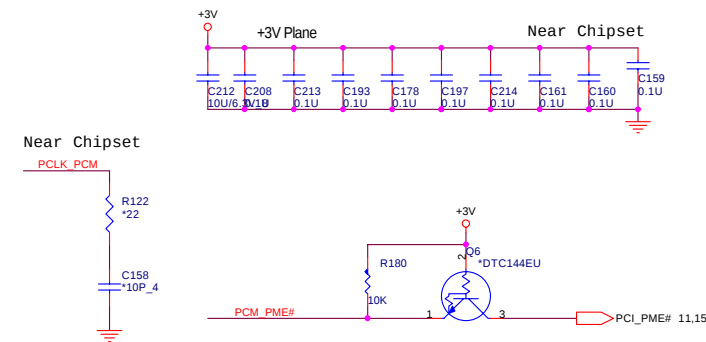
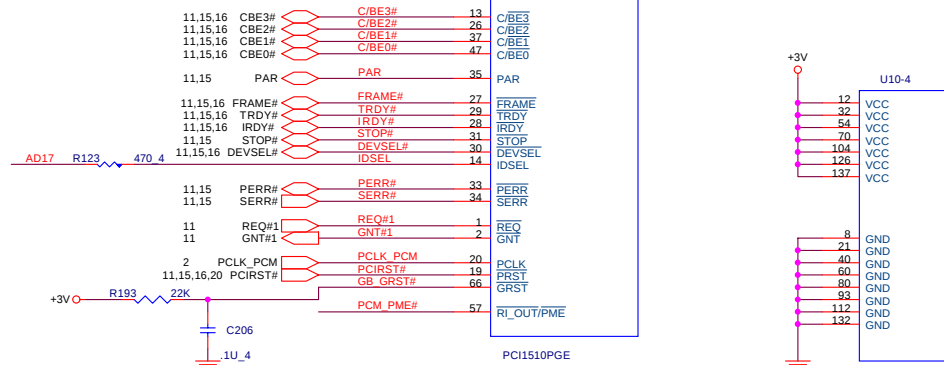
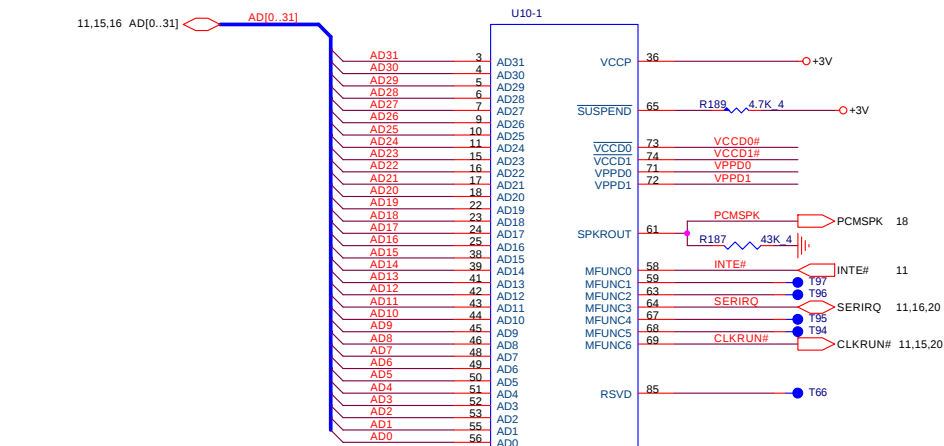
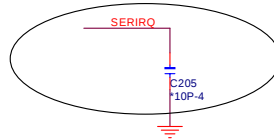
LVDS



CRT



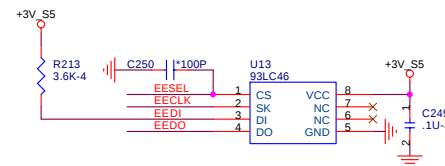
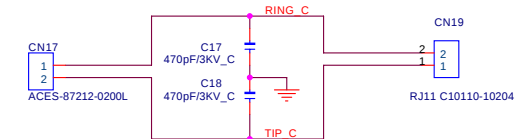
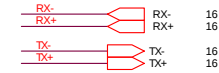
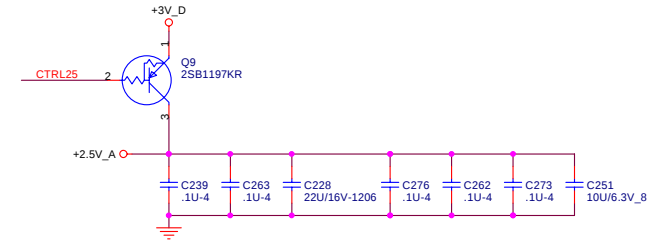
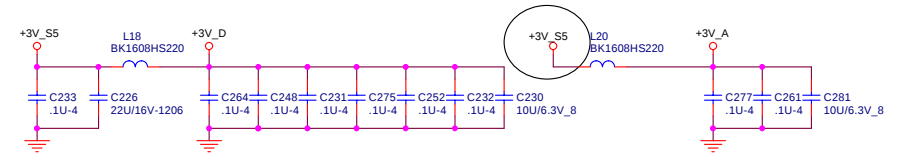
CBS



PROJECT :BH1
Quanta Computer Inc.

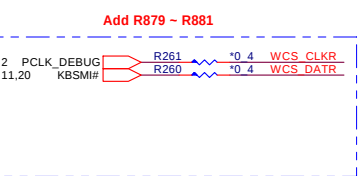
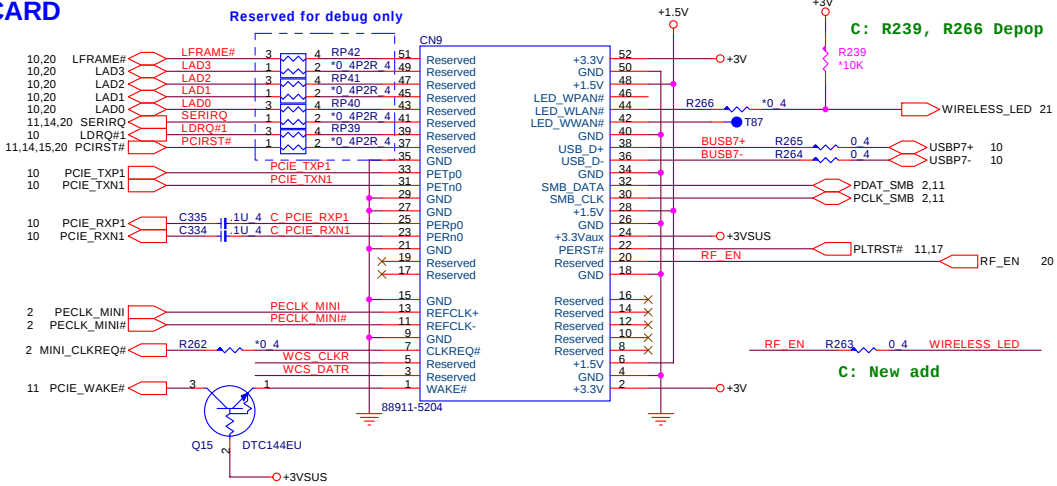
Size	Document Number PCI1510	Rev C
Date:	Tuesday, October 25, 2005	Sheet 14 of 27

LAN

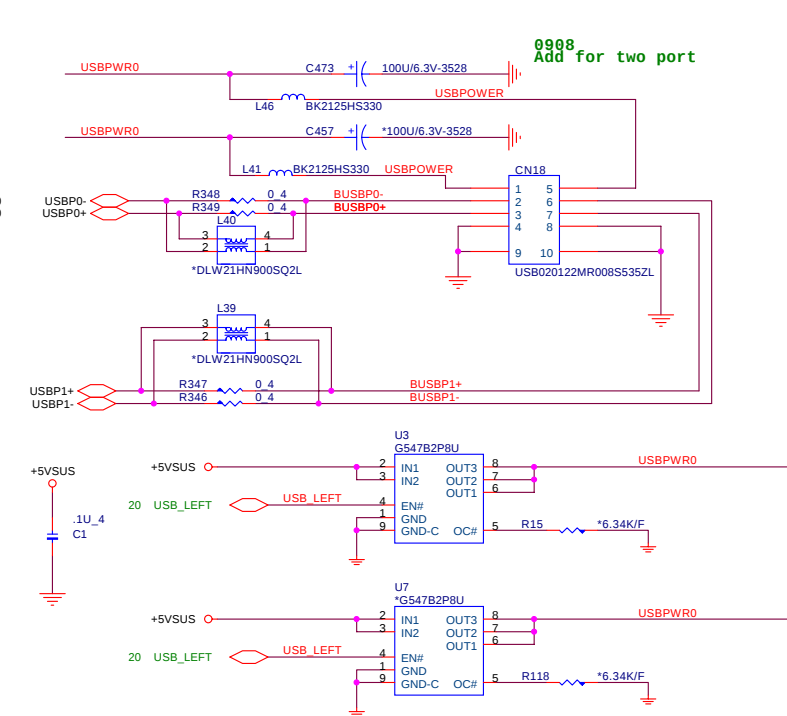


Size	Document Number LAN (RTL8100)	Rev C
Date:	Tuesday, October 25, 2005	Sheet 15 of 27

MINI CARD

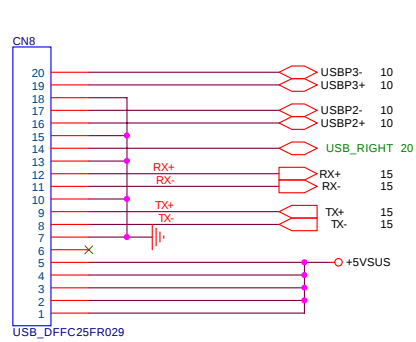


USB PORT x2



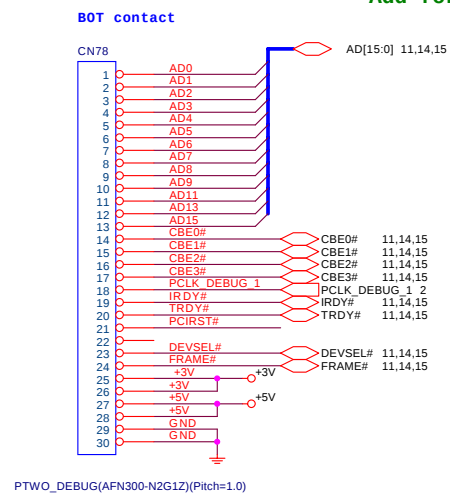
USB/LAN BOARD

1018 change to FPC type

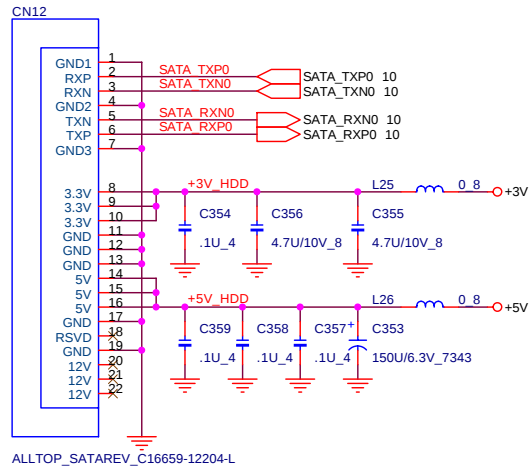


Debug card interface

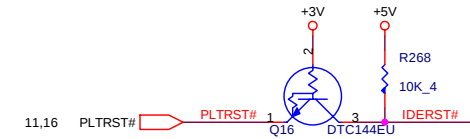
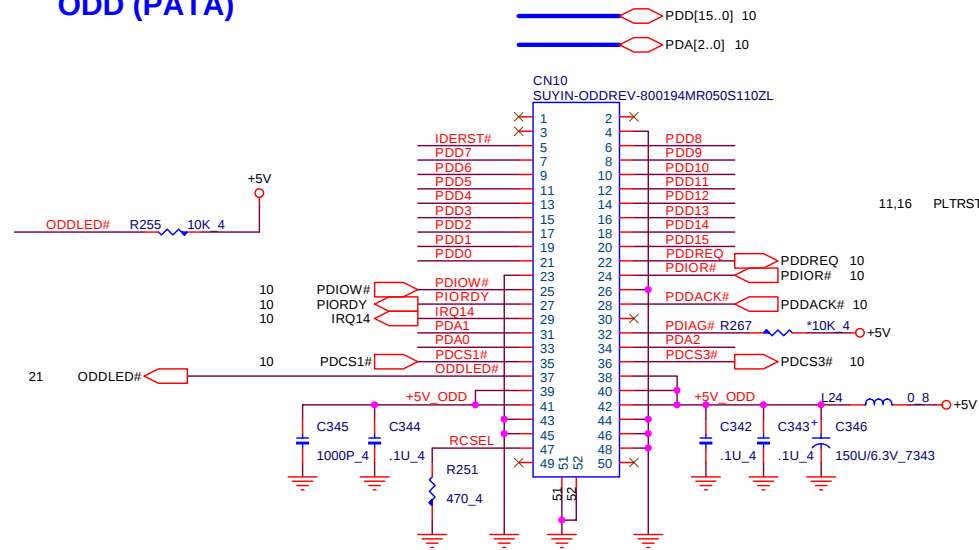
Add for debug 0907



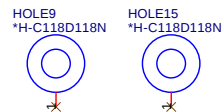
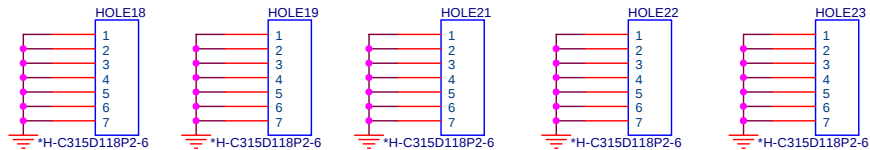
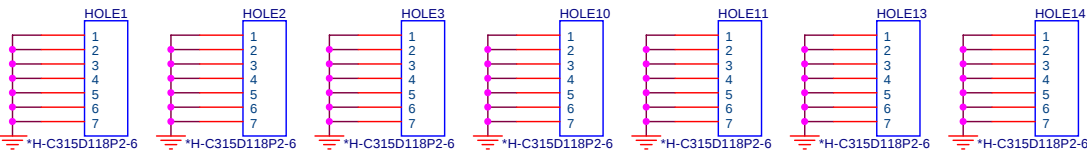
HDD (SATA)



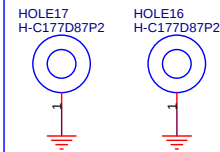
ODD (PATA)



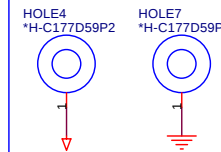
SCREW HOLE



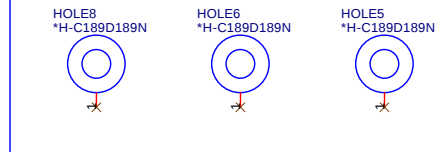
MINI CARD



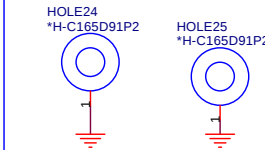
MODEM



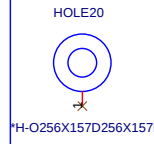
CPU



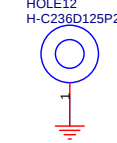
BATT



Wireless Antenna



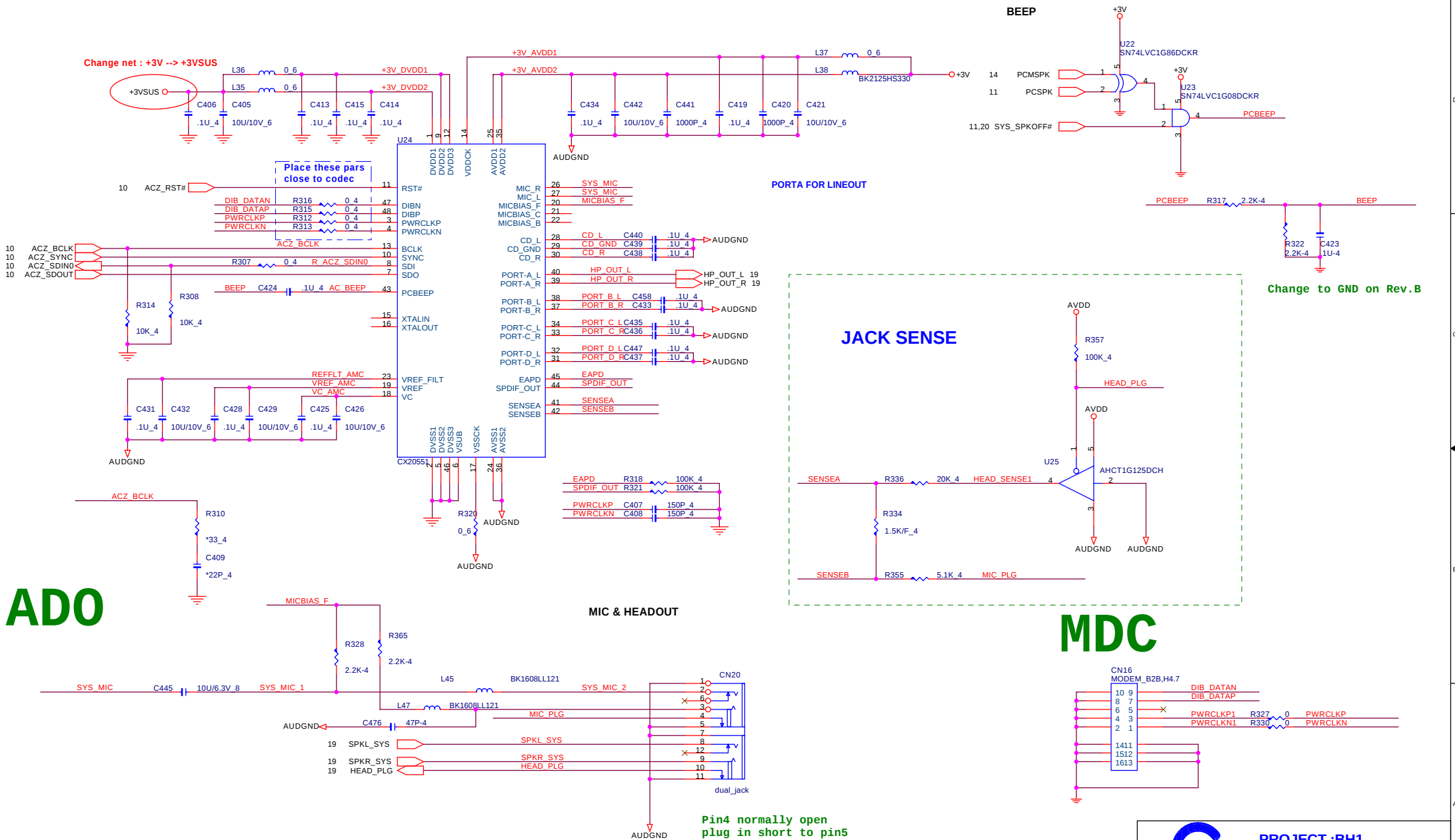
NB



PROJECT :BH1
Quanta Computer Inc.

Size	Document Number HDD/ODD/SCREW	Rev C
Date:	Tuesday, October 25, 2005	Sheet 17 of 27

ADO

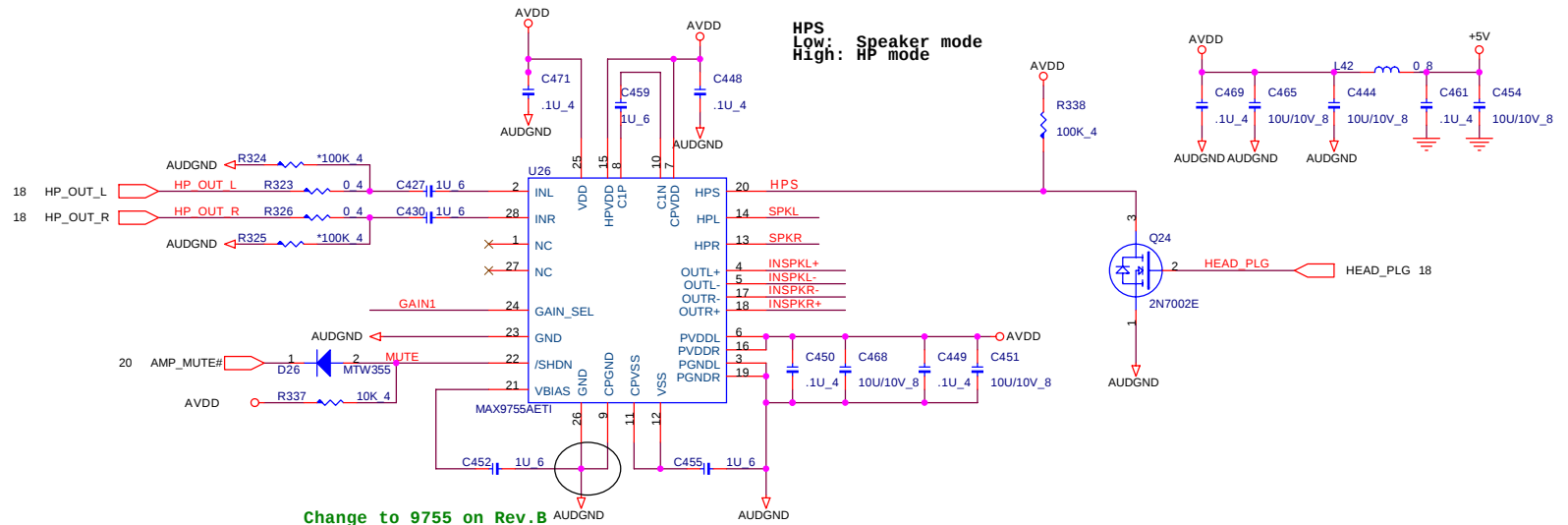


PROJECT :BH1
Quanta Computer Inc.

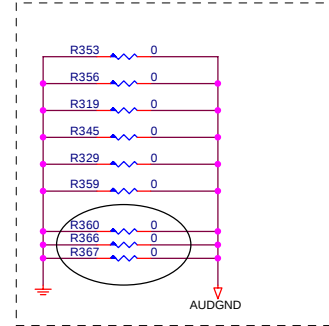
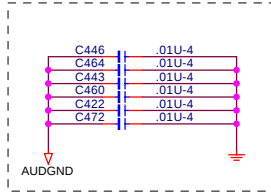
Size	Document Number	Rev
	AUDIO (CODEC/AMP)	C

Date: Tuesday, October 25, 2005 Sheet 18 of 27

GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0

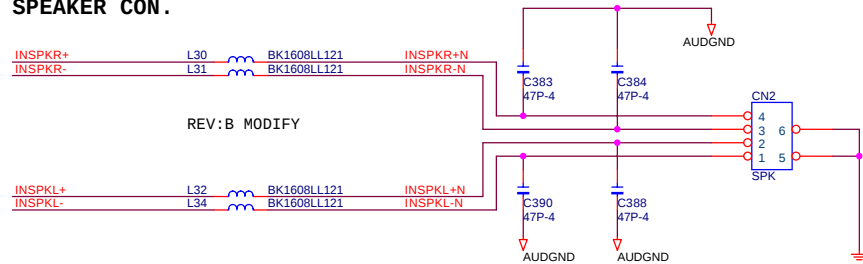


Change to 9755 on Rev.B

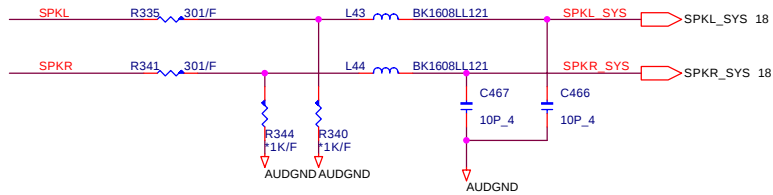


B: add on connector side

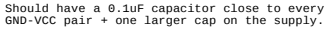
SPEAKER CON.



REV:B MODIFY



PROJECT :BH1
Quanta Computer Inc.



I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL, HCFGGBAH, HCFGGBAL)+1	
1 1	Reserved	

```
4.25 SHBM=1: Enable shared memory with host BIOS
```

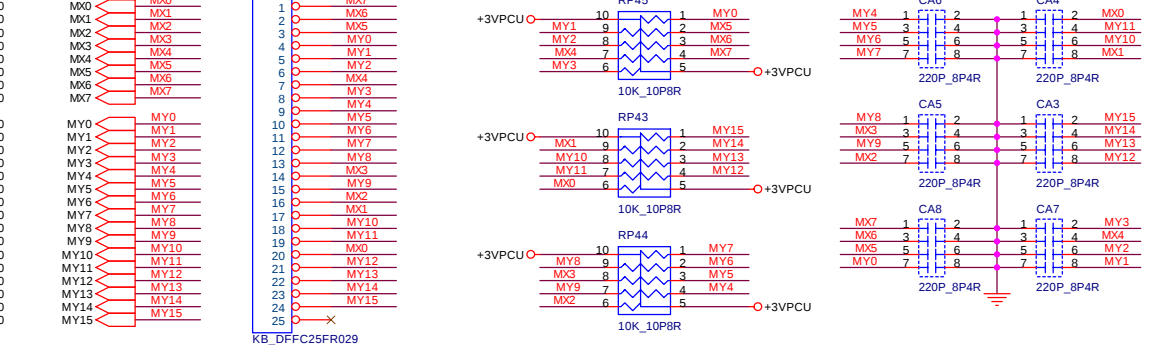
MBCLK R248 4.7K-4

MBDATA R249 4.7K-4

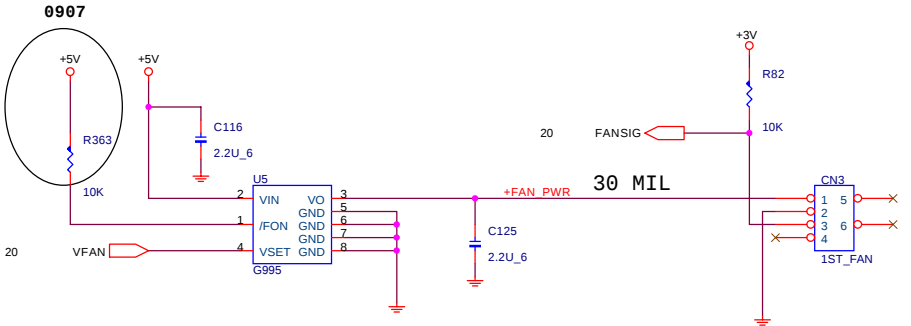
WIRELESS_SW# R253 4.7K-4

BIU configuration should match flash speed used

INT K/B

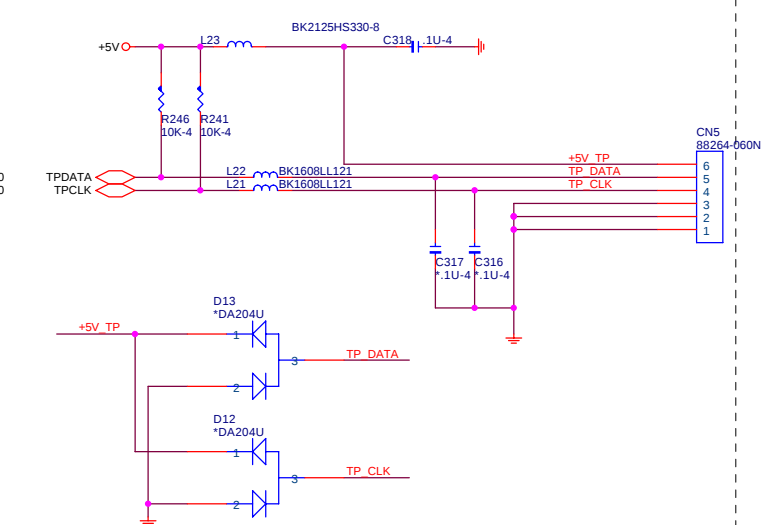


FAN CONTROL

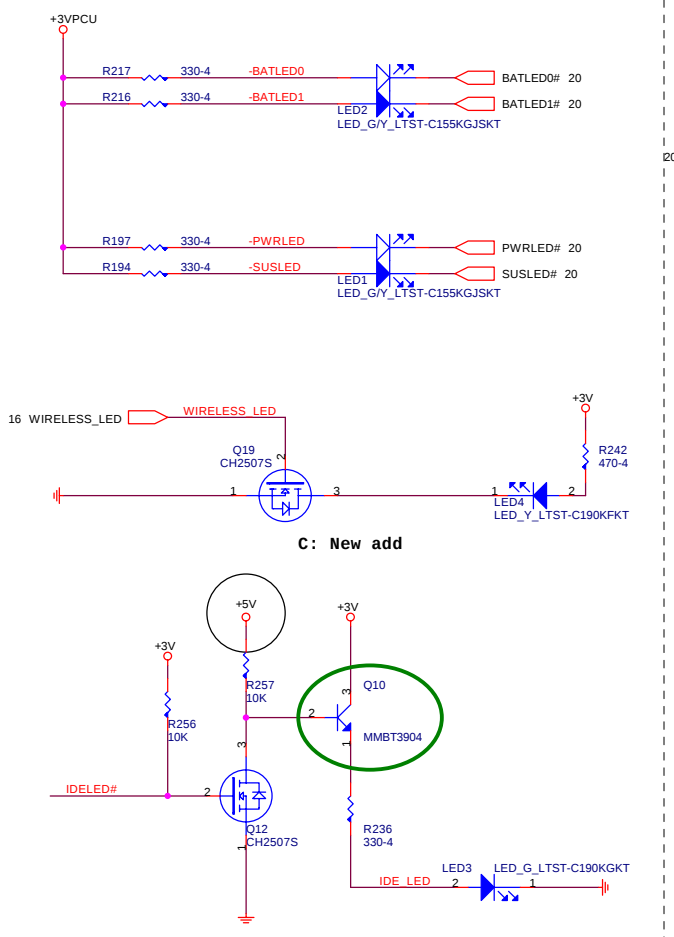


TP

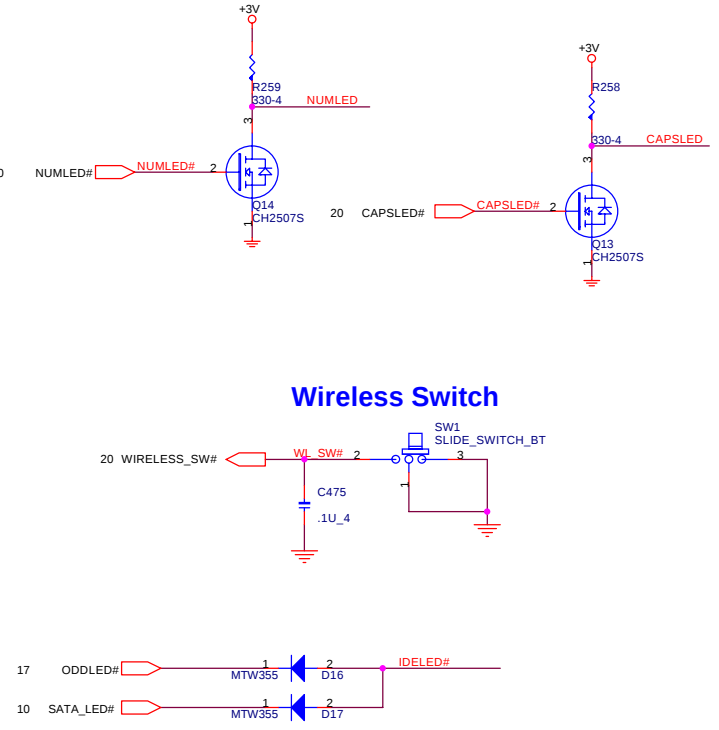
20 MIL



LED



Wireless Switch



LED BD

