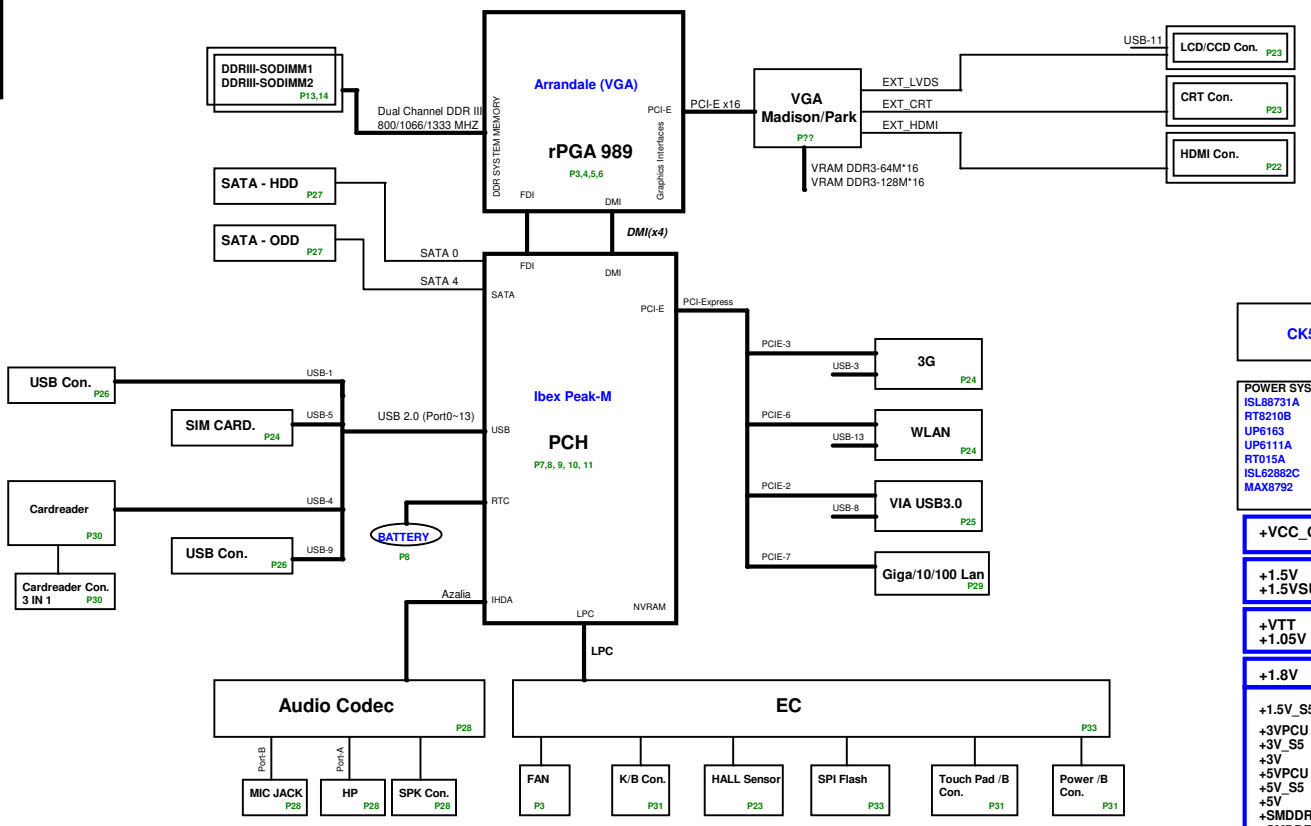
PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND1
- LAYER 3 : IN1
- LAYER 4 : VCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND2
- LAYER 8 : BOT

BU5D Block Diagram



CK505
P2

POWER SYSTEM

ISL88731A	P33
RT8210B	P34
UP6163	P35
UP6111A	P36
RT015A	P37
ISL62882C	P38
MAX8792	P40

+VCC_CORE

+1.5V
+1.5VSUS

+VTT
+1.05V

+1.8V

+1.5V_S5

+3VPCU
+3V_S5
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF

Quanta Computer Inc.
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Block Diagram
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Table of Contents

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
+5V_TMA	+5V	MAIN_ON	S0
WIMAX_P	+3.3V	WMAX_P for EC	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_S5	+1.5V	S5_ON	S0~S5
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V~+1.1V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		GFXVR_EN	S0

GND PLANE	PAGE
GND_SIGNAL	32
CARD_GND	21
AGND_DC/DC	31
GND	ALL

ITEM	Value Code	FUNCTIONS
1	EV@	DISCRETE
2	IV@	UMA
3	U3@	USB 3.0
4	U2@	USB 2.0 (colay W USB 3.0)
5	HM@	HDMI
6	NHM@	No HDMI
7	EHM@	External HDMI
8	3G@	3G
9	C@	Cost issue
10	MDC@	Modem
11	S3@	S3 Power Reduction
12	NS3@	No S3 Power Reduction
13	NGS@	No G-SENSOR
14	51@	1G LAN
15	52@	10/100 LAN
16	GS@	G-SENSOR
17	NMDC@	No Modem

Quanta Computer Inc.

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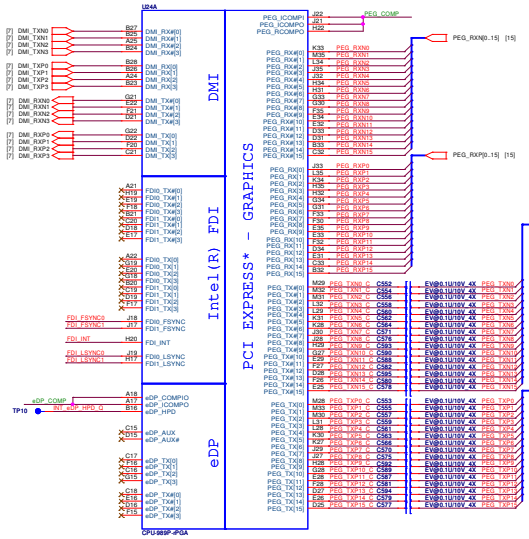
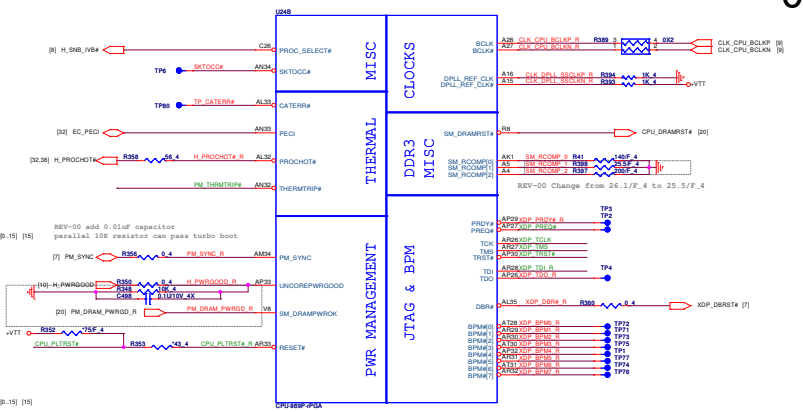
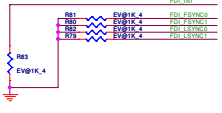
Sandy Bridge Processor (DMI,PEG,FDI)



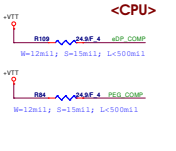
Sandy Bridge Processor (CLK,MISC,JTAG)



FDI Disabling (Discrete Only) <VGA>

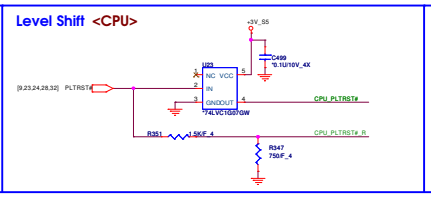


DP & PEG Compensation <CPU>

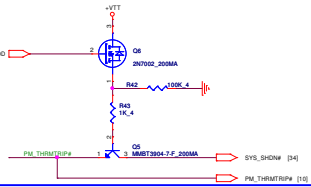


Processor pull-up <CPU>

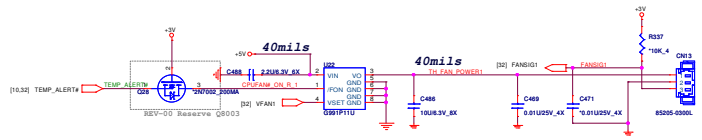
Level Shift <CPU>



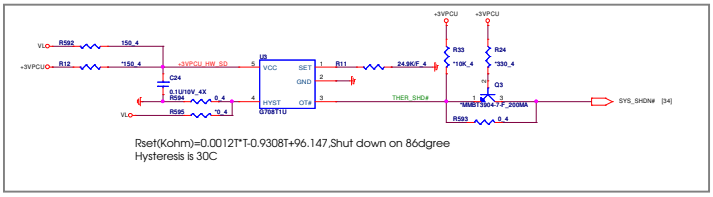
Thermal Trip<CPU>



FAN Control-->For one FAN solution <THC>



CPU Thermal sensor / MB Local TEMP <THC>



REV-C3A Change VCC PIN5 of U3 from +3VPCU to VL
Add R592,R594,R593
Reverse R12,R595,R33,R24,Q3

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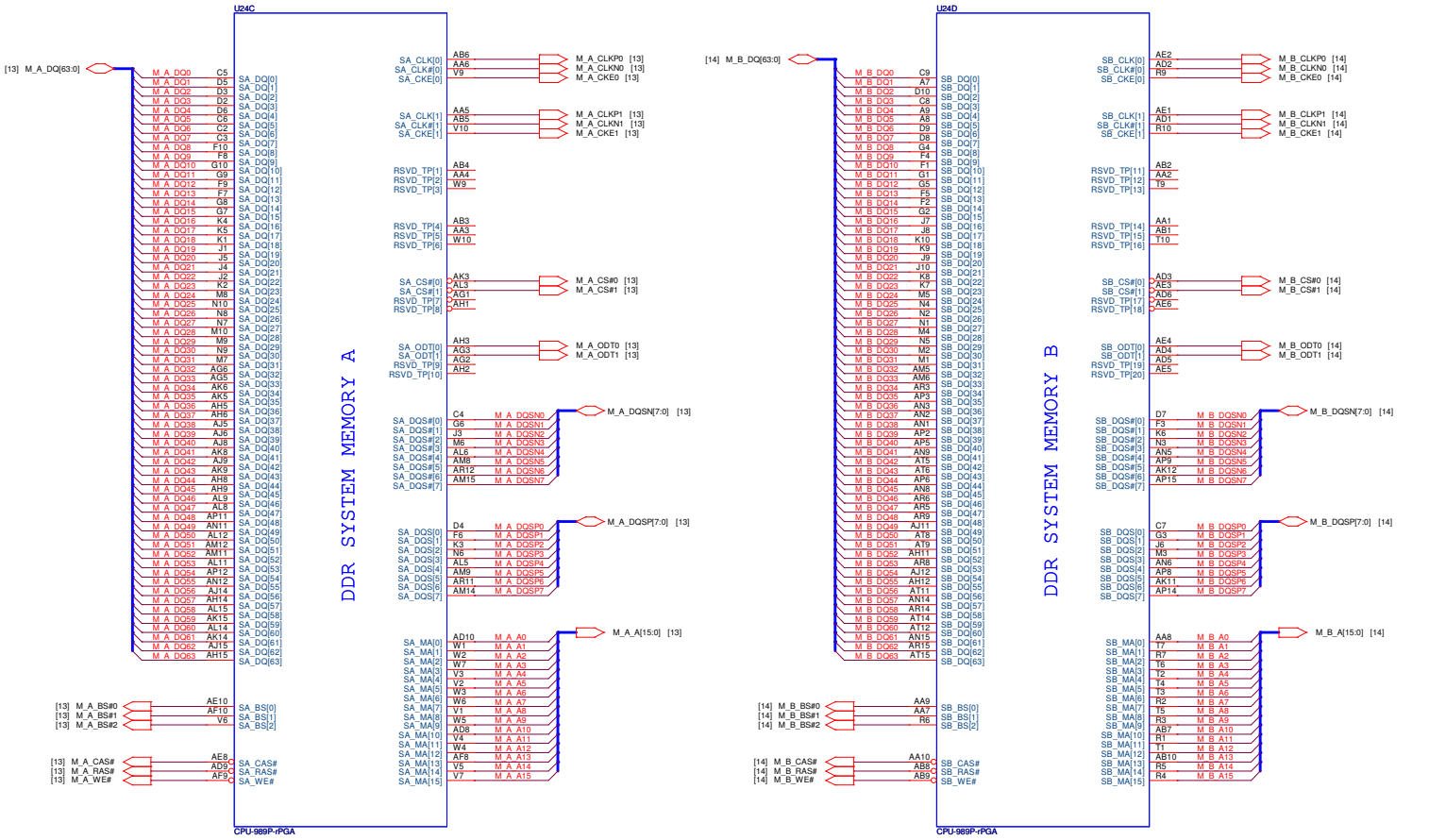
Sandy Bridge Processor (DDR3)



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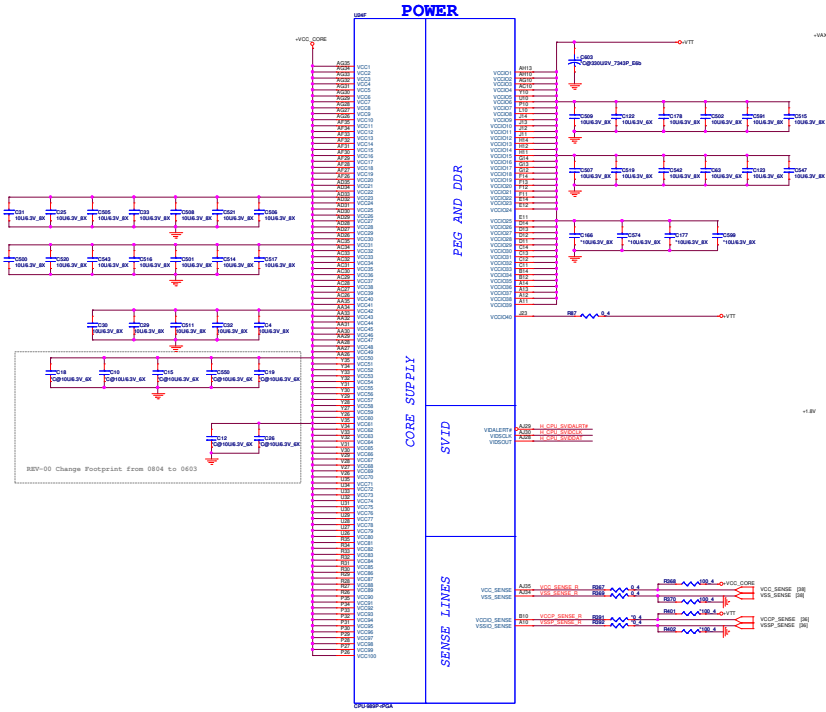
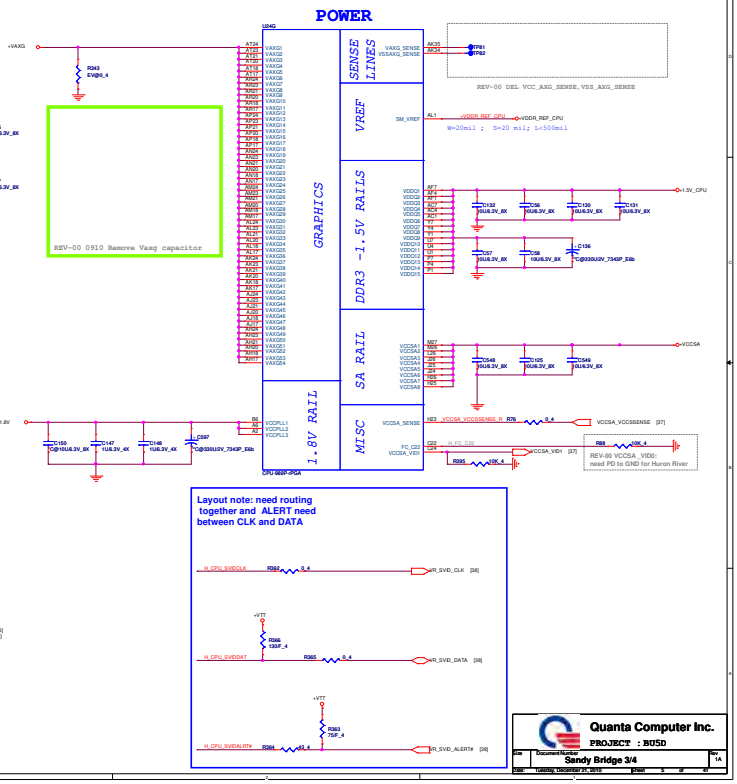
Sandy Bridge Processor (POWER)



Sandy Bridge Processor (GRAPHIC POWER)



Layout note: need routing together and ALERT need between CLK and DATA

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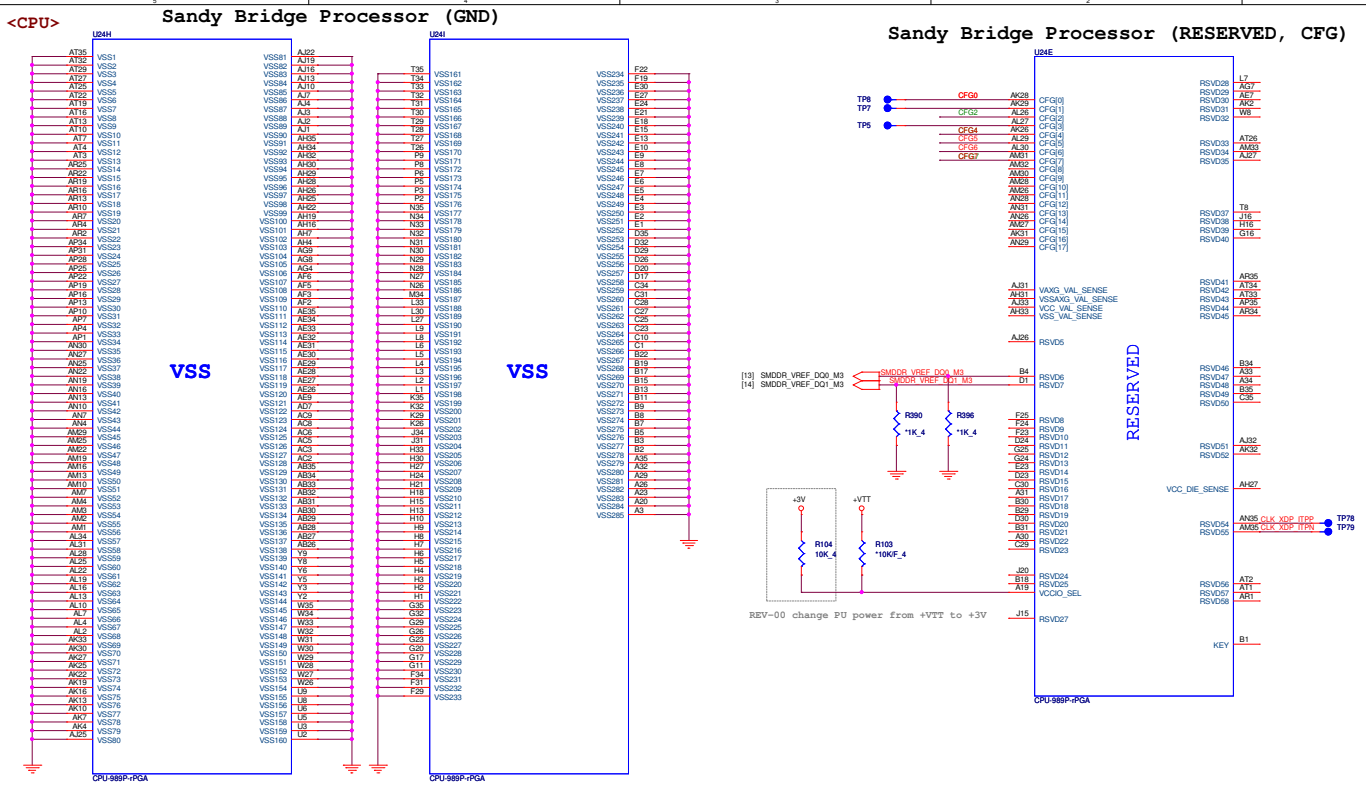
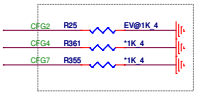


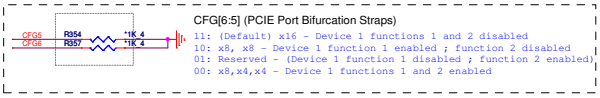
Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



REV-00 change to 5% tolerance



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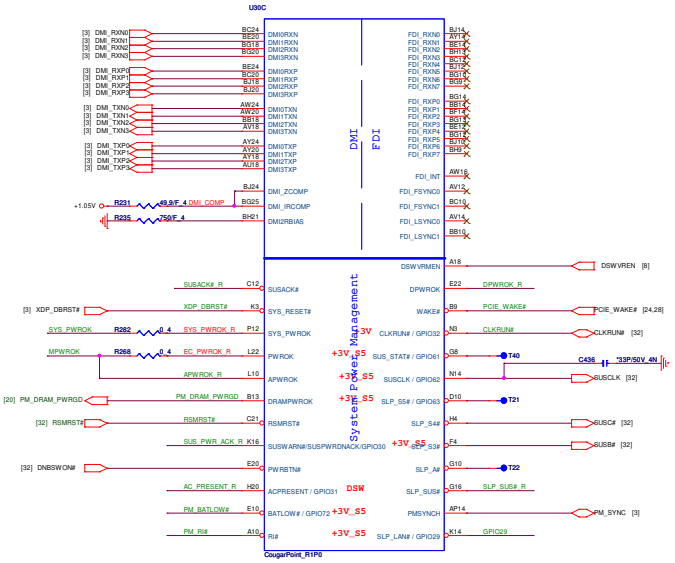
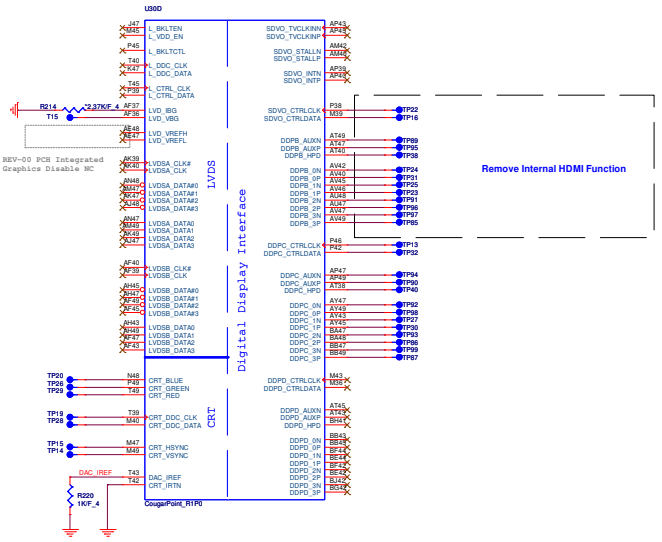
<CLG>

07

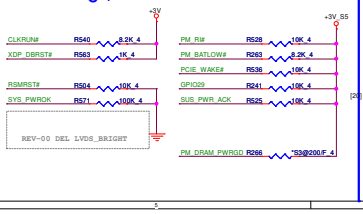
Cougar Point (DMI,FDI,PM)



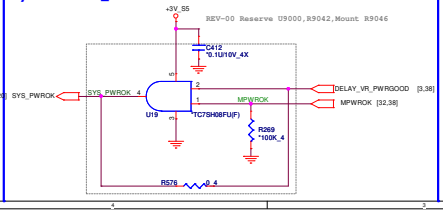
Cougar Point (LVDS,DDI)



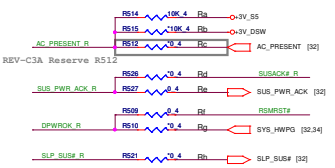
PCH Pull-high/low <CLG>



System PWR_OK <CLG>



Deep Sx <CLG>



Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

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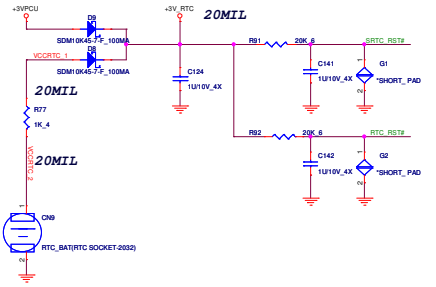
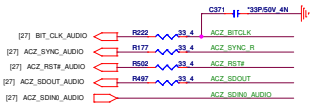
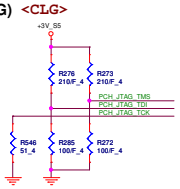
RTC Circuitry(RTC) <RTC>



HDA Bus(CLG) <ADO>

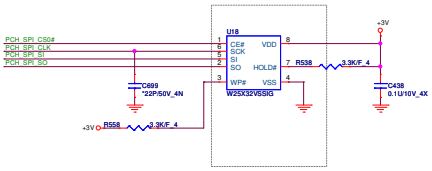


PCH JTAG Debug (CLG) <CLG>



PCH Dual SPI (CLG) <CLG>

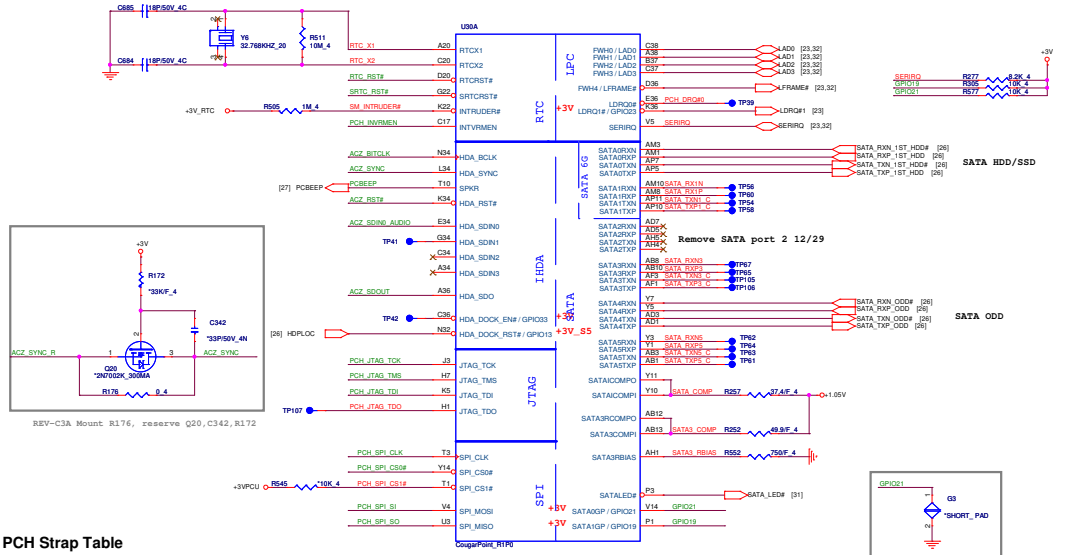
MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE339ZP0N00



REV-00 change footprint
from socket type to W25X32VSSIG

PCH2 (CLG) <CLG> <ADO>

Cougar Point (HDA,JTAG,SATA)



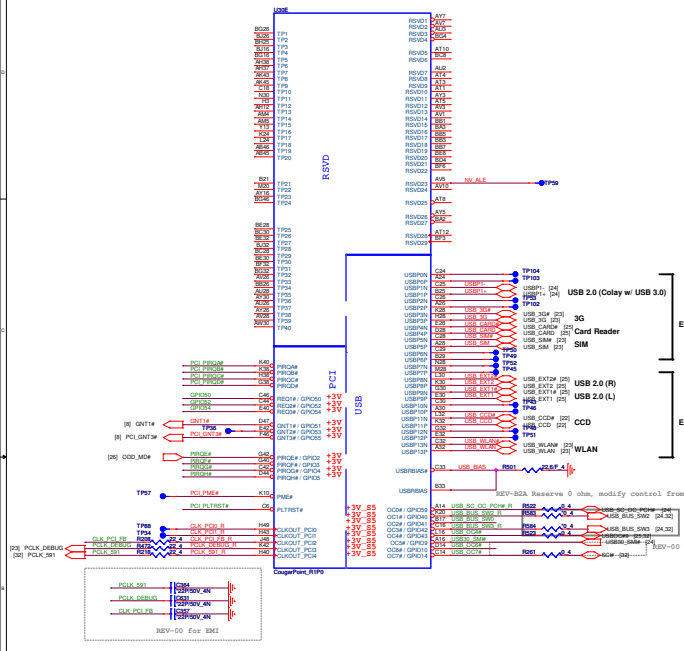
REV-C3A Mount R176, reserve Q20,C342,R172

REV-B2A Add G3 for Clear CMOS password

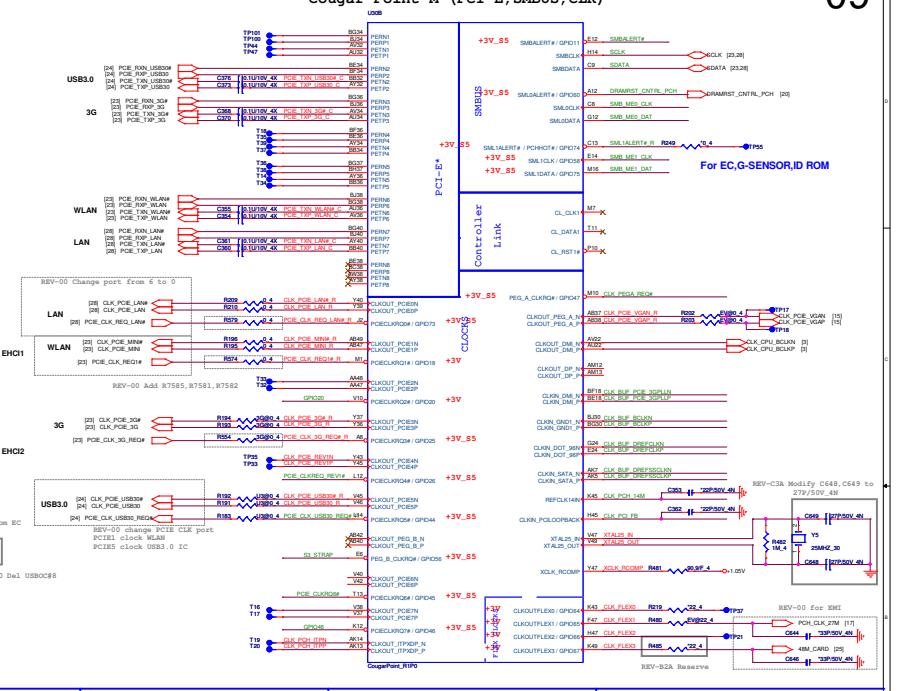
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R281 *1K_4 PCBEEP
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R483 *1K_4 PCI_GNT3# [9]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R513 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GPIO19 / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC	R479 *1K_4 GNT1# [9] R560 *1K_4 GPIO19
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V R498 *1K_4 ACZ_SDOUT ACZ_SDOUT [32]
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R543 2.2K_4 R544 2.7K_4 1.8V DF_TVS [10] H_SNB_IVB# [3]
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	+3VPCU R265 *10K_4 R271 *1K_4 PLL_ODVR_EN [10]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R179 1K_4 ACZ_SYNC
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality	+3V_S5 R542 1K_4 GPIO15 [10]
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	DSWVRMEN [7] +3V_RTC R518 330K_4 R517 *330K_4
INIT3_3V#	Reserved	PWROK	1 = Default (weak pull-up 20K)	Should not pull low. leave as No Connect
GNT2#/ GPIO53	ESI Strap (Server Only)	PWROK	1 = Default. Should not be pulled low for desktop and mobile	Should not pull low for desktop and mobile
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
SATA3GP/ GPIO37	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled
SATA2GP/ GPIO36	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled

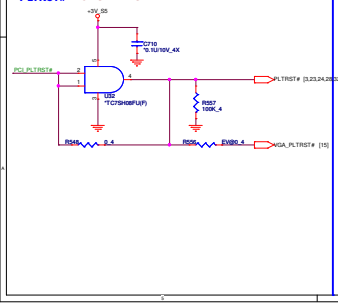
Cougar Point-M (PCI,USB,NVRAM)



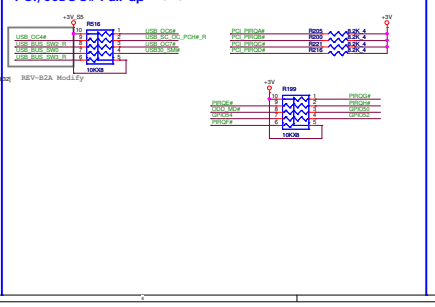
Cougar Point-M (PCI-E,SMBUS,CLK)



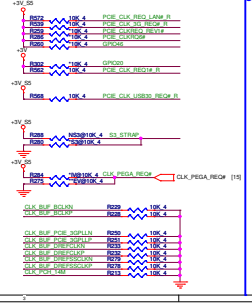
<CLG> <VGA>



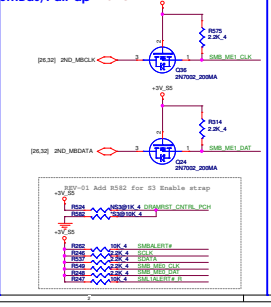
PCI/USBOC# Pull-up <CLG>



CLK_REQ/Strap Pin <CLG>



SMBus/Pull-up <CLG>



	33MHz	27MHz	48/24MHz	14.318MHz	25MHz
CLK_FLEX0	●	●	●	●	
CLK_FLEX1		●	●	●	
CLK_FLEX2	●	●	●	●	●
CLK_FLEX3		●	●	●	

Quanta Computer Inc.

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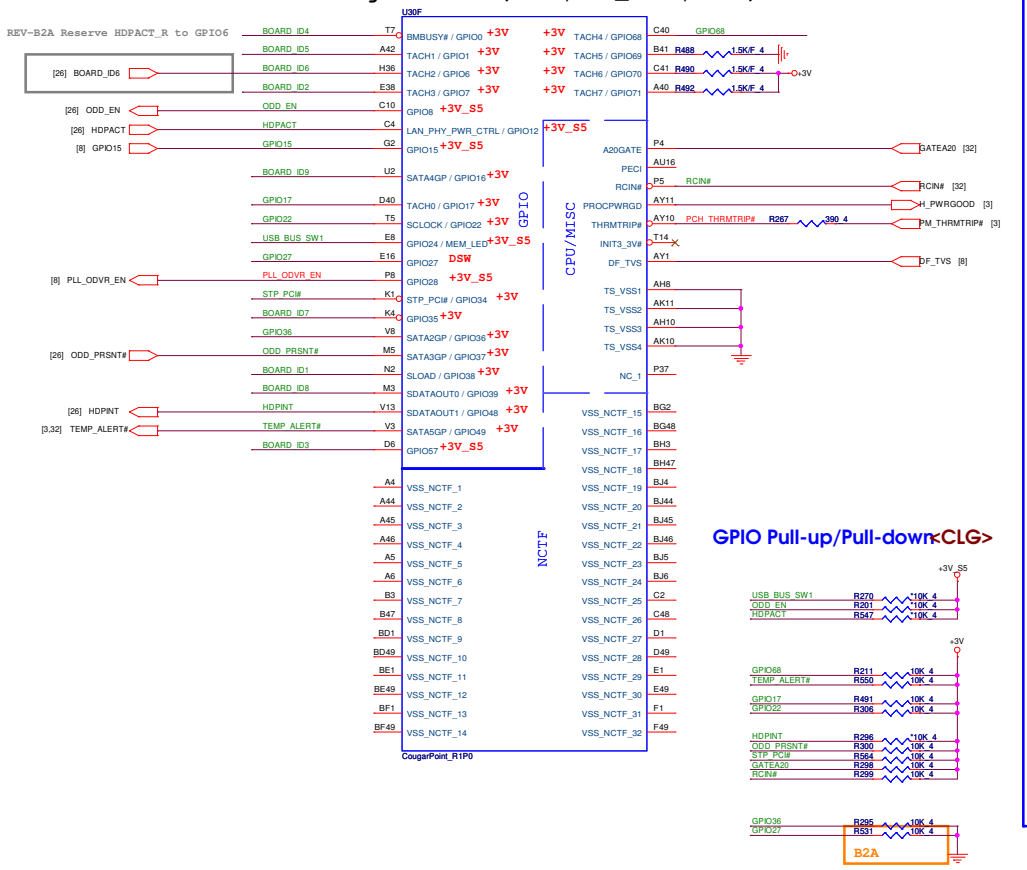
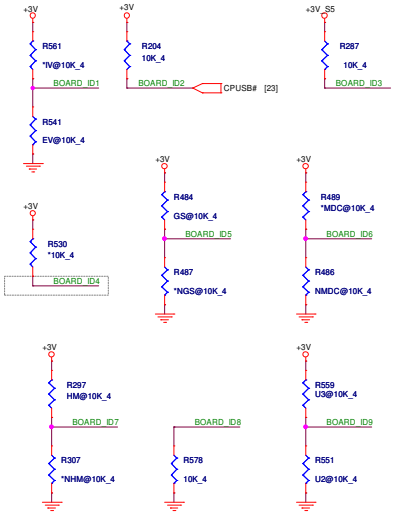
Cougar Point (GPIO,VSS_NCTF,RSVD)



GPIO Pull-up/Pull-down<CLG>

BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9
UMA SKU VGA SKU	H L								
W/O 3G W/ 3G		H L							
W/O LED_KB W/ LED_KB			H L						
14" 15"				H L					
W G-SNR W/O G-SNR					H L				
W/ MDC W/O MDC						H L			
W/ HDMI W/O HDMI							H L		
NC 13"								H L	
W/ USB3.0 W/O USB3.0									H L



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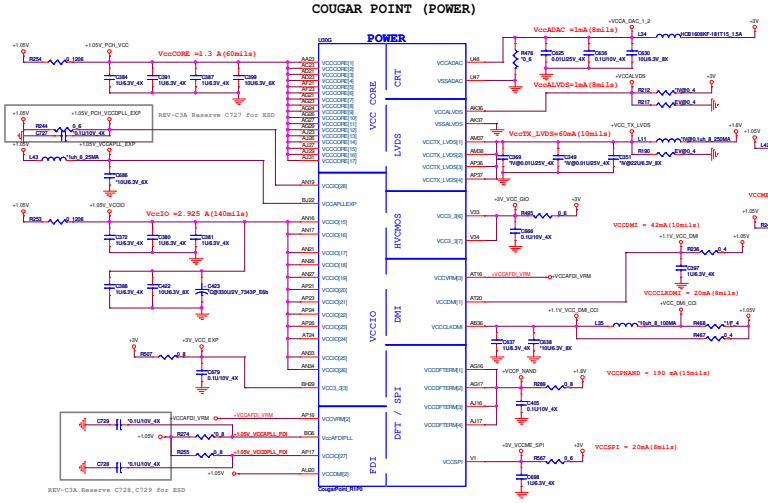
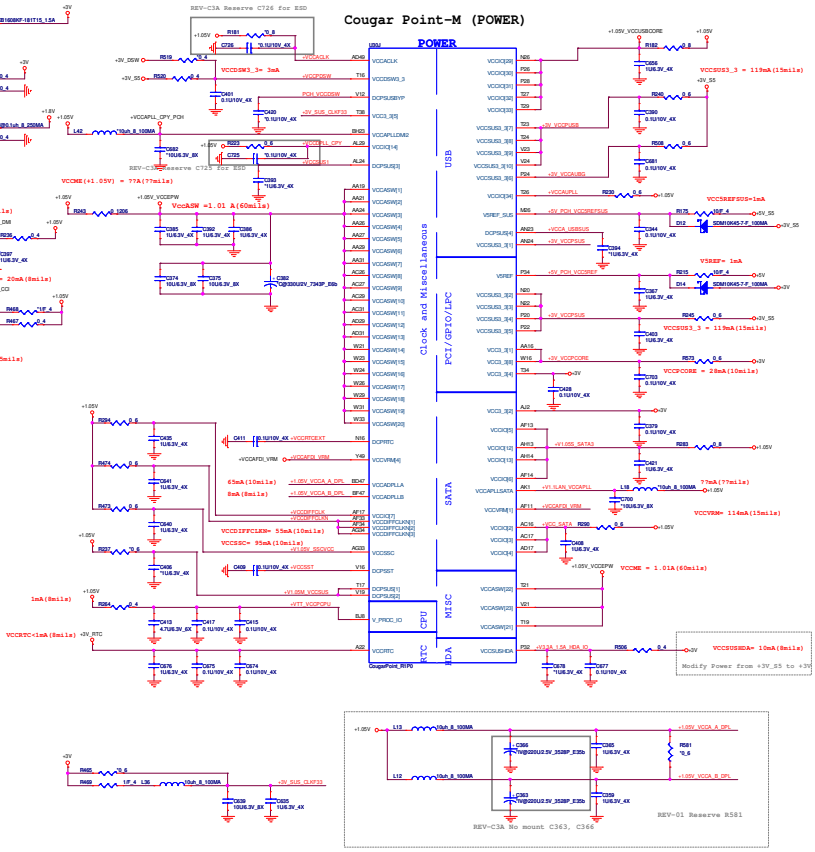
COUGAR POINT (POWER)



Cougar Point-M (POWER)



Modify Power from +3V_S5 to +3V

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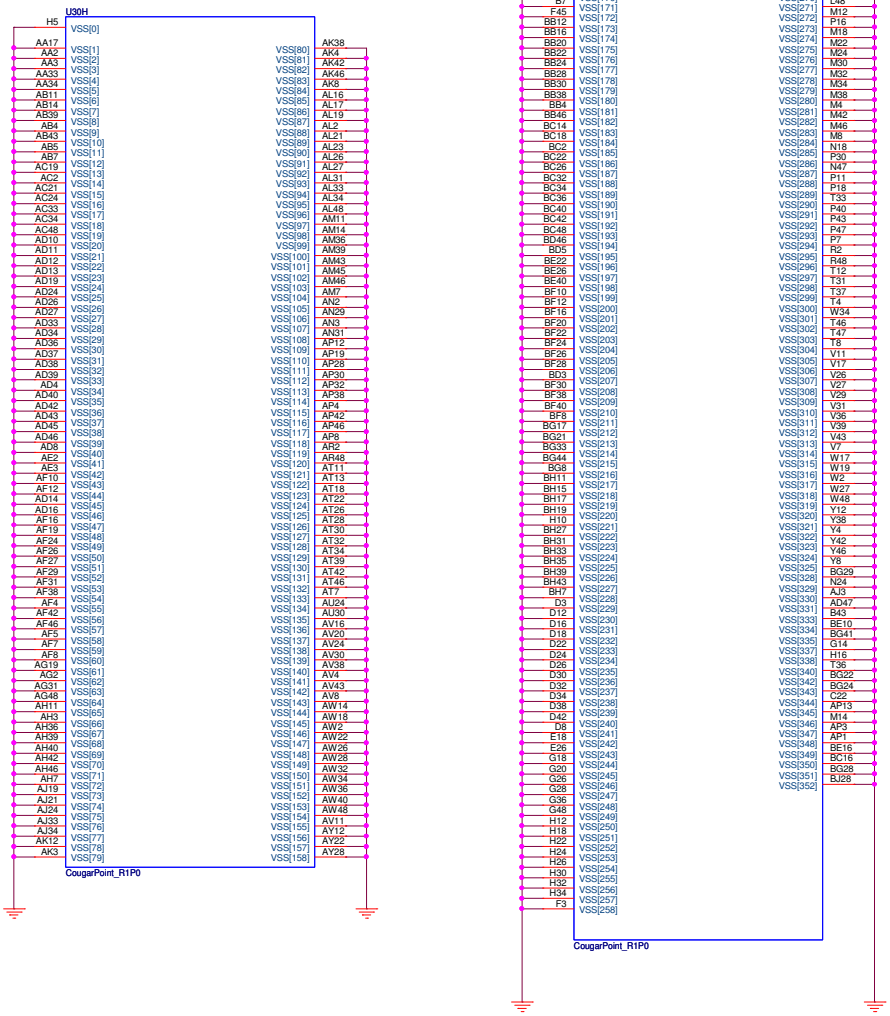
IBEX PEAK-M (GND)



Quanta Computer Inc.		
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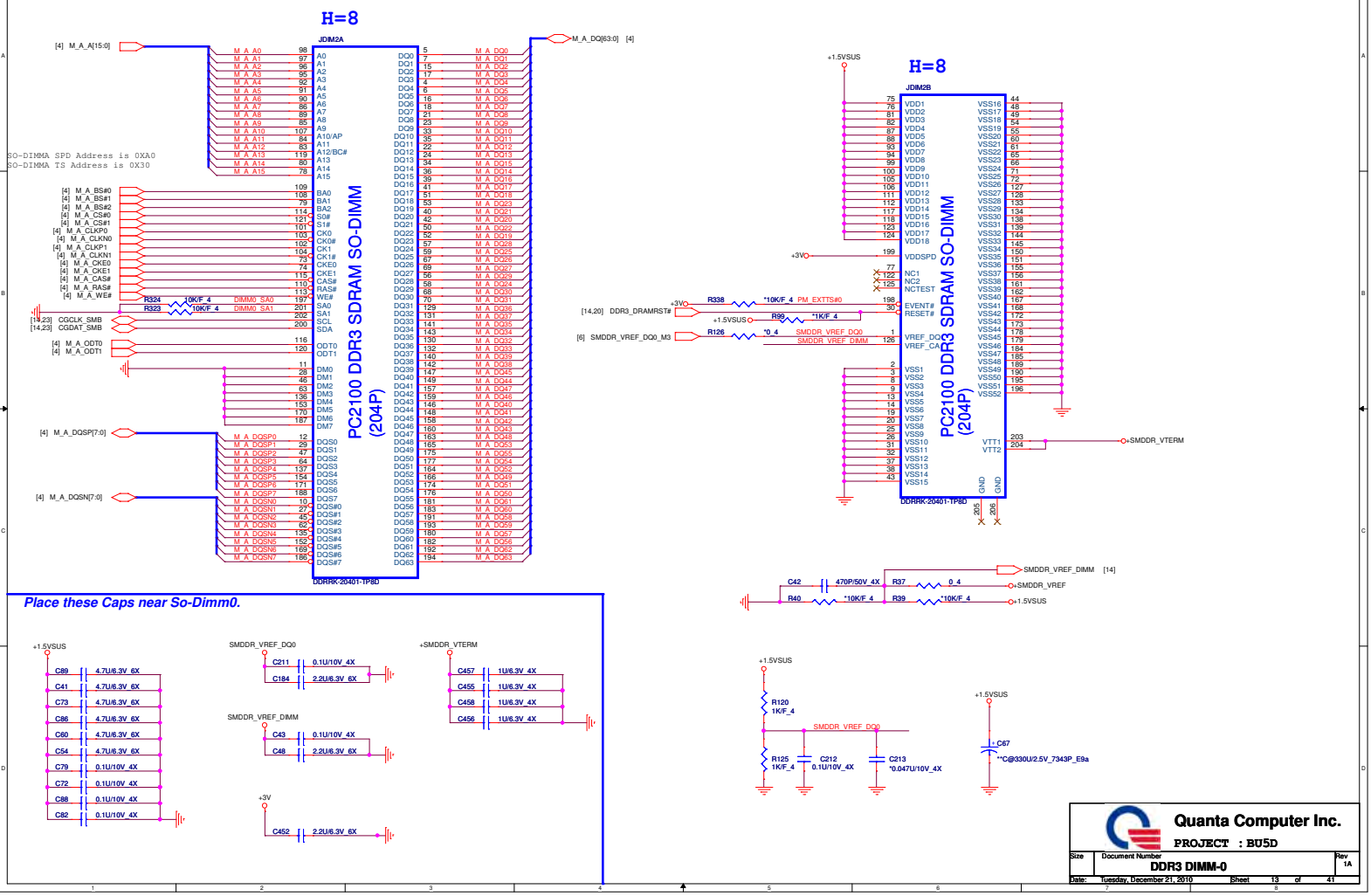
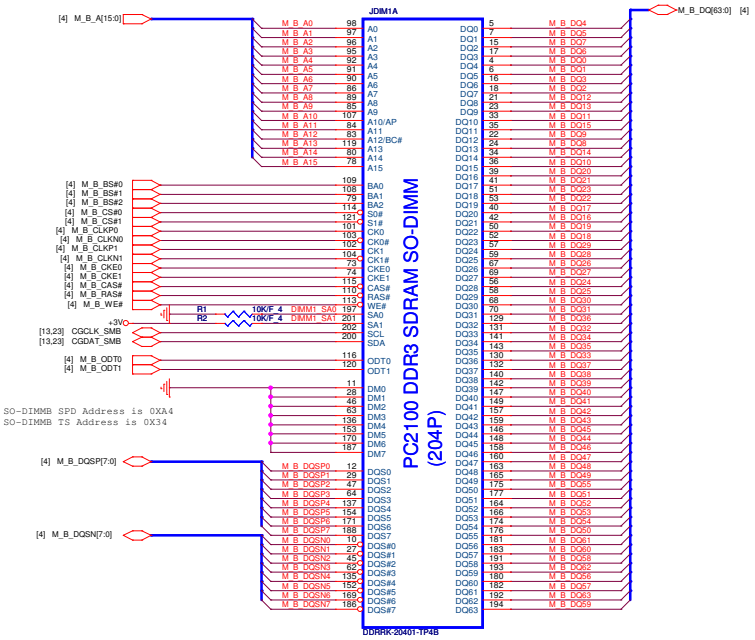
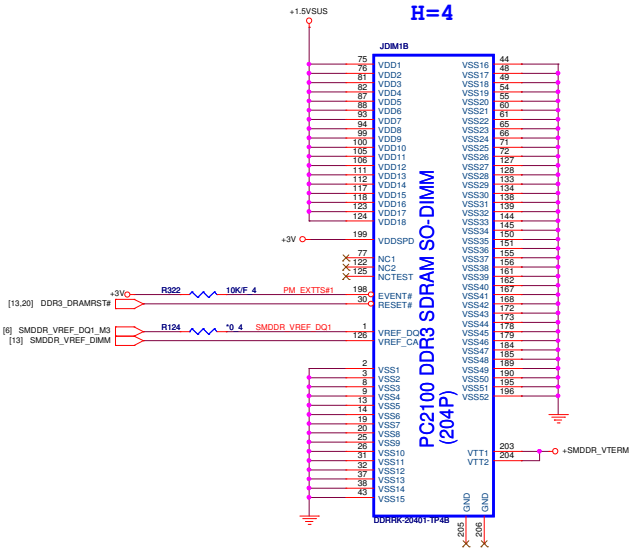
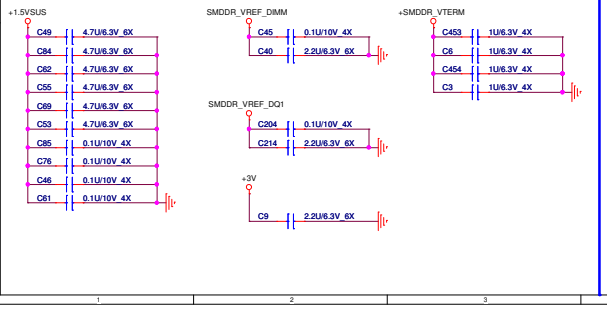

H=8
JDIM2A
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDRRK-20401-TP8D
SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30
H=8
JDIM2B
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDRRK-20401-TP8D
Place these Caps near So-Dimm0.
Quanta Computer Inc.
PROJECT : BU5D
DDR3 DIMM-0
Tuesday, December 21, 2010

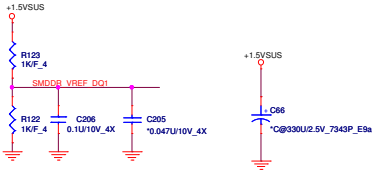
H=4





Place these Caps near So-Dimm1.





Quanta Computer Inc.			
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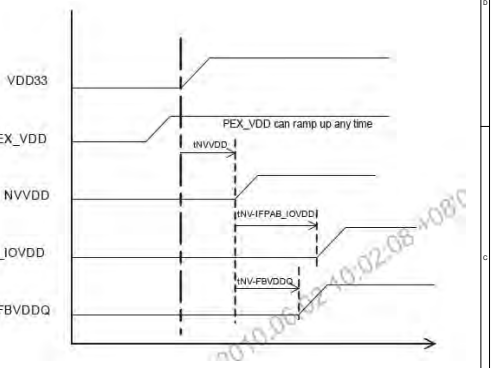
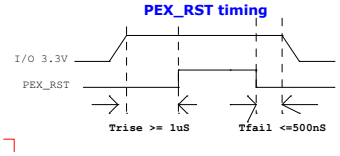
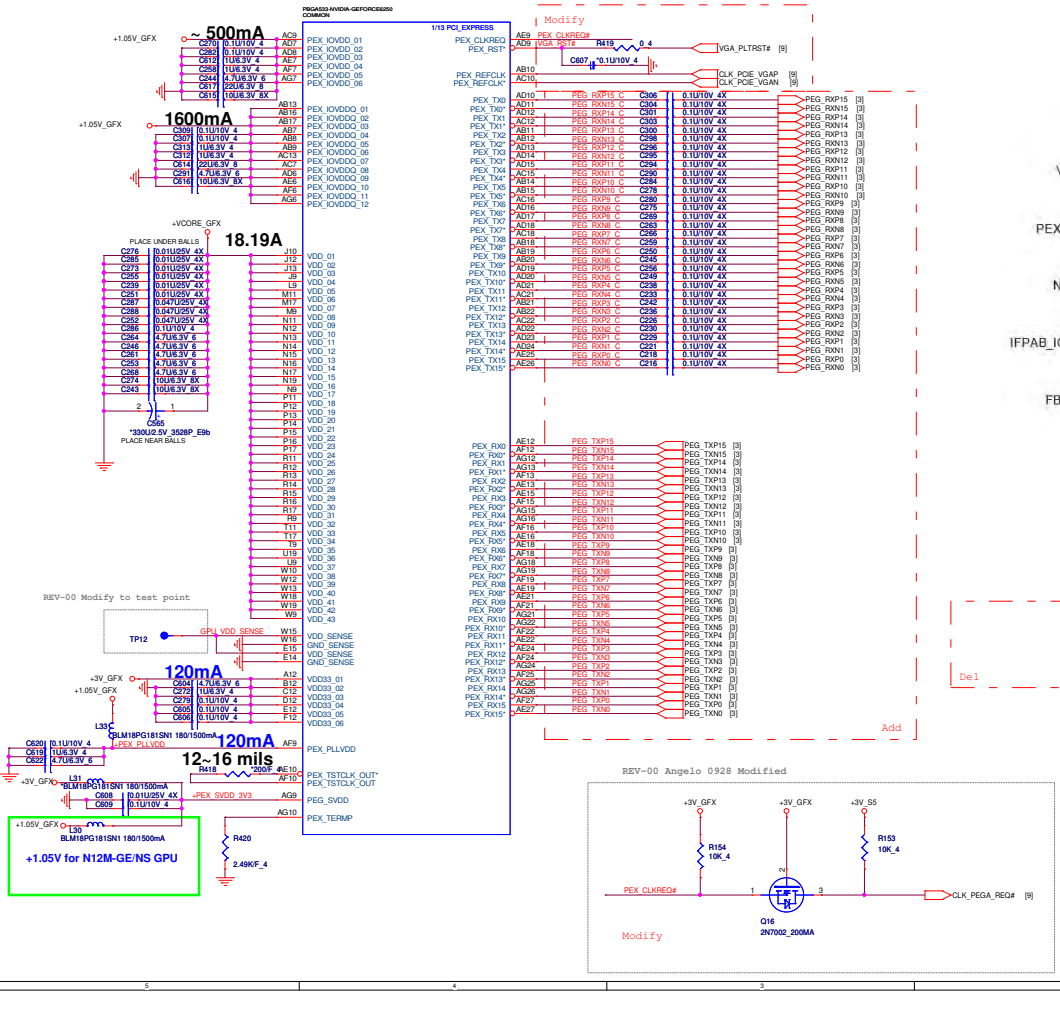
power up sequence



PEX_RST timing





[3,6,7,8,9,10,11,13,14,17,18,21,22,23,25,27,30,31,32,34,39] +3V_GFX
[3,5,6,7,8,9,11,16,17,32,36,38,40] +1.05V_GFX
[40] +VCORE_GFX
[3,7,8,9,10,11,20,23,24,28,31,34,35,39] +3V_S5

Quanta Computer Inc.

PROJECT : BU5D

Size	Document Number	Rev
	N12M-GE (PCIE I/F)	1A
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2.16A

+1.5V_GFX

U27B

PBGA533-NVIDIA-GEFORCE6250

COMMON

2/13 FRAME_BUFFER

C257 0.047U/25V_4X
C265 0.047U/25V_4X
C235 0.047U/25V_4X
C248 0.01U/25V_4X
C241 0.01U/25V_4X
C232 0.01U/25V_4X
C231 4.7U/6.3V_6
C525 4.7U/6.3V_6

FBVDDQ_01 A13
FBVDDQ_02 B13
FBVDDQ_03 C13
FBVDDQ_04 D13
FBVDDQ_05 D14
FBVDDQ_06 E13
FBVDDQ_07 F13
FBVDDQ_08 F14
FBVDDQ_09 F15
FBVDDQ_10 F16
FBVDDQ_11 F17
FBVDDQ_12 F19
FBVDDQ_13 F22
FBVDDQ_14 H23
FBVDDQ_15 H26
FBVDDQ_16 J15
FBVDDQ_17 J16
FBVDDQ_18 J18
FBVDDQ_19 J19
FBVDDQ_20 L19
FBVDDQ_21 L23
FBVDDQ_22 L26
FBVDDQ_23 M19
FBVDDQ_24 N22
FBVDDQ_25 U22
FBVDDQ_26 Y22

FBA_D0 D22
FBA_D1 E24
FBA_D2 E22
FBA_D3 D24
FBA_D4 D26
FBA_D5 C27
FBA_D6 B27
FBA_D7 B21
FBA_D8 C21
FBA_D9 C19
FBA_D10 C18
FBA_D11 D18
FBA_D12 B18
FBA_D13 C16
FBA_D14 E21
FBA_D15 F21
FBA_D16 D20
FBA_D17 F20
FBA_D18 D17
FBA_D19 F18
FBA_D20 D16
FBA_D21 E16
FBA_D22 A22
FBA_D23 C24
FBA_D24 D21
FBA_D25 B22
FBA_D26 C22
FBA_D27 A25
FBA_D28 B25
FBA_D29 A26
FBA_D30 D31
FBA_D31 U24
FBA_D32 V24
FBA_D33 V23
FBA_D34 R24
FBA_D35 T23
FBA_D36 R23
FBA_D37 P24
FBA_D38 P22
FBA_D39 AC24
FBA_D40 AB23
FBA_D41 AB24
FBA_D42 W24
FBA_D43 AA22
FBA_D44 W23
FBA_D45 W22
FBA_D46 V22
FBA_D47 AA25
FBA_D48 W27
FBA_D49 W26
FBA_D50 W25
FBA_D51 AB25
FBA_D52 AB26
FBA_D53 AD26
FBA_D54 AD27
FBA_D55 V25
FBA_D56 R25
FBA_D57 V26
FBA_D58 V27
FBA_D59 R26
FBA_D60 T25
FBA_D61 N25
FBA_D62 N26
FBA_D63

VMA_DQ0
VMA_DQ1
VMA_DQ2
VMA_DQ3
VMA_DQ7
VMA_DQ5
VMA_DQ6
VMA_DQ4
VMA_DQ8
VMA_DQ9
VMA_DQ10
VMA_DQ11
VMA_DQ12
VMA_DQ13
VMA_DQ14
VMA_DQ15
VMA_DQ16
VMA_DQ17
VMA_DQ18
VMA_DQ19
VMA_DQ20
VMA_DQ21
VMA_DQ22
VMA_DQ23
VMA_DQ24
VMA_DQ25
VMA_DQ26
VMA_DQ27
VMA_DQ28
VMA_DQ29
VMA_DQ30
VMA_DQ31
VMA_DQ32
VMA_DQ33
VMA_DQ34
VMA_DQ35
VMA_DQ36
VMA_DQ37
VMA_DQ38
VMA_DQ39
VMA_DQ40
VMA_DQ41
VMA_DQ42
VMA_DQ43
VMA_DQ44
VMA_DQ45
VMA_DQ46
VMA_DQ47
VMA_DQ48
VMA_DQ49
VMA_DQ50
VMA_DQ51
VMA_DQ52
VMA_DQ53
VMA_DQ54
VMA_DQ55
VMA_DQ56
VMA_DQ57
VMA_DQ58
VMA_DQ59
VMA_DQ60
VMA_DQ61
VMA_DQ62
VMA_DQ63

REV-00 Change ball name and net for GB1b.

REV-00 Change ball name and net for GB1b.

[19] VMA_DQ[63..0]
[19] VMA_DM[7..0]
[19] VMA_WDQS[7..0]
[19] VMA_RDQS[7..0]

TP83 FBA_CMD1
TP84 FBA_CMD17

[19] FBA_CMD0 G24
[19] FBA_CMD2 F25
[19] FBA_CMD3 F26
[19] FBA_CMD4 G26
[19] FBA_CMD5 G27
[19] FBA_CMD6 G25
[19] FBA_CMD7 J25
[19] FBA_CMD8 J24
[19] FBA_CMD9 H24
[19] FBA_CMD10 H22
[19] FBA_CMD11 J26
[19] FBA_CMD12 G22
[19] FBA_CMD13 G23
[19] FBA_CMD14 J22
[19] FBA_CMD15 J27
[19] FBA_CMD16 M24
L24
[19] FBA_CMD18 J23
[19] FBA_CMD19 K23
[19] FBA_CMD20 K22
[19] FBA_CMD21 M23
[19] FBA_CMD22 K24
[19] FBA_CMD23 M27
[19] FBA_CMD24 N27
[19] FBA_CMD25 M26
[19] FBA_CMD26 K26
[19] FBA_CMD27 K27
[19] FBA_CMD28 K25
[19] FBA_CMD29 M25
[19] FBA_CMD30 L22

(FBA_CMD25)FBA_CMD0
(FBA_CMD23)FBA_CMD1
FBA_CMD2
(FBA_CMD0)FBA_CMD3
(FBA_CMD10)FBA_CMD4
(FBA_CMD26)FBA_CMD5
(FBA_CMD14)FBA_CMD6
FBA_CMD7
(FBA_CMD1)FBA_CMD8
(FBA_CMD22)FBA_CMD9
(FBA_CMD20)FBA_CMD10
(FBA_CMD24)FBA_CMD11
(FBA_CMD18)FBA_CMD12
(FBA_CMD9)FBA_CMD13
(FBA_CMD29)FBA_CMD14
(FBA_CMD6)FBA_CMD15
(FBA_CMD27)FBA_CMD16
(FBA_CMD15)FBA_CMD17
(FBA_CMD11)FBA_CMD18
(FBA_CMD16)FBA_CMD19
(FBA_CMD28)FBA_CMD20
(FBA_CMD3)FBA_CMD21
(FBA_CMD17)FBA_CMD22
(FBA_CMD5)FBA_CMD23
(FBA_CMD4)FBA_CMD24
(FBA_CMD21)FBA_CMD25
(FBA_CMD6)FBA_CMD26
(FBA_CMD13)FBA_CMD27
(FBA_CMD19)FBA_CMD28
(FBA_CMD12)FBA_CMD29
FBA_CMD30

(FBA_D35)FBA_D36
(FBA_D36)FBA_D35
(FBA_D37)FBA_D39
(FBA_D38)FBA_D37
(FBA_D39)FBA_D38

(FBA_D52)FBA_D55
(FBA_D55)FBA_D52
(FBA_D54)FBA_D53

[19] VMA_CLK0 F24
[19] VMA_CLK0# F23
[19] VMA_CLK1 N24
[19] VMA_CLK1# N23

VMA_CLK0
VMA_CLK0#
VMA_CLK1
VMA_CLK1#

FBA_CLK0
FBA_CLK0*
FBA_CLK1
FBA_CLK1*

+1.5V_GFX R414 40.2/F_4 FB_CAL_PD_VDDQ B15
R415 40.2/F_4 FB_CAL_PU_GND A15
R413 60.4/F_4 FB_CAL_TERM_GND B16
+1.5V_GFX R136 10K/F_4 FBA_DEBUG M22

FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
(FBA_DEBUG)FBA_DEBUG0

For debug only
10mA

+1.05V_GFX 15mils width 200mA
L32 PBY160808T-301Y-N_6 +FB_PLLAVDD R19
300 ohm/100MHz
ESR=0.25ohm
C611 4.7U/6.3V_6
C234 1U/6.3V_4
C610 0.1U/10V_4
C613 10U/6.3V_8X
T19
AC19

FB_PLLAVDD
FB_DLLAVDD
FB_PLLAVDD

FBA_DQS_WP0 C25
FBA_DQS_WP1 A19
FBA_DQS_WP2 E19
FBA_DQS_WP3 A24
FBA_DQS_WP4 T22
FBA_DQS_WP5 AA24
FBA_DQS_WP6 AA26
FBA_DQS_WP7 T27

VMA_WDQS0
VMA_WDQS1
VMA_WDQS2
VMA_WDQS3
VMA_WDQS4
VMA_WDQS5
VMA_WDQS6
VMA_WDQS7

FBA_DQS_RN0 D25
FBA_DQS_RN1 A18
FBA_DQS_RN2 B24
FBA_DQS_RN3 R22
FBA_DQS_RN4 Y24
FBA_DQS_RN5 AA27
FBA_DQS_RN6 R27
FBA_DQS_RN7

VMA_RDQS0
VMA_RDQS1
VMA_RDQS2
VMA_RDQS3
VMA_RDQS4
VMA_RDQS5
VMA_RDQS6
VMA_RDQS7

FB_VREF A16 +FB_VREF1 TP84

FBA_CMD0 R388 10K/F_4
FBA_CMD3 R387 10K/F_4
FBA_CMD16 R110 10K/F_4
FBA_CMD19 R111 10K/F_4
FBA_CMD20 R112 10K/F_4

U27I

COMMON PBGA533-NVIDIA-GEFORCE6250

13/13 GND_NC

AC11 GND_01
AC12 GND_02
AC1 GND_03
AC2 GND_04
AC23 GND_05
AC25 GND_06
AC26 GND_07
AC5 GND_08
AC8 GND_09
AF11 GND_10
AF14 GND_11
AF17 GND_12
AF2 GND_13
AF20 GND_14
AF23 GND_15
AF25 GND_16
AF5 GND_17
AF8 GND_18
B11 GND_19
B14 GND_20
B17 GND_21
B2 GND_22
B20 GND_23
B23 GND_24
B26 GND_25
B5 GND_26
B8 GND_27
E11 GND_28
E17 GND_30
E2 GND_31
E20 GND_32
E23 GND_33
E26 GND_34
E5 GND_35
E8 GND_36
H2 GND_37
H5 GND_38
J11 GND_39
J14 GND_40
J17 GND_41
K16 GND_42
K9 GND_43
L11 GND_44
L12 GND_45
L13 GND_46
L14 GND_47
L15 GND_48
L16 GND_49
L17 GND_50
L2 GND_51
L5 GND_52
M12 GND_53
M13 GND_54
M14 GND_55
M15 GND_56
M16 GND_57
P19 GND_58
P2 GND_59
P23 GND_60
P26 GND_61
P5 GND_62
P9 GND_63
T12 GND_64
T13 GND_65
T14 GND_66
T15 GND_67
T16 GND_68
U11 GND_69
U12 GND_70
U13 GND_71
U14 GND_72
U15 GND_73
U16 GND_74
U17 GND_75
U2 GND_76
U23 GND_77
U26 GND_78
U5 GND_79
V19 GND_80
V9 GND_81
W11 GND_82
W14 GND_83
W17 GND_84
Y2 GND_85
Y23 GND_86
Y26 GND_87
Y5 GND_88

NC_01 C15
NC_02 D15
(NC_03)PGOOD R147 10K/F_4

nVIDIA comment 8/18

[3,5,6,7,8,9,11,15,17,32,36,38,40] +1.05V_GFX
[19,40] +1.5V_GFX

Quanta Computer Inc.

PROJECT : BU5D

Size	Document Number	Rev
	N12M-GE (MEMORY/GND)	1A
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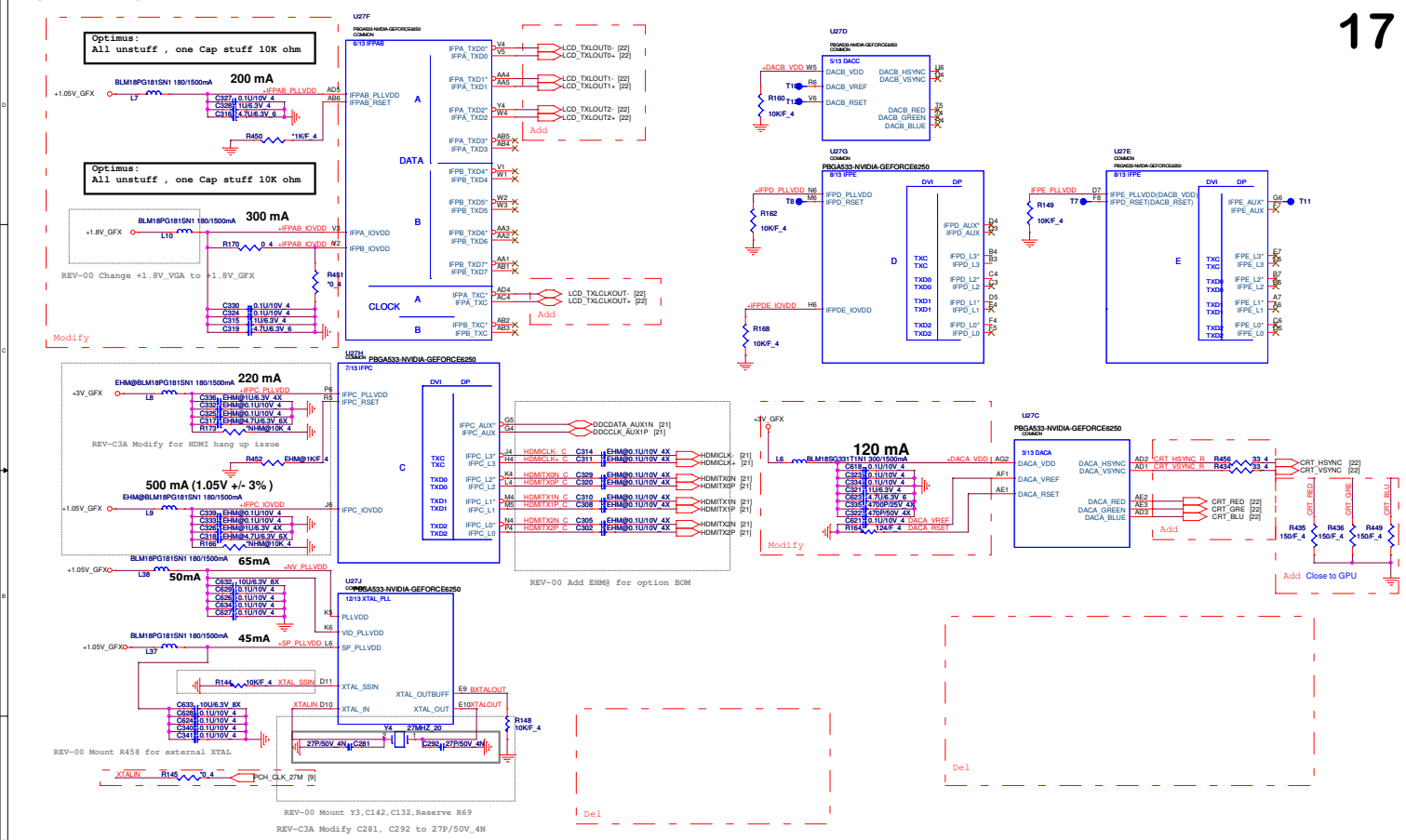

Quanta Computer Inc.
PROJECT : BU5D
Size | Document Number: N12M-GE (DISPLAY) | Rev 1A
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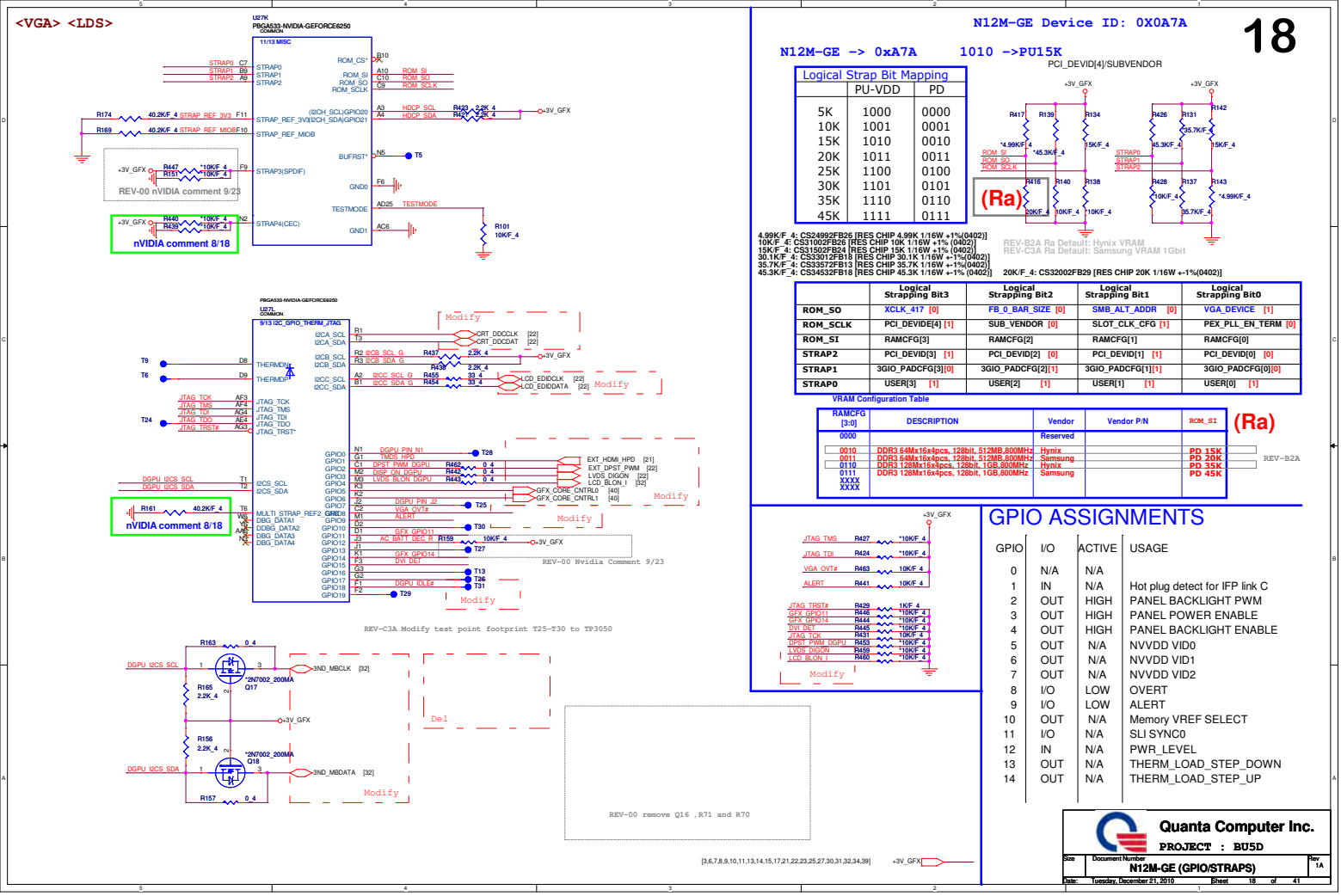

N12M-GE Device ID: 0X0A7A

N12M-GE -> 0xA7A 1010 ->PU15K

PCI_DEVID[4]/SUBVENDOR

Logical Strap Bit Mapping		
	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]

REV-B2A Ra Default: Hynix VRAM
REV-C3A Ra Default: Samsung VRAM 1Gbit

20K/F_4: CS32002FB29 [RES CHIP 20K 1/16W +-1%(0402)]

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	XCLK_417 [0]	FB_0_BAR_SIZE [0]	SMB_ALT_ADDR [0]	VGA_DEVICE [1]
ROM_SCLK	PCI_DEVIDE[4] [1]	SUB_VENDOR [0]	SLOT_CLK_CFG [1]	PEX_PLL_EN_TERM [0]
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3] [1]	PCI_DEVID[2] [0]	PCI_DEVID[1] [1]	PCI_DEVID[0] [0]
STRAP1	3GIO_PADCFG[3][0]	3GIO_PADCFG[2][1]	3GIO_PADCFG[1][1]	3GIO_PADCFG[0][0]
STRAP0	USER[3] [1]	USER[2] [1]	USER[1] [1]	USER[0] [1]

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0010	DDR3 64Mx16x4pcs, 128bit, 512MB,800MHz	Hynix		PD 15K
0011	DDR3 64Mx16x4pcs, 128bit, 512MB,800MHz	Samsung		PD 20K
0110	DDR3 128Mx16x4pcs, 128bit, 1GB,800MHz	Hynix		PD 35K
0111	DDR3 128Mx16x4pcs, 128bit, 1GB,800MHz	Samsung		PD 45K
XXXX				
XXXX				

(Ra)

REV-B2A

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	Memory VREF SELECT
11	I/O	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	THERM_LOAD_STEP_DOWN
14	OUT	N/A	THERM_LOAD_STEP_UP

Quanta Computer Inc.
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<VGA>

REV-B2A Hynix 64Mx16 P/N: AKD5LZWTW02--1st
Hynix 128Mx16 P/N: AKD5MGWTW00--2nd

CHANNEL A: 256MB/512MB DDR3

REV-C3A Default Samsung 1Gbit

[16] VMA_DQ[63..0]
[16] VMA_DM[7..0]
[16] VMA_WDQS[7..0]
[16] VMA_RDQS[7..0]

U12 U26 U11 U25

96-BALL SDRAM DDR3 VRAM_DDR3

+1.5V_GFX

R102 240/F_4
R379 240/F_4
R69 240/F_4
R380 240/F_4

R75 240/F_4 VMA_CLK0 VMA_CLK0#

R377 1.33K/F_4
R378 1.33K/F_4
C538 0.1U/10V_4

R73 1.33K/F_4
R72 1.33K/F_4
C113 0.1U/10V_4
VREFD_VMA1

R74 240/F_4 VMA_CLK1 VMA_CLK1#

R71 1.33K/F_4
R70 1.33K/F_4
C108 0.1U/10V_4
VREFC_VMA3

R375 1.33K/F_4
R376 1.33K/F_4
C532 0.1U/10V_4
VREFD_VMA3

Left
C153 0.1U/10V_4
C111 0.1U/10V_4
C112 1U/6.3V_4
C109 1U/6.3V_4

Right
C115 1U/6.3V_4
C114 1U/6.3V_4
C101 10U/6.3V_6X
C127 0.1U/10V_4
C116 0.1U/10V_4
C98 0.1U/10V_4

U10

Left
C536 1U/6.3V_4
C537 1U/6.3V_4
C567 0.1U/10V_4
C568 0.1U/10V_4

Right
C569 1U/6.3V_4
C539 0.1U/10V_4
C541 0.1U/10V_4
C540 0.1U/10V_4
C523 10U/6.3V_6X
C152 1U/6.3V_4

U31

Left
C106 0.1U/10V_4
C103 0.1U/10V_4
C135 1U/6.3V_4
C105 1U/6.3V_4

Right
C97 0.1U/10V_4
C102 0.1U/10V_4
C104 1U/6.3V_4
C107 0.1U/10V_4
C110 1U/6.3V_4
C100 10U/6.3V_6X

U11

Left
C528 0.1U/10V_4
C529 0.1U/10V_4
C530 0.1U/10V_4
C526 1U/6.3V_4
C531 1U/6.3V_4
C524 10U/6.3V_6X

Right
C534 0.1U/10V_4
C527 0.1U/10V_4
C535 1U/6.3V_4
C533 1U/6.3V_4

U30

[16,40] +1.5V_GFX

Quanta Computer Inc.
PROJECT : BU5D

Size	Document Number	Rev
	DDR3 VRAM (BGA96)	1A
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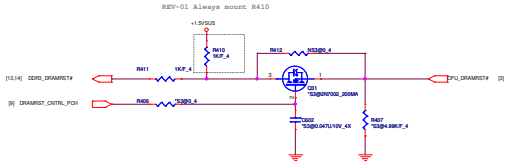
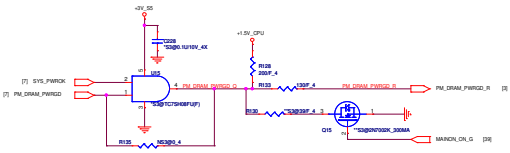
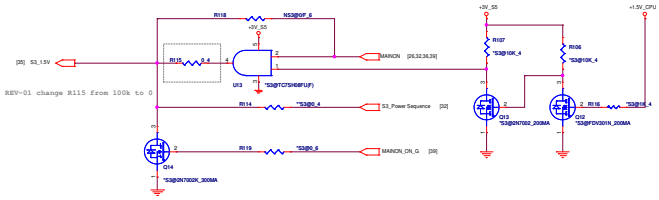
S3 power Reduction (SM_DRAMRST#)<S3P> <CLG> <4>



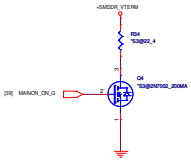
S3 power Reduction (SM_DRAMPWROK)<S3P> <3>



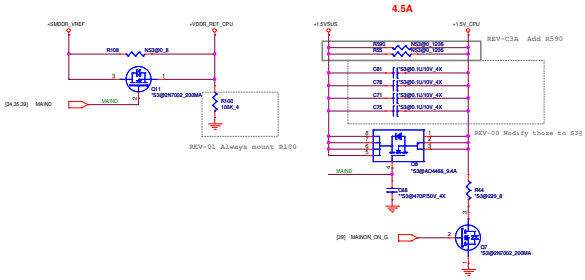
For S3 power Reduction Sequence<S3P> <3>



For S3 power Reduction VTT discharge<S3P> <13>



S3 power Reduction (CPU Power)<S3P> <5>



Quanta Computer Inc.

PROJECT : BU5D

Size | Document Number | Rev

S3 power Reduction | 1A

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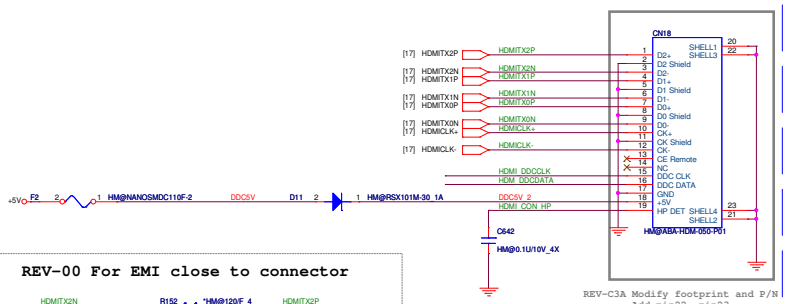
HDMI Conn <HDM>

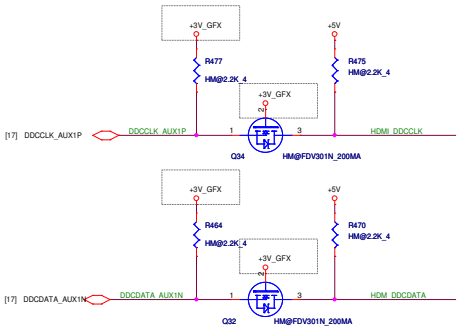
HDMI-CONN



REV-00 For EMI close to connector

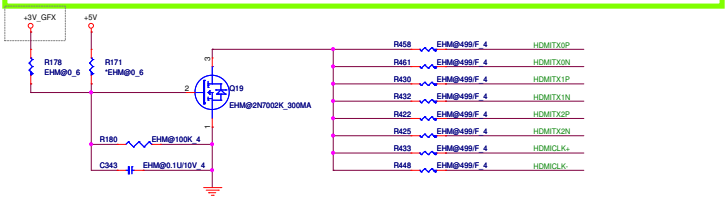
HDMITX2N	R152	*HM@120/F_4	HDMITX2P
HDMITX1N	R155	*HM@120/F_4	HDMITX1P
HDMITX0N	R167	*HM@120/F_4	HDMITX0P
HDMICLK-	R158	*HM@120/F_4	HDMICLK+

HDMI-SMBus <HDM>

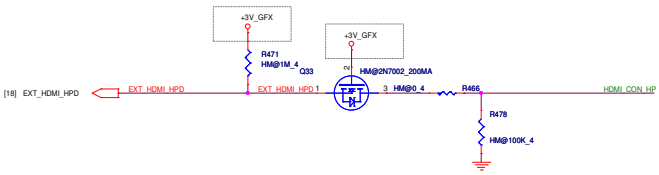


REV-00 Nvidia Comment +3V_GFX to instead of +3V
as below power rails to avoid power leakage issue

HDMI-passive level shift <HDM>



HDMI-HPD <HDM>



REV-00 Del External HDMI-HPD

Quanta Computer Inc.
PROJECT : BU5D

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	HDMI CONN	1A
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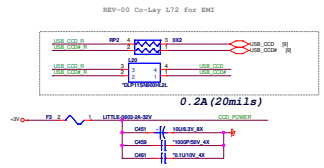
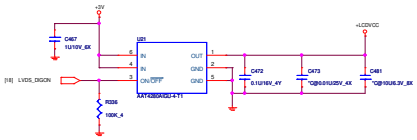
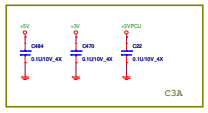
CCD <CCD>

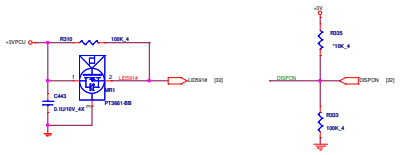


LCD POWER SWITCH <LDS>

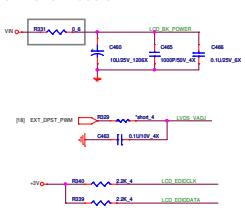


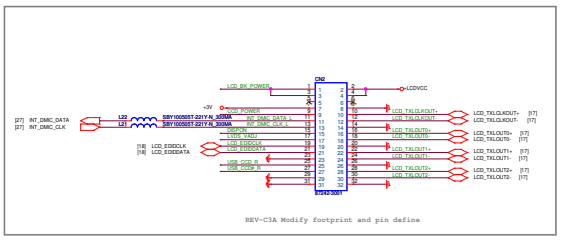
HALL SENSOR&BACK LIGHT SWITCH <HSR>



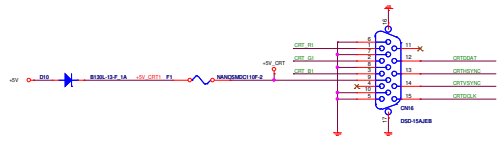


LCD Panel Module <LDS> <ADO>

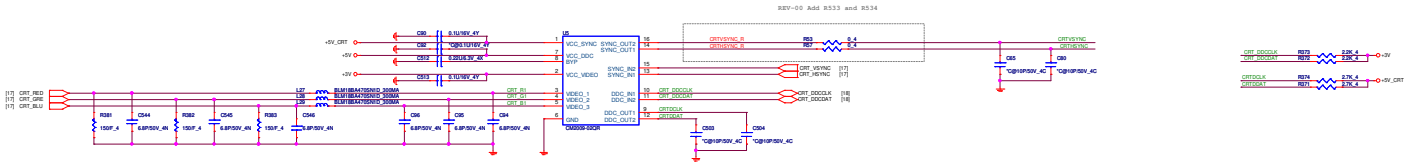




CRT CONN Interface <CRT>



<CRT>



Quanta Computer Inc.			
PROJECT : BU5D			
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	LCD/LED Panel/CCD		1A
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MINI Card Slot#1 <MNW>
(WiFi)

Before RAMP must to remove
debug card component

REV-C3A Mount C474

SMBus(DDR3/WLAN/3G)

MINI Card Slot#2 <MNT>
3G

REV-C3A Add R591

For SIM Card on daughtor board

REV-00 Co-Lay L77 for EMI

REV-00 update NEW footprint bl121-12r-tand-12p-1
REV-02A Modify footprint and pin define

REV-00 Add Q10,R7,R201 for CLK REQ#

Quanta Computer Inc.
PROJECT : BU5D

Size	Document Number	Rev
	MINI CARD(WLAN/3G/SIM Card)	1A
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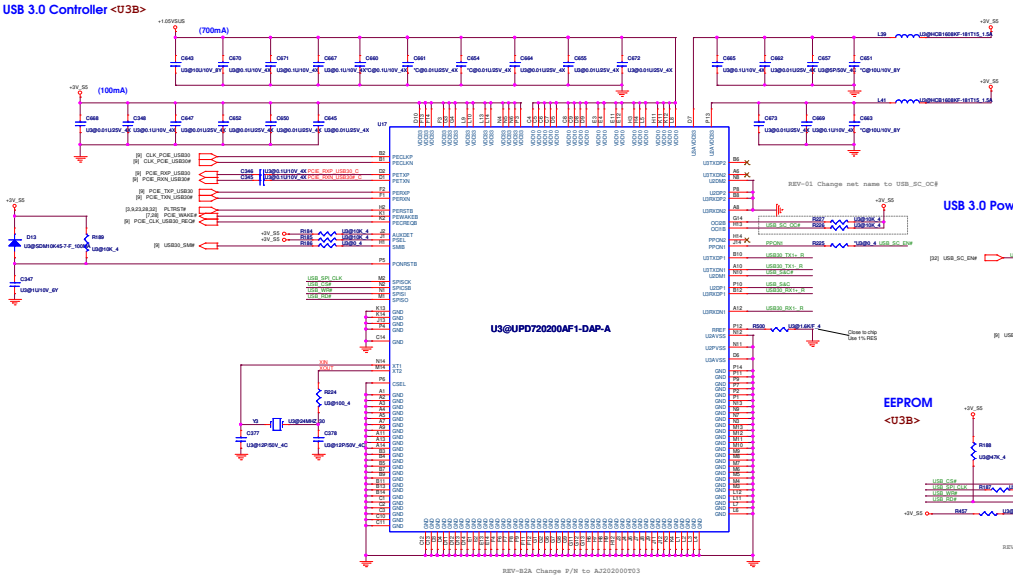
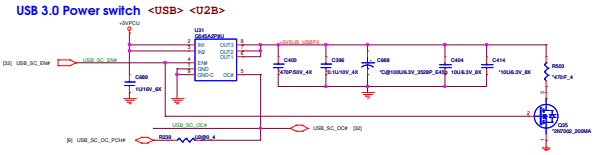
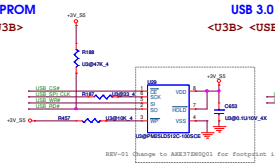
USB 3.0 Controller <U3B>



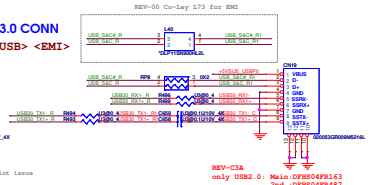
USB 3.0 Power switch <USB> <U2B>



EEPROM <U3B>

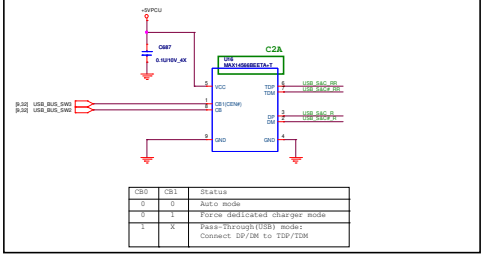


USB 3.0 CONN <U3B> <USB> <EMI>



USB 2.0 Colay <U3B> <U2B>

USB w S&C MAXIM solution <SLC>



CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

Quanta Computer Inc.			
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	USB 3.0(UPD720200F1-A)		1A
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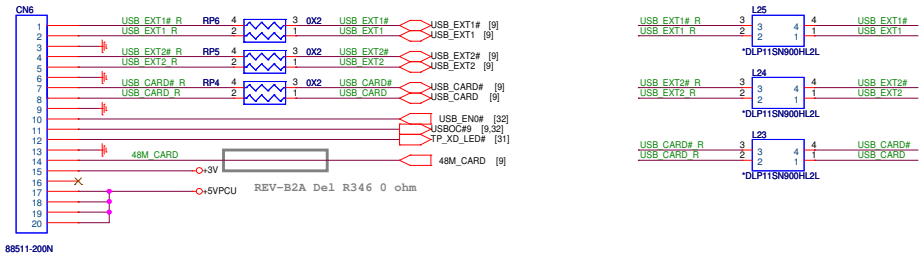
USB2.0 Left 1
USB2.0 Left 2 <U2B> <MMC> <EMI>



Quanta Computer Inc.		
PROJECT : BU5D		
Size	Document Number: HDMI CONN	Rev: 1A
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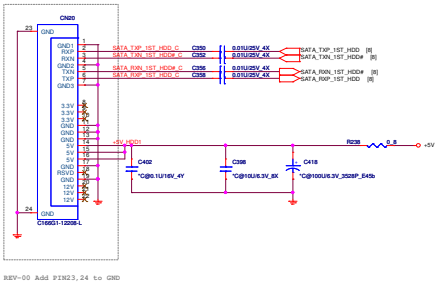
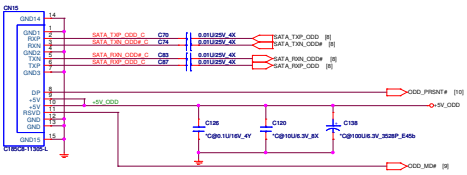
HDD Interface <H1D>

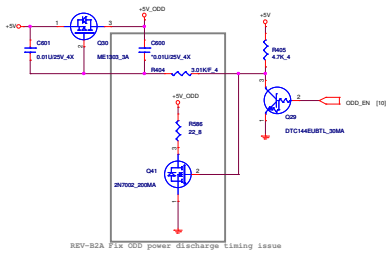


REV-00 Add PIN23,24 to GND

ODD Interface <ODD>

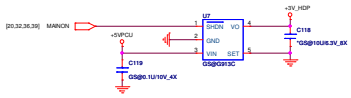


ODD Zero power . (Only for Intel) <OZP>

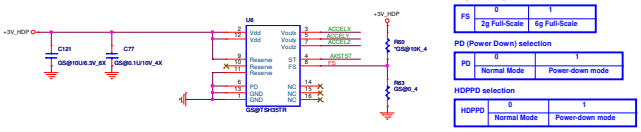


REV-B2A Fix ODD power discharge timing issue

3D-LDO Power <GSR>



3D-Sensor IC <GSR>



FS (Full Scale) selection

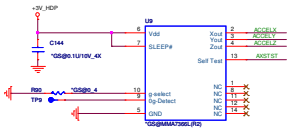
FS	0	1
	2g Full-Scale	6g Full-Scale

PD (Power Down) selection

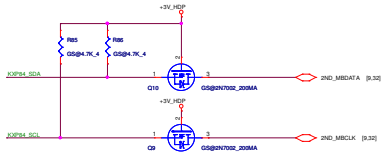
PD	0	1
	Normal Mode	Power-down mode

HDPPD selection

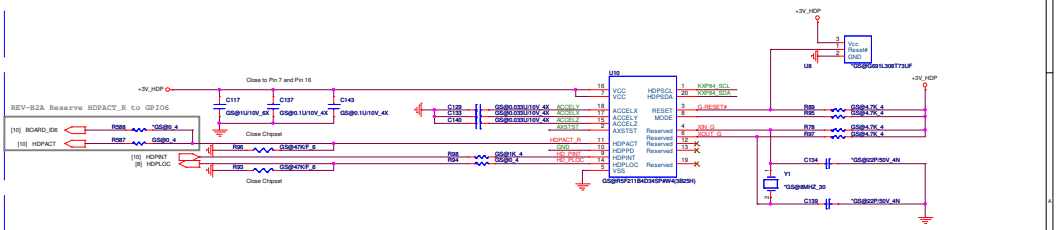
HDPPD	0	1
	Normal Mode	Power-down mode



3D-SMBus <GSR>



3D-u-micro P <GSR>



Quanta Computer Inc.			
PROJECT : BU5D			
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	HDD/ODD/MDC		1A
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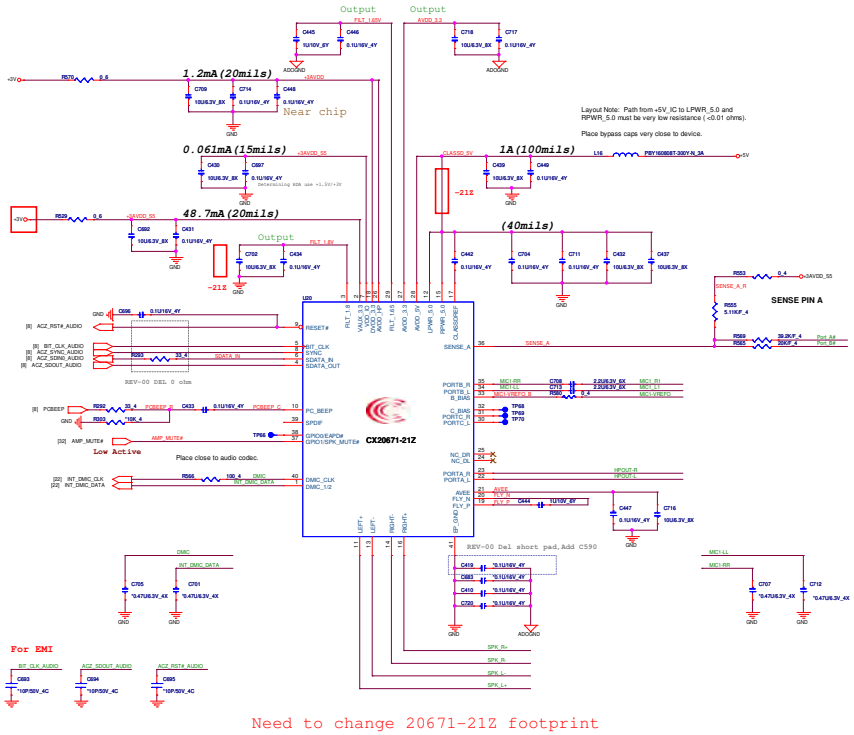
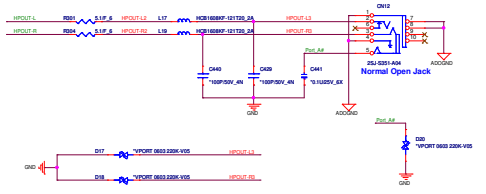
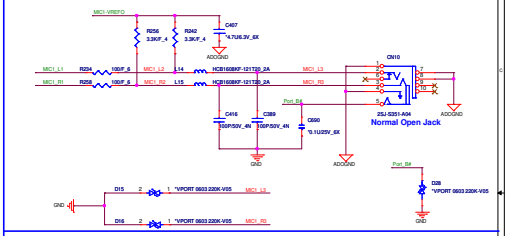
Codec (CX20671-21Z) <ADO>



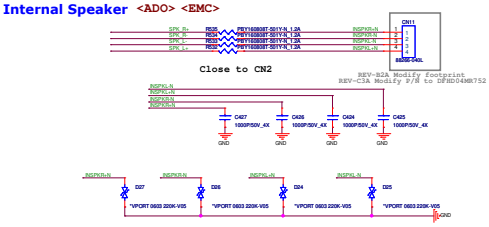
HP <ADO> <EMC>



External MIC <ADO> <EMC>



Internal Speaker <ADO> <EMC>



Quanta Computer Inc.

PROJECT : BU5D

Audio Codec(CX20671-21Z)

Rev: 1A

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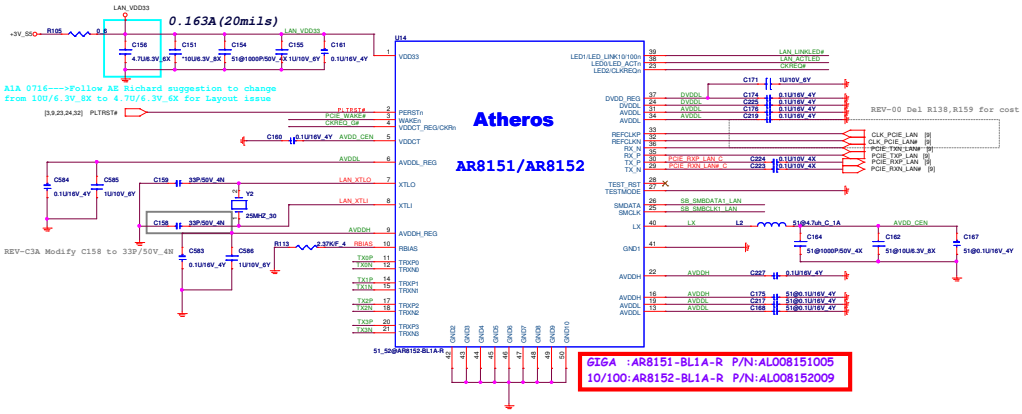
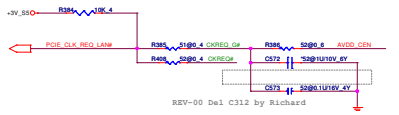
Atheros Lan <LAN> <LNG> <LN1> Default 10/100



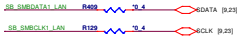
<LAN> <LNG> <LN1>



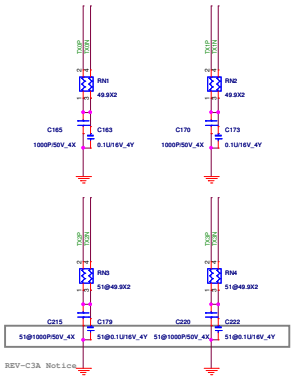
REV-00 Del R138,R159 for cost down

LAN-Wake up function

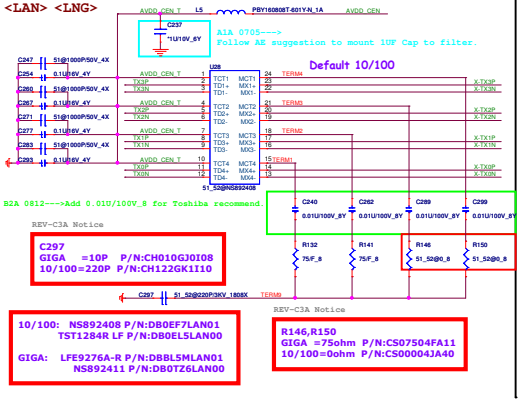
LAN-SM-Bus <LAN>



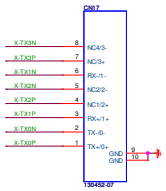
PLACE NEAR LAN IC SIDE <LAN> <LNG>



TRANSFORMER <LAN> <LNG>

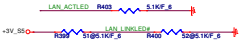


RJ45 <LAN> <LNG> <LN1>

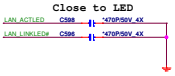


LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

Power on Strapping pin



Close to LED



Quanta Computer Inc.			
PROJECT : BU5D			
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	Atheros Lan		1A
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3 IN 1 CARD READER

3 IN 1 CARD READER

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	Card Reader (RTS5138)	1A
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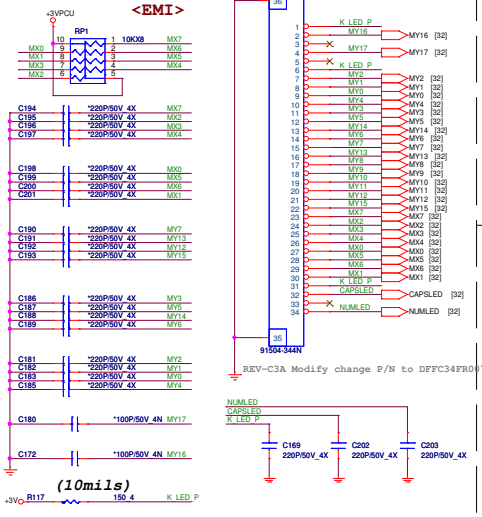
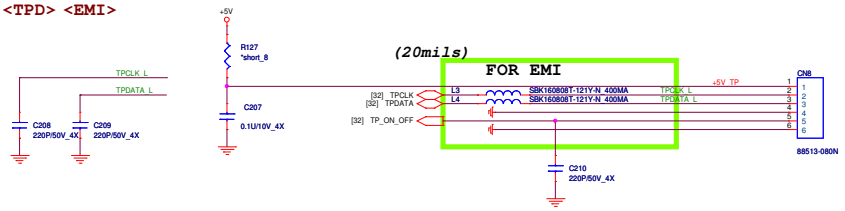
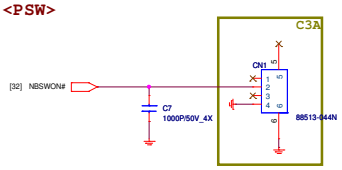
INT KeyBoard <KBC> <EMI>



TP board <TPD> <EMI>

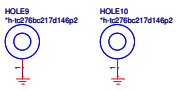


Power board <PSW>

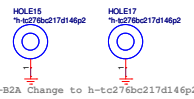


HOLE

CPU h-tc276bc217d146p2



VGA



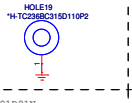
REV-B2A Change to h-tc276bc217d146p2

MINI CARD H-TC217BC142D102P2

REV-B2A Change to h-tc217bc138d102p2

HDD&ODD

H-TC236BC315D110P2



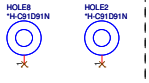
Pad-c197

h-tc315bc256d110p2

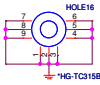
REV-B2A Change to h-tc315bc256d110p2

REV-00 Change GND to ADOGND

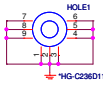
H-C91D91N



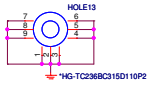
HG-TC315BC236D110P2



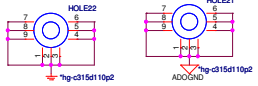
HG-C236D110P2



HG-TC236BC315D110P2

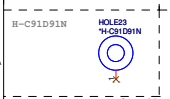


hg-c315d110p2



REV-B2A Change to hg-c315d110p2

H-C91D91N



REV-C3A Add

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Size	Document Number: KB/TP&TP/PB/FL/LEB/MMB/B-CAS	Rev: 1A
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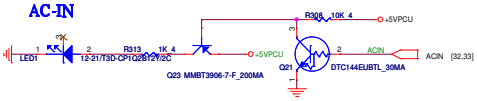
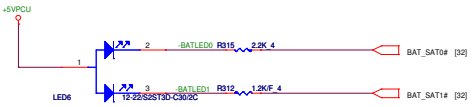
LED <LED>

AC-IN



BATERRY

D3A : LED luminance to light,1K-ohm change 2.2K-ohm.

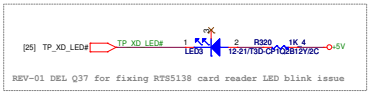


RF LED

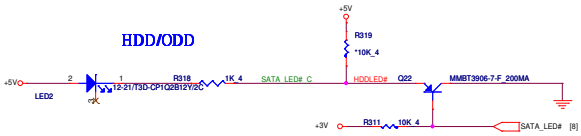
POWER

D3A : LED luminance to light,1K-ohm change 2.2K-ohm.

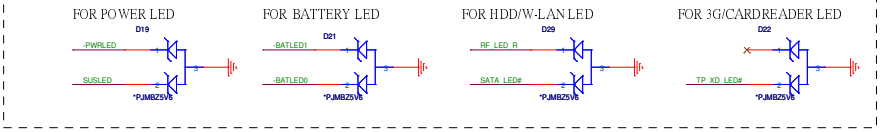
CARDREADER



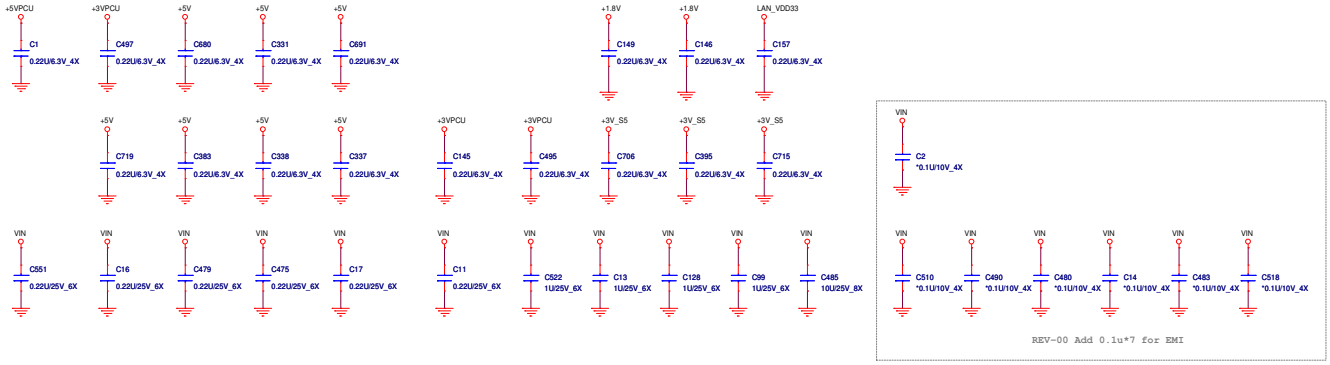
HDD/ODD



ESD Protect <EMC>



<EMI>



Quanta Computer Inc.

PROJECT : BU5D

Size	Document Number	Rev
	LED/HOLE	1A
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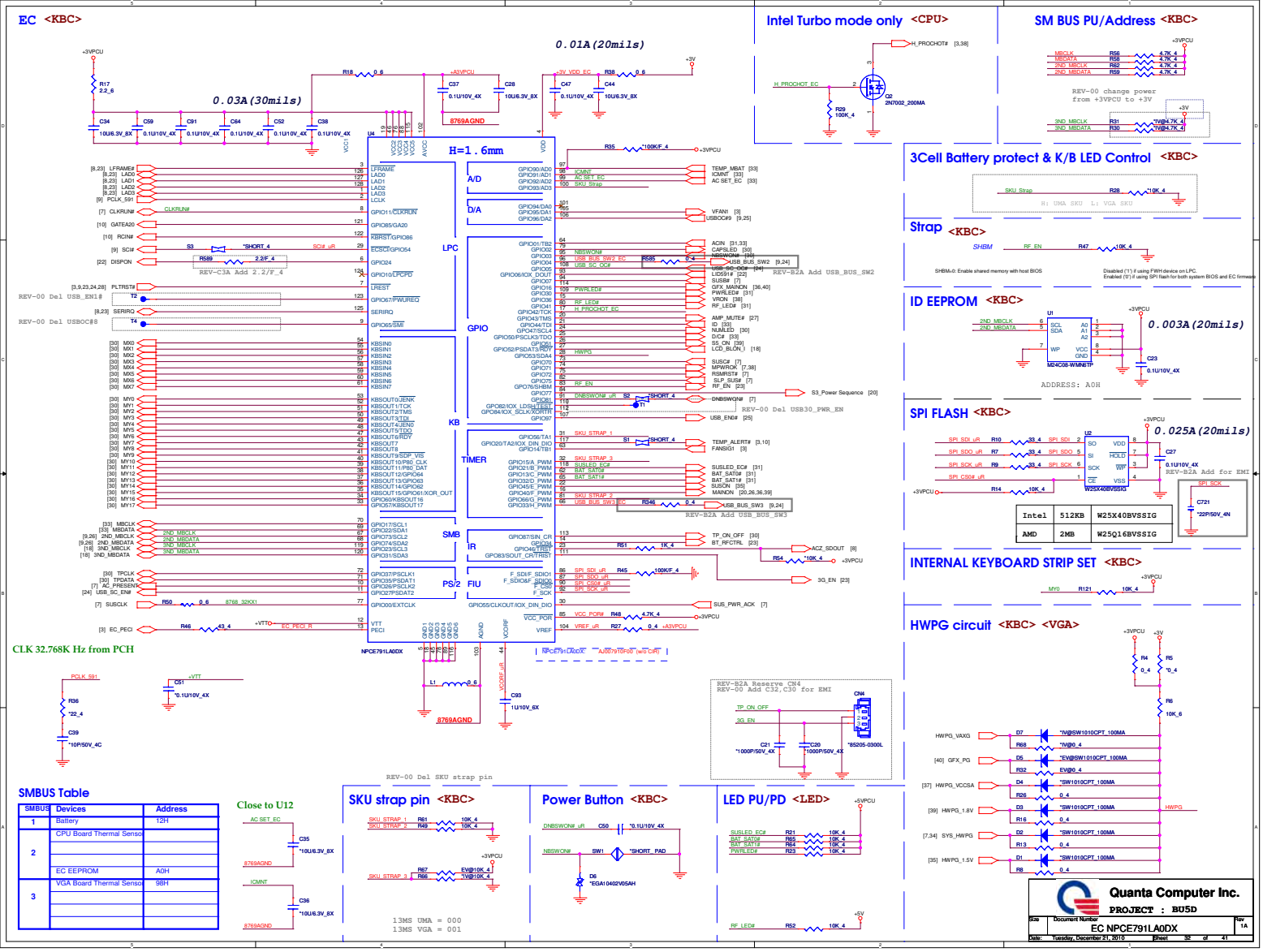
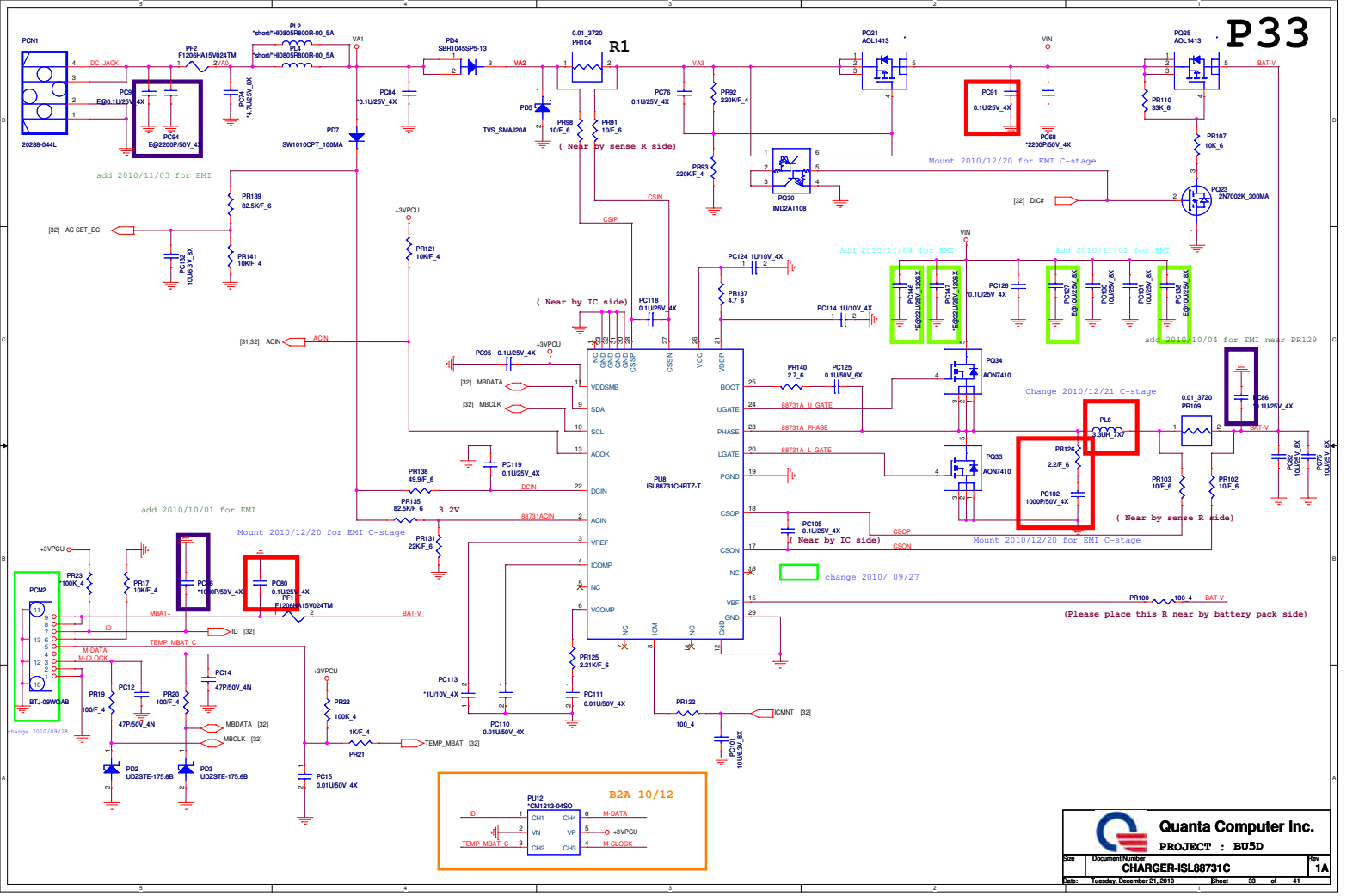

EC <KBC>
0.01A(20mils)
0.03A(30mils)
H=1.6mm
LPC
A/D
D/A
GPIO
KB
TIMER
SMB
IR
PS/2
FIU
NPCE791LA0DX
8769AGND
REV-00 Del SKU strap pin
CLK 32.768K Hz from PCH
Intel Turbo mode only <CPU>
H_PROCHOT_EC
Q2
2N7002_200MA
SM BUS PU/Address <KBC>
REV-00 change power from +3VPCU to +3V
3Cell Battery protect & K/B LED Control <KBC>
Strap <KBC>
SHBM
ID EEPROM <KBC>
M24C08-WMN6TP
ADDRESS: A0H
SPI FLASH <KBC>
0.025A(20mils)
W25X40BVSSIG
Intel 512KB W25X40BVSSIG
AMD 2MB W25Q16BVSSIG
INTERNAL KEYBOARD STRIP SET <KBC>
HWPG circuit <KBC> <VGA>
SMBUS Table
SMBUS Devices Address
1 Battery 12H
2 CPU Board Thermal Sensor
EC EEPROM A0H
3 VGA Board Thermal Sensor 98H
Close to U12
SKU strap pin <KBC>
13MS UMA = 000
13MS VGA = 001
Power Button <KBC>
LED PU/PD <LED>
Quanta Computer Inc.
PROJECT : BU5D
EC NPCE791LA0DX
Rev 1A
Tuesday, December 21, 2010



Quanta Computer Inc.

PROJECT : BU5D

Size	Document Number	Rev
	CHARGER-ISL88731C	1A

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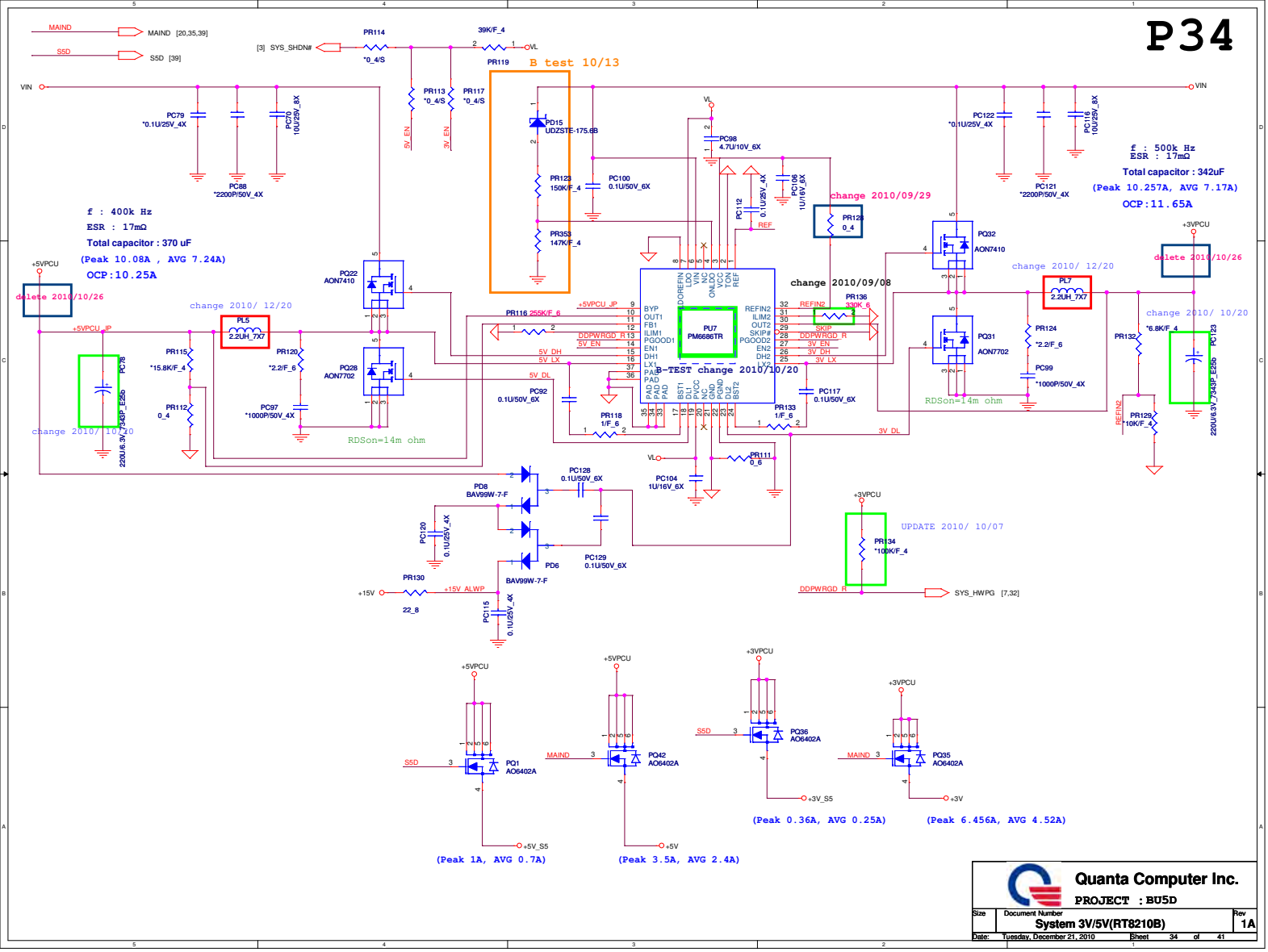

Quanta Computer Inc.			
PROJECT : BU5D			
Size	Document Number		Rev
	System 3V/5V(RT8210B)		1A
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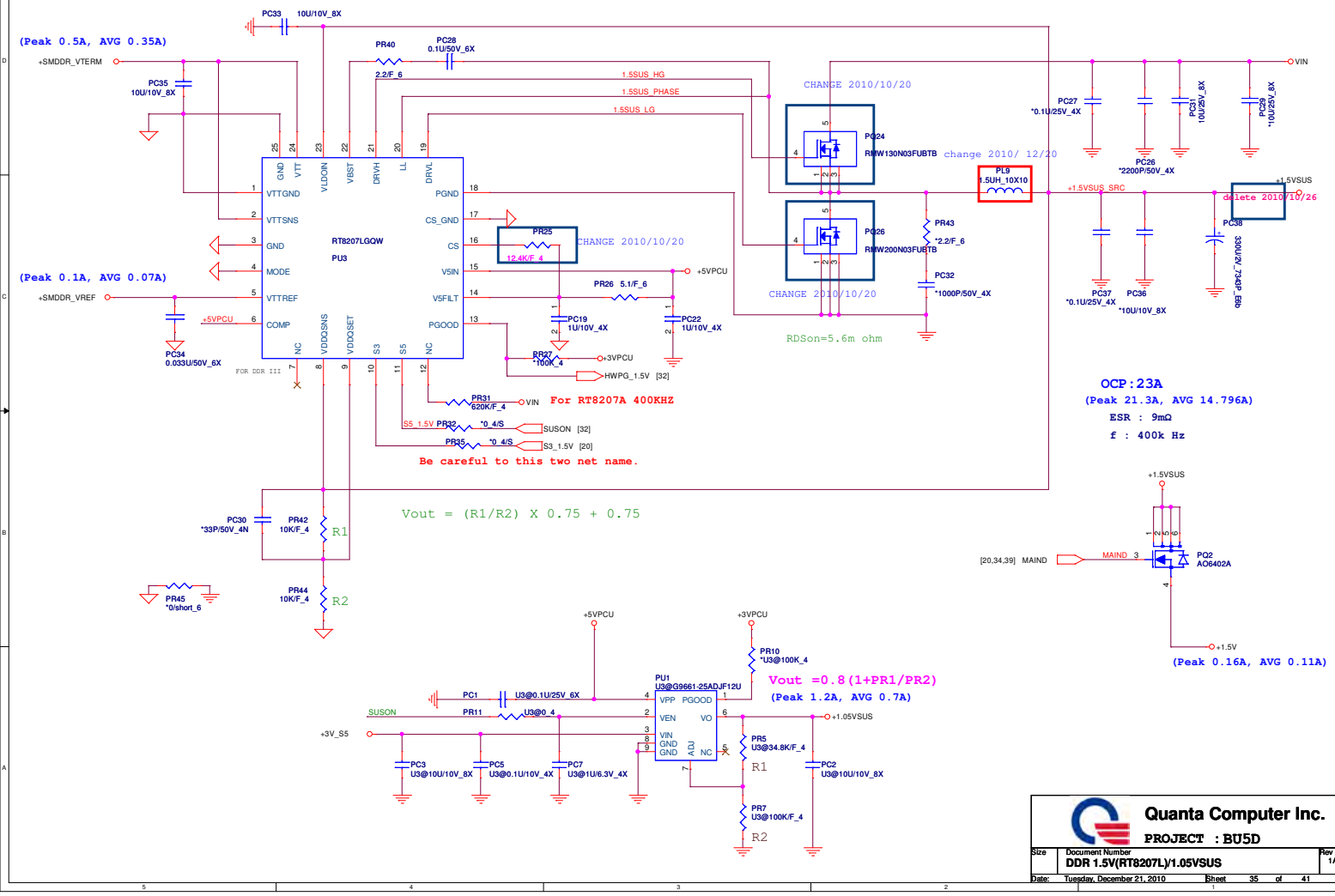

Quanta Computer Inc.

PROJECT : BU5D

Size	Document Number	Rev
	DDR 1.5V(RT8207L)/1.05VSUS	1A

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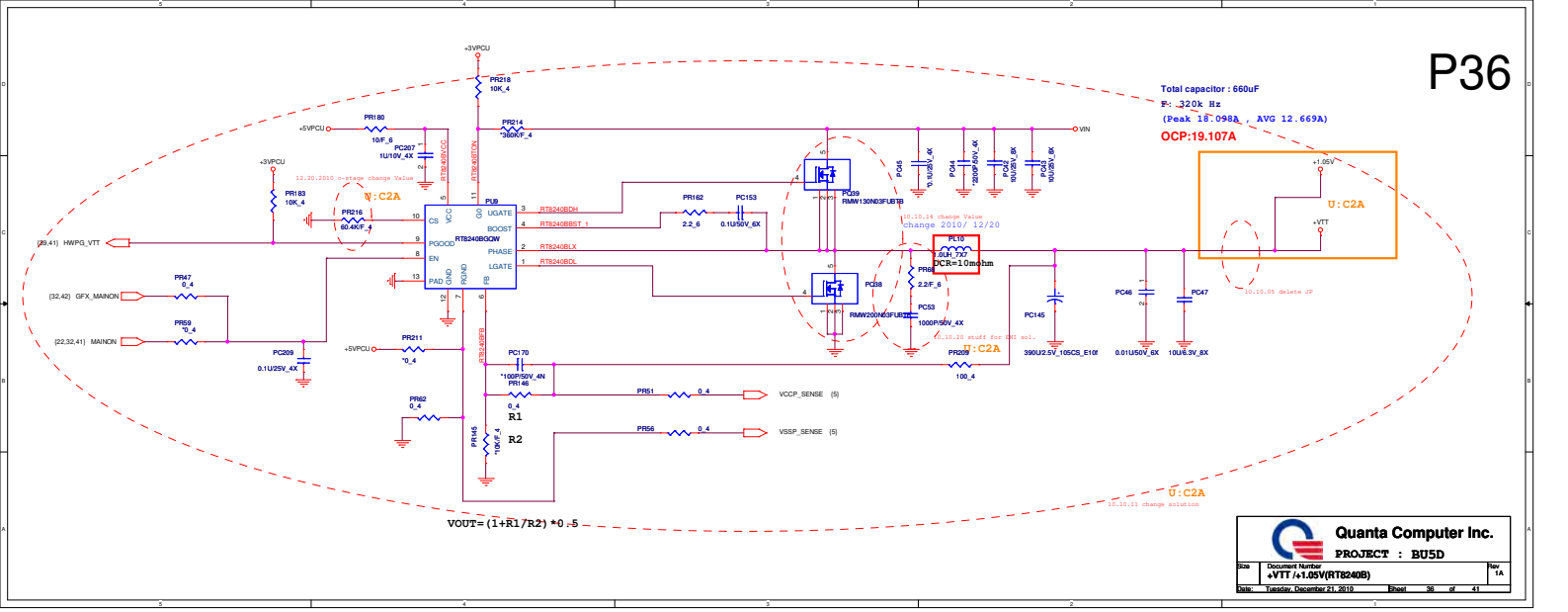
Total capacitor : 660uF
F: 320k Hz
(Peak 18.098A , AVG 12.669A)
OCP:19.107A
VOUT= (1+R1/R2) *0.5
R1
R2
RT8240BGQW
PR218 10K_4
PR214 *390K_4
PR180 10/F_6
PC207 1U/10V_4X
PR183 10K_4
PR216 60.4K/F_4
PR162 2.2_6
PC153 0.1U/50V_6X
PC170 *100P/50V_4N
PR146 0_4
PR51 0_4
PR56 0_4
PR62 0_4
PR145 10K_4
PR211 *0_4
PC209 0.1U/25V_4X
PR47 0_4
PR59 *0_4
PC45 *0.1U/25V_4X
PC44 *220P/50V_4X
PC43 10U/25V_6X
PC42 10U/25V_6X
PC39 RMW130N03FUBTB
PC38 RMW200N03FUBTB
PL10 1.0uH_7X7 DCR=10mohm
PR63 2.2/F_6
PC53 1000P/50V_4X
PR209 100_4
PC145 390U/2.5V_105CS_E10
PC46 0.01U/50V_6X
PC47 10U/6.3V_8X
VCCP_SENSE (5)
VSSP_SENSE (5)
U:C2A
12.20.2010 c-stage change Value
10.10.14 change Value
change 2010/ 12/20
10.10.20 stuff for EMI sol.
10.10.05 delete JP
10.10.11 change solution
Quanta Computer Inc.
PROJECT : BU5D
+VTT /+1.05V(RT8240B)
Tuesday, December 21, 2010
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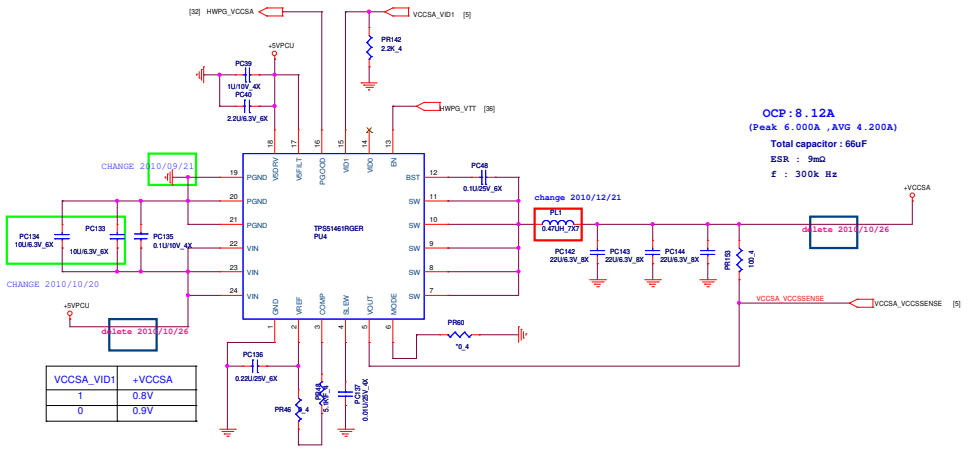

VCCSA_VID1	+VCCSA
1	0.8V
0	0.9V

Quanta Computer Inc.

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		1A

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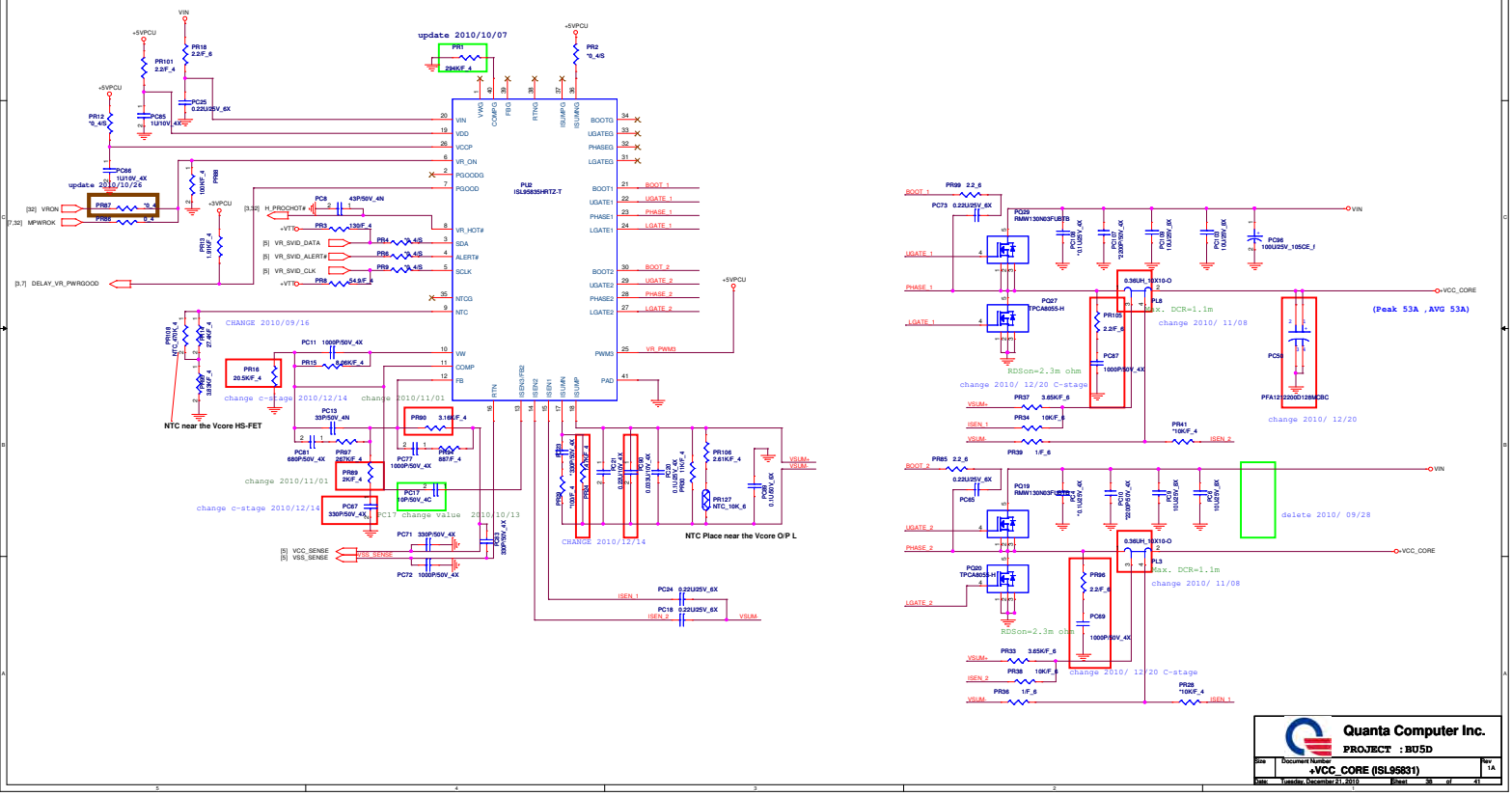

Quanta Computer Inc.			
PROJECT : BU5D			
Size	Document Number		Rev
	+VCC_CORE (ISL95831)		1A
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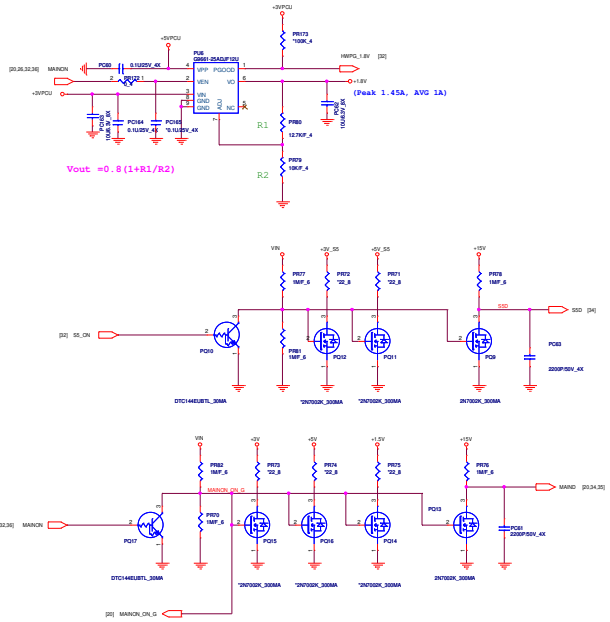

Quanta Computer Inc.

PROJECT : BU5D

Size	Document Number	Rev
	Discharge	1A
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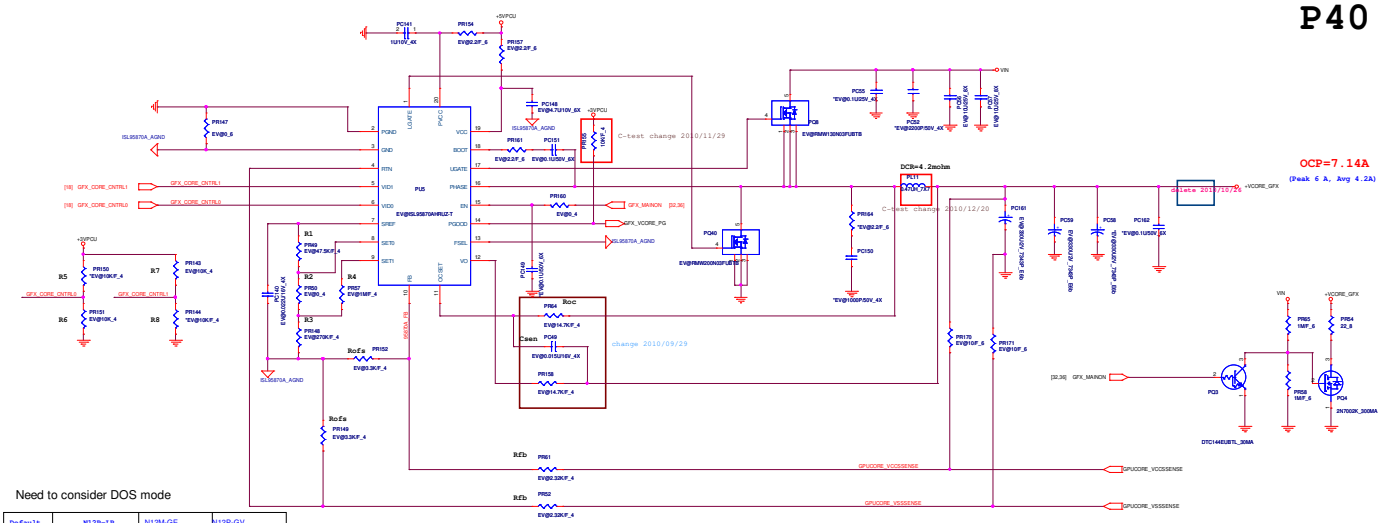
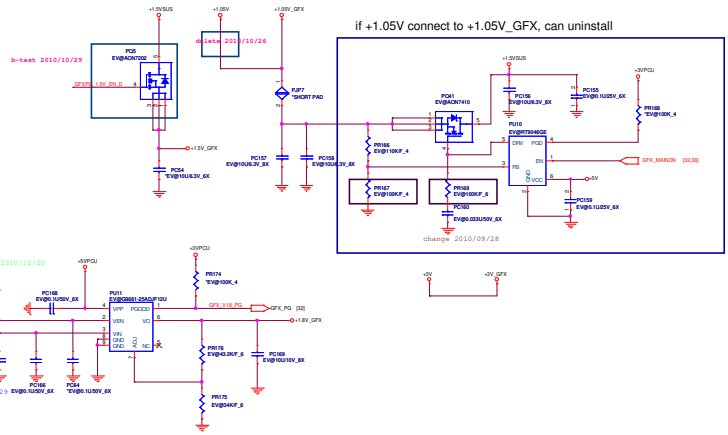
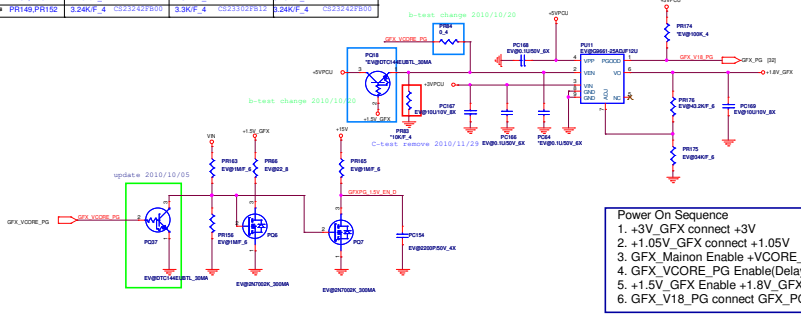


Default	N12P-LP	N12M-GE	N12P-GV
PR150 R5	10K CS31002JB28	NC	10K CS31002JB28
PR151 R6	NC	10K CS31002JB28	NC
PR143 R7	NC	10K CS31002JB28	10K CS31002JB28
PR144 R8	10K CS31002JB28	NC	NC

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	N12P-LP	N12M-GE	N12P-GV
LOW	LOW	0.925V	1.0V	0.98V
LOW	HIGH	0.90V Default	1.0V	0.98V
HIGH	LOW	0.9V	1.0V Default	0.98V
HIGH	HIGH	0.825V	0.85V	0.98V Default

		N12P-LP	N12M-GE	N12P-GV
R1	PR149	22.6K/F_4 CS32262FB15	47.5K/F_4 CS34752FB14	0_4 CS00002JB38
R2	PR50	0_4 CS00002JB38	0_4 CS00002JB38	0_4 CS00002JB38
R3	PR148	243K/F_4 CS42432FB02	270K/F_4 CS42702JB10	300K/F_4 CS43002JB18
R4	PR57	750K/F_4 CS47502FB14	1M/F_4 CS51002FB11	1M/F_4 CS51002FB11
Rfb	PR61,PR52	2.10K/F_4 CS22102FB12	2.32K/F_4 CS22322FB00	3.16K/F_4 CS23162FB00
Rofs	PR149,PR152	3.24K/F_4 CS23242FB00	3.3K/F_4 CS23302FB13	3.24K/F_4 CS23242FB00





Power On Sequence
1. +3V_GFX connect +3V
2. +1.05V_GFX connect +1.05V
3. GFX_Mainon Enable +VCORE_GFX
4. GFX_VCORE_PG Enable(Delay) +1.5V_GFX
5. +1.5V_GFX Enable +1.8V_GFX
6. GFX_V18_PG connect GFX_PG

Power Off Sequence
compare +VCC3_GFX with +V1.8_GFX

Quanta Computer Inc.			
PROJECT : BU5D			
Size	Document Number		Rev
	+VGACORE(ISL95870AHRUZ-T)		1A
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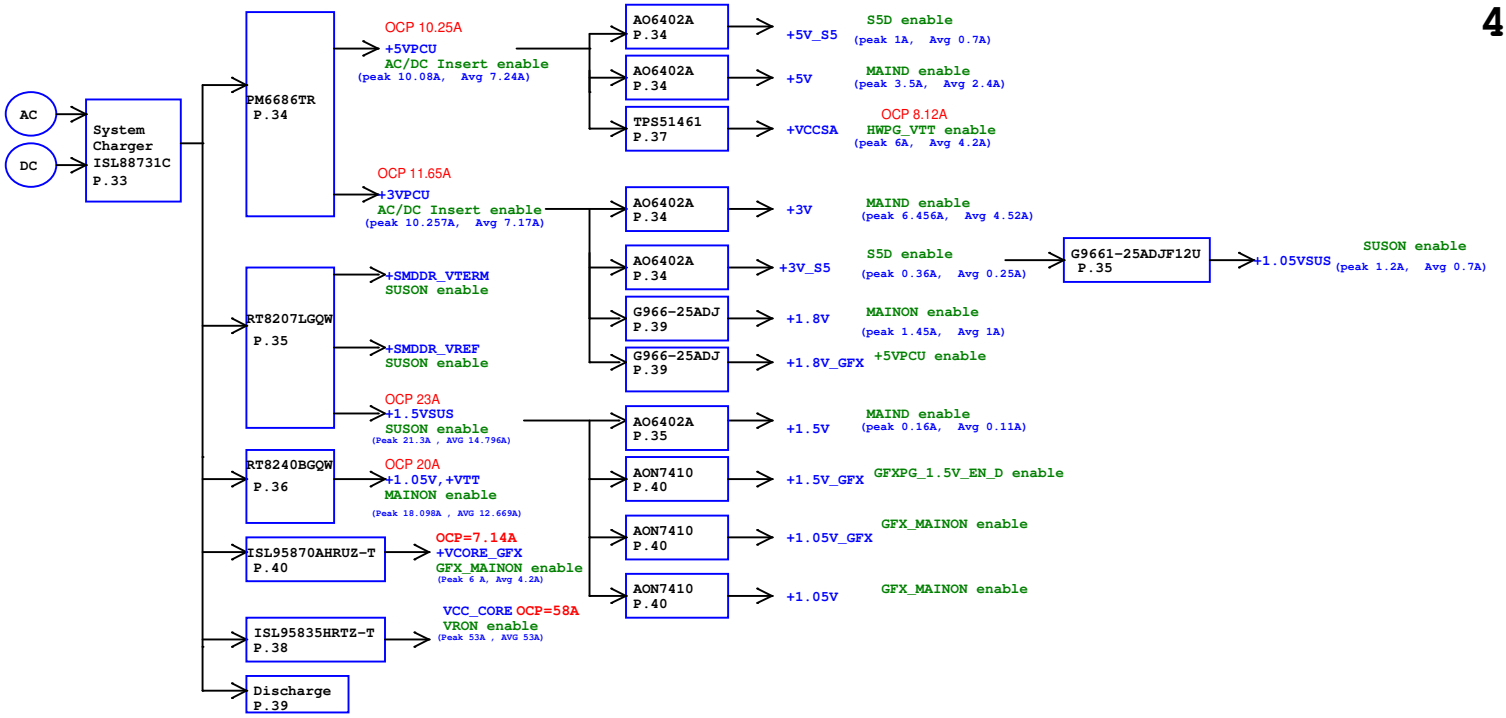

Quanta Computer Inc.
PROJECT : BU5D
Size | Document Number: POWER TREE TABLE | Rev: 1A
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