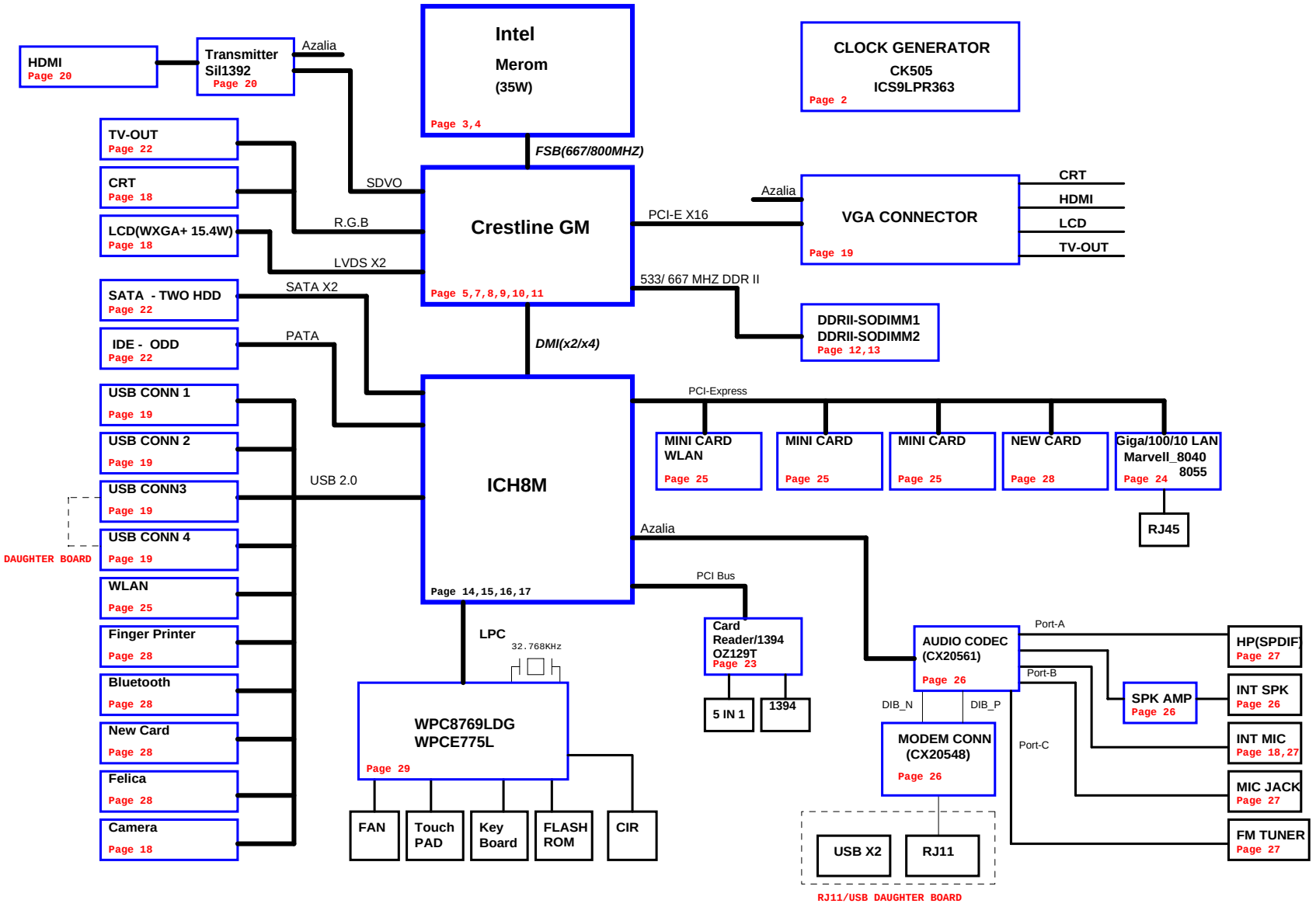
BL5S Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

- VCC_CORE
- +1.5V
- +1.05V
- +1.25V
- +1.8VSUS
- +3VPCU
  +3V_S5
  +3VSUS
  +3V
  +5VPCU
  +5V_S5
  +5V
  SMDDR_VTERM
  SMDDR_VREF

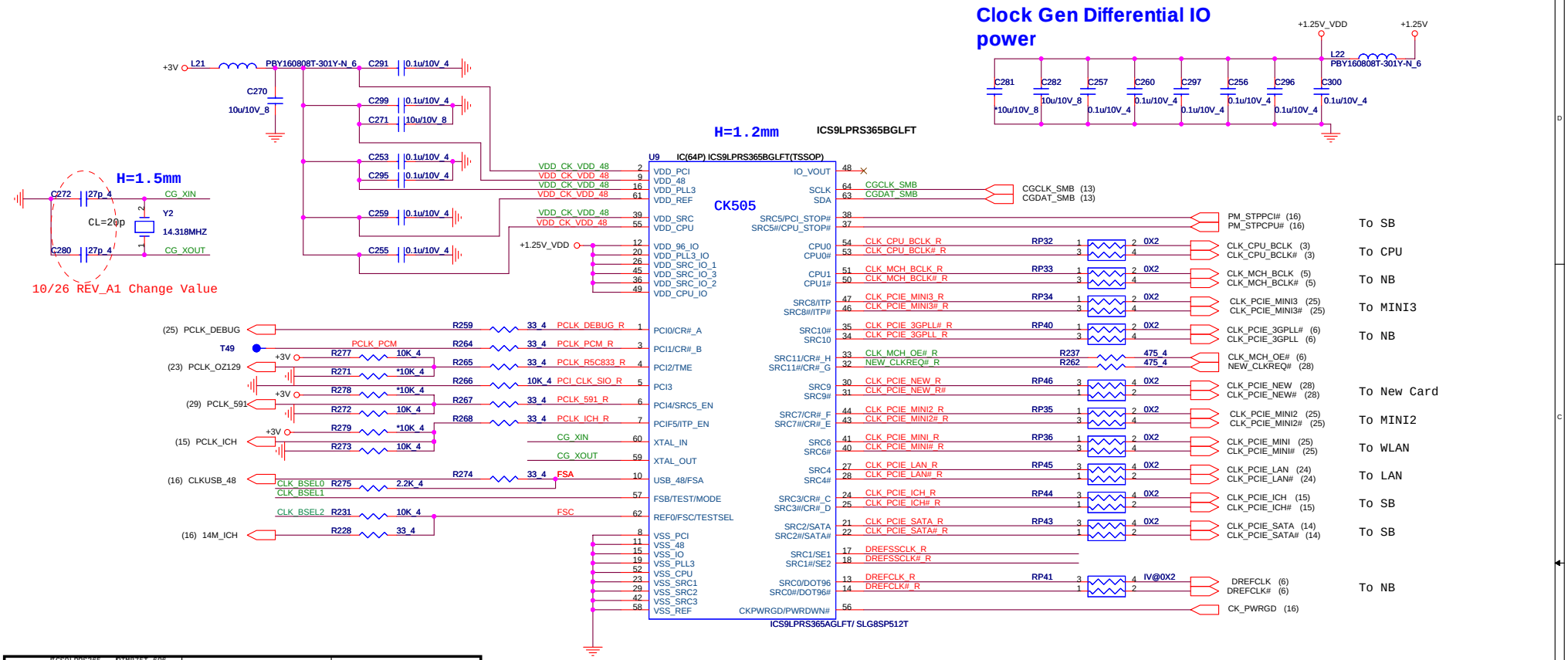


Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	Block Diagram	1A

Date: Tuesday, January 22, 2008 Sheet 1 of 37

Clock Generator



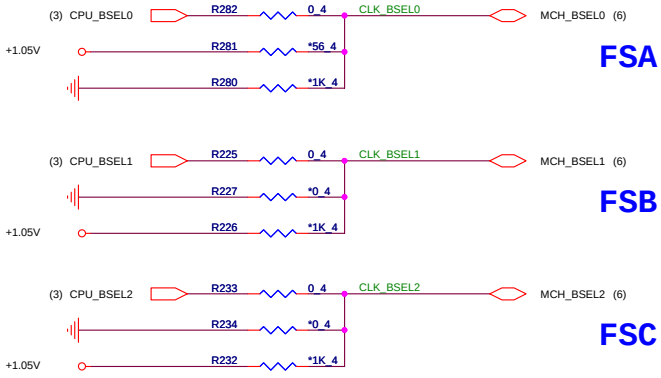
Clock Gen Differential IO power

	ICS9LPRS365 (ALPRS365K13)	RTM8751-606 (AL000875K06)	PULL HIGH	PULL DOWN
Pin 4	PCI2/TME	PCI2/TME internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 5	PCI-3	PCI-3/SRC5_EN internal PD	PIN37/38 IS SRC5	PIN37/38 IS PCI_STOP/CPU_STOP (default)
Pin 6	PCI-4/27M_SEL	PCI-4/27M_SEL internal PD	PIN 17/18 IS 27MHz	PIN 17/18 IS SRC/DOT (default)
Pin 7	PCIF-5/ITP_EN	PCIF-5/ITP_EN internal PD	PIN 46/47 IS CPUITP	PIN 46/47 IS SRC8 (default)

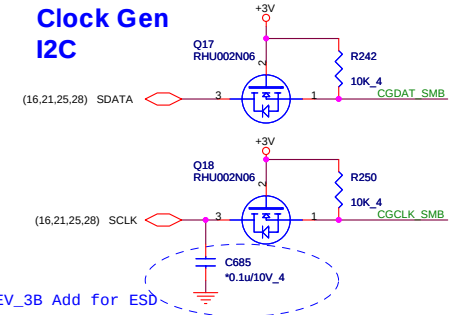
CPU Clock select

BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



Clock Gen I2C



Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	CLK. GEN./ CK505	1A

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CPU(HOST)

U22A

ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED

(5) H_A#[16:3]
H_A#3 J4 A[3]#
H_A#4 L5 A[4]#
H_A#5 L4 A[5]#
H_A#6 K5 A[6]#
H_A#7 M3 A[7]#
H_A#8 N2 A[8]#
H_A#9 J1 A[9]#
H_A#10 N3 A[10]#
H_A#11 P5 A[11]#
H_A#12 P2 A[12]#
H_A#13 L2 A[13]#
H_A#14 P4 A[14]#
H_A#15 P1 A[15]#
H_A#16 R1 A[16]#
(5) H_ADSTB0# M1 ADSTB[0]#
(5) H_REQ#[4:0]
H_REQ#0 K3 REQ[0]#
H_REQ#1 H2 REQ[1]#
H_REQ#2 K2 REQ[2]#
H_REQ#3 J3 REQ[3]#
H_REQ#4 L1 REQ[4]#
(5) H_A#[35:17]
H_A#17 Y2 A[17]#
H_A#18 U5 A[18]#
H_A#19 R3 A[19]#
H_A#20 W6 A[20]#
H_A#21 U4 A[21]#
H_A#22 Y5 A[22]#
H_A#23 U1 A[23]#
H_A#24 R4 A[24]#
H_A#25 T5 A[25]#
H_A#26 T3 A[26]#
H_A#27 W2 A[27]#
H_A#28 W5 A[28]#
H_A#29 Y4 A[29]#
H_A#30 U2 A[30]#
H_A#31 V4 A[31]#
H_A#32 W3 A[32]#
H_A#33 AA4 A[33]#
H_A#34 AB2 A[34]#
H_A#35 AA3 A[35]#
(5) H_ADSTB1# V1 ADSTB[1]#
(14) H_A20M# A6 A20M#
(14) H_FERR# A5 FERR#
(14) H_IGNNE# C4 IGNNE#
(14) H_STPCLK# D5 STPCLK#
(14) H_INTR C6 LINT0
(14) H_NMI B4 LINT1
(14) H_SMI# A3 SMI#
M4 RSVD[01]
N5 RSVD[02]
T2 RSVD[03]
V3 RSVD[04]
B2 RSVD[05]
C3 RSVD[06]
D2 RSVD[07]
D22 RSVD[08]
D3 RSVD[09]
F6 RSVD[10]

ADS# H1 → H_ADS# (5)
BNR# E2 → H_BNR# (5)
BPRI# G5 → H_BPRI# (5)
DEFER# H5 → H_DEFER# (5)
DRDY# F21 → H_DRDY# (5)
DBSY# E1 → H_DBSY# (5)
BR0# F1 → H_BREQ#0 (5)
IERR# D20 — H_IERR# — R40 56.2_4 — +1.05V
INIT# B3 → H_INIT# (14)
LOCK# H4 → H_LOCK# (5)
RESET# C1 → H_CPURST# (5)
RS[0]# F3 → H_RS#0 (5)
RS[1]# F4 → H_RS#1 (5)
RS[2]# G3 → H_RS#2 (5)
TRDY# G2 → H_TRDY# (5)
HIT# G6 → H_HIT# (5)
HITM# E4 → H_HITM# (5)

12/06 REV_3A Add C666
H_CPURST# — C666 0.1u/10V_4

BPM[0]# AD4 → T28
BPM[1]# AD3 → T25
BPM[2]# AD1 → T26
BPM[3]# AC4 → T27
PRDY# AC2 → T24
PREQ# AC1 → T29
TCK AC5 XDP_TCK
TDI AA6 XDP_TDI
TDO AB3 → T77
TMS AB5 XDP_TMS
TRST# AB6 XDP_TRST#
DBR# C20 XDP_DBRESET# — R43 0_4 — SYS_RST# (16)

01/17 REV_3B Add C674
C674 0.1u/10V_4

PROCHOT# D21 H_PROCHOT_R# — R41 56.2_4 — +1.05V; R42 *2.2K_4 — H_PROCHOT# (32)
THERMDA A24 H_THERMDA
THERMDC B25 H_THERMDC
THERMTRIP# C7 THERMTRIP#_PWR

BCLK[0] A22 → CLK_CPU_BCLK (2)
BCLK[1] A21 → CLK_CPU_BCLK# (2)

Merom Ball-out Rev 1a

U22B

DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC

(5) H_D#[15:0]
H_D#0 E22 D[0]#
H_D#1 F24 D[1]#
H_D#2 E26 D[2]#
H_D#3 G22 D[3]#
H_D#4 F23 D[4]#
H_D#5 G25 D[5]#
H_D#6 E25 D[6]#
H_D#7 E23 D[7]#
H_D#8 K24 D[8]#
H_D#9 G24 D[9]#
H_D#10 J24 D[10]#
H_D#11 J23 D[11]#
H_D#12 H22 D[12]#
H_D#13 F26 D[13]#
H_D#14 K22 D[14]#
H_D#15 H23 D[15]#
(5) H_DSTBN#0 J26 DSTBN[0]#
(5) H_DSTBP#0 H26 DSTBP[0]#
(5) H_DINV#0 H25 DINV[0]#

D[32]# Y22 → H_D#32
D[33]# AB24 → H_D#33
D[34]# V24 → H_D#34
D[35]# V26 → H_D#35
D[36]# V23 → H_D#36
D[37]# T22 → H_D#37
D[38]# U25 → H_D#38
D[39]# U23 → H_D#39
D[40]# Y25 → H_D#40
D[41]# W22 → H_D#41
D[42]# Y23 → H_D#42
D[43]# W24 → H_D#43
D[44]# W25 → H_D#44
D[45]# AA23 → H_D#45
D[46]# AA24 → H_D#46
D[47]# AB25 → H_D#47
DSTBN[2]# Y26 → H_DSTBN#2 (5)
DSTBP[2]# AA26 → H_DSTBP#2 (5)
DINV[2]# U22 → H_DINV#2 (5)

H_D#[47:32] (5)
H_D#[63:48] (5)

(5) H_D#[31:16]
H_D#16 N22 D[16]#
H_D#17 K25 D[17]#
H_D#18 P26 D[18]#
H_D#19 R23 D[19]#
H_D#20 L23 D[20]#
H_D#21 M24 D[21]#
H_D#22 L22 D[22]#
H_D#23 M23 D[23]#
H_D#24 P25 D[24]#
H_D#25 P23 D[25]#
H_D#26 P22 D[26]#
H_D#27 T24 D[27]#
H_D#28 R24 D[28]#
H_D#29 L25 D[29]#
H_D#30 T25 D[30]#
H_D#31 N25 D[31]#
(5) H_DSTBN#1 L26 DSTBN[1]#
(5) H_DSTBP#1 M26 DSTBP[1]#
(5) H_DINV#1 N24 DINV[1]#

D[48]# AE24 → H_D#48
D[49]# AD24 → H_D#49
D[50]# AA21 → H_D#50
D[51]# AB22 → H_D#51
D[52]# AB21 → H_D#52
D[53]# AC26 → H_D#53
D[54]# AD20 → H_D#54
D[55]# AE22 → H_D#55
D[56]# AE23 → H_D#56
D[57]# AC25 → H_D#57
D[58]# AE21 → H_D#58
D[59]# AD21 → H_D#59
D[60]# AC22 → H_D#60
D[61]# AD23 → H_D#61
D[62]# AF22 → H_D#62
D[63]# AC23 → H_D#63
DSTBN[3]# AE25 → H_DSTBN#3 (5)
DSTBP[3]# AF24 → H_DSTBP#3 (5)
DINV[3]# AC20 → H_DINV#3 (5)

+1.05V — R51 1K/F_4 — R50 2K/F_6

H_GTLREF AD26 — R45 *1K_4 — R44 *1K_4
CPU_TEST1 C23
CPU_TEST2 D25
CPU_TEST3 C24
CPU_TEST4 AE26
CPU_TEST5 AF1
CPU_TEST6 A26
T9 T73 T23 T8

(2) CPU_BSEL0 B22
(2) CPU_BSEL1 B23
(2) CPU_BSEL2 C21
BSEL[0] BSEL[1] BSEL[2]

COMP[0] R26 — COMP0 R49 27.4/F_6
COMP[1] U26 — COMP1 R48 54.9/F_4
COMP[2] AA1 — COMP2 R170 27.4/F_6
COMP[3] Y1 — COMP3 R173 54.9/F_4

DPRSTP# E5 → ICH_DPRSTP# (6,14,32)
DPSLP# B5 → H_DPSLP# (14)
DPWR# D24 → H_DPWR# (5)
PWRGOOD D6 → H_PWRGD (14)
SLP# D7 → H_CPUSLP# (5)
PSI# AE6 → PSI# (32)

Merom Ball-out Rev 1a

CPU Thermal monitor

U19 LM95245
THERM_MBCLK 8 SCLK — VCC 1 LM86VCC
THERM_MBDATA 7 SDA — DXP 2 H_THERMDA
THERM_ALERT#_R 6 ALERT# — DXN 3 H_THERMDC
THER_SHD# 4 OVERT# — GND 5

01/17 REV_3B mount C666

+3V
Q37 RHU002N06
(29) 2ND_MBCLK — THERM_MBCLK
Q38 RHU002N06
(29) 2ND_MBDATA — THERM_MBDATA
R440 10K_4 R438 10K_4 R445 200_6 LM86VCC
C458 0.1u/10V_4
C459 2200p_4
H=1.75mm
U20 *MAX6657 ADDRESS: 98H
SCLK VCC SDA DXP ALERT# DXN OVERT# GND
H_THERMDA H_THERMDC

10/22 REV_A1 Mount R434
+3V — R434 10K_4
(16) THERM_ALERT# — R435 *0_4 — THERM_ALERT#_R
+3V — R436 10K_4 — THER_SHD#

CPU FAN

10/29 REV_A1 Add for ESD
10/26 REV_A1 Add for ESD

+3V — R431 330_4 — Q36 MMBT3904
THER_SHD# — SYS_SHDN# (31)

+5V — C433 2.2u/6.3V_6 — R415 0_4
(19) SYSFANON#
(29) VFAN
H=1.75mm
U17 G995
VIN VO /FON GND VSET GND
C436 10u/10V_8 C434 0.01u_4
TH_FAN_POWER
FANPWR = 1.6*VSET

(29) FANSIG
VPORT_6 D49 — R423 10K_4 — *VPORT_6 D50
D44 VPORT_6 C440 *0.01u_4
CN17 PTI_CWY030-B0G1Z
12/04 REV_3A DNI C440

PU/PD (ITP700)

+1.05V
XDP_TMS R174 39_4
XDP_TDI R175 150_4
XDP_TCK R171 27_4
XDP_TRST# R172 680_4

Thermal Trip

+1.05V
10/22 REV_A1 Del C452,Add R614
(6,16,32) DELAY_VR_PWRGOOD
Q39 FDV301N — R437 *10K_4 — D36 *BAS316 — R614 100K_6
R439 56.2_4
R613 1K_4
10/22 REV_A1 Add R613
Q40 MMBT3904
THERMTRIP# PWR — SYS_SHDN# (31)
R442 *0_4 — PM_THRMTRIP# (6,14)

Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
Size | Document Number: CPU(1 of 2)/FAN/Thermal | Rev 1A
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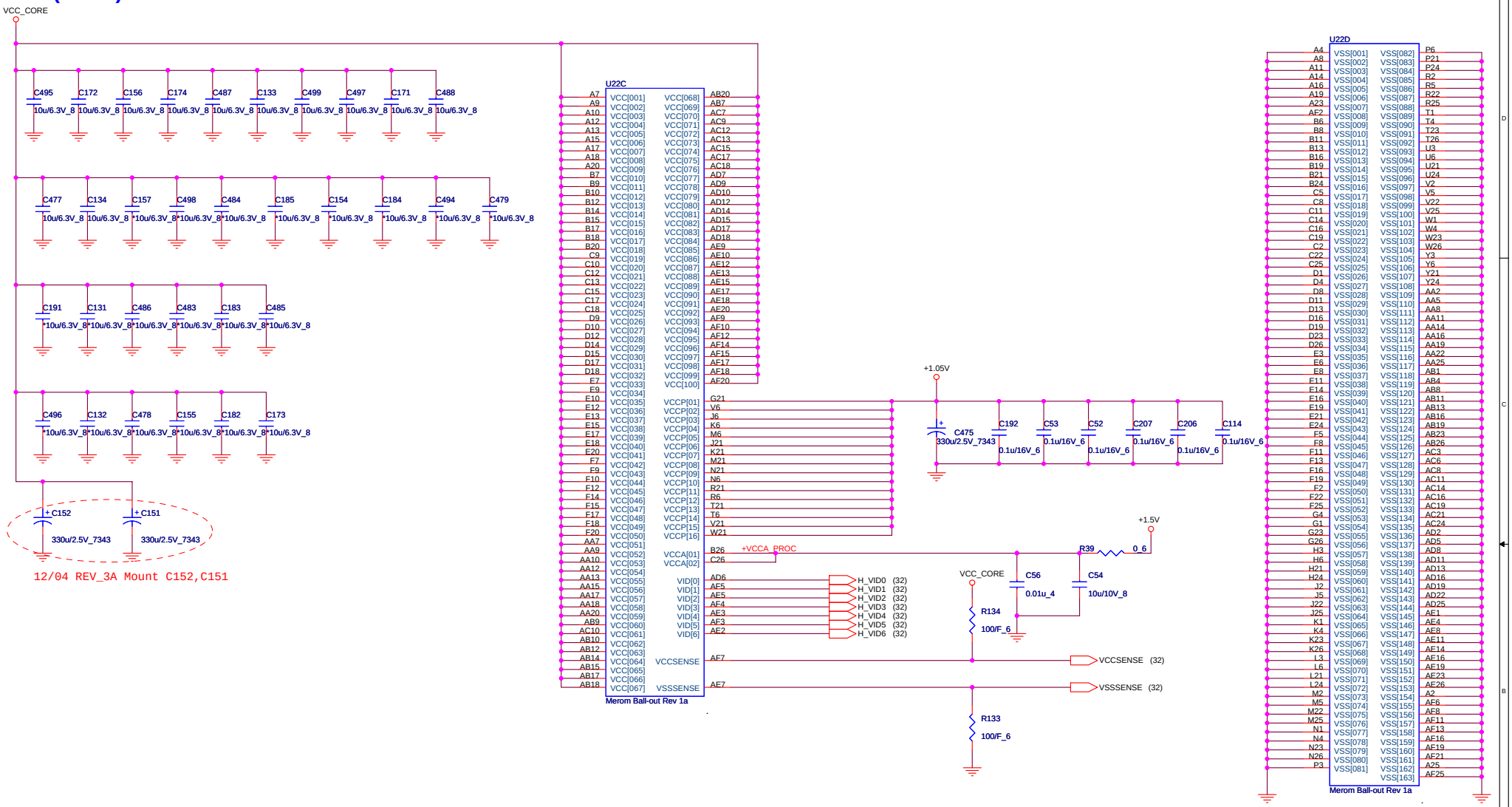
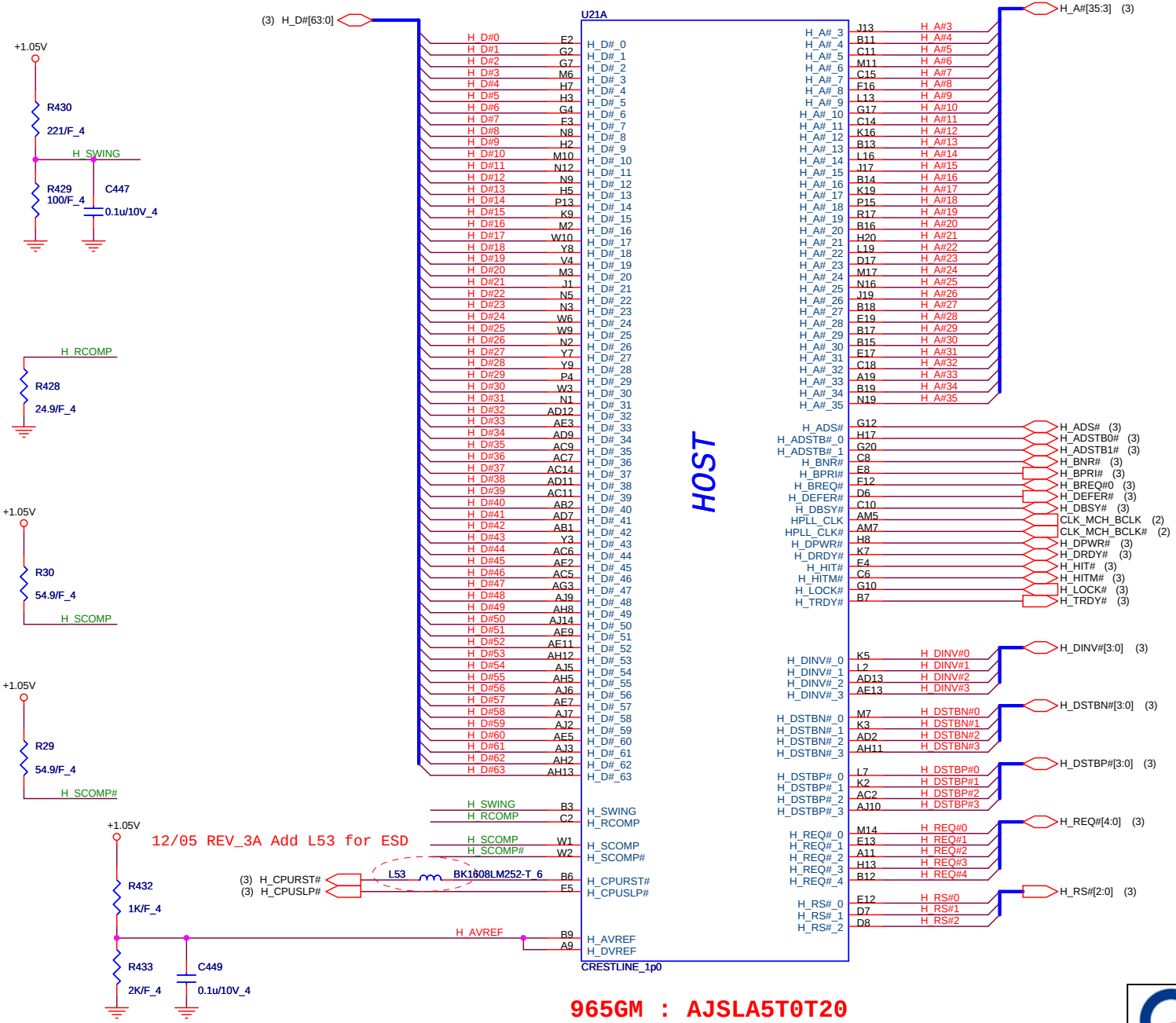
CPU(Power)



Quanta Computer Inc.		
PROJECT : BL5S Santa Rosa		
Size	Document Number: CPU(2 of 2)	Rev: 1A
Date: Tuesday, January 22, 2008	Sheet 4 of 37	

NB(HOST)



965GM : AJSLA5T0T20
965PM : AJSLA5U0T25
960GL : AJSLA5V0T09

Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	GMCH HOST(1 of 7)	1A
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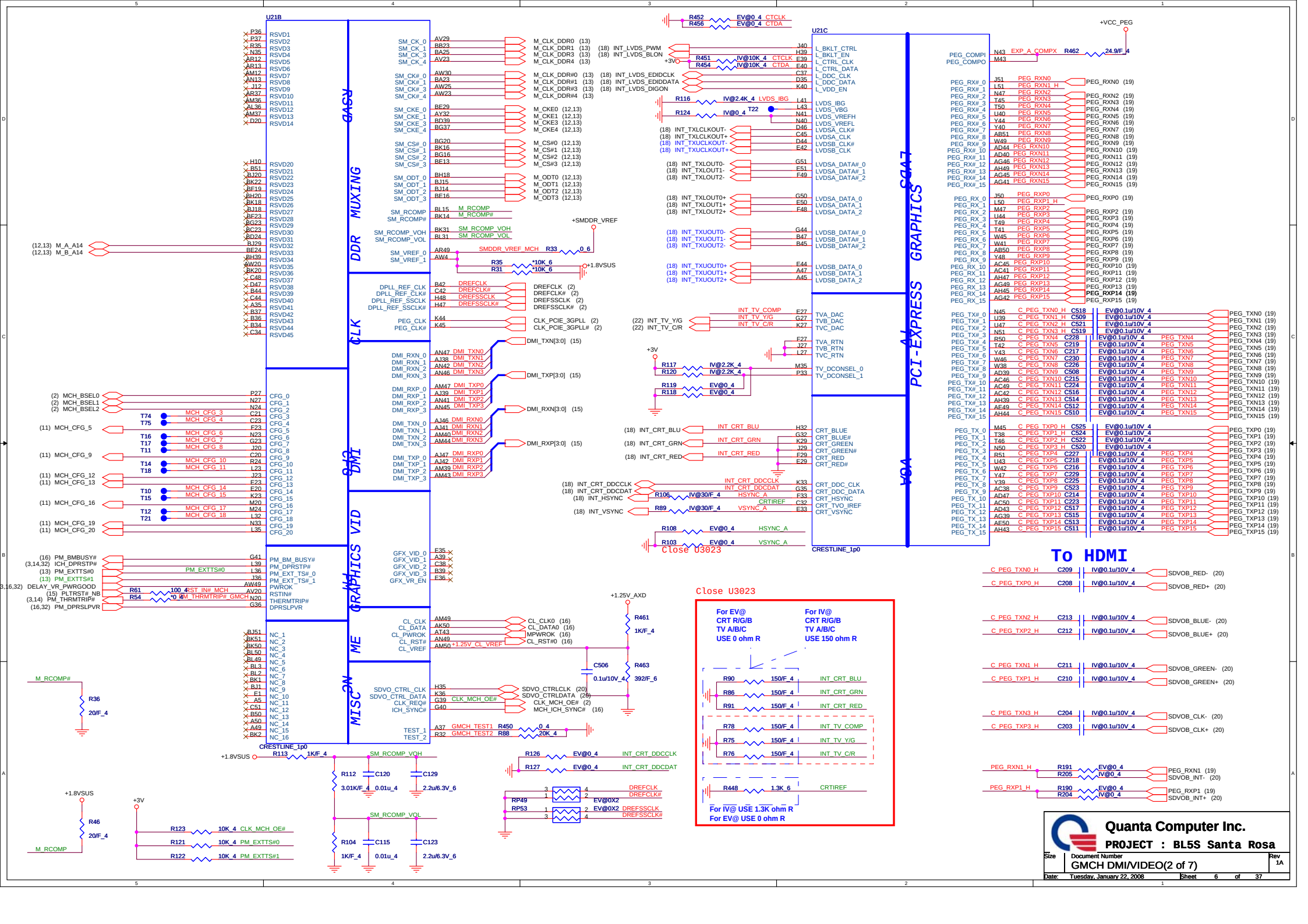
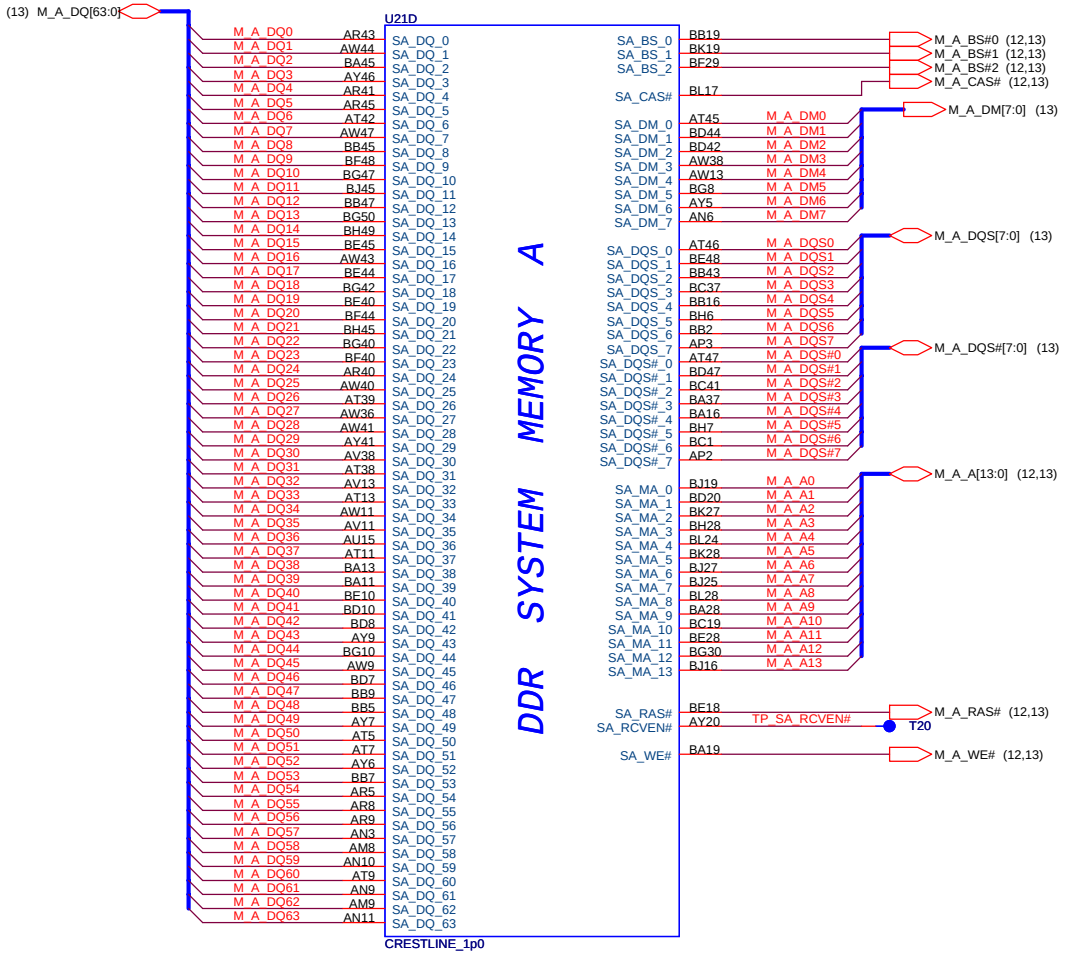
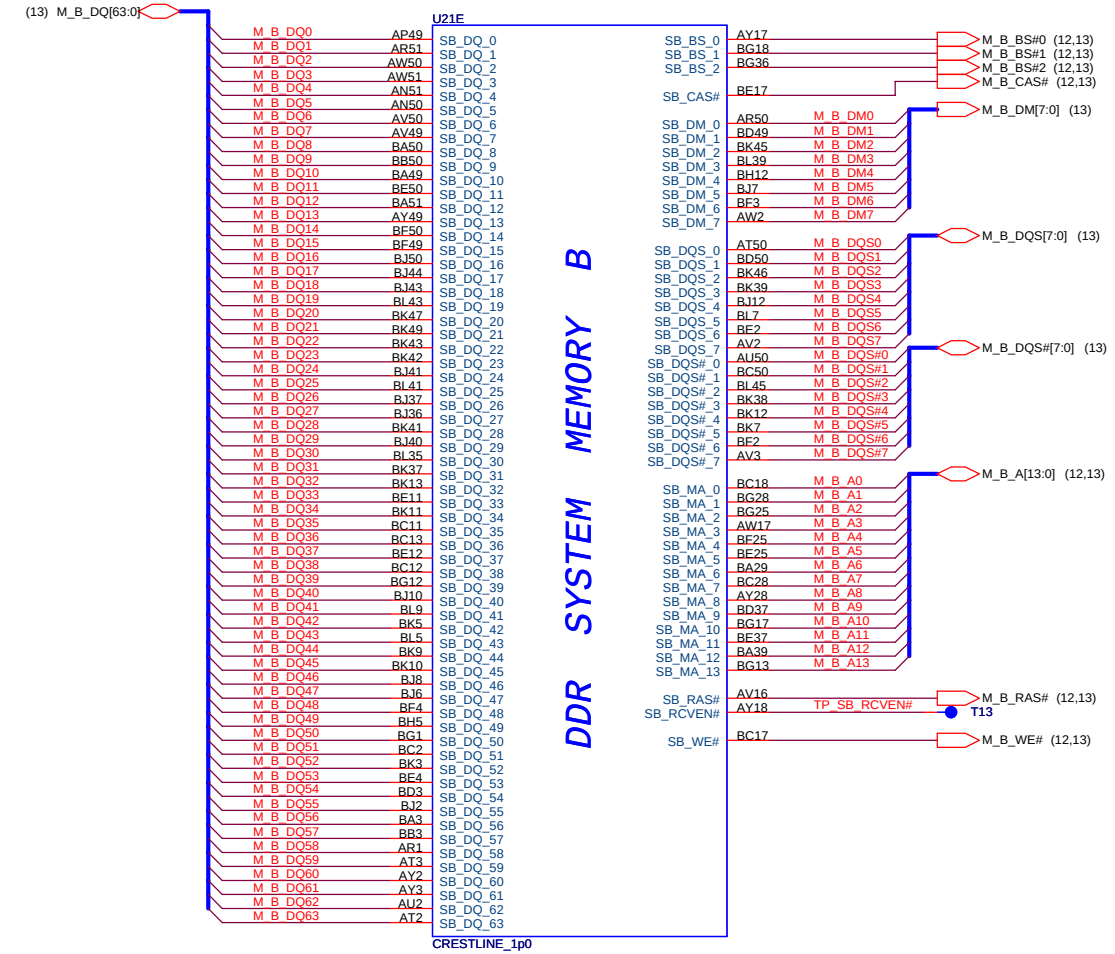

U21B
U21C
EASY
DDR MUXING
CLK
DMI
GRAPHICS VID
MISC
PCI-EXPRESS GRAPHICS
CRESTLINE_1p0
Close U3023
To HDMI
For EV@ CRT R/G/B TV A/B/C USE 0 ohm R
For IV@ CRT R/G/B TV A/B/C USE 150 ohm R
For IV@ USE 1.3K ohm R
For EV@ USE 0 ohm R
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
GMCH DMI/VIDEO(2 of 7)
Tuesday, January 22, 2008
Sheet 6 of 37

NB(Memory controller)





Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	MCH DDR(3 of 7)	1A

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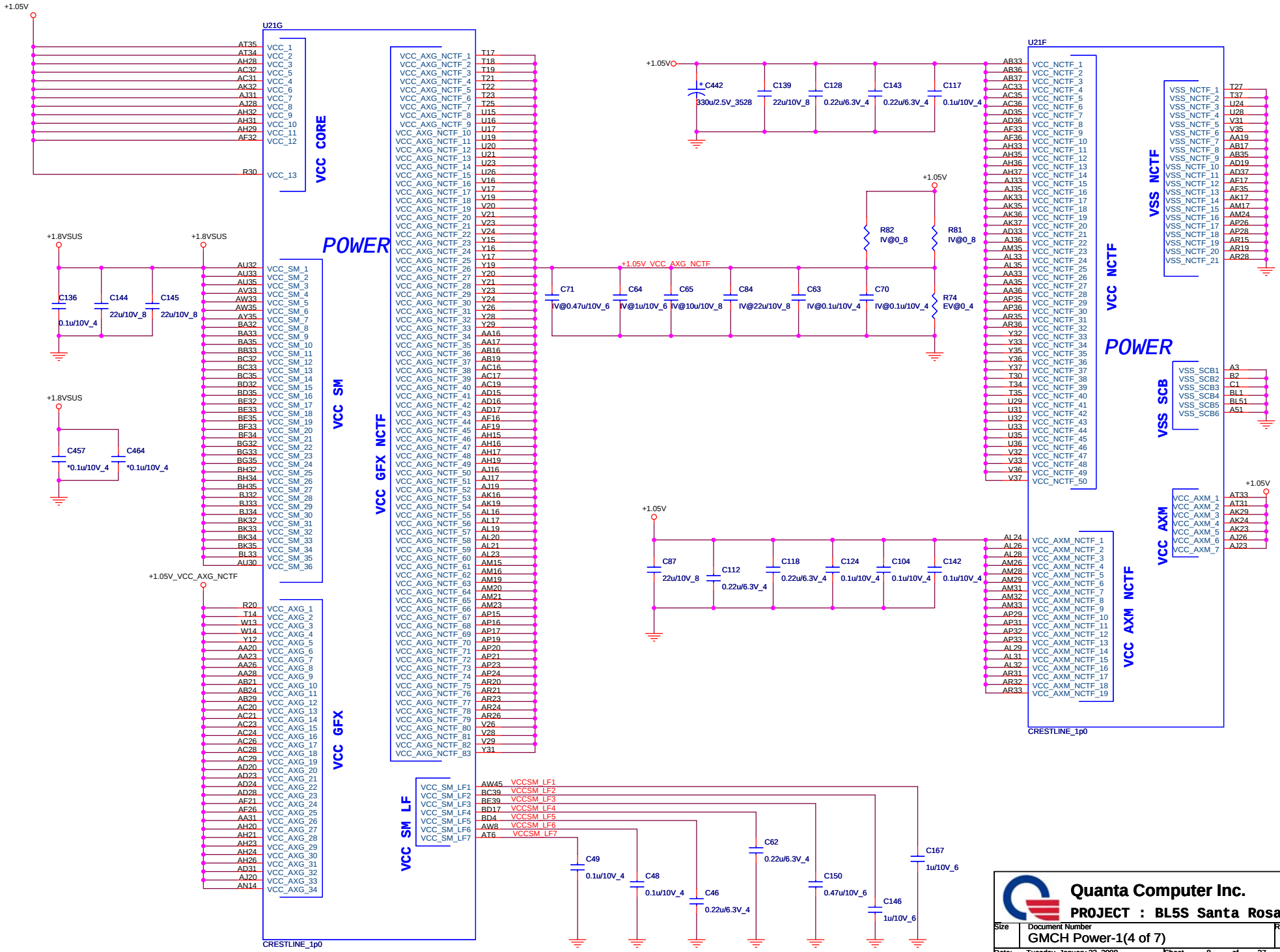
NB(Power-1)


+1.05V
U21G
VCC CORE
VCC_1
VCC_2
VCC_3
VCC_5
VCC_4
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
VCC_11
VCC_12
VCC_13
R30
POWER
+1.8VSUS
C136
0.1u/10V_4
C144
22u/10V_8
C145
22u/10V_8
VCC SM
VCC_SM_1
VCC_SM_2
VCC_SM_3
VCC_SM_4
VCC_SM_5
VCC_SM_6
VCC_SM_7
VCC_SM_8
VCC_SM_9
VCC_SM_10
VCC_SM_11
VCC_SM_12
VCC_SM_13
VCC_SM_14
VCC_SM_15
VCC_SM_16
VCC_SM_17
VCC_SM_18
VCC_SM_19
VCC_SM_20
VCC_SM_21
VCC_SM_22
VCC_SM_23
VCC_SM_24
VCC_SM_25
VCC_SM_26
VCC_SM_27
VCC_SM_28
VCC_SM_29
VCC_SM_30
VCC_SM_31
VCC_SM_32
VCC_SM_33
VCC_SM_34
VCC_SM_35
VCC_SM_36
C457
*0.1u/10V_4
C464
*0.1u/10V_4
+1.05V_VCC_AXG_NCTF
VCC GFX
VCC_AXG_1
VCC_AXG_2
VCC_AXG_3
VCC_AXG_4
VCC_AXG_5
VCC_AXG_6
VCC_AXG_7
VCC_AXG_8
VCC_AXG_9
VCC_AXG_10
VCC_AXG_11
VCC_AXG_12
VCC_AXG_13
VCC_AXG_14
VCC_AXG_15
VCC_AXG_16
VCC_AXG_17
VCC_AXG_18
VCC_AXG_19
VCC_AXG_20
VCC_AXG_21
VCC_AXG_22
VCC_AXG_23
VCC_AXG_24
VCC_AXG_25
VCC_AXG_26
VCC_AXG_27
VCC_AXG_28
VCC_AXG_29
VCC_AXG_30
VCC_AXG_31
VCC_AXG_32
VCC_AXG_33
VCC_AXG_34
VCC GFX NCTF
VCC_AXG_NCTF_1
VCC_AXG_NCTF_2
VCC_AXG_NCTF_3
VCC_AXG_NCTF_4
VCC_AXG_NCTF_5
VCC_AXG_NCTF_6
VCC_AXG_NCTF_7
VCC_AXG_NCTF_8
VCC_AXG_NCTF_9
VCC_AXG_NCTF_10
VCC_AXG_NCTF_11
VCC_AXG_NCTF_12
VCC_AXG_NCTF_13
VCC_AXG_NCTF_14
VCC_AXG_NCTF_15
VCC_AXG_NCTF_16
VCC_AXG_NCTF_17
VCC_AXG_NCTF_18
VCC_AXG_NCTF_19
VCC_AXG_NCTF_20
VCC_AXG_NCTF_21
VCC_AXG_NCTF_22
VCC_AXG_NCTF_23
VCC_AXG_NCTF_24
VCC_AXG_NCTF_25
VCC_AXG_NCTF_26
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VCC_AXG_NCTF_37
VCC_AXG_NCTF_38
VCC_AXG_NCTF_39
VCC_AXG_NCTF_40
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VCC_AXG_NCTF_45
VCC_AXG_NCTF_46
VCC_AXG_NCTF_47
VCC_AXG_NCTF_48
VCC_AXG_NCTF_49
VCC_AXG_NCTF_50
VCC_AXG_NCTF_51
VCC_AXG_NCTF_52
VCC_AXG_NCTF_53
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VCC_AXG_NCTF_59
VCC_AXG_NCTF_60
VCC_AXG_NCTF_61
VCC_AXG_NCTF_62
VCC_AXG_NCTF_63
VCC_AXG_NCTF_64
VCC_AXG_NCTF_65
VCC_AXG_NCTF_66
VCC_AXG_NCTF_67
VCC_AXG_NCTF_68
VCC_AXG_NCTF_69
VCC_AXG_NCTF_70
VCC_AXG_NCTF_71
VCC_AXG_NCTF_72
VCC_AXG_NCTF_73
VCC_AXG_NCTF_74
VCC_AXG_NCTF_75
VCC_AXG_NCTF_76
VCC_AXG_NCTF_77
VCC_AXG_NCTF_78
VCC_AXG_NCTF_79
VCC_AXG_NCTF_80
VCC_AXG_NCTF_81
VCC_AXG_NCTF_82
VCC_AXG_NCTF_83
VCC SM LF
VCC_SM_LF1
VCC_SM_LF2
VCC_SM_LF3
VCC_SM_LF4
VCC_SM_LF5
VCC_SM_LF6
VCC_SM_LF7
VCCSM_LF1
VCCSM_LF2
VCCSM_LF3
VCCSM_LF4
VCCSM_LF5
VCCSM_LF6
VCCSM_LF7
C49
0.1u/10V_4
C48
0.1u/10V_4
C46
0.22u/6.3V_4
C62
0.22u/6.3V_4
C150
0.47u/10V_6
C146
1u/10V_6
C167
1u/10V_6
CRESTLINE_1p0
+1.05V_VCC_AXG_NCTF
C71
IV@0.47u/10V_6
C64
IV@1u/10V_6
C65
IV@10u/10V_8
C84
IV@22u/10V_8
C63
IV@0.1u/10V_4
C70
IV@0.1u/10V_4
R82
IV@0_8
R81
IV@0_8
R74
EV@0_4
+1.05V
C442
330u/2.5V_3528
C139
22u/10V_8
C128
0.22u/6.3V_4
C143
0.22u/6.3V_4
C117
0.1u/10V_4
U21F
VCC_NCTF_1
VCC_NCTF_2
VCC_NCTF_3
VCC_NCTF_4
VCC_NCTF_5
VCC_NCTF_6
VCC_NCTF_7
VCC_NCTF_8
VCC_NCTF_9
VCC_NCTF_10
VCC_NCTF_11
VCC_NCTF_12
VCC_NCTF_13
VCC_NCTF_14
VCC_NCTF_15
VCC_NCTF_16
VCC_NCTF_17
VCC_NCTF_18
VCC_NCTF_19
VCC_NCTF_20
VCC_NCTF_21
VCC_NCTF_22
VCC_NCTF_23
VCC_NCTF_24
VCC_NCTF_25
VCC_NCTF_26
VCC_NCTF_27
VCC_NCTF_28
VCC_NCTF_29
VCC_NCTF_30
VCC_NCTF_31
VCC_NCTF_32
VCC_NCTF_33
VCC_NCTF_34
VCC_NCTF_35
VCC_NCTF_36
VCC_NCTF_37
VCC_NCTF_38
VCC_NCTF_39
VCC_NCTF_40
VCC_NCTF_41
VCC_NCTF_42
VCC_NCTF_43
VCC_NCTF_44
VCC_NCTF_45
VCC_NCTF_46
VCC_NCTF_47
VCC_NCTF_48
VCC_NCTF_49
VCC_NCTF_50
VCC NCTF
VSS NCTF
VSS_NCTF_1
VSS_NCTF_2
VSS_NCTF_3
VSS_NCTF_4
VSS_NCTF_5
VSS_NCTF_6
VSS_NCTF_7
VSS_NCTF_8
VSS_NCTF_9
VSS_NCTF_10
VSS_NCTF_11
VSS_NCTF_12
VSS_NCTF_13
VSS_NCTF_14
VSS_NCTF_15
VSS_NCTF_16
VSS_NCTF_17
VSS_NCTF_18
VSS_NCTF_19
VSS_NCTF_20
VSS_NCTF_21
POWER
VSS SCB
VSS_SCB1
VSS_SCB2
VSS_SCB3
VSS_SCB4
VSS_SCB5
VSS_SCB6
C87
22u/10V_8
C112
0.22u/6.3V_4
C118
0.22u/6.3V_4
C124
0.1u/10V_4
C104
0.1u/10V_4
C142
0.1u/10V_4
VCC AXM NCTF
VCC_AXM_NCTF_1
VCC_AXM_NCTF_2
VCC_AXM_NCTF_3
VCC_AXM_NCTF_4
VCC_AXM_NCTF_5
VCC_AXM_NCTF_6
VCC_AXM_NCTF_7
VCC_AXM_NCTF_8
VCC_AXM_NCTF_9
VCC_AXM_NCTF_10
VCC_AXM_NCTF_11
VCC_AXM_NCTF_12
VCC_AXM_NCTF_13
VCC_AXM_NCTF_14
VCC_AXM_NCTF_15
VCC_AXM_NCTF_16
VCC_AXM_NCTF_17
VCC_AXM_NCTF_18
VCC_AXM_NCTF_19
VCC AXM
VCC_AXM_1
VCC_AXM_2
VCC_AXM_3
VCC_AXM_4
VCC_AXM_5
VCC_AXM_6
VCC_AXM_7
CRESTLINE_1p0
Quanta Computer Inc.
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NB(Power-2)

CRT/TV Disable/Enable guideline

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TVO	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TVO	3.3V	GND	VSSABG_DAC	GND	GND
VCCA_B_TVO	3.3V	GND	VCC_SYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V

EXTERNAL INTERNAL

IV&EV Dis/Enable setting

IV&EV Dis/Enable setting

IV&EV Dis/Enable setting

IV&EV Dis/Enable setting

U21H

CRESTLINE_1p0

POWER

<FAE>
INT VGA disable
VCCD_TVDAC still
+1.5V

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GMCH Power-2(5 of 7)
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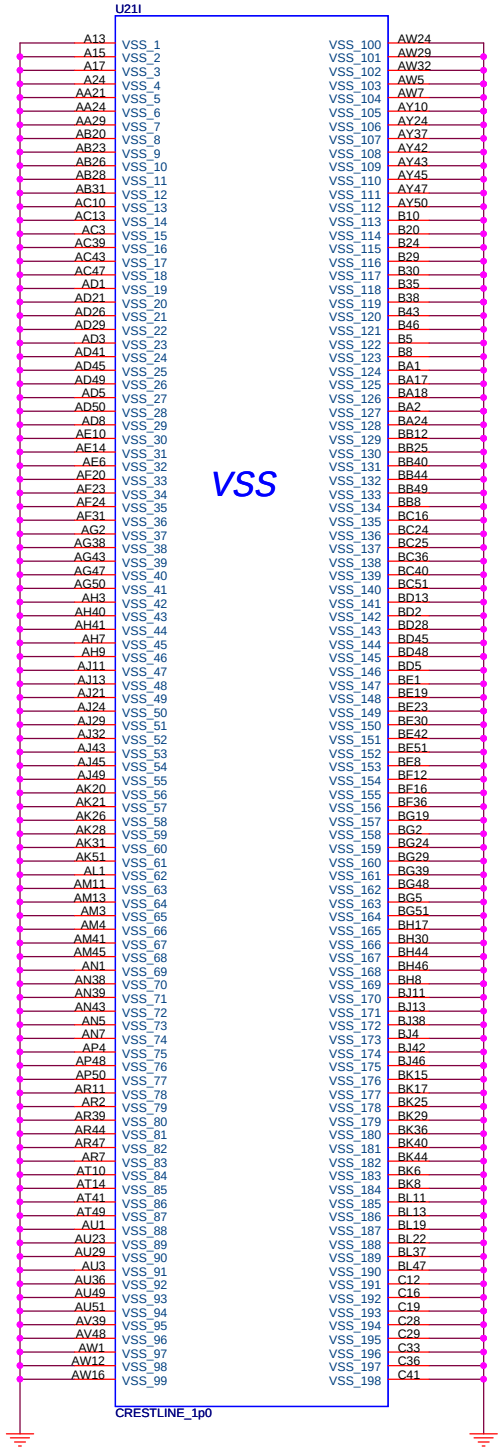
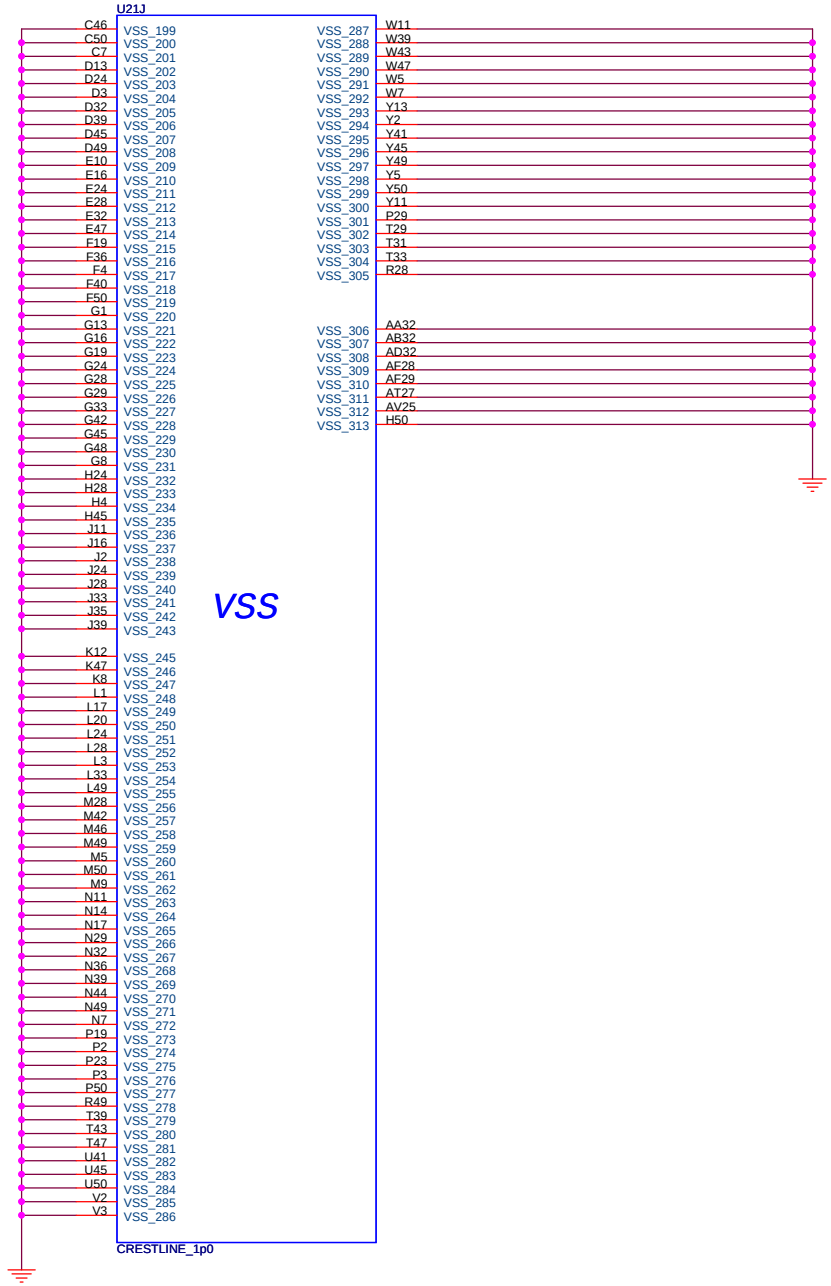
NB(Power-3)





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PROJECT : BL5S Santa Rosa		
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Strap table

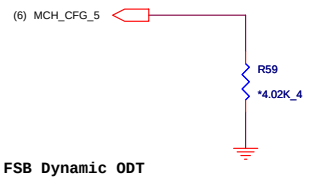
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

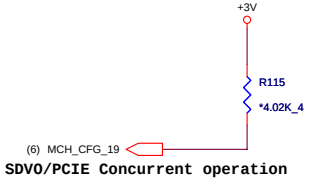
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane

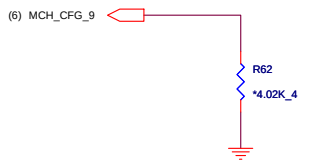


XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

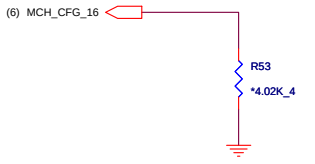


SDVO Present

Strap define at External DVI control page

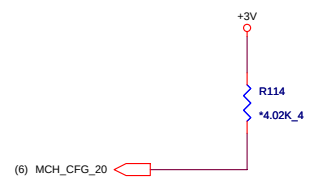
FSB Dynamic ODT

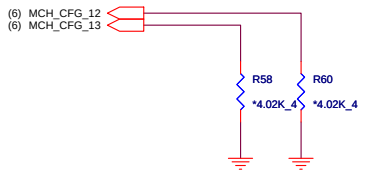
MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port





Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	GMCH Strap(7 of 7)	1A

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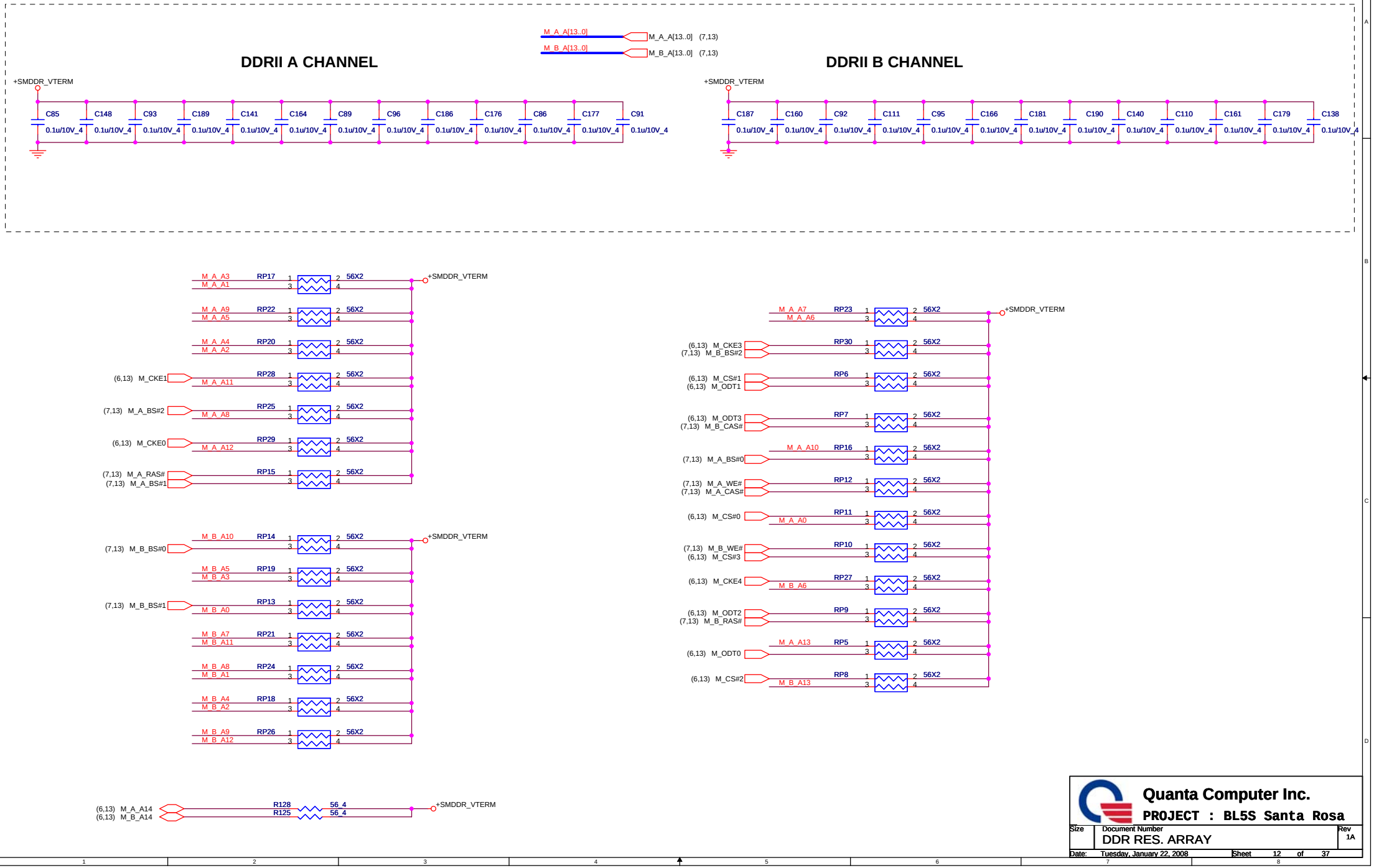
DDR2 Dual channel A/B PU



Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	DDR RES. ARRAY	1A

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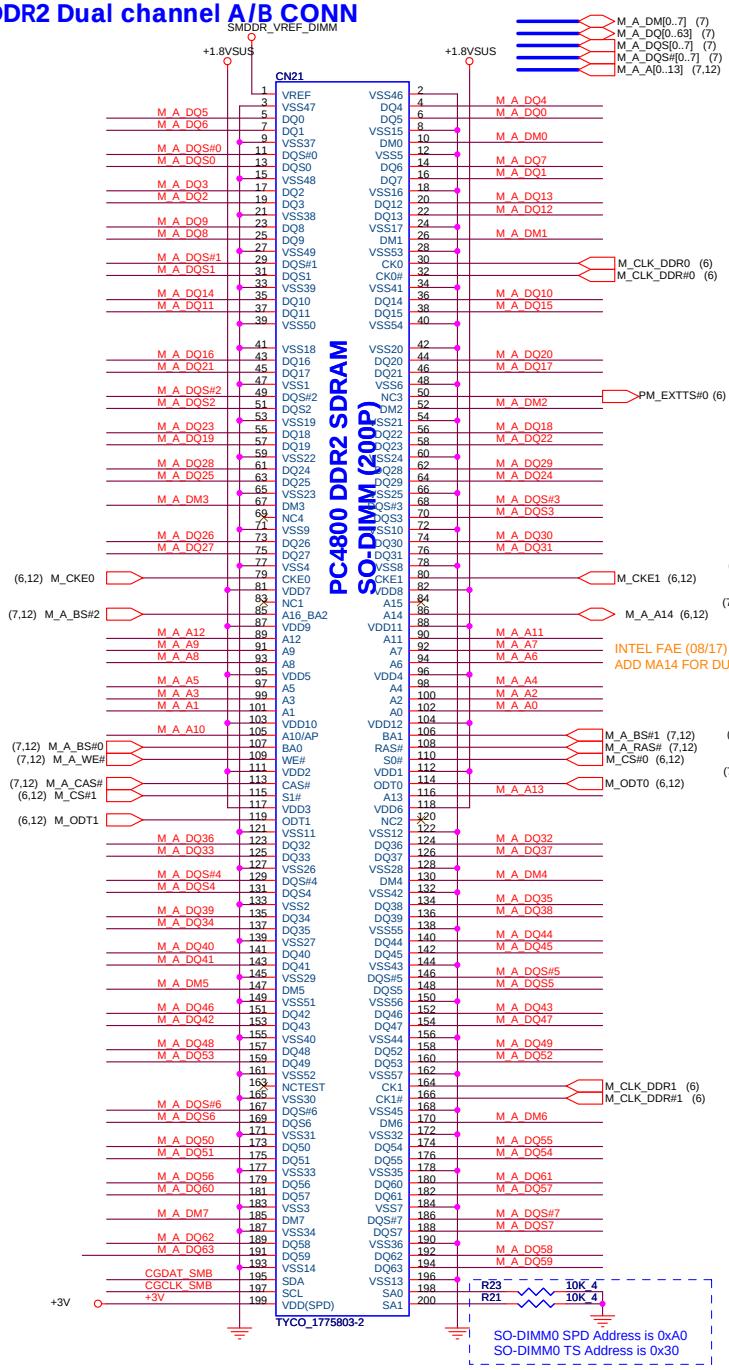
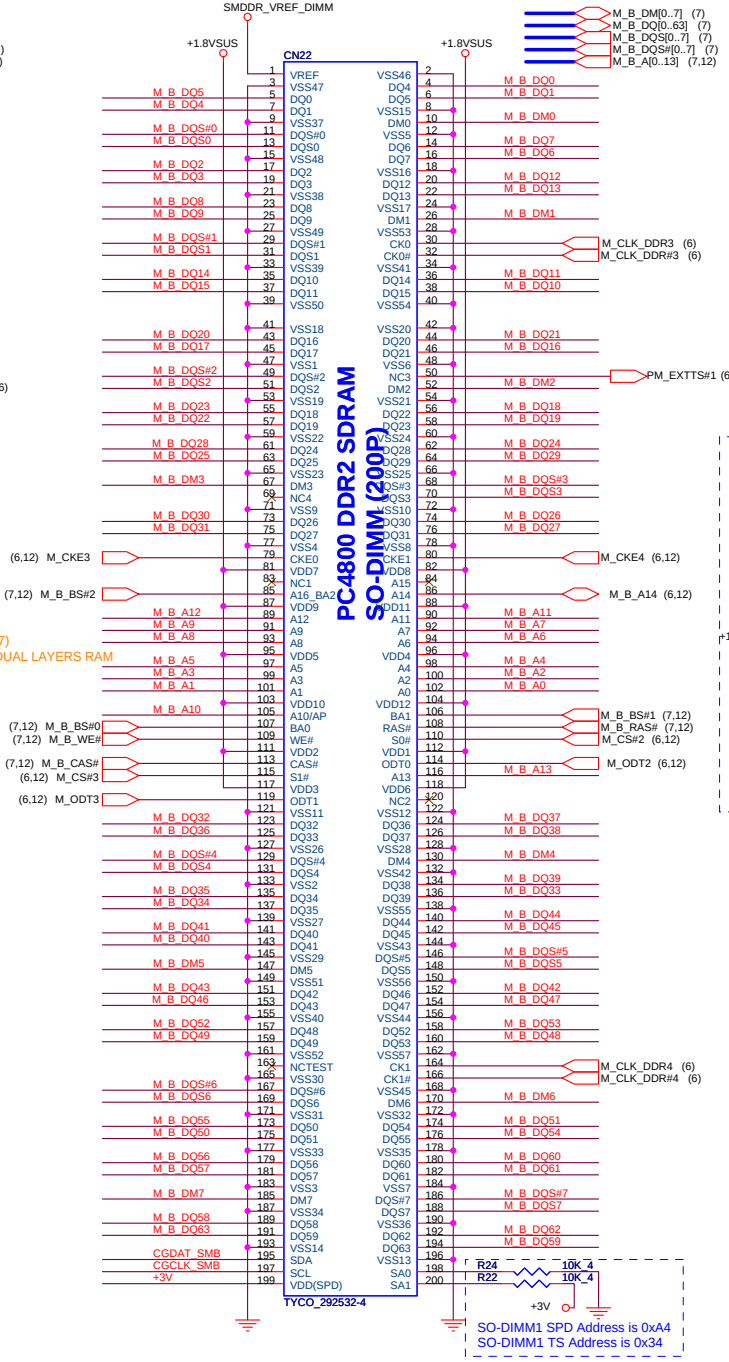
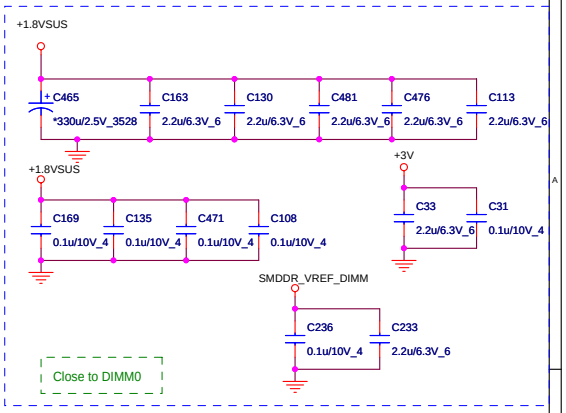
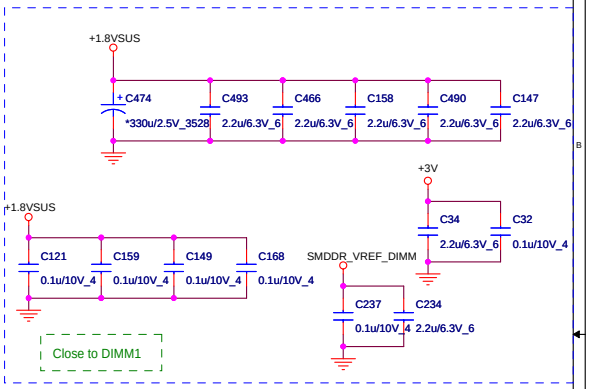
DDR2 Dual channel A/B CONN



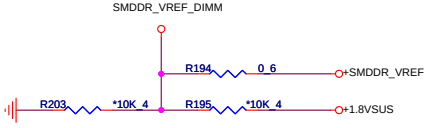


INTEL FAE (08/17)
ADD MA14 FOR DUAL LAYERS RAM





CGCLK_SMB — CGCLK_SMB (2)
CGDAT_SMB — CGDAT_SMB (2)



Standard Type H: 6.5mm

CLOCK 0,1
CKE 0,1

Standard Type H: 11mm

CLOCK 3,4
CKE 2,3

Quanta Computer Inc.	
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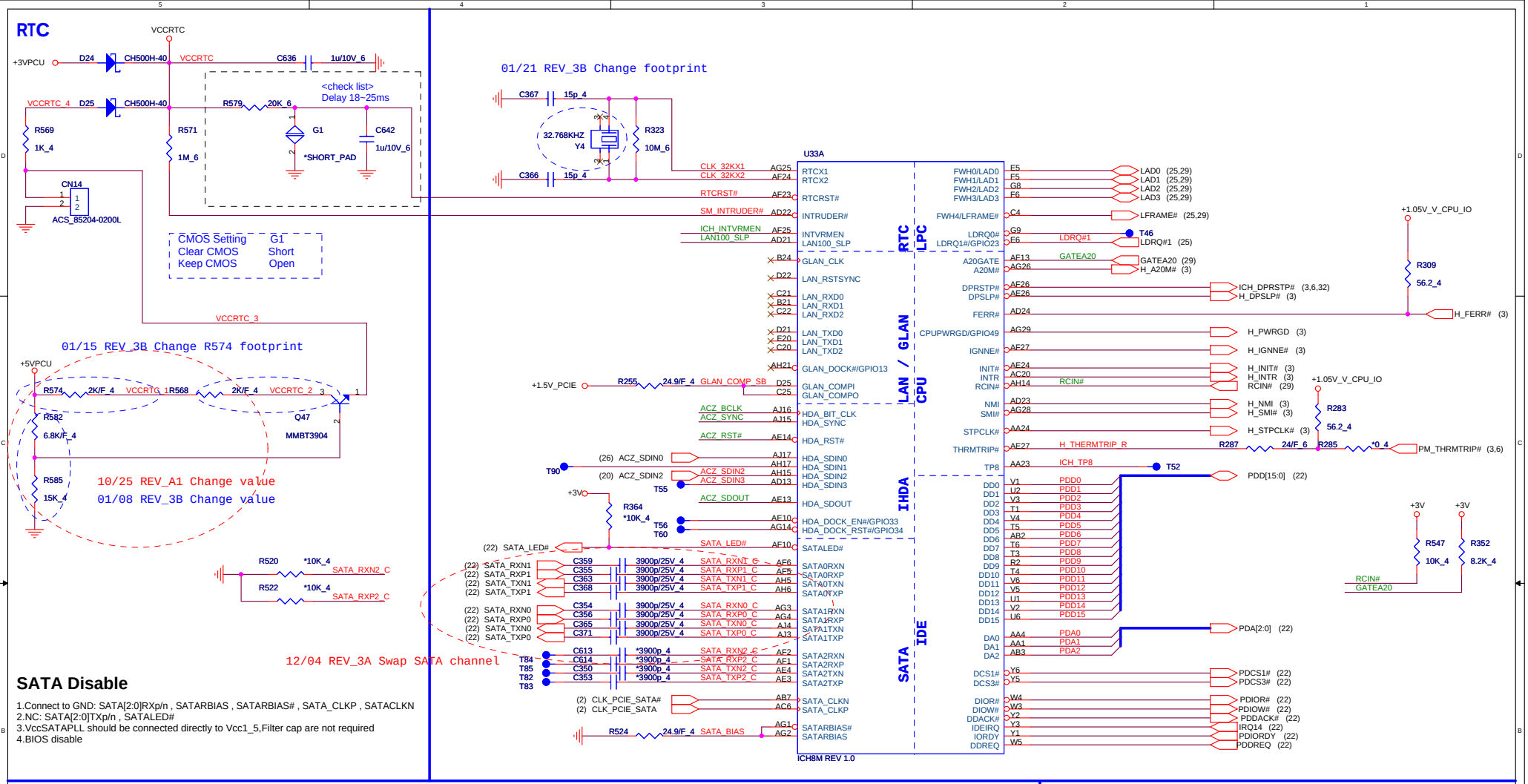
RTC
VCCRTC
+3VPCU
D24
CH500H-40
C636
1u/10V_6
VCCRTC_4
D25
R579
20K_6
R569
1K_4
R571
1M_6
G1
C642
1u/10V_6
*SHORT_PAD
<check list>
Delay 18~25ms
CN14
ACS_85204-0200L
CMOS Setting G1
Clear CMOS Short
Keep CMOS Open
01/21 REV_3B Change footprint
C367
15p_4
C366
15p_4
32.768KHZ
Y4
R323
10M_6
U33A
CLK_32KX1
CLK_32KX2
RTCRST#
SM_INTRUDER#
ICH_INTVRMEN
LAN100_SLP
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
RTC
LPC
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
LAN / GLAN
CPU
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
IHDA
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
SATA
IDE
ICH8M REV 1.0
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
LAD0 (25,29)
LAD1 (25,29)
LAD2 (25,29)
LAD3 (25,29)
LFRAME# (25,29)
LDRQ#1
LDRQ#1 (25)
GATEA20
GATEA20 (29)
H_A20M# (3)
ICH_DPRSTP# (3,6,32)
H_DPSLP# (3)
H_FERR# (3)
H_PWRGD (3)
H_IGNNE# (3)
H_INIT# (3)
H_INTR (3)
RCIN# (29)
H_NMI (3)
H_SMI# (3)
H_STPCLK# (3)
H_THERMTRIP_R
ICH_TP8
T52
PDD[15:0] (22)
PDA[2:0] (22)
PDCS1# (22)
PDCS3# (22)
PDIOR# (22)
PDIOW# (22)
PDDACK# (22)
IRQ14 (22)
PDIORDY (22)
PDDREQ (22)
+1.05V_V_CPU_IO
R309
56.2_4
R283
56.2_4
R287
24/F_6
R285
*0_4
PM_THRMTRIP# (3,6)
+3V
R547
10K_4
R352
8.2K_4
RCIN#
GATEA20
01/15 REV_3B Change R574 footprint
+5VPCU
R574
2K/F_4
R568
2K/F_4
R582
6.8K/F_4
Q47
MMBT3904
R585
15K_4
10/25 REV_A1 Change value
01/08 REV_3B Change value
VCCRTC_3
VCCRTC_2
VCCRTC_1
+1.5V_PCIE
R255
24.9/F_4
GLAN_COMP_SB
ACZ_BCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN2
ACZ_SDIN3
ACZ_SDOUT
SATA_LED#
R364
*10K_4
T90
T55
T56
T60
T84
T85
T82
T83
R520
*10K_4
R522
*10K_4
SATA_RXN2_C
SATA_RXP2_C
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
C359
C355
C363
C368
C354
C356
C365
C371
C613
C614
C350
C353
3900p/25V_4
*3900p_4
CLK_PCIE_SATA#
CLK_PCIE_SATA
R524
24.9/F_4
SATA_BIAS
12/04 REV_3A Swap SATA channel
SATA Disable
1.Connect to GND: SATA[2:0]RXp/n , SATARBIAS , SATARBIAS# , SATA_CLKP , SATACLKN
2.NC: SATA[2:0]TXp/n , SATALED#
3.VccSATAPLL should be connected directly to Vcc1_5,Filter cap are not required
4.BIOS disable
SB Strap
ICH8-M Internal VR Enable strap
(Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)
INTVRMEN
Low = Internal VR disable
High = Internal VR enable(Default)
ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1.05)
LAN100_SLP
Low = Internal VR disable
High = Internal VR enable(Default)
XOR Chain Entrance Strap
ICH_RSV0 | HDA_SDOUT | Description
0 | 0 | RSVD
0 | 1 | Enter XOR Chain
1 | 0 | Normal opration(Default)
1 | 1 | Set PCIE port config bit 1
VCCRTC
R325
332K_6
ICH_INTVRMEN
R326
*0_4
R303
332K_6
LAN100_SLP
R312
*0_4
+3V
R368
*1K_6
ACZ_SDOUT
ICH_TP3 (16)
R539
*1K_4
HDA
BIT_CLK_AUDIO
R370
*22_4
C387
*22p/50V_4
BIT_CLK_HDMI
R551
*22_4
C386
*22p/50V_4
ACZ_SDOUT
R372
33_4
ACZ_SDOUT_AUDIO (26)
R351
33_4
ACZ_SDOUT_HDMI (20)
ACZ_SYNC
R549
33_4
ACZ_SYNC_AUDIO (26)
R533
33_4
ACZ_SYNC_HDMI (20)
ACZ_BCLK
R550
33_4
BIT_CLK_AUDIO (26)
R535
33_4
BIT_CLK_HDMI (20)
ACZ_RST#
R371
33_4
ACZ_RST#_AUDIO (26)
R350
33_4
ACZ_RST#_HDMI (20)
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PROJECT : BL5S Santa Rosa
Size
Document Number
ICH8M HOST(1 of 4)
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1A
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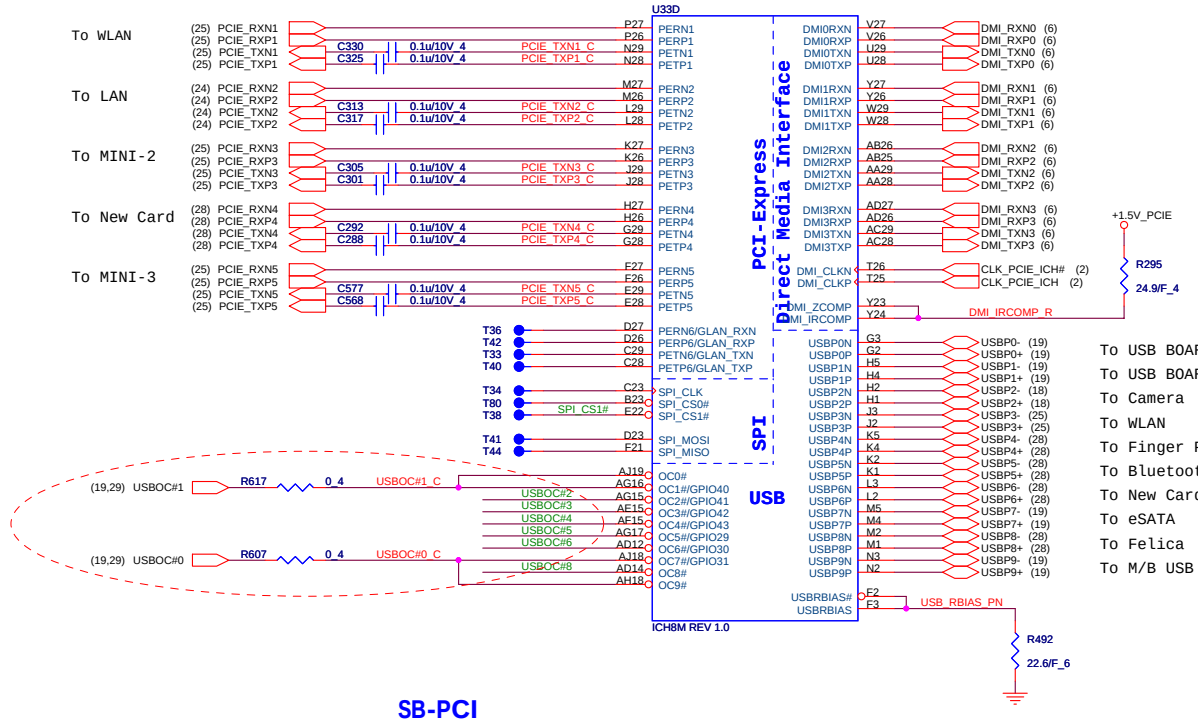
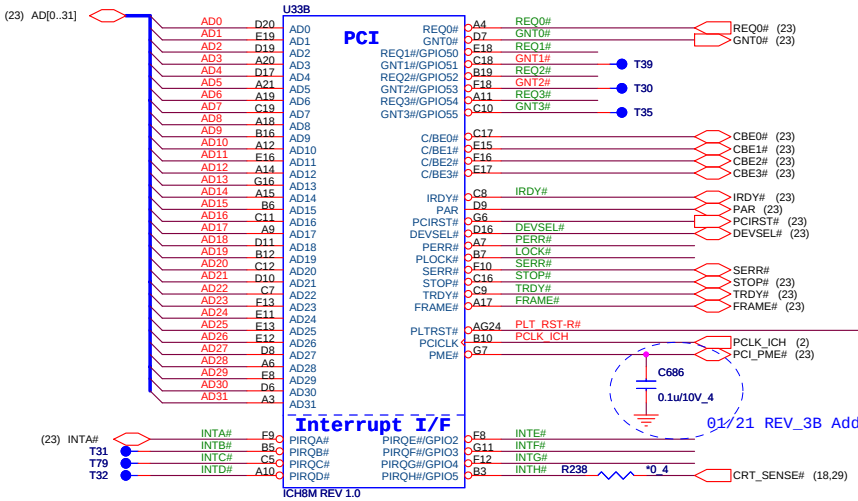
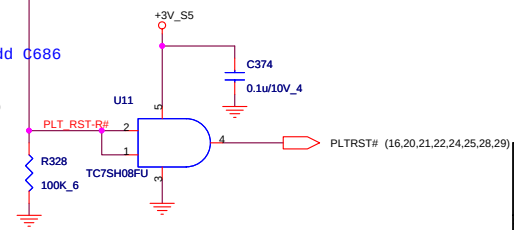
SB-PCIE/USB/DMI



SB-PCI



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#	OZ129



A16 SWAP Override strap

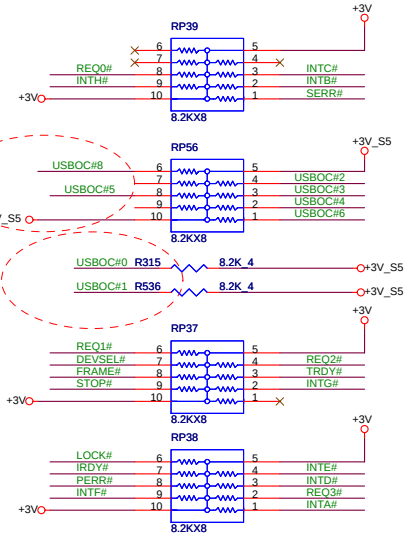
PCI_GNT#3	Low = A16 swap override enabled High = Default

GNT3# R251 *1K_4

ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

SPI_CS1# R258 *1K_4
GNT0# R253 *1K_4



Quanta Computer Inc.	
PROJECT : BL5S Santa Rosa	
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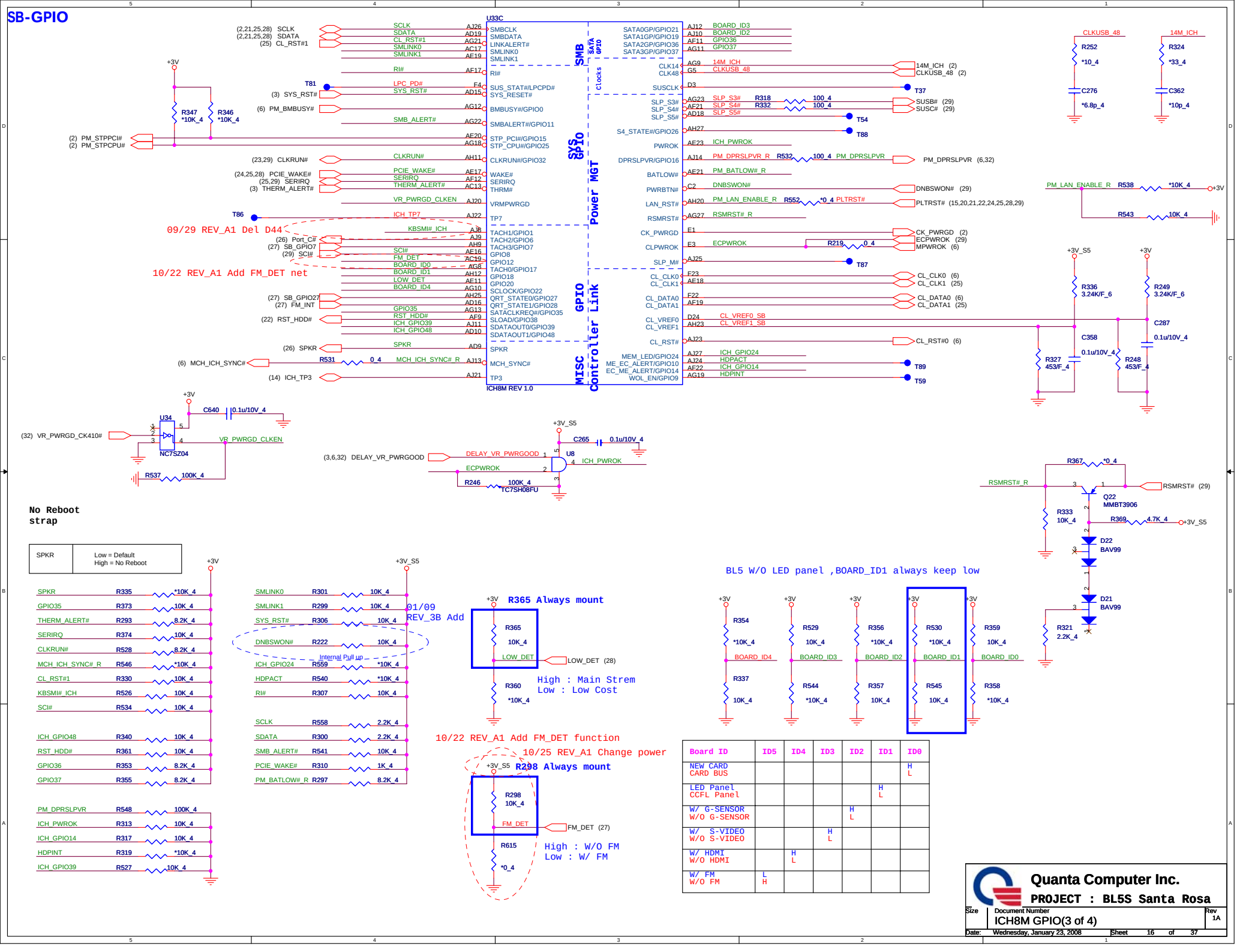
SB-GPIO


U33C
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
BMBUSY#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP7
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
GPIO12
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SPKR
MCH_SYNC#
TP3
SMB
CLOCKS
SATA GPIO
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
iCH8M REV 1.0
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST#
MEM_LED/GPIO24
ME_EC_ALERT/GPIO10
EC_ME_ALERT/GPIO14
WOL_EN/GPIO9
09/29 REV_A1 Del D44
10/22 REV_A1 Add FM_DET net
NC7SZ04
TC7SH08FU
No Reboot strap
SPKR | Low = Default High = No Reboot
01/09 REV_3B Add
Internal Pull up
R365 Always mount
High : Main Strem
Low : Low Cost
10/22 REV_A1 Add FM_DET function
10/25 REV_A1 Change power
R298 Always mount
High : W/O FM
Low : W/ FM
BL5 W/O LED panel ,BOARD_ID1 always keep low
Board ID | ID5 | ID4 | ID3 | ID2 | ID1 | ID0
NEW CARD CARD BUS | | | | | | H L
LED Panel CCFL Panel | | | | | H L |
W/ G-SENSOR W/O G-SENSOR | | | | H L | | |
W/ S-VIDEO W/O S-VIDEO | | | H L | | | |
W/ HDMI W/O HDMI | | H L | | | | |
W/ FM W/O FM | L H | | | | | |
Quanta Computer Inc.
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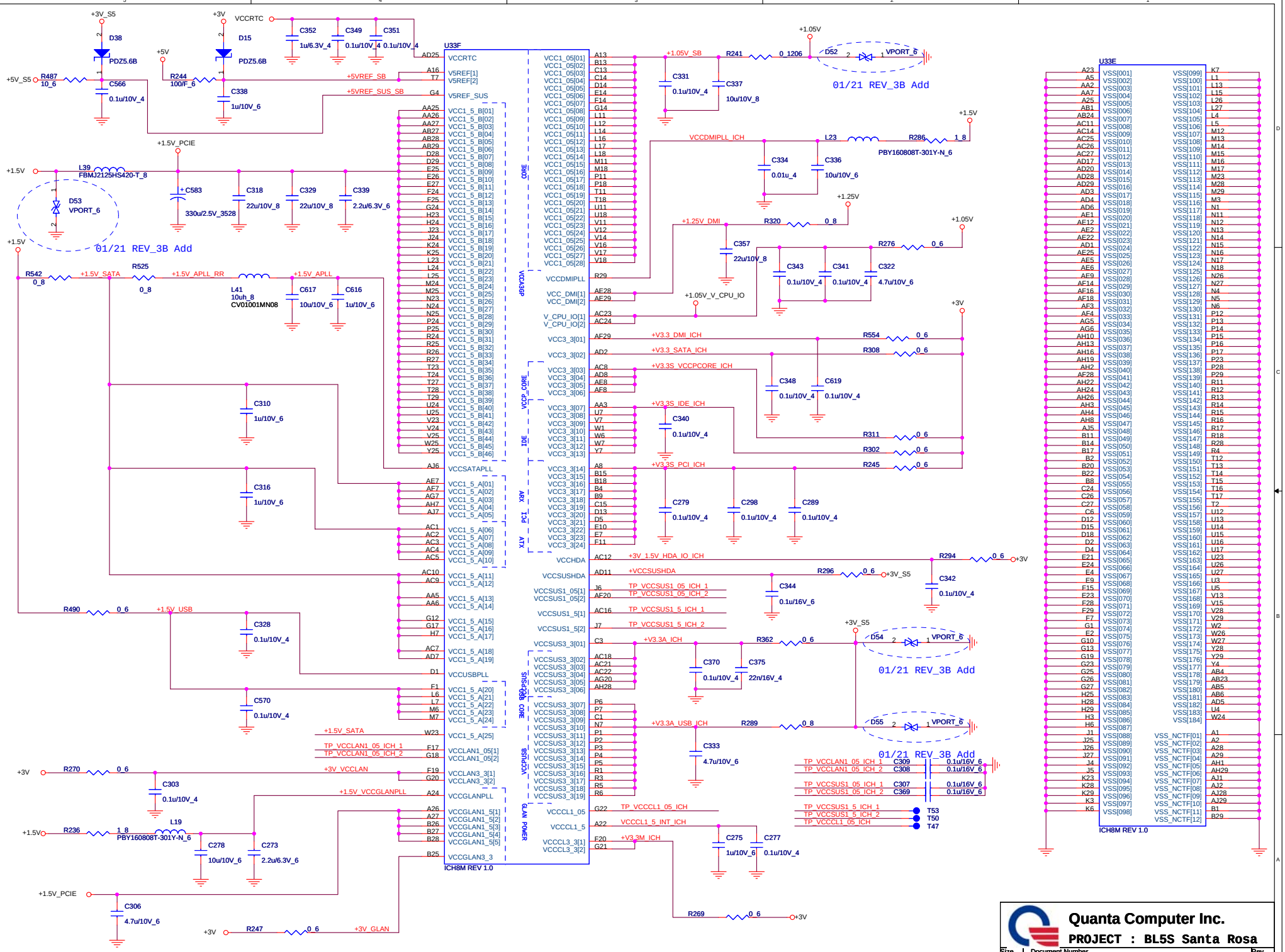
U33F
ICH8M REV 1.0
U33E
ICH8M REV 1.0
01/21 REV_3B Add
01/21 REV_3B Add
01/21 REV_3B Add
01/21 REV_3B Add
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1A
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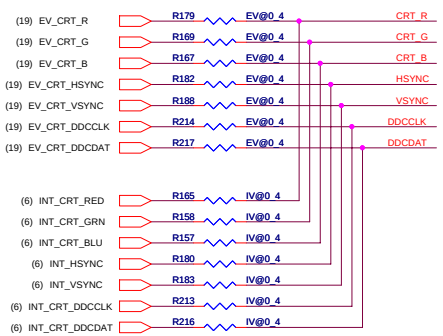
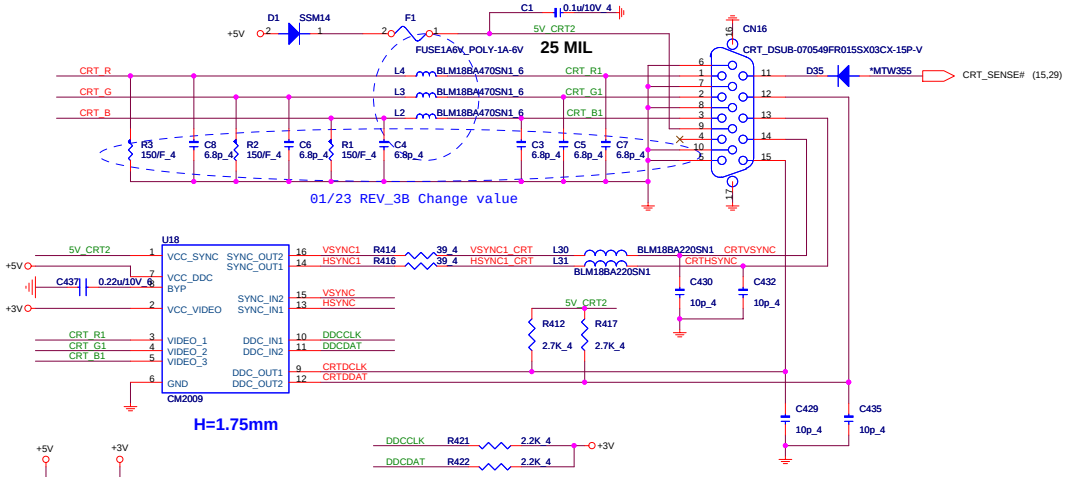
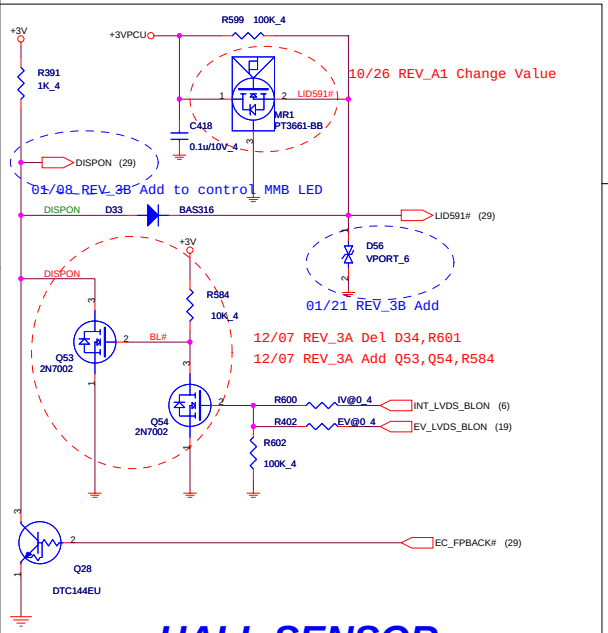
CRT PORT

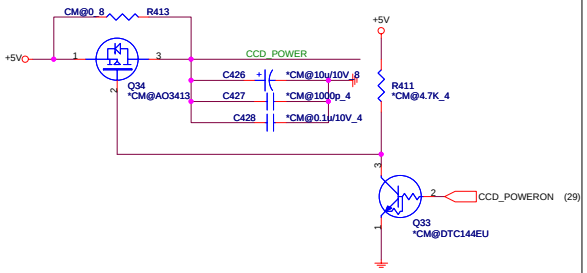


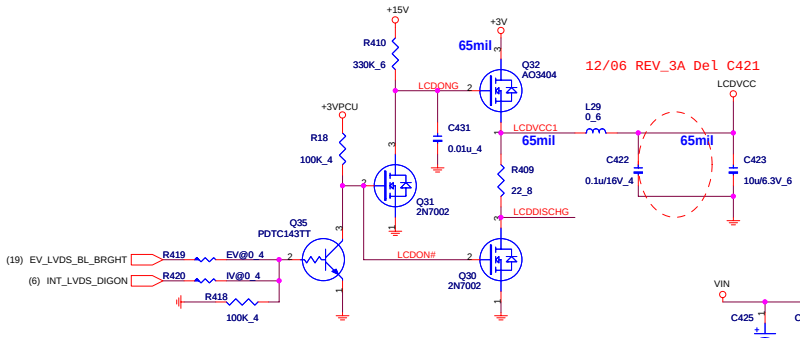


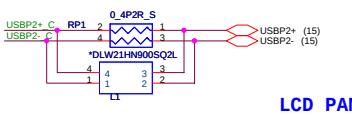


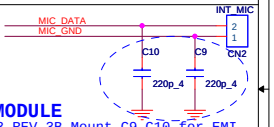
HALL SENSOR

CAMERA MODULE





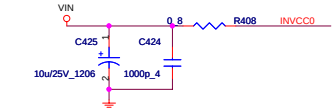


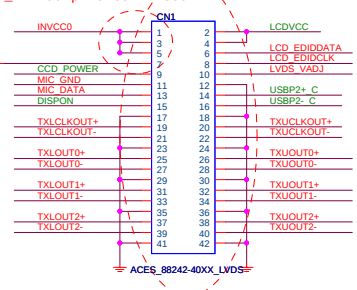


LCD PANEL MODULE

01/03 REV_3B Mount C9,C10 for EMI

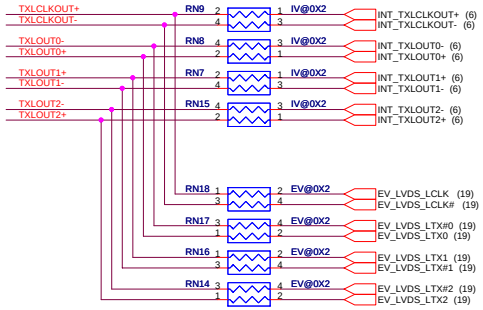
10/22 REV_A1 Add pin3 to INVCC0

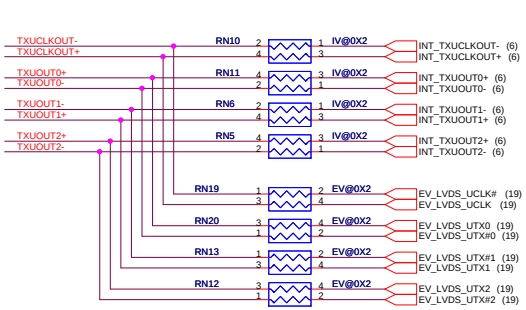


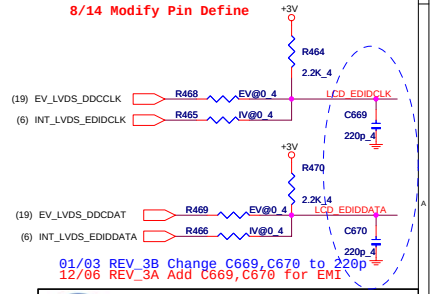


10/22 REV_A1 Change P/N

8/14 Modify Pin Define







01/03 REV_3B Change C669,C670 to 220p

12/06 REV_3A Add C669,C670 for EMI

Quanta Computer Inc.

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VGA

CN25

(6) PEG_TXN15 / (6) PEG_TXP15 — PEG_TXN15 / PEG_TXP15 — PEG_RXN15 / PEG_RXP15 — PEG_RXN15 (6) / PEG_RXP15 (6)
(6) PEG_TXN14 / (6) PEG_TXP14 — PEG_TXN14 / PEG_TXP14 — PEG_RXN14 / PEG_RXP14 — PEG_RXN14 (6) / PEG_RXP14 (6)
(6) PEG_TXN13 / (6) PEG_TXP13 — PEG_TXN13 / PEG_TXP13 — PEG_RXN13 / PEG_RXP13 — PEG_RXN13 (6) / PEG_RXP13 (6)
(6) PEG_TXN12 / (6) PEG_TXP12 — PEG_TXN12 / PEG_TXP12 — PEG_RXN12 / PEG_RXP12 — PEG_RXN12 (6) / PEG_RXP12 (6)
(6) PEG_TXN11 / (6) PEG_TXP11 — PEG_TXN11 / PEG_TXP11 — PEG_RXN11 / PEG_RXP11 — PEG_RXN11 (6) / PEG_RXP11 (6)
(6) PEG_TXN10 / (6) PEG_TXP10 — PEG_TXN10 / PEG_TXP10 — PEG_RXN10 / PEG_RXP10 — PEG_RXN10 (6) / PEG_RXP10 (6)
(6) PEG_TXN9 / (6) PEG_TXP9 — PEG_TXN9 / PEG_TXP9 — PEG_RXN9 / PEG_RXP9 — PEG_RXN9 (6) / PEG_RXP9 (6)
(6) PEG_TXN8 / (6) PEG_TXP8 — PEG_TXN8 / PEG_TXP8 — PEG_RXN8 / PEG_RXP8 — PEG_RXN8 (6) / PEG_RXP8 (6)
(6) PEG_TXN7 / (6) PEG_TXP7 — PEG_TXN7 / PEG_TXP7 — PEG_RXN7 / PEG_RXP7 — PEG_RXN7 (6) / PEG_RXP7 (6)
(6) PEG_TXN6 / (6) PEG_TXP6 — PEG_TXN6 / PEG_TXP6 — PEG_RXN6 / PEG_RXP6 — PEG_RXN6 (6) / PEG_RXP6 (6)
(6) PEG_TXN5 / (6) PEG_TXP5 — PEG_TXN5 / PEG_TXP5 — PEG_RXN5 / PEG_RXP5 — PEG_RXN5 (6) / PEG_RXP5 (6)
(6) PEG_TXN4 / (6) PEG_TXP4 — PEG_TXN4 / PEG_TXP4 — PEG_RXN4 / PEG_RXP4 — PEG_RXN4 (6) / PEG_RXP4 (6)
(6) PEG_TXN3 / (6) PEG_TXP3 — PEG_TXN3 / PEG_TXP3 — PEG_RXN3 / PEG_RXP3 — PEG_RXN3 (6) / PEG_RXP3 (6)
(6) PEG_TXN2 / (6) PEG_TXP2 — PEG_TXN2 / PEG_TXP2 — PEG_RXN2 / PEG_RXP2 — PEG_RXN2 (6) / PEG_RXP2 (6)
(6) PEG_TXN1 / (6) PEG_TXP1 — PEG_TXN1 / PEG_TXP1 — PEG_RXN1 / PEG_RXP1 — PEG_RXN1 (6) / PEG_RXP1 (6)
(6) PEG_TXN0 / (6) PEG_TXP0 — PEG_TXN0 / PEG_TXP0 — PEG_RXN0 / PEG_RXP0 — PEG_RXN0 (6) / PEG_RXP0 (6)

(18) EV_CRT_DDCCLK / (18) EV_CRT_DDCDAT — EV_CRT_DDCCLK / EV_CRT_DDCDAT — CLK_MXM# / CLK_MXM — CLK_MXM# (2) / CLK_MXM (2)
(21) EV_HDMI_DDCCLK / (21) EV_HDMI_DDCDATA — EV_HDMI_DDCCLK / EV_HDMI_DDCDAT — GFXRST# / SYSFANON# — GFXRST# (15) / SYSFANON# (3)
(18) EV_LVDS_DDCCLK / (18) EV_LVDS_DDCDAT — EV_LVDS_DDCCLK / EV_LVDS_DDCDAT — GFXON / GFXPG — GFXPG (29)
3ND_MBDATA — 3ND_MBDATA (21,28,29)
3ND_MBCLK — 3ND_MBCLK (21,28,29)
EV_LVDS_BLON — EV_LVDS_BLON (18)
EV_LVDS_BL_BRGHT — EV_LVDS_BL_BRGHT (18)
DVI_HPD — DVI_HPD (21)
(18) EV_CRT_R — EV_CRT_R — EV_CRT_HSYNC — EV_CRT_HSYNC (18)
(18) EV_CRT_G — EV_CRT_G — EV_CRT_VSYNC — EV_CRT_VSYNC (18)
(18) EV_CRT_B — EV_CRT_B
(18) EV_LVDS_LTX#2 / (18) EV_LVDS_LTX2 — EV_LVDS_LTX#2 / EV_LVDS_LTX2 — EV_LVDS_UTX#2 / EV_LVDS_UTX2 — EV_LVDS_UTX#2 (18) / EV_LVDS_UTX2 (18)
(18) EV_LVDS_LTX#1 / (18) EV_LVDS_LTX1 — EV_LVDS_LTX#1 / EV_LVDS_LTX1 — EV_LVDS_UTX#1 / EV_LVDS_UTX1 — EV_LVDS_UTX#1 (18) / EV_LVDS_UTX1 (18)
(18) EV_LVDS_LTX#0 / (18) EV_LVDS_LTX0 — EV_LVDS_LTX#0 / EV_LVDS_LTX0 — EV_LVDS_UTX#0 / EV_LVDS_UTX0 — EV_LVDS_UTX#0 (18) / EV_LVDS_UTX0 (18)
(18) EV_LVDS_LCLK# / (18) EV_LVDS_LCLK — EV_LVDS_LCLK# / EV_LVDS_LCLK — EV_LVDS_UCLK# / EV_LVDS_UCLK — EV_LVDS_UCLK# (18) / EV_LVDS_UCLK (18)
(22) EV_TV_C/R — EV_TV_C/R
(22) EV_TV_Y/G — EV_TV_Y/G
T94 — EV_TV_COMP
10/24 REV_A1 Modify
(21) EV_HDMICLK- / (21) EV_HDMICLK+ — EV_HDMICLK- / EV_HDMICLK+
(21) EV_HDMITX2N / (21) EV_HDMITX2P — EV_HDMITX2N / EV_HDMITX2P
(21) EV_HDMITX1N / (21) EV_HDMITX1P — EV_HDMITX1N / EV_HDMITX1P
(21) EV_HDMITX0N / (21) EV_HDMITX0P — EV_HDMITX0N / EV_HDMITX0P

VIN_VGA — VIN
VIN_VGA — R478 — *0_8 — VIN
*Tyco
10/16 REV_A1 Modify

VIN
C536 0.1u/50V_6
+5V
C532 0.1u/10V_4
C535 10u/10V_6
+3V
C533 0.1u/10V_4
C534 10u/10V_6

USB

+5VPCU — F3 POLY SWITCH 1.5A/6V_1206 — USBPOWER
C419 4.7u/10V_6
U16 RT9711BPF
IN1 IN2 EN# GND GND-C OUT3 OUT2 OUT1 OC#
USBPWR0
(29) USB_EN#
R394 *100K_6 +5VPCU
USBOC#0 (15,29)

09/20 REV_A1 Modify

(15) USBP9+ / (15) USBP9- — USBP9+ / USBP9-
01/17 REV_3B Del R513,R494,R523,R521,L38,L40
(15) USBP7+ / (15) USBP7- — USBP7+ / USBP7-

MAINON (29,33,34,35)

USBPWR0 — C565 100u/6.3V_3528 — USBP7- / USBP7+ — CN28 USB
09/23 REV_A1 Change footprint

USBPWR0 — C606 100u/6.3V_3528 — USBP9- / USBP9+ — CN32 USB
09/23 REV_A1 Change footprint

USB board connector

+5VPCU — C663 0.1u/10V_4 — USB_EN#1 — C664 0.1u/10V_4
10/24 REV_A1 Add for EMI

USB
01/09 REV_3B Add
Close CN12
USBP9- D42 EGA_4 D19 EGA_4 USBP0-
USBP9+ D43 EGA_4 D18 EGA_4 USBP0+
USBP7- D39 EGA_4 D17 EGA_4 USBP1-
USBP7+ D40 EGA_4 D16 EGA_4 USBP1+
USBPWR0 D41 VPORT_6 D20 VPORT_6 +5VPCU

09/20 REV_A1 Modify
CN11
(15,29) USBOC#1 — +5VPCU
(15) USBP1+ / (15) USBP1- / (15) USBP0+ / (15) USBP0- — USBP1+ / USBP1- / USBP0+ / USBP0-
(29) USB_EN#1 — +5VPCU
BT@88266-100XX-XXX-10P-R
09/29 REV_A1 Modify

Quanta Computer Inc.
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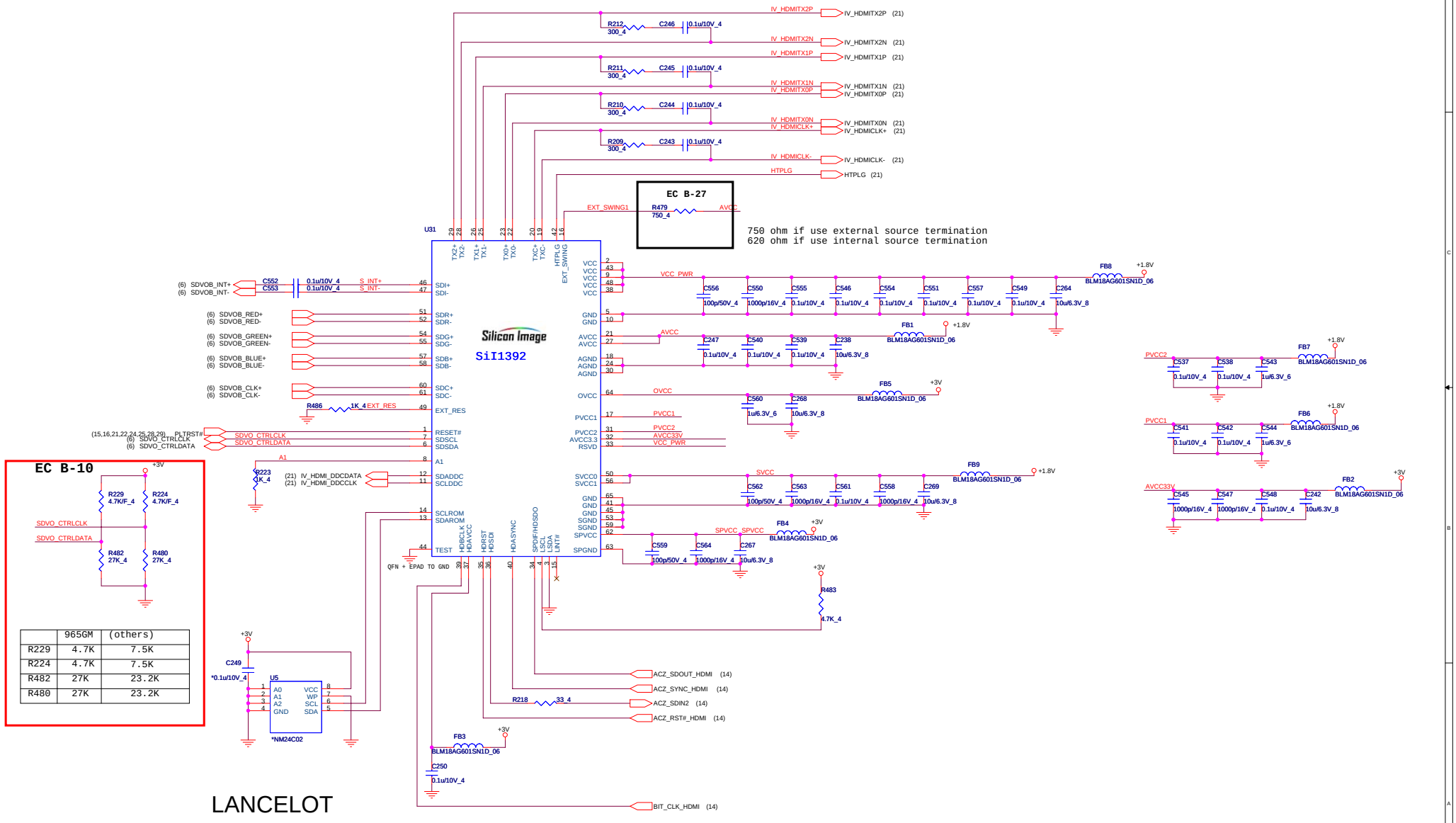
SiI1392 HDMI TX

LAYOUT RULES:

Route traces with 100 Ohm Differential Impedance

Avoid placing GND Copper or traces adjacent to TMDS Trace

Put these 4 resistors and 4 capacitors as close as possible to the TMDS output pins of the Sil1392



	965GM	(others)
R229	4.7K	7.5K
R224	4.7K	7.5K
R482	27K	23.2K
R480	27K	23.2K

Quanta Computer Inc.		
PROJECT : BL5S Santa Rosa		
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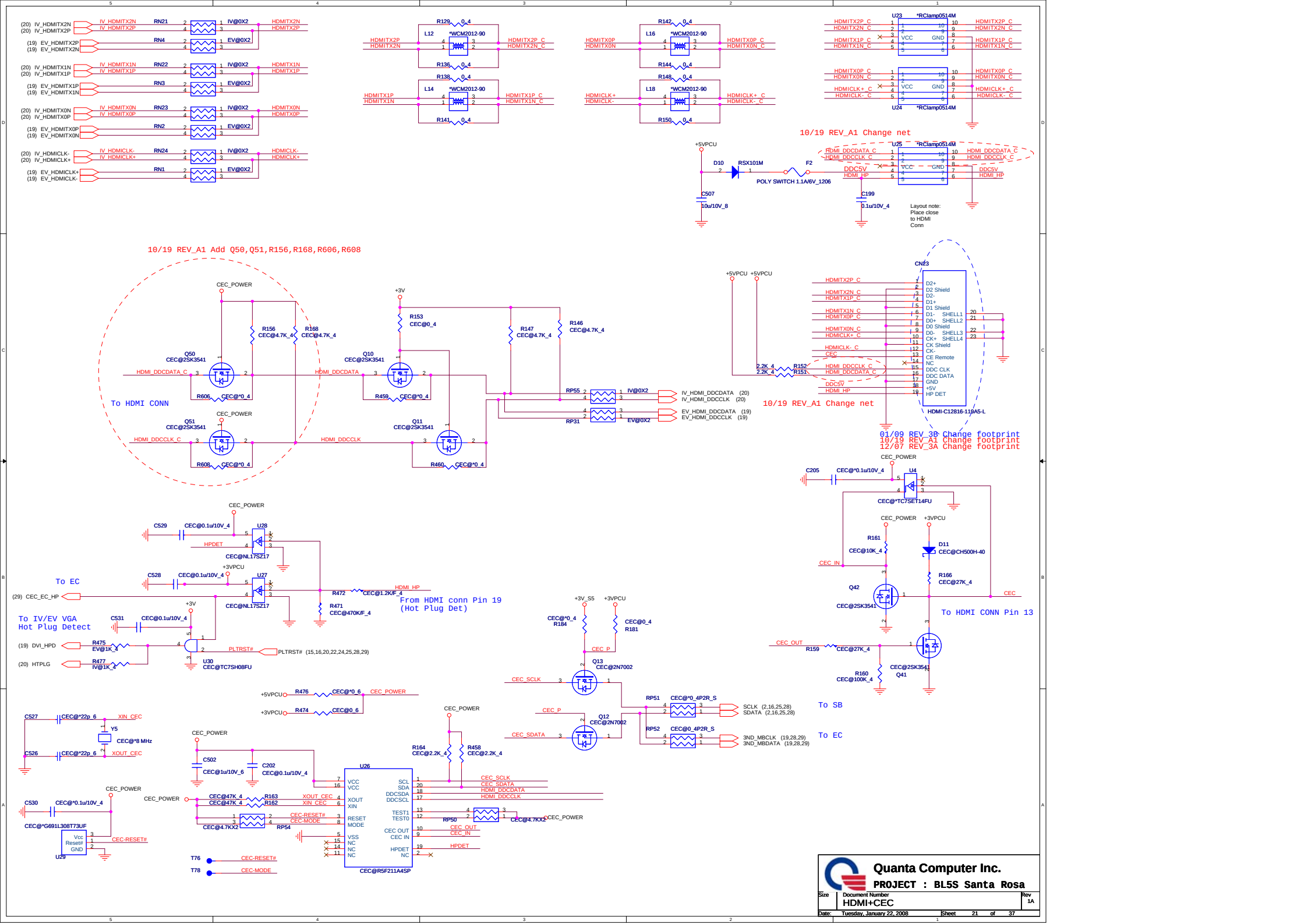
(20) IV_HDMITX2N
(20) IV_HDMITX2P
(19) EV_HDMITX2P
(19) EV_HDMITX2N
RN21
RN4
IV@0X2
EV@0X2
HDMITX2N
HDMITX2P
(20) IV_HDMITX1N
(20) IV_HDMITX1P
(19) EV_HDMITX1P
(19) EV_HDMITX1N
RN22
RN3
HDMITX1N
HDMITX1P
(20) IV_HDMITX0N
(20) IV_HDMITX0P
(19) EV_HDMITX0P
(19) EV_HDMITX0N
RN23
RN2
HDMITX0N
HDMITX0P
(20) IV_HDMICLK-
(20) IV_HDMICLK+
(19) EV_HDMICLK+
(19) EV_HDMICLK-
RN24
RN1
HDMICLK-
HDMICLK+
R129 0_4
L12 *WCM2012-90
R136 0_4
R138 0_4
L14 *WCM2012-90
R141 0_4
R142 0_4
L16 *WCM2012-90
R144 0_4
R148 0_4
L18 *WCM2012-90
R150 0_4
U23 *RClamp0514M
U24 *RClamp0514M
VCC
GND
10/19 REV_A1 Change net
+5VPCU
D10
RSX101M
F2
POLY SWITCH 1.1A/6V_1206
DDC5V
HDMI_HP
C507
10u/10V_8
C199
0.1u/10V_4
U25 *RClamp0514M
HDMI_DDCDATA_C
HDMI_DDCCLK_C
Layout note:
Place close
to HDMI
Conn
10/19 REV_A1 Add Q50,Q51,R156,R168,R606,R608
CEC_POWER
+3V
R153 CEC@0_4
R156 CEC@4.7K_4
R168 CEC@4.7K_4
R147 CEC@4.7K_4
R146 CEC@4.7K_4
Q50 CEC@2SK3541
Q10 CEC@2SK3541
Q51 CEC@2SK3541
Q11 CEC@2SK3541
HDMI_DDCDATA_C
HDMI_DDCDATA
HDMI_DDCCLK_C
HDMI_DDCCLK
R606 CEC@*0_4
R459 CEC@*0_4
R608 CEC@*0_4
R460 CEC@*0_4
To HDMI CONN
RP55 IV@0X2
RP31 EV@0X2
IV_HDMI_DDCDATA (20)
IV_HDMI_DDCCLK (20)
EV_HDMI_DDCDATA (19)
EV_HDMI_DDCCLK (19)
+5VPCU +5VPCU
2.2K_4
R152
R151
CN23
HDMI-C12816-119A5-L
D2+
D2 Shield
D2-
D1+
D1 Shield
D1- SHELL1
D0+ SHELL2
D0 Shield
D0- SHELL3
CK+ SHELL4
CK Shield
CK-
CE Remote
NC
DDC CLK
DDC DATA
GND
+5V
HP DET
10/19 REV_A1 Change net
01/09 REV_3B Change footprint
10/19 REV_A1 Change footprint
12/07 REV_3A Change footprint
C205 CEC@*0.1u/10V_4
U4 CEC@*TC7SET14FU
+3VPCU
R161 CEC@10K_4
D11 CEC@CH500H-40
CEC_IN
R166 CEC@27K_4
Q42 CEC@2SK3541
CEC
To HDMI CONN Pin 13
CEC_OUT
R159 CEC@27K_4
R160 CEC@100K_4
Q41 CEC@2SK3541
To SB
To EC
C529 CEC@0.1u/10V_4
U28 CEC@NL17SZ17
HPDET
C528 CEC@0.1u/10V_4
U27 CEC@NL17SZ17
To EC
(29) CEC_EC_HP
R472 CEC@1.2K/F_4
HDMI_HP
R471 CEC@470K/F_4
From HDMI conn Pin 19
(Hot Plug Det)
To IV/EV VGA
Hot Plug Detect
C531 CEC@0.1u/10V_4
(19) DVI_HPD
R475 EV@1K_4
(20) HTPLG
R477 IV@1K_4
PLTRST#
PLTRST# (15,16,20,22,24,25,28,29)
U30 CEC@TC7SH08FU
+3V_S5
+3VPCU
CEC@*0_4 R184
CEC@0_4 R181
CEC_P
Q13 CEC@2N7002
CEC_SCLK
Q12 CEC@2N7002
CEC_SDATA
RP51 CEC@*0_4P2R_S
RP52 CEC@0_4P2R_S
SCLK (2,16,25,28)
SDATA (2,16,25,28)
3ND_MBCLK (19,28,29)
3ND_MBDATA (19,28,29)
+5VPCU R476 CEC@*0_6
+3VPCU R474 CEC@0_6
C527 CEC@*22p_6
XIN_CEC
Y5
CEC@*8 MHz
C526 CEC@*22p_6
XOUT_CEC
C530 CEC@*0.1u/10V_4
CEC@*G691L308T73UF
U29
CEC-RESET#
C502 CEC@1u/10V_6
C202 CEC@0.1u/10V_4
R163 CEC@47K_4
R162 CEC@47K_4
XOUT_CEC
XIN_CEC
CEC-RESET#
CEC-MODE
RP54 CEC@4.7KX2
T76 CEC-RESET#
T78 CEC-MODE
U26 CEC@R5F211A4SP
VCC
XOUT
XIN
RESET
MODE
VSS
NC
SCL
SDA
DDCSDA
DDCSCL
TEST1
TEST0
CEC OUT
CEC IN
HPDET
R164 CEC@2.2K_4
R458 CEC@2.2K_4
CEC_SCLK
CEC_SDATA
HDMI_DDCDATA
HDMI_DDCCLK
RP50 CEC@4.7KX2
CEC_OUT
CEC_IN
HPDET
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
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HDMI+CEC
Rev
1A
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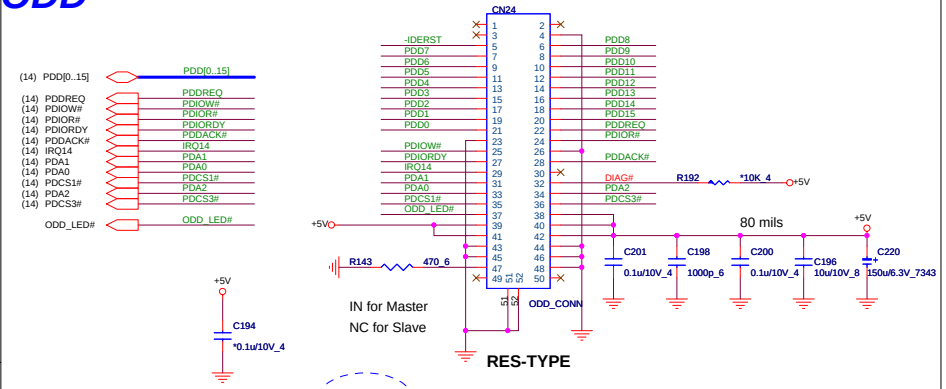
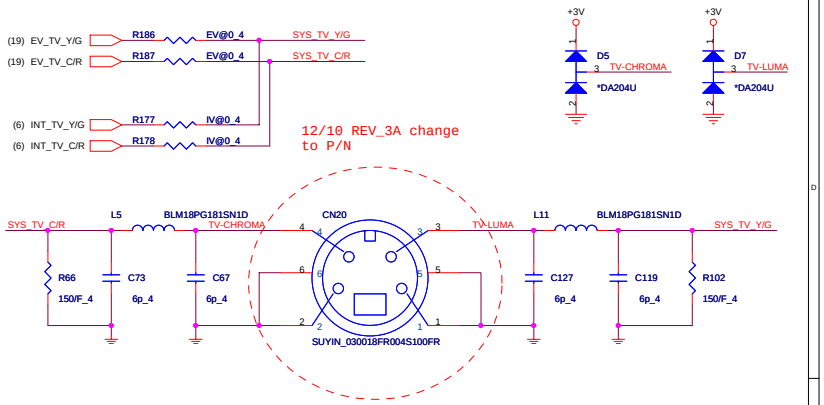
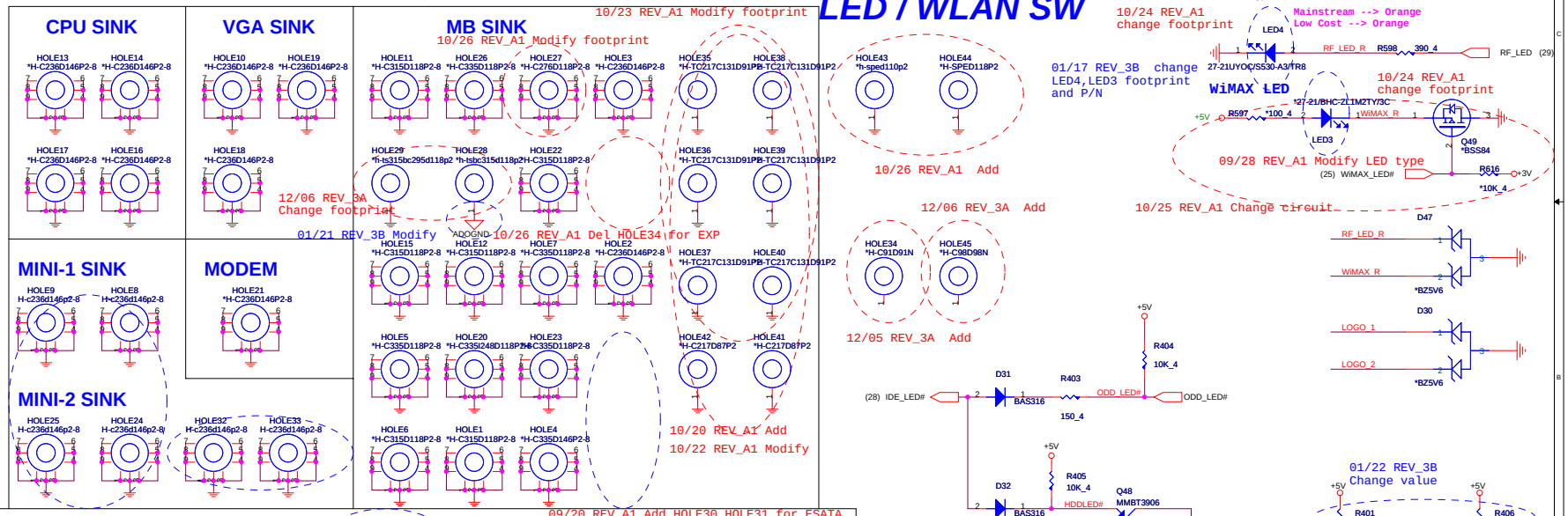
ODD

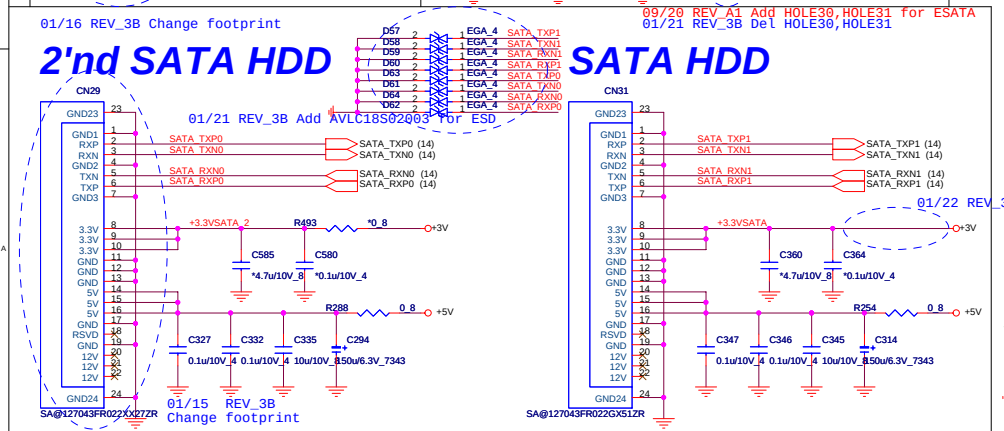


TVOUT



LED / WLAN SW





Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
Size
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PATA/ODD/TV/LED
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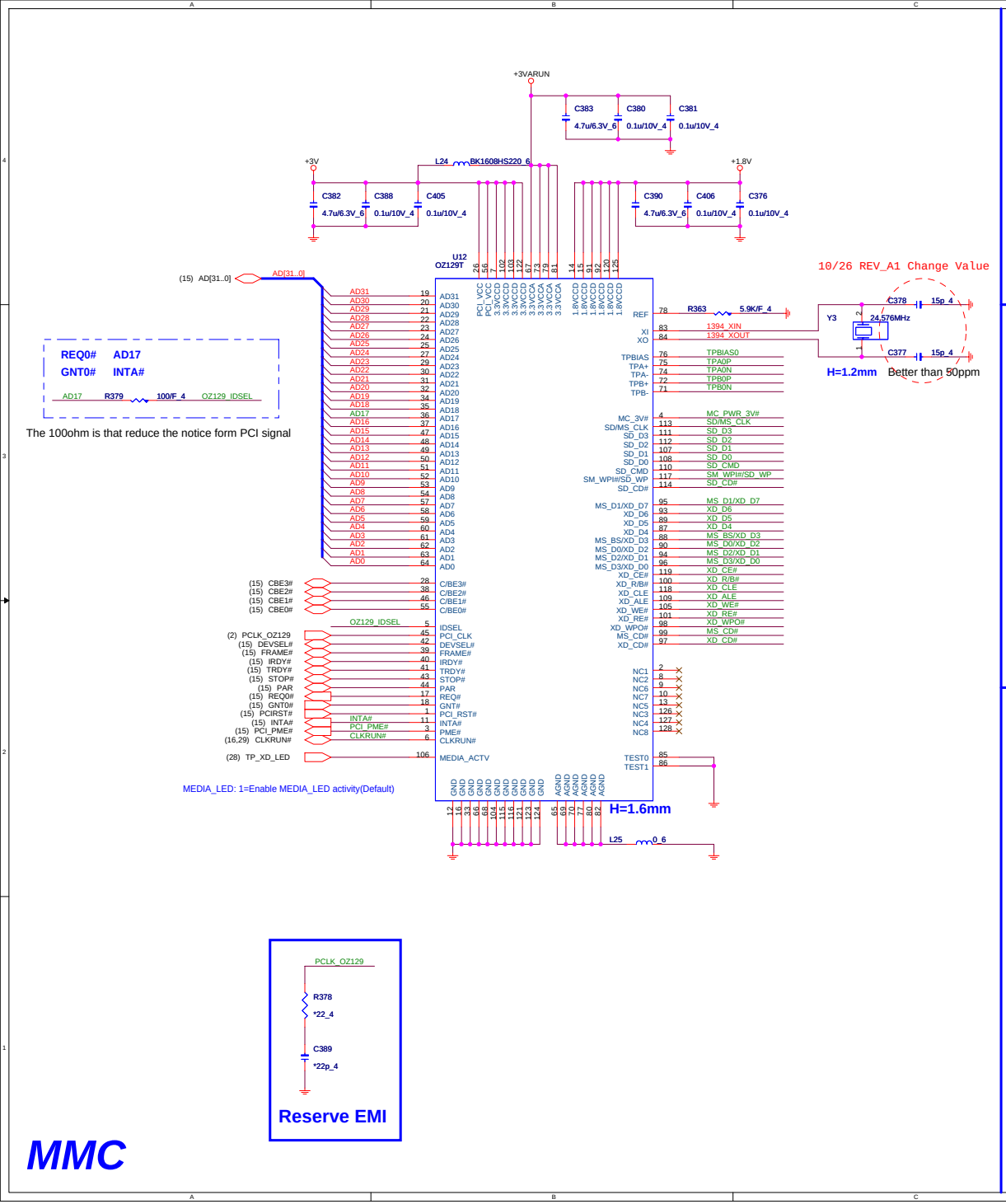
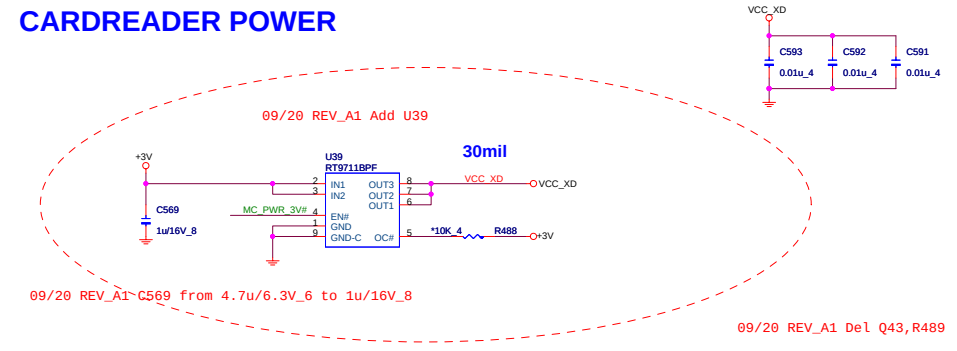
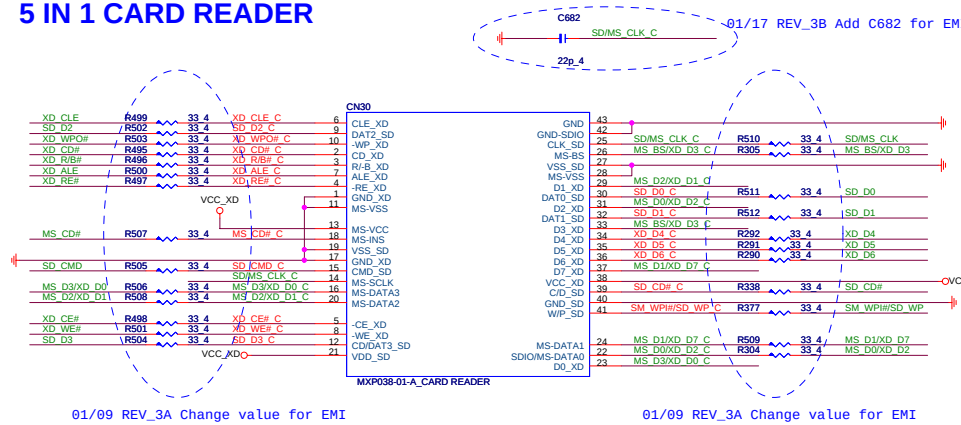


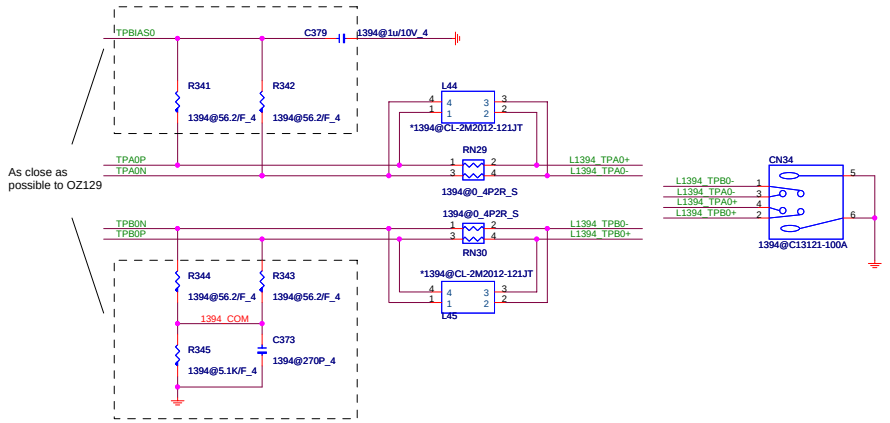
CARDREADER POWER



5 IN 1 CARD READER



1394



Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	OZ129T (Card Reader/1394)	1A

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LAN_MARVELL_88E8040/88E8055/88E8072

10/100 : 88E8040 P/N : AL008040001
GIGA : 88E8055 P/N : AJ080550000
GIGA : 88E8072 P/N : AL008072000

U32 — 88E805X (MARVELL)

(15) PCIE_RXN2 / (15) PCIE_RXP2 / (15) PCIE_TXN2 / (15) PCIE_TXP2 — C581 0.1u/10V_4, C578 0.1u/10V_4 — PCIE_RXN2_C, PCIE_RXP2_C — TX_N, TX_P, RX_N, RX_P

(2) CLK_PCIE_LAN# / (2) CLK_PCIE_LAN — REFCLKN, REFCLKP

SPI_DI, SPI_DO, SPI_CLK, SPI_CS

+3V_S5 — R491 40@4.7K_4 — PU_VDDO_TTL — PU_VDDO_TTL, CLKREQn

VPD_DATA, VPD_CLK

(15,16,20,21,22,25,28,29) PLTRST# — R518 0_4 — PERSTn/TSTPT

(16,25,28) PCIE_WAKE# — WAKEn

R517 2K/F_4 — LAN_RSET — RSET

TESTMODE

+3V / +3V_S5 — VMAIN_AVLBL, VAUX_AVLBL

SWITCH_VAUX, SWITCH_VCC

+3V_S5 — R519 4.7K_4 — LOM_DISABLE# — LOM_DISABLEn

(29) LOM_DISABLE — D6 *BAS316

LAN_XIN, LAN_XOUT — XTALI, XTALO

GND10, GND1, GND2, GND3, GND4, GND5, GND6, GND7, GND8, GND9

88E8040T

VDDO_TTL, VDD_TTL, AVDDH → +3V_S5

AVDD, AVDDL, NC, VDD25, CTRL18 → +2.5V_1.8V_LAN

VDD, CTRL12, TSTPT, HSDACN, HSDACP → +1.2V_LAN

LED_ACTn, LED_LINK10/100n, LED_LINK1000n, LED_LINKn — 100MBPS# R514 *0_4, 1000MBPS# R515 *0_4, 10_1000MBPS# R516 0_4 — LAN_ACTLED#, LAN_LINKLED#

MDIN[3:0], MDIP[3:0] — TX3N, TX3P, TX2N, TX2P, TX1N, TX1P, TX0N, TX0P

LAN_RSET
2K Ohm for 8040
4.87K Ohm for 8055/8072

12/05 REV_3A Add D6

10/24 REV_A1 Add

C605 27p_4 — LAN_XIN
Y6 25MHz-S — H = 0.8mm
C604 27p_4 — LAN_XOUT

10/24 REV_A1 Modify

DELTA ~~10/100 : LFE8696-R P/N : DB0MA8LAN00~~
H = 4mm ~~GIGA : LFE9249-R P/N : DB0ZR1LAN11~~

HWS ~~10/100 : HPL-4001B P/N : DB0SA1LAN01~~
H = 4mm GIGA : HPL-68 P/N : DB0ZB1LAN12

BOTHHAND 10/100 : TST1284 LF P/N : DB0KN7LAN24
H = 4mm ~~GIGA : GST5009-LF P/N : DBKN1NLAN03~~

U6 TRANSFORMER
+2.5V_1.8V_LAN, TX3P, TX3N, TX2P, TX2N, TX1P, TX1N, TX0P, TX0N
TCT1/TD1+/TD1-/MCT1/MX1+/MX1-, TCT2/TD2+/TD2-/MCT2/MX2+/MX2-, TCT3/TD3+/TD3-/MCT3/MX3+/MX3-, TCT4/TD4+/TD4-/MCT4/MX4+/MX4-
TERM4, TERM3, TERM2, TERM1 — X-TX3P, X-TX3N, X-TX2P, X-TX2N, X-TX1P, X-TX1N, X-TX0P, X-TX0N
C266 0.1u/16V_4 — C241 1000p_4
C232 1000p/3KV_1808 — TERM9
R208 75/F_4, R220 75/F_4, R230 *55_72@75/F_4, R235 *55_72@75/F_4

TERMINATION PLANE

+3V_S5 — L20 55_72@BK1608HS220_6_1A — AUX3V_S5

C274 10u/6.3V_8, C611 0.1u/16V_4, C598 0.1u/16V_4, C607 0.1u/16V_4, C610 0.1u/16V_4, C573 0.1u/16V_4

C239 55_72@4.7u/6.3V_6, C235 55_72@0.1u/16V_4

R215 55_72@4.7K_4 — CTRL18 — Q15 55_72@BCP69T1

25 mil Trace width

C240 55_72@4.7u/6.3V_6

+2.5V_1.8V_LAN: C586 0.1u/16V_4, C579 0.1u/16V_4, C595 0.1u/16V_4, C600 0.1u/16V_4, C594 0.1u/16V_4, C587 0.1u/16V_4, C590 0.1u/16V_4, C603 40@4.7u/6.3V_6

C261 55_72@4.7u/6.3V_6, C254 55_72@0.1u/16V_4

R239 55_72@4.7K_4 — CTRL12 — Q16 55_72@BCP69T1

25 mil Trace width

C263 55_72@4.7u/6.3V_6

+1.2V_LAN: C608 0.1u/16V_4, C612 0.1u/16V_4, C596 0.1u/16V_4, C609 0.1u/16V_4, C574 0.1u/16V_4, C572 0.1u/16V_4, C576 0.1u/16V_4, C575 0.1u/16V_4, C571 40@4.7u/6.3V_6

RN28 55/49.9/F_4P2R — LAN_N1 — C601 55@0.1u/16V_4, C602 55@1000p_4
RN27 55/49.9/F_4P2R — LAN_N2 — C599 55@0.1u/16V_4, C597 55@1000p_4
RN26 55/49.9/F_4P2R — LAN_N3 — C588 55@0.1u/16V_4, C589 55@1000p_4
RN25 55/49.9/F_4P2R — LAN_N4 — C584 55@0.1u/16V_4, C582 55@1000p_4

12/10 REV_3A DNI R485,R484,U7
Mount R481

+3V_S5 — R485 *4.7K_4, R484 *4.7K_4
VPD_DATA, VPD_CLK
U7 *24LC08 — SDA, SCL, WP, GND, VCC, A0, A1, A2
R481 0_4

EEPROM No Use
VPD_DATA Pull Down

CN26 RJ45-CONN
+3V_S5 — R189 220_4 — LAN_ACTLED#, LAN_VCC3
C222 470p/50V_4 — LAN_ACTLED#
C248 470p/50V_4 — LAN_LINKLED#
C221 470p/50V_4 — +3V_S5
X-TX3N, X-TX3P, X-TX1N, X-TX2N, X-TX2P, X-TX1P, X-TX0N, X-TX0P
+3V_S5 — R243 220_4 — LAN_VCC4, LAN_LINKLED#
GND, GND — R473, R240

01/16 REV_3B change footprint

Quanta Computer Inc.
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Mini PCI-E Card
WLAN

MINI-Card I

09/28 REV_A1 Modify

02/15 REV_3C Modify

10/26 REV_A1 Modify

09/28 REV_A1 Modify

CN19

minipal-c15706-52p-ldv

To BT

2N7002E-LF Q1

MINI-Card II

09/20 REV_A1 Modify

CN39

3G@minipal-c15706-52p-ldv

MINI-Card III

CN33

minipal-c15706-52p-ldv

01/18 REV_3B Add PAD

PAD1 EMIPAD

12/07 REV_3A Add

EMI

12/07 REV_3A Add

H= 8mm

Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	MINI PCIE/HOLE	1A

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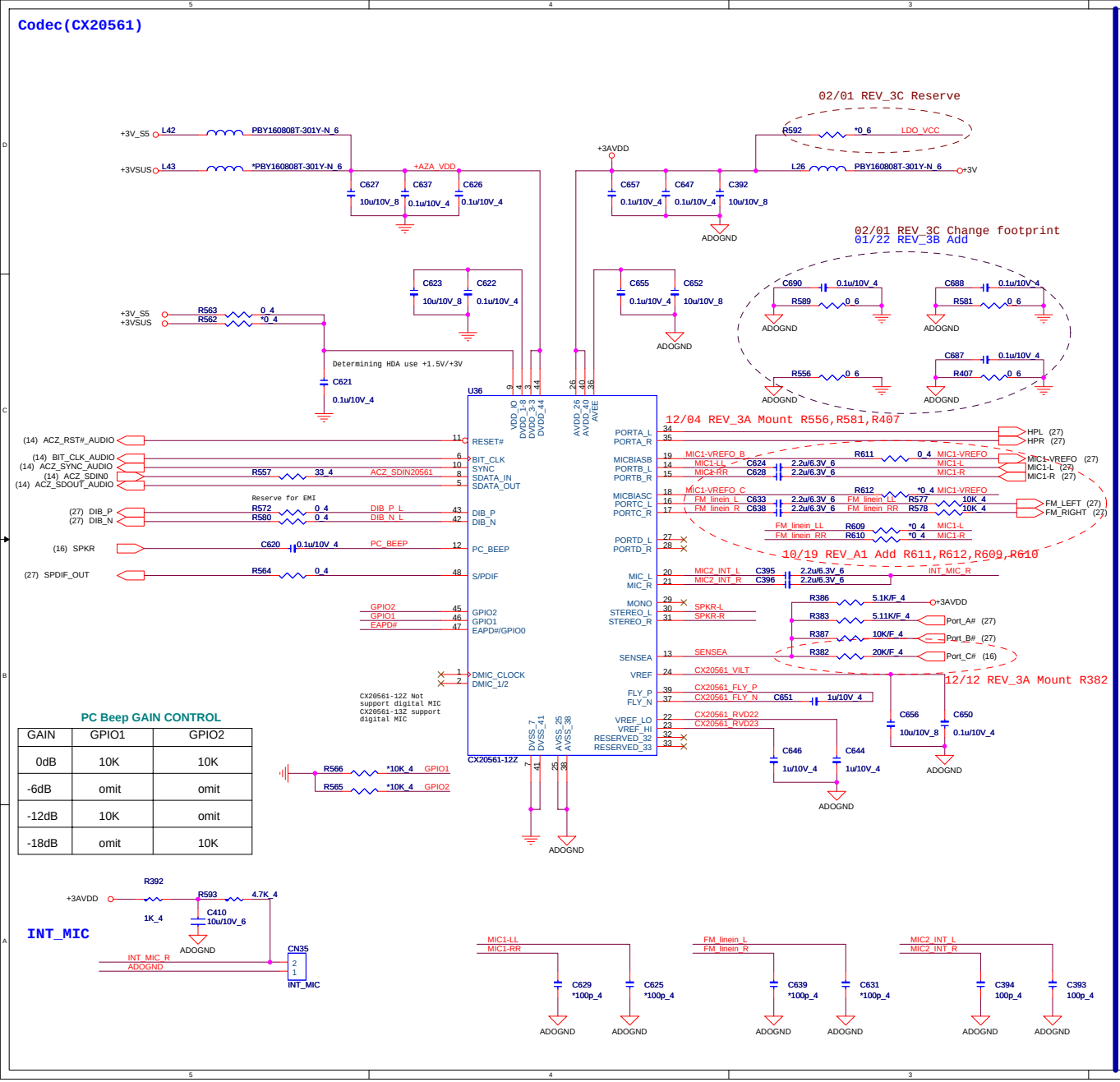
Codec(CX20561)

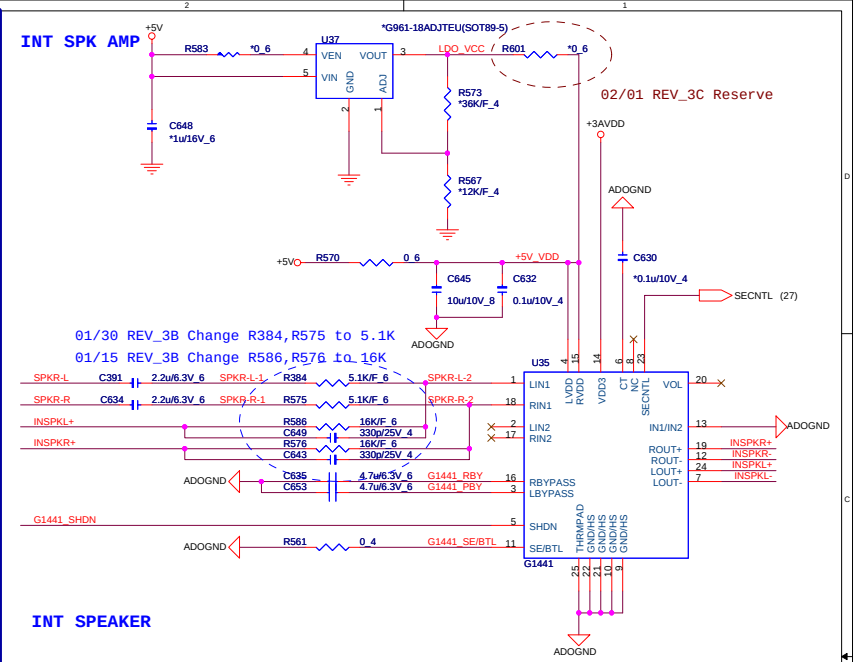


PC Beep GAIN CONTROL

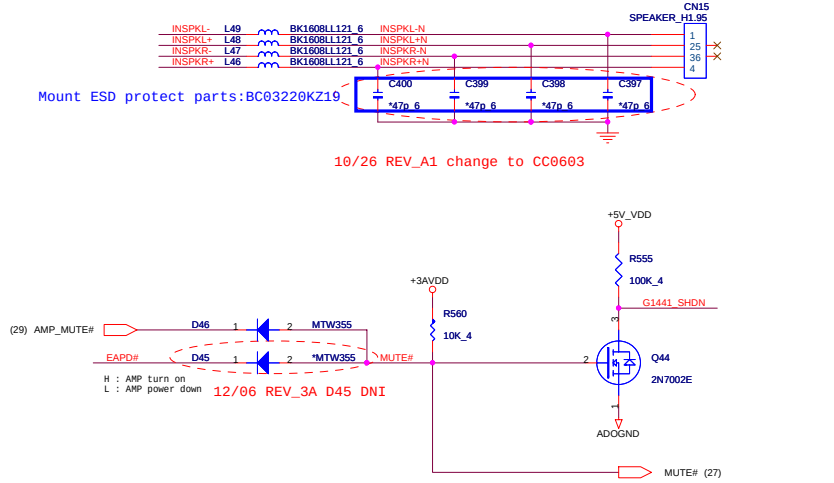
GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

INT_MIC

INT SPK AMP



INT SPEAKER



Quanta Computer Inc.	
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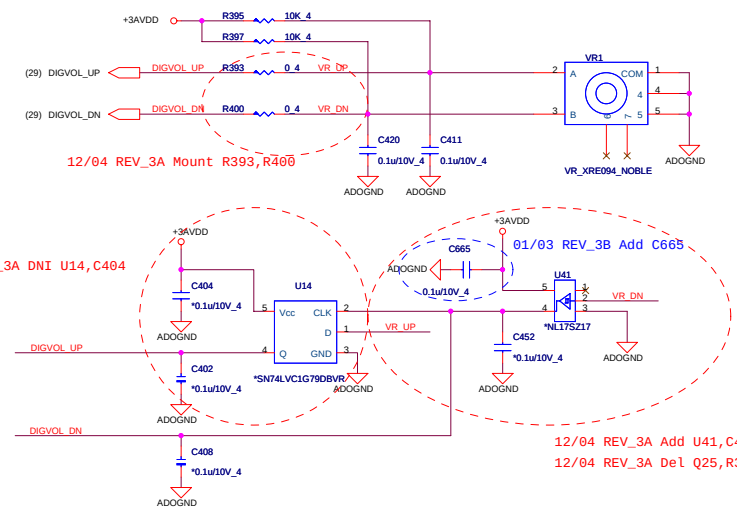
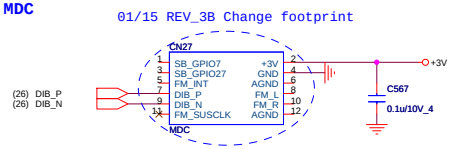
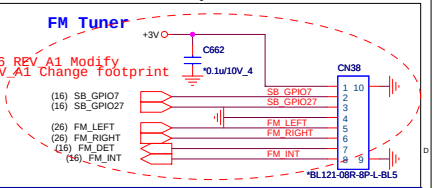
VR



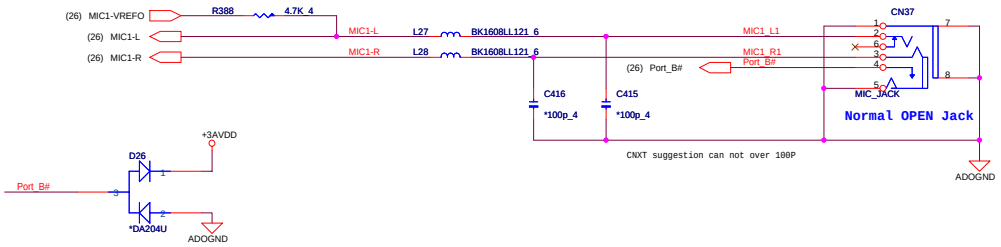
MDC



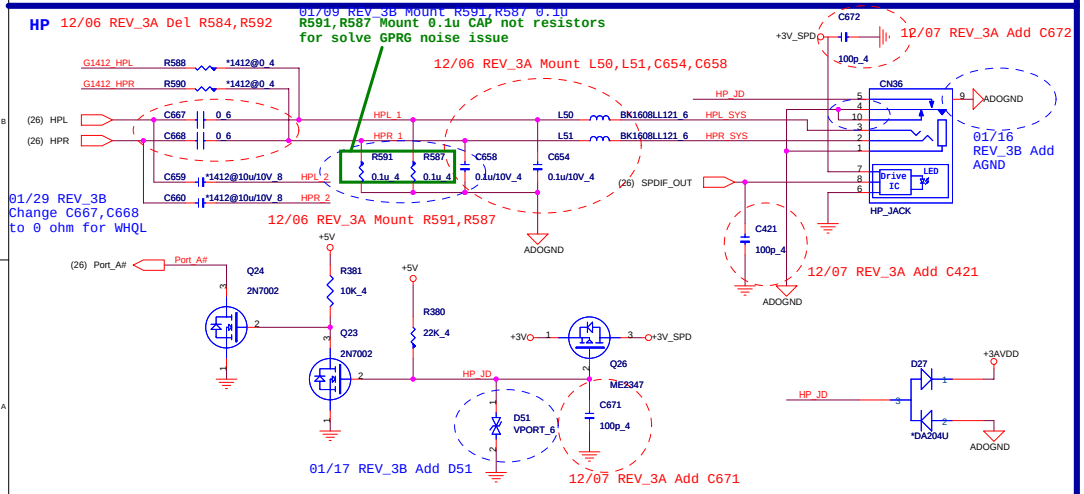
FM Tuner



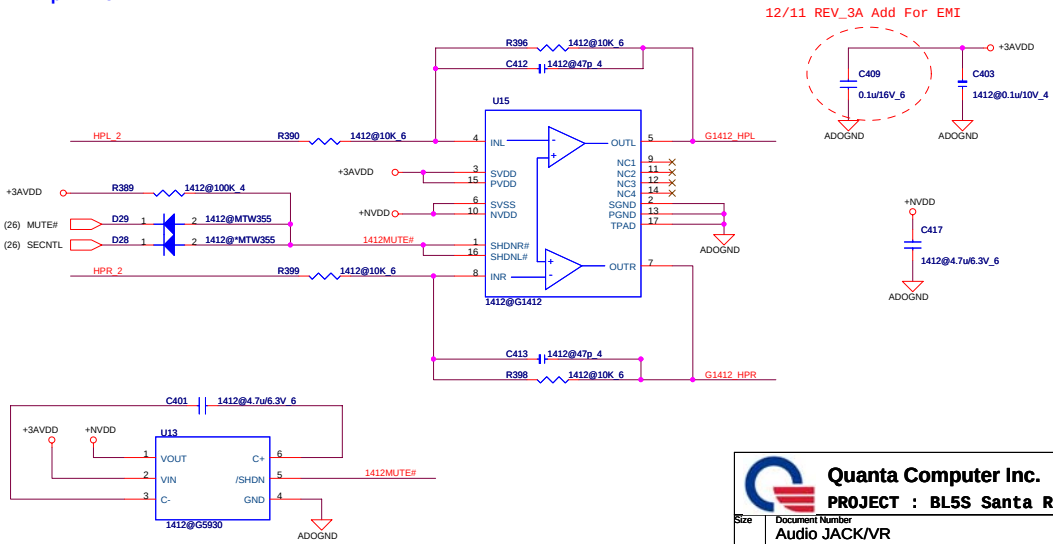
SYSTEM MIC



HP



HP Amplifier



Quanta Computer Inc.
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Size: Document Number: Audio JACK/VR Rev: 1A
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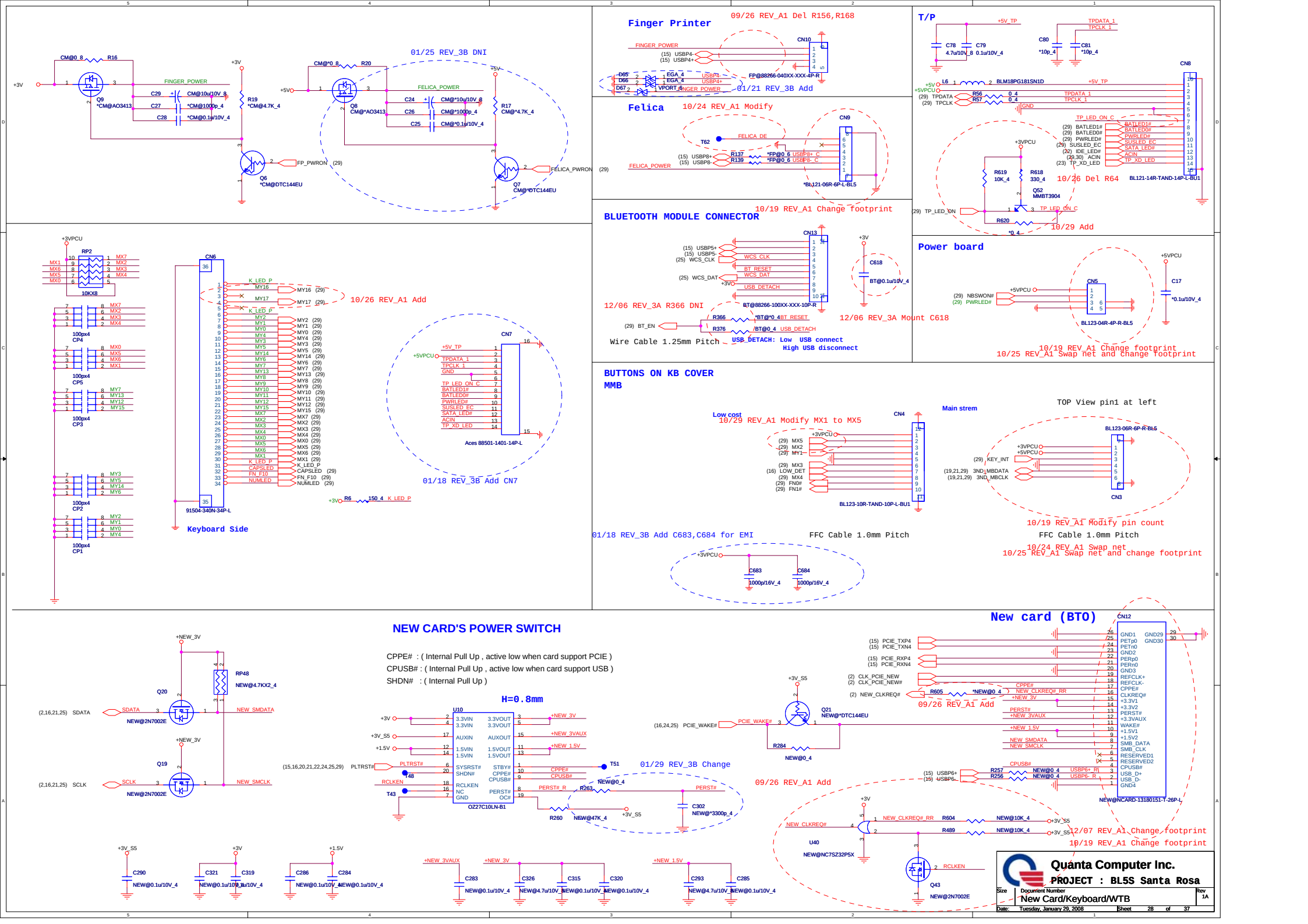
Finger Printer
09/26 REV_A1 Del R156,R168
01/21 REV_3B Add
T/P
Felica
10/24 REV_A1 Modify
10/19 REV_A1 Change footprint
BLUETOOTH MODULE CONNECTOR
12/06 REV_3A R366 DNI
12/06 REV_3A Mount C618
Wire Cable 1.25mm Pitch
USB_DETACH: Low USB connect
High USB disconnect
Power board
10/19 REV_A1 Change footprint
10/25 REV_A1 Swap net and change footprint
01/25 REV_3B DNI
10/26 REV_A1 Add
01/18 REV_3B Add CN7
Keyboard Side
BUTTONS ON KB COVER
MMB
Low cost
10/29 REV_A1 Modify MX1 to MX5
Main strem
TOP View pin1 at left
10/19 REV_A1 Modify pin count
FFC Cable 1.0mm Pitch
10/24 REV_A1 Swap net
10/25 REV_A1 Swap net and change footprint
01/18 REV_3B Add C683,C684 for EMI
FFC Cable 1.0mm Pitch
NEW CARD'S POWER SWITCH
CPPE# : (Internal Pull Up , active low when card support PCIE)
CPUSB# : (Internal Pull Up , active low when card support USB)
SHDN# : (Internal Pull Up)
H=0.8mm
01/29 REV_3B Change
New card (BTO)
09/26 REV_A1 Add
12/07 REV_A1 Change footprint
10/19 REV_A1 Change footprint
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
New Card/Keyboard/WTB
Tuesday, January 29, 2008
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SMBUS Table

SMBUS	Devices
1	Battery
2	CPU Thermal Sensor 3D Sensor EC EEPROM
3	VGA Board Thermal Sensor Touch Sensor

10/26 REV_A1 Add R64,R73,R176

09/20 REV_A1 Modify

09/29 REV_A1 Modify

10/26 REV_A1 Modify

10/22 REV_A1 Modify

10/24 REV_A1 Add

09/20 REV_A1 Modify

01/08 REV_3B Add to control MMB LED

10/22 REV_A1 Modify

SM BUS PU

I/O Base Address

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

12/05 REV_3A R38 DNI,R47 mount

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID

H=1.75mm

ADDRESS: A0H

SPI FLASH

H=2.16mm

INTERNAL KEYBOARD STRIP SET

CIR (Copy from PB2A)

Only for 8769/775C

10/19 REV_A1 Change footprint
10/21 REV_A1 Change pin define
12/07 REV_3A Change P/N

WPC8763LDG:	AL008763B00
WPC8769LDG:	AJ087690F08
WPCE775L:	AJ007750F00
WPCE775C:	AJ007750F01

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Size	Document Number	Rev
	EC-WPCE775C	1A

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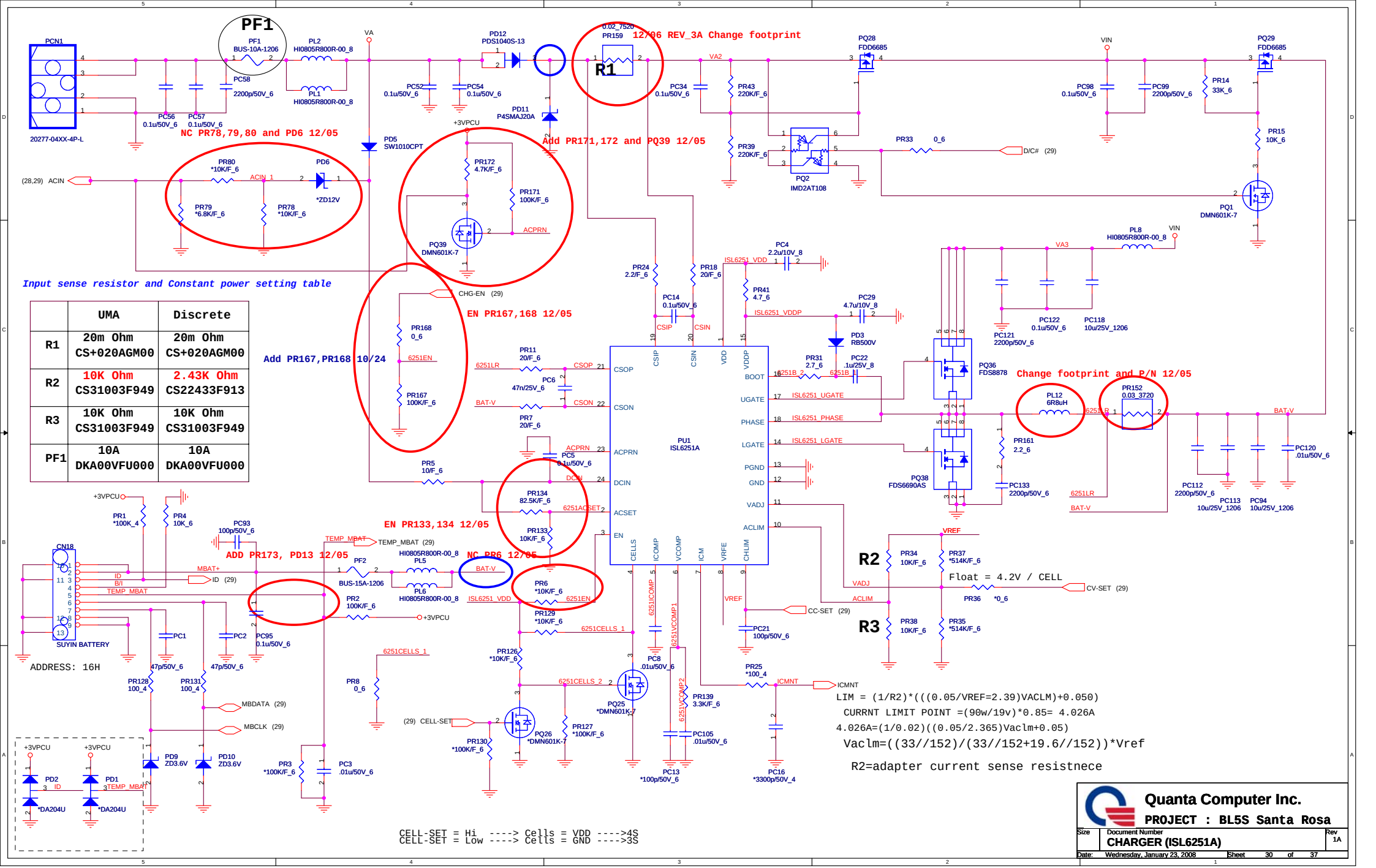

	UMA	Discrete
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	10K Ohm CS31003F949	2.43K Ohm CS22433F913
R3	10K Ohm CS31003F949	10K Ohm CS31003F949
PF1	10A DKA00VFU000	10A DKA00VFU000

Quanta Computer Inc.
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Size	Document Number	Rev
	CHARGER (ISL6251A)	1A

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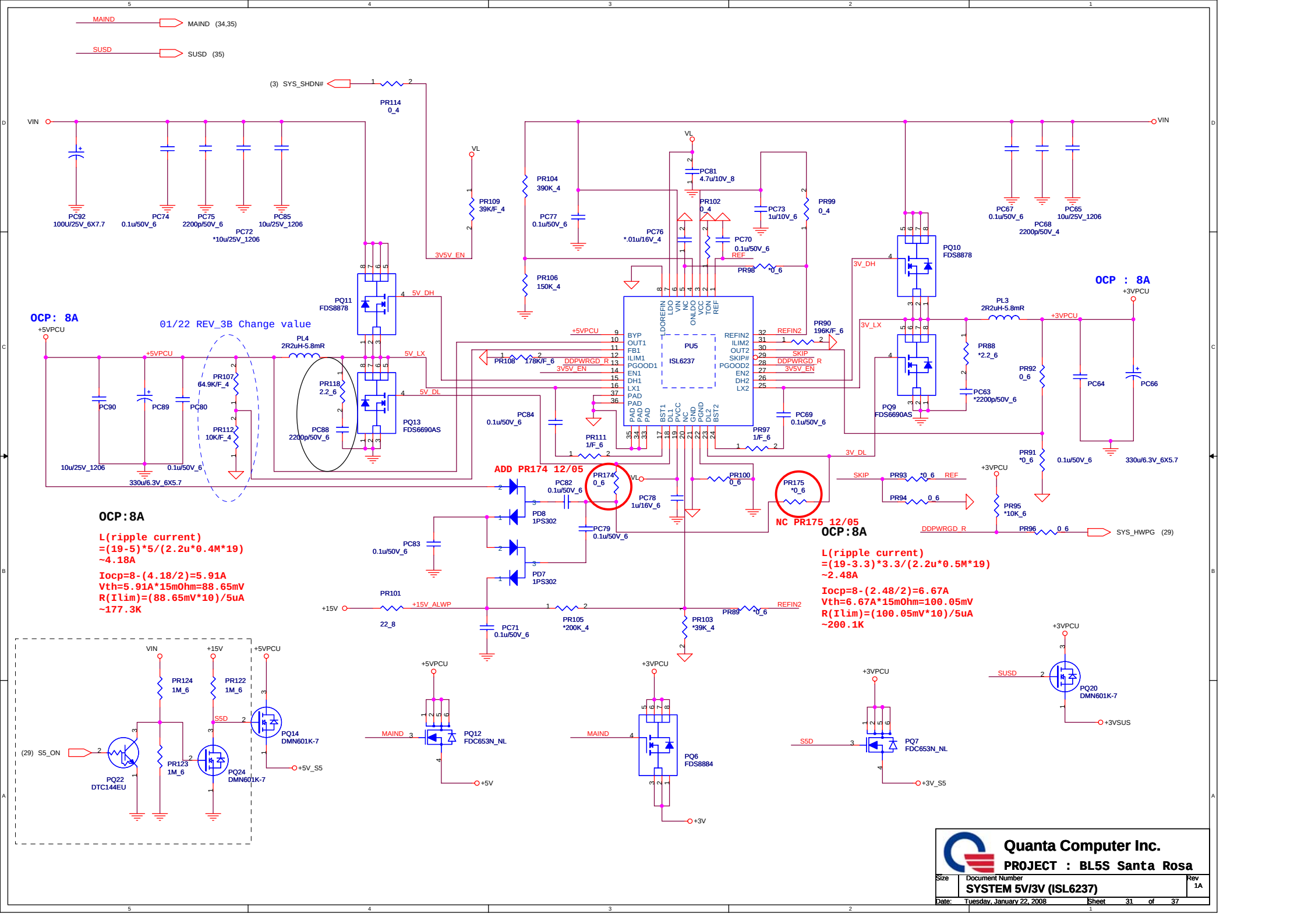
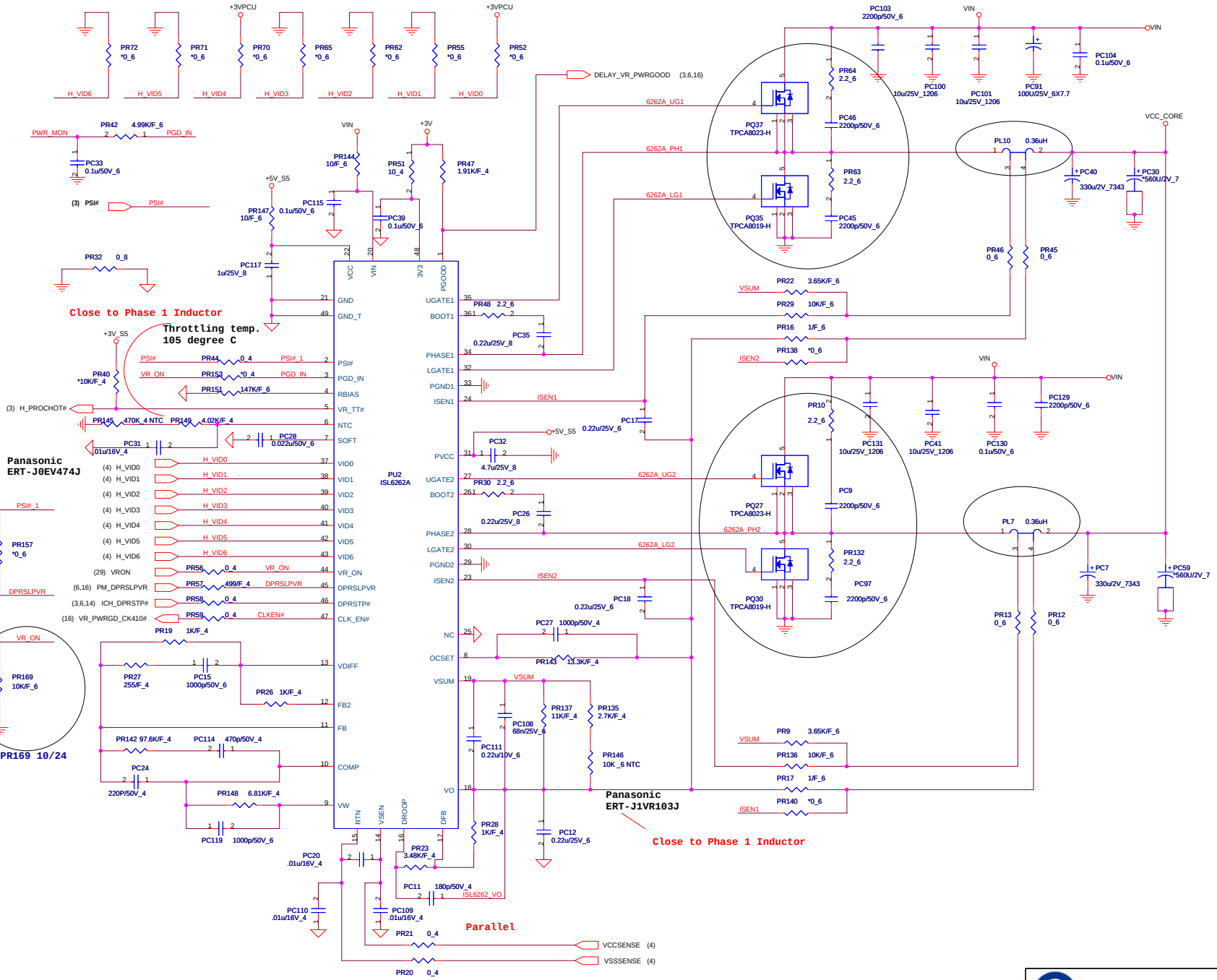
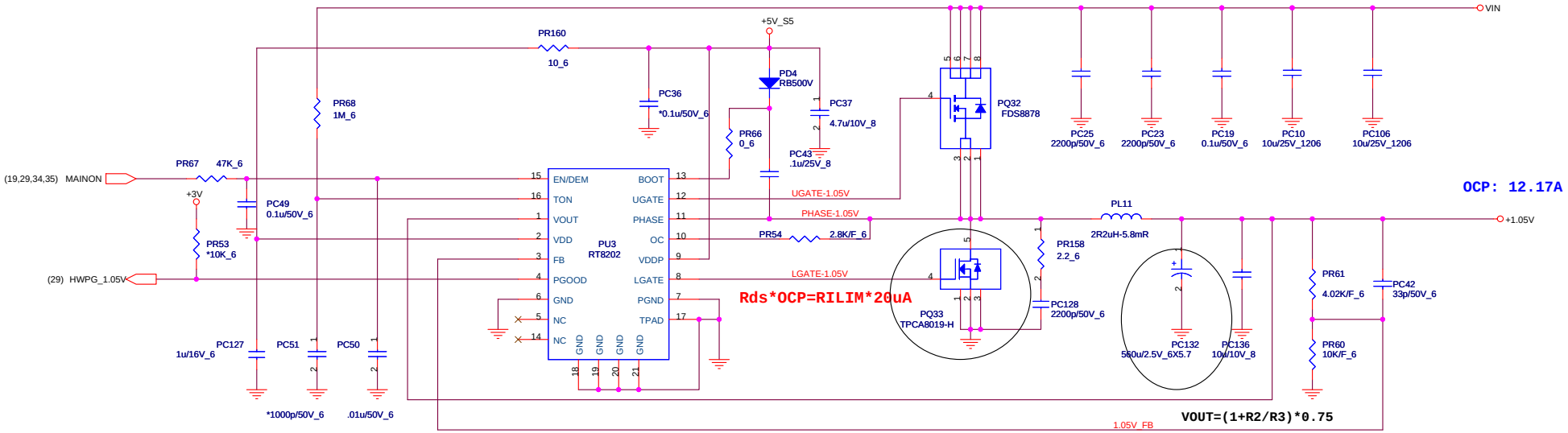

MAIND
MAIND (34,35)
SUSD
SUSD (35)
(3) SYS_SHDN#
PR114 0_4
VIN
VL
3V5V_EN
PR109 39K/F_4
PR104 390K_4
PR77 0.1u/50V_6
PR106 150K_4
PC92 100U/25V_6X7.7
PC74 0.1u/50V_6
PC75 2200p/50V_6
PC72 *10u/25V_1206
PC85 10u/25V_1206
PC81 4.7u/10V_8
PR102 0_4
PC73 1u/10V_6
PR99 0_4
PC76 *.01u/16V_4
PC70 0.1u/50V_6
REF
PR98 *0_6
PC67 0.1u/50V_6
PC68 2200p/50V_4
PC65 10u/25V_1206
PQ10 FDS8878
3V_DH
OCP : 8A
+3VPCU
PL3 2R2uH-5.8mR
3V_LX
PR88 *2.2_6
PC63 *2200p/50V_6
PR92 0_6
PC64
PC66
PQ9 FDS6690AS
PR91 *0_6
0.1u/50V_6
330u/6.3V_6X5.7
PQ11 FDS8878
5V_DH
OCP: 8A
01/22 REV_3B Change value
+5VPCU
PL4 2R2uH-5.8mR
5V_LX
PR107 64.9K/F_4
PR118 2.2_6
PR112 10K/F_4
PC88 2200p/50V_6
PQ13 FDS6690AS
5V_DL
PC90
PC89
PC80
10u/25V_1206
0.1u/50V_6
330u/6.3V_6X5.7
PR108 178K/F_6
DDPWRGD_R
3V5V_EN
PU5 ISL6237
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD
LDOREFIN LDO VIN NC ONLOCC VCC TON REF
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DL1 PVCC NC GND GND DL2 BST2
PR90 196K/F_6
REFIN2
SKIP
PC84 0.1u/50V_6
PR111 1/F_6
PC69 0.1u/50V_6
PR97 1/F_6
3V_DL
ADD PR174 12/05
PR174 0_6
PC82 0.1u/50V_6
PD8 1PS302
PC78 1u/16V_6
PR100 0_6
PR175 *0_6
NC PR175 12/05
SKIP
PR93 *0_6
REF
PR94 0_6
PR95 *10K_6
DDPWRGD_R
PR96 0_6
SYS_HWPG (29)
OCP:8A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=8-(4.18/2)=5.91A
Vth=5.91A*15mOhm=88.65mV
R(Ilim)=(88.65mV*10)/5uA
~177.3K
PC79 0.1u/50V_6
PC83 0.1u/50V_6
PD7 1PS302
PR101
+15V
+15V_ALWP
22_8
PR105 *200K_4
PC71 0.1u/50V_6
PR103 *39K_4
PR89 *0_6
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=100.05mV
R(Ilim)=(100.05mV*10)/5uA
~200.1K
PR124 1M_6
PR122 1M_6
S5D
(29) S5_ON
PR123 1M_6
PQ22 DTC144EU
PQ24 DMN601K-7
PQ14 DMN601K-7
+5V_S5
+5VPCU
MAIND
PQ12 FDC653N_NL
+5V
+3VPCU
PQ6 FDS8884
+3V
PQ7 FDC653N_NL
+3V_S5
SUSD
PQ20 DMN601K-7
+3VSUS
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
Size
Document Number
SYSTEM 5V/3V (ISL6237)
Rev 1A
Date: Tuesday, January 22, 2008
Sheet 31 of 37



Quanta Computer Inc.			
PROJECT : BL5S Santa Rosa			
Size	Document Number		Rev
	CPU CORE(ISL6262A)		1A
Date: Tuesday, January 22, 2008		Sheet 32 of 37	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

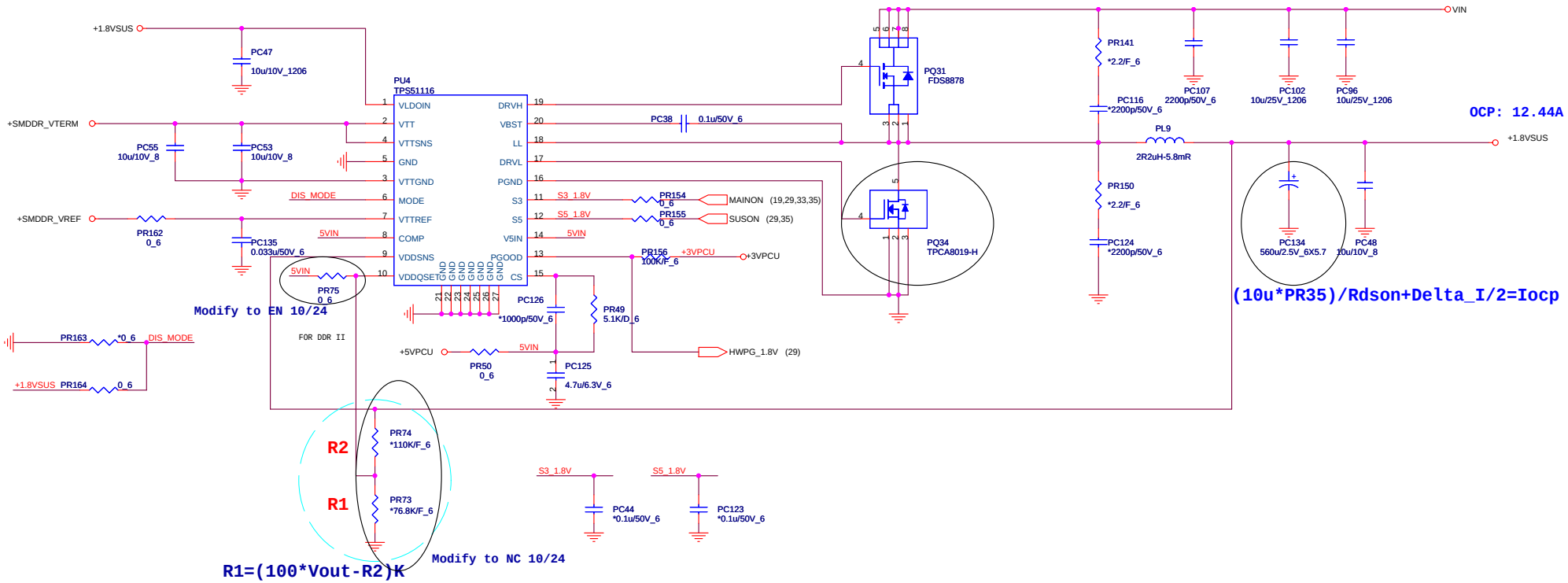
AOL1412 Rds=4.6mOhm
12.17A OCP --- OC=2.8K

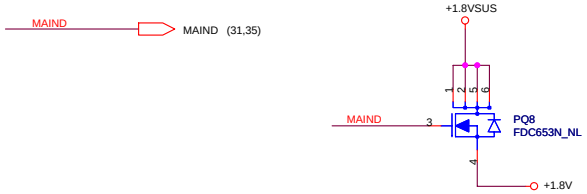
SI7636 Rds=4.8mOhm
11.67A OCP --- OC=2.8K

Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

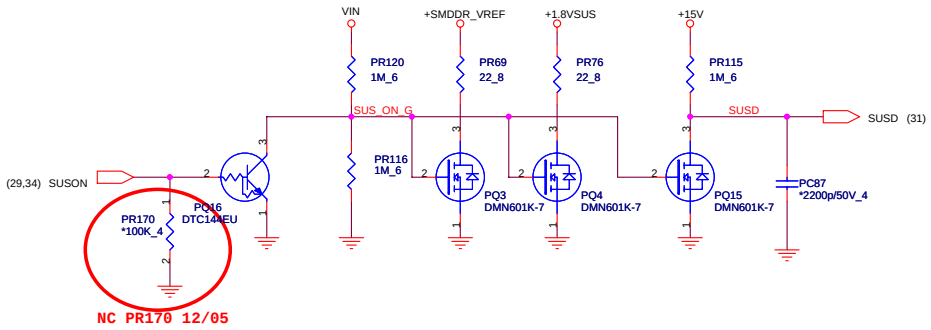
Size	Document Number	Rev
	VTT 1.05V (RT8202)	1A

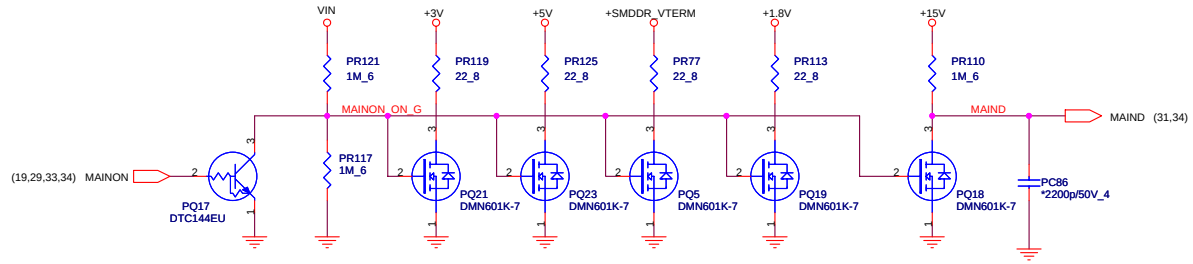
Date: Tuesday, January 22, 2008 Sheet 33 of 37

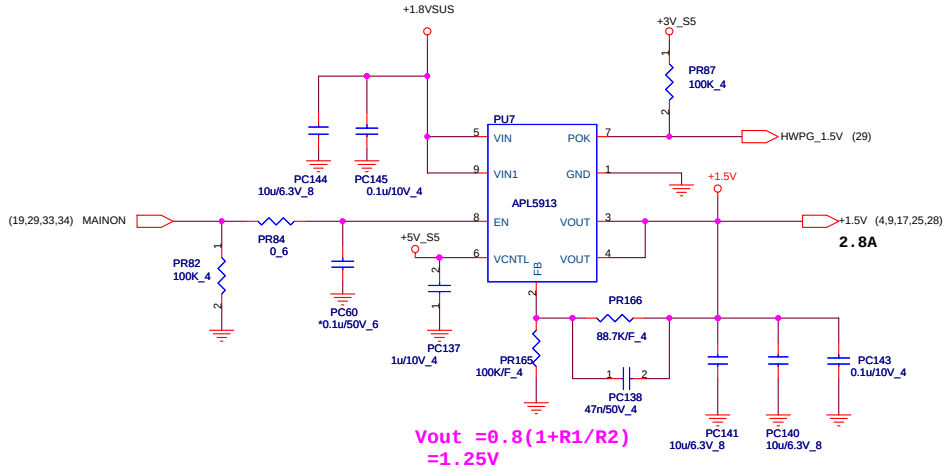


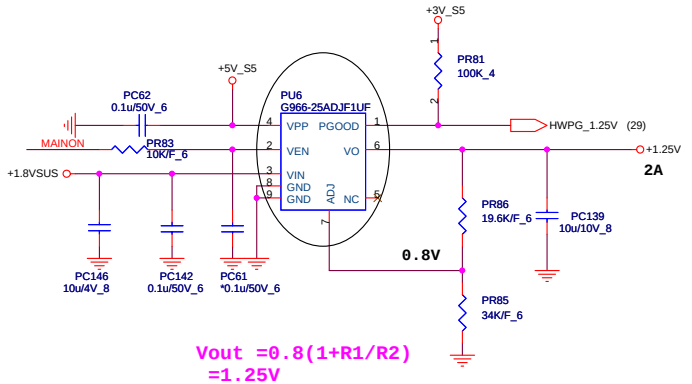


Quanta Computer Inc.		
PROJECT : BL5S Santa Rosa		
Size	Document Number: DDR 1.8V(TPS51116)	Rev: 1A
Date: Tuesday, January 22, 2008	Sheet 34 of 37	









Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	Discharge (1.25V/1.5V)	1A
Date: Tuesday, January 22, 2008	Sheet 35 of 37	

Model	REV	DATE	CHANGE LIST	NOTE
BL5S	00	20070824	FIRST RELEASED : 20070824	
	1A	20070914	FIRST RELEASED : E200709-2519	

Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	Change List	1A

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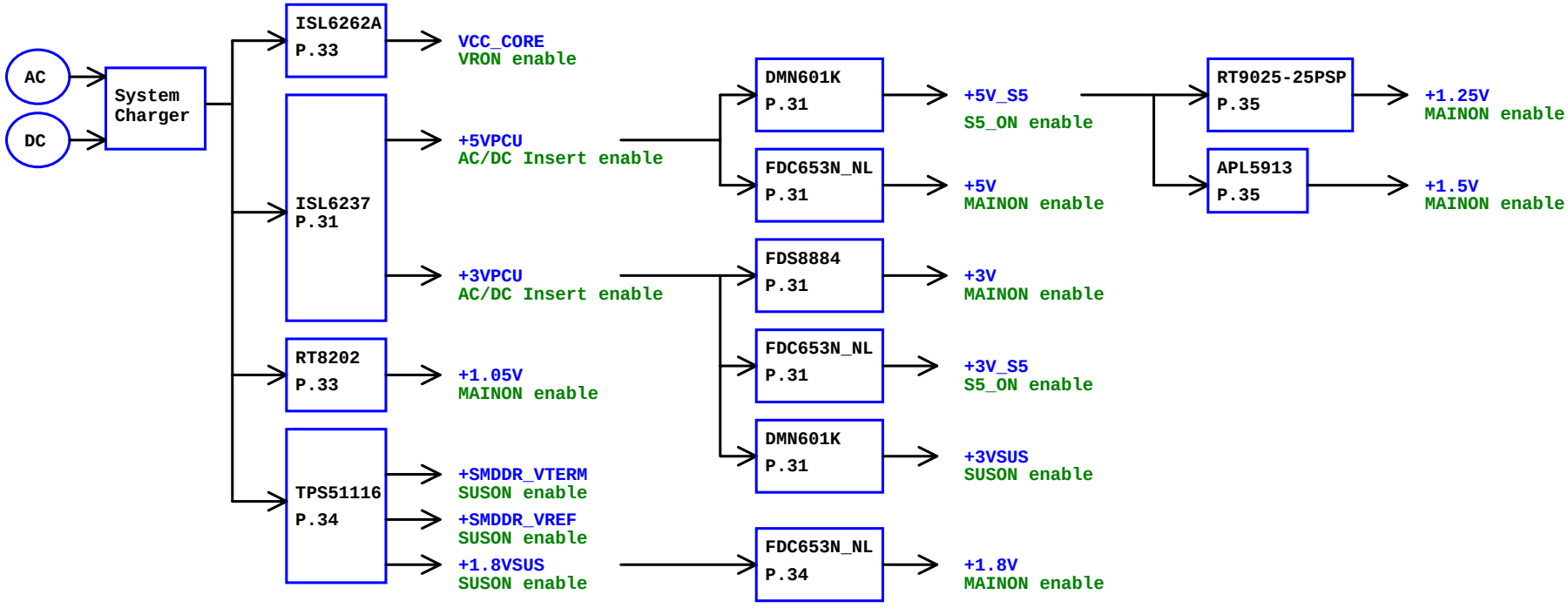

Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+1.8VSUS	GMCH, DDR
+SMDDR_VREF	GMCH, DDR
+SMDDR_VTERM	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T) Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	HDMI, Cardreader (OZ129T)
+1.25V	CLK, GMCH, ICH8M