

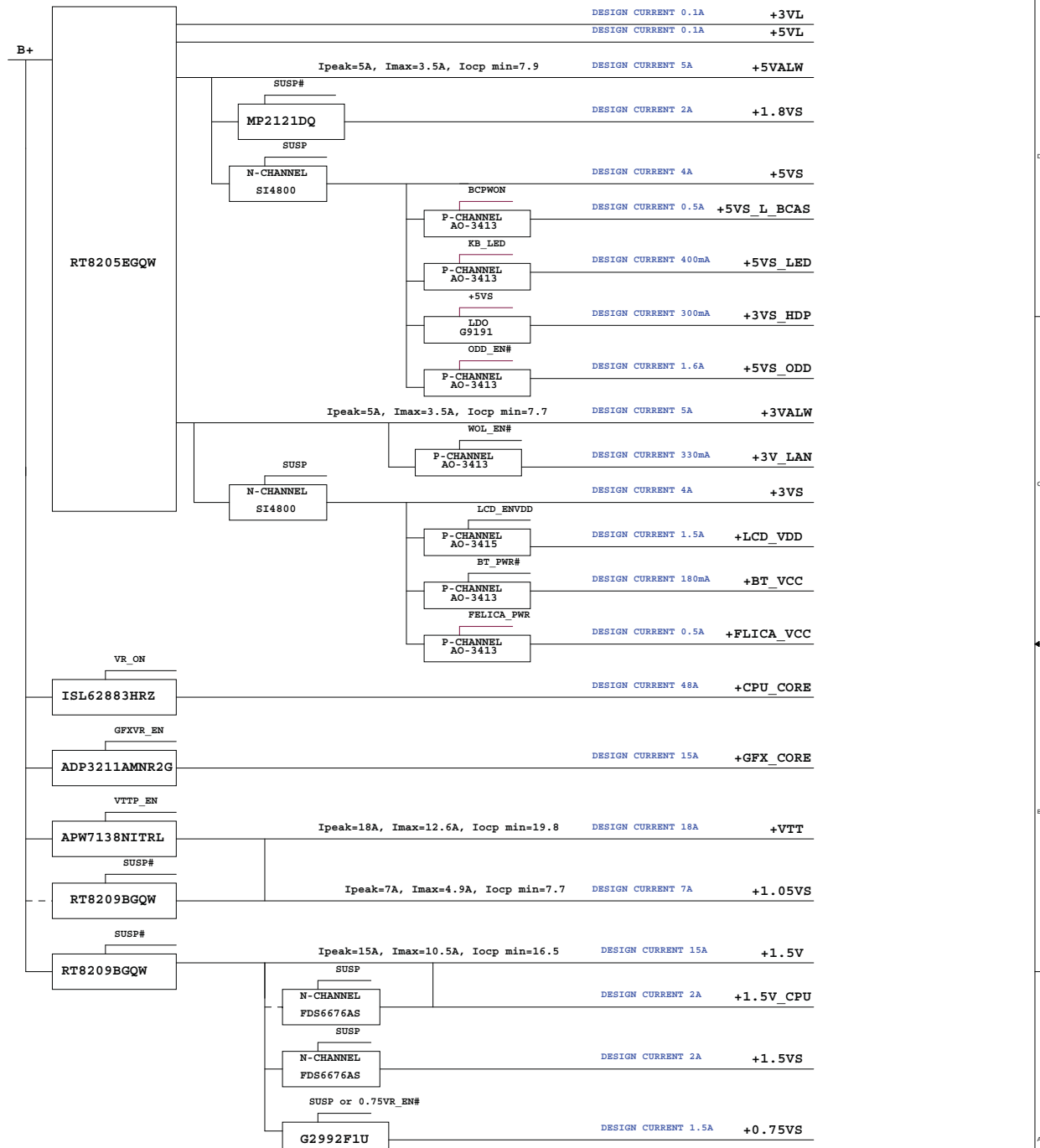
NWQAA

Marseille 10

LA-6061P REV 2.0 Schematic

Intel Processor (ARD) / PCH (HM55)
2010-03-24 Rev 2.0

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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b	+3VS	G-Sensor	40 H	0100 0000 b
				+3VS	Light Sensor	52 H	0101 0010 b
Power	Device	HEX	Address				
+3VL	Cap. Sensor		Virtual I2C				

BTO Option Table

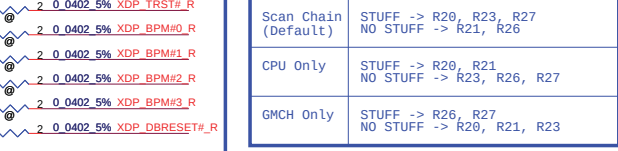
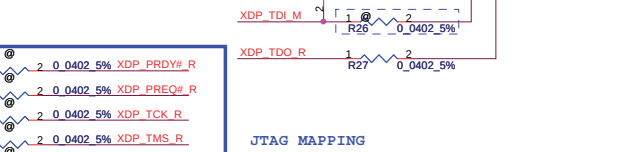
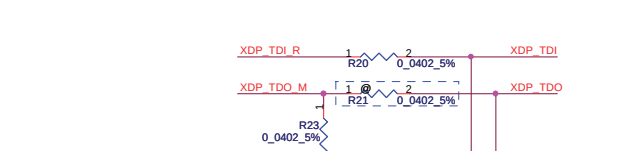
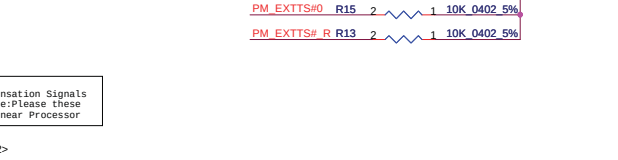
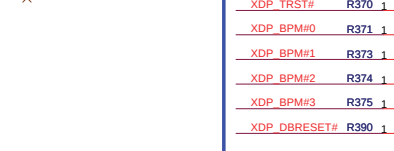
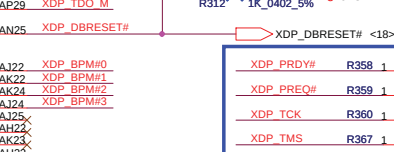
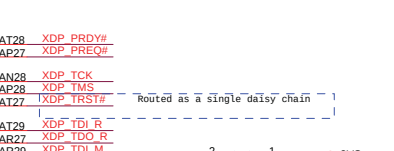
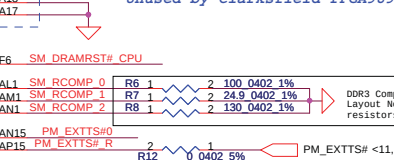
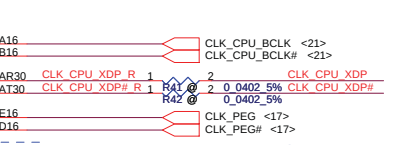
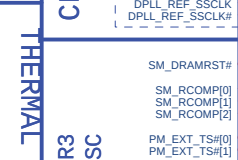
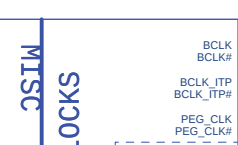
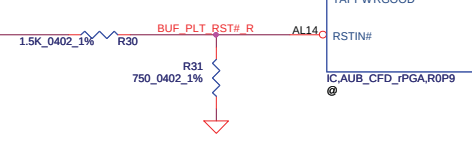
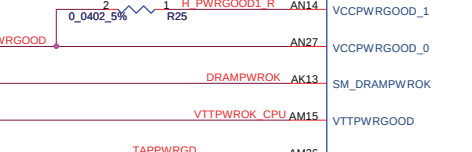
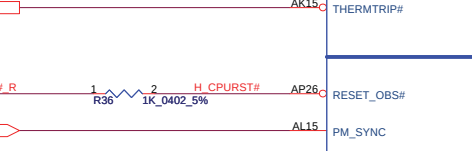
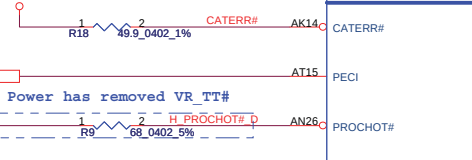
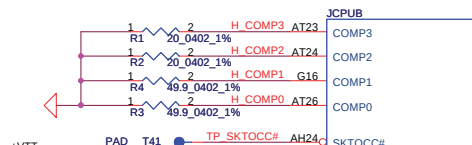
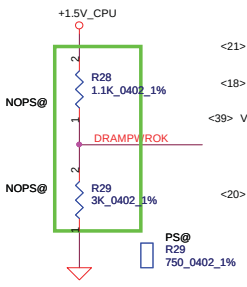
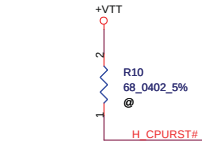
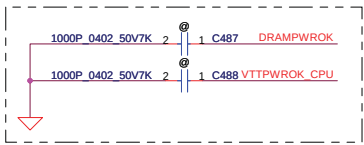
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description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FPE@	MDC@	CIR@	KBL@

Function	Felica	BLUE TOOTH	G-SENSOR	Camera & Mic	HDMI		Card reader	
description	Felica	BLUE TOOTH	G-SENSOR	Camera & Mic	HDMI		JMB385C/389C	
explain	Felica	BLUE TOOTH	G-SENSOR	Camera & Mic	UMA	CEC	JMB385C	JMB389C
BTO	FELICA@	BT@	GSENSOR@	CAM@	IHDMI@	CEC@	JMB385@	JMB389@

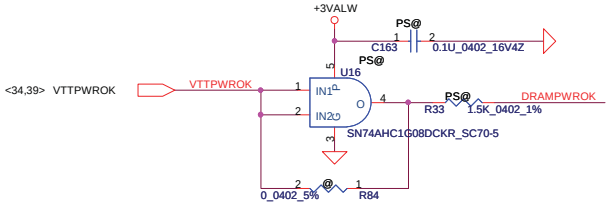
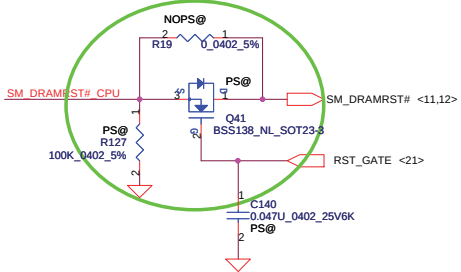
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description	S3 Power Saving		New Card
explain	No Power Saving	Power Saving	New Card
BTO	NOPS@	PS@	NEW@

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

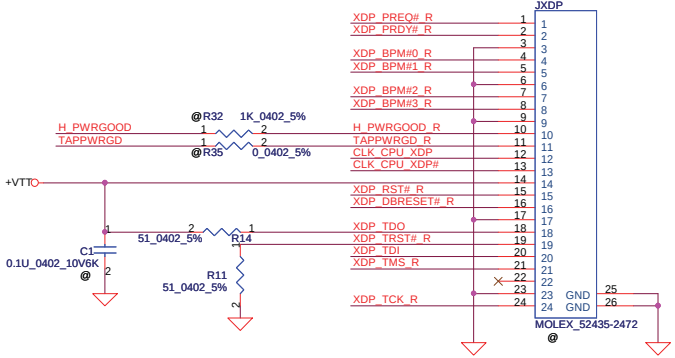
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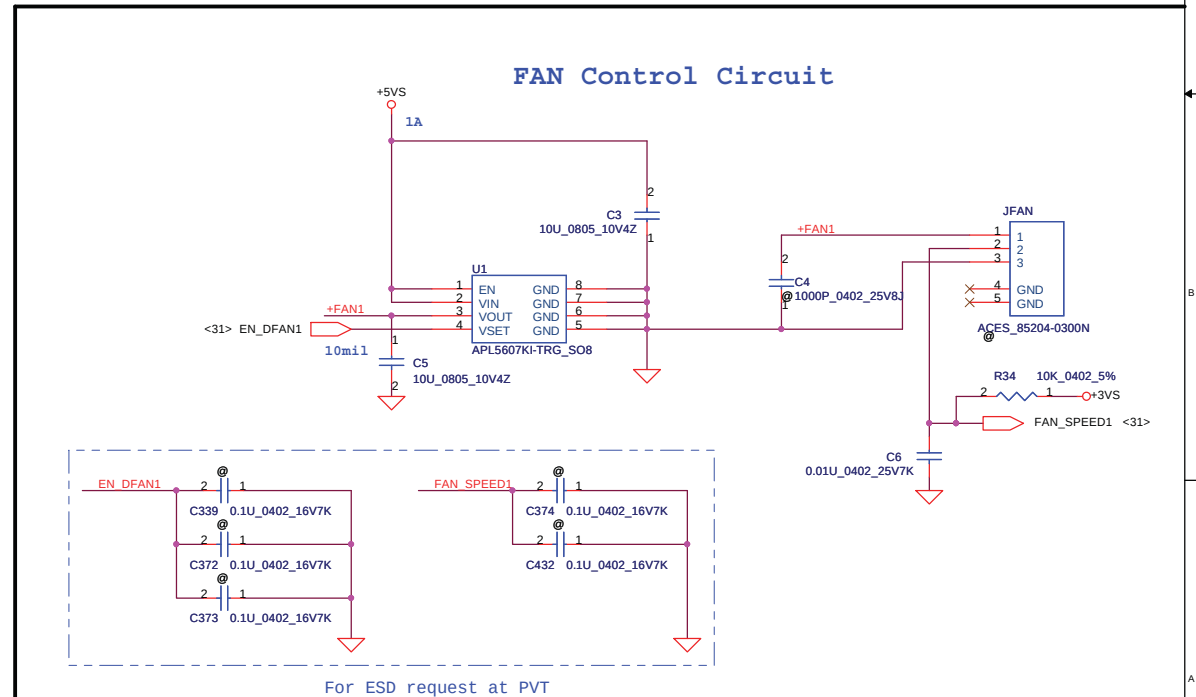
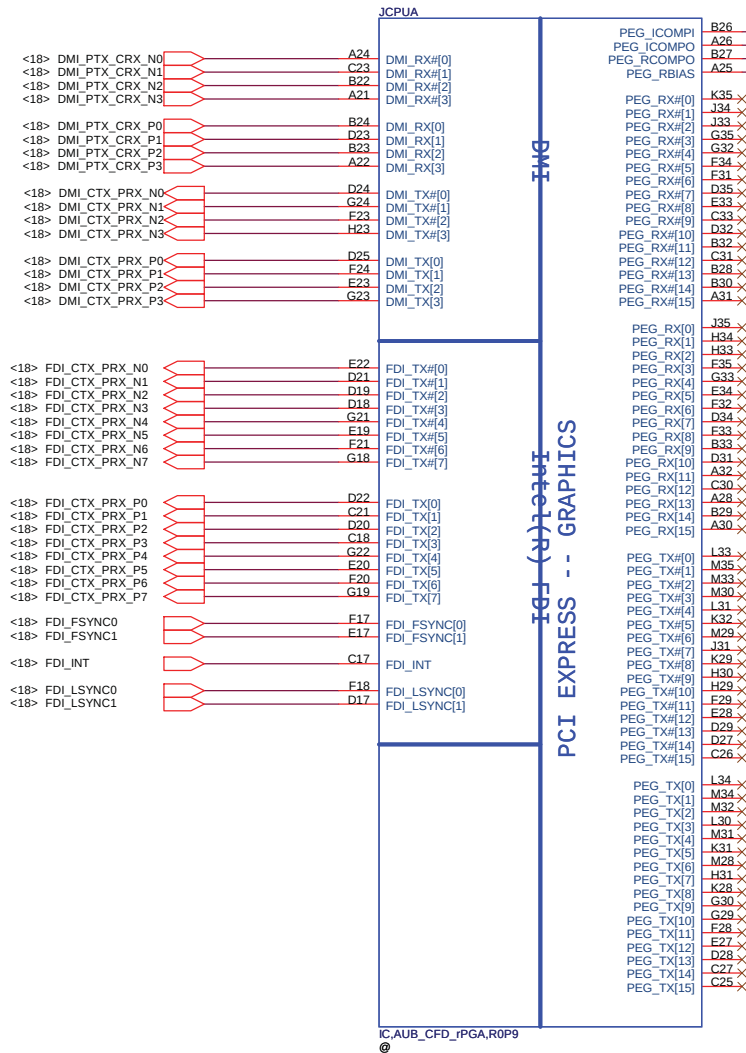
For S3 CPU Power Saving



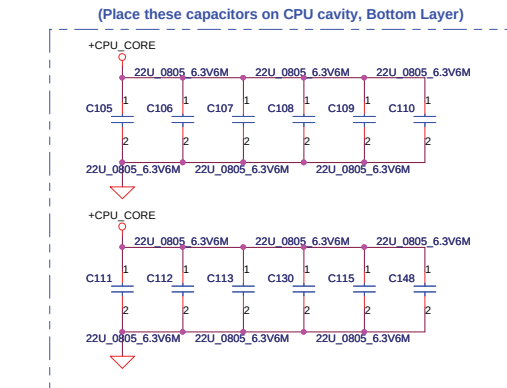
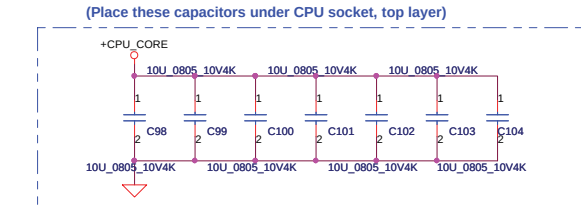
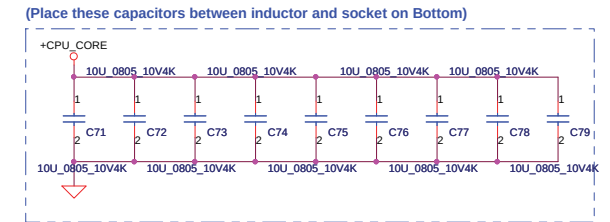
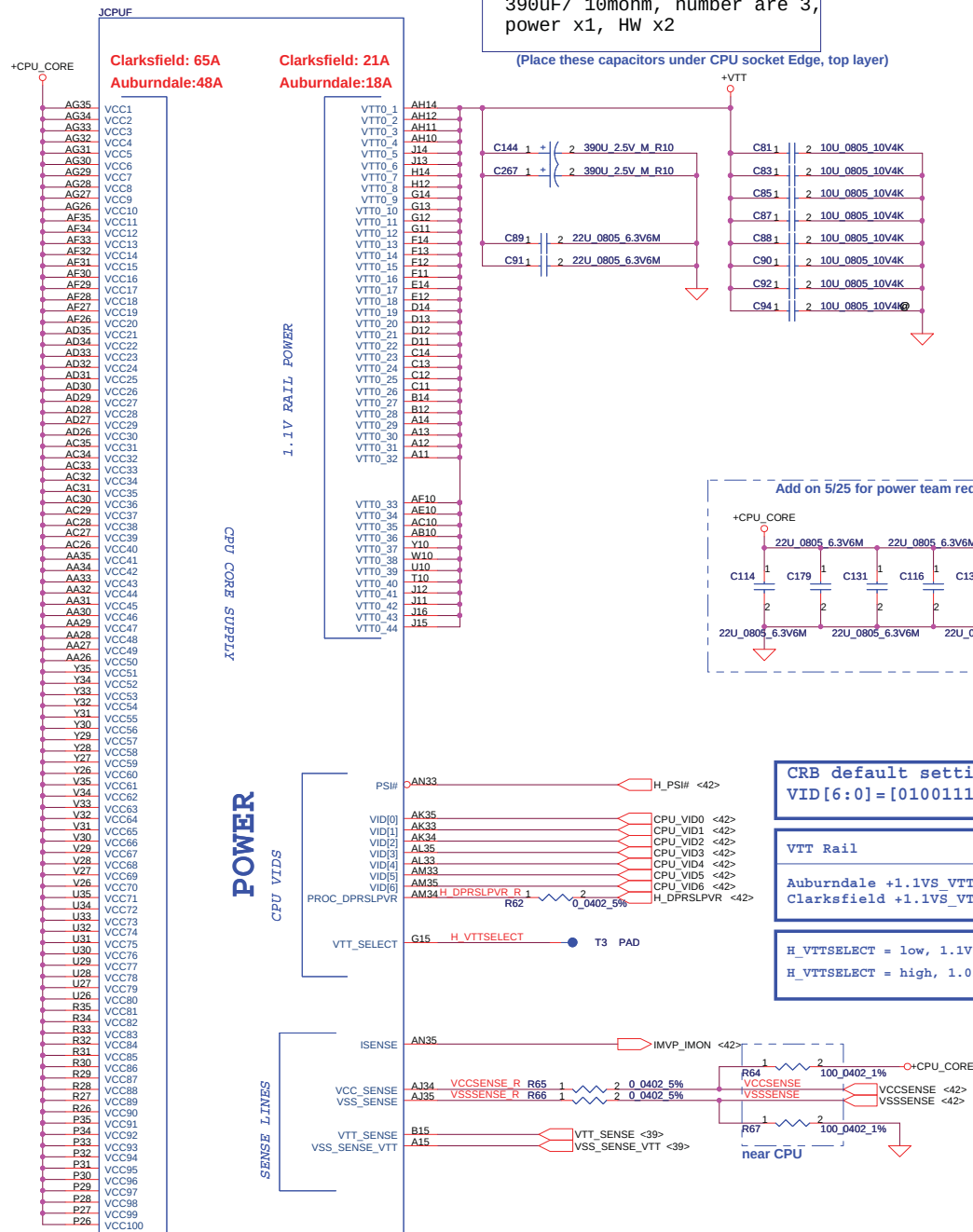
XDP Connector



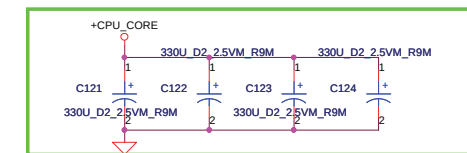
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TOP side (under inductor)

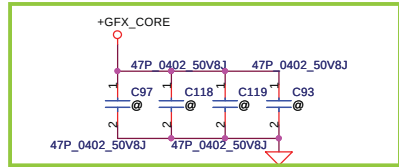


Check list:

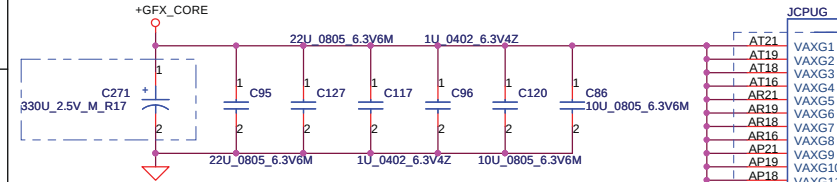
+CPU_CORE: 6x 470uF, 12x 22uF, 17x 10uF
+VTT: 4x 330uF, 7x 22uF, 8x 10uF

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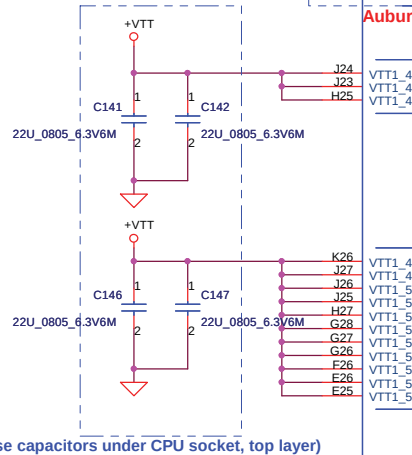
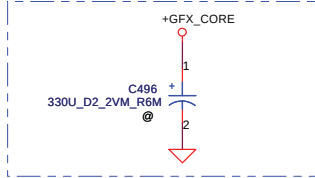
For EMI request



Change C271 to 4.5mm height OS-CON at PVT



Add C496 Co-Layout with C271



(Place these capacitors under CPU socket, top layer)

JCPUG
AT21 VAXG1
AT19 VAXG2
AT18 VAXG3
AT16 VAXG4
AR21 VAXG5
AR18 VAXG6
AR16 VAXG7
AP19 VAXG8
AP18 VAXG9
AP16 VAXG10
AN21 VAXG11
AN19 VAXG12
AN18 VAXG13
AN16 VAXG14
AM21 VAXG15
AM18 VAXG16
AM16 VAXG17
AL21 VAXG18
AL19 VAXG19
AL18 VAXG20
AK21 VAXG21
AK19 VAXG22
AK18 VAXG23
AJ21 VAXG24
AJ19 VAXG25
AJ18 VAXG26
AH21 VAXG27
AH19 VAXG28
AH18 VAXG29
AH16 VAXG30
AH14 VAXG31
AH12 VAXG32
AH10 VAXG33
AH08 VAXG34
AH06 VAXG35
AH04 VAXG36

Auburndale:22A

Clarksfield: 5A
Auburndale:3A

POWER

Clarksfield: 21A
Auburndale:18A

PEG & DM1

DDR3 - 1.5V RAILS

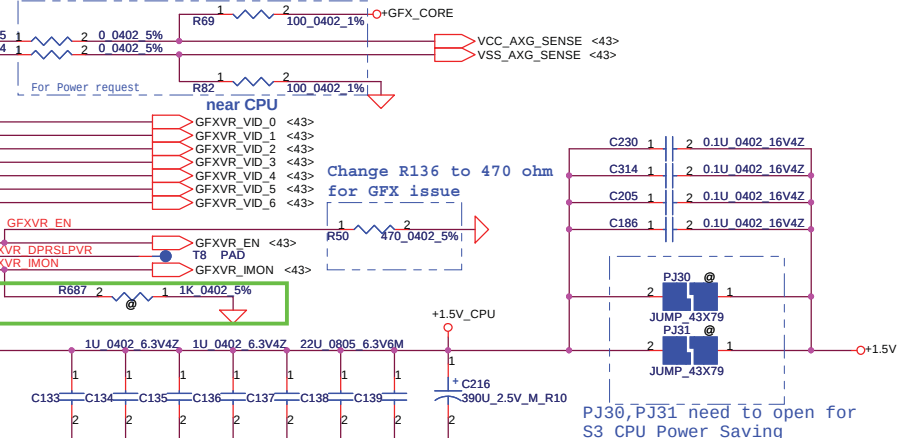
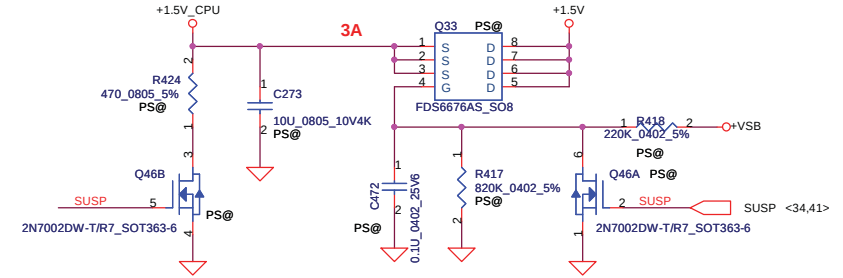
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VDDQ03
VDDQ04
VDDQ05
VDDQ06
VDDQ07
VDDQ08
VDDQ09
VDDQ10
VDDQ11
VDDQ12
VDDQ13
VDDQ14
VDDQ15
VDDQ16
VDDQ17
VDDQ18

VTT0_59
VTT0_60
VTT0_61
VTT0_62
VTT1_63
VTT1_64
VTT1_65
VTT1_66
VTT1_67
VTT1_68

VCCPLL1
VCCPLL2
VCCPLL3

Clarksfield: 0.6A
Auburndale:1.35A

For S3 CPU Power Saving



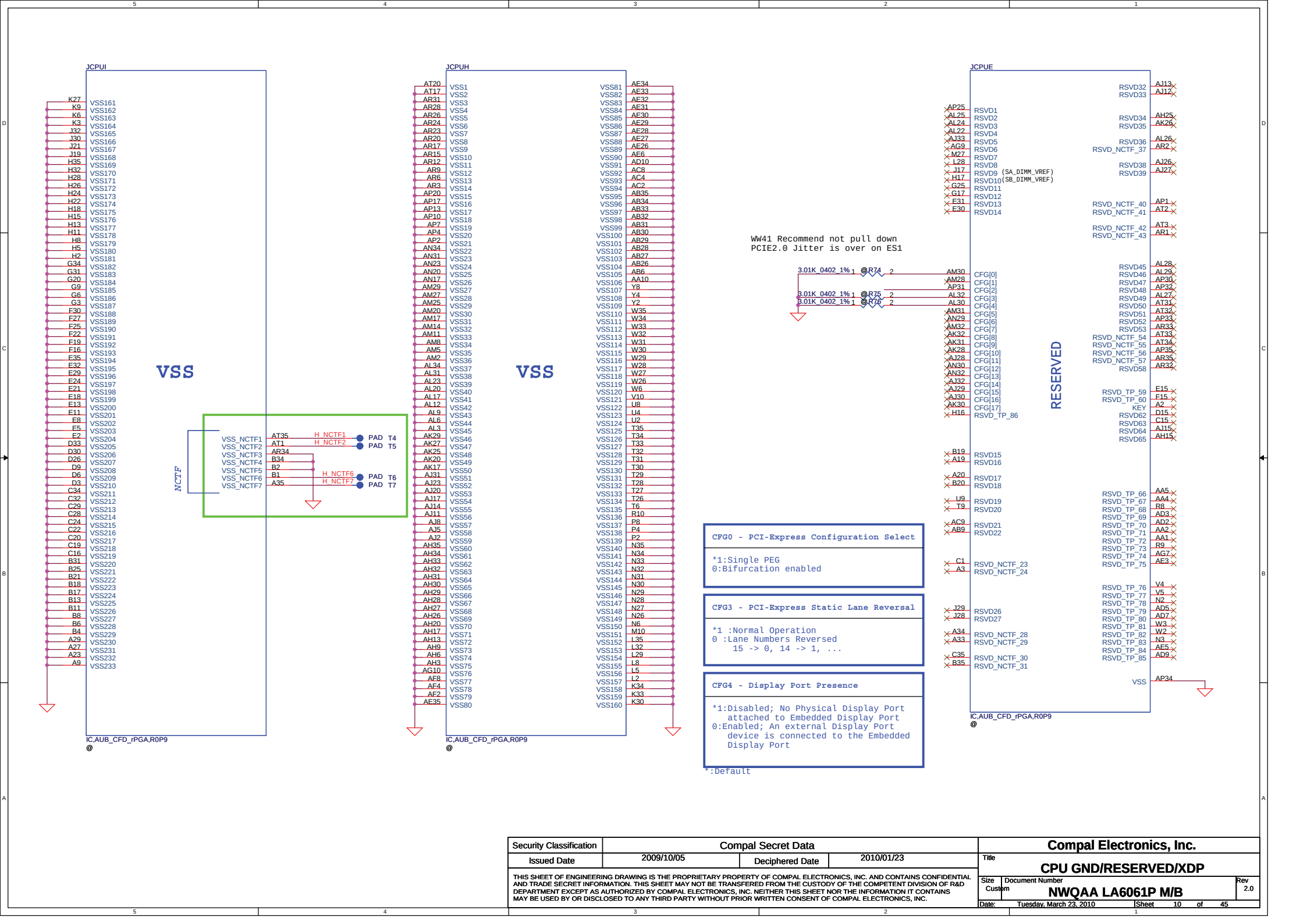
Change R136 to 470 ohm for GFX issue

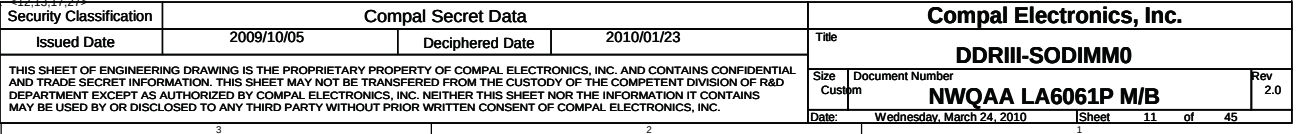
PJ30, PJ31 need to open for S3 CPU Power Saving

(Place these capacitors under CPU socket Edge, top layer)

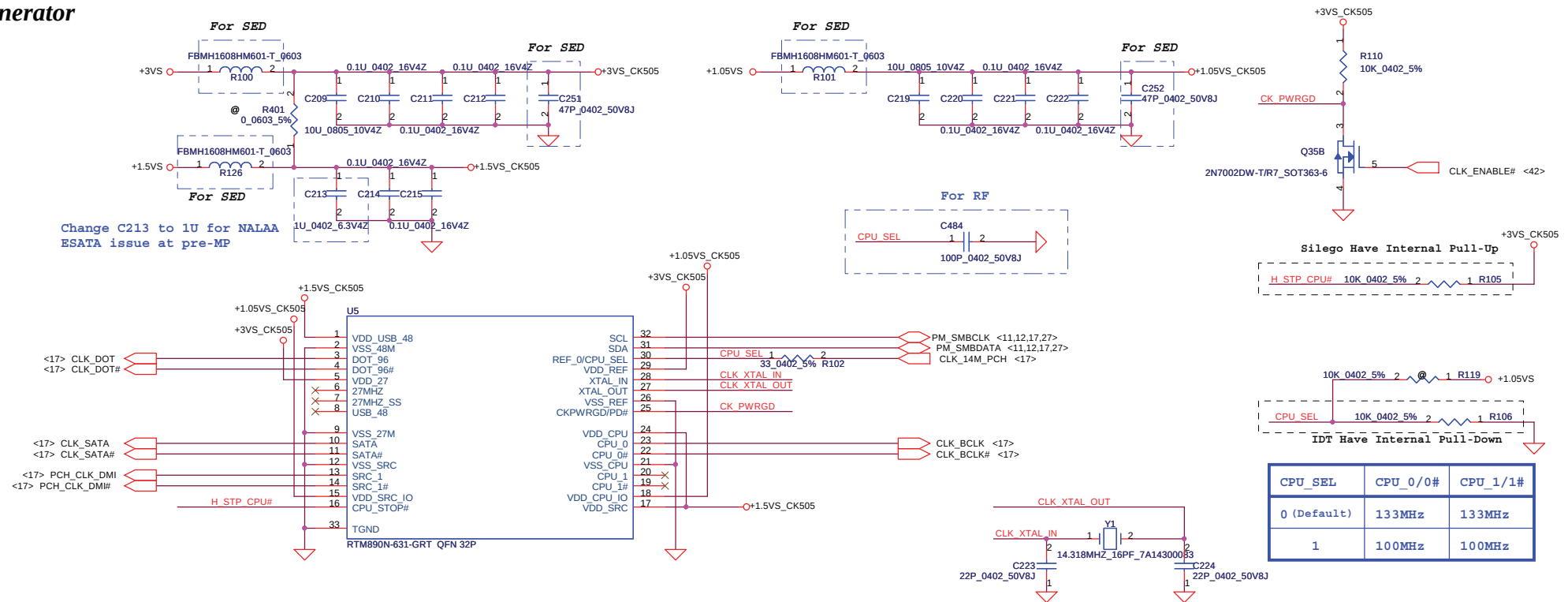
(Place these capacitors under CPU socket, top layer)

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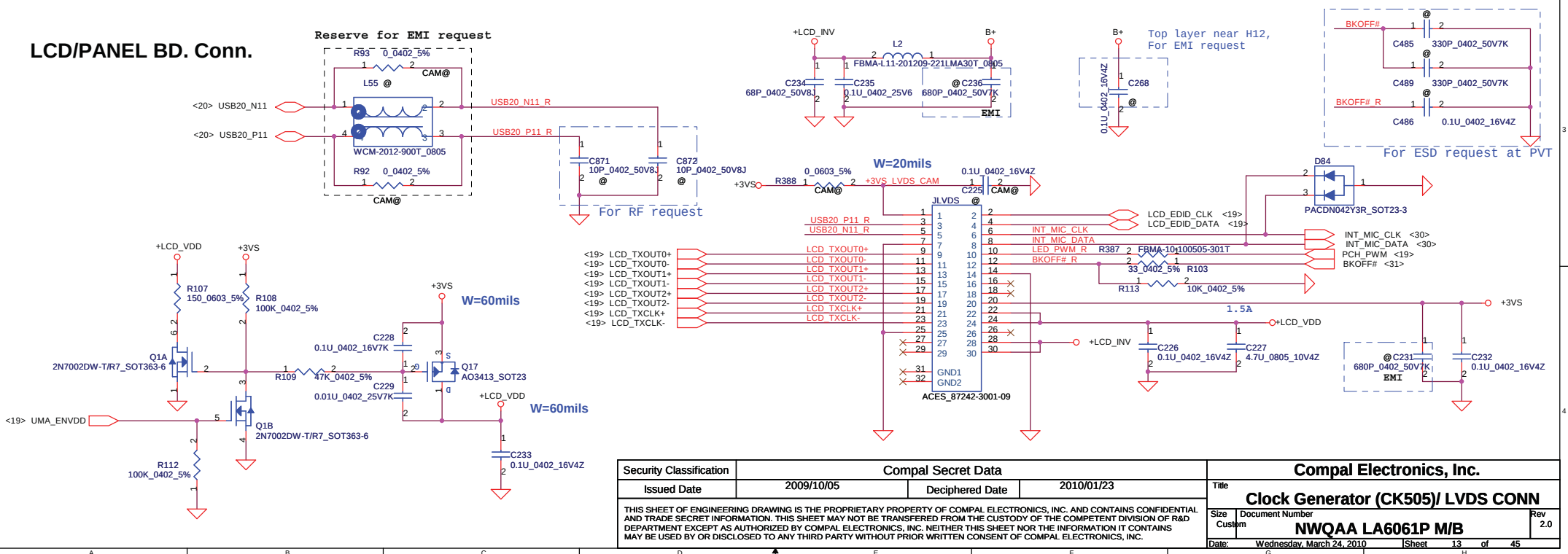




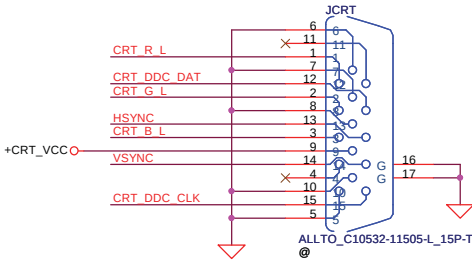
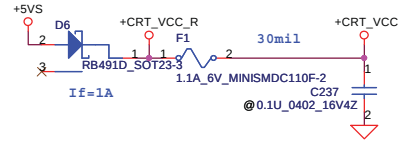
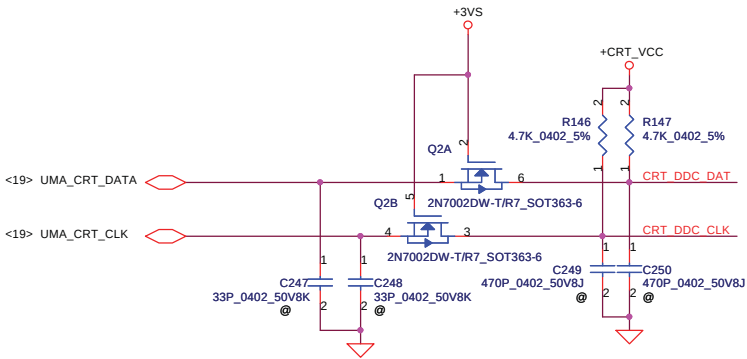
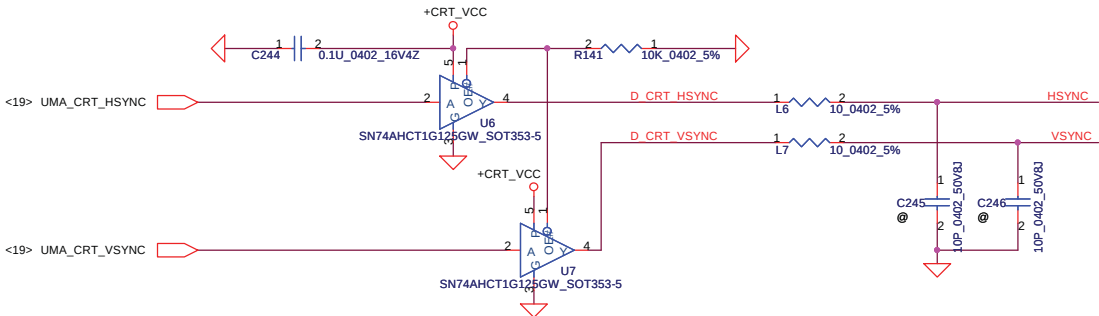
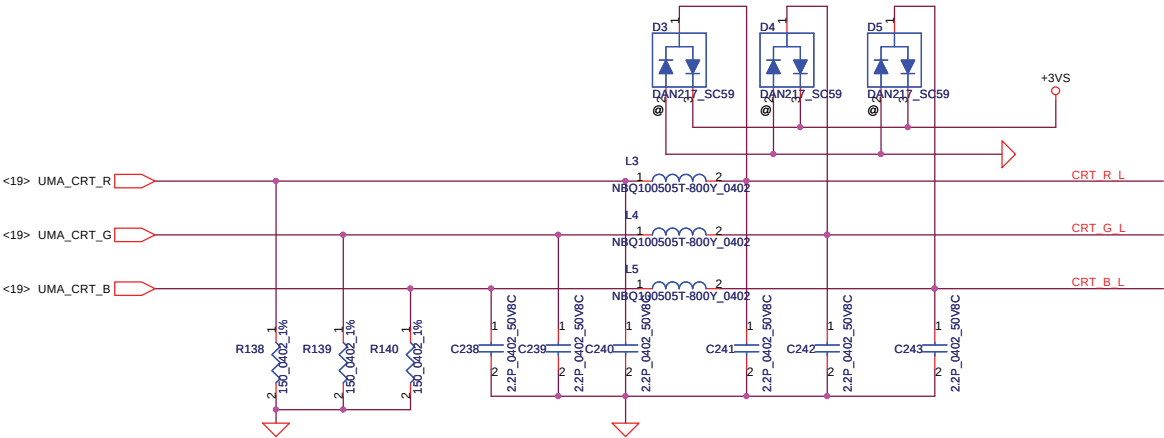
Clock Generator



LCD/PANEL BD. Conn.

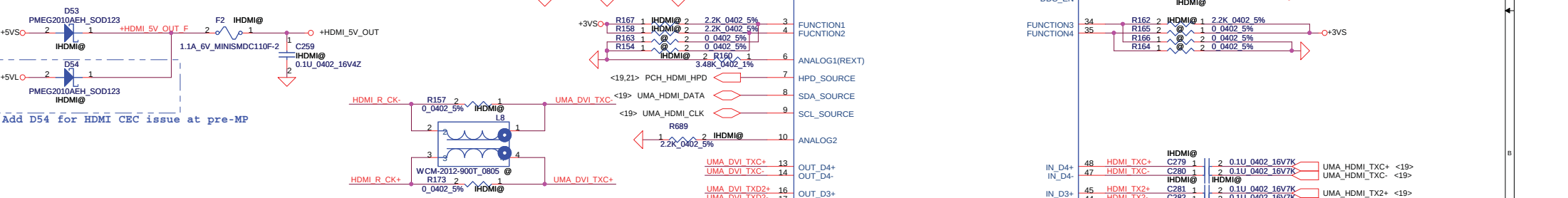
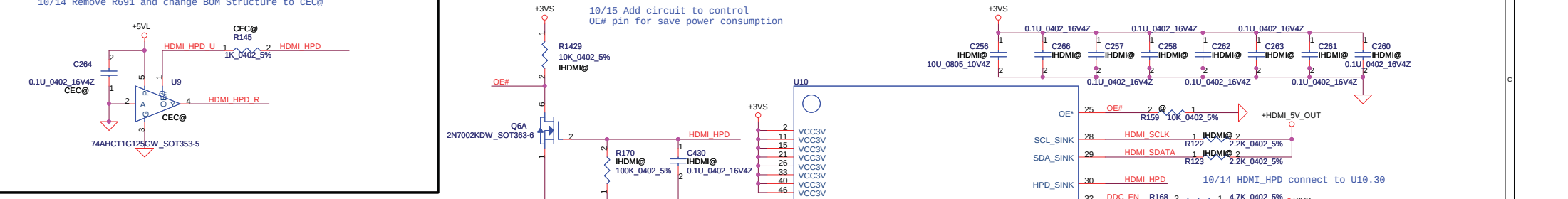
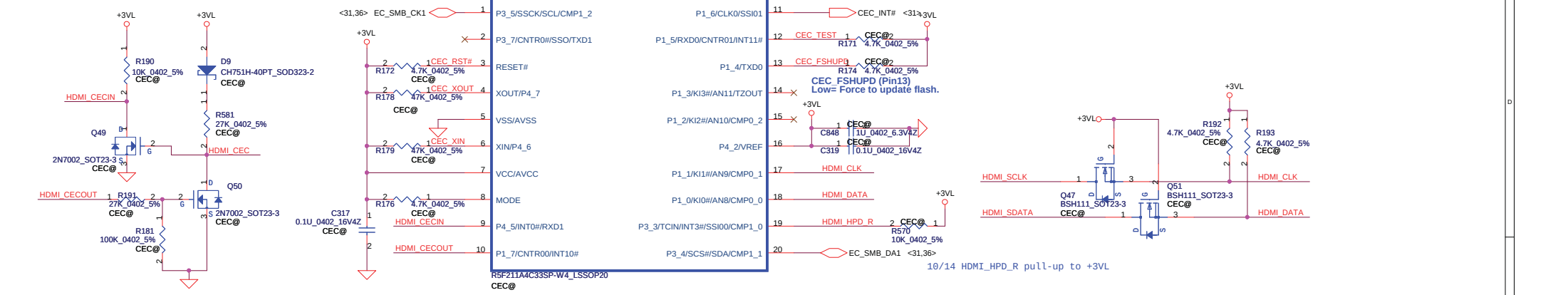


CRT CONNECTOR

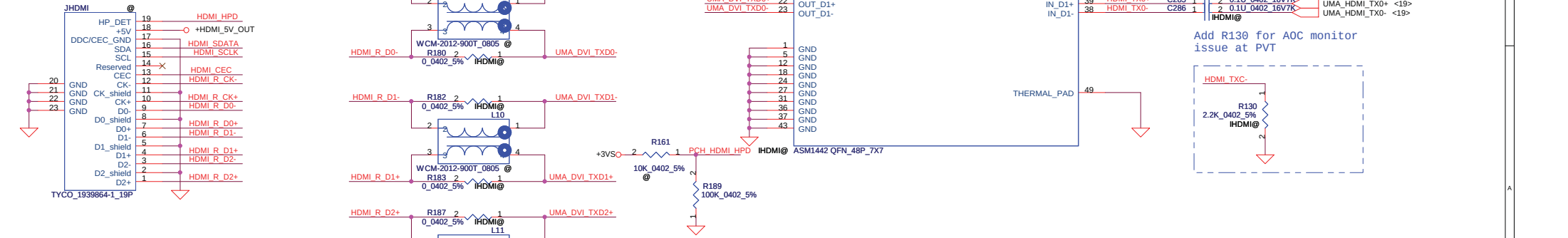


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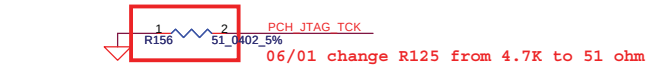
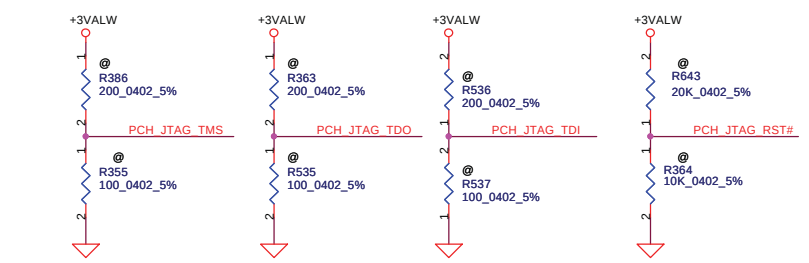
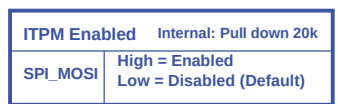
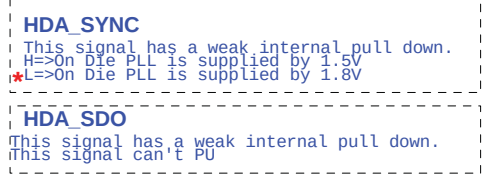
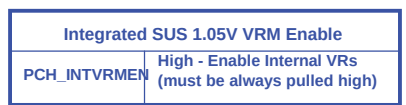
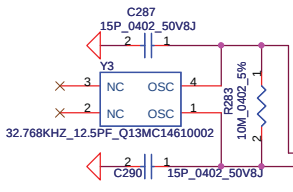
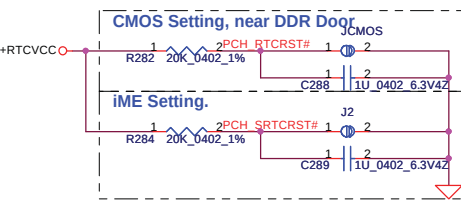
HDMI CEC Controller



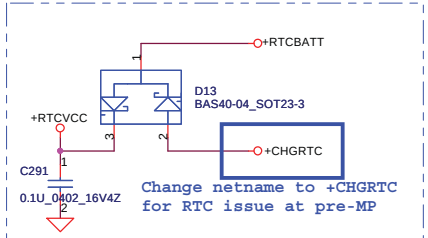
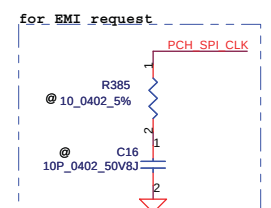
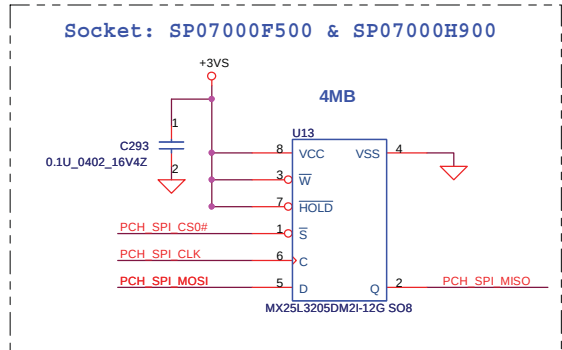
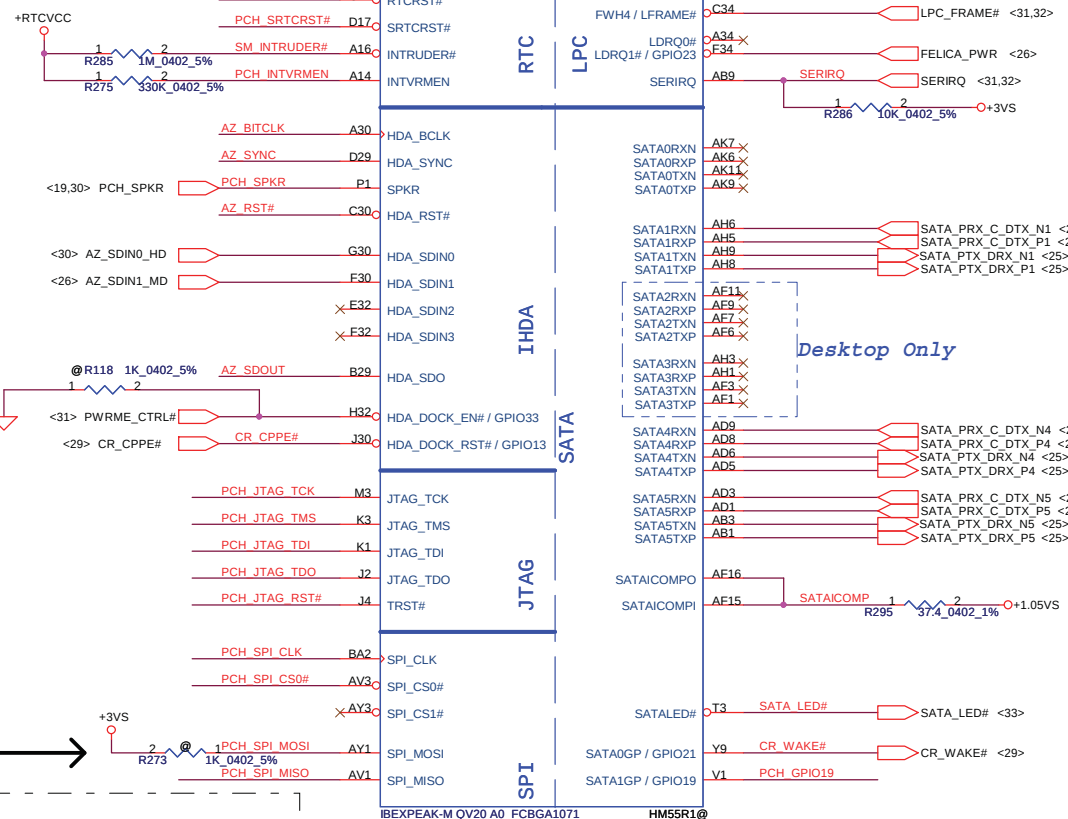
HDMI Connector



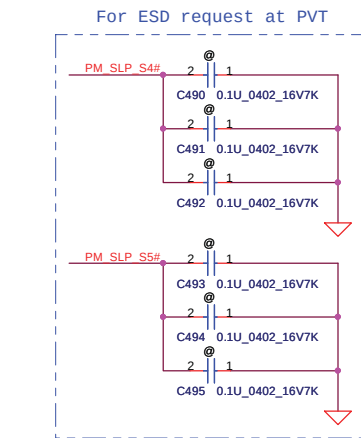
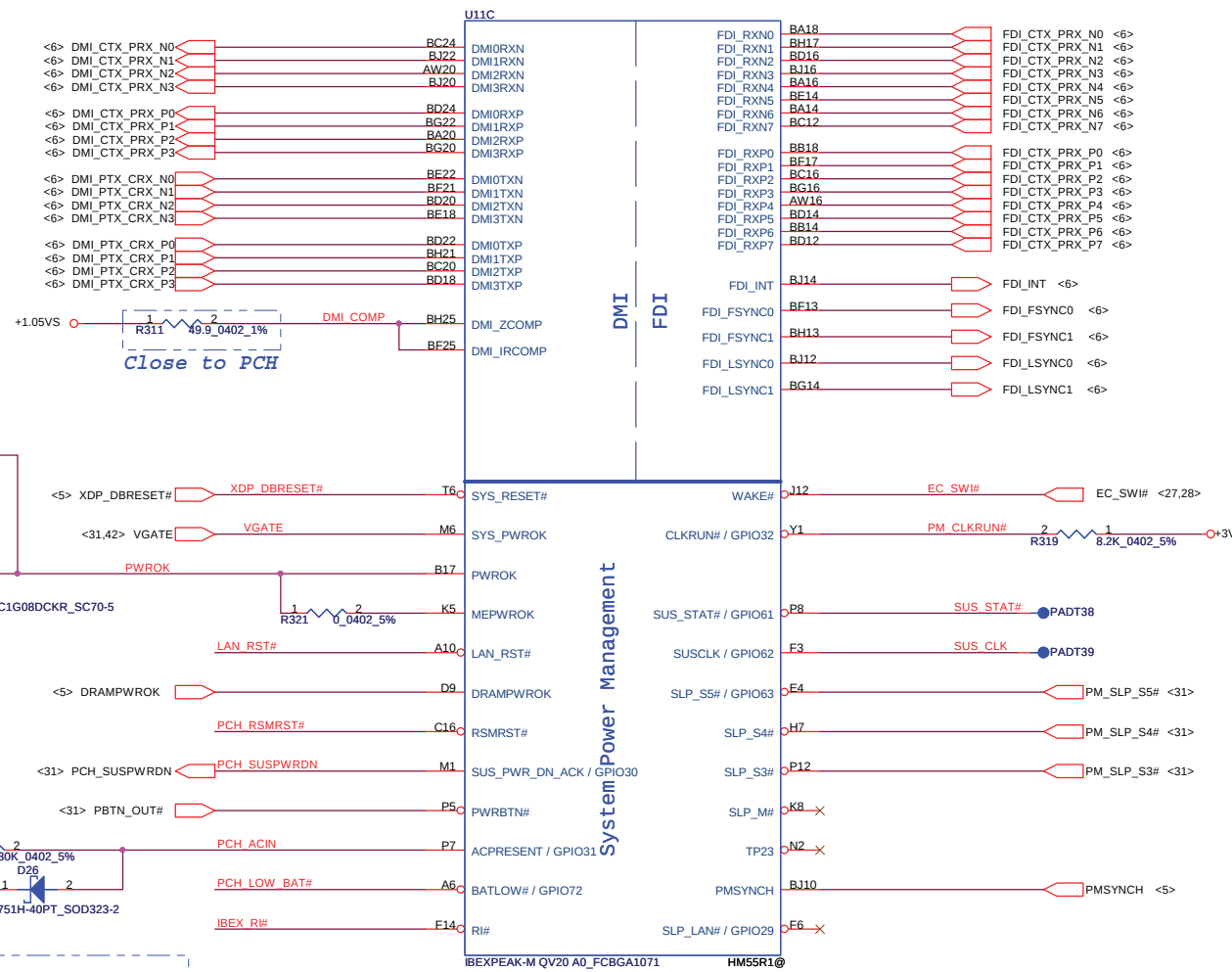
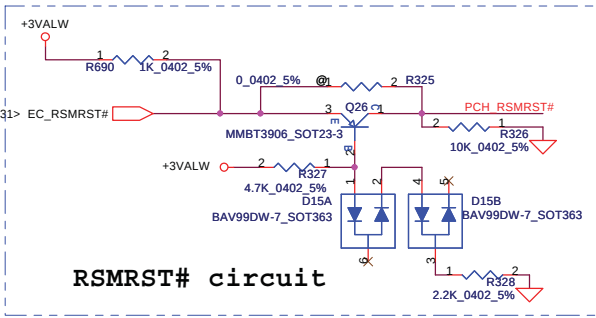
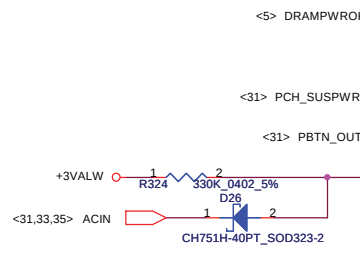
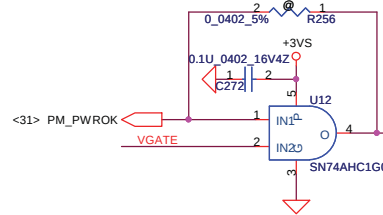
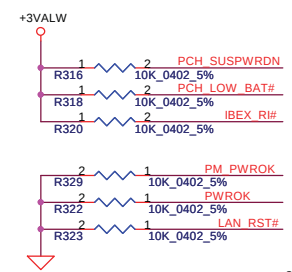
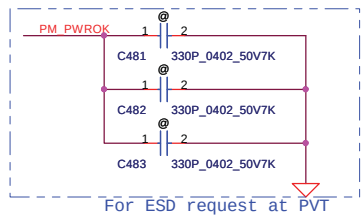
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Issued Date		2009/10/05	Deciphered Date	2010/01/23	Title		
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					Size	Document Number	Rev
					Date	Wednesday, March 24, 2010	Sheet
					NWQAA LA6061P M/B		
					2.0		



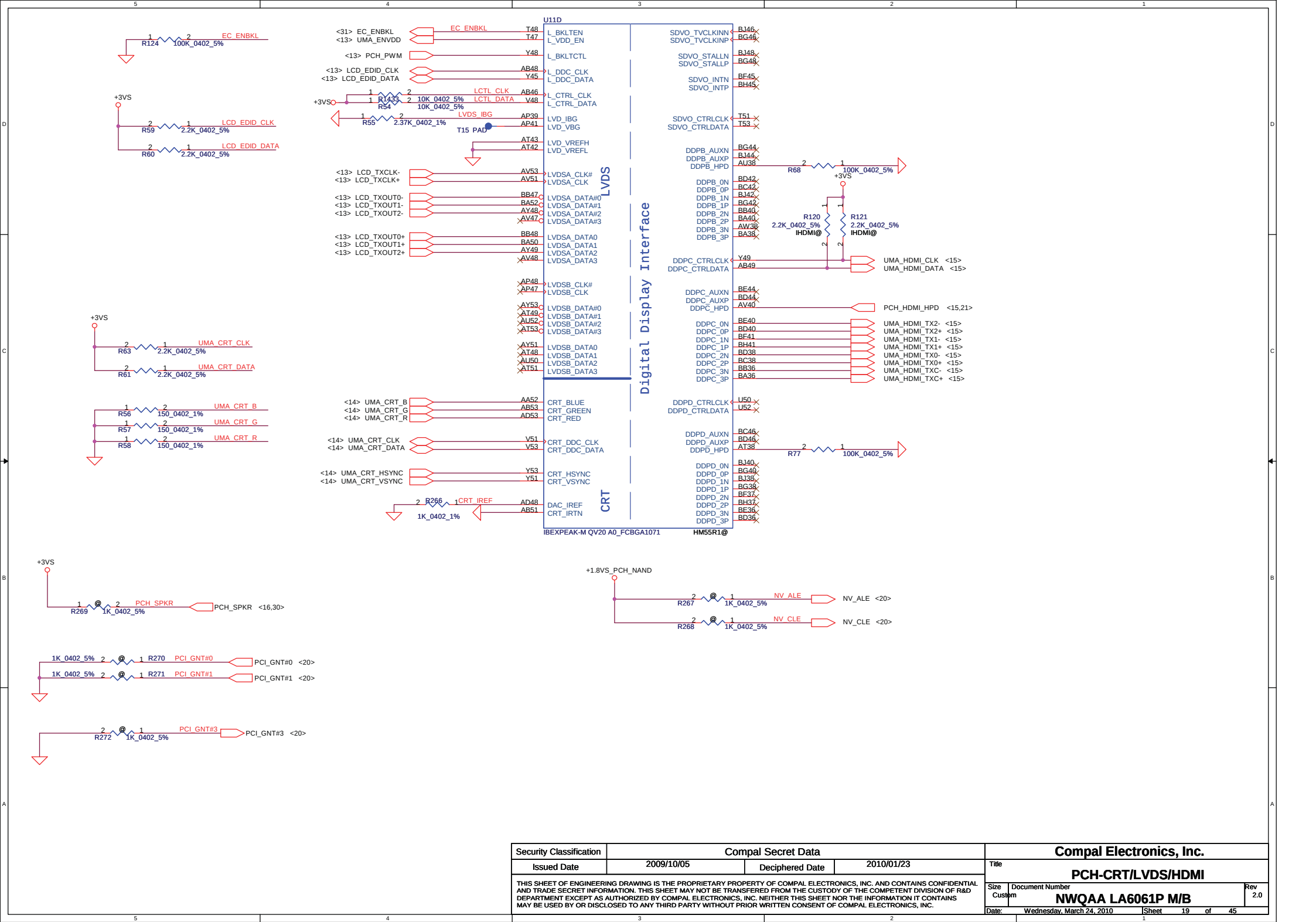
PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	280ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TCK	R356	200ohm	200ohm	20Kohm	No Install
PCH_JTAG_RST#	R537	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20Kohm	20Kohm	No Install	No Install
PCH_JTAG_RST#	R353	10Kohm	10Kohm	No Install	No Install

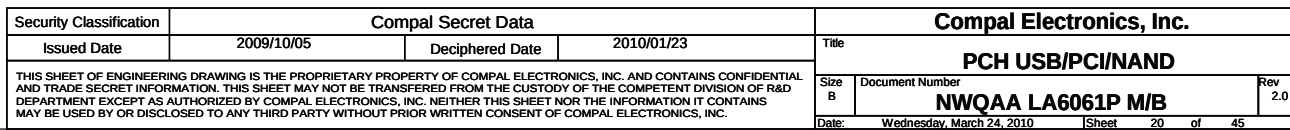
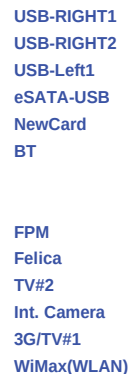


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2009/10/05		Deciphered Date		2010/01/23		Title			
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Size	Document Number	NWQAA LA6061P M/B		Rev		2.0					
Date	Wednesday, March 24, 2010	Sheet		16		of		45			



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Size	Document Number	Rev		Date	
B	NWQAA LA6061P M/B	2.0		Wednesday, March 24, 2010	
Sheet		18		of 45	





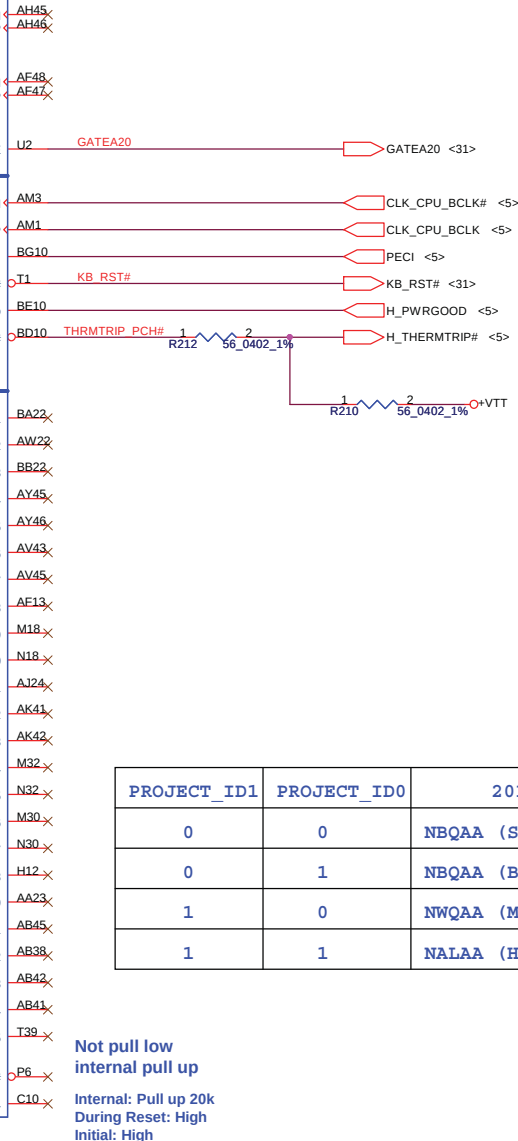
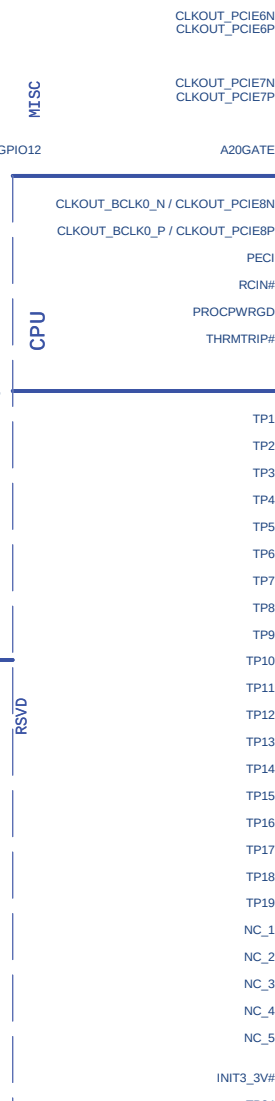
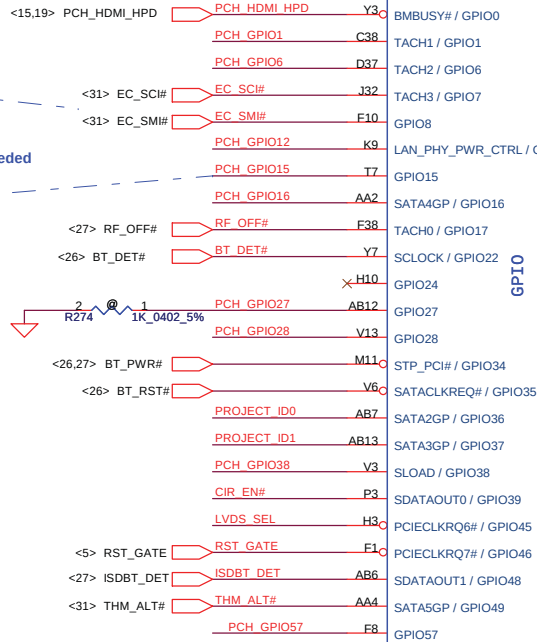
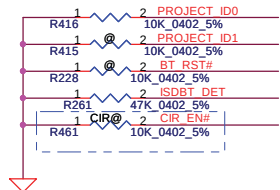
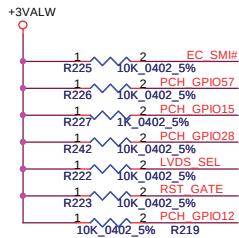
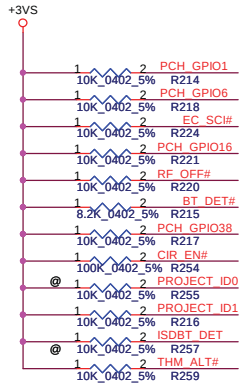
GPIO8 Not pull down

Internal: Pull up 20k
During Reset: High
Initial: High

GPIO15
a Strong pull up may be needed
for GPIO Functionality
Internal: Pull down 20k
During Reset: Low
Initial: Low

On-Die PLL VR

PCH_GPIO27 High = Enabled (Default)
Low = Disabled



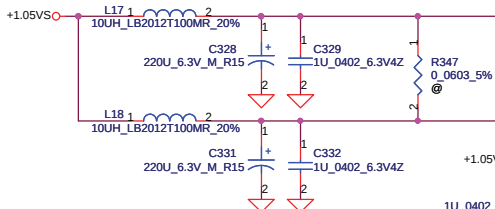
PROJECT_ID1	PROJECT_ID0	2010 Project ID setting
0	0	NBQAA (Streamline-M/-S 11.6/13.3")
0	1	NBQAA (Bordeaux 14")
1	0	NWQAA (Marseille 16")
1	1	NALAA (Hamburg 17.3")

Not pull low
internal pull up
Internal: Pull up 20k
During Reset: High
Initial: High

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2009/10/05		Deciphered Date		2010/01/23		Title			
Size		B		Document Number		Rev		PCH CPU/GPIO			
Date		Wednesday, March 24, 2010		Sheet		21		NWQAA LA6061P M/B			

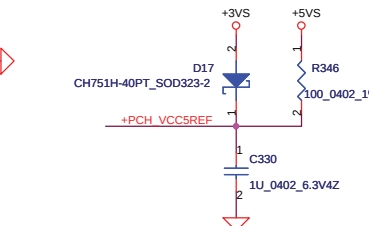
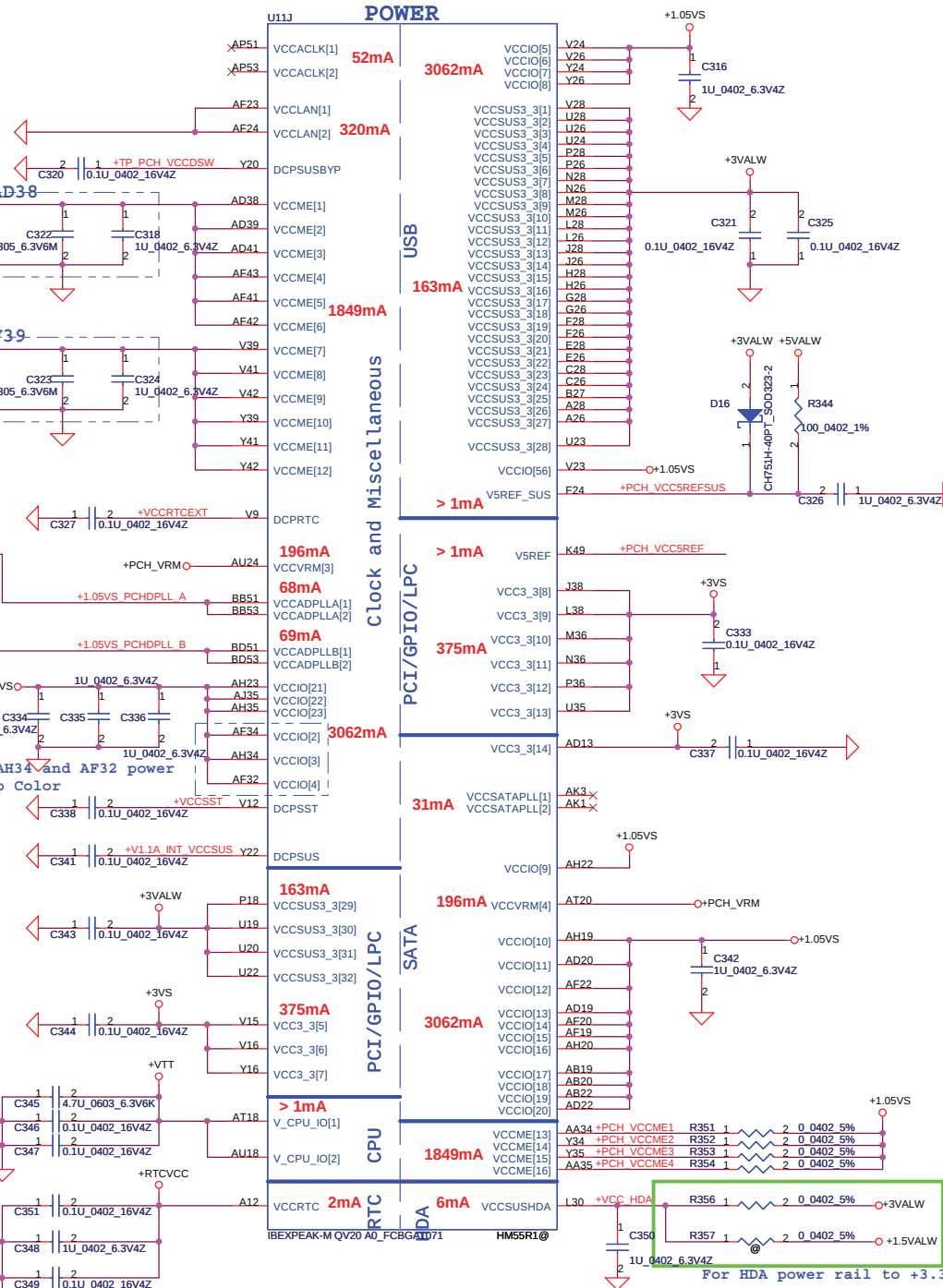
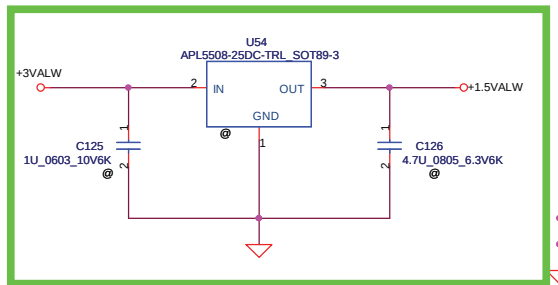
VccLAN may be grounded if Intel LAN is disabled

If two VccME rails can be combined, only total 2 x 22 μ F and 2 x 1 μ F caps are necessary



Short AF34, AH34 and AF32 power for HDMI Deep Color

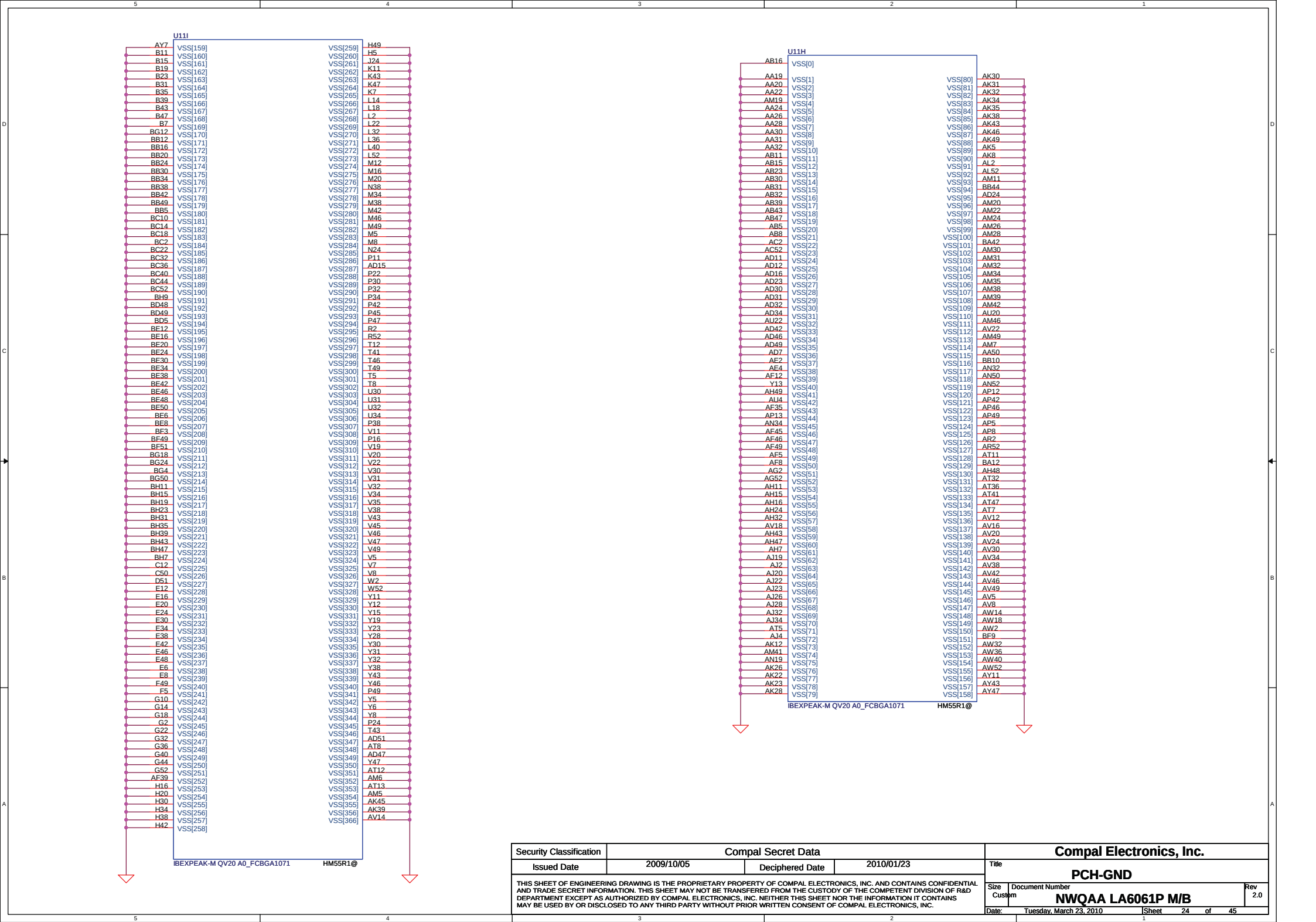
For HDA power rail to +1.5V



VCCSUSHDA can be either 1.5V or 3.3V

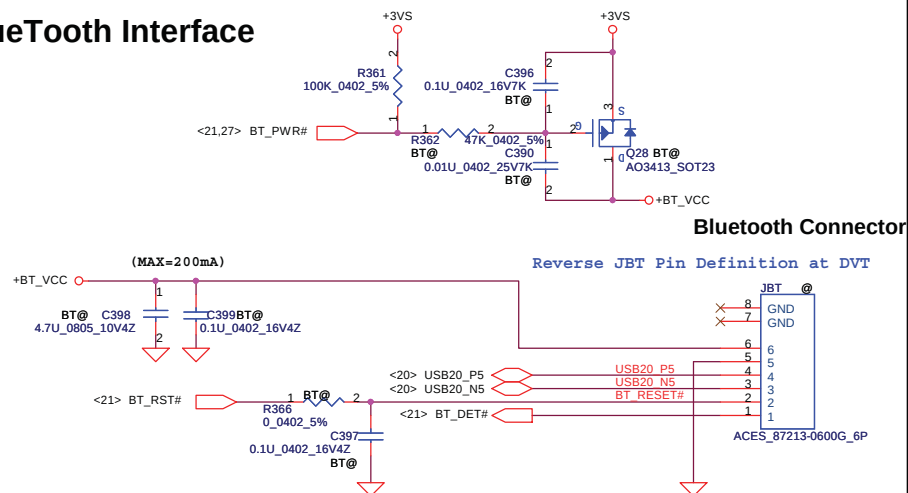
For HDA power rail to +3.3V(default) /+1.5V

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				Custom	NWQAA LA6061P M/B
				Date	Tuesday, March 23, 2010
				Sheet	23 of 45

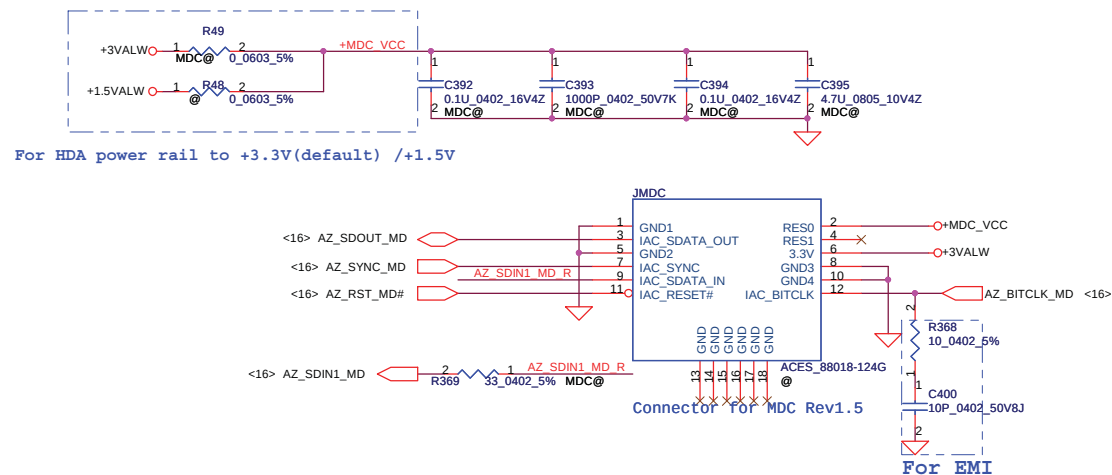


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Issued Date	2009/10/05	Deciphered Date	2010/01/23	Title	
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Size	Document Number	Rev		2.0	
Custom	NWQAA LA6061P M/B				
Date:	Tuesday, March 23, 2010	Sheet	24	of	45

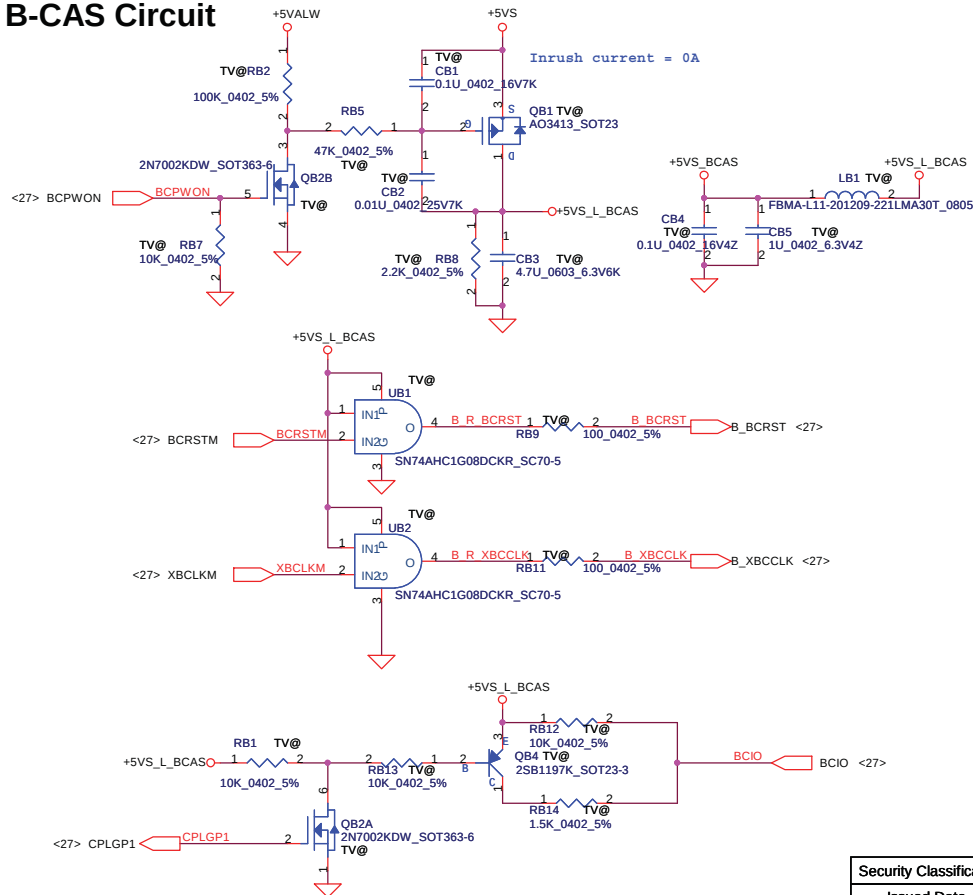
Bluetooth Interface



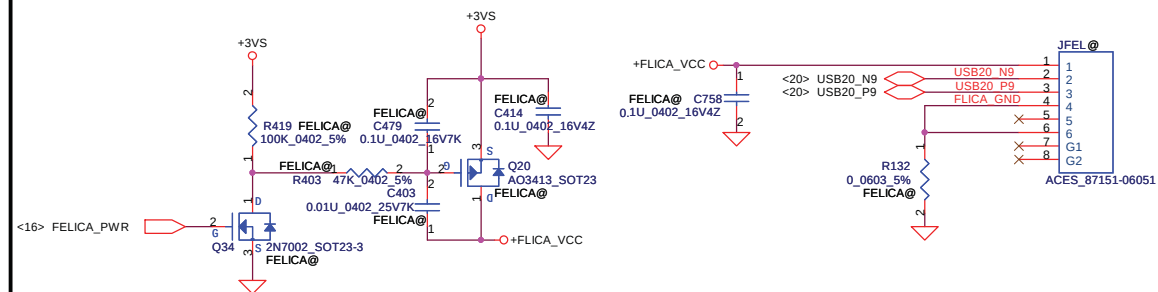
MDC 1.5 Conn.



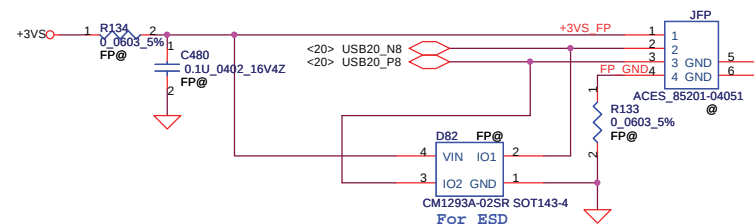
B-CAS Circuit



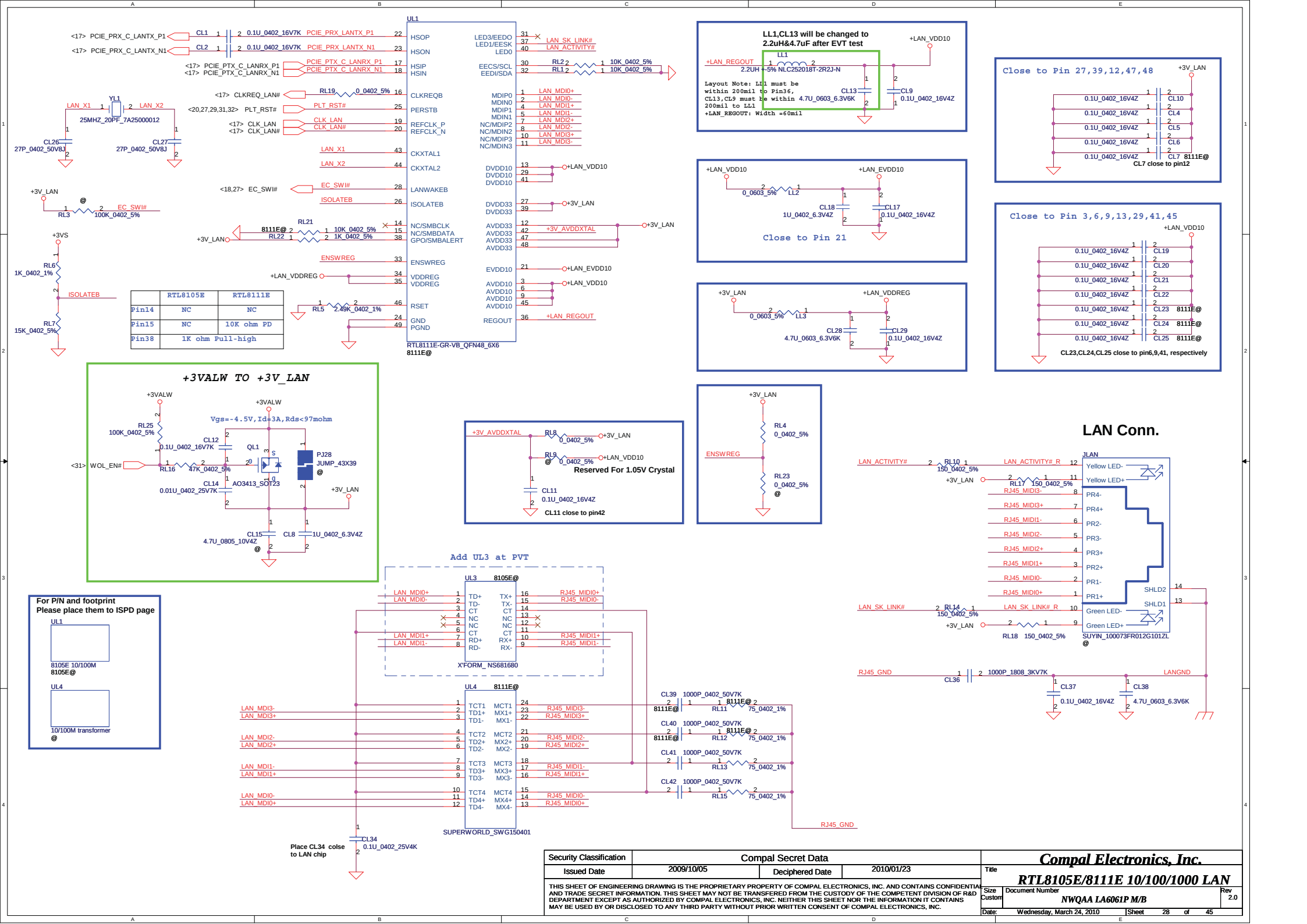
Felica



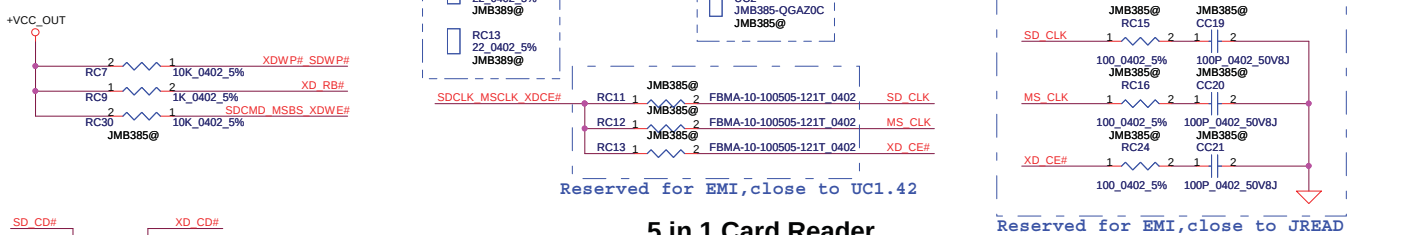
Finger printer



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Issued Date	2009/10/05	Deciphered Date	2010/01/23	Title BT/FP/Felica/B-CAS				
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UC2 JMB389@

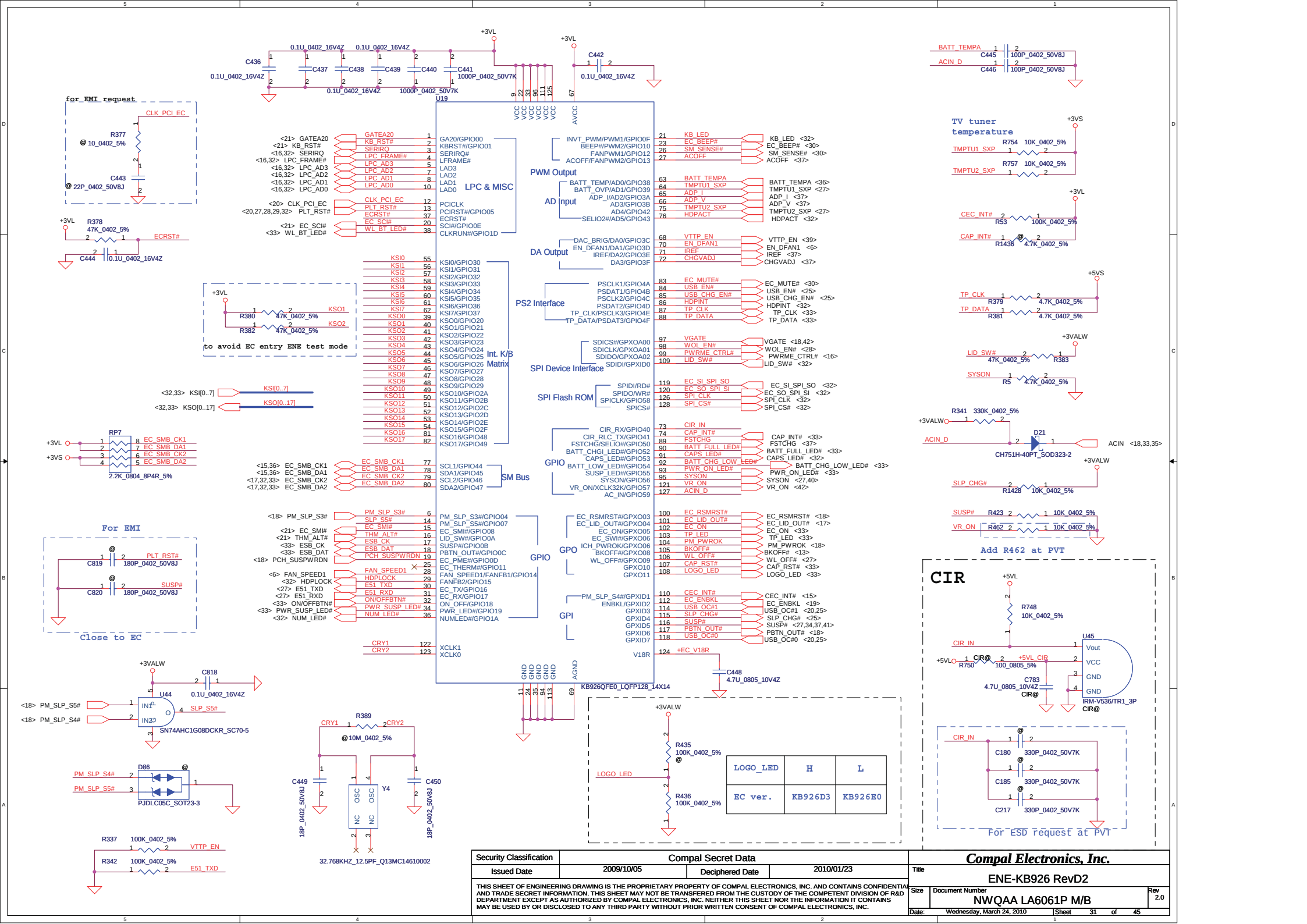


MS

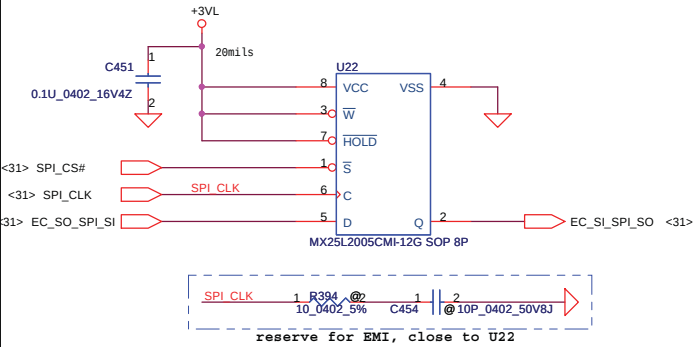


The diagram shows the I/O pin connections for MDIO7 and MDIO14. MDIO7 is connected to RC28 (10K_0402_5%) and 10K_0402_5%. MDIO14 is connected to RC26 (10K_0402_5%) and RC25 (200K_0402_5%). Both pins are connected to a 3.3V supply.

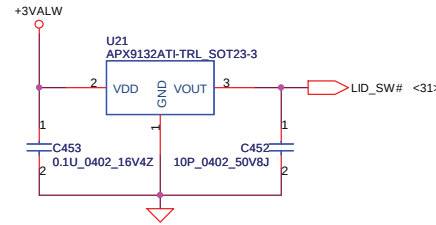
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2009/10/05	Deciphered Date	2010/04/07	Title		
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				Size	Document Number	Rev
				Custom	NWQAA LA6061P M/B	2.0
				Date:	Wednesday, March 24, 2010	Sheet 29 of 45



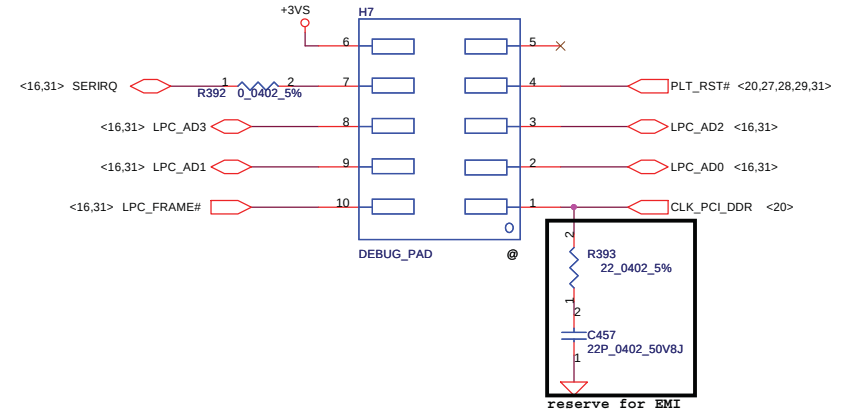
SPI Flash (256KB)



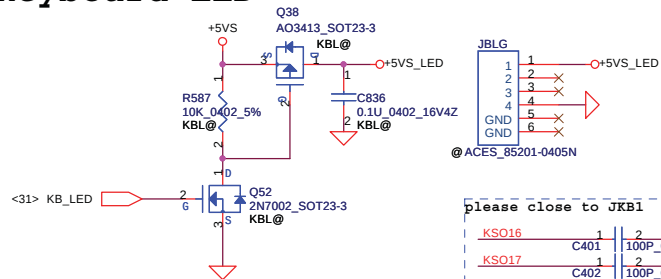
Lid SW



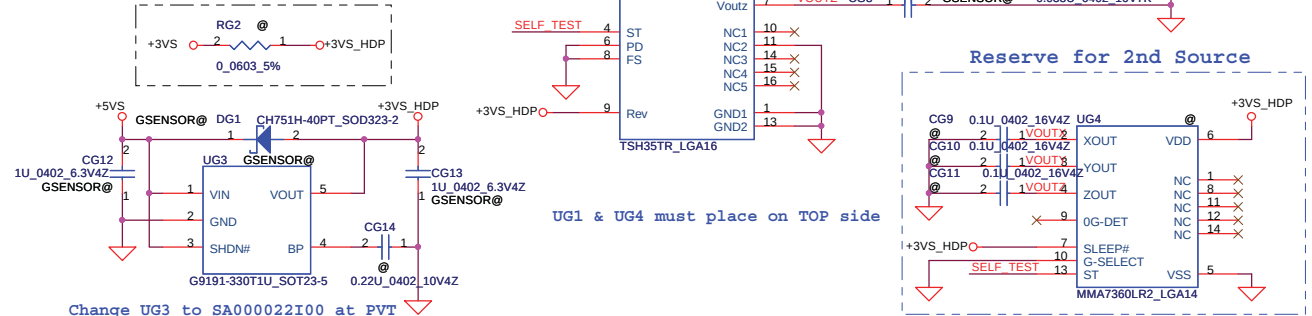
LPC Debug Port Please place the PAD under DDR DIMM.



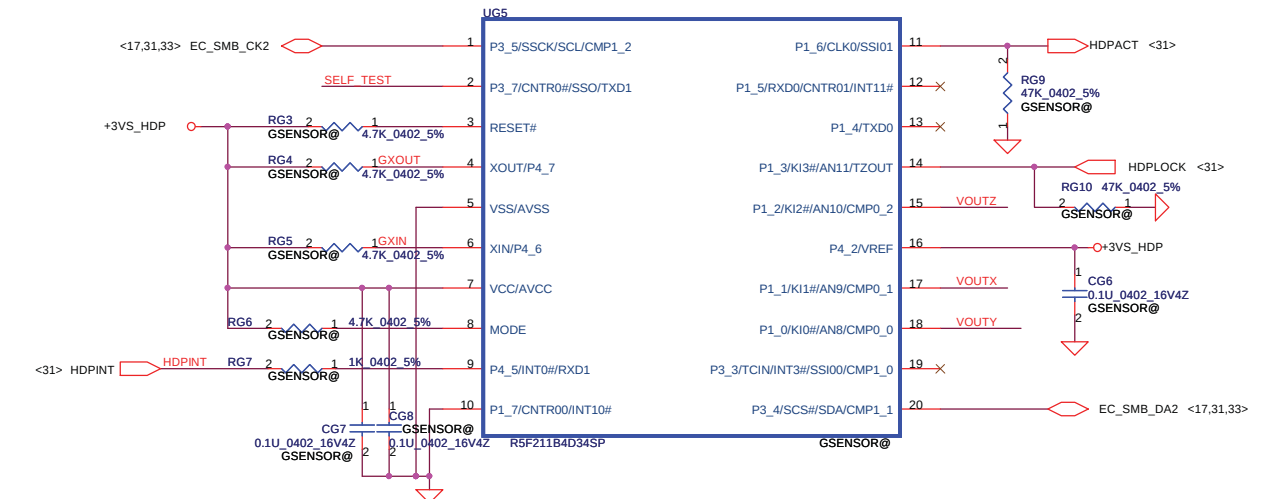
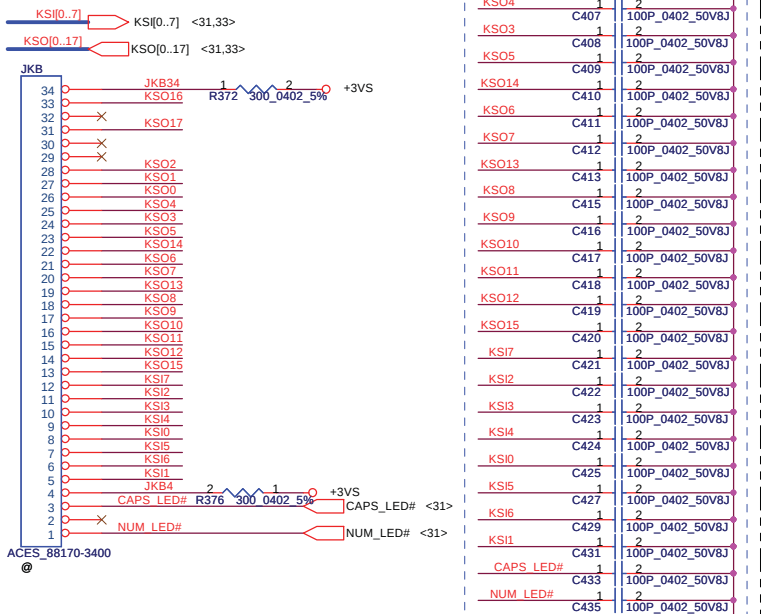
Keyboard LED



G-Sensor

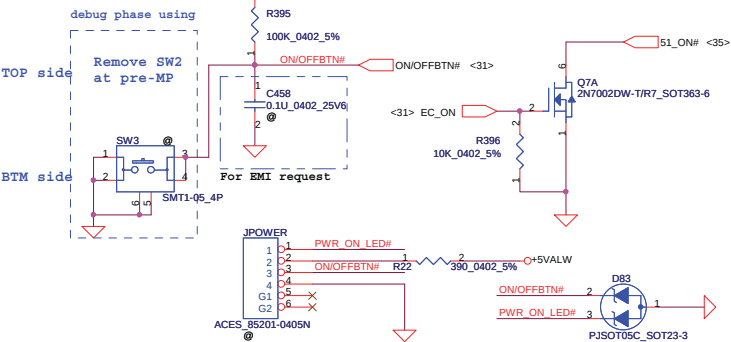


KEYBOARD CONN.

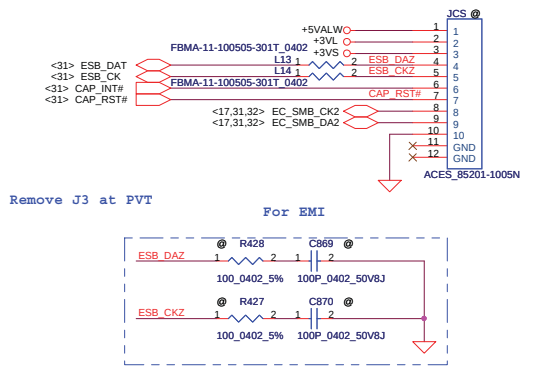


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Issued Date	2009/10/05	Deciphered Date	2010/01/23	SPI ROM/TP/KB/Debug	
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				NWQAA LA6061P M/B	
				Date	Wednesday, March 24, 2010
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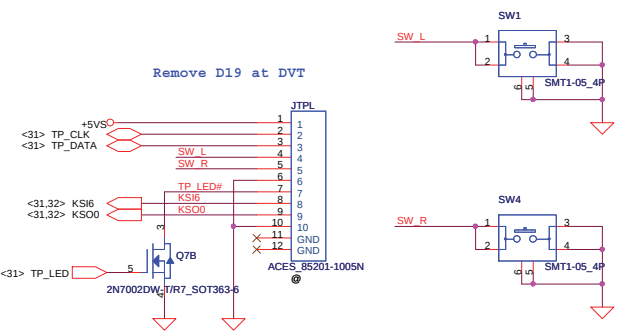
Power Button



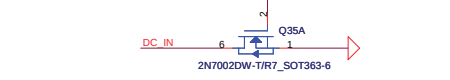
Caps Sensor/Light Sensor Conn.



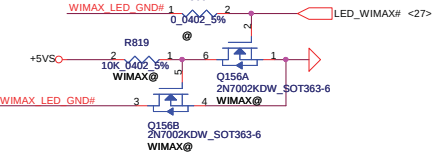
Touchpad & Light Pipe Connector



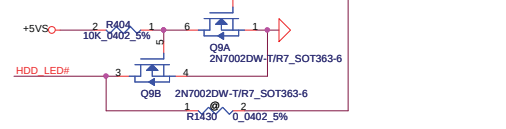
DC-IN LED



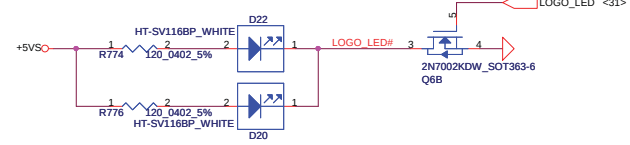
WiMAX LED



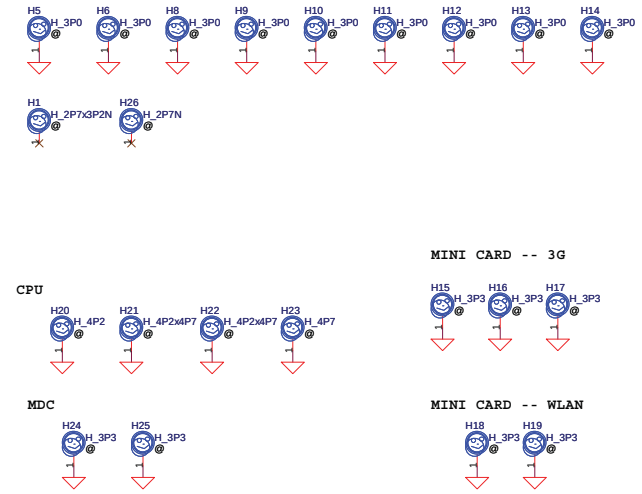
HDD LED



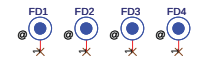
Logo LED



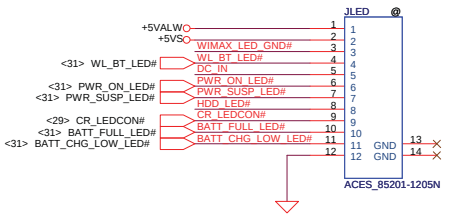
Screw Hole



PCB Fedical Mark PAD

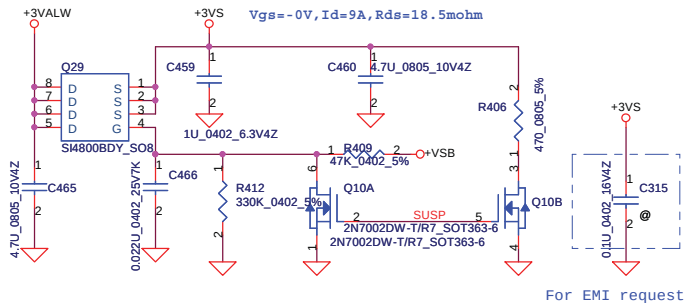
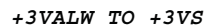


LED/B Connector



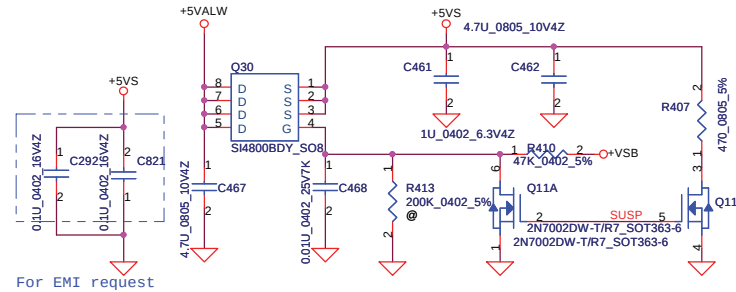
ISPD





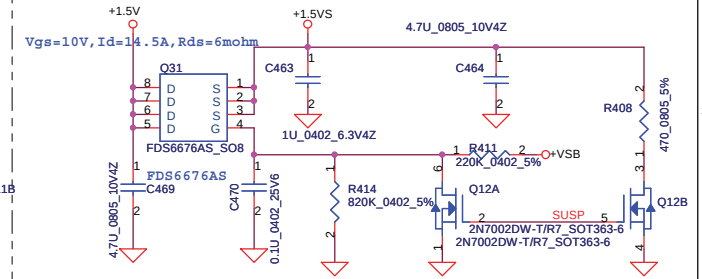
For EMI request

+5VALW TO +5VS

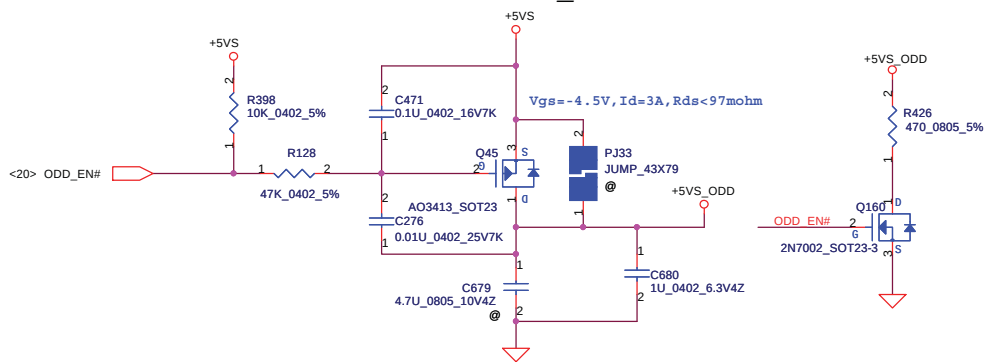


For EMI request

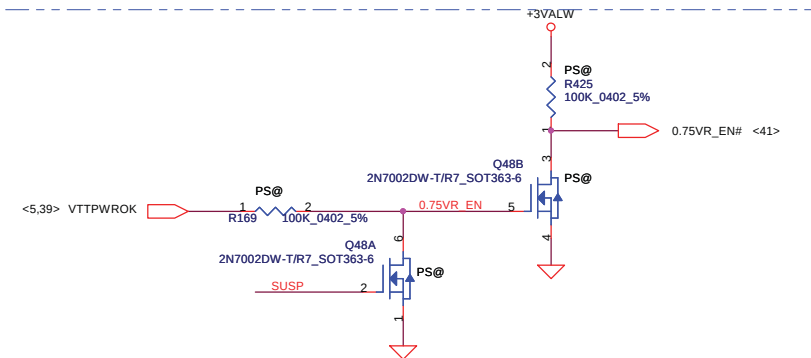
+1.5V to +1.5VS



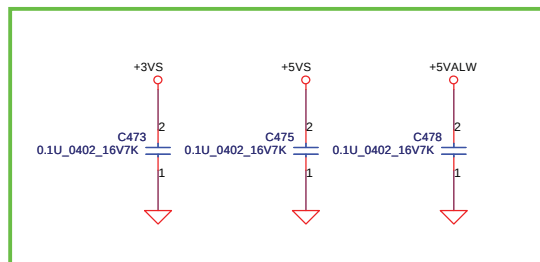
+5VS TO +5VS ODD



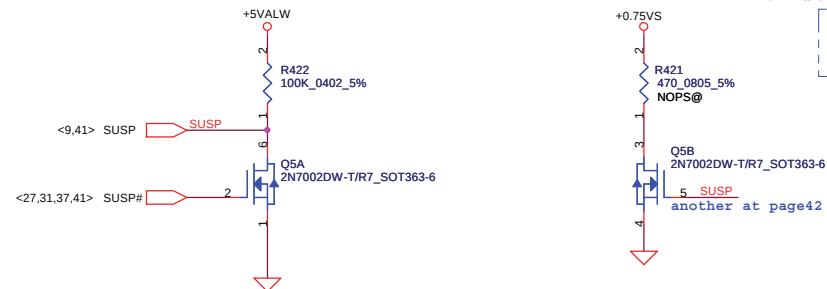
For S3 CPU Power Saving



Reserve for EMI test

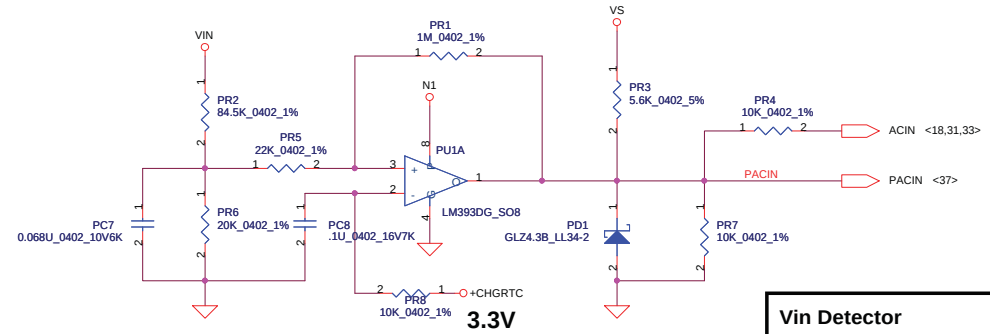
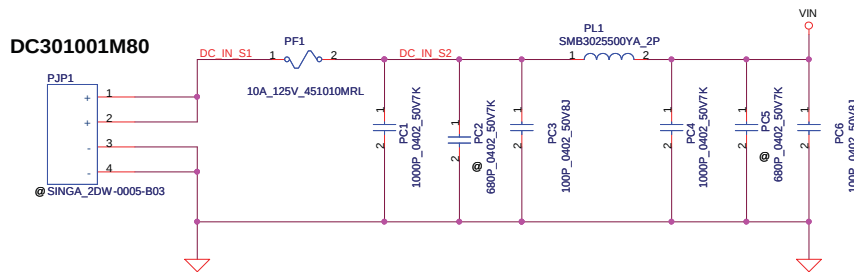


For S3 CPU Power Saving

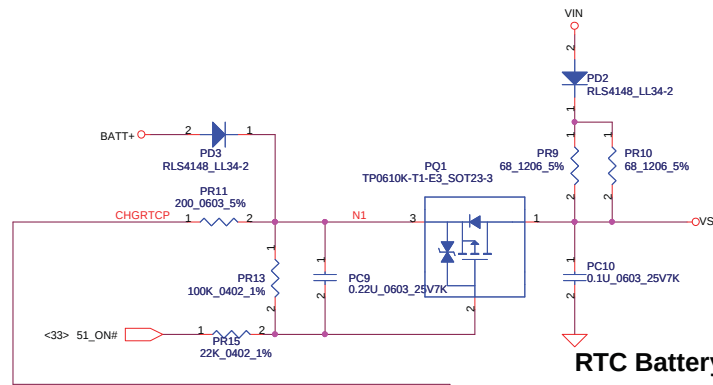


another at page42

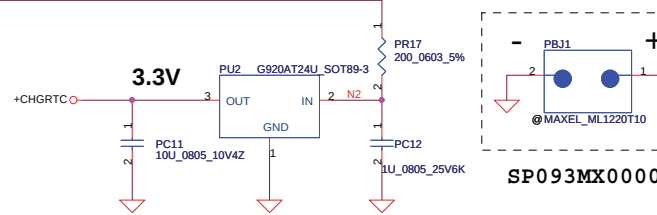
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Issued Date	2009/10/05	Deciphered Date	2010/01/23	Title DC-DC INTERFACE		
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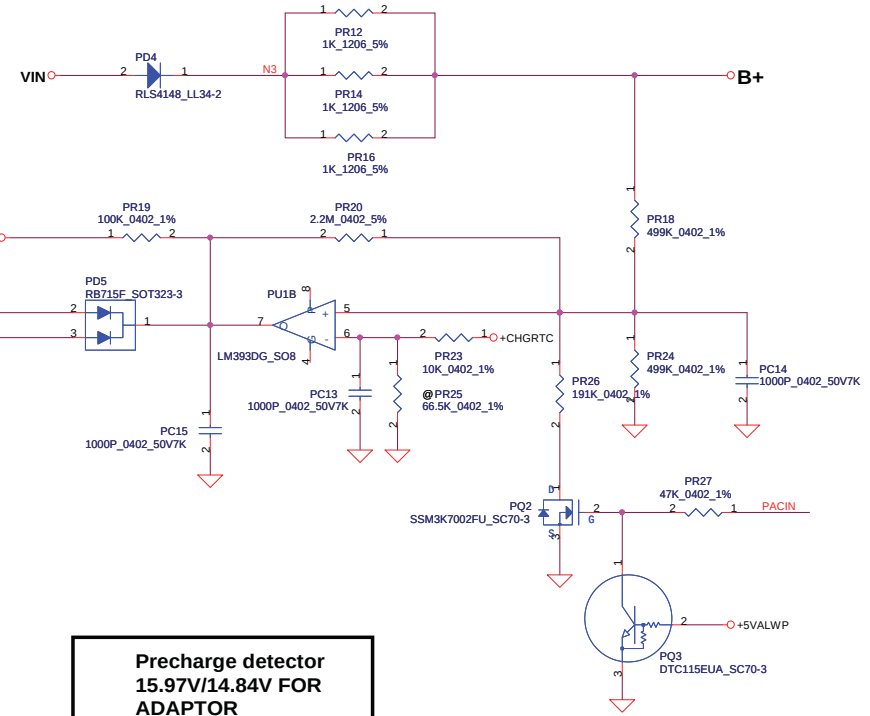
Vin Detector		
High	18.384	17.901 17.430
Low	17.728	17.257 16.976



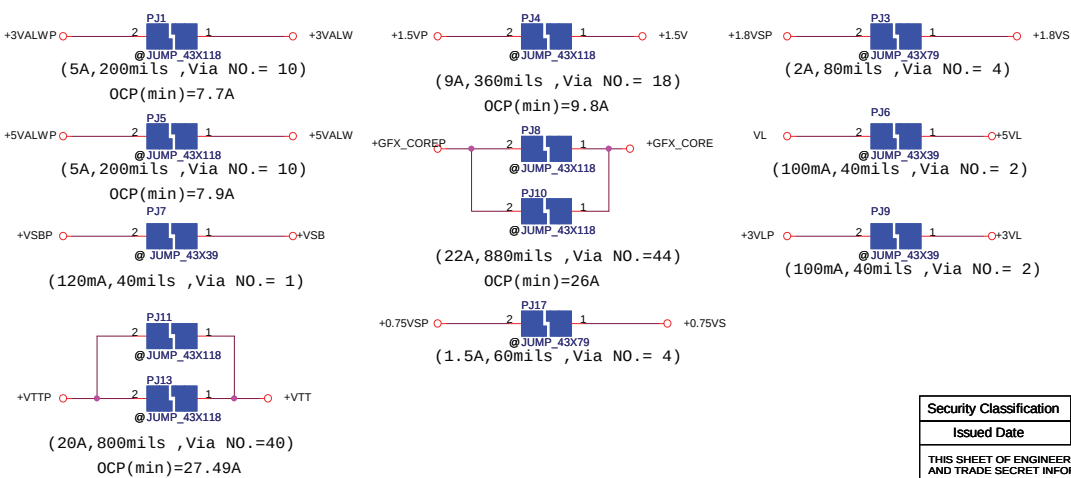
RTC Battery



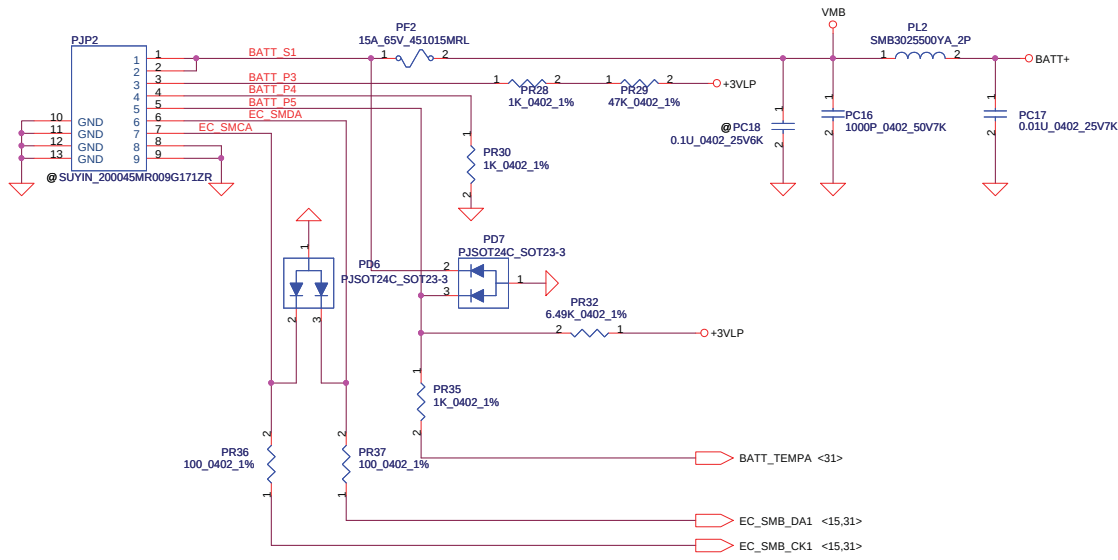
SP093MX0000



**Precharge detector
15.97V/14.84V FOR
ADAPTOR**

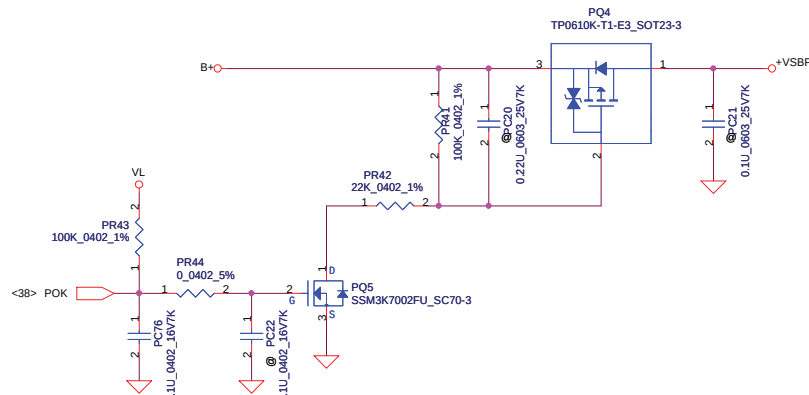
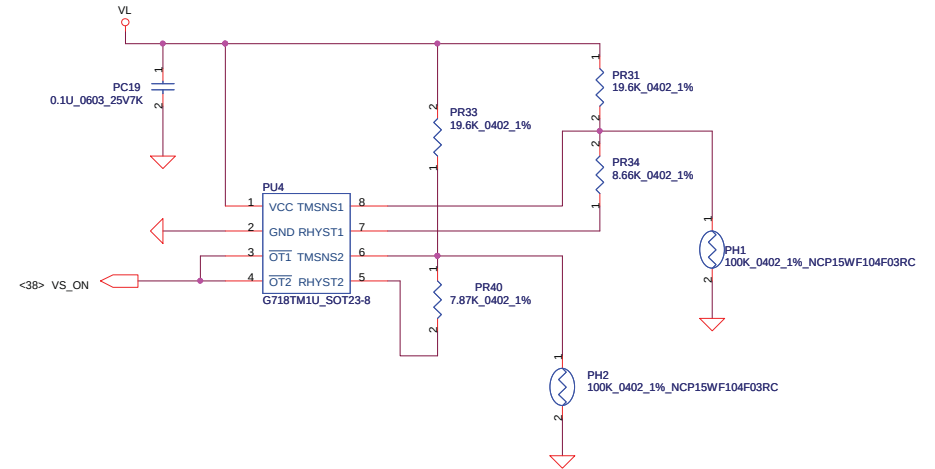


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Deciphered Date				2010/01/23				NWQAA LA6061P M/B			
Title				Size				Rev 2.0			
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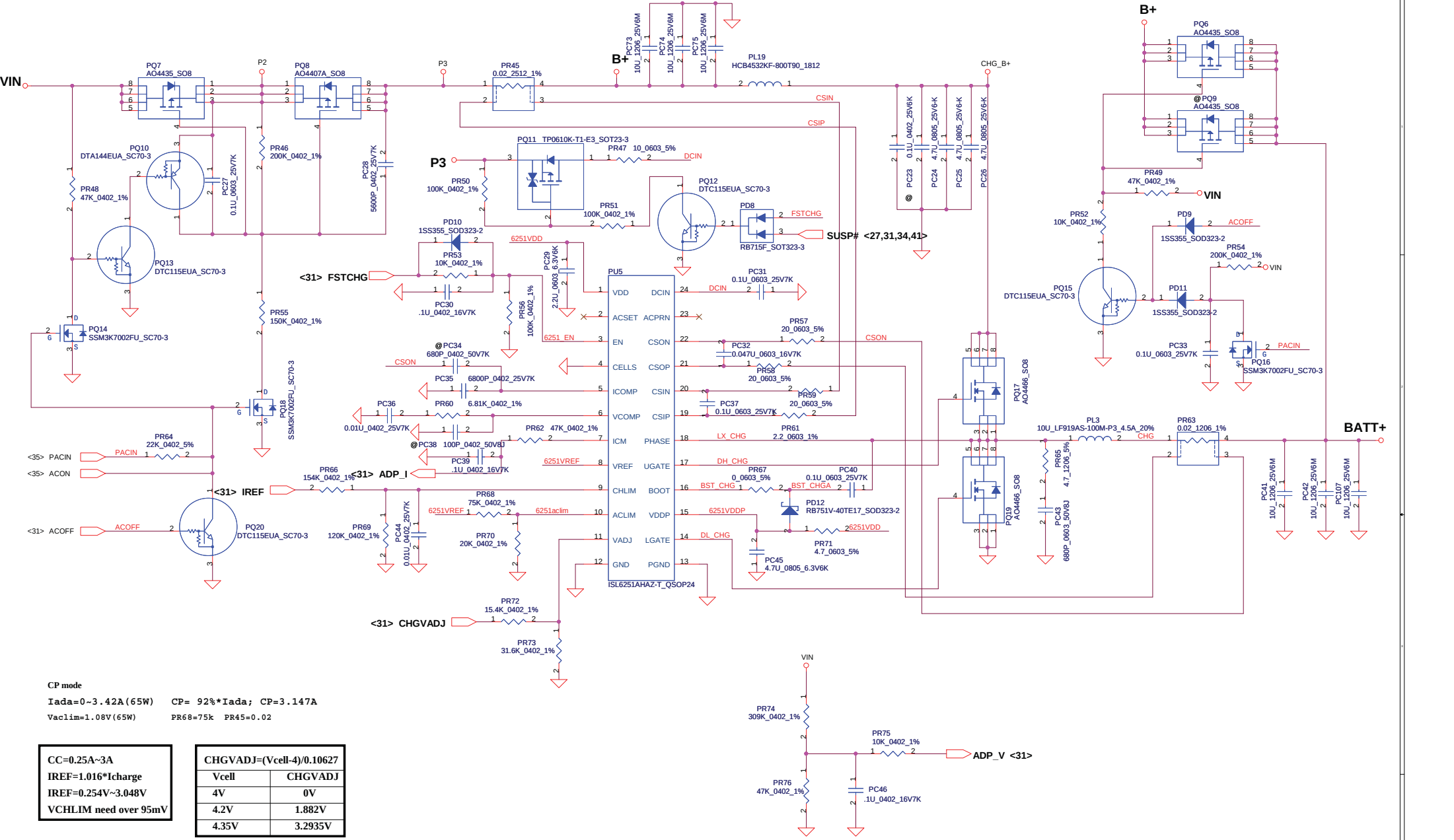


PH1 under CPU bottom side :
CPU thermal protection at 95degree C
Recovery at 56 degree C

PH2 near main Battery CONN :
BAT. thermal protection at 95 degree C
Recovery at 48 degree C



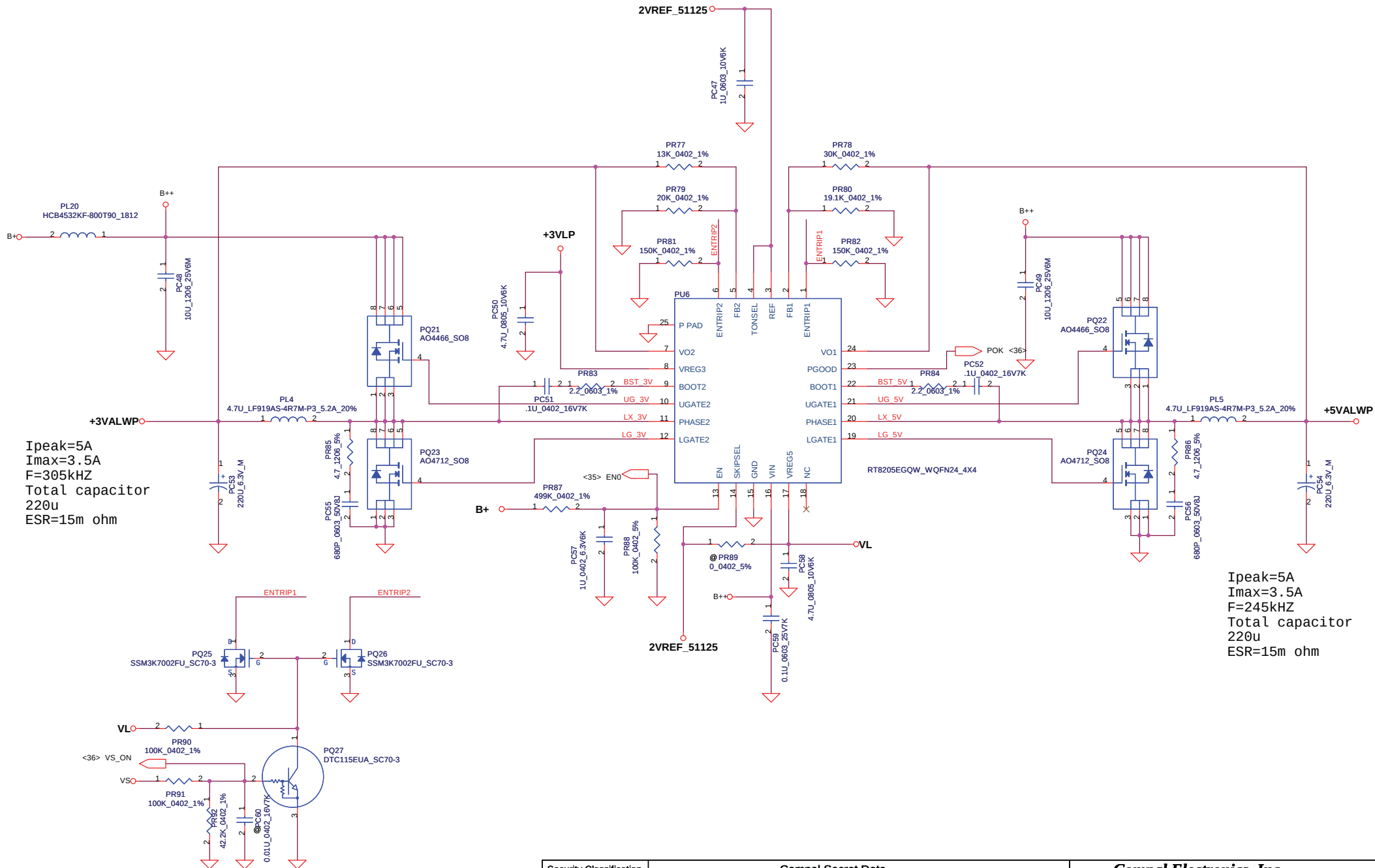
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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
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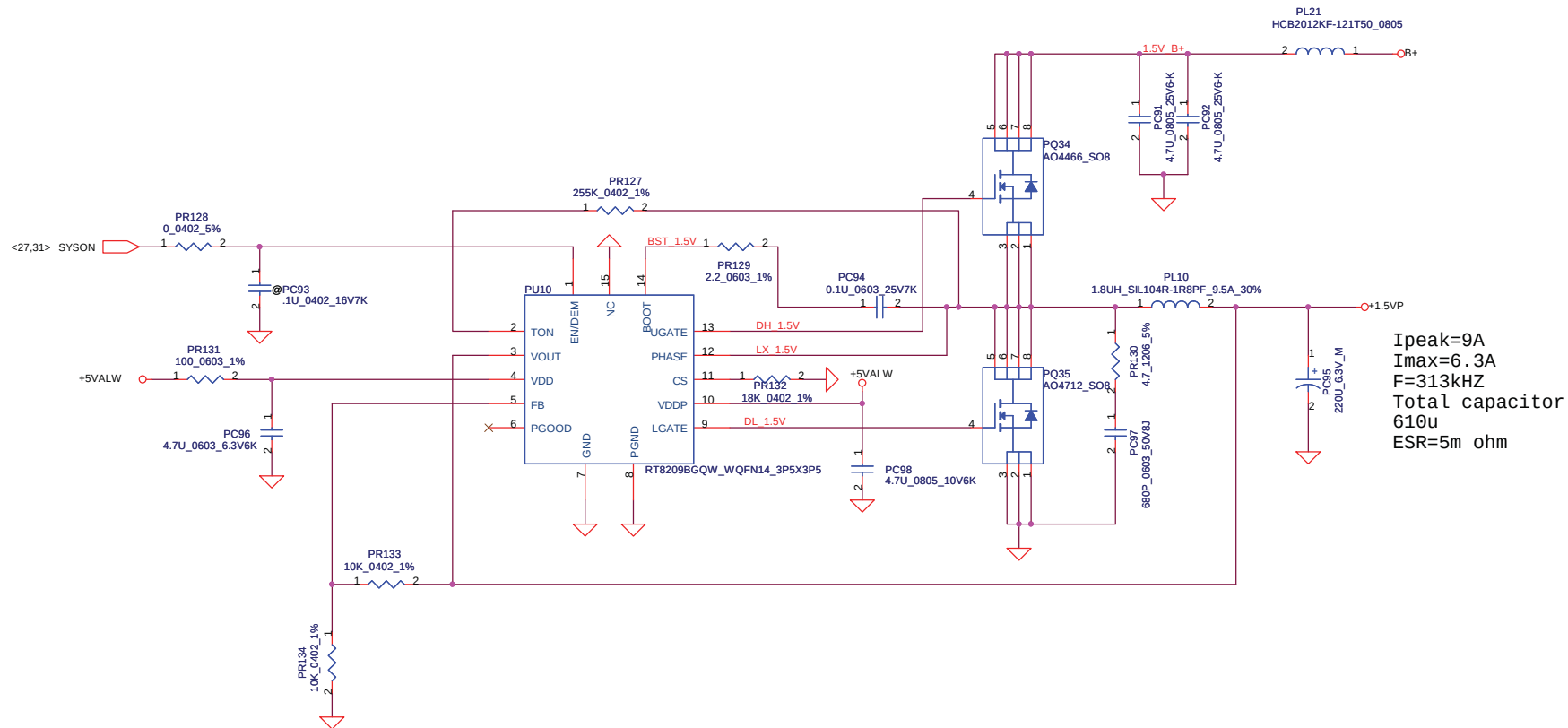
CP mode
 $I_{ada}=0\sim3.42A(65W)$ $CP=92\%*I_{ada}$; $CP=3.147A$
 $V_{aclim}=1.08V(65W)$ $PR68=75k$ $PR45=0.02$

$CC=0.25A\sim3A$
 $I_{REF}=1.016*I_{charge}$
 $I_{REF}=0.254V\sim3.048V$
 V_{CHLIM} need over 95mV

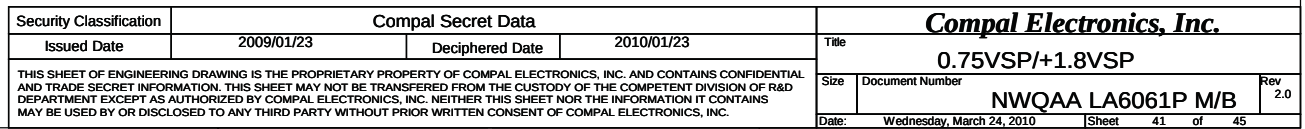
CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V



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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	+1.5VP
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	+CPU CORE
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NO DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT	P39-PWR_+VTTTP	Change PR141 2.26k to 2.43k	Modify VTTTPWR0K voltage (2009/11/25)
EVT	P39-PWR_+VTTTP	Remove PC71 33P, PC72 2200P, PR101 33.2k	APW7138 not use this function (2009/11/25)
EVT	P38-PWR_3VALWP/5VALWP	Change PR92 49.9k to 42.2k	Modify VS divider voltage to drive MOS (2009/11/25)
EVT	P42-PWR_CPU_CORE	Change PL12,PL14 SH000005680 to SH00000IK00	Use 5% DCR choke (2009/11/25)
EVT	P43-PWR_GM VGA_CORE	Change PH5 SL20000058L to SL200000500	Use Compal PN (2009/11/25)
DVT	P48-PWR_BATTERY CONN / OTP	Add PD6, PD7 ESD diode	For ESD solution(2009/12/28)
DVT	P43-PWR_GM VGA_CORE	Change PL16 SH00000HK00 to SH00000IK00	Use same PN choke (2009/12/28)
DVT	P42-PWR_CPU_CORE	Change PC114, PC111, PC185 from SF000000F80 to SF000000W00	Cost down (2009/12/28)
DVT	P43-PWR_GM VGA_CORE	Change PC161 to SGA000002680	For DVT budding(thermal issue), it will change to original type for PVT (2009/12/28)
DVT	P50-PWR_3VALWP/5VALWP	Change PR83,PR84 0 to 2.2	Add boost resistor(For EMI solution)(2009/12/28)
		Add PR85,PR86 4.7 and PC55,PC56 680P	Add snubber(For EMI solution)(2009/12/28)
DVT	P42-PWR_CPU_CORE	Change PR166,PR207 0 to 2.2	
		Add PR169,PR210 4.7 and PC118,PC150 680P	
DVT	P55-PWR_GM VGA_CORE	Change PR234 0 to 2.2	Add boost resistor(For EMI solution)(2009/12/28)
		Add PR235 4.7 and PC163 680P	Add snubber(For EMI solution)(2009/12/28)
DVT	P48-PWR_BATTERY CONN / OTP	Change PR33 10k,PR31 21k to 19.6k, PR34 9.53k to 8.66k, PR40 47k to 7.87k	Adjust OTP setting point(2009/12/28)
DVT	P39-PWR_+VTTTP	Change PR98 4.99k to 6.49k	Adjust VTT_DIS OCP to 27.49A (2009/12/31)
DVT	P49-PWR_CHARGER	Add PC73,PC74,PC75 10U	Reserve for EMI solution(2009/12/28)
DVT	P42-PWR_CPU_CORE	Change PR204 8.25k to 8.87k	Adjust resistor for Imon (2009/12/31)
DVT	P55-PWR_GM VGA_CORE	Change PR247 34.8k to 40.2k	Adjust GFX load line (2009/12/31)
DVT	P41-PWR_0.75VSP/1.8VSP	Change PC90 SE025681K80 to SE024681J80	Use same PN (2009/12/31)
PVT	P41-PWR_0.75VSP/1.8VSP	Remove PR136, Add PR137 0 Ohm	For S3 power saving function (2010/02/03)
PVT	P43-PWR_GM VGA_CORE	Change PC161 to SF000002000	Change to original type for PVT (2010/02/03)
PVT	P49-PWR_CHARGER	Change PC24,PC25,PC26 4.7U to 10U	For EMI solution(ISN test) (2010/02/03)
PVT	P49-PWR_CHARGER	Add PC107 10U	For EMI solution(ISN test) (2010/02/03)
PVT	P49-PWR_CHARGER	Add PC73,PC74,PC75 10U	For EMI solution(ISN test) (2010/02/03)
PVT	P49-PWR_CHARGER	Add PC76 0.1U	For ESD solution (2010/02/03)
PVT	P38-PWR_3VALWP/5VALWP	Change PQ27 from SSMK7002 to DTC115EUA	Use low Vth Transistor (2010/02/03)
PVT	P43-PWR_GM VGA_CORE	Change PQ46 TPCA8030 to NTMFS4921NHT1G	For EMI solution (2010/02/03)
Pre MP	P52-PWR_1.05VSP/1.8VSP	Change PR123 316k to 25.5k,PR124 402k to 51.1k	Adjust 1.8V voltage divided resistor (2010/03/07)
Pre MP	P52-PWR_1.05VSP/1.8VSP	Change PU9 from MP2121 to SY8033	MP2121 ESD fail (2010/03/07)
Pre MP	P52-PWR_1.05VSP/1.8VSP	Delete PR125 0 Ohm	Change for SY8033 solution(2010/03/07)
		Change PC85 from 0.1U to 22U	
		Delete PC87 10UF, PC84 0.1U	
Pre MP	P52-PWR_1.05VSP/1.8VSP	Change PC86 10U to 68P	Improve 1.8V transient under shoot(2010/03/07)
Pre MP	P49-PWR_CHARGER	Change PC24,PC25,PC26 10U to 4.7U	10U 0805 size price too high(2010/03/07)
Pre MP	P47-PWR_DCIN/DECTOR	Change PC12 from SE033105Z80 to SE000001380	Change PN(2010/03/07)

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PIR (Product Improve Record)

NWQAA LA-6061P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2
GERBER-OUT DATE: 2009/12/30

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/7	25	Add +5VALW for JPIO pin5	For BACK_SENSE detect
2	12/7	13	Remove JLVDS pin10 and pin12 for +LCDVDD_R	3D Panel max. current is 1.5A
3	12/8	33	Combine JTOUCH and JLP to JTPL and remove C648	For ME cost down
4	12/17	33	Remove D19	Move D19 to LS-6061P
5	12/18	26	Reverse JBT pin definition	Due to pin reverse
6	12/18	30	Add RA43	For codec EC_MUTE# issue
7	12/21	29	Change JREAD to Push-push type (R015-211-LM-A)	For PRD update
8	12/21	13	Move LED_PWM and BKOFF#_R to JLVDS pin10 and pin12	For avoiding +LCD_INV short issue
9	12/22	32	Change H7 footprint to "DEBUG_PAD-MB-S"	For debug use
10	12/23	27	Add D24 and Q36 for BT_CTRL	For WLAN & BT combo module
11	12/23	21	Add R461	For CIR_EN#
12	12/24	25	Change JPIO footprint and reverse its pin definition	For ME request
13	12/24	15	Add R145	For U9 ESD damage issue
14	12/24	29	Add F3	For Card reader issue
15	12/29	25	Add R148 and R149	For Sleep & play music
16	12/29	13	Add C871 and C872	For RF request

NWQAA LA-6061P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2 TO 0.3
GERBER-OUT DATE: 2010/02/08

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	1/15	30	Add RA43	For sleep & music on battery mode
2	1/21	31	Add R462	Avoid VR_ON floating
3	1/25	32	Change UG3 to SA000022I00	For LDO issue
4	1/25	33	Change SW2 to @	For ME interfere issue
5	2/1	15	Add R130	For AOC monitor issue
6	2/1	31	Change U19 to SA00001J5A0	For KB926 E0 version
7	2/1	29	Remove F3	For UC1 ES2 sample
8	2/1	16	Add D19 and R150	For RTC charge issue
9	2/2	31	Add CAP_RST# to EC	For ESD issue
10	2/3	29	Change RC7 to 33 ohm	For EMI request

NWQAA LA-6061P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3 TO 1.0
GERBER-OUT DATE: 2010/03/15

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/6	29	Add QC2 and RC16	For O2 B0 workaround
2	3/7	16	Change D13.2 power to +CHGRTC	For RTC issue
3	3/12	33	Change H15-H19 to H_3P3	For ME request
4	3/15	33	Remove SW2	For ESD request
5	3/15	30	Change CA9 and CA10 to 1U	For cut-off frequency
6	3/16	30	Change MONO_IN to AGND	For high frequency noise issue

NWQAA LA-6061P SCHEMATIC CHANGE LIST
REVISION CHANGE: 1.0 TO 2.0
GERBER-OUT DATE: 2010/03/19

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/17	29	Change cardreader to JMB385/389	For customer request
2	3/18	31	Remove D86	For ESD request
3	3/18	22	Add R52	For CRT wave issue
4	3/19	22	Change L12 to 2.2 ohm	For CRT wave issue
5	3/22	15	Add D54	For HDMI CEC issue
6	3/24	13	Change C213 to 1U	For NALAA ESATA performance low issue

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