

PWWAA

LC Marseille

LA-6842P REV 0.2 Schematic

Intel Processor (ARD) /PCH (HM55)

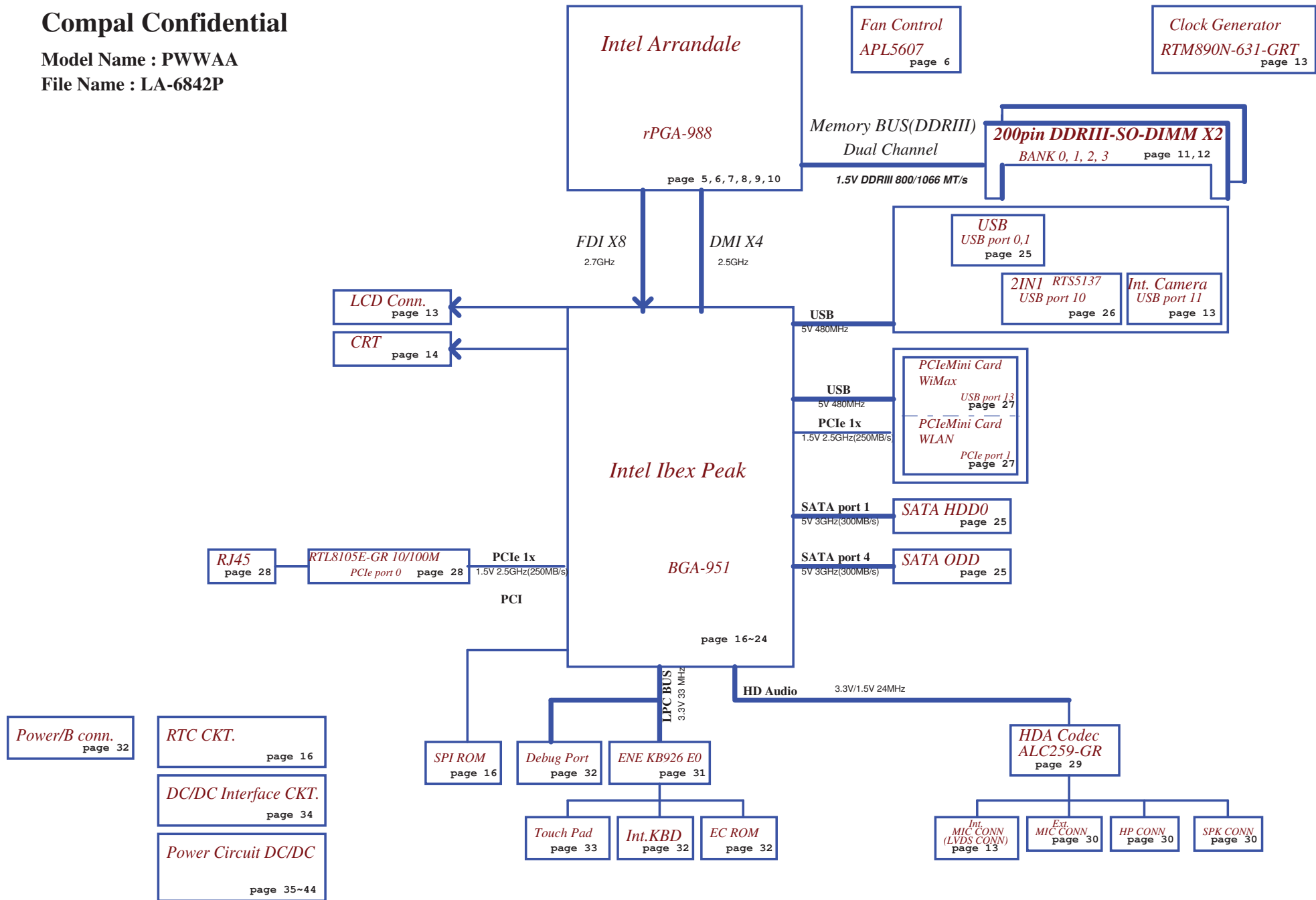
2010-07-22 Rev 0.2

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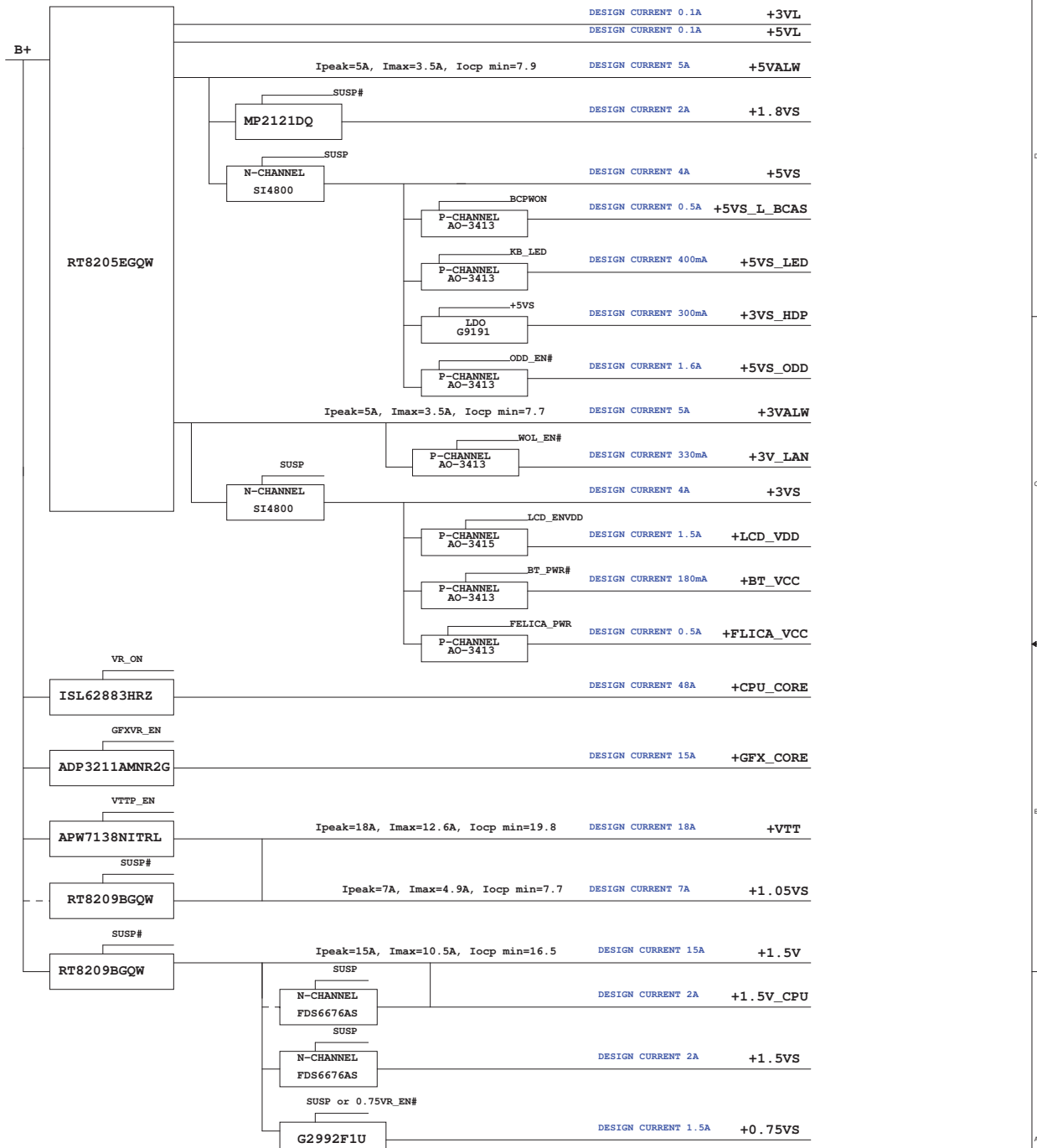
Compal Confidential

Model Name : PWWAA

File Name : LA-6842P



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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		

EC SM Bus1 Address

EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
Power	Device	HEX	Address				

BTO Option Table

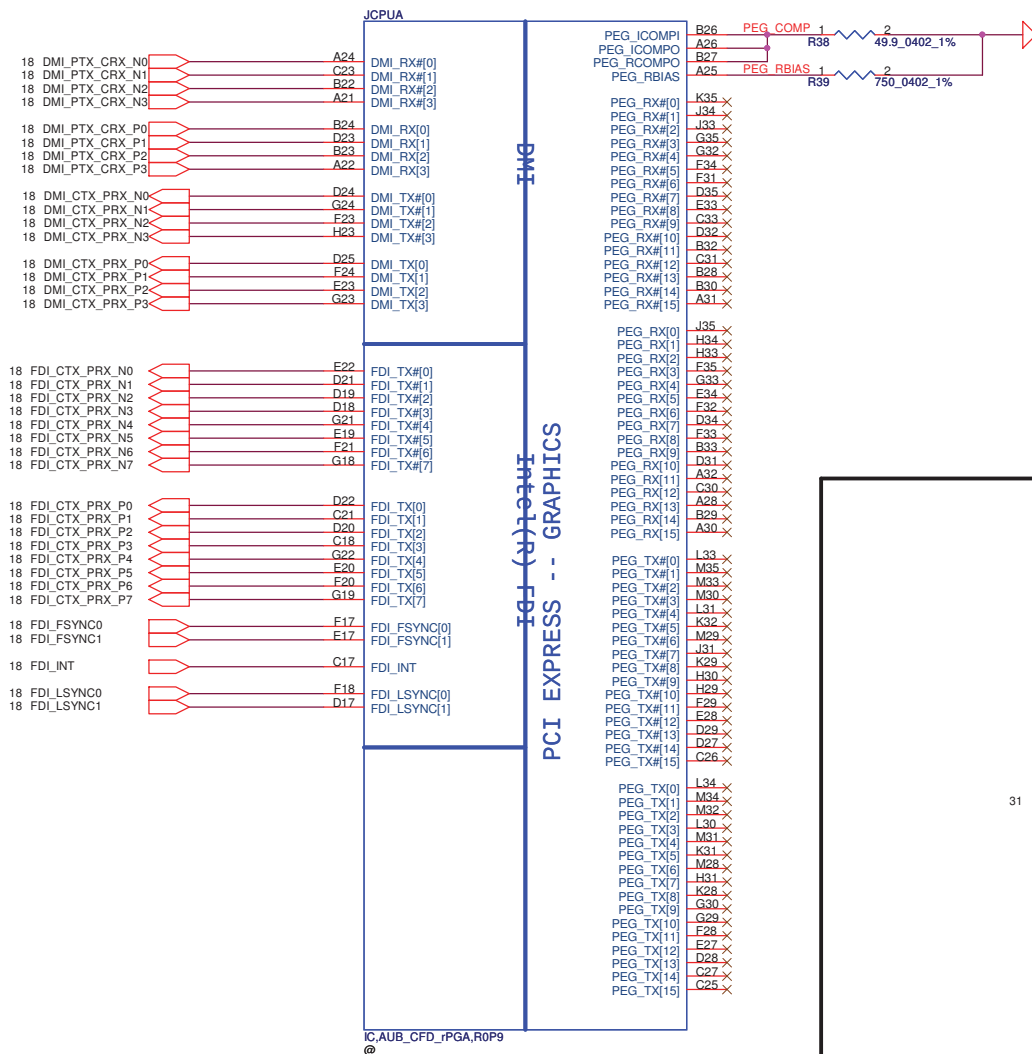
Function	MINI PCI-E SLOT		LAN					
description			SLOT1	LAN				
explain			WLAN/BT	10/100M				
BTO								

Function				Camera & Mic		
description				Camera & Mic		
explain				Camera & Mic		
BTO				CAM@		

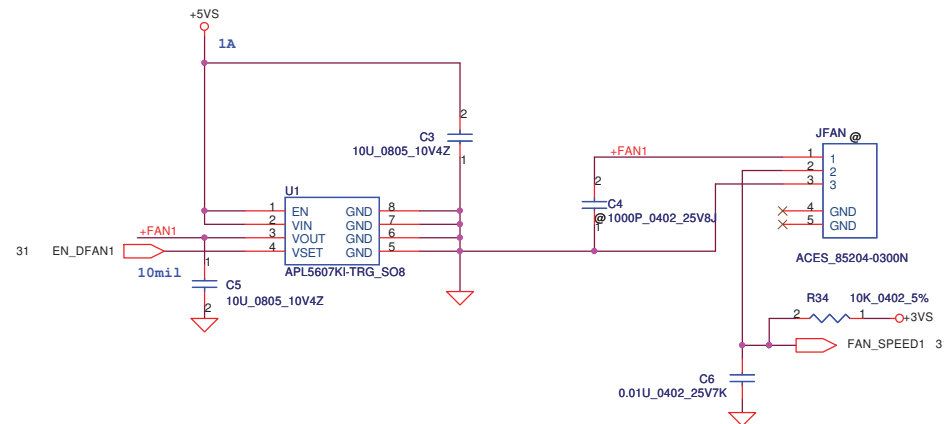
Function	S3 Power Saving	
description	S3 Power Saving	
explain		Power Saving
BTO		

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

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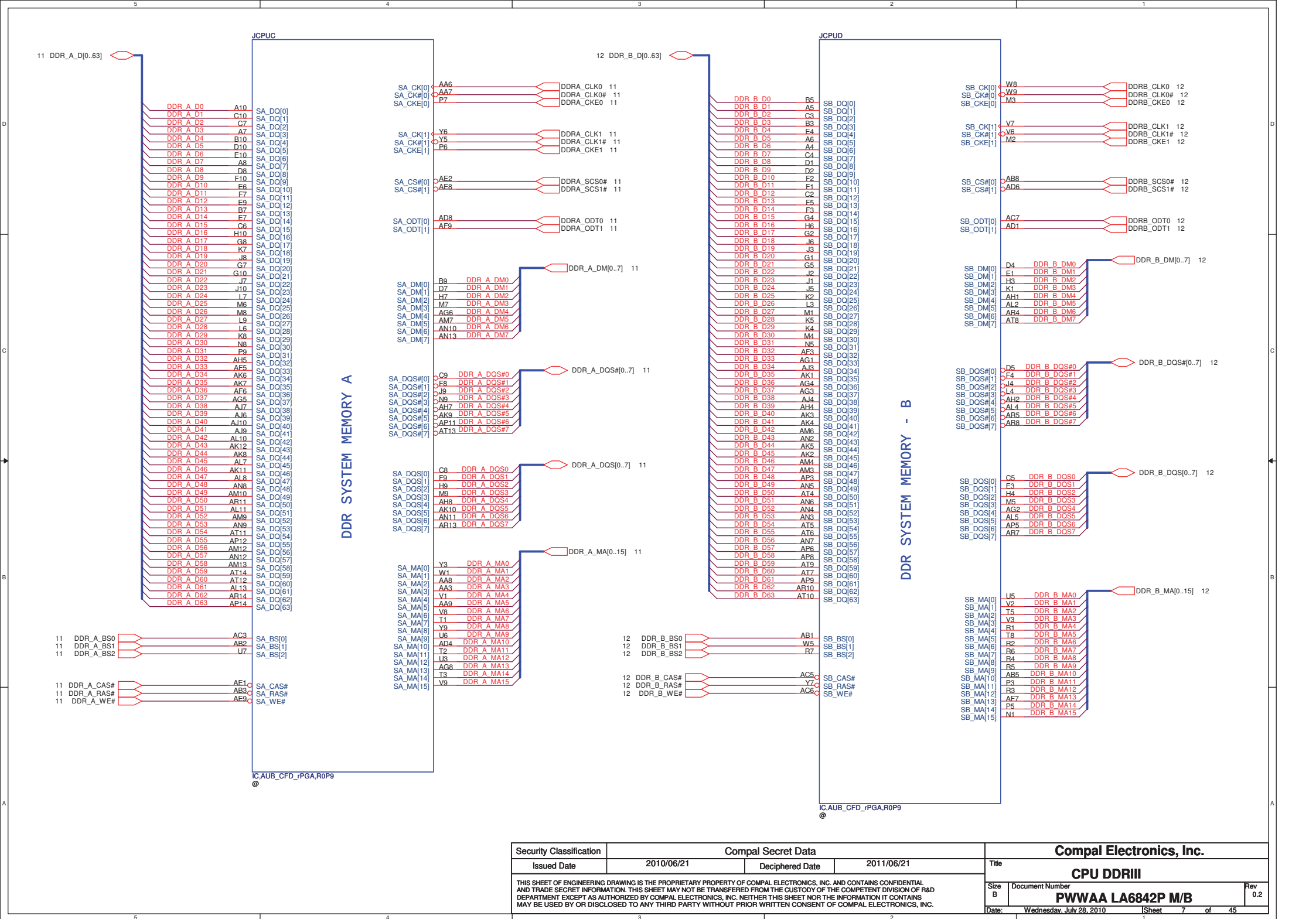


FAN Control Circuit

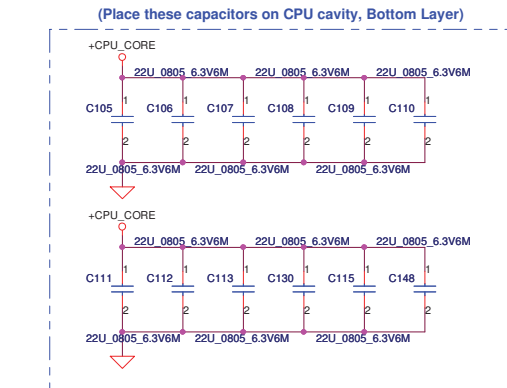
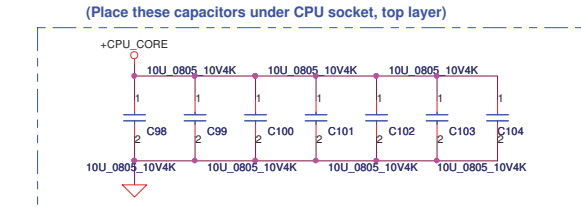
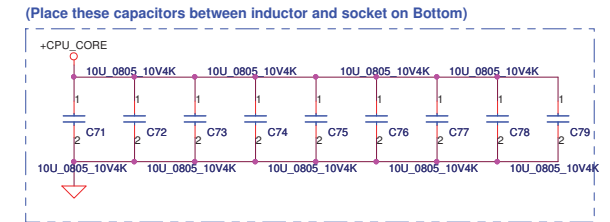
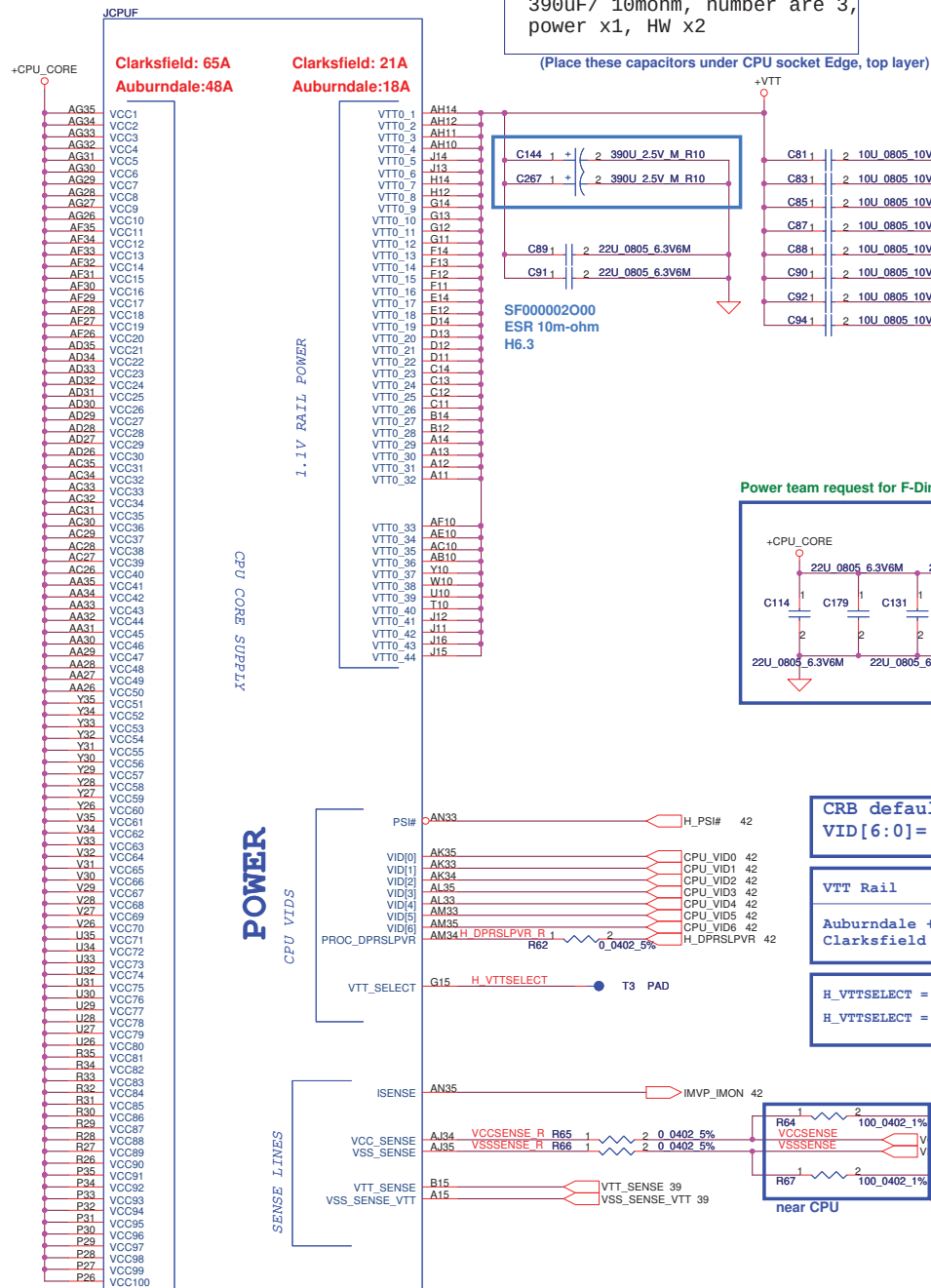


Remove Cap, for EMI

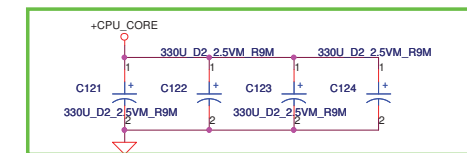
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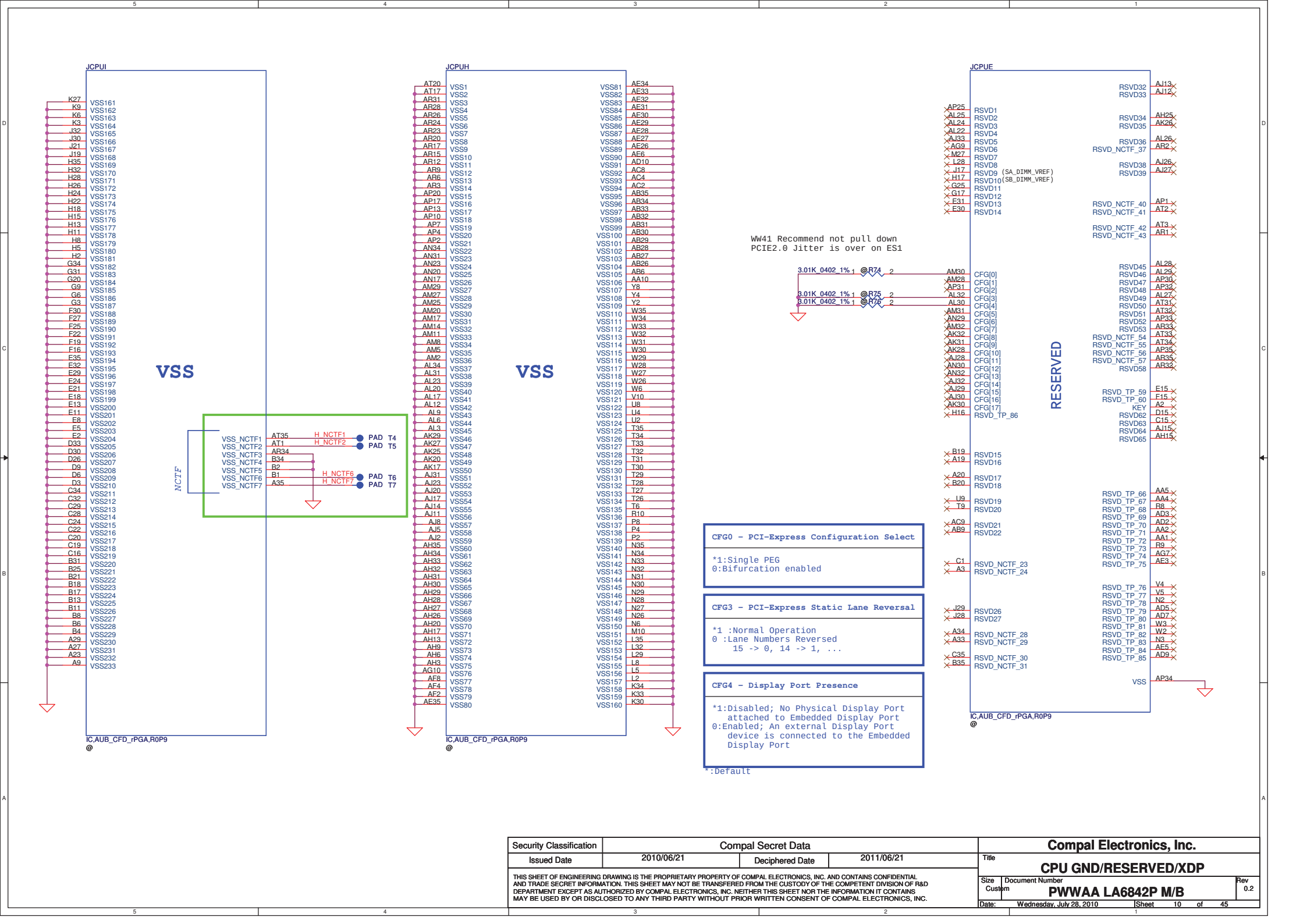
TOP side (under inductor)

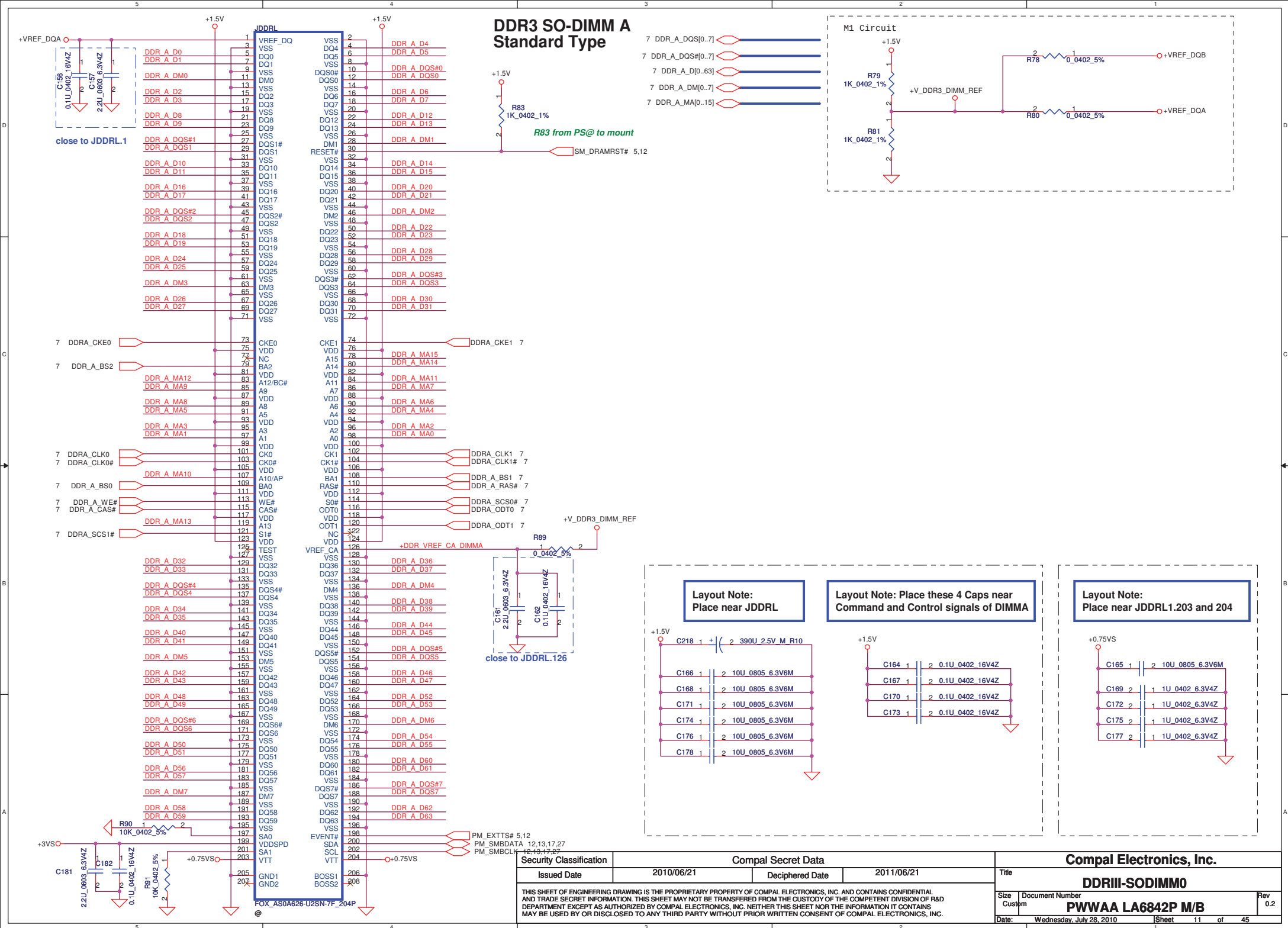


Check list:

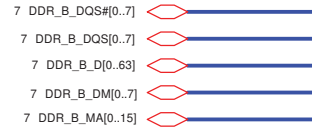
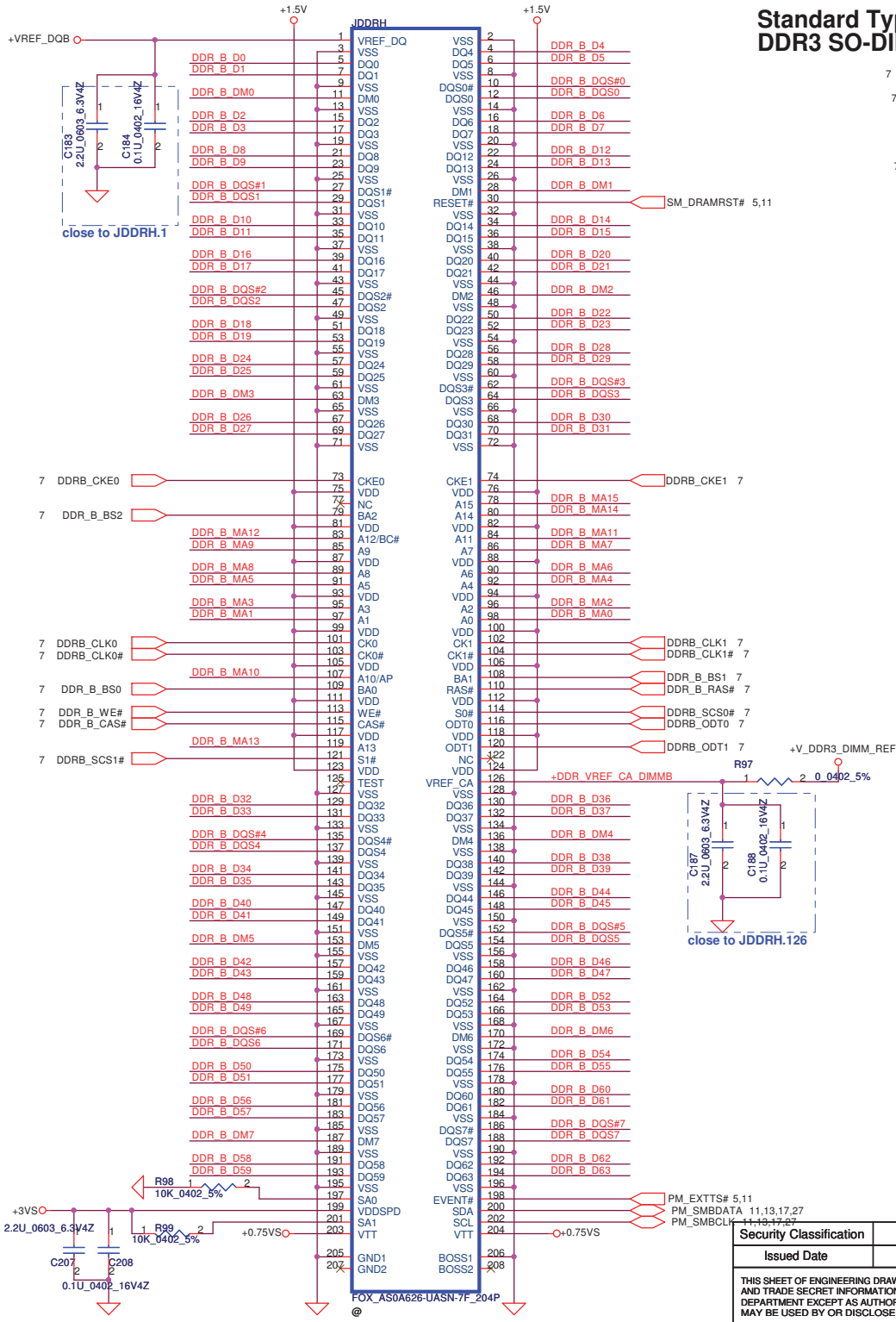
+CPU_CORE: 6x 470uF, 12x 22uF, 17x 10uF
+VTT: 4x 330uF, 7x 22uF, 8x 10uF

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						Size		Document Number		PWWAA LA6842P M/B		Rev 0.2	
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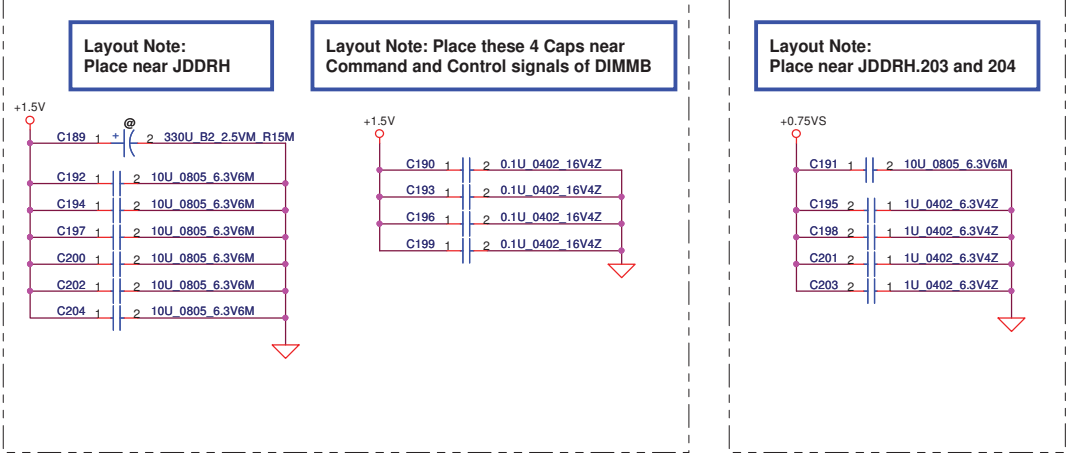
Standard Type DDR3 SO-DIMM B



Layout Note:
Place near JDDRRH

Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB

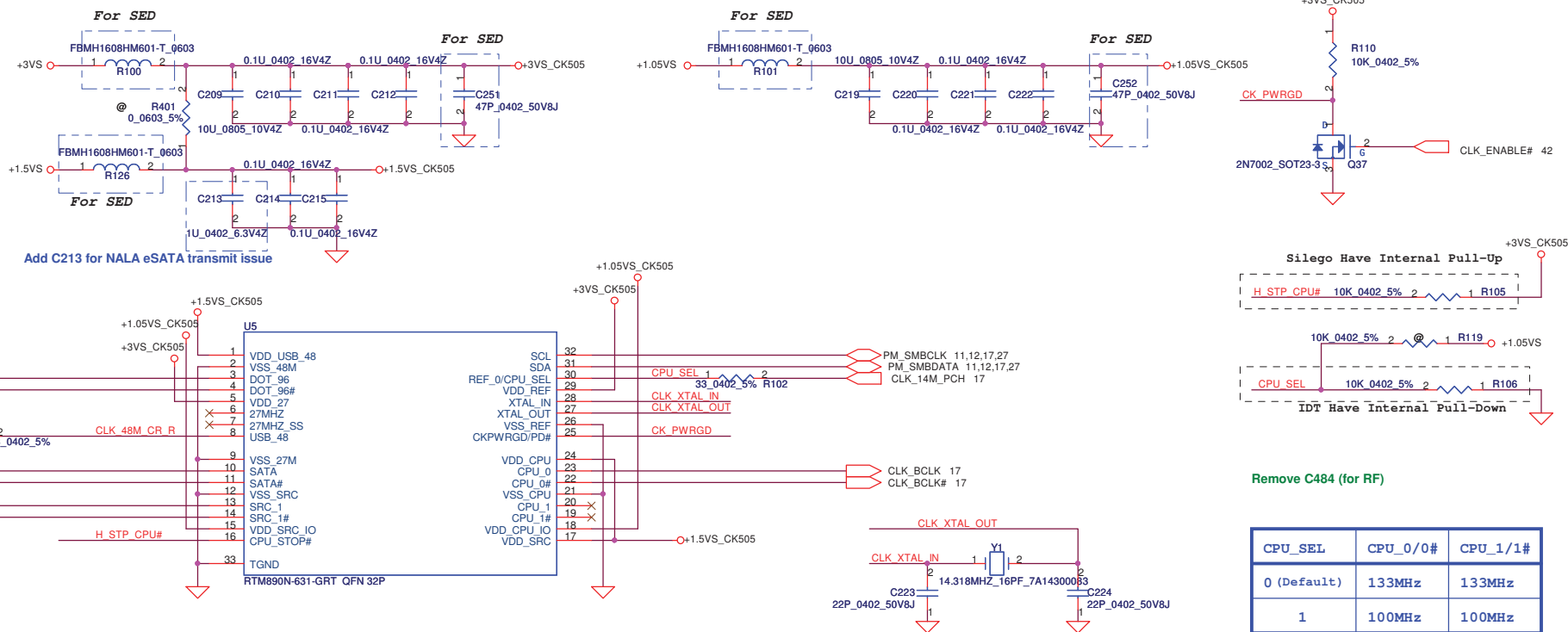
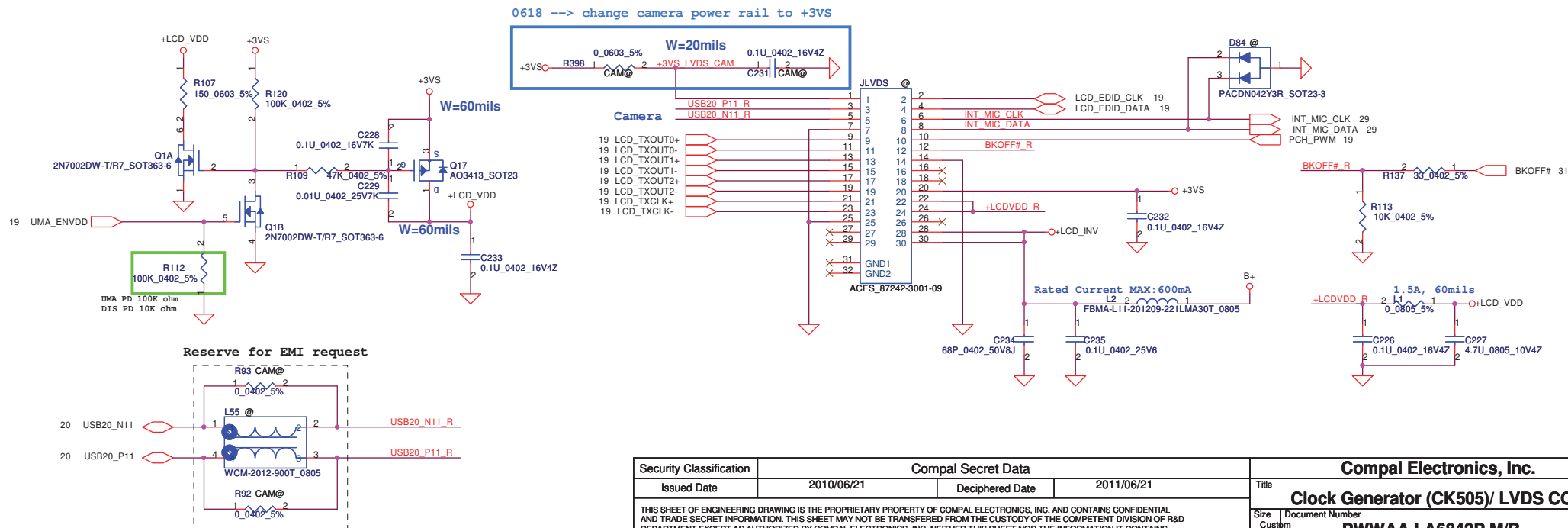
Layout Note:
Place near JDDRRH.203 and 204



11.19.17.27

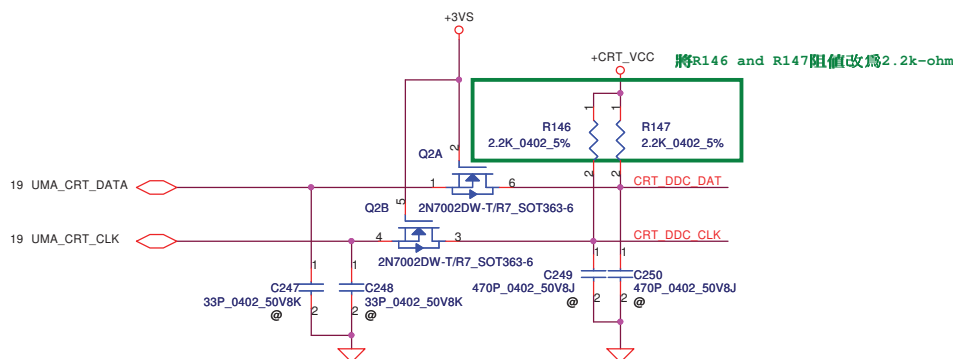
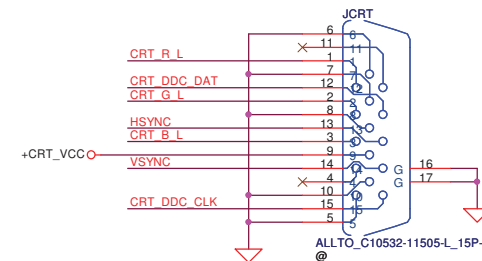
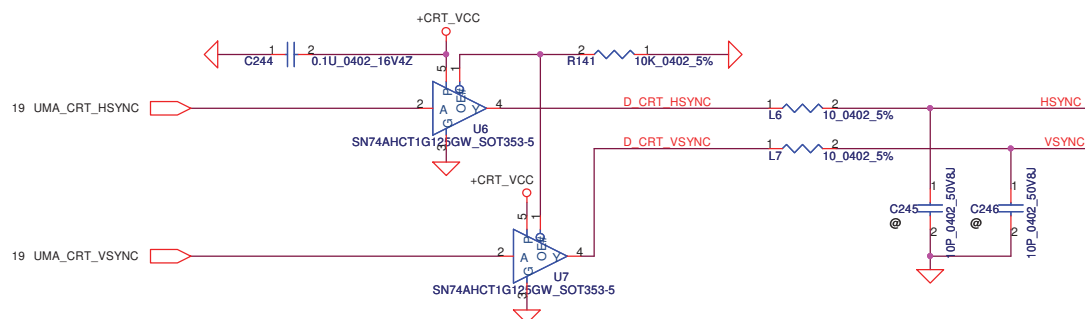
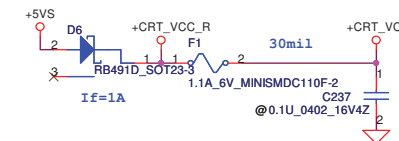
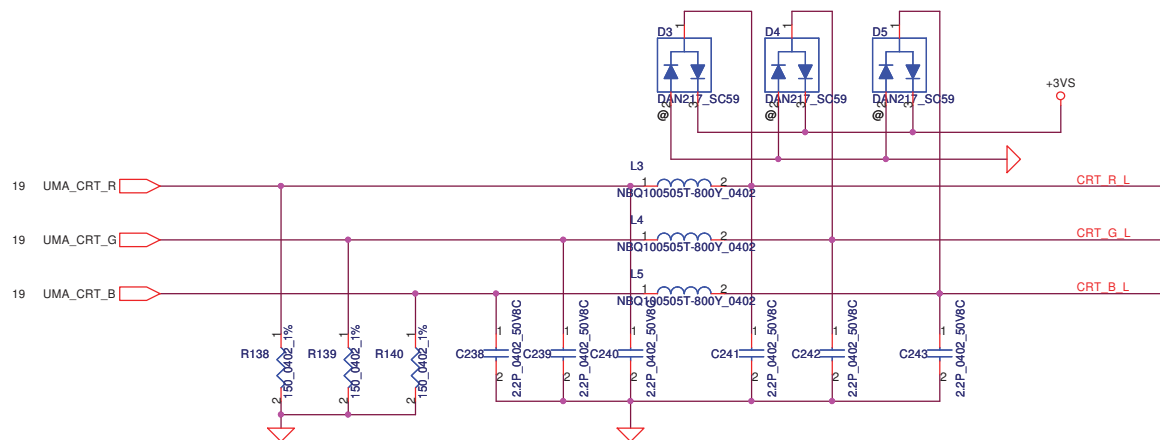
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Clock Generator

**LVDS / Int.Camera / Int.MIC Conn**

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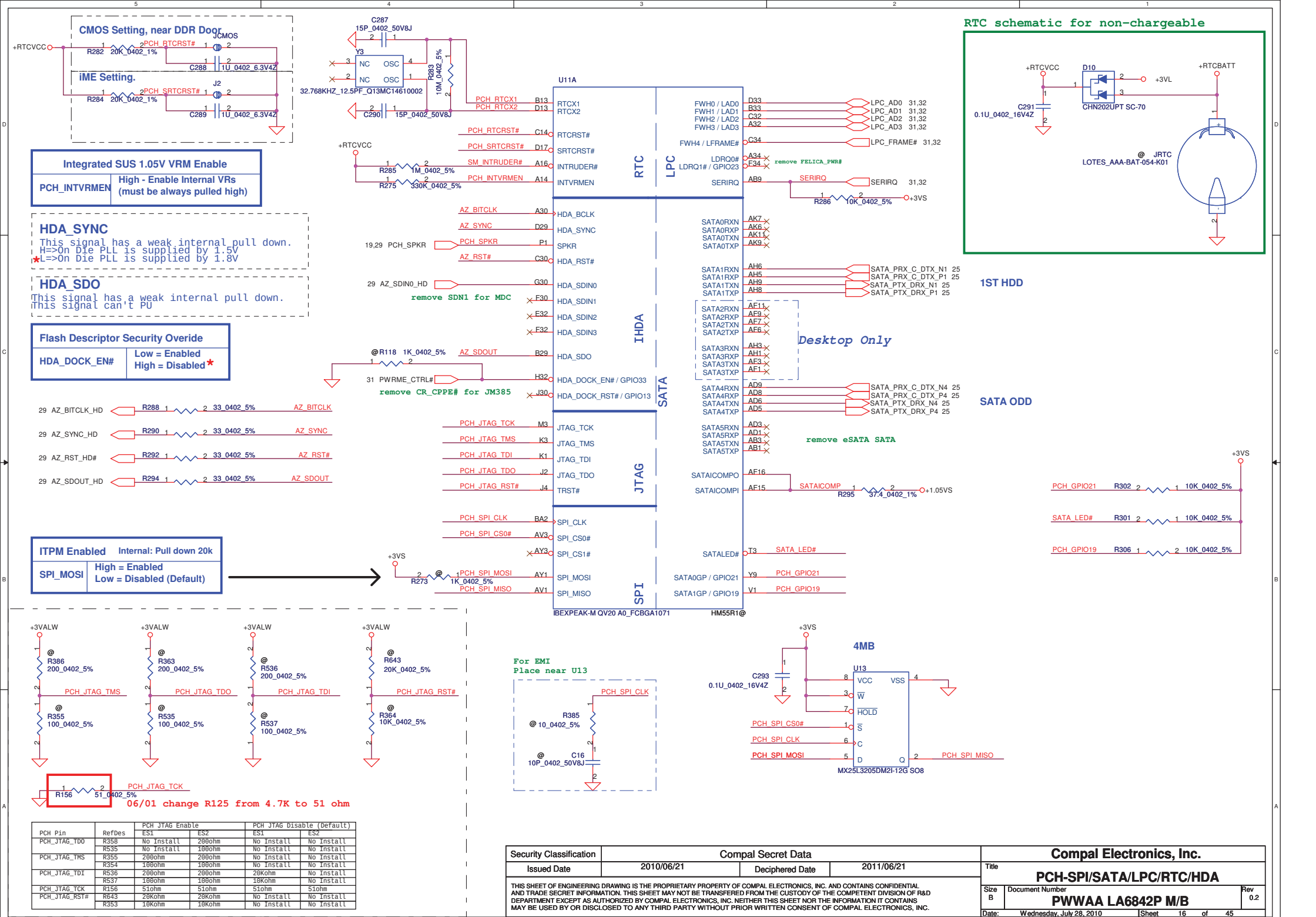
CRT CONNECTOR



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0624 --> Remove BIOS ROM Debug Circuit

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For LAN

28 PCIE_PRX_C_LANTX_N1
28 PCIE_PRX_C_LANTX_P1
28 PCIE_PT_X_C_LANRX_N1
28 PCIE_PT_X_C_LANRX_P1

For WLAN

27 PCIE_PRX_WLANTX_N2
27 PCIE_PRX_WLANTX_P2
27 PCIE_PT_X_C_WLANRX_N2
27 PCIE_PT_X_C_WLANRX_P2

remove NewCard PCIE

remove JET PCIE

remove CardReader PCIE

LAN

WLAN

+3VS
10K_0402_5% R244
PCH_GPIO20 form CLKREQ_NEW# to PCH_GPIO20

10K_0402_5% R248
CLKREQ_WLAN# form CLKREQ_WLAN# to PCH_GPIO20

+3VALW
10K_0402_5% R246
CLKREQ_LAN# form CLKREQ_LAN# to PCH_GPIO25

10K_0402_5% R245
PCH_GPIO25 form CLKREQ_JET# to PCH_GPIO25

10K_0402_5% R249
PCH_GPIO26 form CLKREQ_CR# to PCH_GPIO26

10K_0402_5% R250
PCH_GPIO44 form CLKREQ_CR# to PCH_GPIO26

10K_0402_5% R251
PCH_GPIO56 form CLKREQ_CR# to PCH_GPIO26

U11B

PCIE_PRX_C_LANTX_N1 BG30
PCIE_PRX_C_LANTX_P1 BJ30
PCIE_PT_X_C_LANRX_N1 BF29
PCIE_PT_X_C_LANRX_P1 BH29

AW30
BA30
PCIE_PT_X_C_WLANRX_N2 C274
PCIE_PT_X_C_WLANRX_P2 C275

AU30
AU32
AV32
PERN3
PERP3
PETN3
PETP3

BA32
BB32
BD32
BE32
PERN4
PERP4
PETN4
PETP4

BF33
BH33
BI33
BJ32
PERN5
PERP5
PETN5
PETP5

BA34
AW34
BC34
BD34
PERN6
PERP6
PETN6
PETP6

AT34
AU34
AU36
AV36
PERN7
PERP7
PETN7
PETP7

BG34
BJ34
BG36
BJ36
PERN8
PERP8
PETN8
PETP8

NC

28 CLK_LAN#
28 CLK_LAN
28 CLKREQ_LAN#
27 CLK_WLAN#
27 CLK_WLAN
27 CLKREQ_WLAN#

AK48
AK47
CLKOUT_PCIE0N
CLKOUT_PCIE0P
P9
CLKREQ_LAN#
AM43
AM45
CLKOUT_PCIE1N
CLKOUT_PCIE1P
U4
CLKREQ_WLAN#
PCIECLKRQ1# / GPIO18

AK47
AK48
CLKOUT_PCIE2N
CLKOUT_PCIE2P
N4
CLKREQ_WLAN#
PCIECLKRQ2# / GPIO20

AK42
AK41
CLKOUT_PCIE3N
CLKOUT_PCIE3P
A8
CLKREQ_WLAN#
PCIECLKRQ3# / GPIO25

AM51
AM53
CLKOUT_PCIE4N
CLKOUT_PCIE4P
M9
CLKREQ_WLAN#
PCIECLKRQ4# / GPIO26

AJ50
AJ52
CLKOUT_PCIE5N
CLKOUT_PCIE5P
H6
CLKREQ_WLAN#
PCIECLKRQ5# / GPIO44

AK53
AK51
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
P13
CLKREQ_WLAN#
PCIECLKRQ6# / GPIO56

PERN1
PERP1
PETN1
PETP1

PERN2
PERP2
PETN2
PETP2

PERN3
PERP3
PETN3
PETP3

PERN4
PERP4
PETN4
PETP4

PERN5
PERP5
PETN5
PETP5

PERN6
PERP6
PETN6
PETP6

PERN7
PERP7
PETN7
PETP7

PERN8
PERP8
PETN8
PETP8

PCI-E*

controller

Link

PEG

From CLK BUFFER

CLKOUT_DP_N / CLKOUT_BCLK1_N
CLKOUT_DP_P / CLKOUT_BCLK1_P

CLKIN_DMI_N
CLKIN_DMI_P

CLKIN_BCLK_N
CLKIN_BCLK_P

CLKIN_DOT_96N
CLKIN_DOT_96P

CLKIN_SATA_N / CKSSCD_N
CLKIN_SATA_P / CKSSCD_P

REFCLK14IN
J42
CLKIN_PCIELOOPBACK

XTAL25_IN
XTAL25_OUT
XCLK_RCOMP

CLKOUTFLEX0 / GPIO64
CLKOUTFLEX1 / GPIO65
CLKOUTFLEX2 / GPIO66
CLKOUTFLEX3 / GPIO67

SMBALERT# / GPIO11
SMBCLK
SMBDATA

SML0ALERT# / GPIO60
SML0CLK
SML0DATA

SML1ALERT# / GPIO74
SML1CLK / GPIO58
SML1DATA / GPIO75

CL_CLK1
CL_DATA1
CL_RST1#

PEG_A_CLKRQ# / GPIO47
CLKREQ_PEG#

CLKOUT_PEG_A_N
CLKOUT_PEG_A_P

CLKOUT_DMI_N
CLKOUT_DMI_P

CLKOUT_DP_N / CLKOUT_BCLK1_N
CLKOUT_DP_P / CLKOUT_BCLK1_P

CLKIN_DMI_N
CLKIN_DMI_P

CLKIN_BCLK_N
CLKIN_BCLK_P

CLKIN_DOT_96N
CLKIN_DOT_96P

CLKIN_SATA_N / CKSSCD_N
CLKIN_SATA_P / CKSSCD_P

REFCLK14IN
J42
CLKIN_PCIELOOPBACK

XTAL25_IN
XTAL25_OUT
XCLK_RCOMP

CLKOUTFLEX0 / GPIO64
CLKOUTFLEX1 / GPIO65
CLKOUTFLEX2 / GPIO66
CLKOUTFLEX3 / GPIO67

CLKOUT_DP_N / CLKOUT_BCLK1_N
CLKOUT_DP_P / CLKOUT_BCLK1_P

CLKIN_DMI_N
CLKIN_DMI_P

CLKIN_BCLK_N
CLKIN_BCLK_P

CLKIN_DOT_96N
CLKIN_DOT_96P

CLKIN_SATA_N / CKSSCD_N
CLKIN_SATA_P / CKSSCD_P

REFCLK14IN
J42
CLKIN_PCIELOOPBACK

XTAL25_IN
XTAL25_OUT
XCLK_RCOMP

SMBALERT# / GPIO11
SMBCLK
SMBDATA

SML0ALERT# / GPIO60
SML0CLK
SML0DATA

SML1ALERT# / GPIO74
SML1CLK / GPIO58
SML1DATA / GPIO75

CL_CLK1
CL_DATA1
CL_RST1#

PEG_A_CLKRQ# / GPIO47
CLKREQ_PEG#

CLKOUT_PEG_A_N
CLKOUT_PEG_A_P

CLKOUT_DMI_N
CLKOUT_DMI_P

CLKOUT_DP_N / CLKOUT_BCLK1_N
CLKOUT_DP_P / CLKOUT_BCLK1_P

CLKIN_DMI_N
CLKIN_DMI_P

CLKIN_BCLK_N
CLKIN_BCLK_P

CLKIN_DOT_96N
CLKIN_DOT_96P

CLKIN_SATA_N / CKSSCD_N
CLKIN_SATA_P / CKSSCD_P

REFCLK14IN
J42
CLKIN_PCIELOOPBACK

XTAL25_IN
XTAL25_OUT
XCLK_RCOMP

CLKOUTFLEX0 / GPIO64
CLKOUTFLEX1 / GPIO65
CLKOUTFLEX2 / GPIO66
CLKOUTFLEX3 / GPIO67

CLKOUT_DP_N / CLKOUT_BCLK1_N
CLKOUT_DP_P / CLKOUT_BCLK1_P

CLKIN_DMI_N
CLKIN_DMI_P

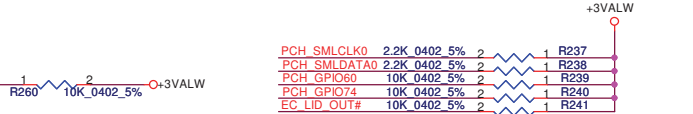
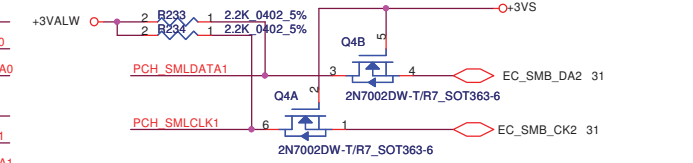
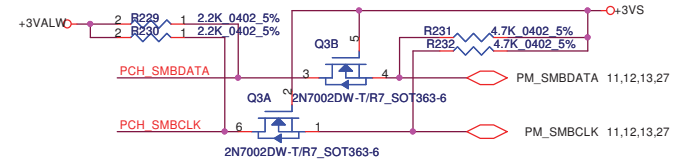
CLKIN_BCLK_N
CLKIN_BCLK_P

CLKIN_DOT_96N
CLKIN_DOT_96P

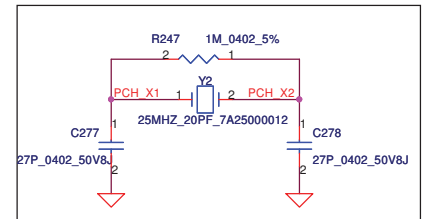
CLKIN_SATA_N / CKSSCD_N
CLKIN_SATA_P / CKSSCD_P

REFCLK14IN
J42
CLKIN_PCIELOOPBACK

XTAL25_IN
XTAL25_OUT
XCLK_RCOMP

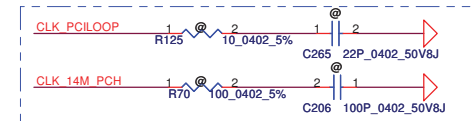


FROM CLK GEN FOR: 133/100/96/14.318 MHZ

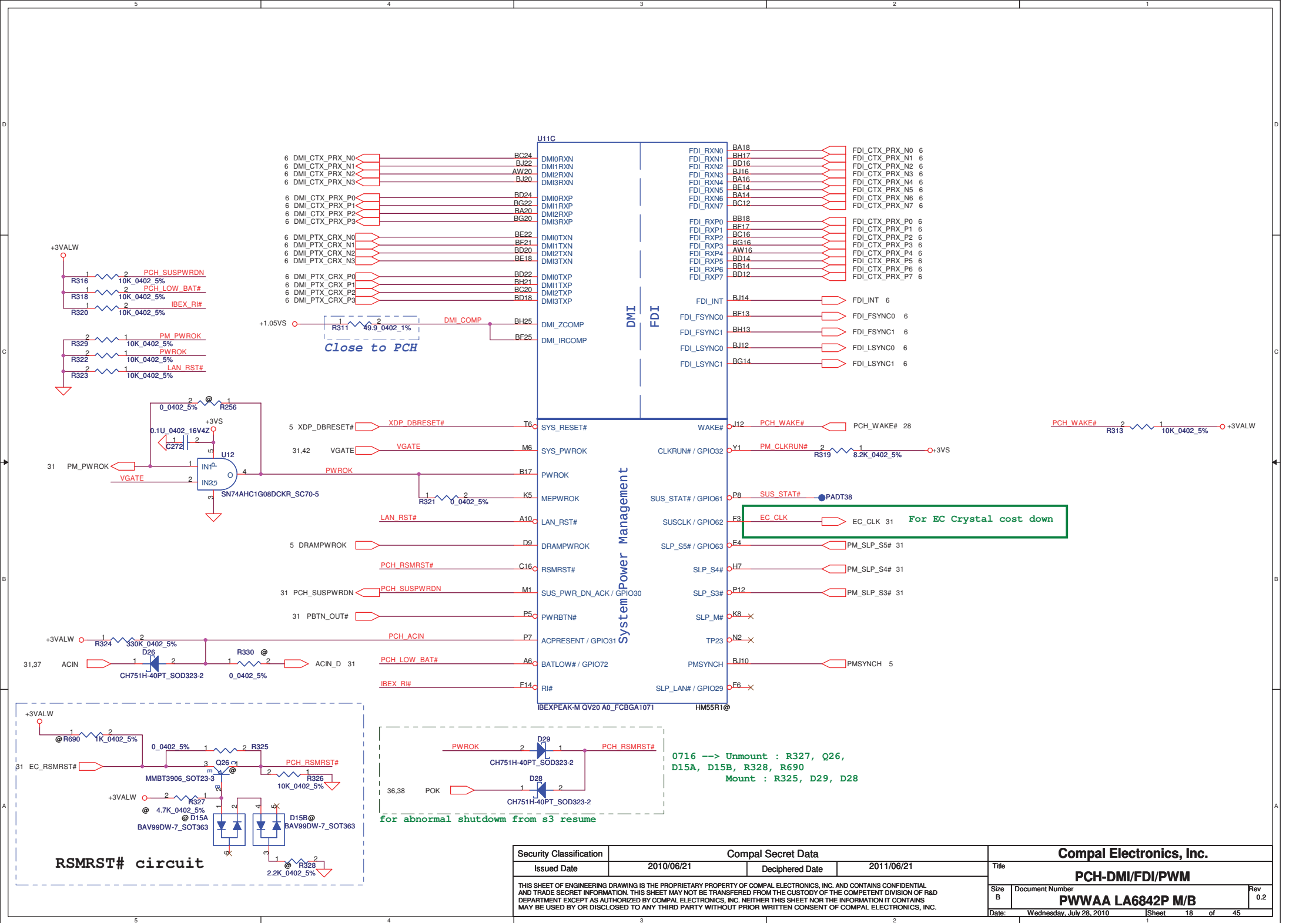


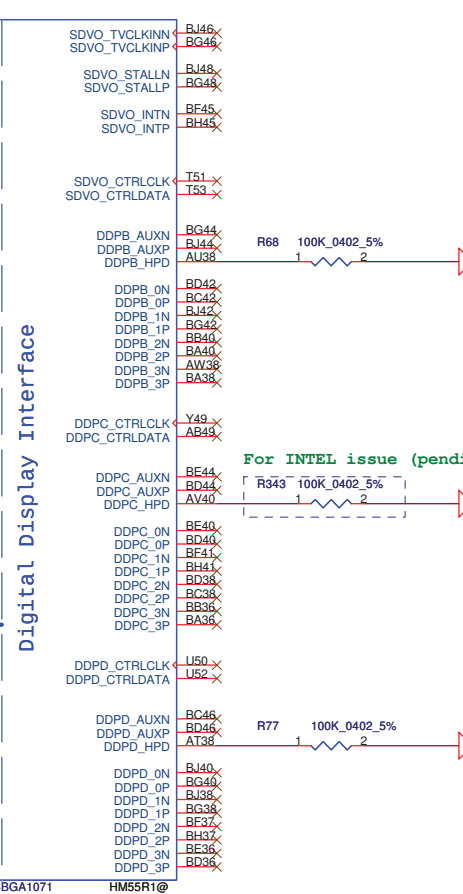
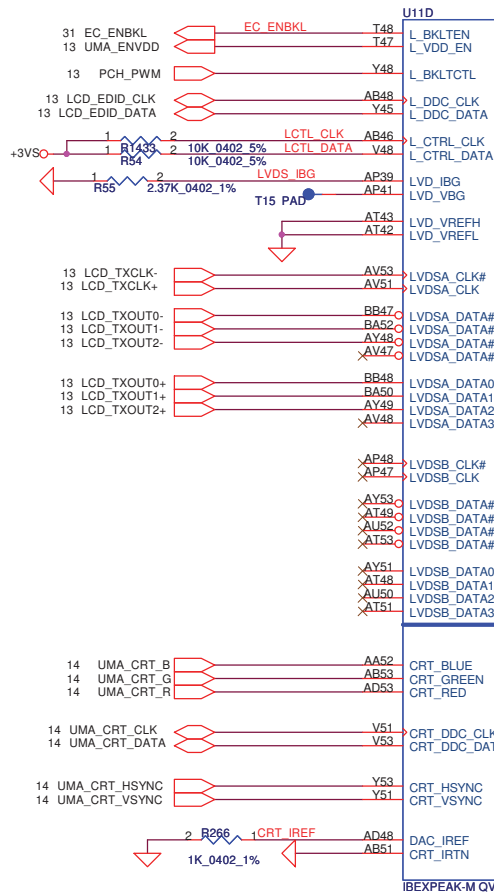
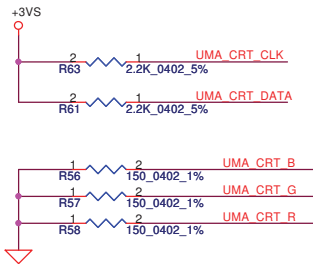
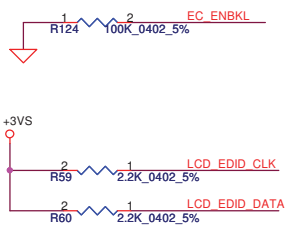
Note: Stuff 0 ohm if 25MHz crystal un-stuff

for EMI request



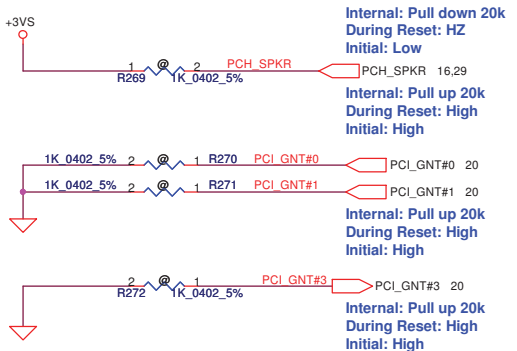
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				Date	Wednesday, July 28, 2010
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For INTEL issue (pending interrupts from the PCH for unused HDMI ports)

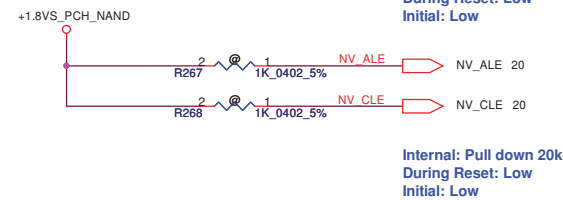
PCH Strap Pin



NO REBOOT Strap		
PCH_SPKR	Low= Disable	High= Enable

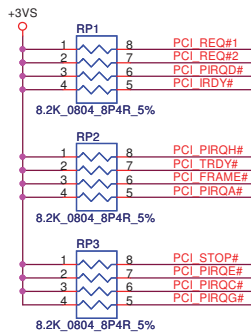
Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI (Default)

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable



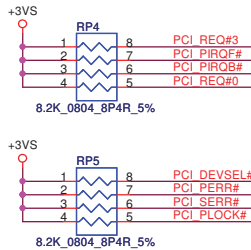
Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)

DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc



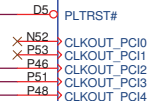
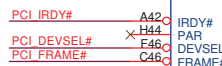
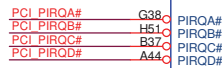
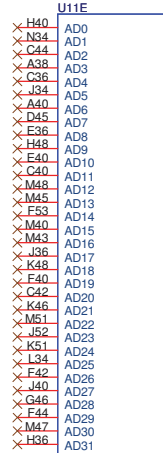
add PCI_REQ#2 for non-ODD_EN#

GNT2#: Not pull low, internal pull up 20K



27,28,31,32 PLT_RST#

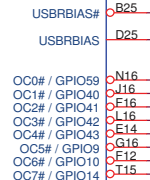
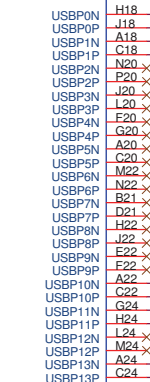
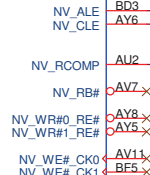
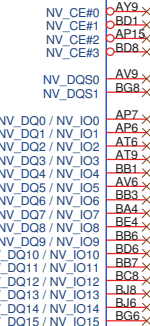
32 CLK_PCI_DDR
 31 CLK_PCI_EC
 17 CLK_PCI_LOOP



PCI

NVRAM

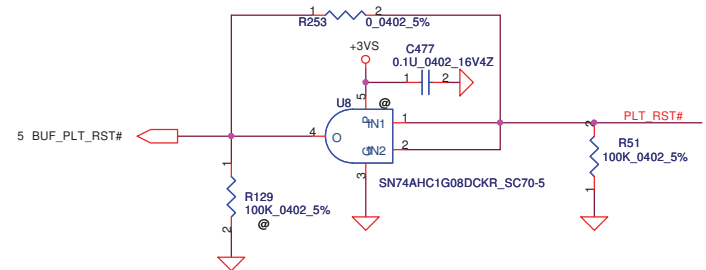
USB



OC0# / GPIO59
 OC1# / GPIO40
 OC2# / GPIO41
 OC3# / GPIO42
 OC4# / GPIO43
 OC5# / GPIO9
 OC6# / GPIO10
 OC7# / GPIO14



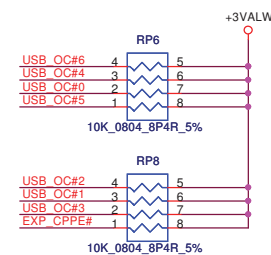
HM55 USB port6/7 NC



USB-LIGHT1
 USB-LIGHT2
 USB-Left1
 remove eSATA
 remove NewCard
 remove BT

remove FingerPr
 remove FELICA
 Card reader(2 in 1)
 Int. Camera
 remove 3G/TV#1
 WiMax(WLAN)

Within 500 mils
 (USB-Right)



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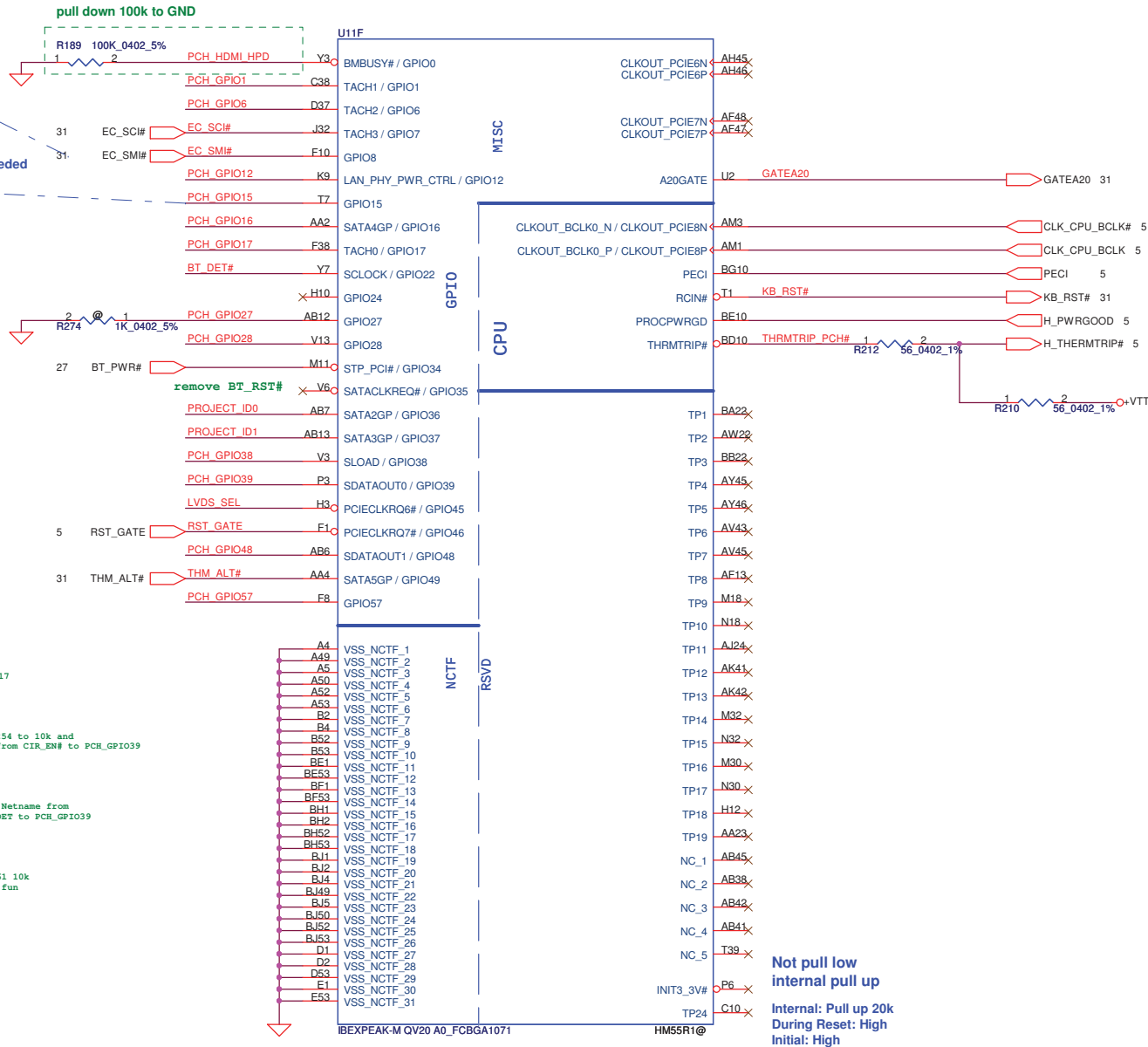
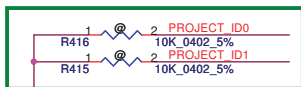
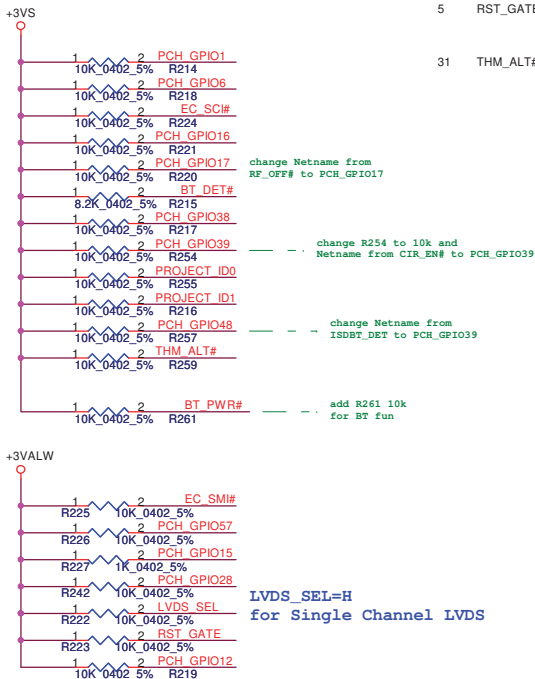
GPIO8
Not pull down
Internal: Pull up 20k
During Reset: High
Initial: High

GPIO15
a Strong pull up may be needed
for GPIO Functionality
Internal: Pull down 20k
During Reset: Low
Initial: Low

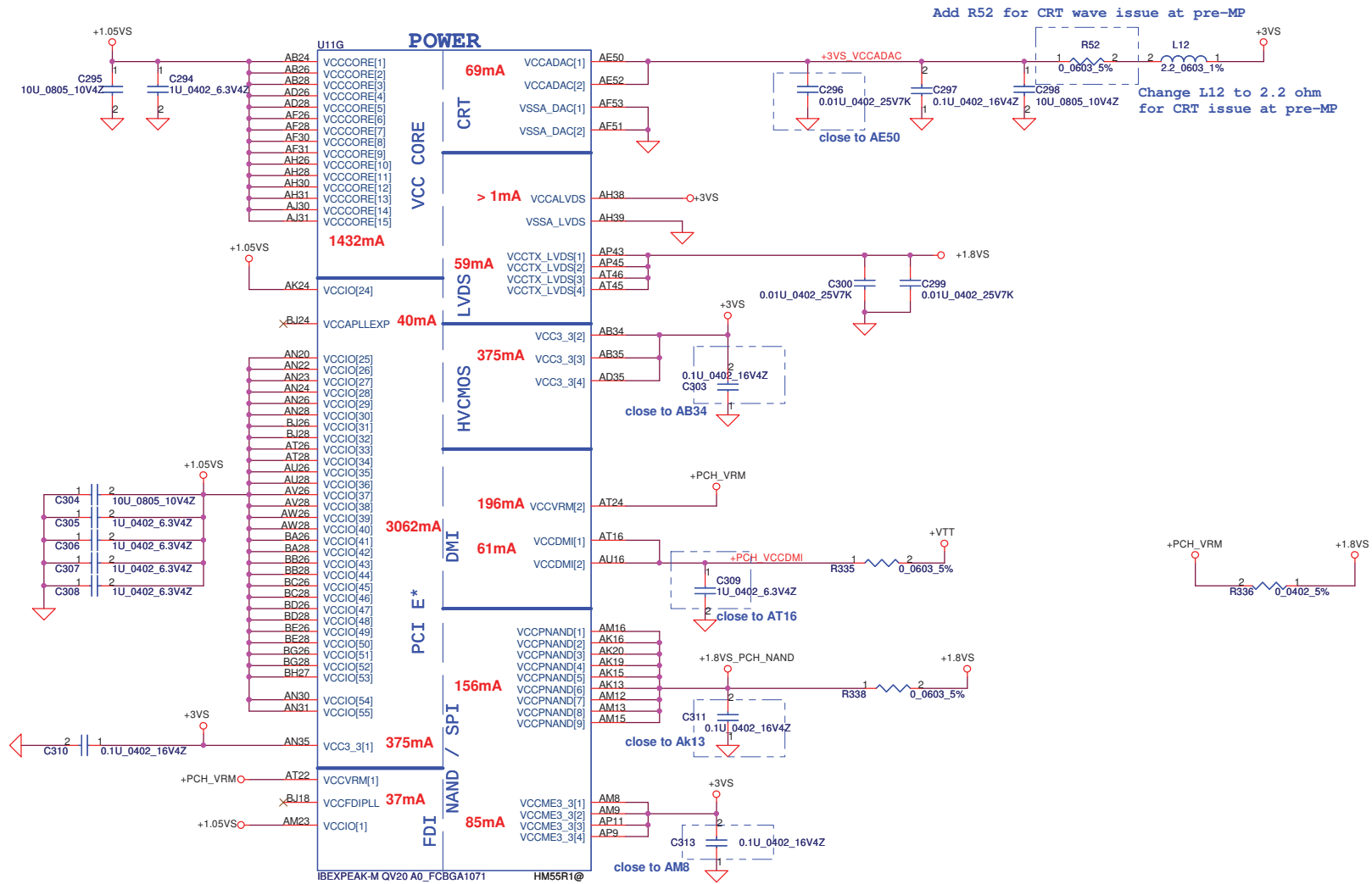
On-Die PLL VR

PCH_GPIO27 High = Enabled (Default)
Low = Disabled

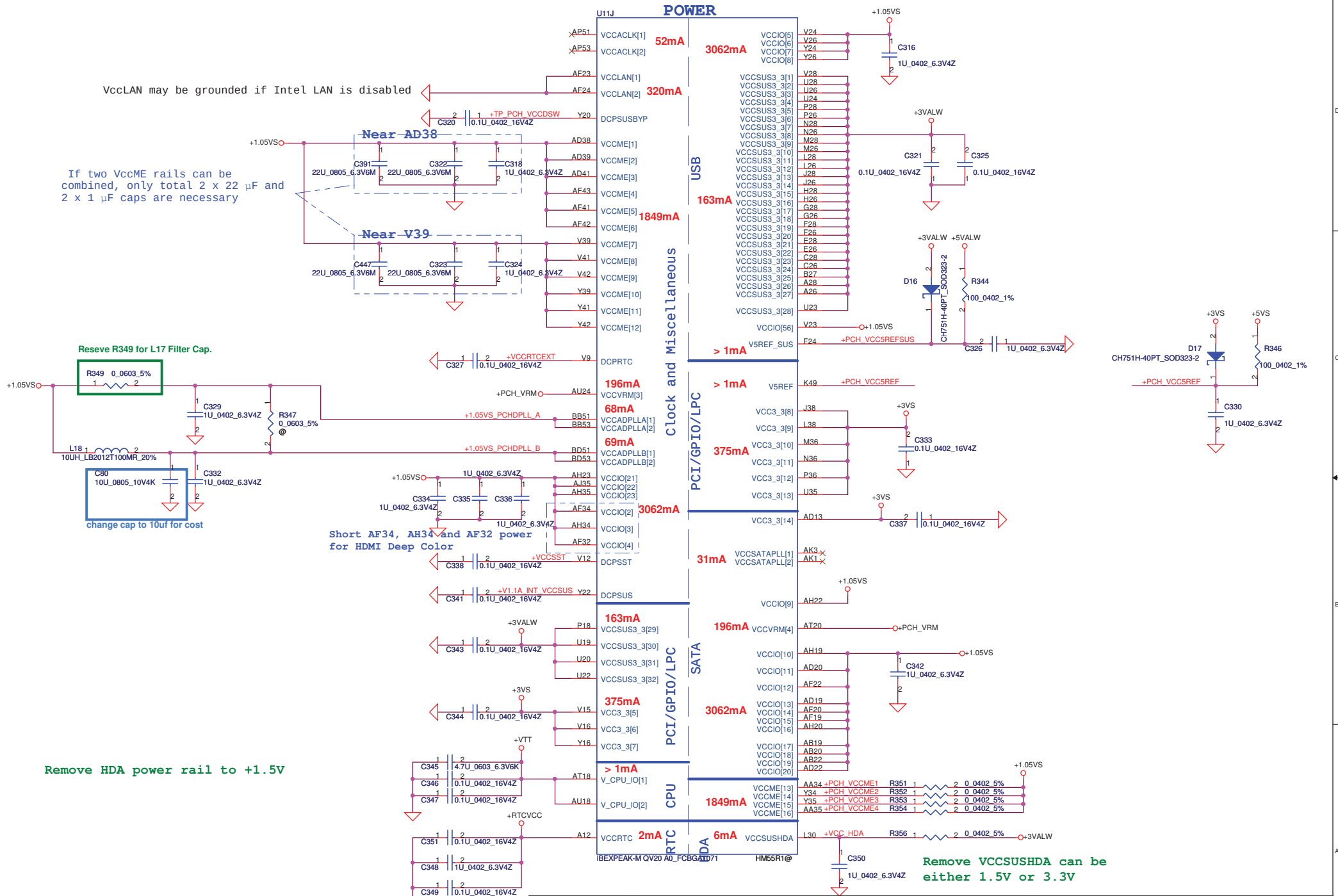
PROJECT_ID		
Name	ID0	ID1
NBQAA 11.6/13.3"	L	L
NBQAA 14"	L	H
*NWQAA 16"	H	L
NALAA 17.3"	H	H



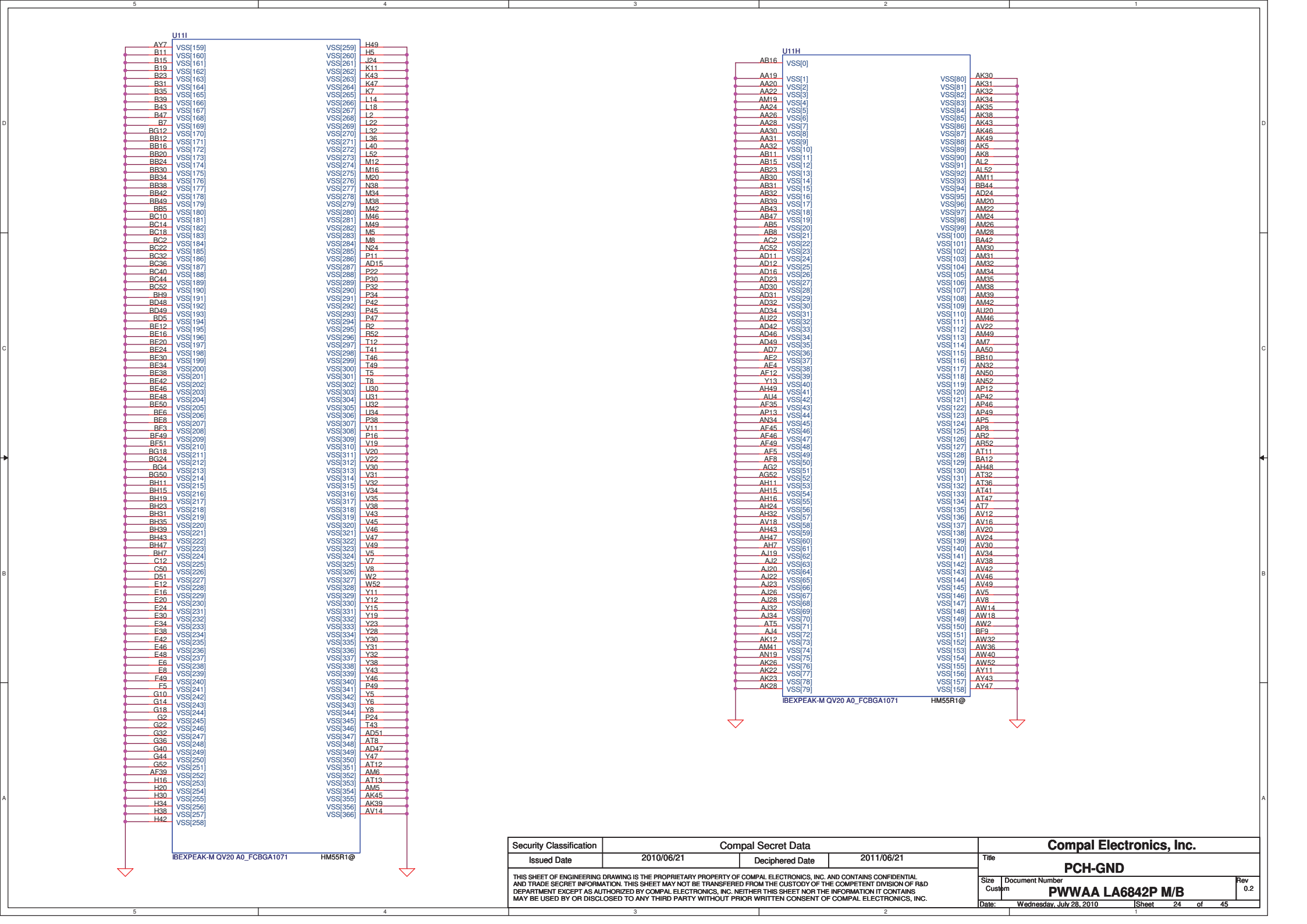
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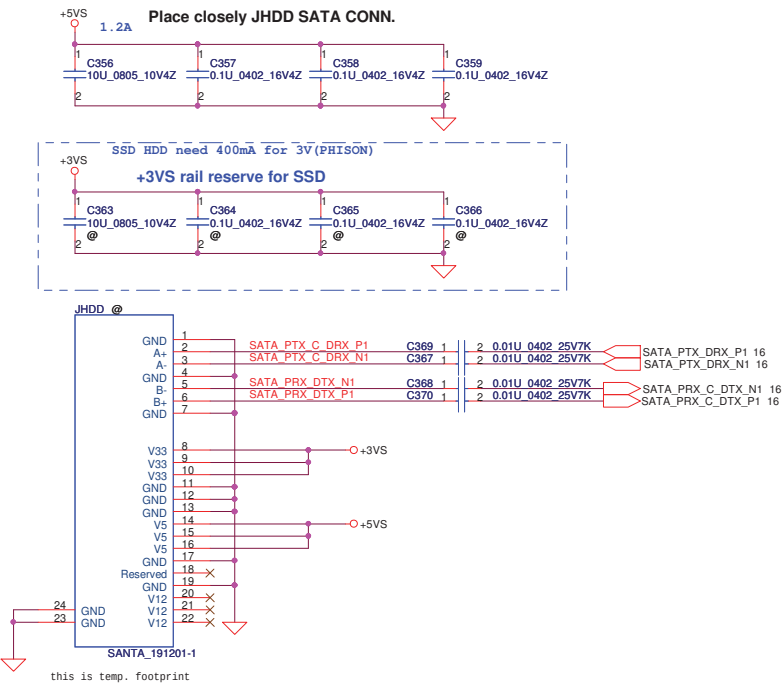
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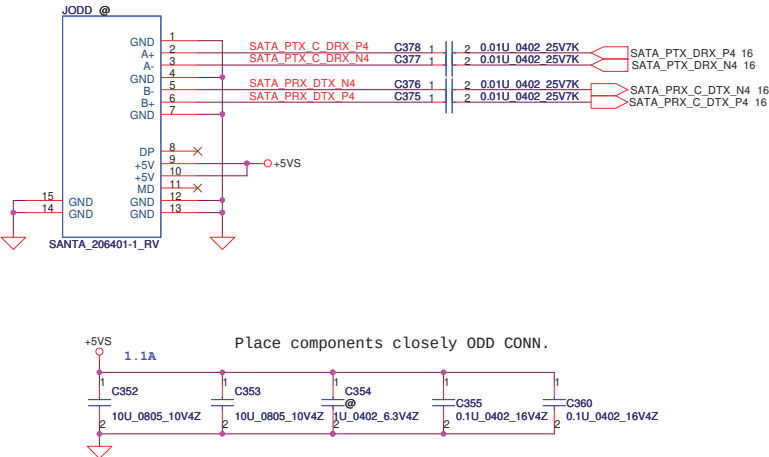
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Issued Date	2010/06/21	Deciphered Date	2011/06/21	Title	
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Custom		PWWAA LA6842P M/B		0.2	
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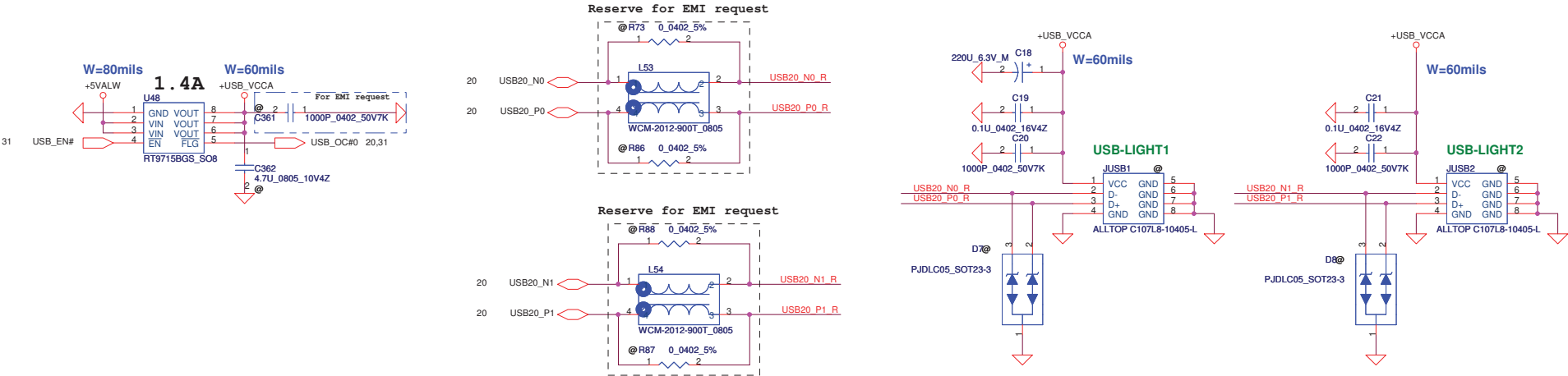
SATA HDD Conn.



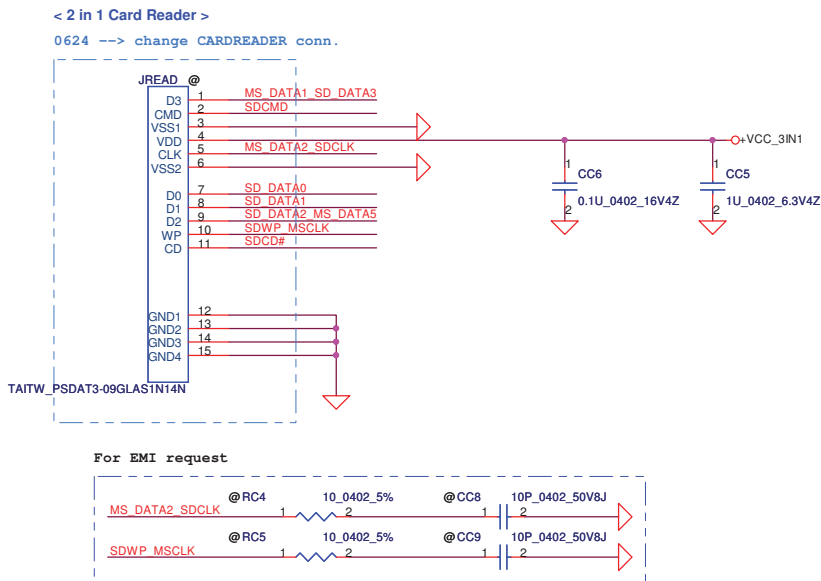
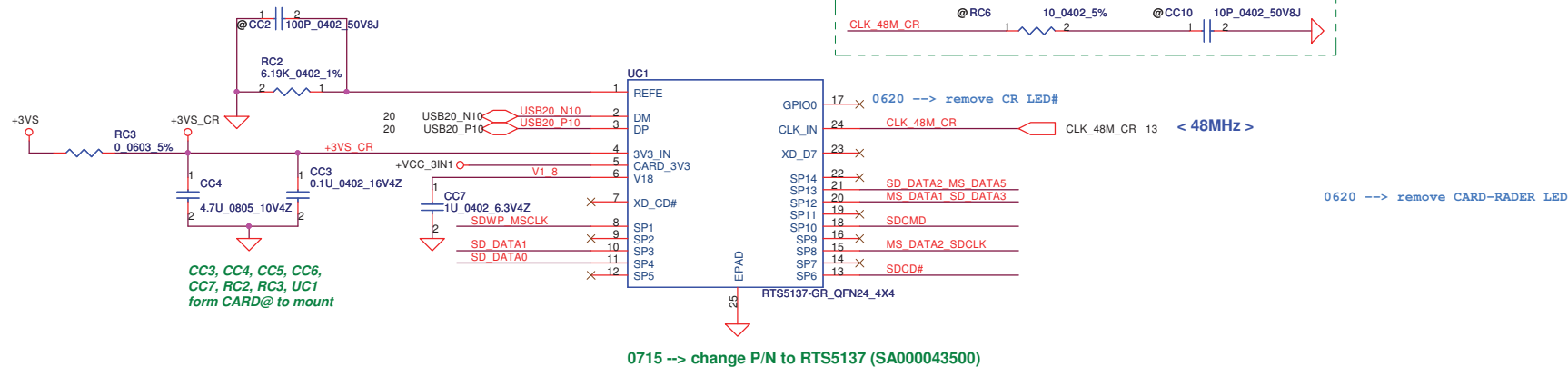
SATA ODD Conn



USB Conn. (2 Port)



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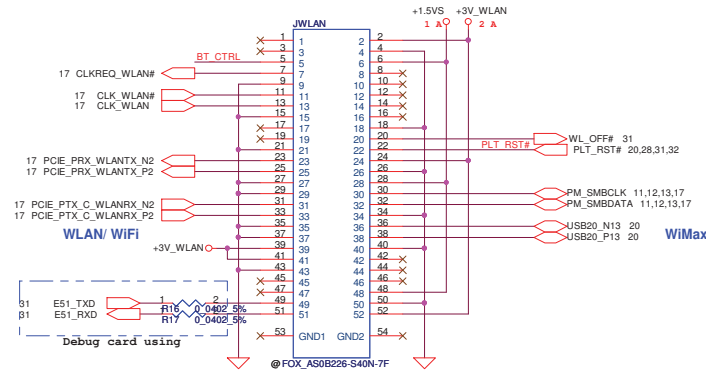
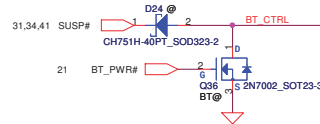
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PCle Mini Card-WLAN/WiMax

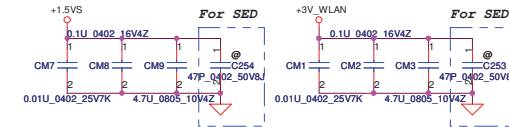
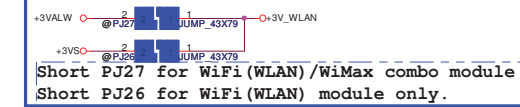
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	HI	LO
BT_PWR#	LO	HI

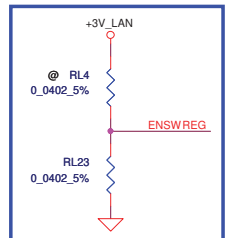
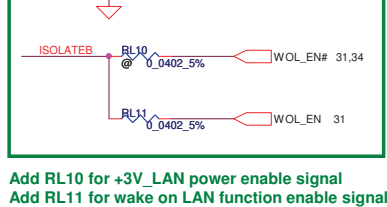
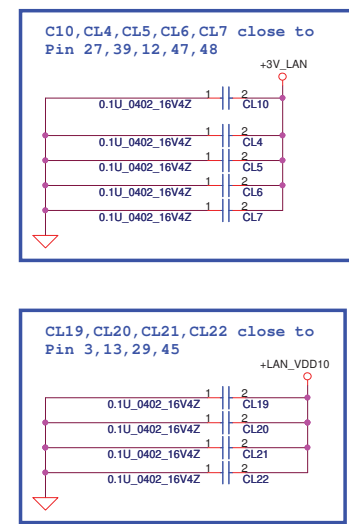
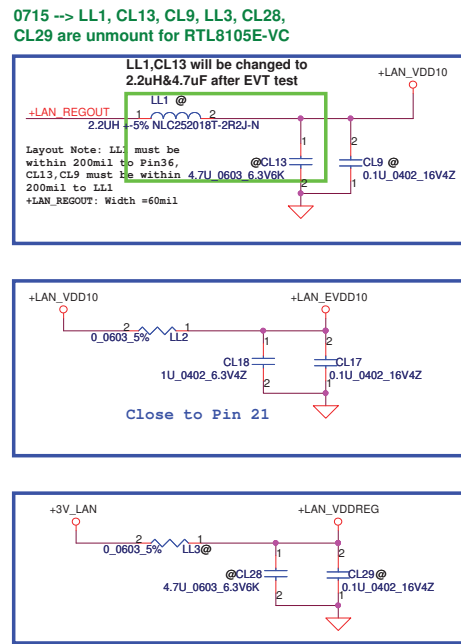
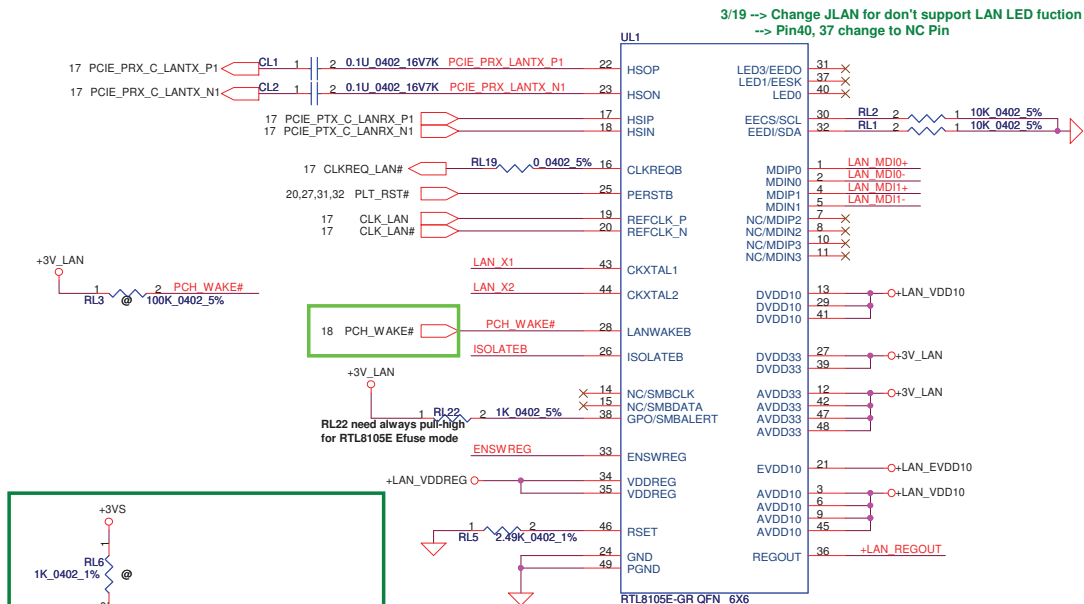
**If +3V_WLAN is +3VS, please
remove D24.



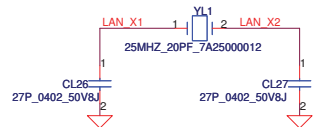
Slot#1 Half PCIe Mini Card-WLAN/WiMax



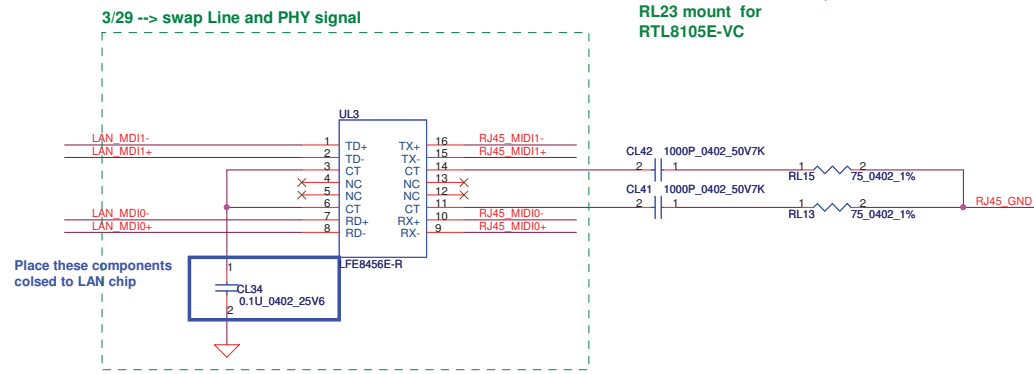
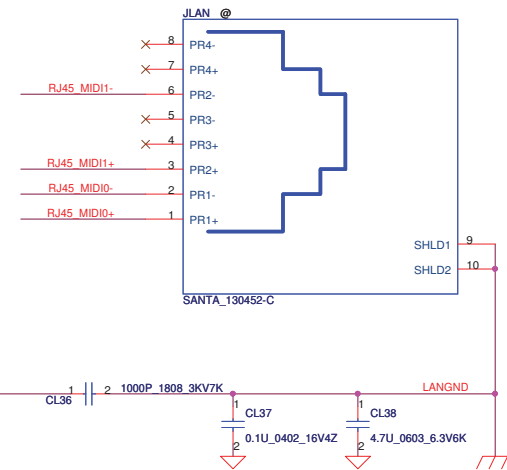
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4/2-->remove RL8, RL9, CL11

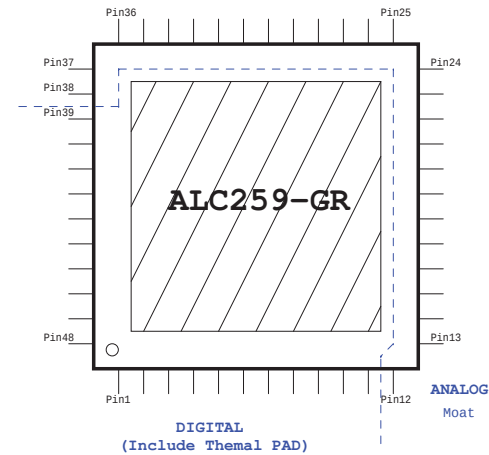
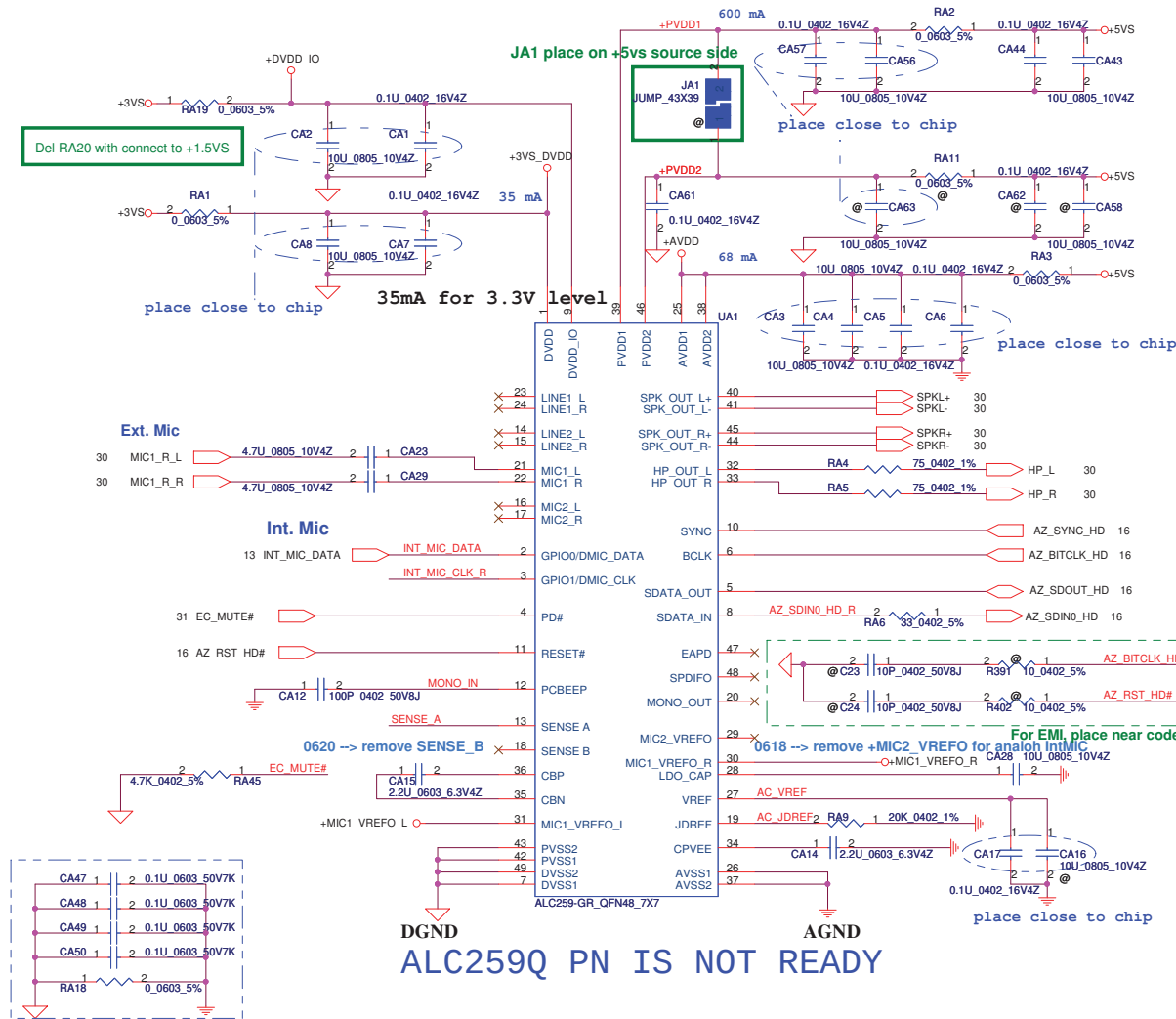


LAN Conn.



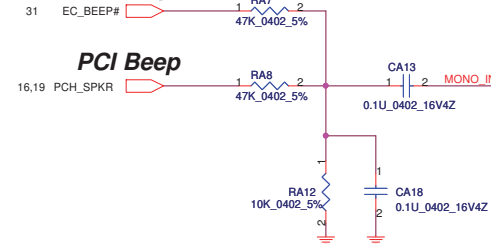
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RTL8105E 10/100 LAN				
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Codec

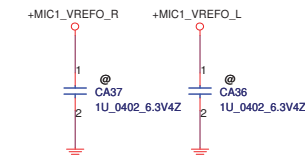


Beep sound

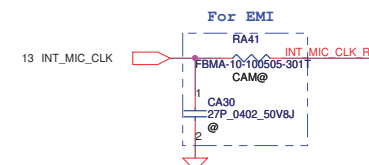
EC Beep



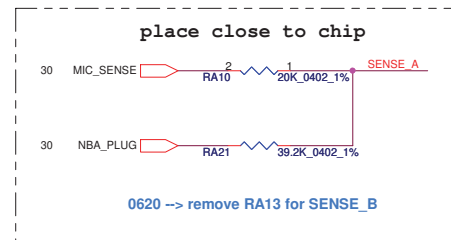
Place close to chip



0618 --> remove +MIC2_VREF0 for analog IntMIC

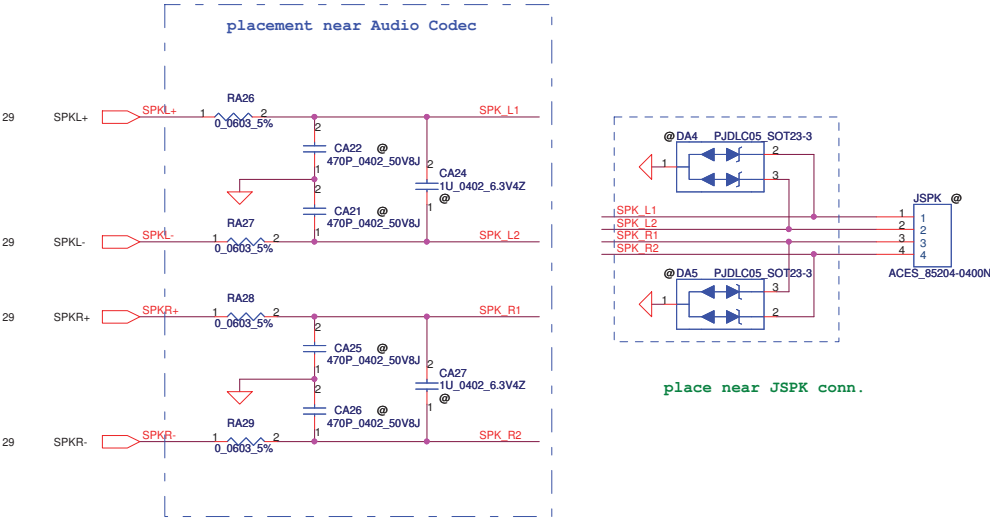


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
	39.2K	PORT-E (PIN 14, 15)	

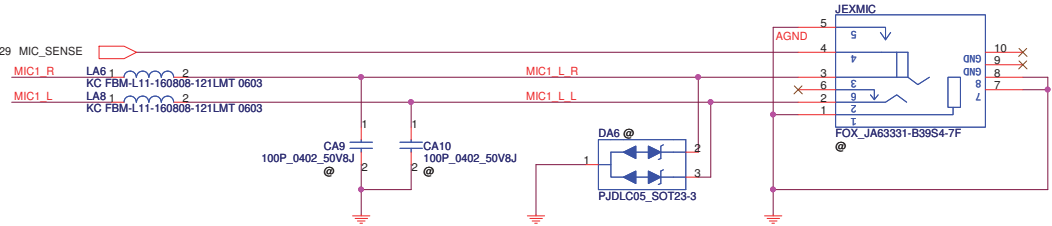


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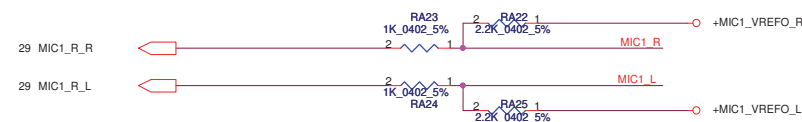
Speaker Connector



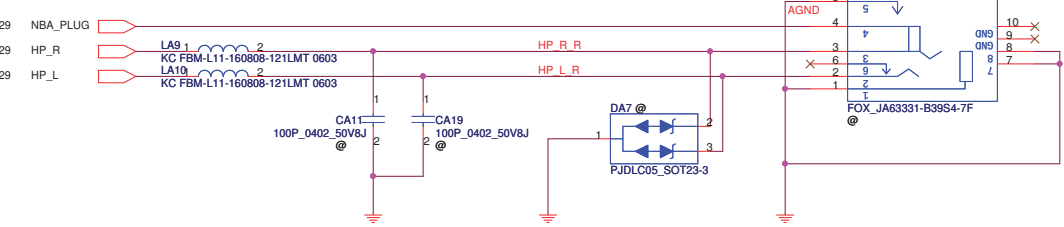
Ex.MIC JACK



Ext.MIC/LINE IN



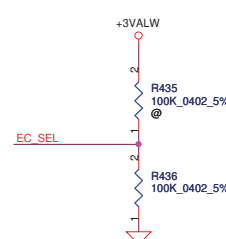
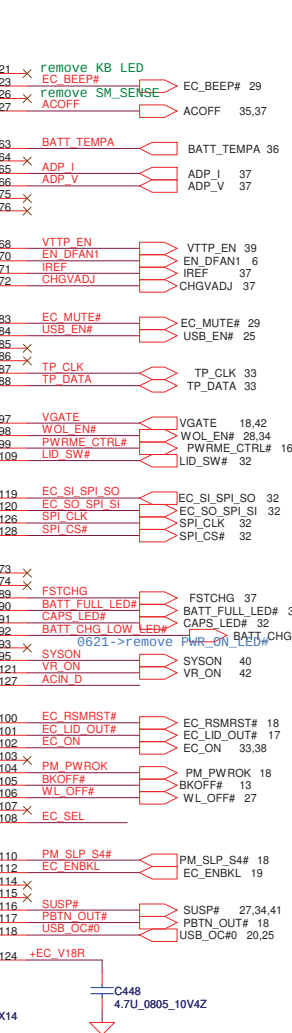
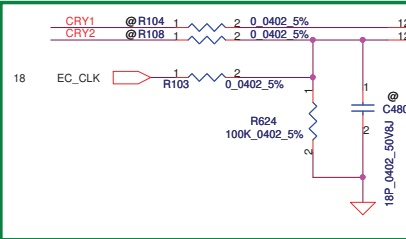
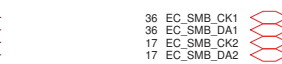
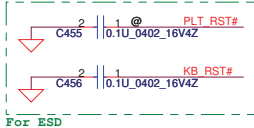
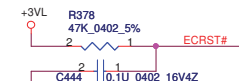
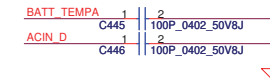
Head Phone JACK



Int. Mic

0618 --> remove Analog IntMIC, and change to DIGITAL MIC

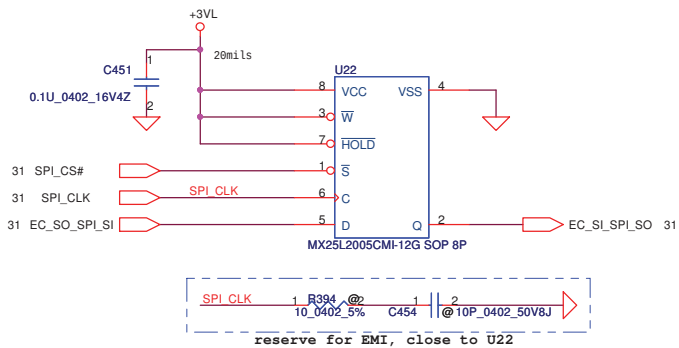
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Issued Date	2010/06/21	Deciphered Date	2011/06/21	Title	
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Size	Document Number	PWWAA LA6842P M/B			Rev
					0.2
Date: Wednesday, July 28, 2010		Sheet		30 of 45	



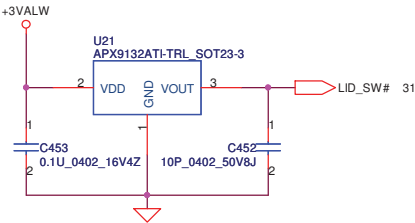
EC SEL	EC Version
High	KB926D3
Low	KB926E0

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					PWWAA LA6842P M/B	0.2	
				Date:	Wednesday, July 28, 2010	Sheet 31 of 45	

SPI Flash (256KB)

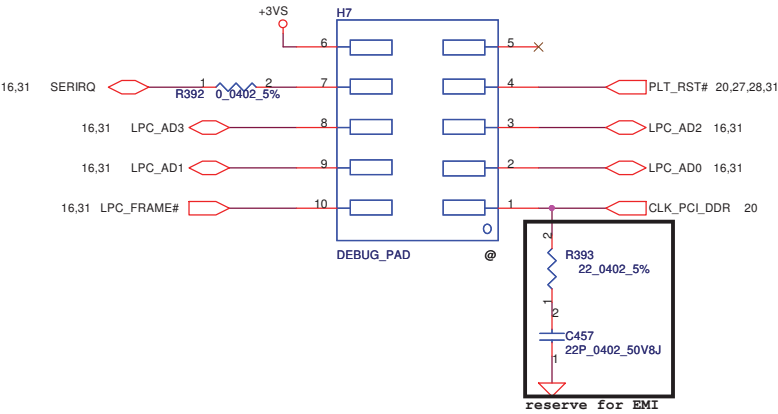


Lid SW



LPC Debug Port

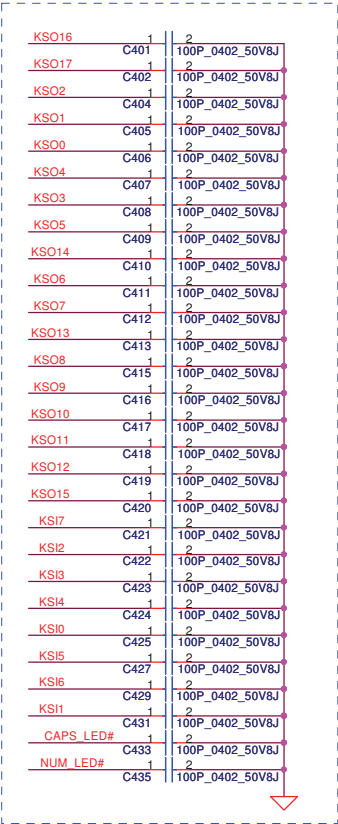
Please place the PAD under DDR DIMM.



KEYBOARD CONN.

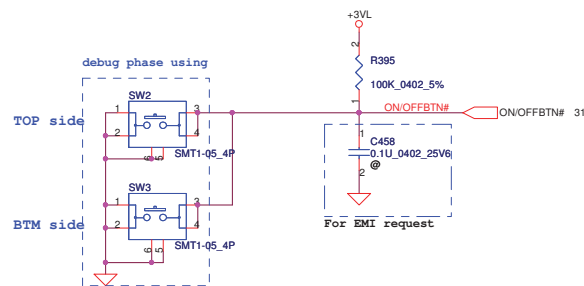


please close to JKB

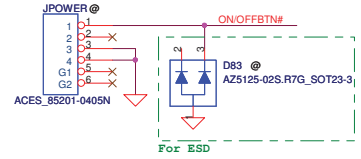


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Size		Document Number		PWWAA LA6842P M/B		Rev 0.2
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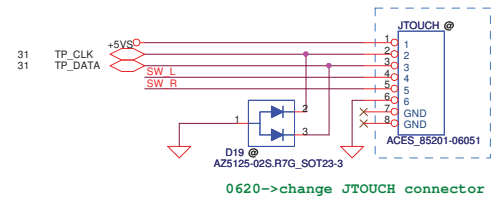
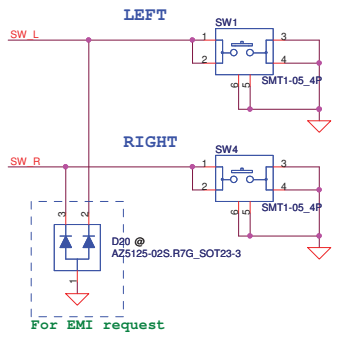
Power Button



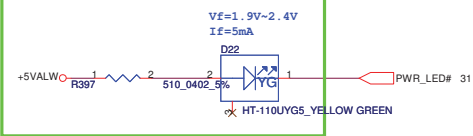
PWR/B to MB Conn.



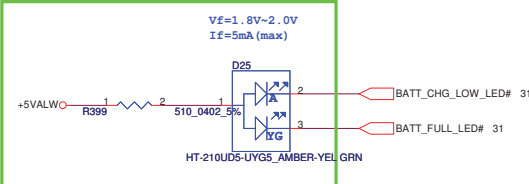
TP Button/Conn.



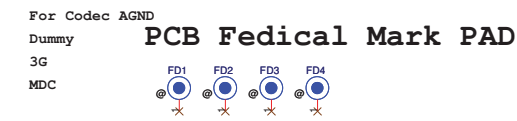
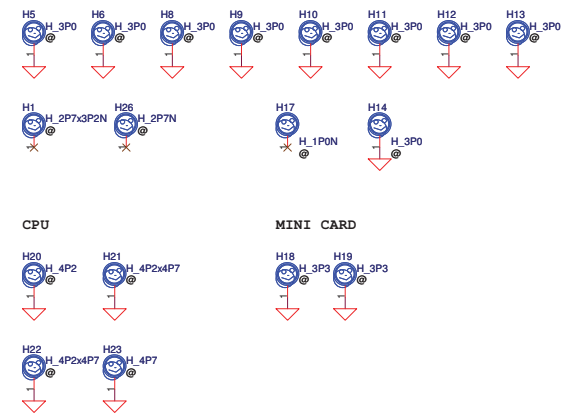
POWER/SUSPEND LED



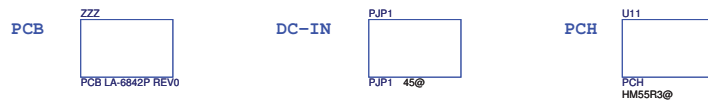
BATT CHARGE/FULL LED



Screw Hole

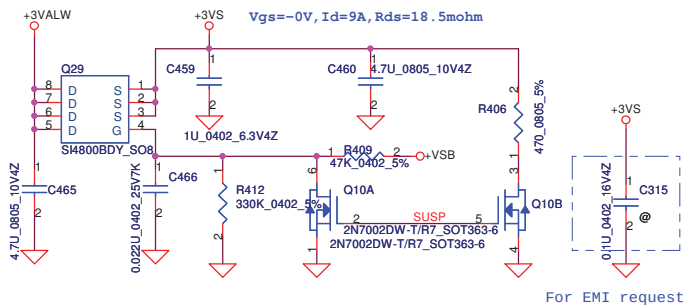


ISPD

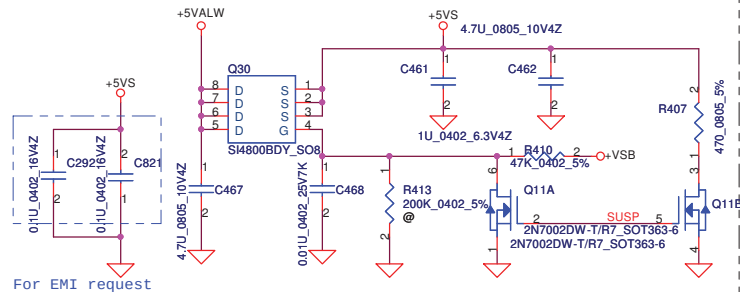


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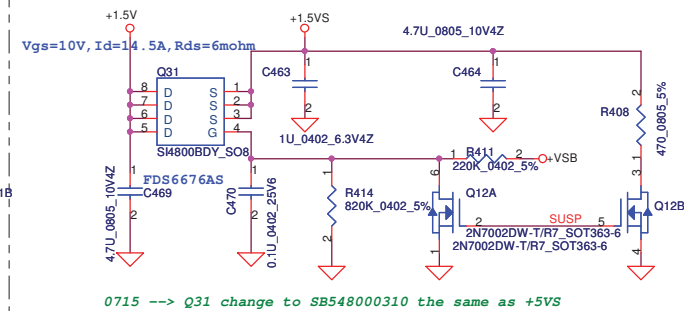
+3VALW TO +3VS



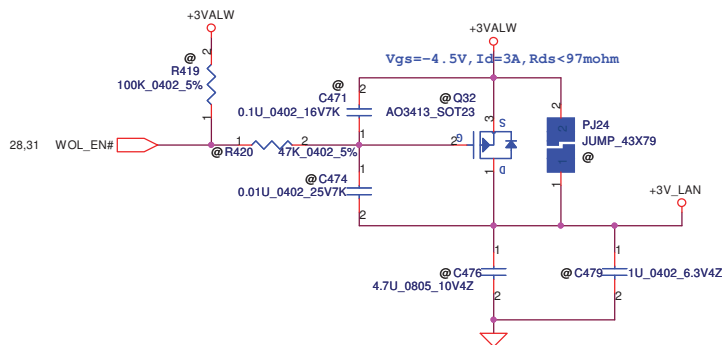
+5VALW TO +5VS



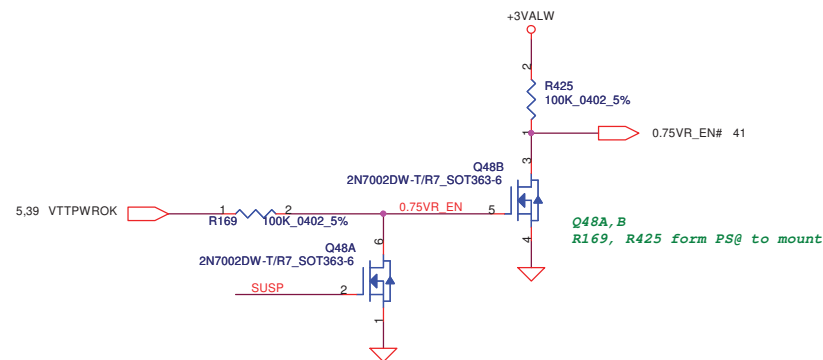
+1.5V to +1.5VS



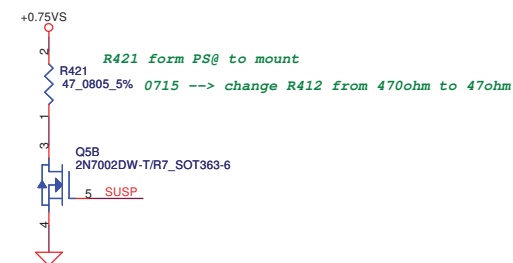
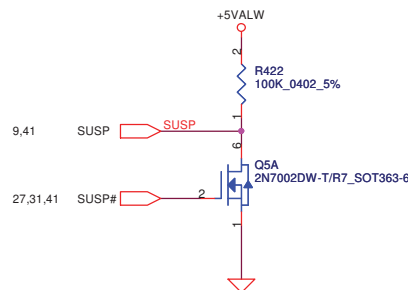
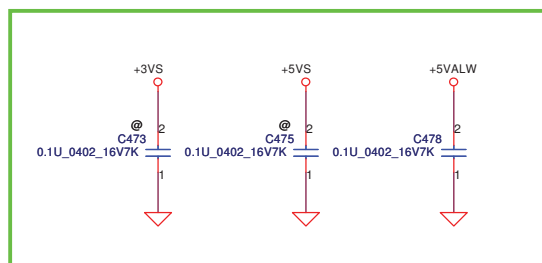
+3VALW TO +3V_LAN



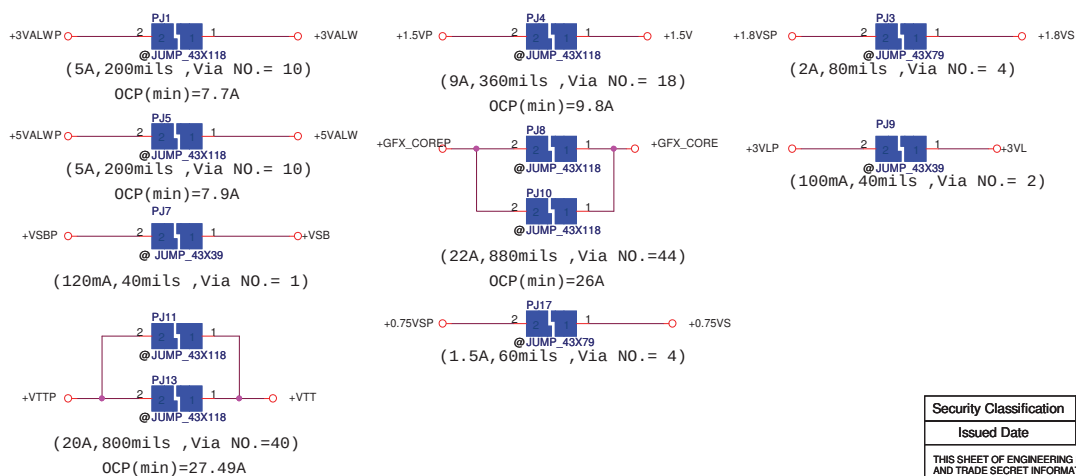
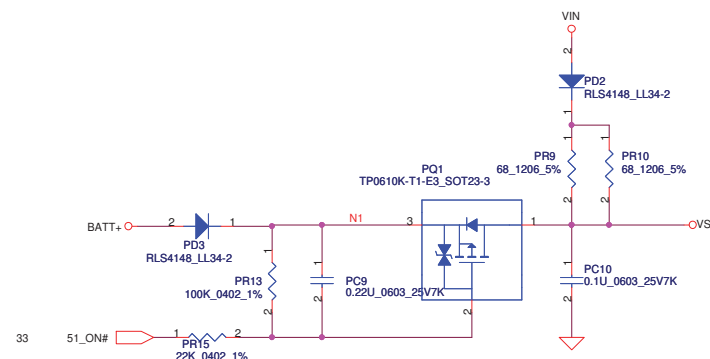
For S3 CPU Power Saving



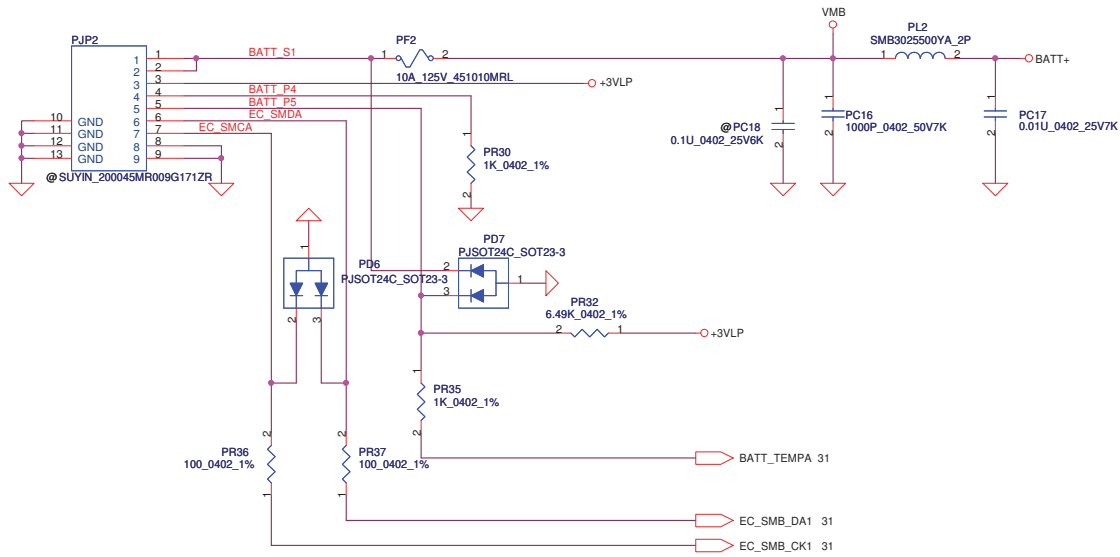
Reserve for EMI test



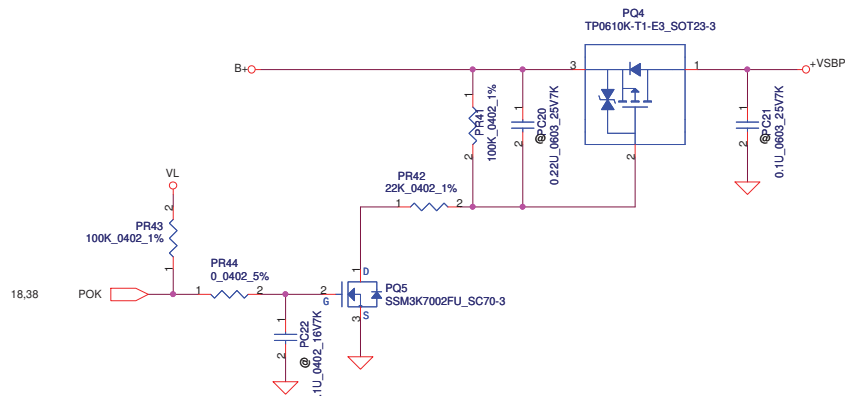
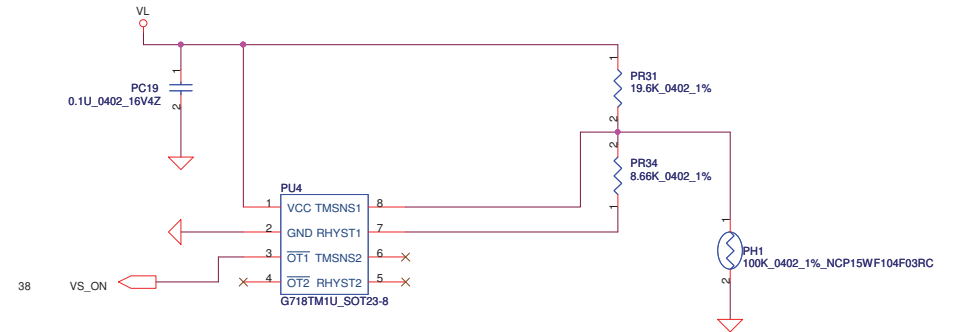
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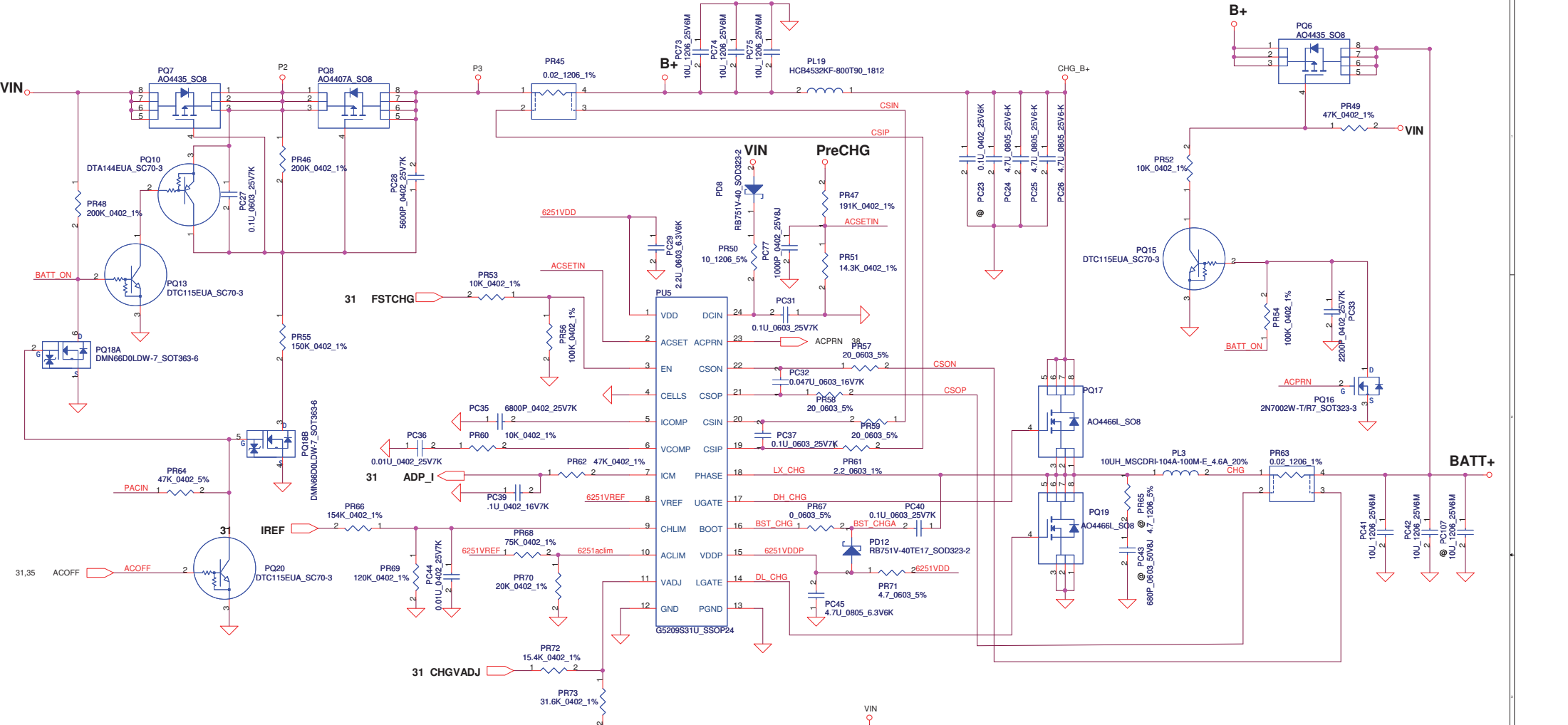
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PH1 under CPU botten side :
CPU thermal protection at 95degree C
Recovery at 56 degree C



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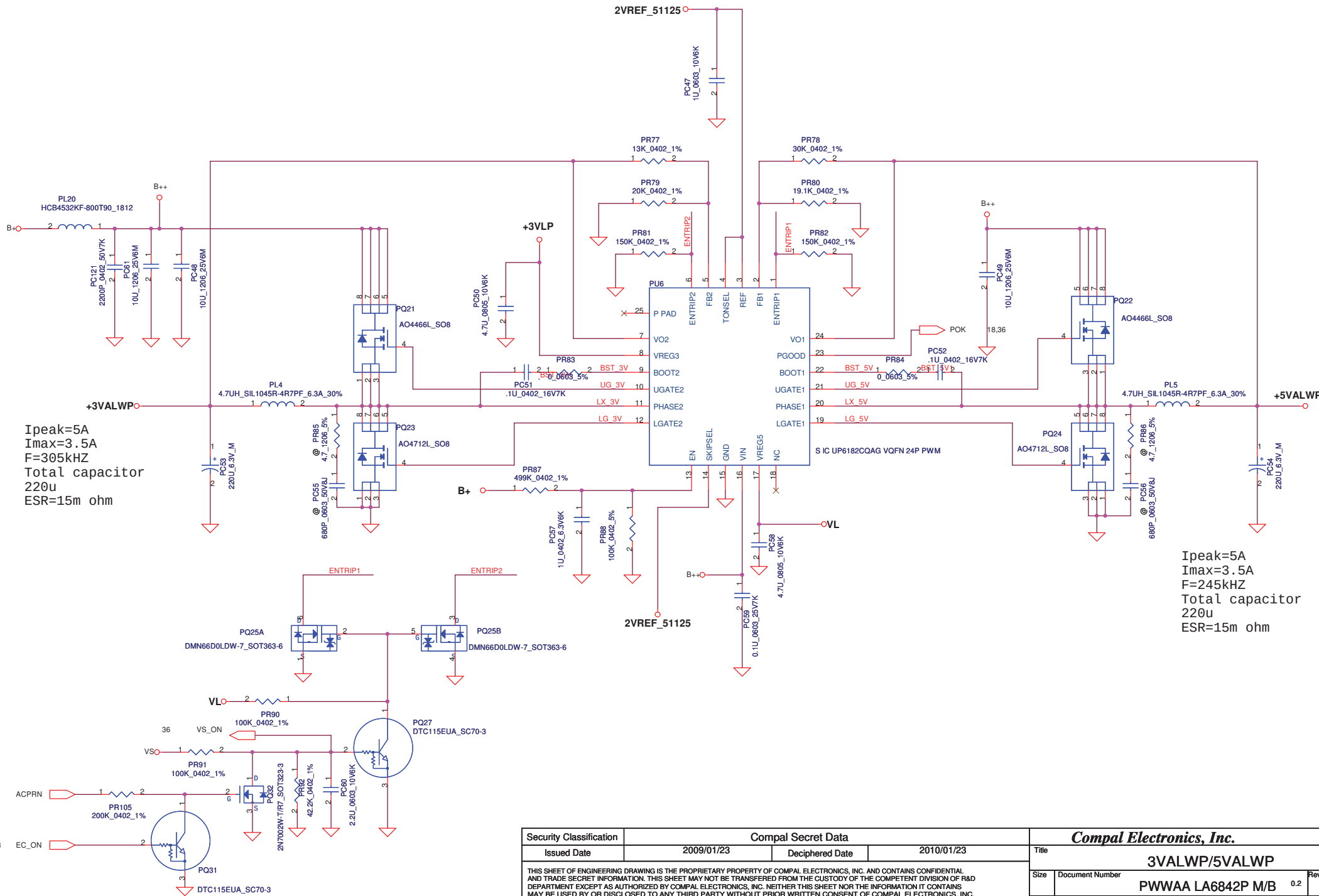


CP mode
 $I_{ada}=0\sim3.42A(65W)$ $CP=92\%*I_{ada}$; $CP=3.147A$
 $V_{aclim}=1.08V(65W)$ $PR68=75k$ $PR45=0.02$

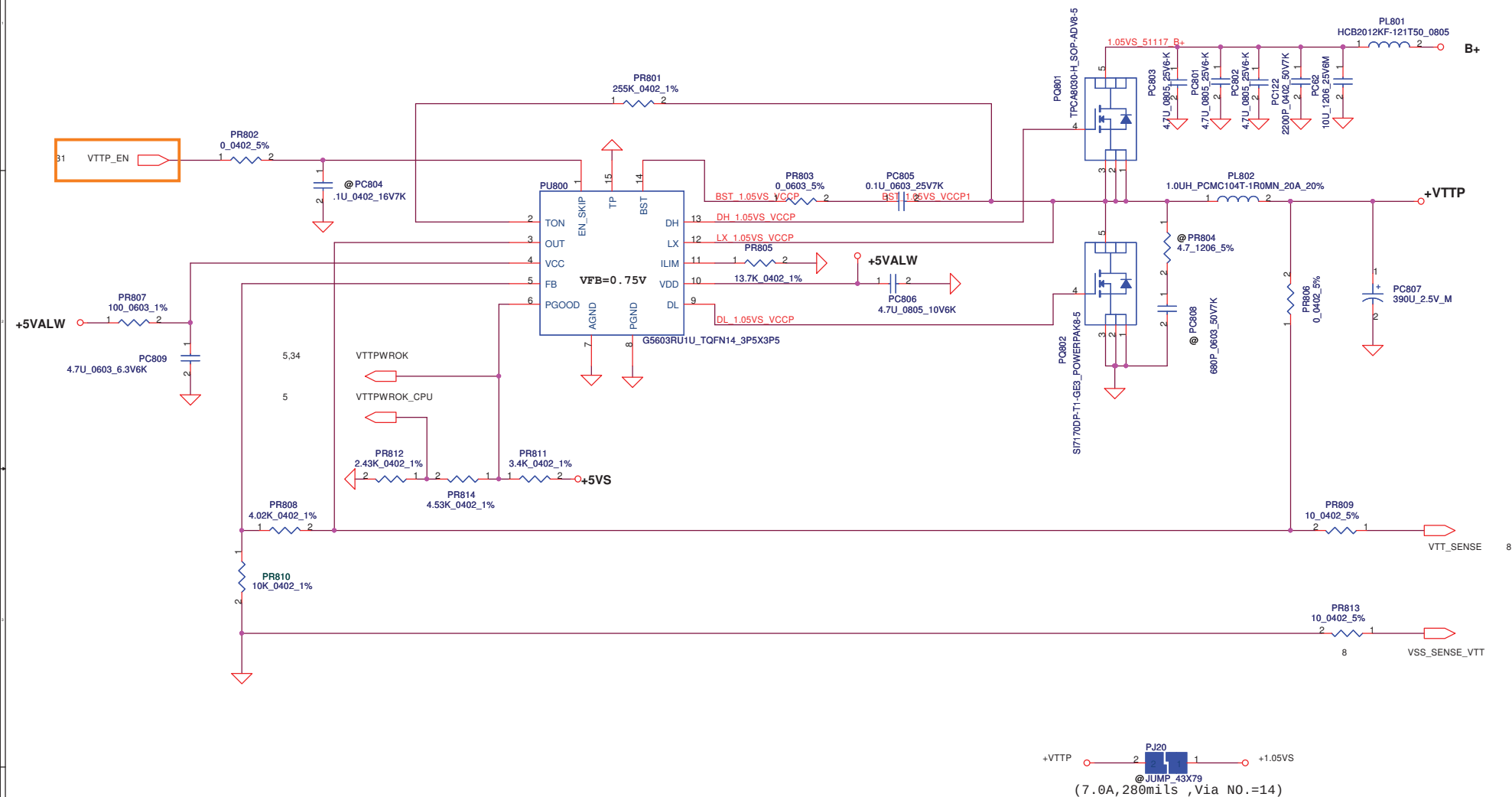
$CC=0.25A\sim3A$
 $I_{REF}=1.016*I_{charge}$
 $I_{REF}=0.254V\sim3.048V$
 V_{CHLIM} need over 95mV

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

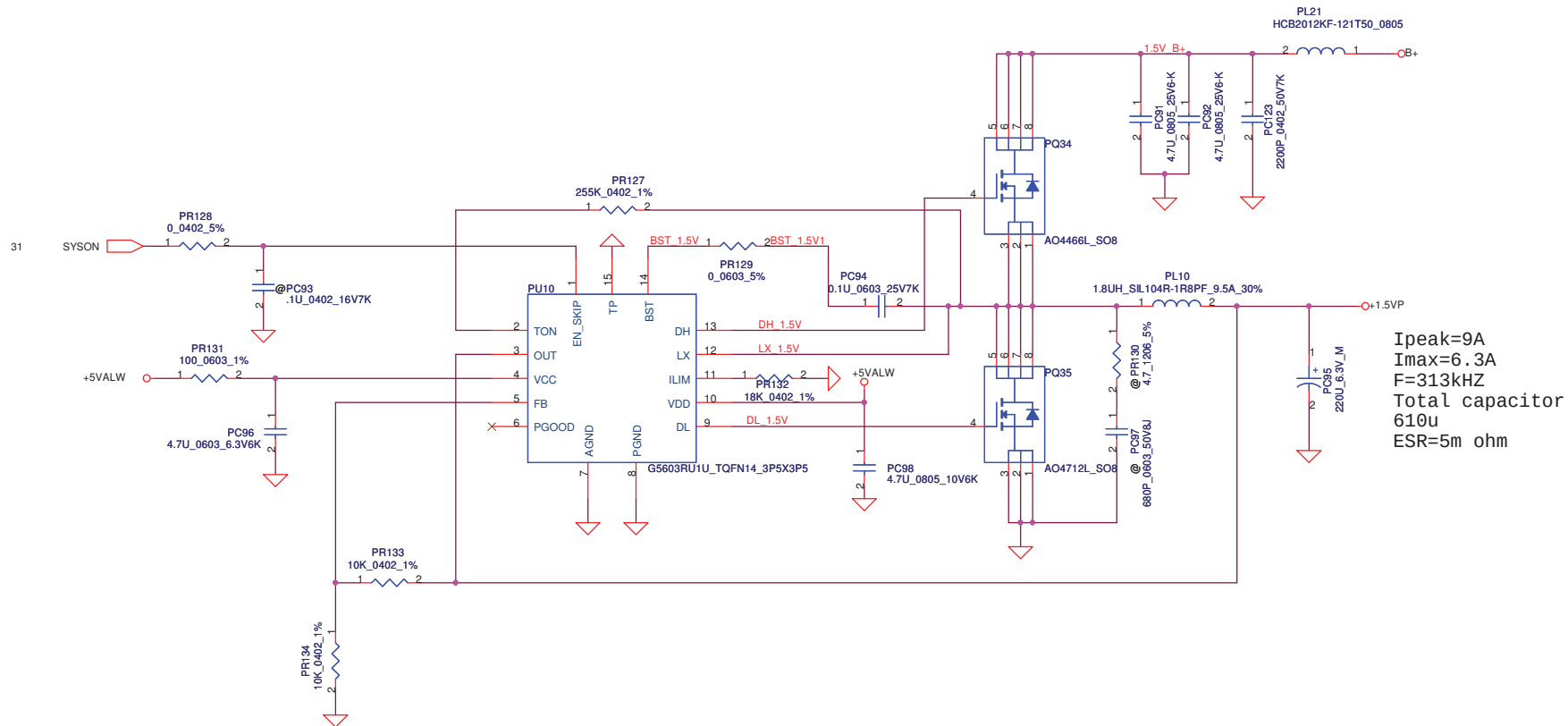
Vin Detector
High 18.089V
Low 17.44V



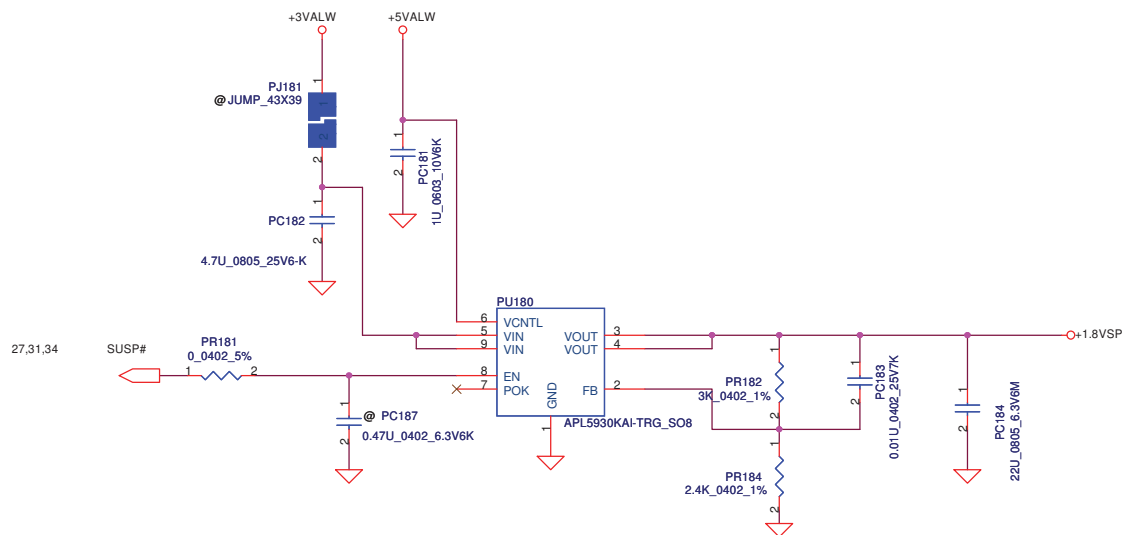
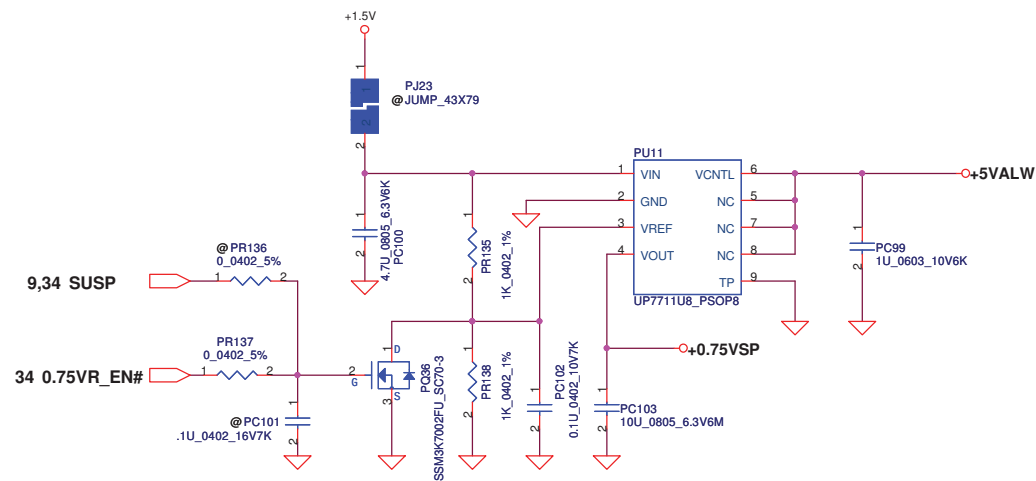
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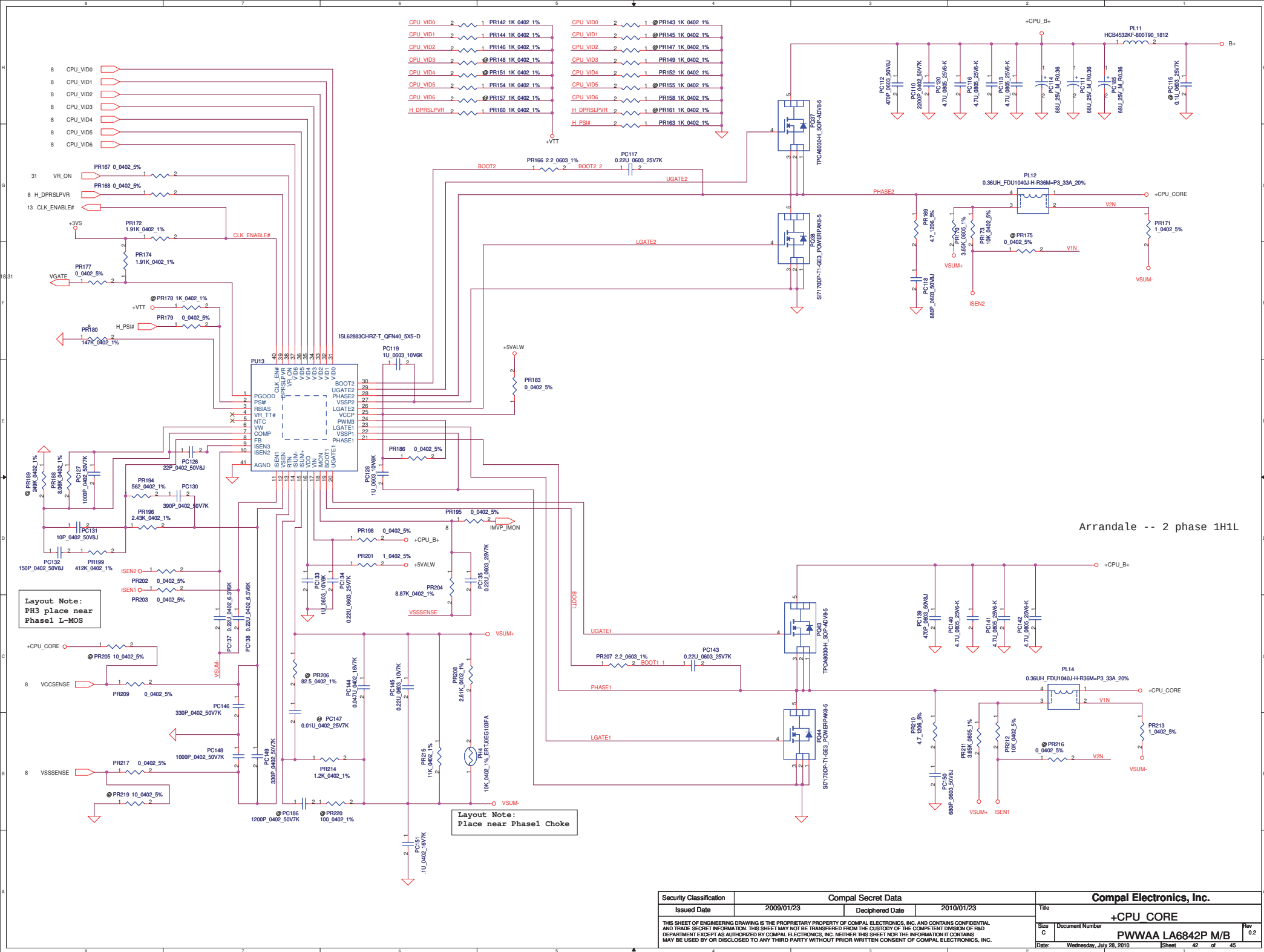


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										0.75VSP/+1.8VSP	
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Arrandale -- 2 phase 1H1L

Layout Note:
PH3 place near
Phasel L-MOS

Layout Note:
Place near Phasel Choke

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
2010/07/13	42		Change PL12,PL14 to SH00000IN00	BOM modify
2010/07/13	43		Change PL16 to SH00000IN00	BOM modify
2010/07/23	36		Change PC19 to SE070104Z80	BOM modify
2010/07/26	36		Add PD6,PD7	EMI request
2010/07/26	37		Add PC73,PC74,PC75(10U_1206)	EMI request
2010/07/26	38		Add PC121(2200P_0402),PC61(10U_1206)	EMI request
2010/07/26	39		Add PC122(2200P_0402),PC62(10U_1206)	EMI request
2010/07/26	40		Add PC123(2200P_0402)	EMI request

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PIR (Product Improve Record)

PWWAA LA-6842P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2
GERBER-OUT DATE: 2010/07/31

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE

1.	20100714	Page13	--> add 10u Cap to +1.5VS_CK505	For eSATA transmit issue
				----> not add 10u Cap into schematic yet

NWQAA LA-6061P SCHEMATIC CHANGE LIST
REVISION CHANGE: 1.0 TO 2.0
GERBER-OUT DATE: 2010/03/19

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE

1	3/17	29	Change cardreader to JMB385/389	For customer request
2	3/18	31	Remove D86	For ESD request
3	3/18	22	Add R52	For CRT wave issue
4	3/19	22	Change L12 to 2.2 ohm	For CRT wave issue
5	3/22	15	Add D54	For HDMI CEC issue
6	3/24	13	Change C213 to 1U	For NALAA ESATA performance low issue

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		Size	Document Number	Rev	
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