

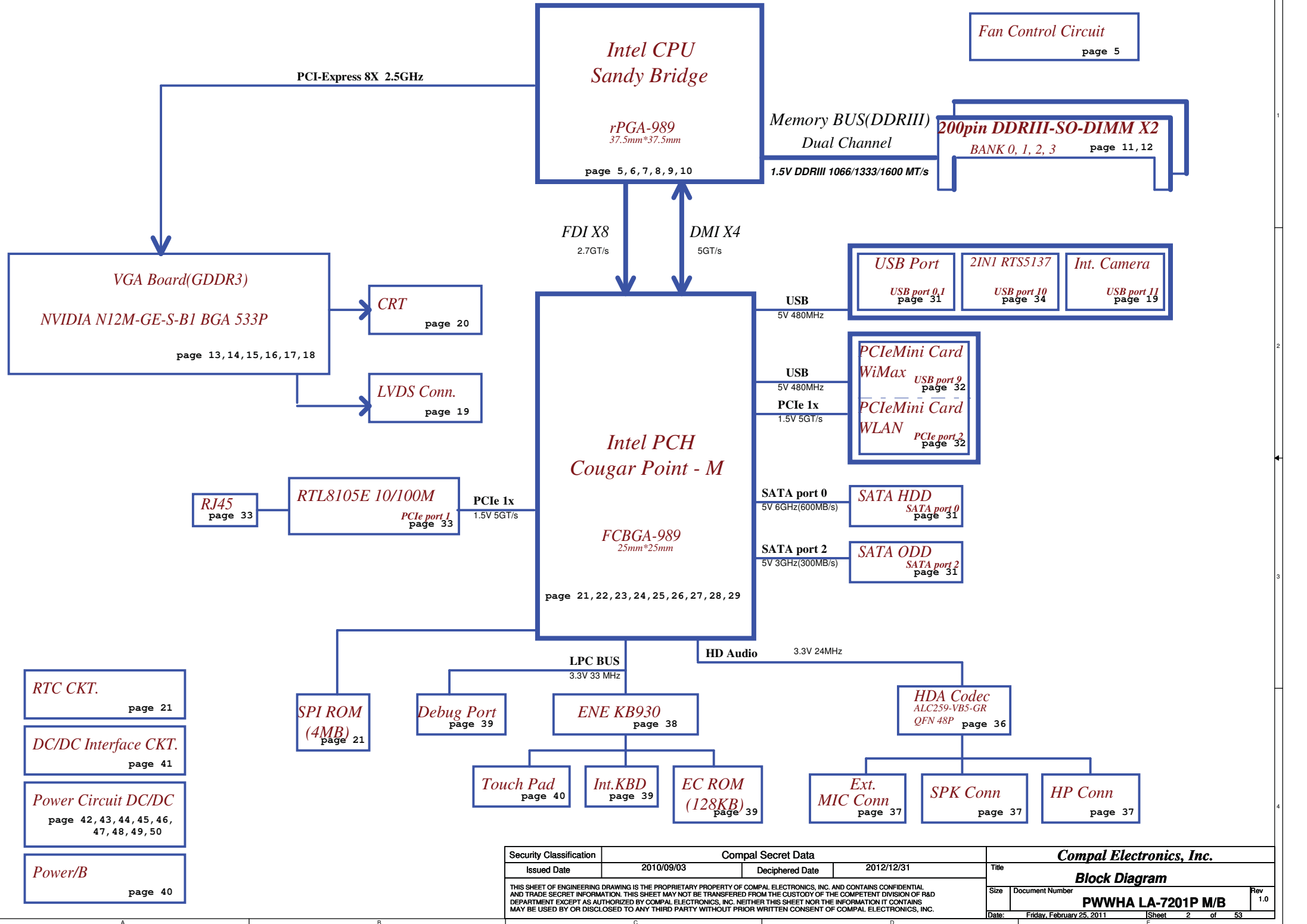
PWWHA

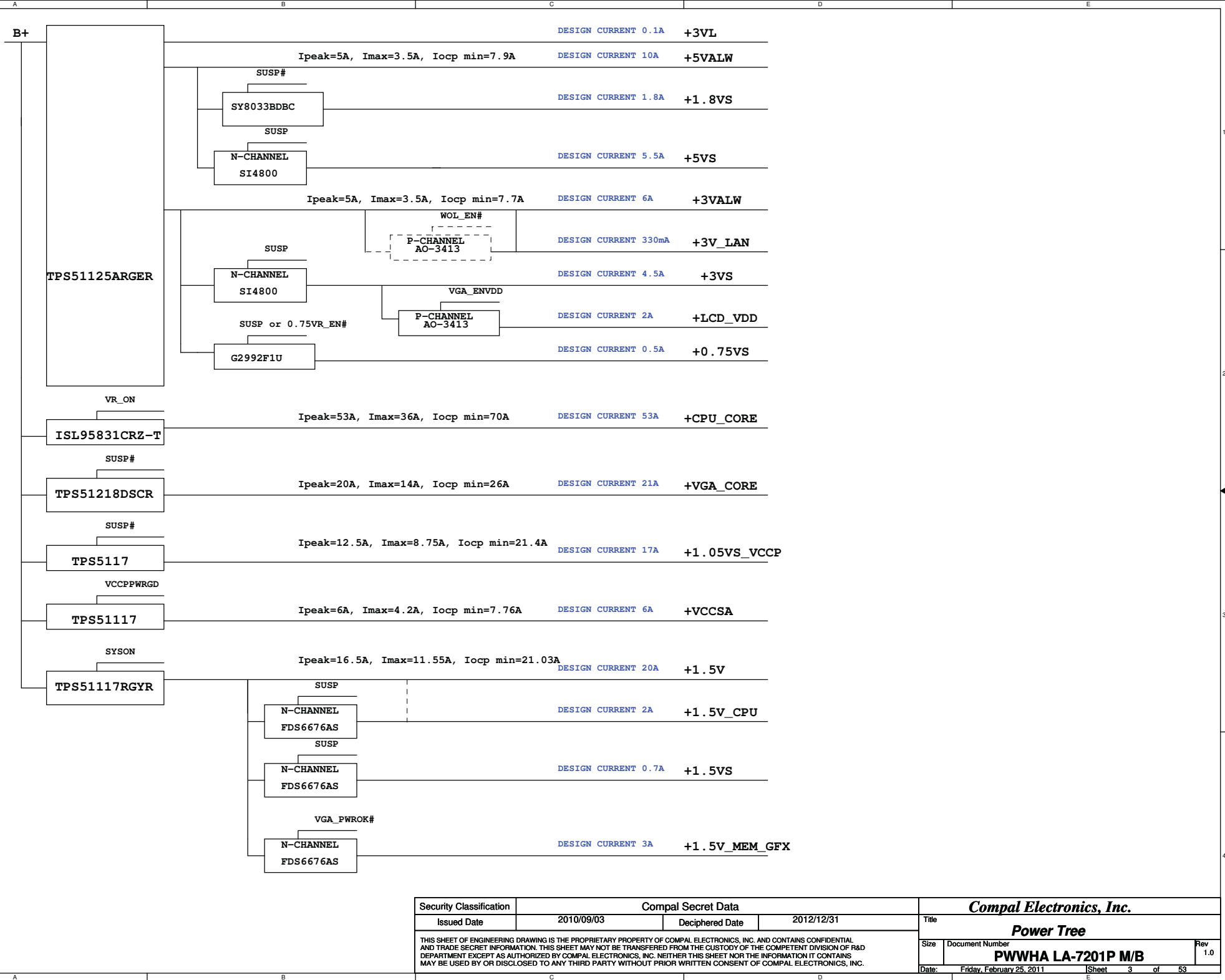
Delhi 10RG

LA-7201P REV 1.0 Schematic

Intel Processor(Sandy Bridge) / PCH(Cougar Point)
2011-01-31 Rev 1.0

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +GFX_CORE
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	WLAN/WIMAX		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b

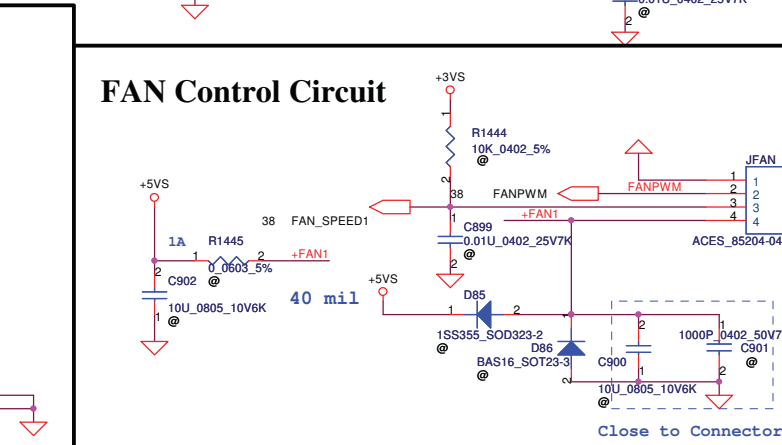
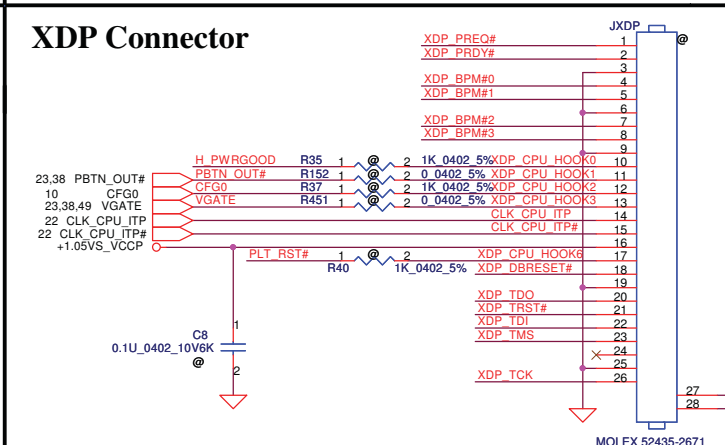
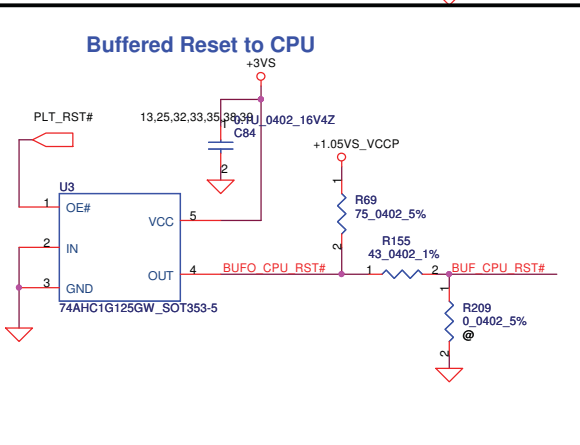
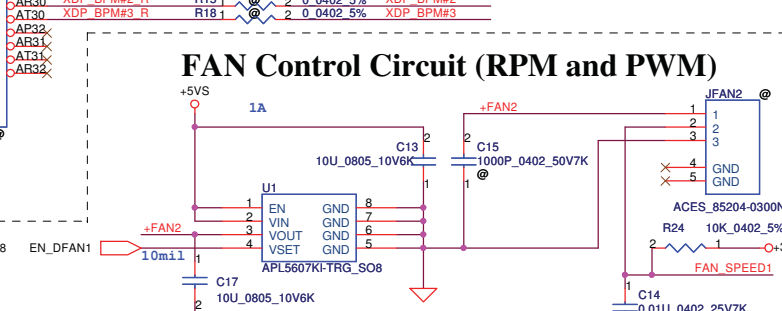
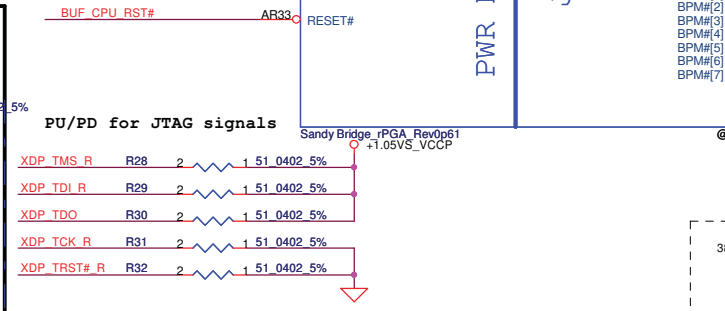
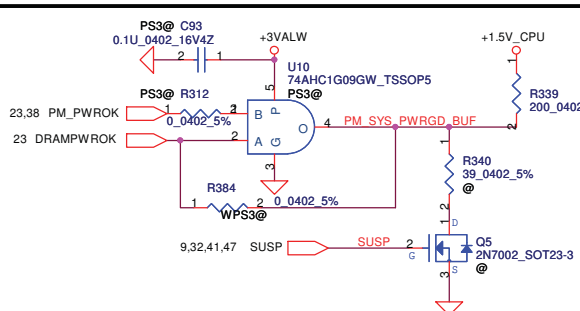
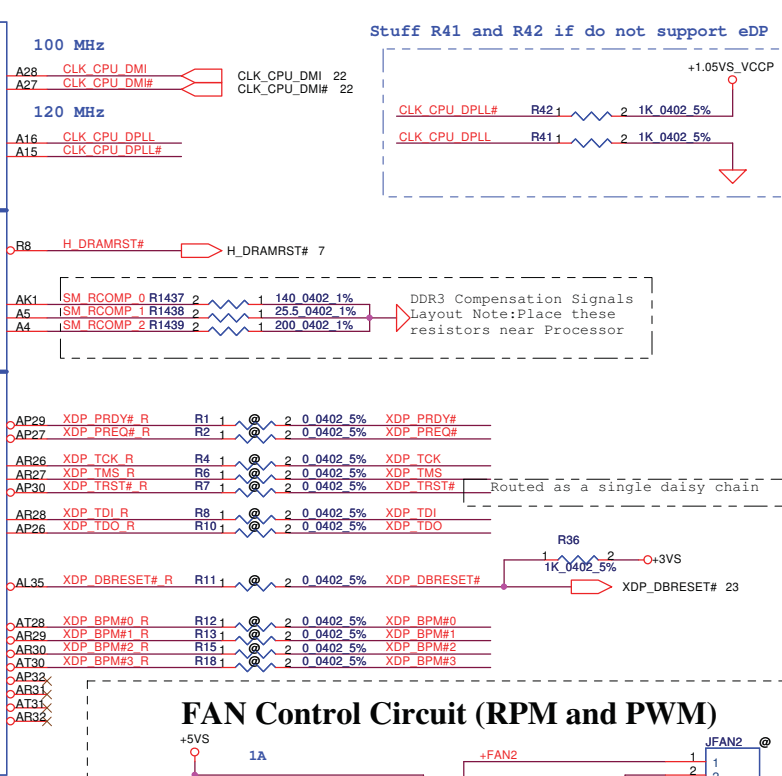
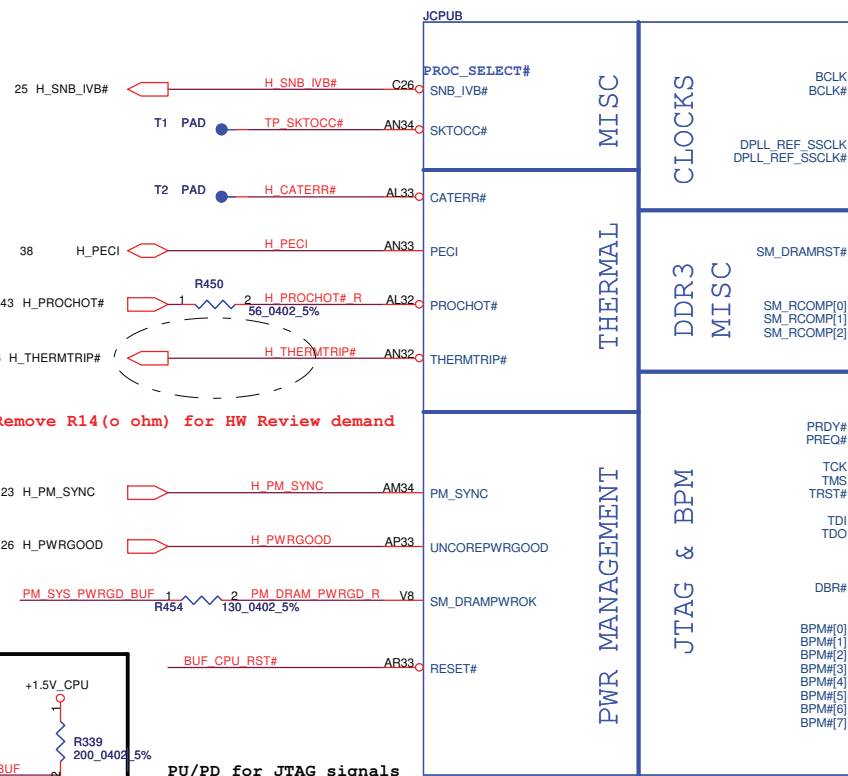
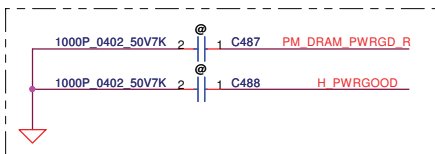
BTO Option Table

Function	DIS only	MINI PCI-E SLOT	LAN			Camera & Mic
description		SLOT1	LAN			Camera & Mic
explain		WIMAX	10/100M	Giga		Camera & Mic
BTO	DIS@	WIMAX@	8105ELDO@	8105ESWR@	8111E@	CAM@

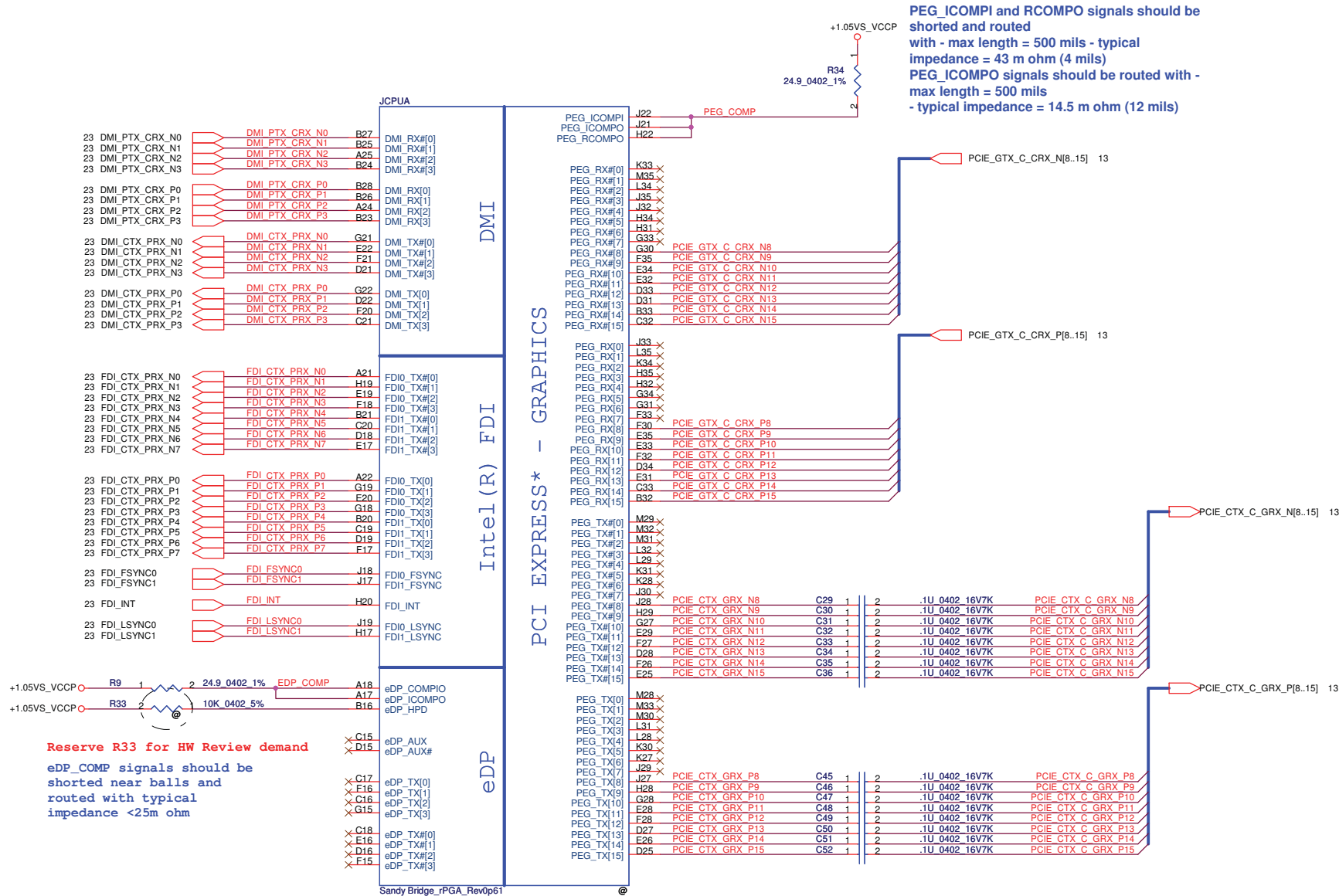
Function	PCH	HDMI/Non-HDMI	EC Chip			Zero ODD
description			930 or 9012			
explain			930	Complete	Simple	
BTO	Q65R3@	HDMI@/NHDMI@	930@	9012@	S9012@	ZODD@

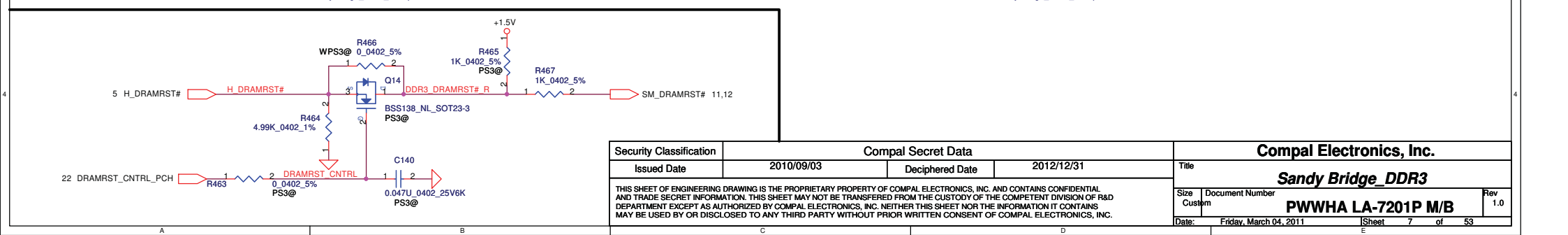
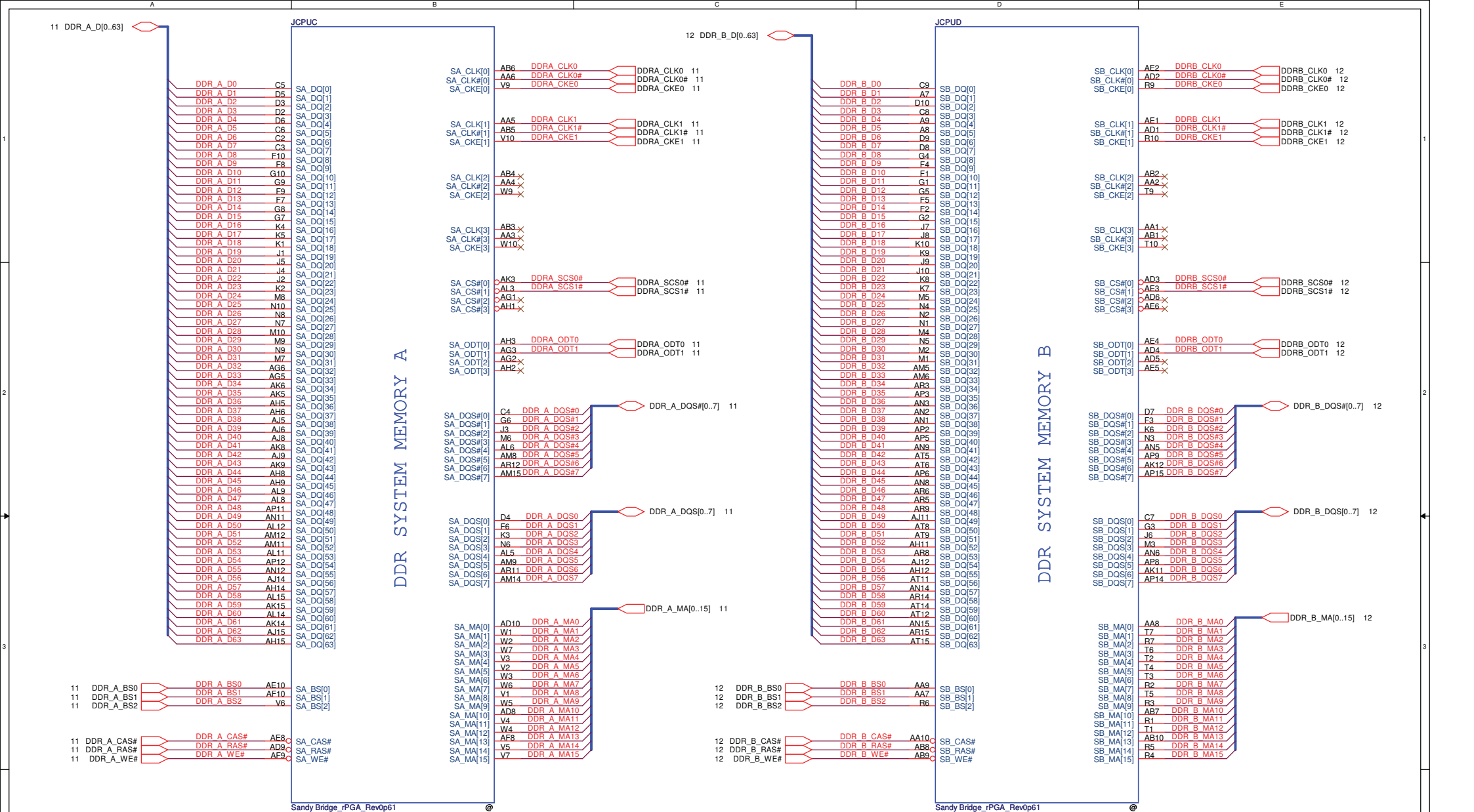
STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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						Size	Document Number		PWWHA LA-7201P M/B		Rev
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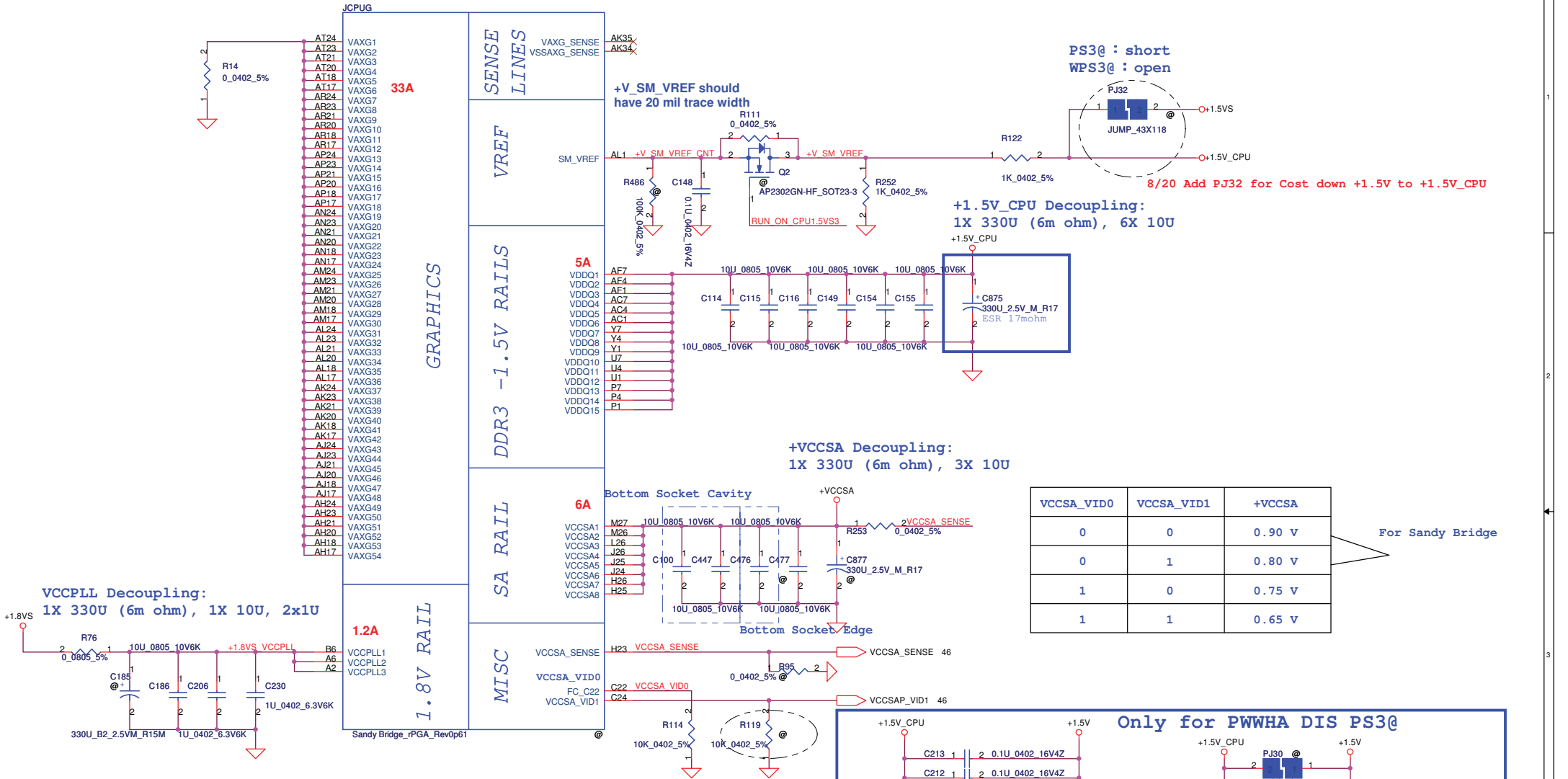


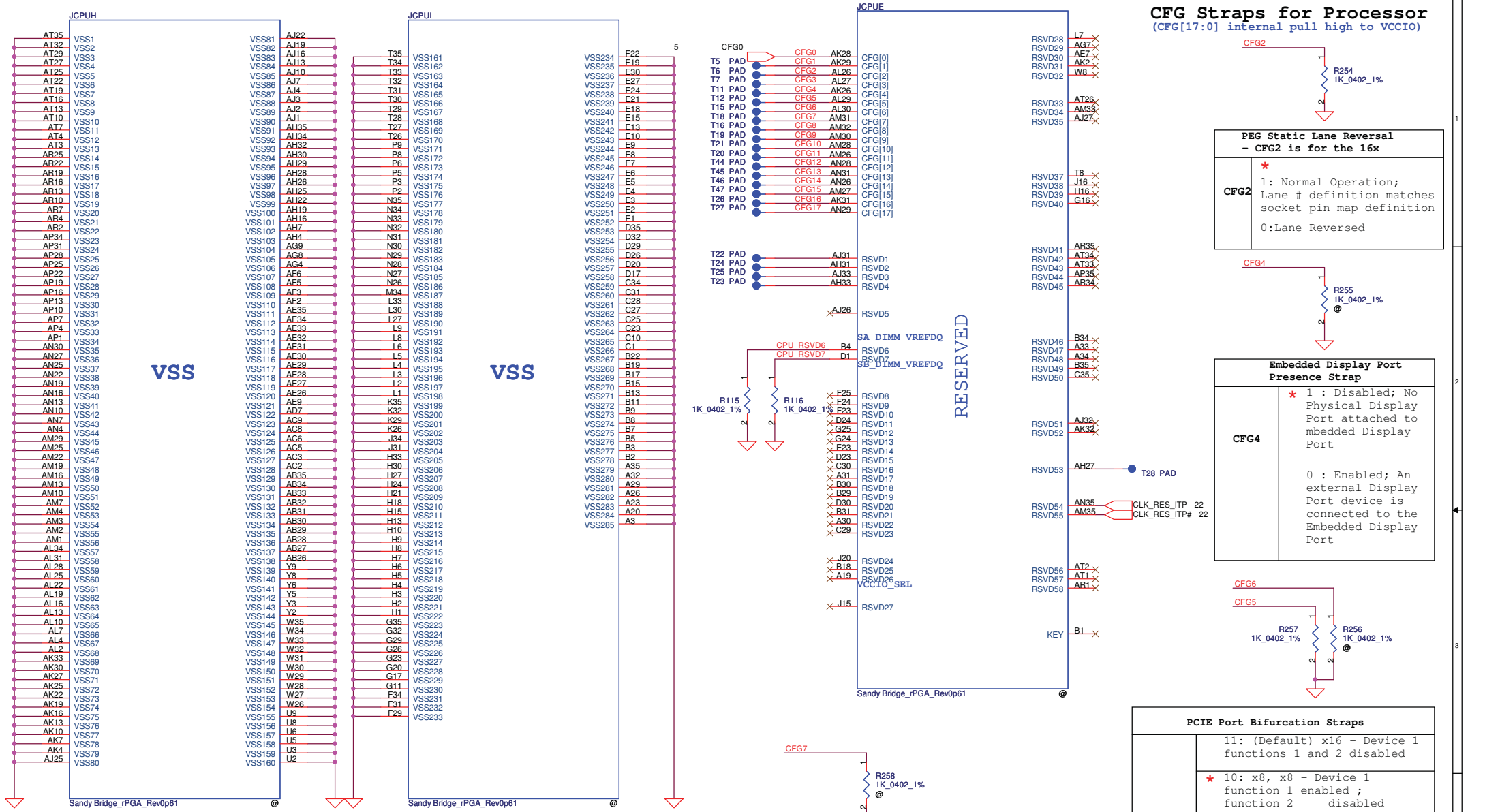
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POWER





CFG Straps for Processor

(CFG[17:0] internal pull high to VCCIO)

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	★ 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

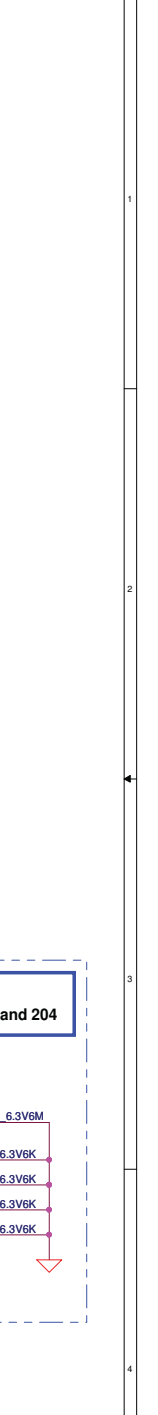
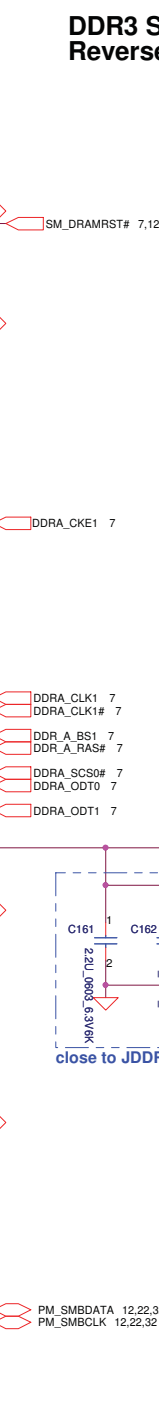
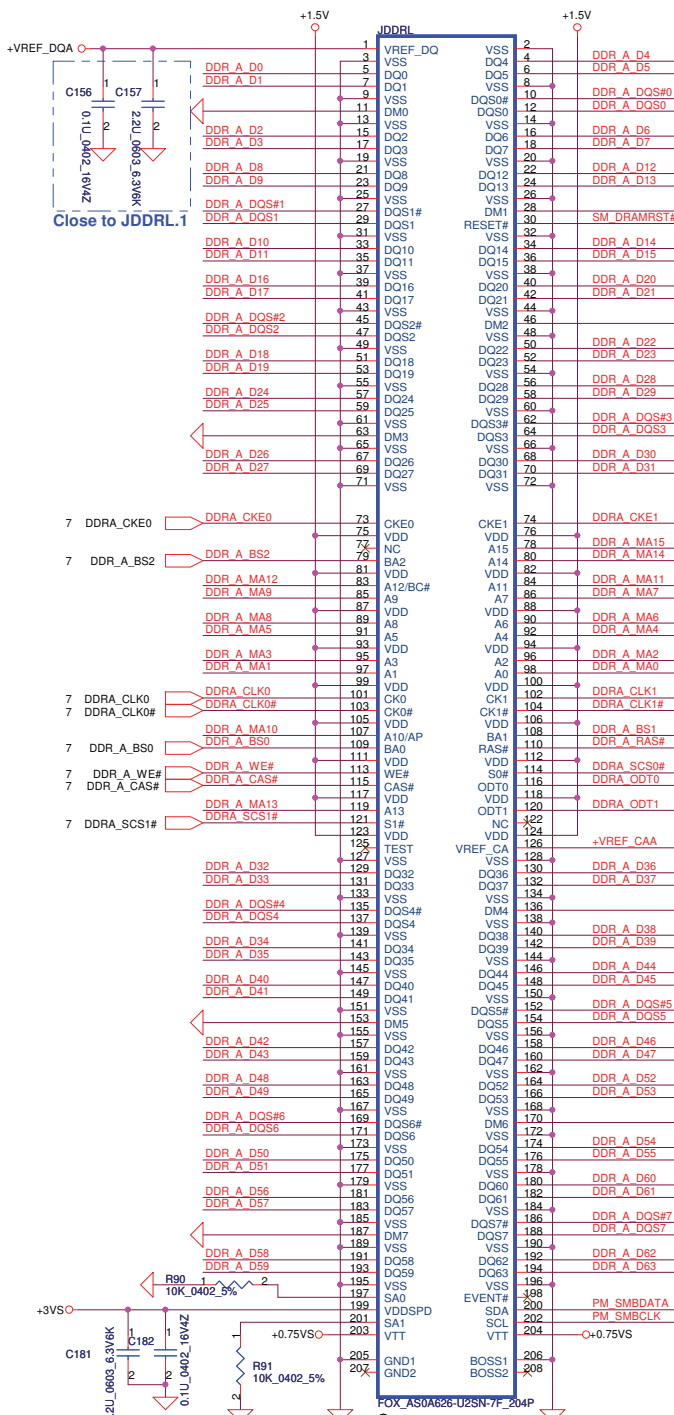
Embedded Display Port Presence Strap	
CFG4	★ 1: Disabled; No Physical Display Port attached to mbedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled
	★ 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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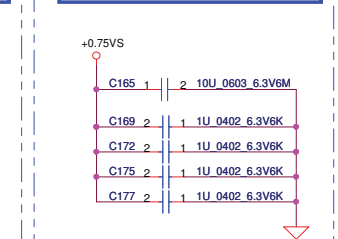
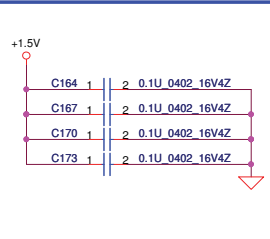
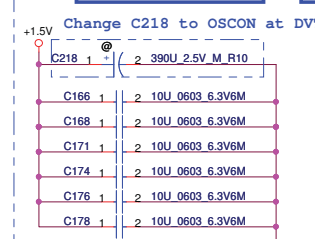
DDR3 SO-DIMM A Reverse Type



Layout Note:
Place near JDDR1

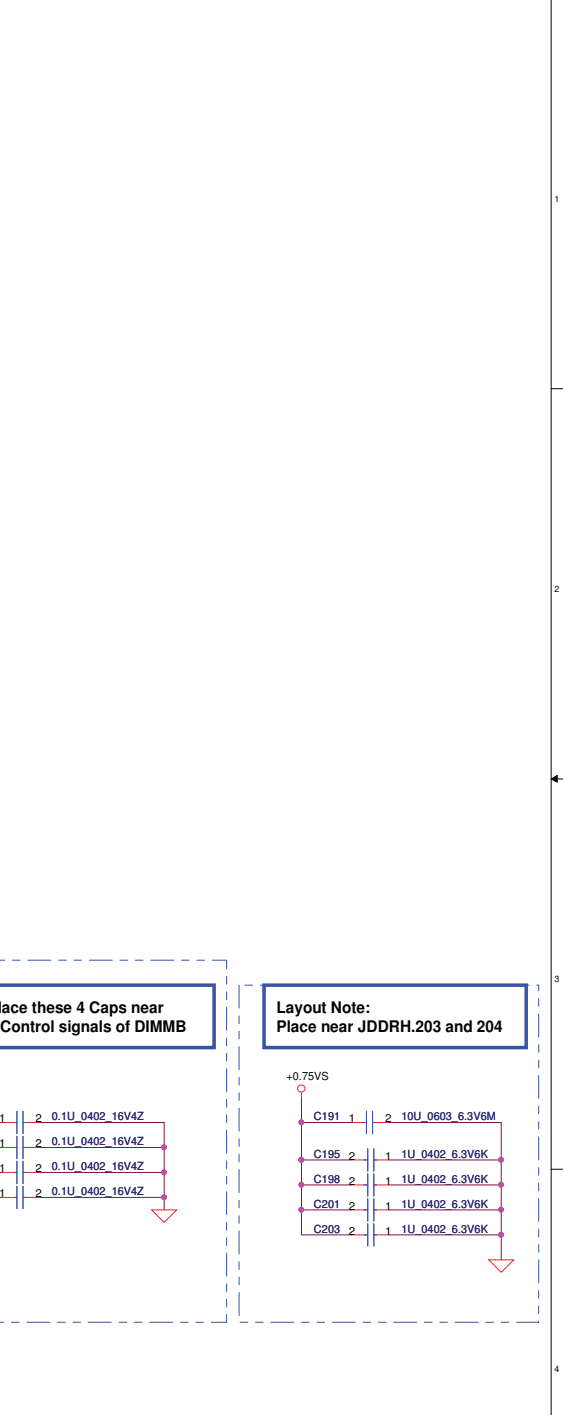
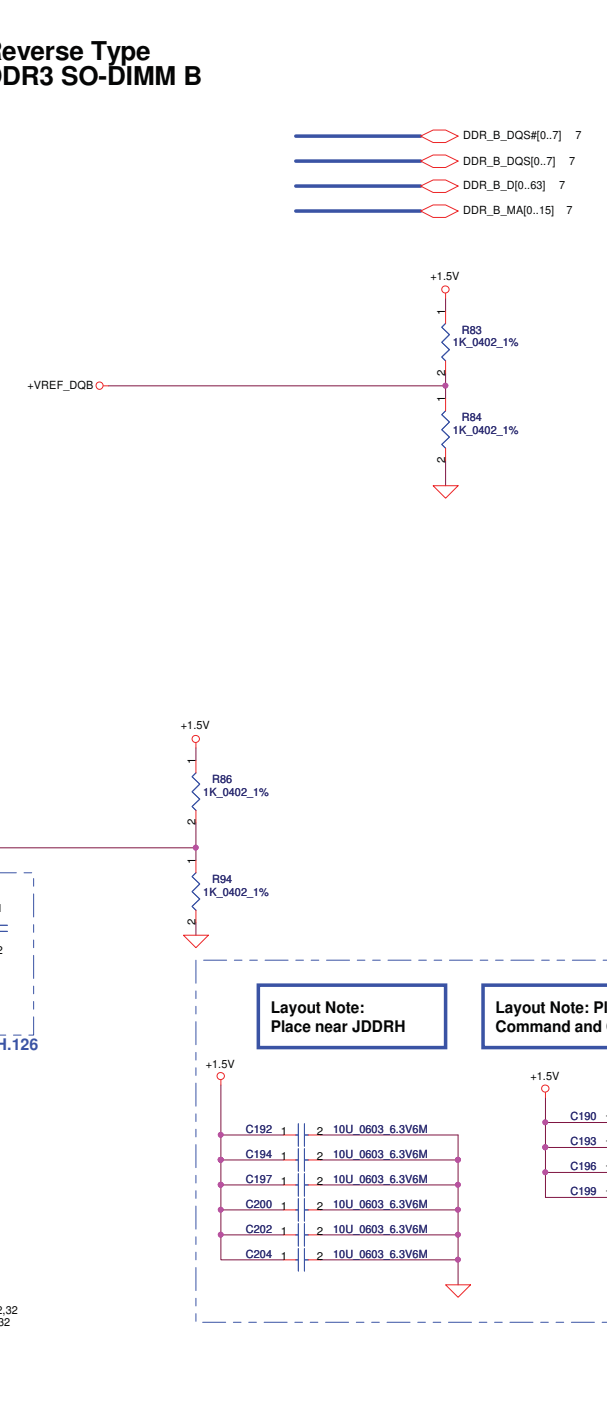
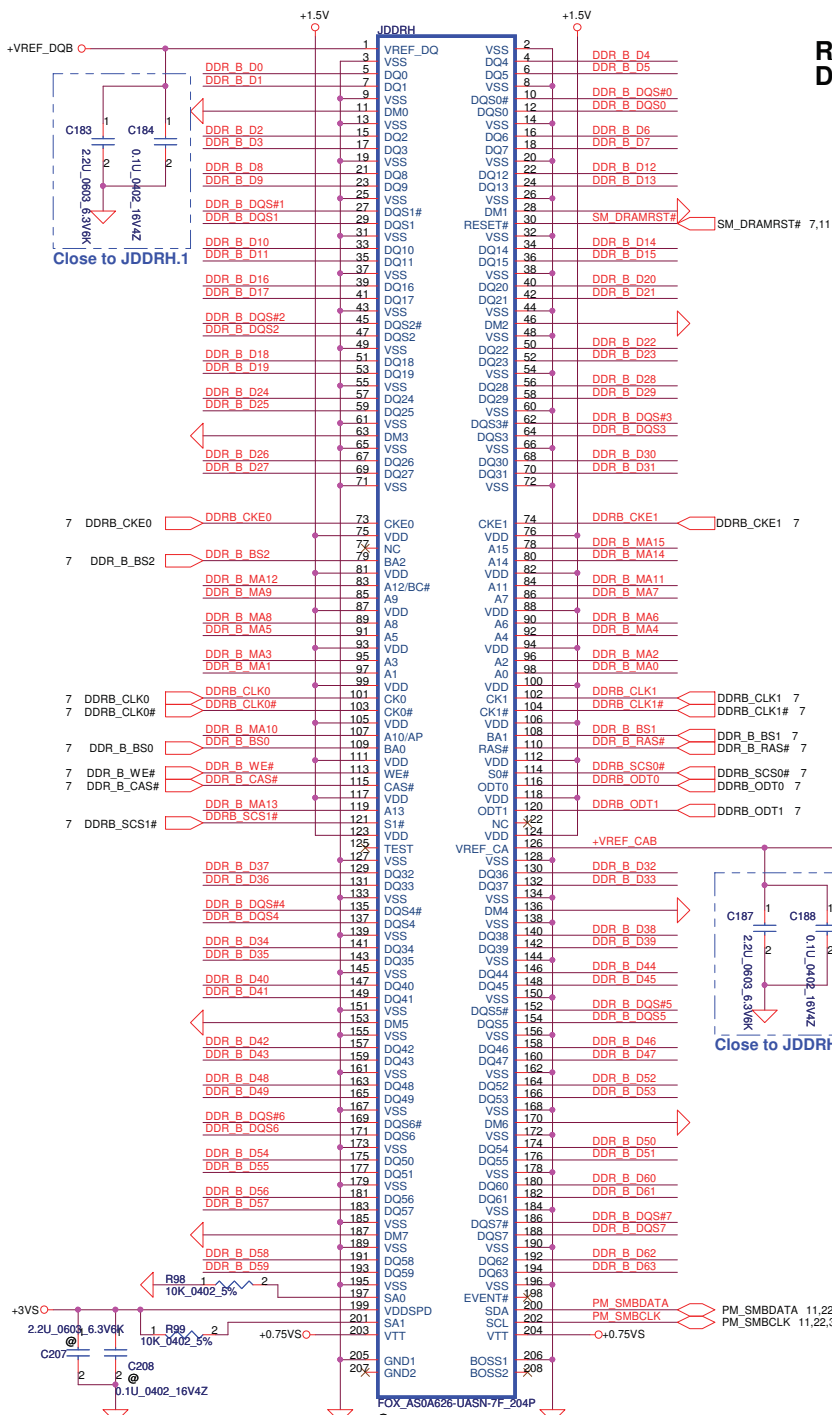
Layout Note: Place these 4 Caps near
Command and Control signals of DIMMA

Layout Note:
Place near JDDR1.203 and 204



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						Size Custom	Document Number		PWWHA LA-7201P M/B		Rev 1.0
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Reverse Type DDR3 SO-DIMM B

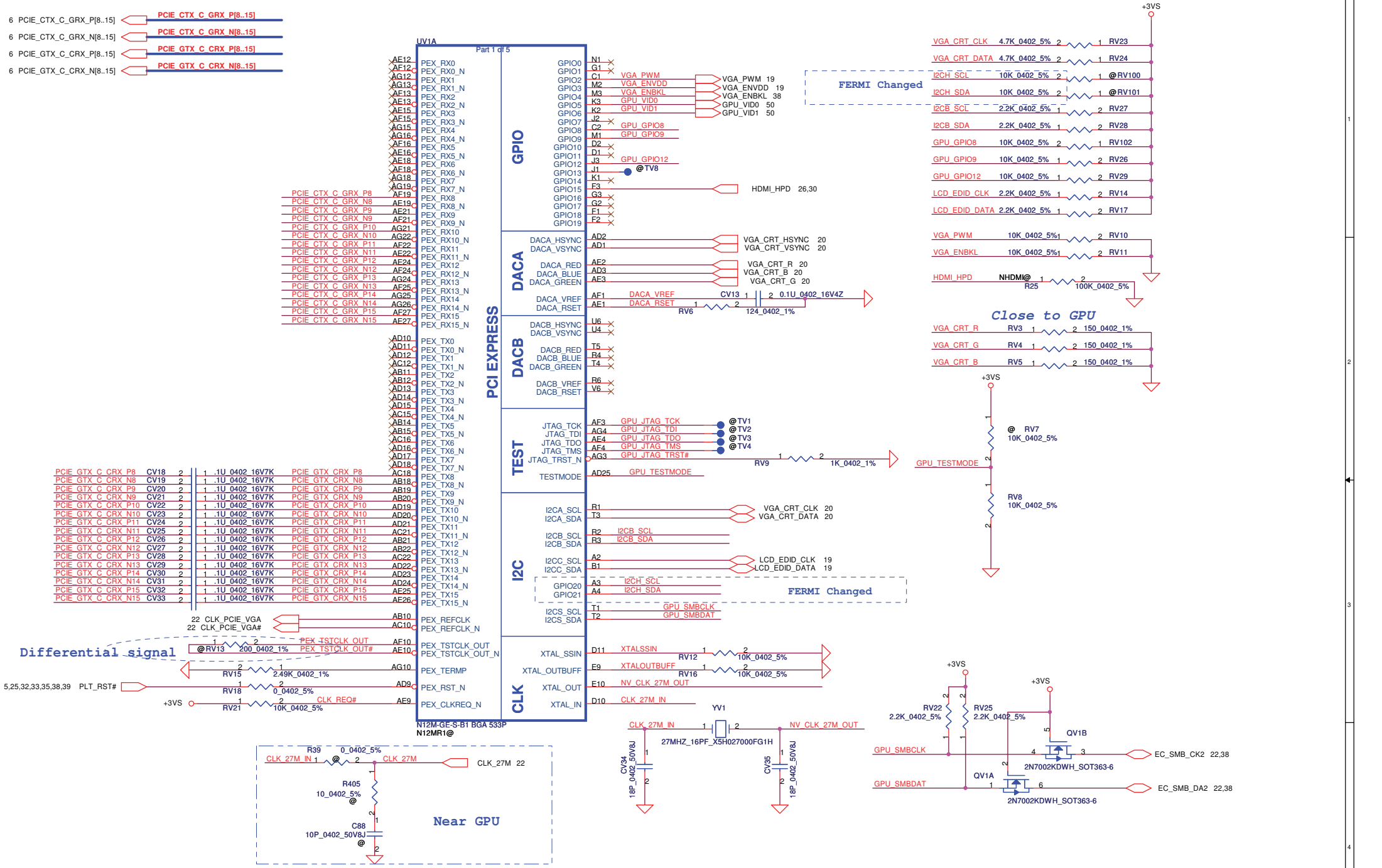


Layout Note:
Place near JDDR.H

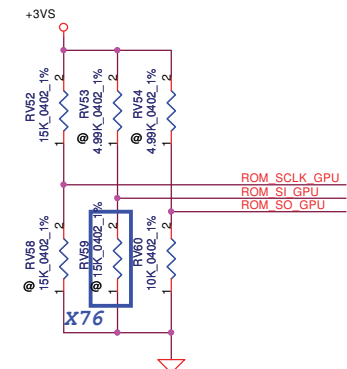
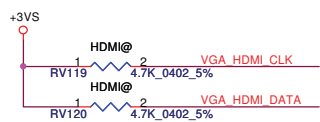
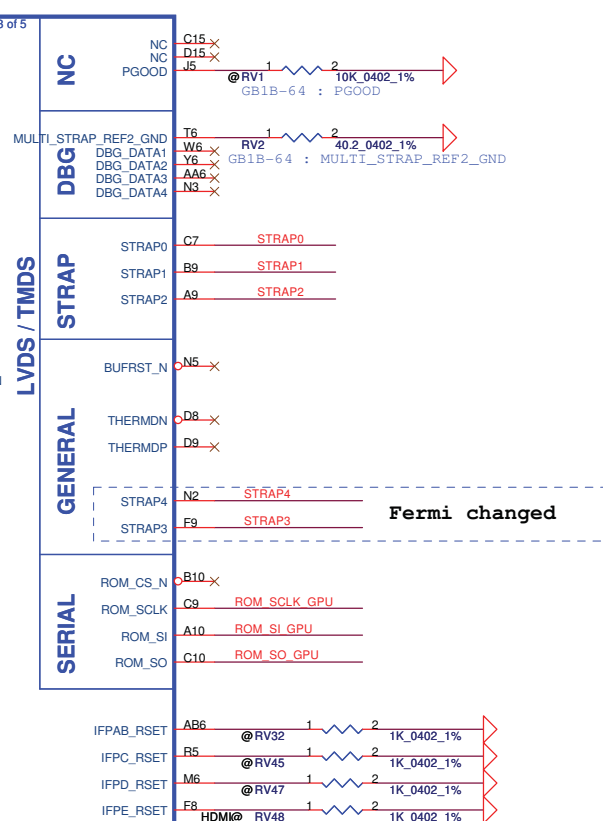
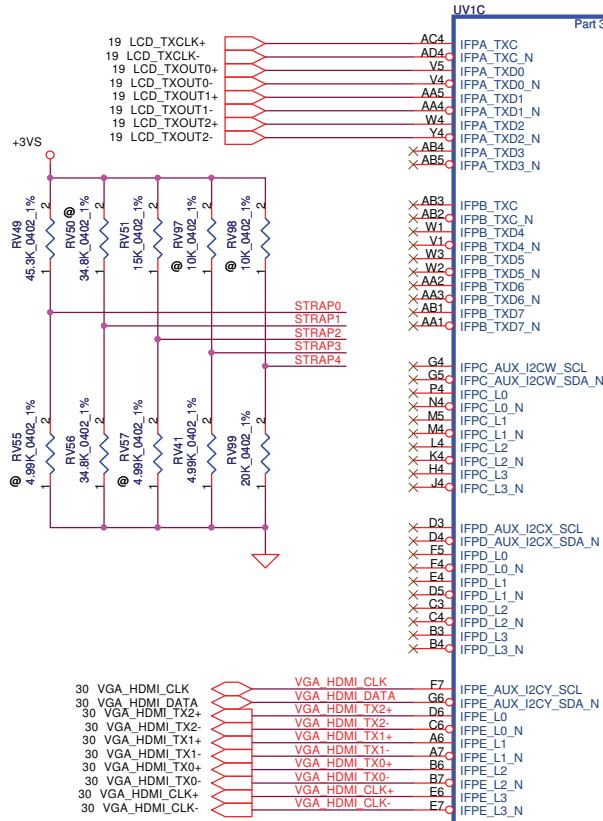
Layout Note: Place these 4 Caps near
Command and Control signals of DIMM B

Layout Note:
Place near JDDR.H.203 and 204

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						Size	Document Number	Rev
						Custom	PWWHA LA-7201P M/B	1.0
						Date:	Friday, March 04, 2011	Sheet

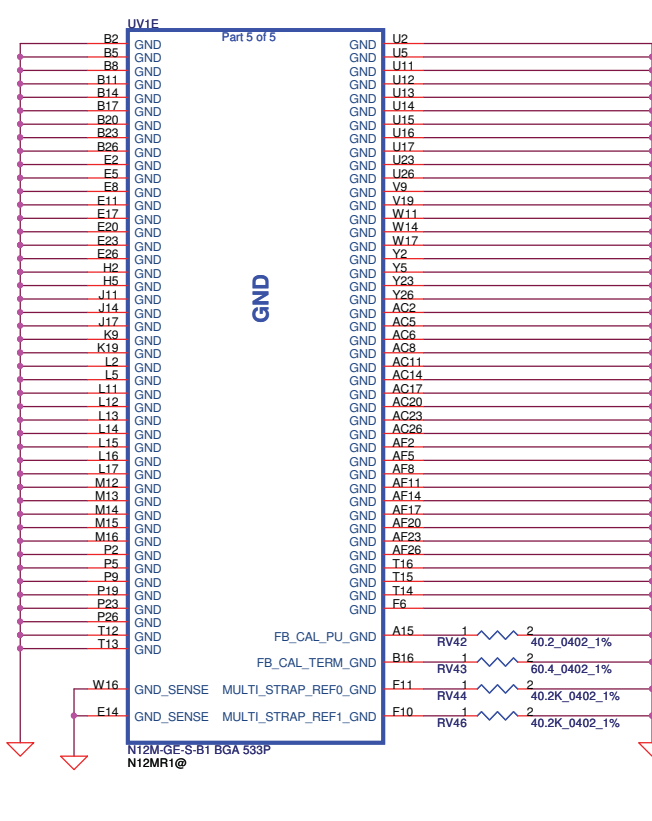


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N12M-GE-S-B1 BGA 533P
N12MR1@

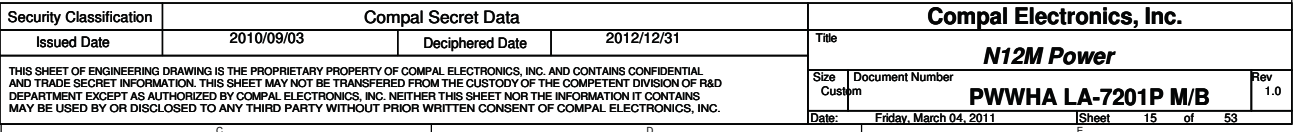
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

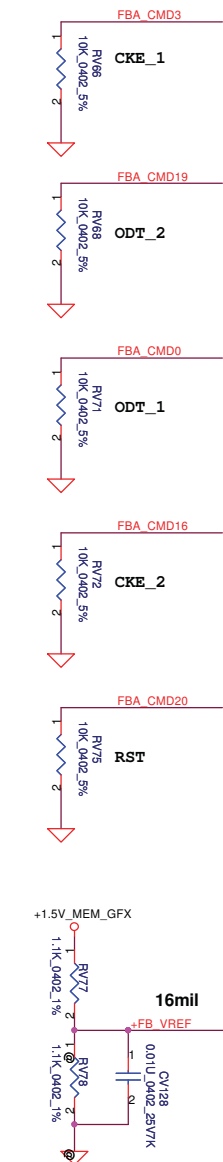


Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Hynix (800MHZ) 64MX16 H5TQ1G63DFR-12C SA0000324C0	512MB	0010	RV59 PD 15K (SD034150280)
Hynix (900MHZ) 128MX16 H5TQ2G63BFR-11C SA00003Y000	1GB	0110	RV59 PD 34.8K (SD034348280)
Samsung (800MHZ) 64MX16 K4W1G1646G-BC12 SA00004HS00	512MB	0011	RV59 PD 20K (SD034200280)
Samsung (900MHZ) 128MX16 K4W2G1646C-HC11 SA000047Q00	1GB	0111	RV59 PD 45.3K (SD034453280)

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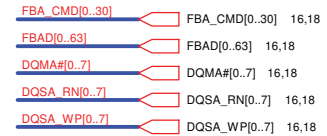
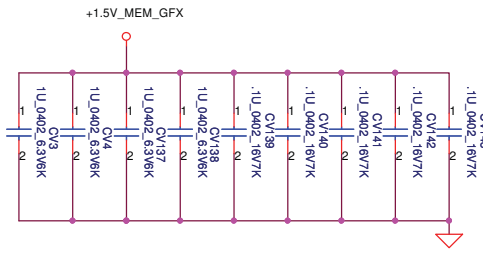
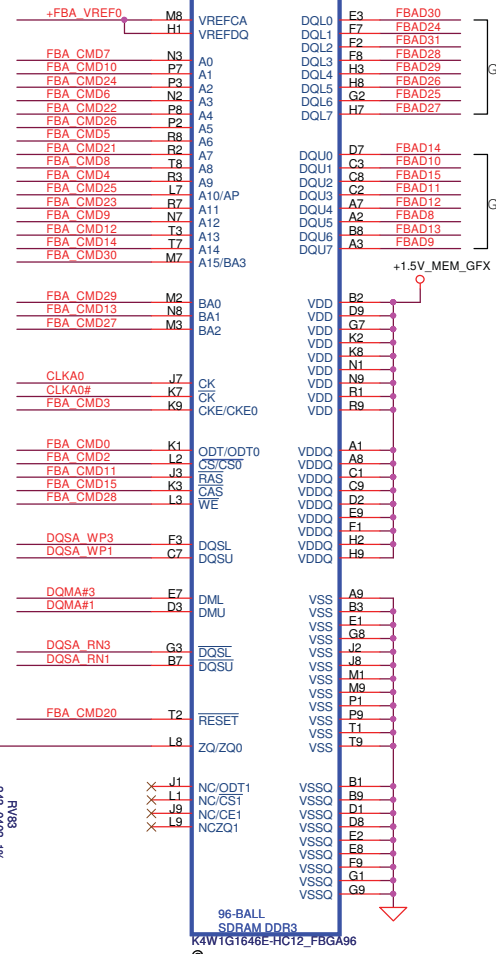
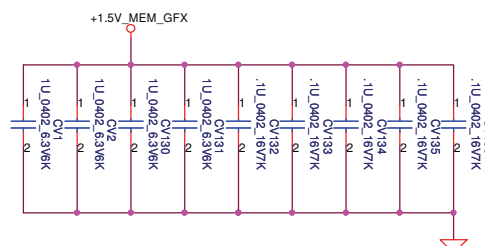
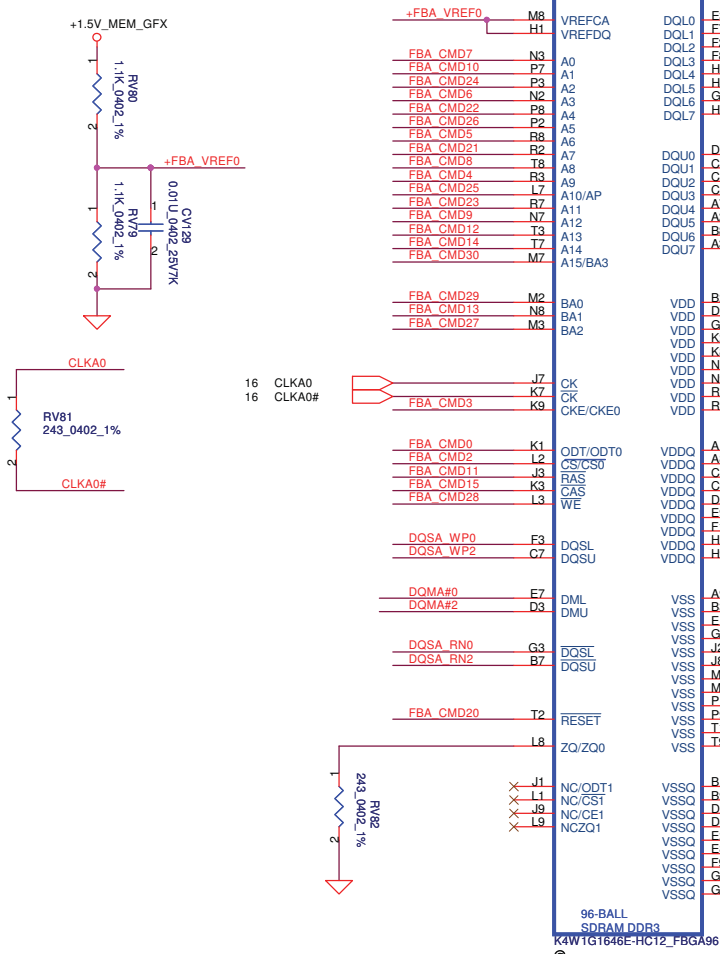
PAD~D TV6@

	DATA Bus	
Address	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

Memory Partition A - Lower 32 bits

16mil

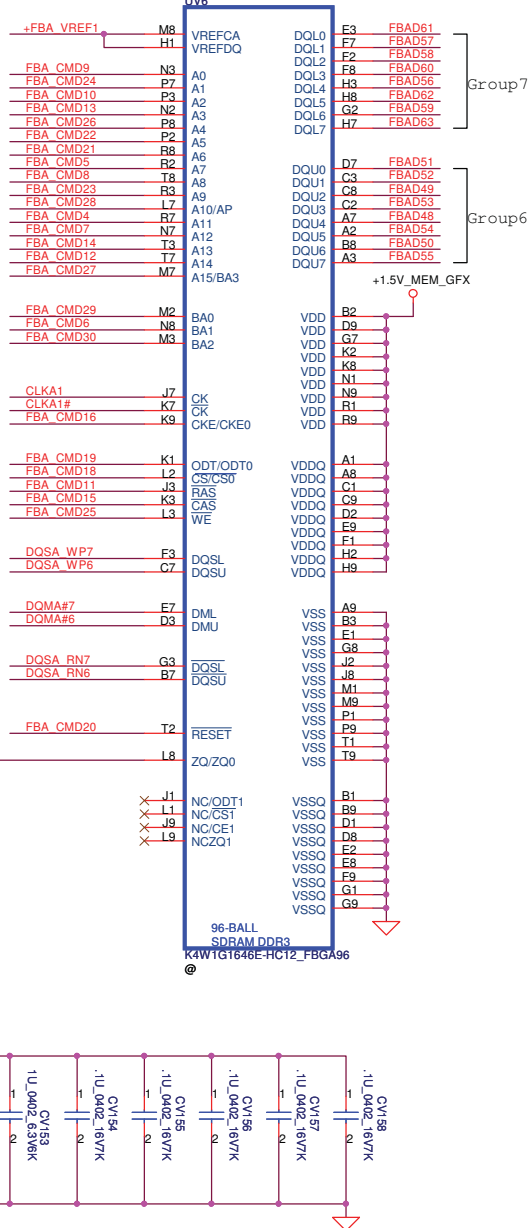
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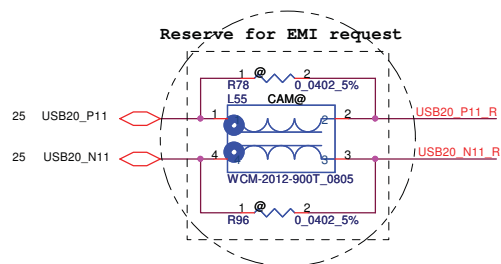
Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

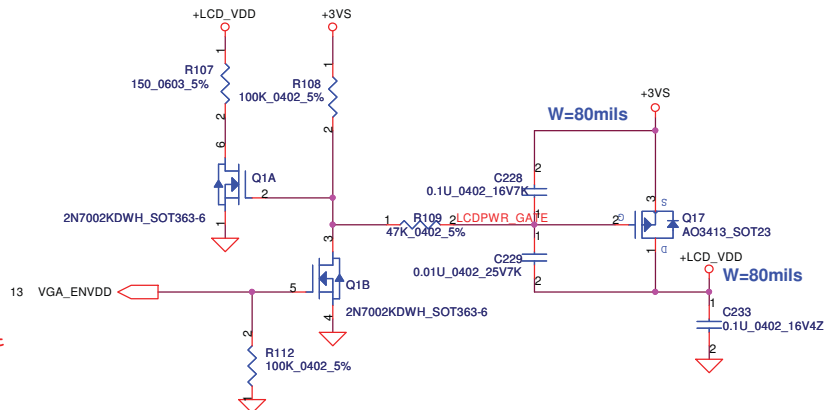
16mil



	DATA Bus	
Address	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

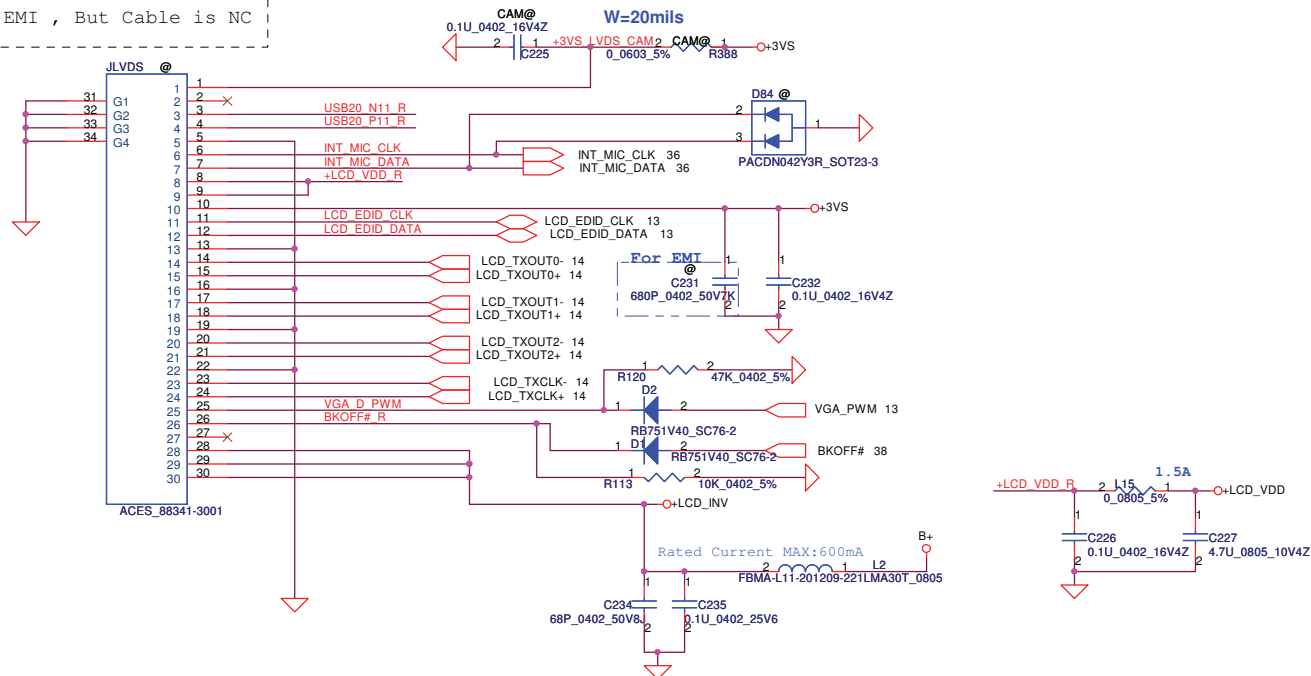


8/20 Swap USB20_P11 and USB20_N11 for layout request



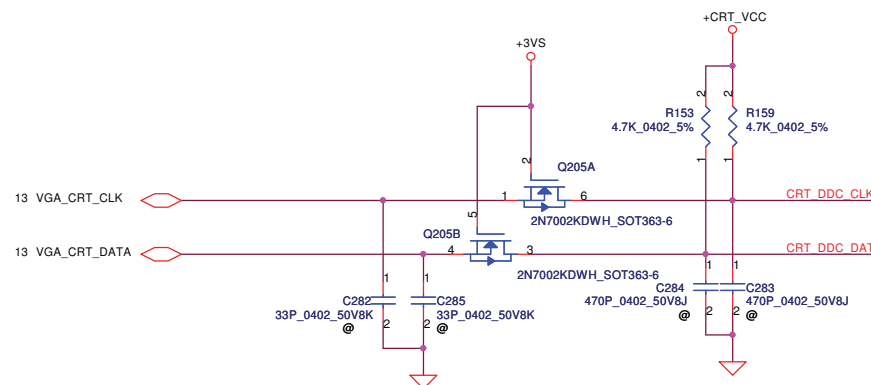
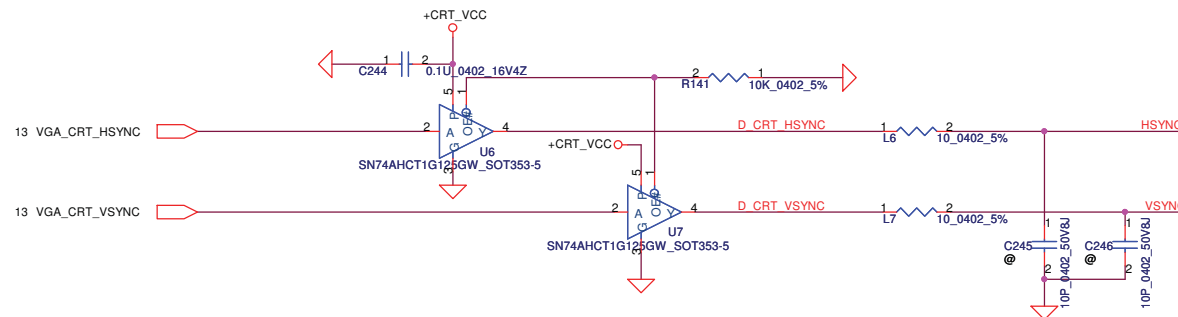
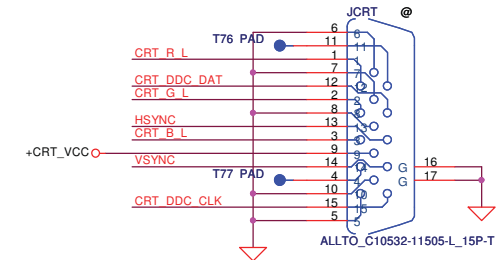
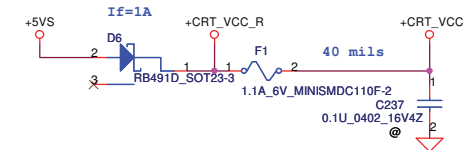
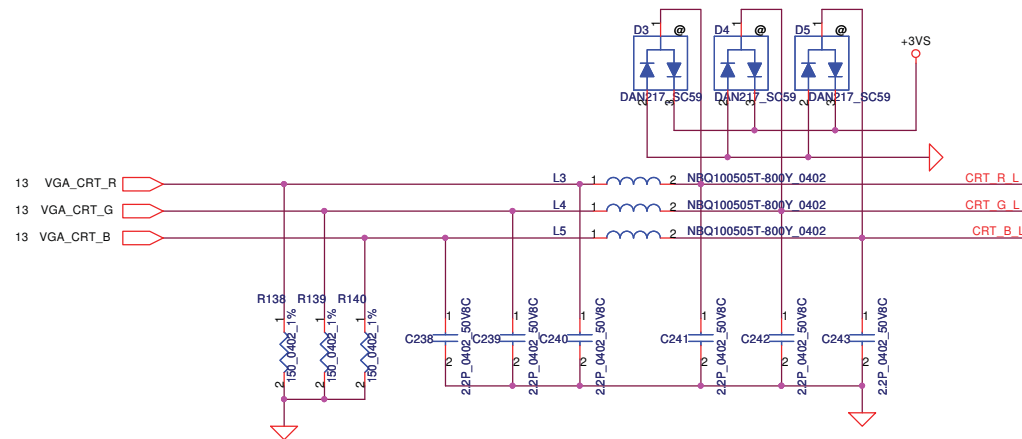
LCD/PANEL BD. Conn.

Pin13 GND for EMI , But Cable is NC

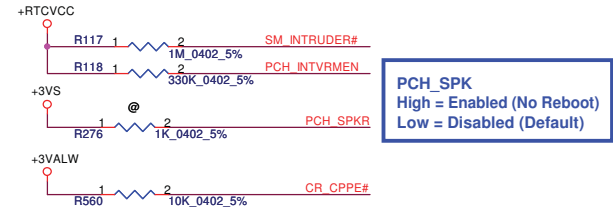
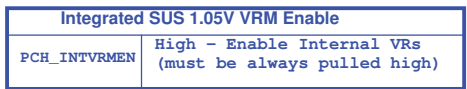
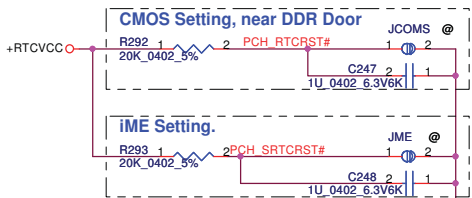


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Size	Custom	Document Number	PWWHA LA-7201P M/B	Rev	1.0
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CRT CONNECTOR



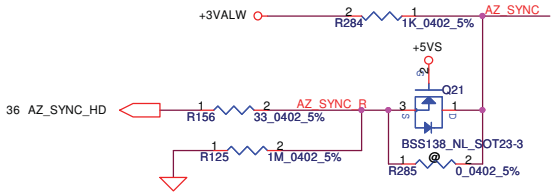
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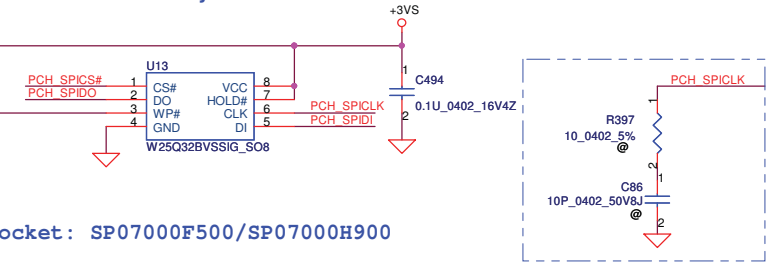
PCH_SPK
High = Enabled (No Reboot)
Low = Disabled (Default)

HDA_SDO
ME debug mode,
this signal has a weak internal pull down
★Low = Disable (default)
High = Enable (flash descriptor security override)

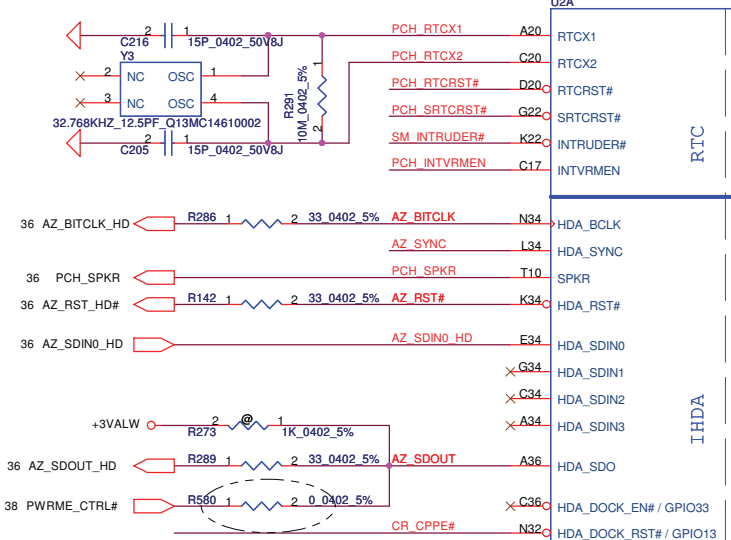
HDA_SYNC
★This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
Need to pull high for Huron River platform



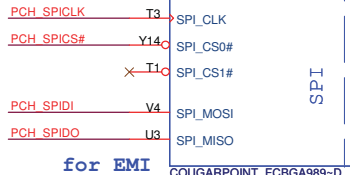
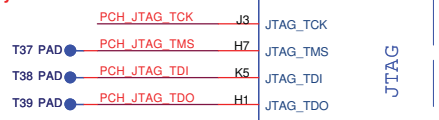
4M Byte



Socket: SP07000F500/SP07000H900
Please close to U2 PCH
8/30 Change U13 from SA000021A00 to SA000031N00 due to EOL of SA000021A00

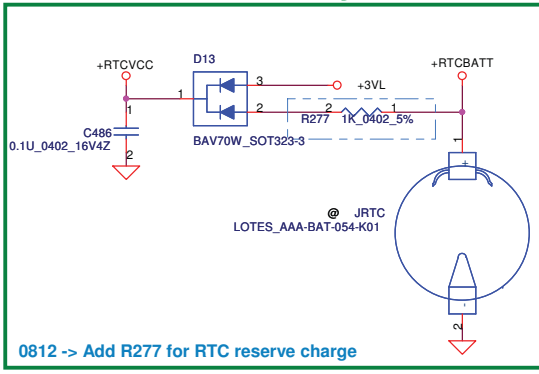


8/30 Change PWRME_CTRL# to HDA_SDO by PCH EDS

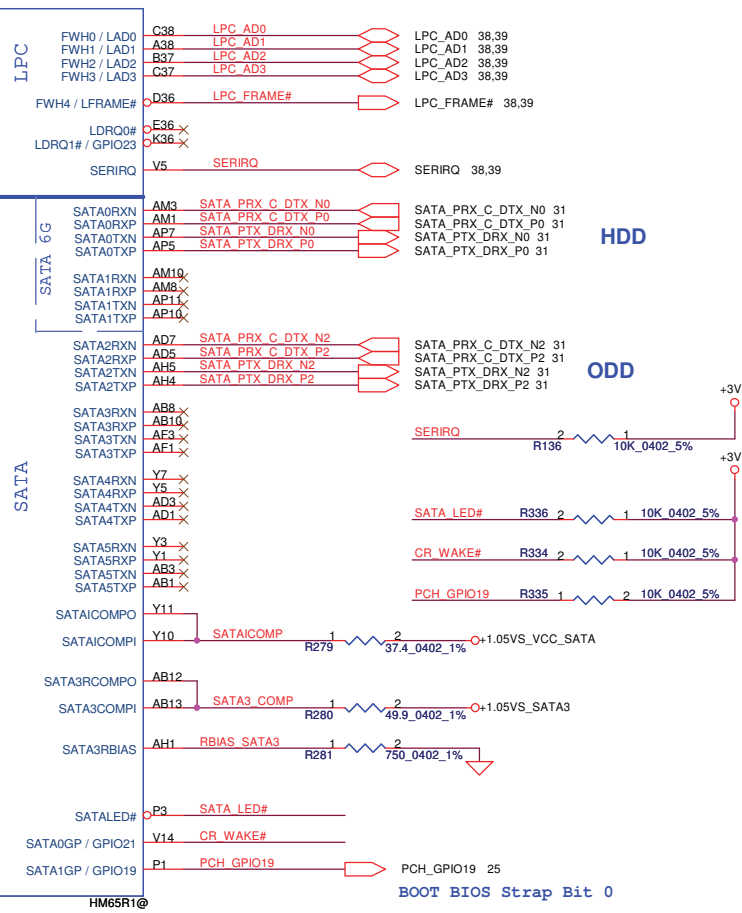


for EMI

RTC schematic for non-chargeable



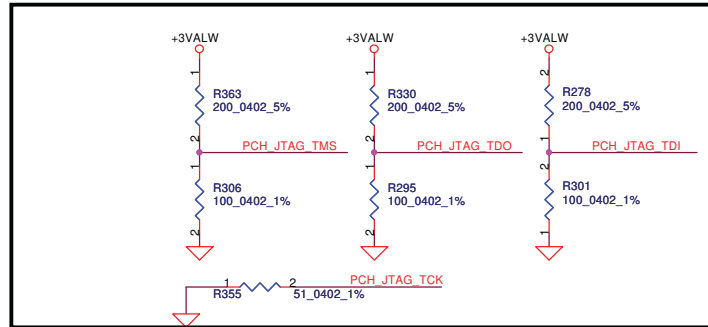
0812 -> Add R277 for RTC reserve charge



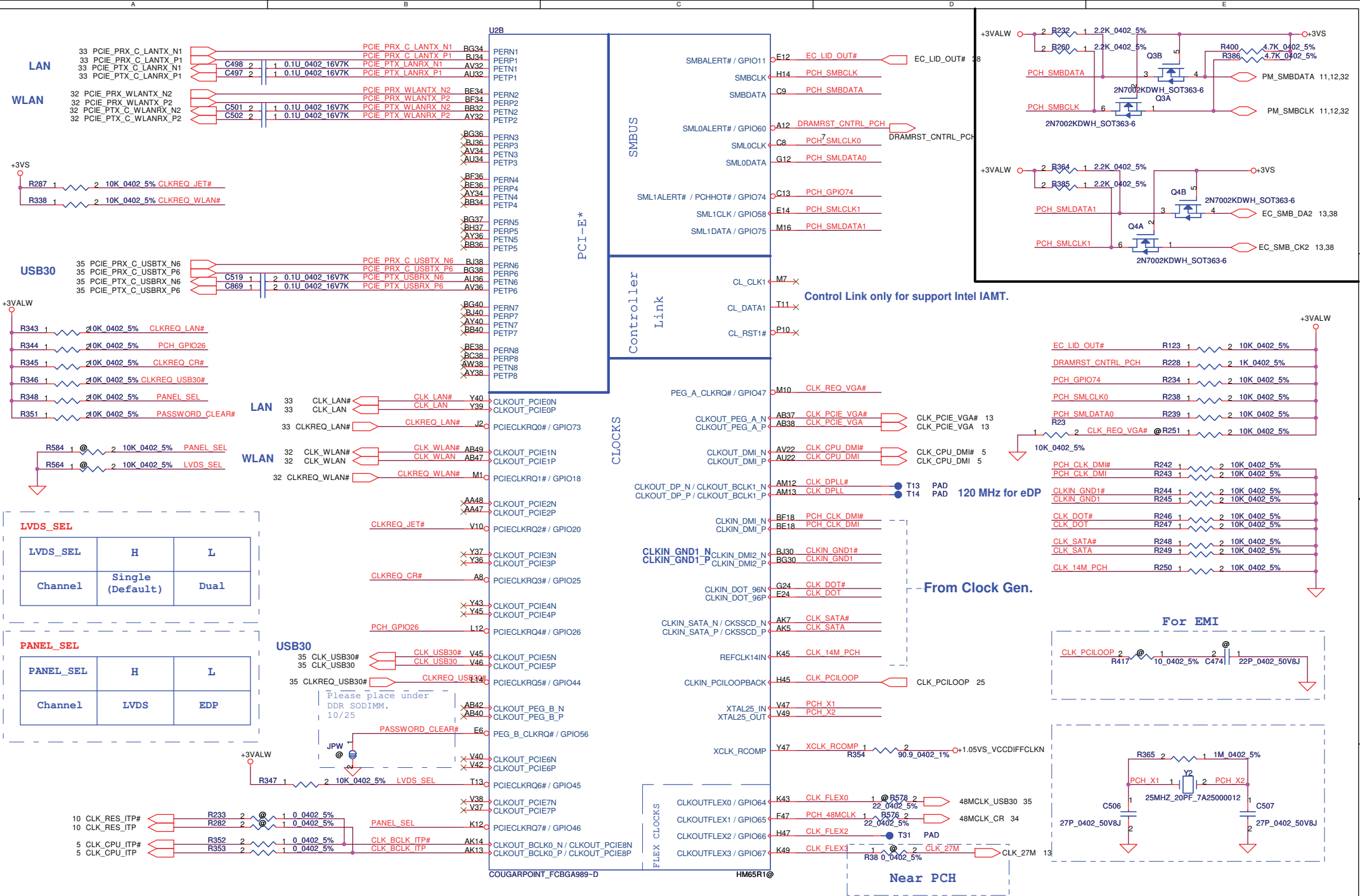
HDD

ODD

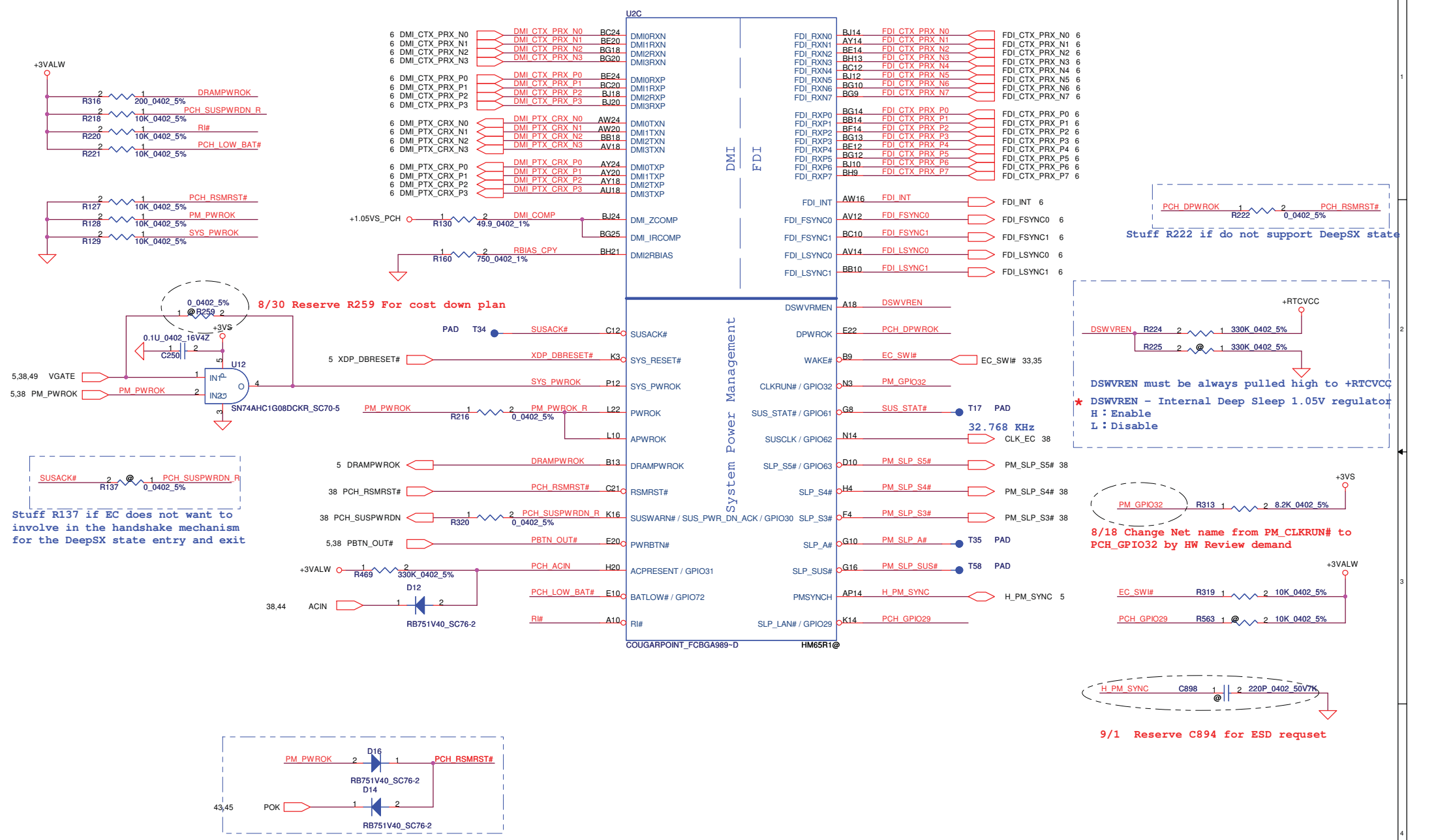
BOOT BIOS Strap Bit 0



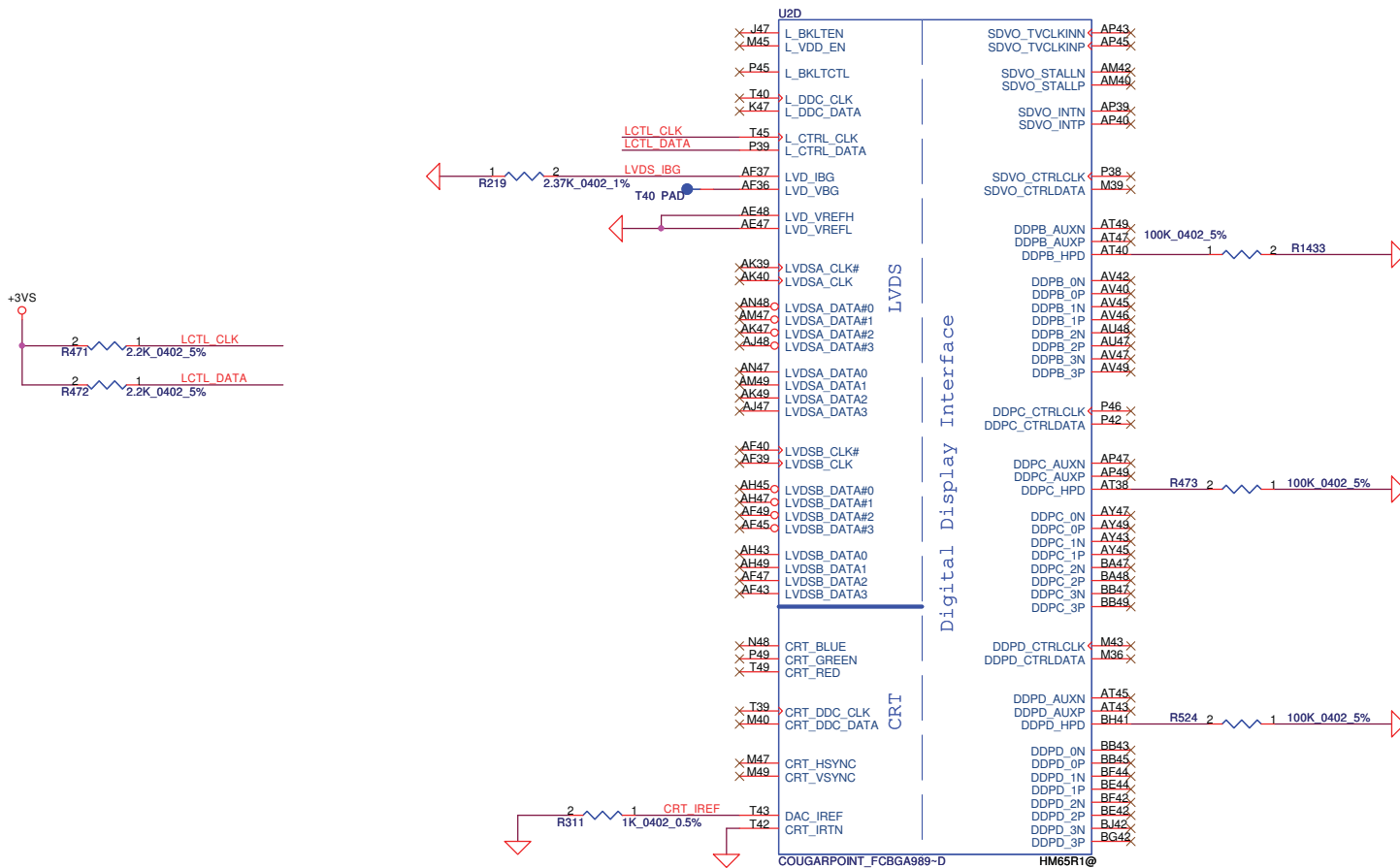
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		Size	Document Number	Rev					
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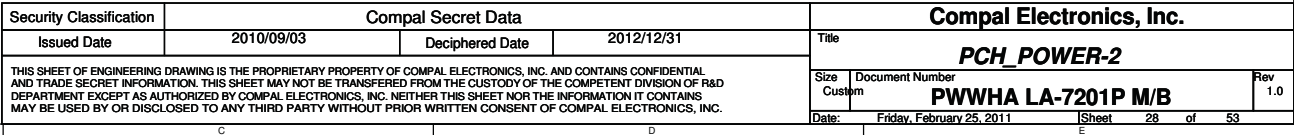
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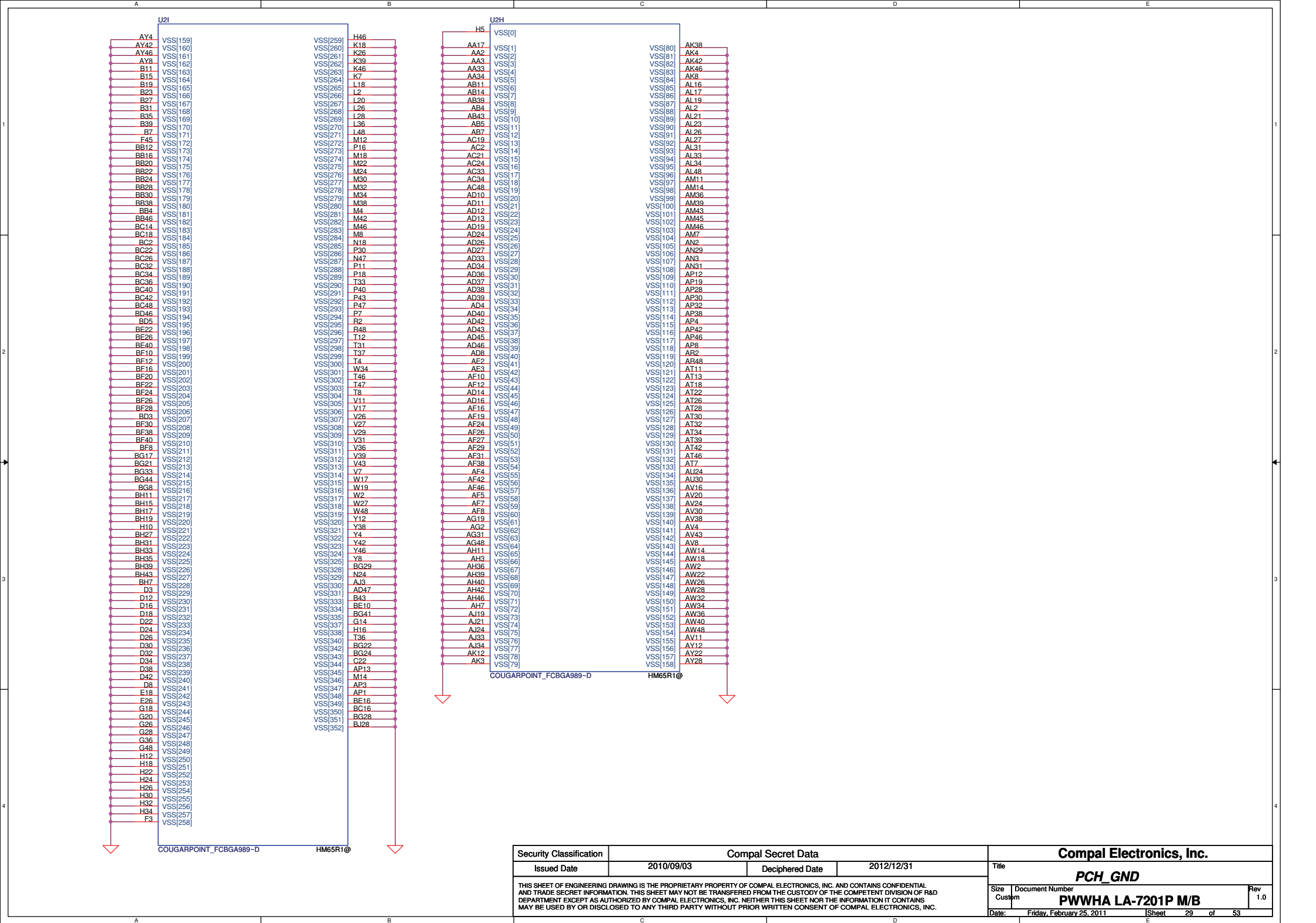


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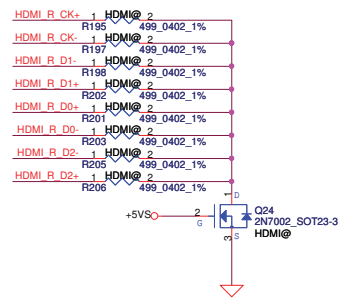
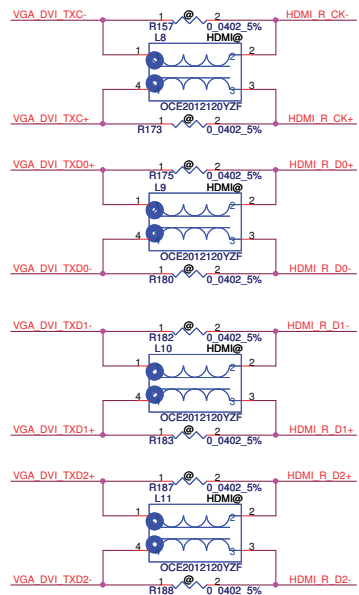
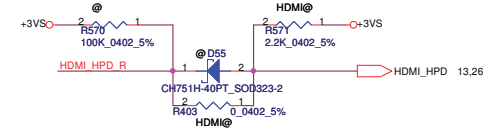
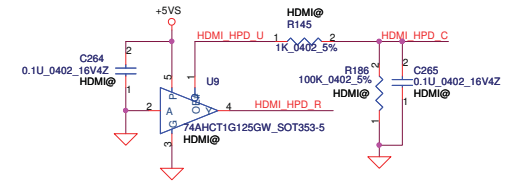
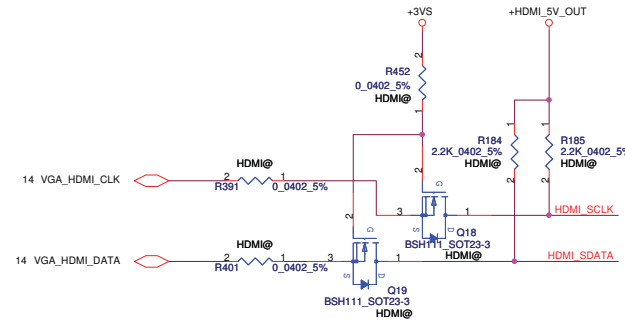




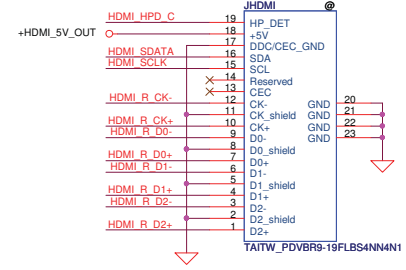
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For DISCRETE

14	VGA_HDMI_CLK+	CV296	1	2	0.1U_0402_16V7K	HDMI@	VGA_DVI_TXC+
14	VGA_HDMI_CLK-	CV293	1	2	0.1U_0402_16V7K	HDMI@	VGA_DVI_TXC-
14	VGA_HDMI_TX0+	CV294	1	2	0.1U_0402_16V7K	HDMI@	VGA_DVI_TXD0+
14	VGA_HDMI_TX0-	CV297	1	2	0.1U_0402_16V7K	HDMI@	VGA_DVI_TXD0-
14	VGA_HDMI_TX1+	CV299	1	2	0.1U_0402_16V7K	HDMI@	VGA_DVI_TXD1+
14	VGA_HDMI_TX1-	CV298	1	2	0.1U_0402_16V7K	HDMI@	VGA_DVI_TXD1-
14	VGA_HDMI_TX2+	CV295	1	2	0.1U_0402_16V7K	HDMI@	VGA_DVI_TXD2+
14	VGA_HDMI_TX2-	CV300	1	2	0.1U_0402_16V7K	HDMI@	VGA_DVI_TXD2-

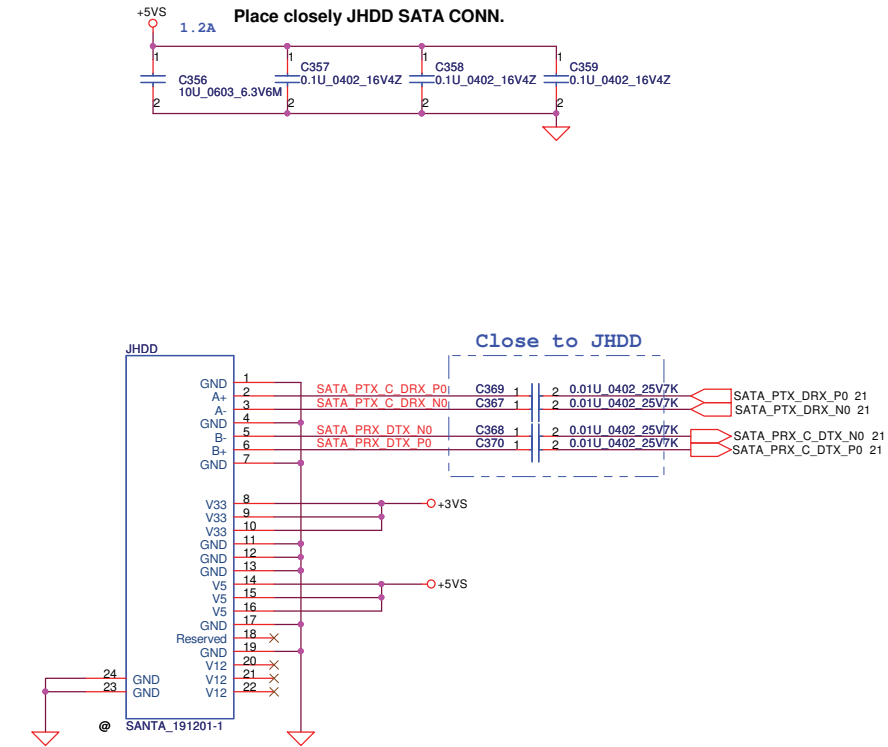


HDMI Connector

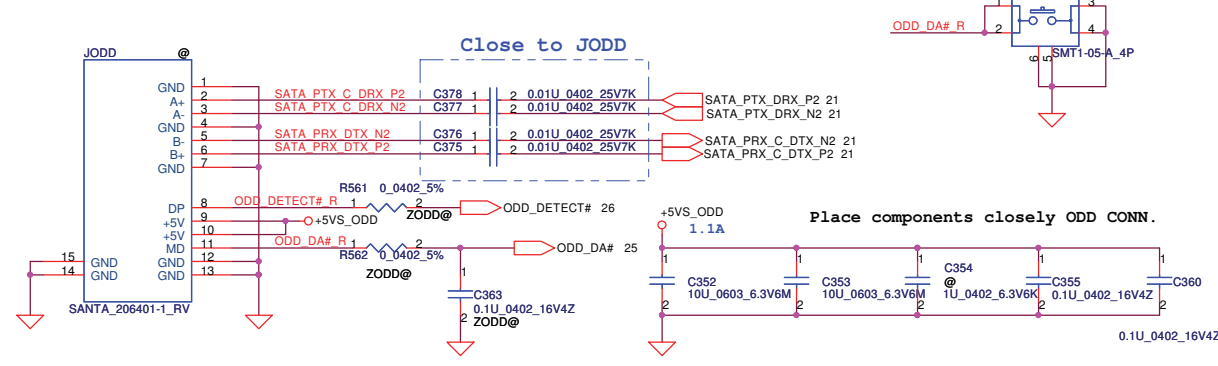


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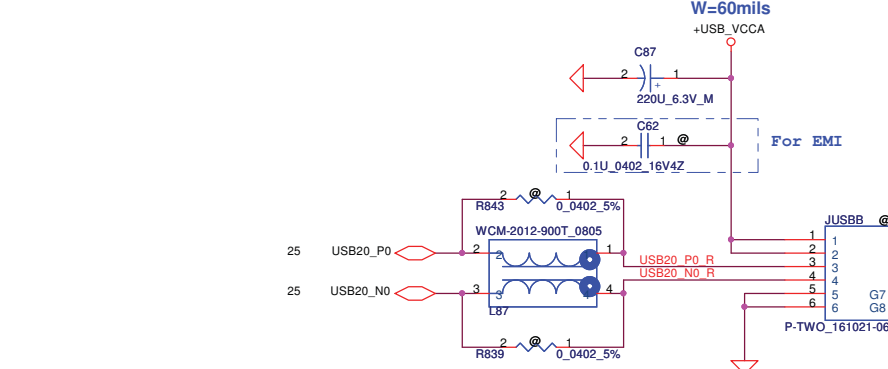
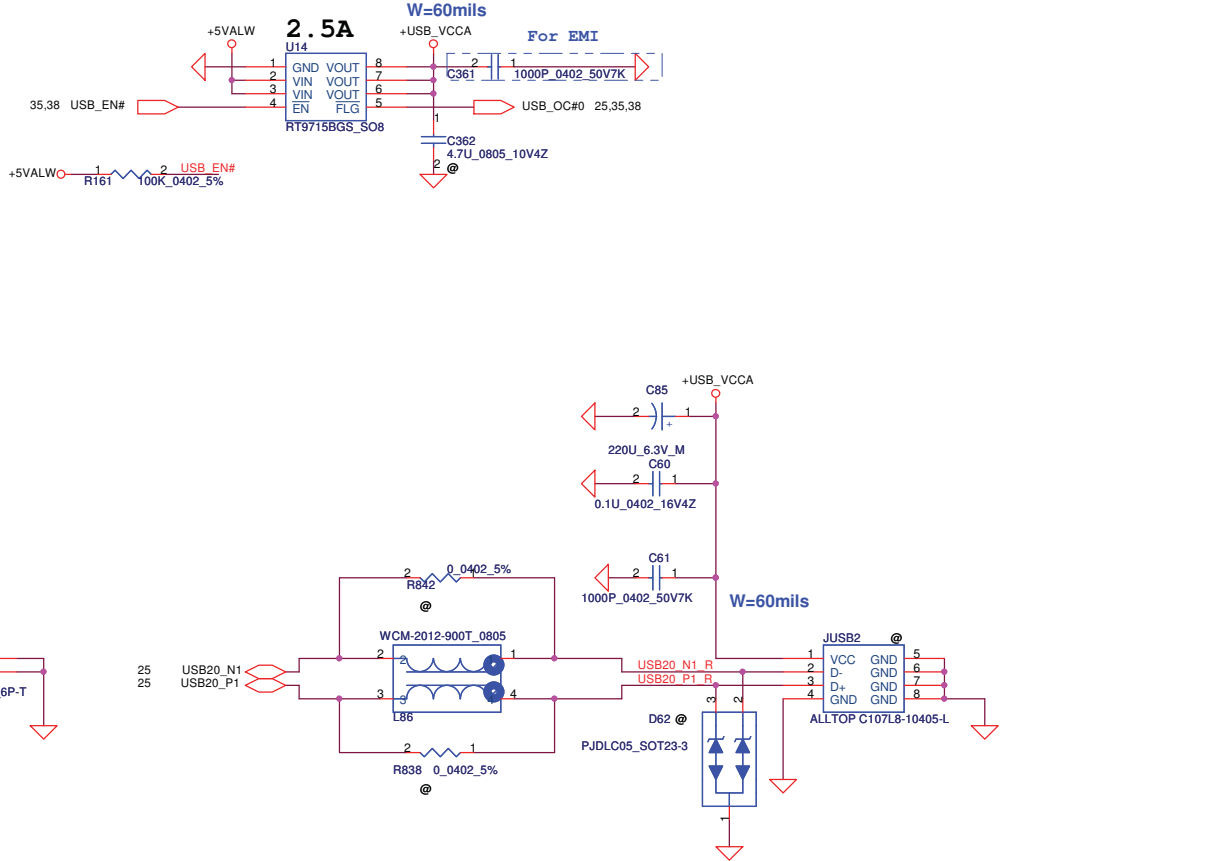
SATA HDD Conn



SATA ODD Conn

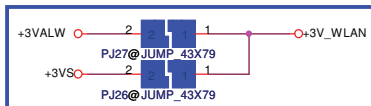


USB Conn

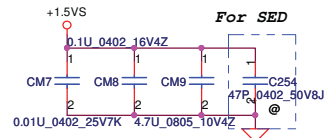
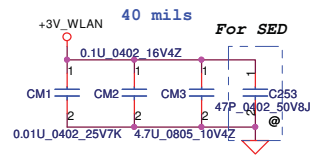


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		PWWHA LA-7201P M/B		1.0	
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Half PCIe Mini Card-WLAN/ WiMax

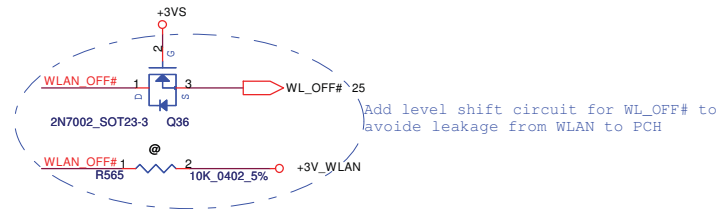
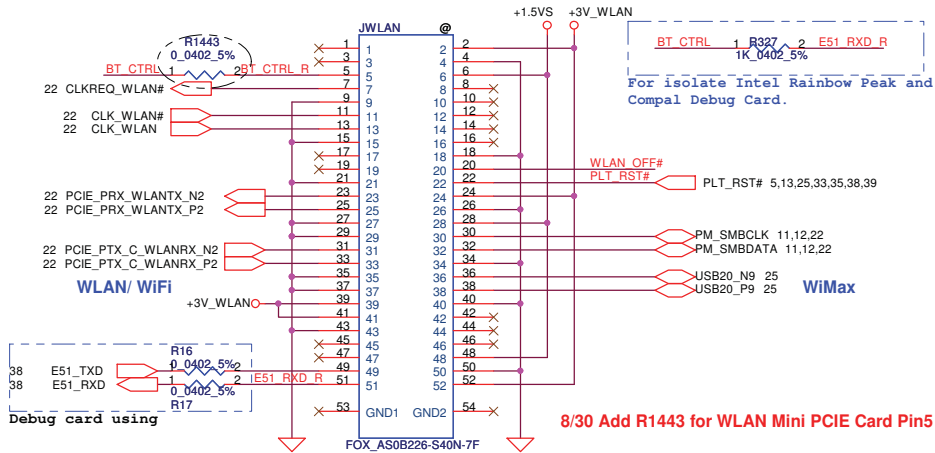
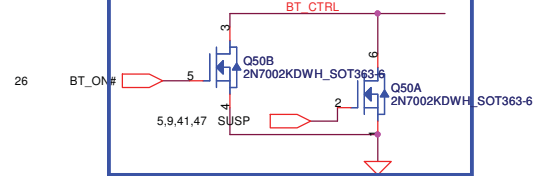


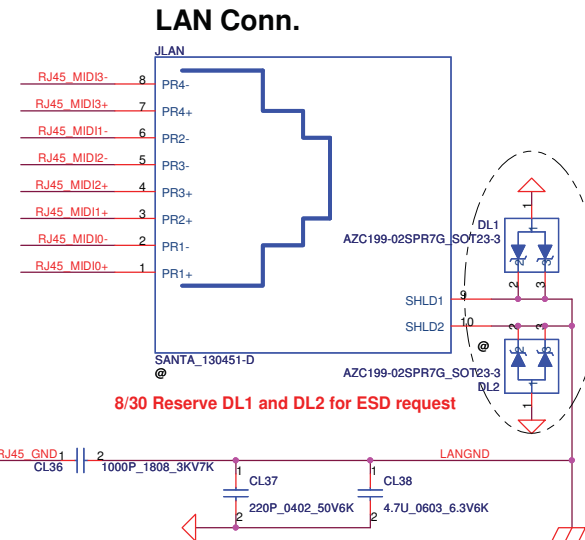
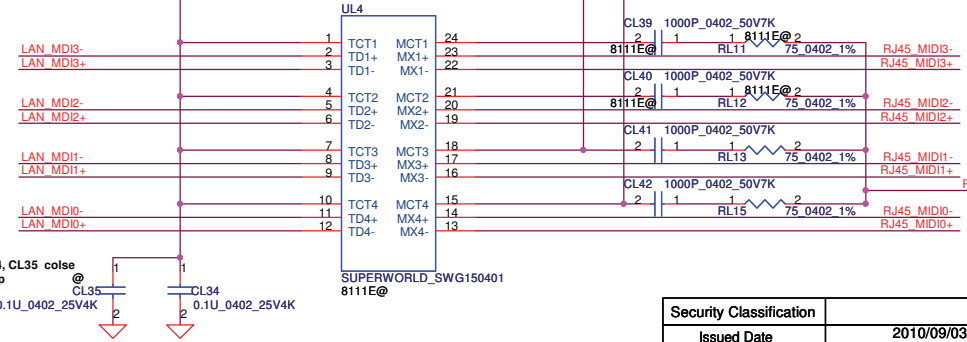
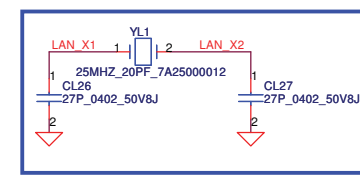
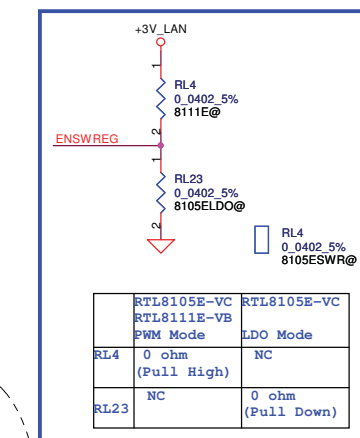
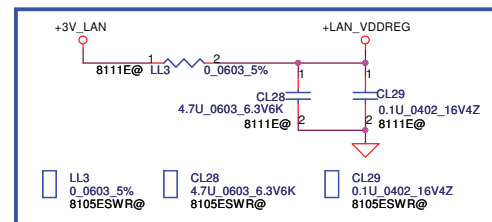
Short PJ27 for Wimax
Short PJ26 for WLAN

WLAN&BT Combo module circuits

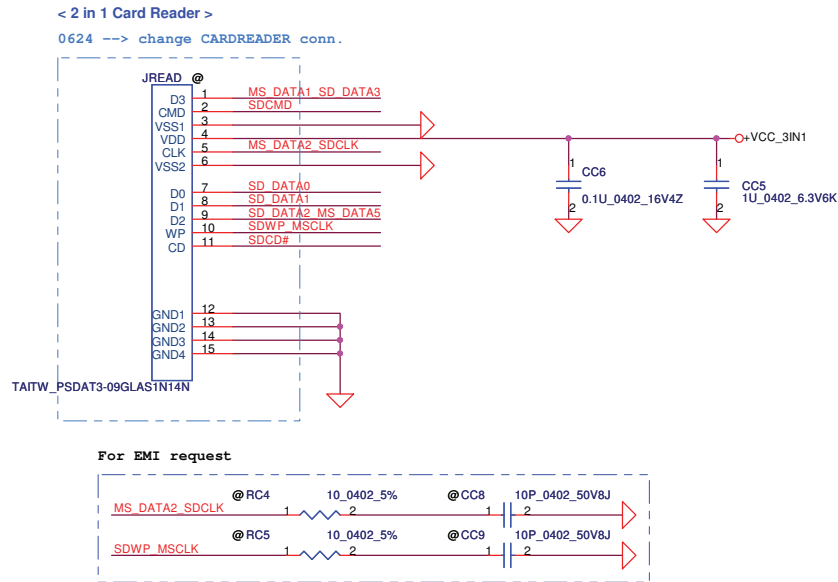
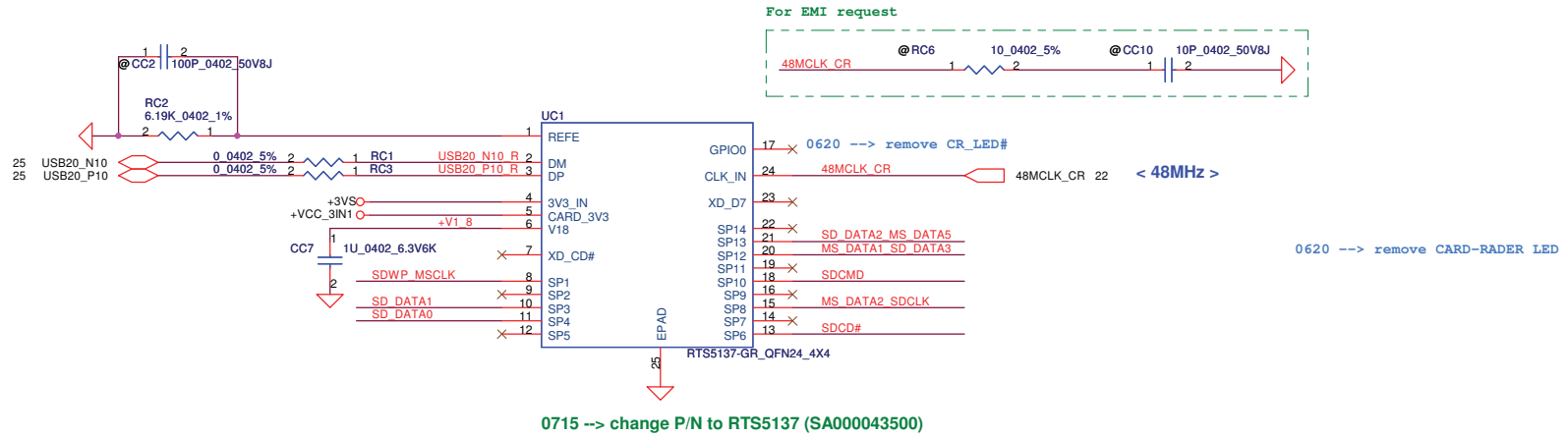
	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H

****If +3V_WLAN is +3VS, please remove D24**



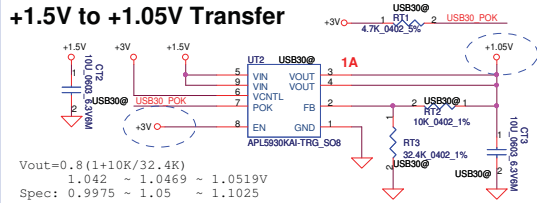


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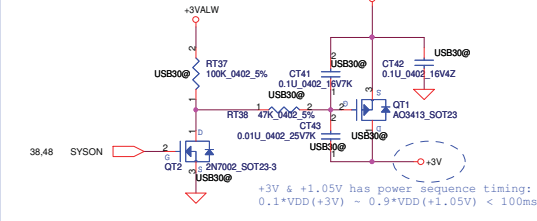


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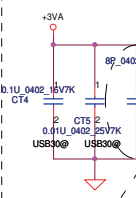
+1.5V to +1.05V Transfer



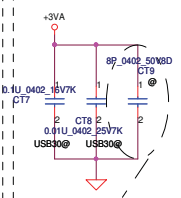
+3VALW to +3V Transfer



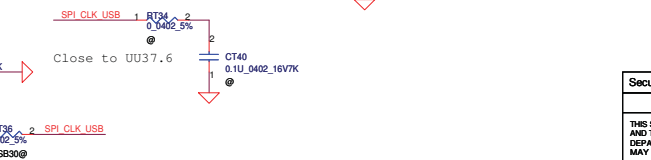
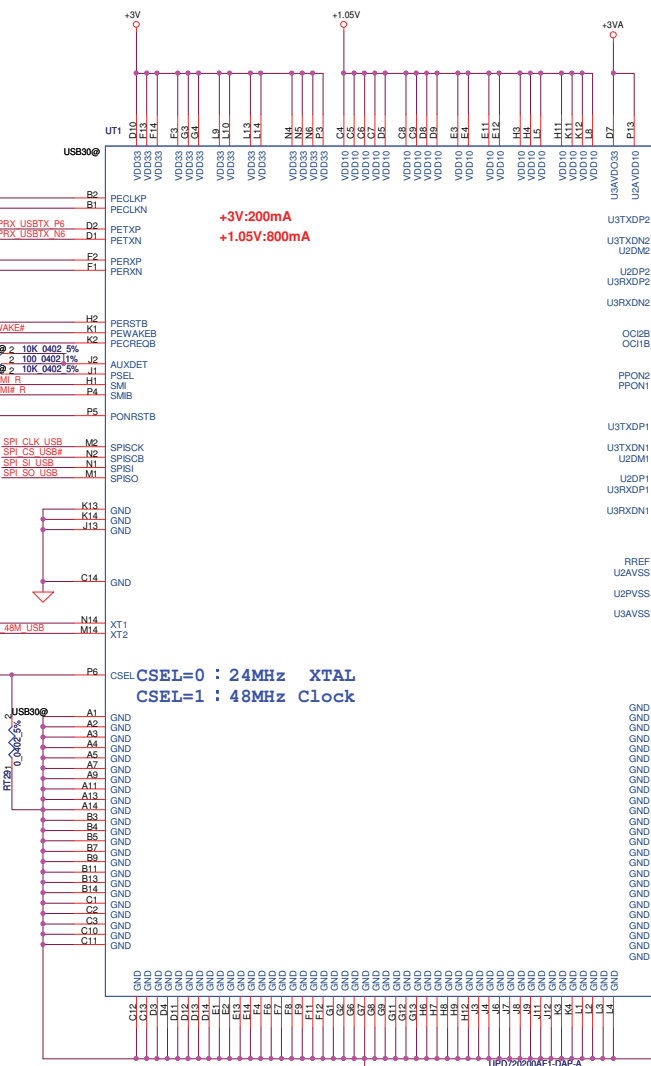
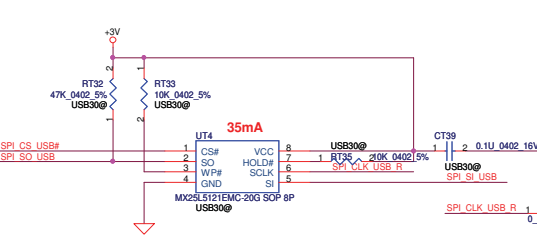
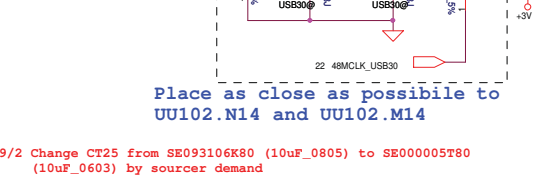
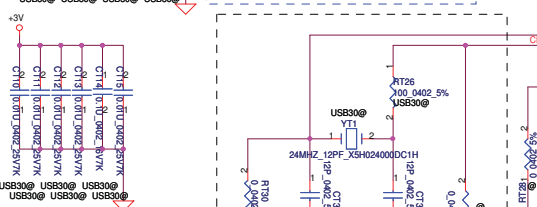
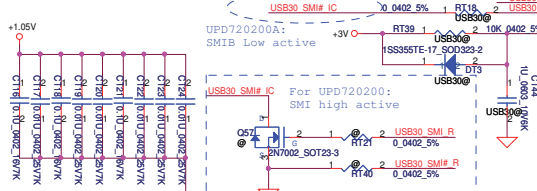
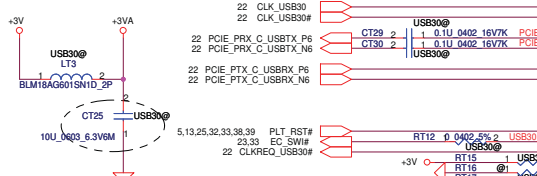
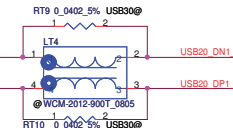
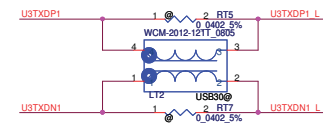
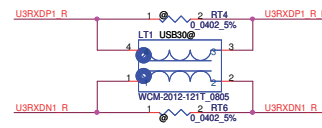
Close to U102.D7



Close to U102.P13

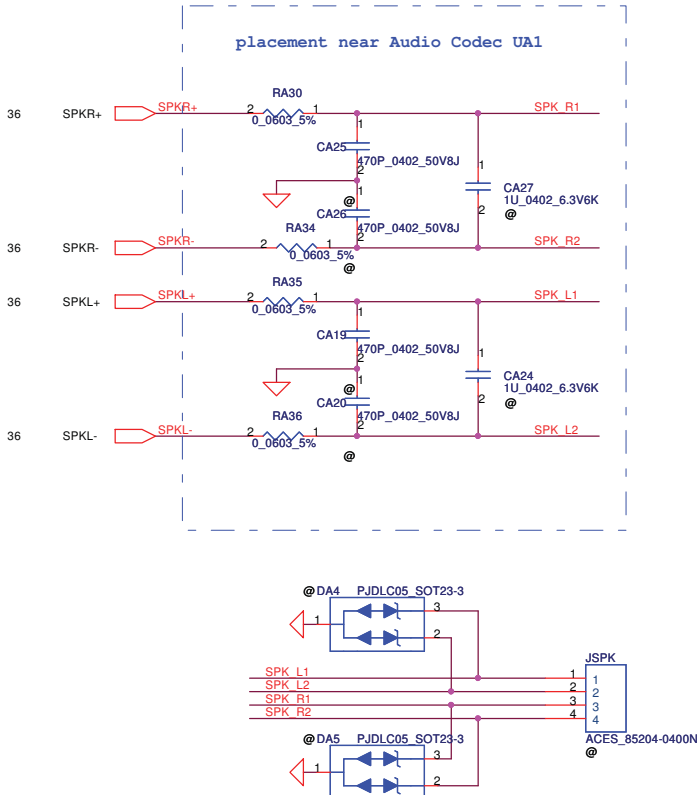


Follow Vendor recommend.



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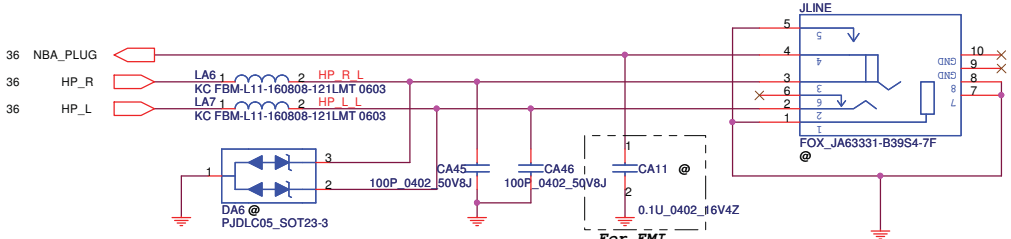
Speaker Connector



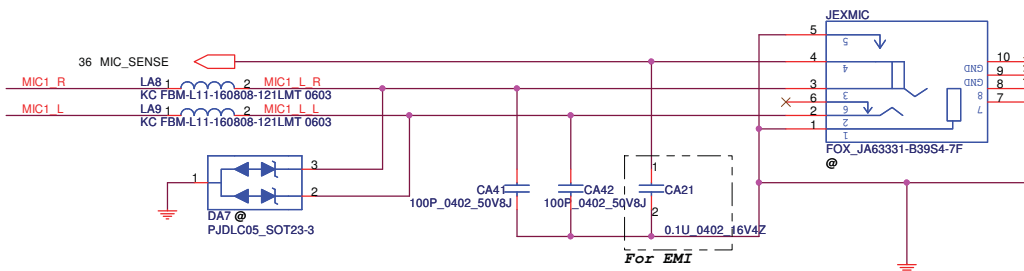
Ext. Mic



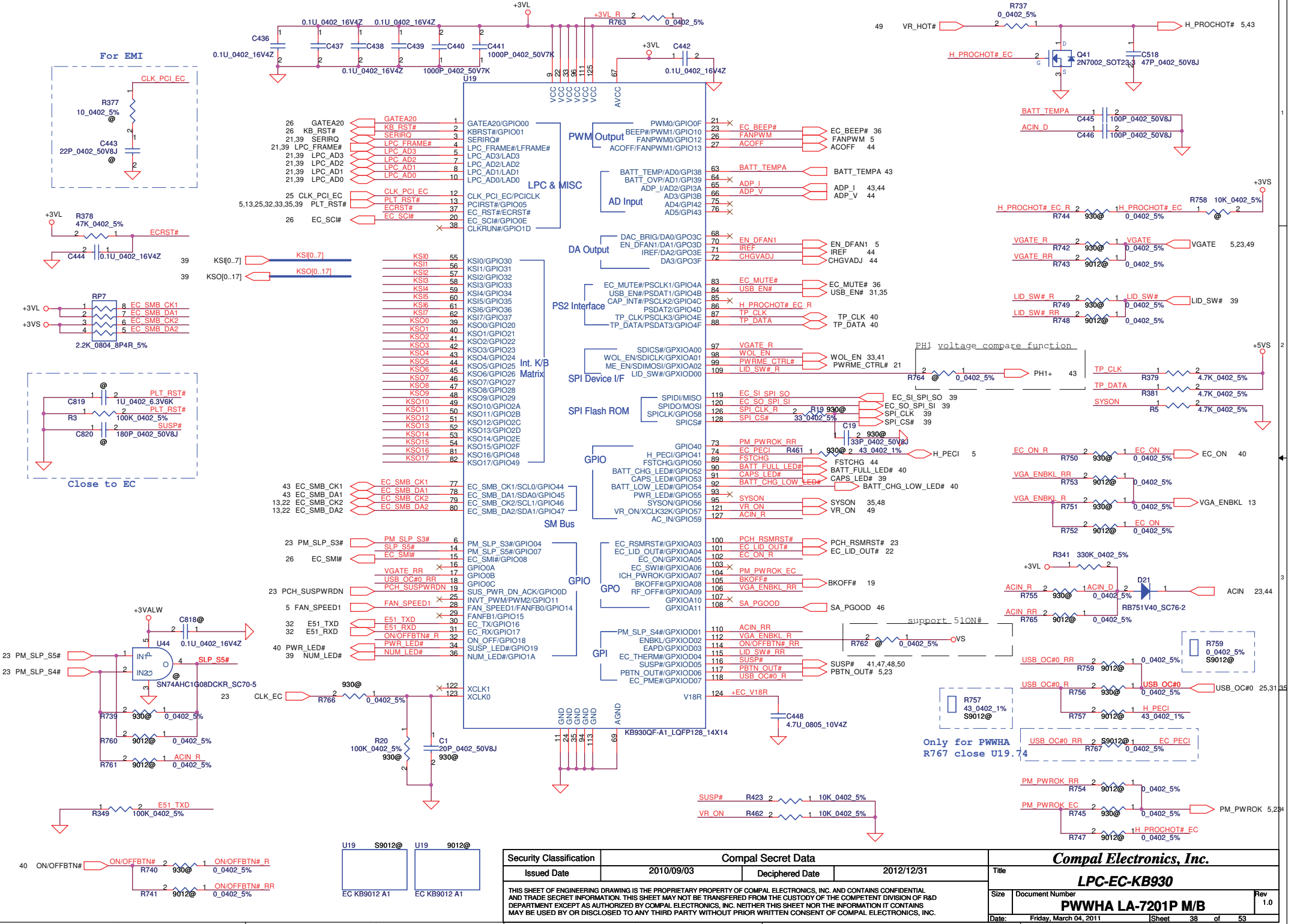
HeadPhone/LINE Out JACK



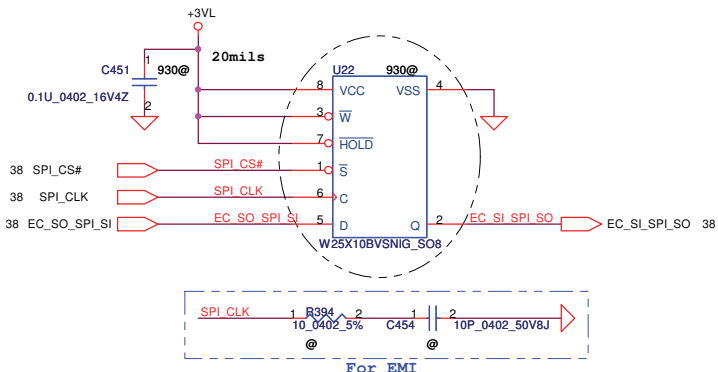
Ext.MIC/LINE IN JACK



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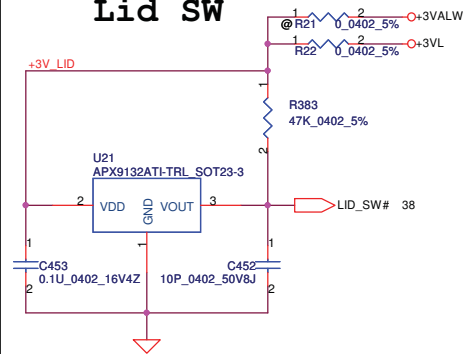
SPI Flash (256KB)



8/30 Change U22 From SA00003GK00 to SA00003GM10 due to EOL of SA00003GK00

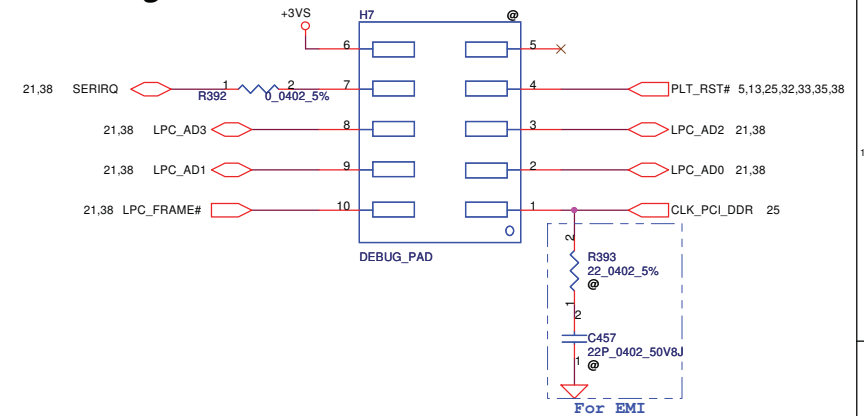
9/03 Change U22 change to SA00003FL10

Lid SW



LPC Debug Port

Place the PAD under DDR DIMM.



KEYBOARD CONN.

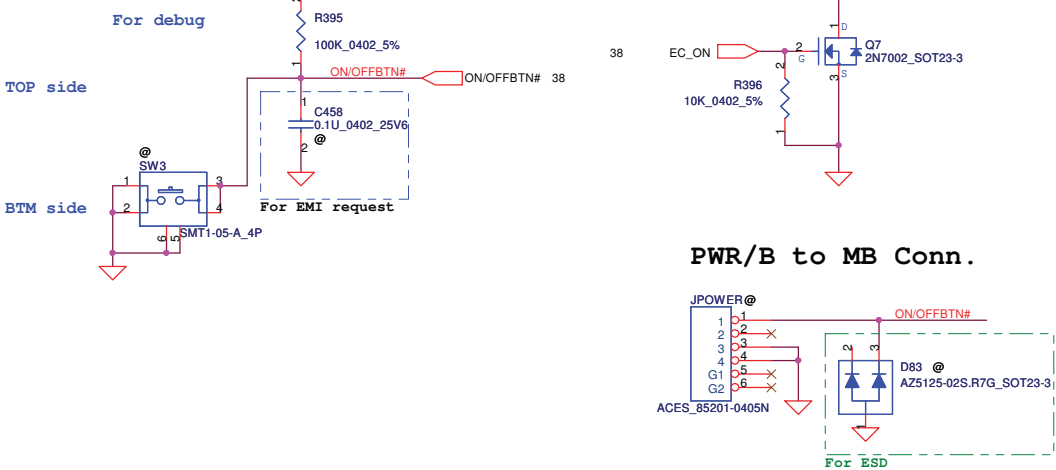
Noticed: KB Connector Pin Definition

Reversed with KB Membrane Pin Definition

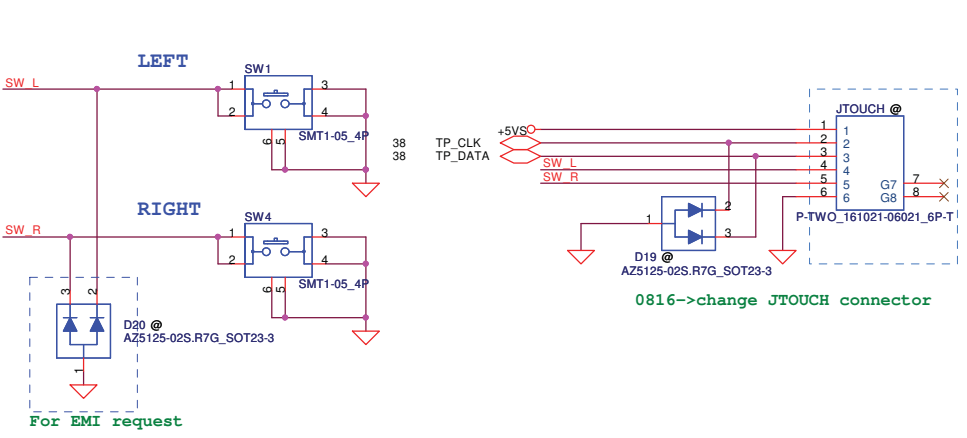


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				Size	Document Number	Rev
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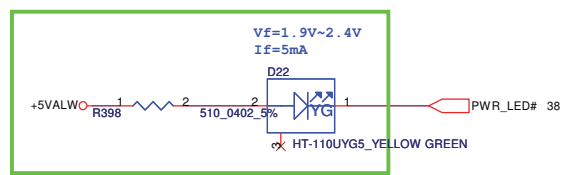
Power Button



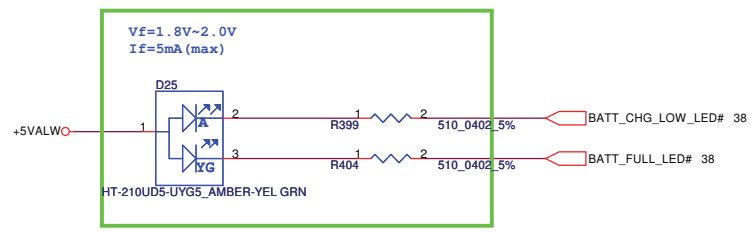
TP Button/Conn.



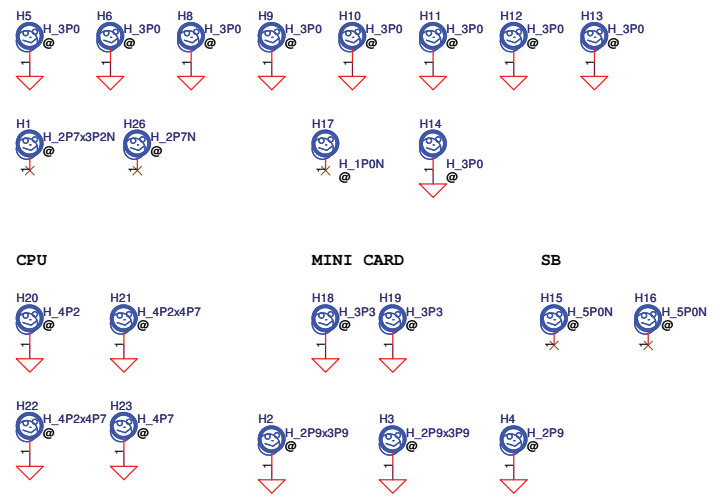
POWER/SUSPEND LED



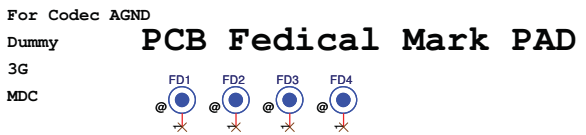
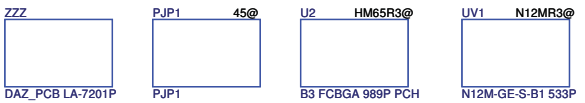
BATT CHARGE/FULL LED



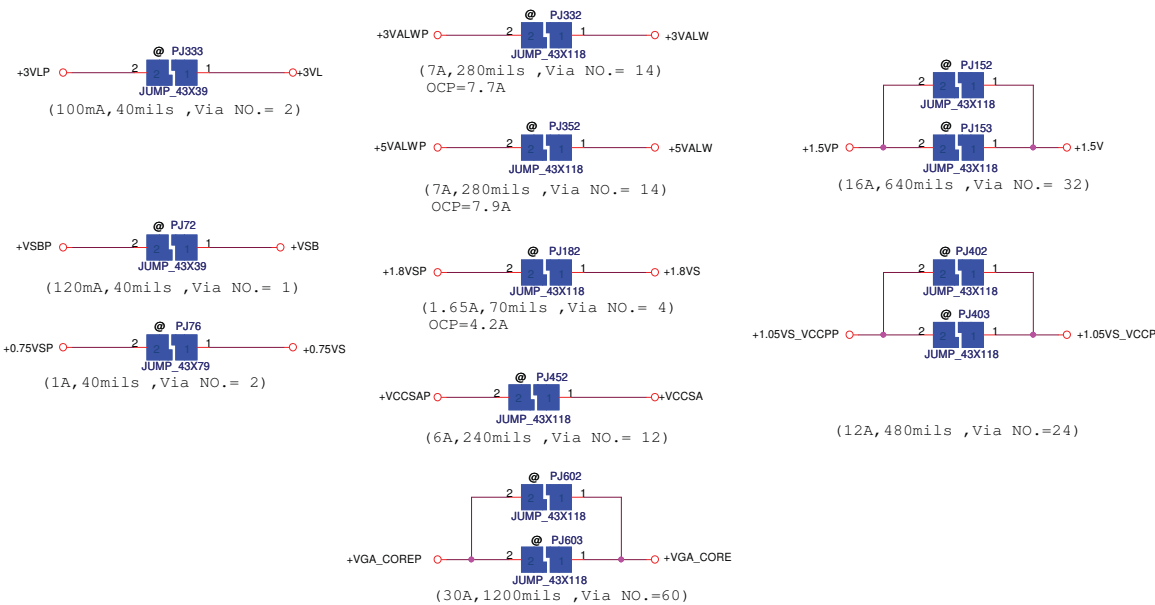
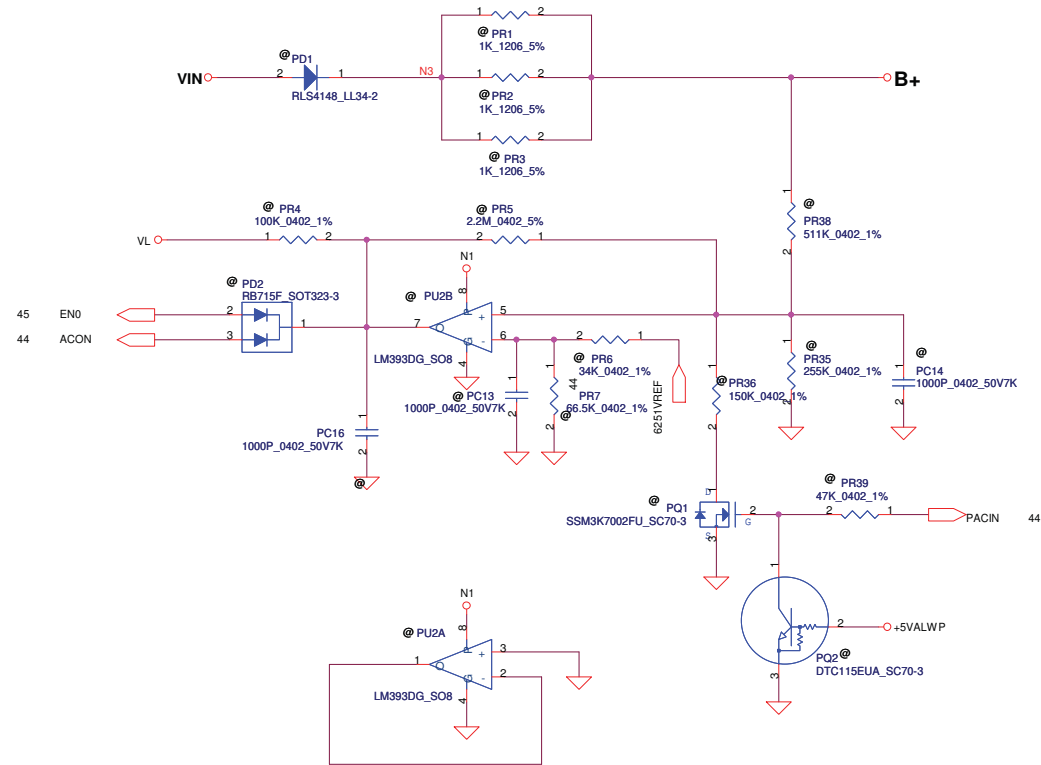
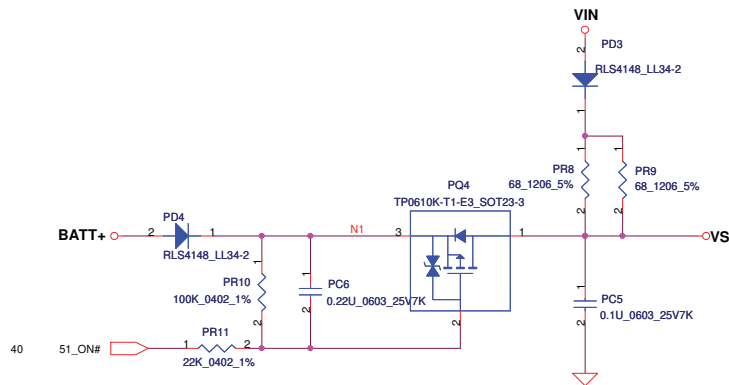
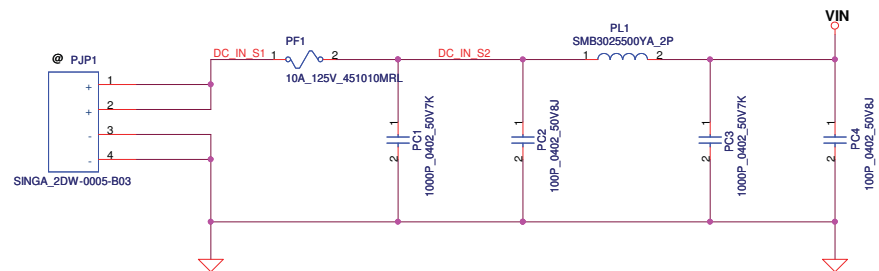
Screw Hole



ISPD



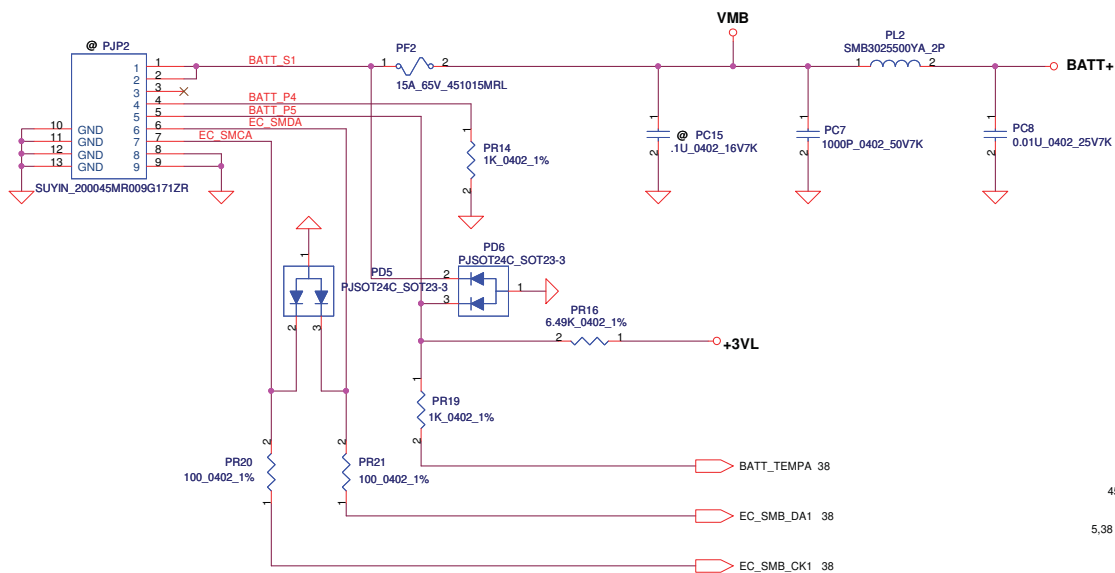
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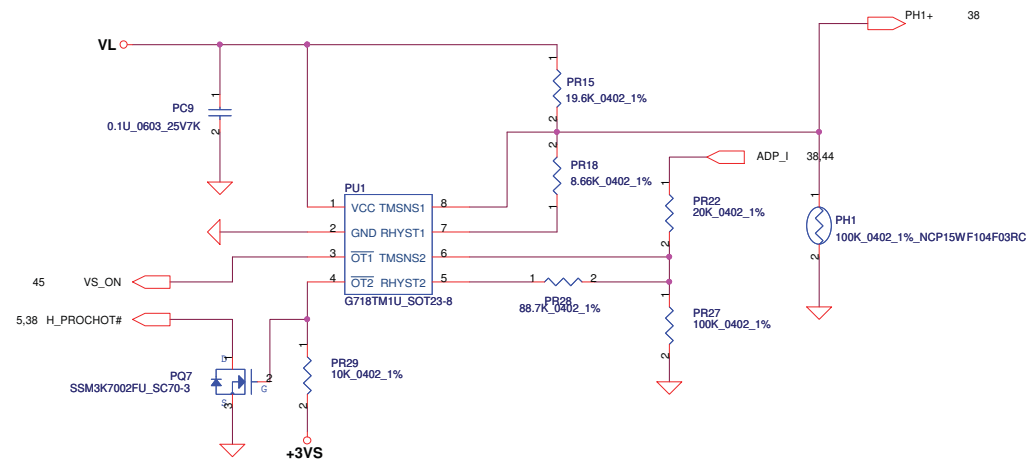
ACIN			
Precharge detector			
	Min.	typ.	Max.
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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2012/12/31				Title				DCIN/VIN DECTOR			
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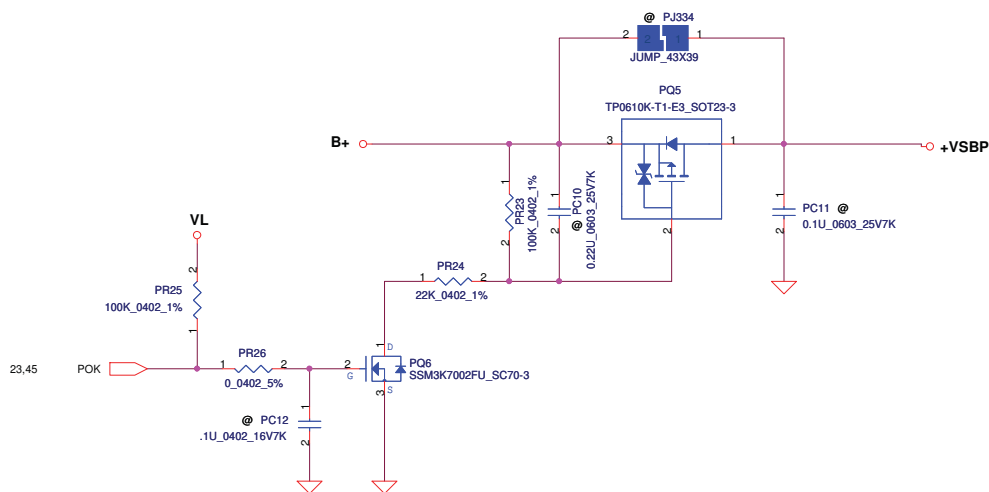
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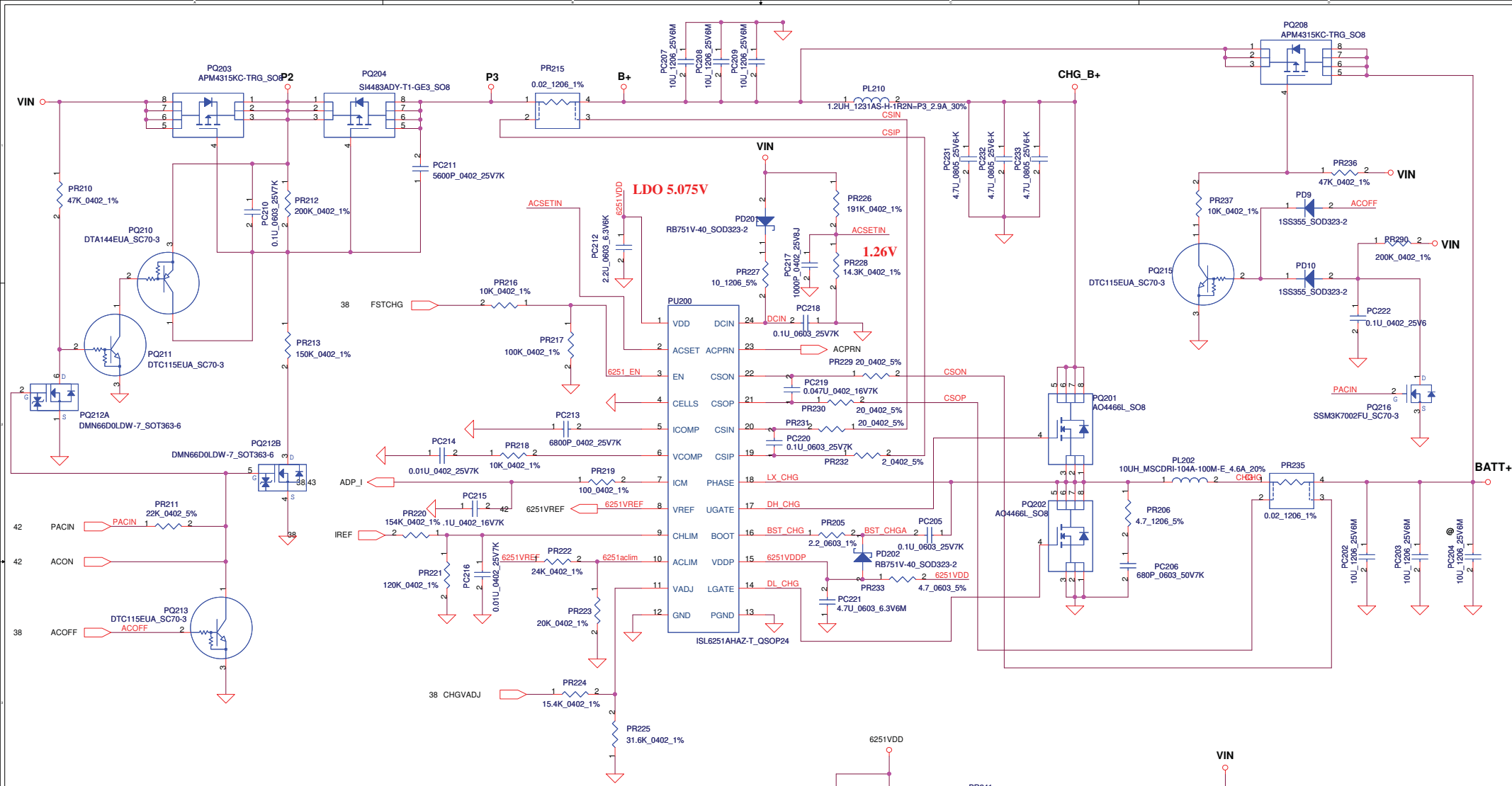


PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C



Adapter	Throttle Watt	Recovery Watt	Throttle Point	Recovery Point
65W_UMA	71.25W	62.4W	1.48V	1.308V
75W_DIS	85.5W	72W	1.78V	1.5V
75W_QCore	85.5W	72W	1.78V	1.5V



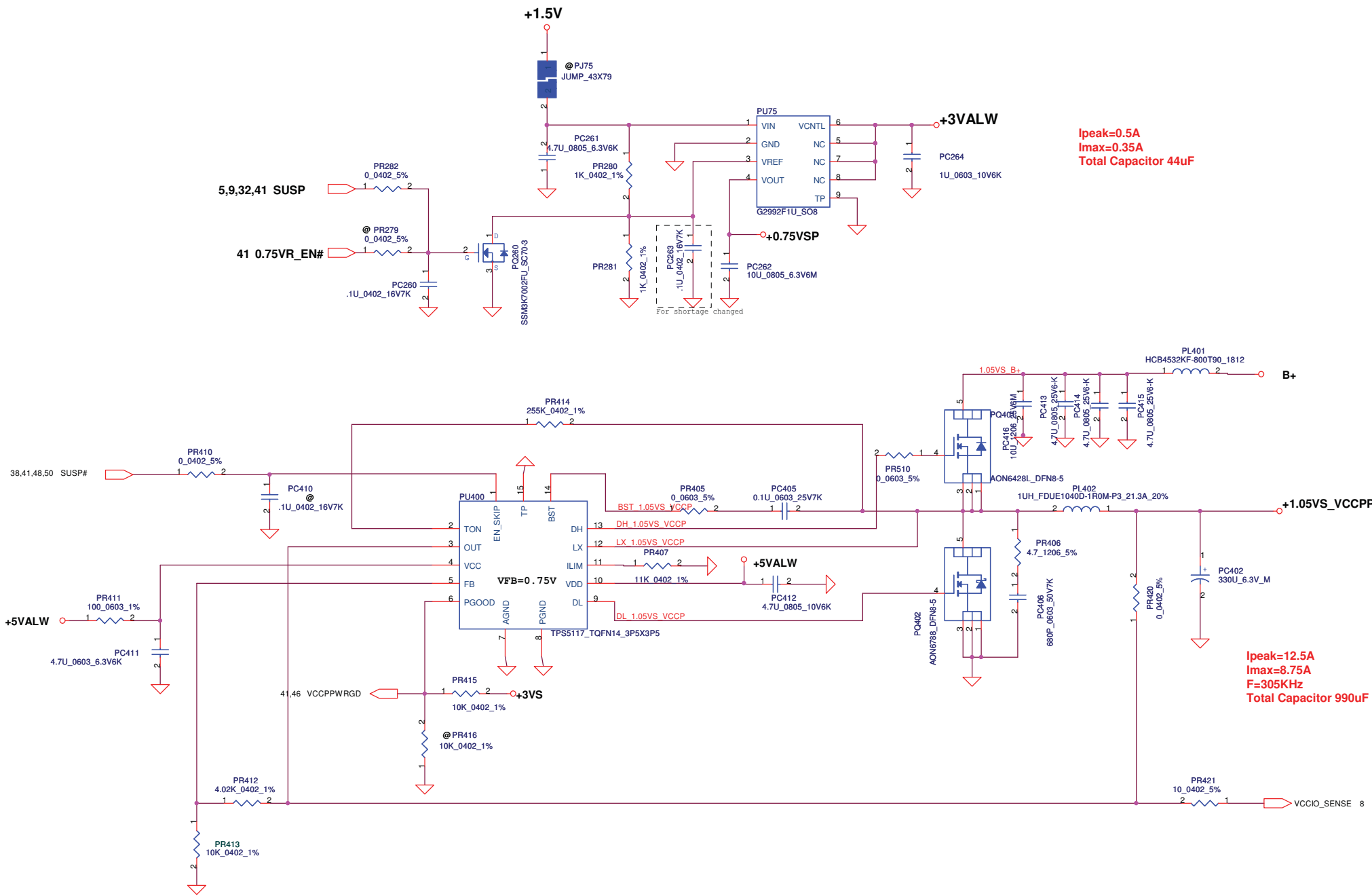


CC=0.25A~3A
 IREF=1.016*I_{charge}
 IREF=0.254V~3.048V
 VCHLIM need over 95mV

CHGVADJ=(V _{cell} -4)*9.445	
V _{cell}	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CP mode	
I _{ada} =0~3.42A (65W)	CP= 92%*I _{ada} ; CP=3.147A
V _{ac} lim=1.08V (65W)	PR222=75k PR223=20k PR215=0.02
I _{ada} =0~3.947A (75W)	CP= 92%*I _{ada} ; CP=3.63A
V _{ac} lim=0.736V (75W)	PR222=24k PR223=20k PR215=0.02

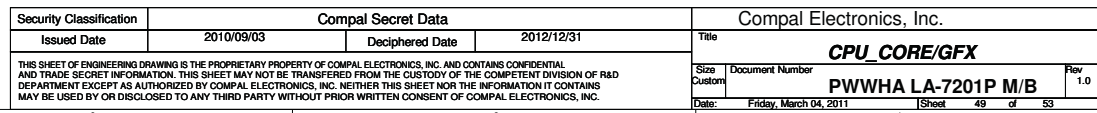
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Ipeak=0.5A
Imax=0.35A
Total Capacitor 44uF

Ipeak=12.5A
Imax=8.75A
F=305KHz
Total Capacitor 990uF

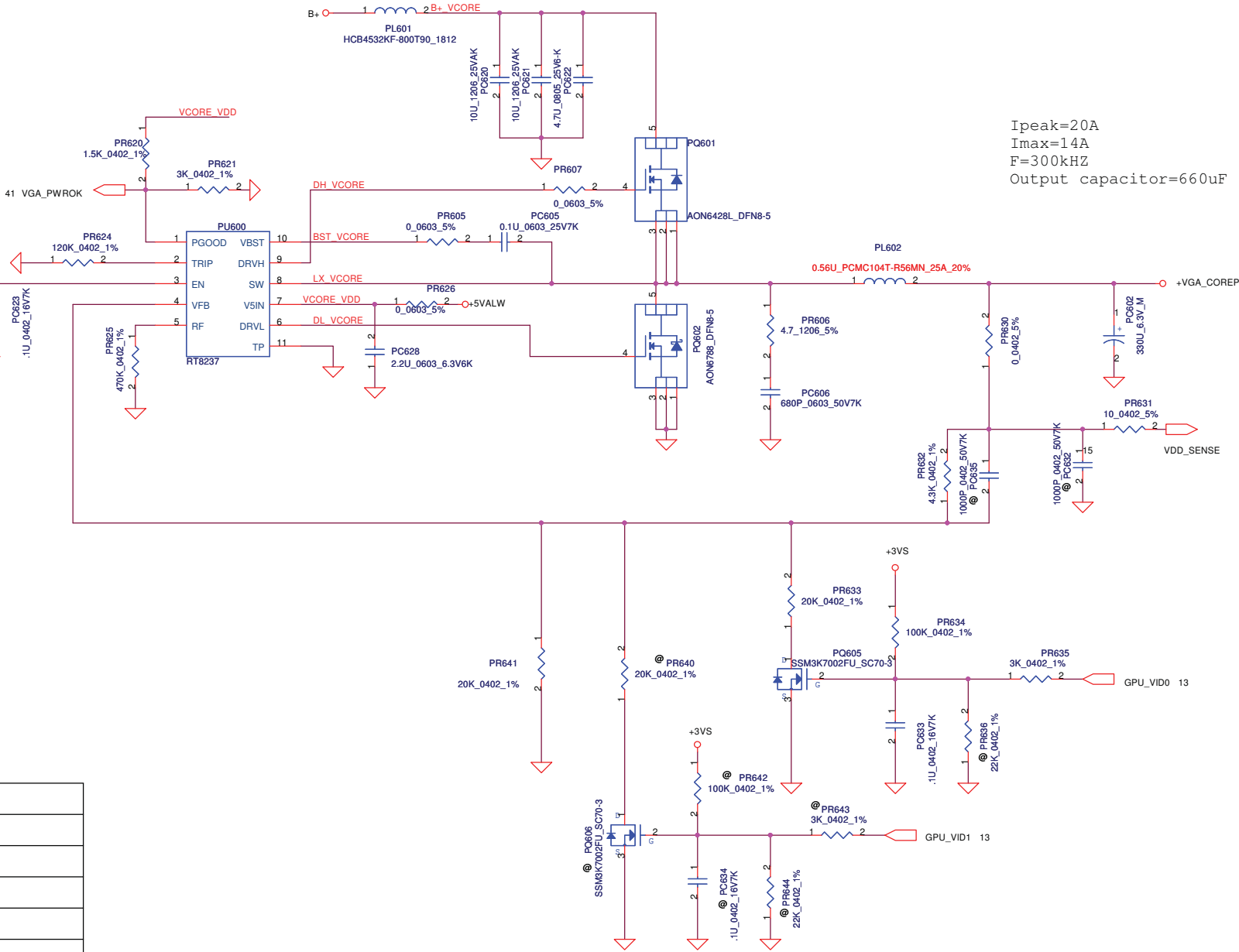
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PR625 = 470Kohm => FSW = 300KHZ
 PR625 = 200Kohm => FSW = 350KHZ
 PR625 = 100Kohm => FSW = 390KHZ
 PR625 = 47Kohm => FSW = 400KHZ

$VFB(0.7) = V_{out} \cdot R_{bottom} / (R_{top} + R_{bottom})$

Pstate	GPU_VID0	GPU_VID1	N12M-GE	
P8/P12	0	x	0.85V	
P0	1	x	1V	
	0	x		
P0(cold)	1	x	1V	
			PR632=4.3K PR633=20K PR641=20K	



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						Size		Document Number		Rev	
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	5		4		3		2		1				
	DATE	PAGE	MODIFICATION LIST					PURPOSE					
D	2010/12/31 (PVT)	P36 Charger	add snubber PR206,PC206					EMI command					
	2010/12/31 (PVT)	P36 Charger	change boost to 2.2 ohm PR205					EMI command					
	2010/12/31 (PVT)	P35 +3VALW/+5VALW	add snubber PR336,PC336,PR356,PC336					EMI command					
	2010/12/31 (PVT)	P37 +1.5VP/+1.8VSP	Change PR155,PR165 to 0 ohm					EMI command					
	2010/12/31 (PVT)	P37 +1.5VP/+1.8VSP	Change PQ151 to POK 5*6					EMI command					
C	2010/12/31 (PVT)	P37 +1.5VP/+1.8VSP	Reserve snubber PR156,PC156					EMI command					
	2010/12/31 (PVT)	P37 +1.5VP/+1.8VSP	add PC165 for MEI					EMI command					
	2010/12/31 (PVT)	P37 +VCCSA	add snubber PR456,PC456					EMI command					
	2010/12/31 (PVT)	P38 +1.05VS/+0.75	change PRQ401 to POK 5x6					EMI command					
	2010/12/31 (PVT)	P38 +1.05VS/+0.75	change PR405,PR510 to 0 ohm					EMI command					
	2010/12/31 (PVT)	P38 +1.05VS/+0.75	change 0.75V enable PR279 tp PR282					HW command					
	2010/12/31 (PVT)	P39 +CPU_CORE	change PC549,PC515,PC525 to correct rating					design change					
	2010/12/31 (PVT)	P39 +CPU_CORE	change PL503,PL504 to DCR 5%					design change					
	2010/12/31 (PVT)	P39 +CPU_CORE	change PC568 PC 566 to 5.8mmm capacitor					design change					
	2010/12/31 (PVT)	P39 +CPU_CORE	change PC551 for load line adjust					design change					
	2010/12/31 (PVT)	P39 +CPU_CORE	change PR560 for program temperture					design change					
	2010/12/31 (PVT)	P39 +CPU_CORE	change PC505,PQ503 change to POK5X6					design change					
	2010/12/31 (PVT)	P40+VGA_CORE	change PU600 to RT8237					design change					
	2010/12/31 (PVT)	P40+VGA_CORE	change PR605,PR607 to 0ohm					design change					
	2010/12/31 (PVT)	P40+VGA_CORE	change PR601 to POK 5X6					EMI command					
	2010/12/31 (PVT)	P40+VGA_CORE	change VID0 and VID1 compont chage					design change					
A	Security Classification		Compal Secret Data			Compal Electronics, Inc.							
	Issued Date		2010/09/03		Deciphered Date		2012/12/31		Title				
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						Size	Document Number						Rev
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Date:						Friday, February 25, 2011		Sheet 51 of 53					
	5		4		3		2		1				

HW PIR (Product Improve Record)

PWWHA LA-7201P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2010/10/29

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	10/29	17	SWAP FBA_CMD2 and FBA_CMD11	Schematic error
2	10/29	18	SWAP FBA_CMD18 and FBA_CMD11	Schematic error
3	10/29	21	Chane +3V_SPI to +3VS	Schematic error
4	10/29	22	Add R23 for CLK_REQ_VGA#	Reserve pull down for clock request

REVISION CHANGE: 0.2 TO 0.3

GERBER-OUT DATE: 2010/11/11

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	11/03	25,31	Add USB20_N9 & USB20_P9	Support Wimax
2	11/03	32	Co-Lay Giga LAN	Giga LAN support
3	11/22	22	Add R584 & R564 for Panel select	For HW common design
4	11/22	5	change D86 (SC100001M00)	For HW common design
5	11/22	5	cancel D85 @	For HW common design
6	11/24	32	LAN 8105E-VC update to 8105E-VL	For HW common design

PWWHA LA-7201P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.4 TO 0.6

GERBER-OUT DATE: 2011/01/18

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	01/15	14	Change RV48 BOM structure from @ to HDMI@.	For HDMI function
2	01/15	15	Add net name +IFPE_IOVDD & +IFPE_PLLVDD	For HDMI function
3	01/15	15	Add LV12,CV160,CV169,CV170,CV173,LV8,CV178,CV159,CV176,CV182,CV215	For HDMI function
4	01/15	38	Add U19 BOM symbol for 9012	For EC 9012
5	01/15	19	Change R120 from 10Kohm to 47Kohm.	For backlight PWM issue
6	01/15	35	Change UT2.6 & RT1 connector from +5VALW to +3V and del CT1.	For LDO leakage issue
7	01/15	41	Add Q31 BOM symbol and add BOM structure PS3@.	For power saving function
8	01/16	13	Change R25 BOM structure from @ to NHDMI@.	For HDMI function
9	01/16	38	Delete U19.123 CLK_EC_R net name	Due to duplicate net name
10	01/16	38	Change U19.104 & R745.2 & R747.2 net name from PM_PWROK_R to PM_PWROK_EC.	Due to duplicate net name
11	01/18	38	Add R757 & R759 & U19 BOM symbol and add BOM structure S9012@	For EC9012 solution
12	01/18	38	Add R767 and BOM structure S9012@	For EC9012 solution
13	01/19	21~29	Change U2 P/N from SA00003P440 to SA00004EE80.	For PCH P/N update
14	01/19	21~29	Change U2 BOM structure from Q65R3@ to HM65R1@.	For BOM structure update
15	01/19	40	Add U2 BOM symbol and BOM structure HM65R3@.	For BOM structure update
16	01/19	33	Change UL3 to SP050006E00	For EMI
17	01/20	5,7,9	Change C93,R312,U10,Q14,R465,R463,C140 BOM structure to PS3@	For BOM structure update
18	01/20	41	Change Q31 BOM symbol structure from PS3@ to @	Only for PWWHA DIS unmount
19	01/20	9	Change Q46,R449,C179,C472,R420,R455,Q33 BOM structure from @ to PS3@	Only for PWWHA DIS PS3@

PWWHA LA-7201P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.6 TO 0.7

GERBER-OUT DATE: 2011/02/18

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	01/31	5	Change JFAN2.2 connect FAN_SPEED1, JFAN2.3 connect GND	For FAN pin define modification
2	02/09	5,38	Change Q5,Q41 from SB570020110 to SB570020020	For common material

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HW PIR (Product Improve Record)

PWWHA LA-7201P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.6 TO 1.0
GERBER-OUT DATE: 2011/02/18

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	01/31	5	Change JFAN2.2 connect FAN_SPEED1, JFAN2.3 connect GND	For FAN pin define modification
2	02/09	5,38	Change Q5,Q41 from SB570020110 to SB570020020	For common material
3	02/17	5	Change C902,R1445,D85,D86,C900,C901,R1444 from mount to @.	For unused PWM FAN
4	02/17	5	Change R24 from @ to mount.	For use RPM FAN
5	02/17	40	Change R396,Q7 from 930@ to mount.	For EC9012 function
6	02/17	31	Add C363	For solving ODD issue
7	02/17	31	Change SW3 from mount to @	For MP phase
8	02/17	41	Change C496,C499,C236,C249,C255 from NLS@ to @	For low cost power switch
9	02/17	41	Change R415,R419 from 47Kohm to 0ohm	For low cost power switch
10	02/17	40	Change ZZZ P/N from DA60000L700 to DAZ0II00101	For MP phase
11	02/17	41	Change C252 from SE070104Z80 to SE071121J80	For low cost power switch
12	02/17	31	Change R561,R562,R457,Q53,R441,R440,C471,C217,Q45 from mount to ZODD@	For zero ODD function
13	02/18	21~29	Change U2 P/N from SA00004EE80 to SA00004EES0	For PCH B3 version
14	02/18	40	Change U2 P/N from SA00004EEA0 to SA00004EET0	For PCH B3 version
15	02/22	40	ADD UV1 BOM symbol and BOM structure N12MR3@.	For N12M R3 P/N
16	02/22	13~16	ADD UV1 BOM structure N12MR1@.	For N12M R1 P/N
17	02/23	32,35,41	Change Q50,Q53,QT3 from SB00000EO00 to SB00000EO10	For common material
18	02/23	41	Change C465,C467 BOM structure from OLS@ to always mount	For low cost power switch

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