BL5M Block Diagram

VCC_CORE

+1.5V

+1.05V

+1.25V

+1.8VSUS
+1.8V

+3VPCU
+3V_S5
+3VSUS
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF

HDMI CEC Page 19

HDMI Level Shift Page 21

CRT Page 20

INT MIC Page 19

LCD PANEL Page 19

Intel PENRYN uFCPGA Page 3,4

FSB(667/800MHZ)

CLOCK GENERATOR
CK505
ICS9LPR363
Page 2

SDVO

CRT

LVDS

NB CANTIGA Page 5,7,8,9,10,11

PCI-E 16X Lan

VGA CONNECTOR (FOX) Page 18

CRT

HDMI

LCD/LED

533/ 667 MHZ DDR II

DDRII-SODIMM1
DDRII-SODIMM2
Page 16, 17

SATA - HDD Page 22

SATA - ODD Page 22

SATA

SATA

DMI(x2/x4)

MINI CARD-3
UMA HD-DVD
Page 25

MINI CARD-4
ROBSON (FTB) Page 25

PCI-Express

PCIE-2

PCIE-4

PCIE-6

PCIE-3

PCIE-1

PCIE-5

MINI CARD-1
WLAN
Page 25

MINI CARD-2
UMA TV/ROBSON
Page 25

NEW CARD Page 27

LAN Connector Page 26

LAN/RJ11/RJ45/USB/RF DAUGHTER BOARD

Marvell LAN
10/100/Giga
88E8040T/88E8055

Transformer

RJ45

RJ11

USB

RF

DAUGHTER BOARD

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USB-0

Camera Page 19

USB-3

WLAN Page 25

USB-5

USB 2.0

SB ICH9M Page 12, 13, 14, 15

Azalia

PCI Bus

LPC

DAUGHTER BOARD

Finger Printer (FTB) Page 26

USB-1

Bluetooth Page 26

USB-2

New Card Page 27

USB-9

M/B USB2 Page 27

USB-7

DAUGHTER BOARD

Felica (FTB) Page 26

USB-4

M/B USB Page 27

USB-6

TV/ROBSON Page 25

USB-8

32.768KHz

WPC8763LDG Page 28

PCMCIA Controller (CB 1410) Page 23

Card Reader/1394 (OZ129T) Page 24

PCMCIA Page 23

5 IN 1 Page 24

1394 Page 24

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Key Board Page 26

FLASH ROM Page 28

CIR Page 28

G-Sensor Page 22

LED Board Page 26

Low Cost Board Page 26

MMB Board Page 26

Power Board Page 26

Touch Pad Board Page 26

DAUGHTER BOARD

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MIC JACK Page 30

INT SPK Page 29

SPK AMP Page 29

Reserve MIC Page 29

Reserve MIC Page 29

Port-A

Port-B

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Port-C

FM TUNER & MDC Page 29

Reserve FM Page 29

MDC Board

RJ11

Quanta Computer Inc.
PROJECT : BL5M Montevina

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Clock Generator

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA

11/01 Modify

10/30 Change Value and need change PN

	ICS9LPRS365 (ALPRS365K13)	RTM875T-606 (AL000875K06)	PULL HIGH	PULL DOWN
Pin 4	PCI2/TME	PCI2/TME internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 5	PCI-3	PCI-3/SRC5_EN internal PD	PIN37/38 IS SRC5	PIN37/38 IS PCI_STOP/CPU_STOP (default)
Pin 6	PCI-4/27M_SEL	PCI-4/27M_SEL internal PD	PIN 17/18 IS 27MHz	PIN 17/18 IS SRC/DOT (default)
Pin 7	PCIF-5/ITP_EN	PCIF-5/ITP_EN internal PD	PIN 46/47 IS CPUITP	PIN 46/47 IS SRC8 (default)

<MAIN>:ICS9LPRS365BGLFT QCI:ALPRS365K13
<SECOND>:SLG8SP512TTR: QCI:AL8SP512K05

To SB
To CPU
To NB
To MINI3
To NB
To New Card
To MINI2
To WLAN
To LAN
To SB
To SB
To NB
To NB
To VGA Card

FREQ. SEL TABLE

BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Clock Gen I2C

11/01 Del C3195

Quanta Computer Inc.
PROJECT : BL5M Montevina

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	CLK. GEN./ CK505	1A

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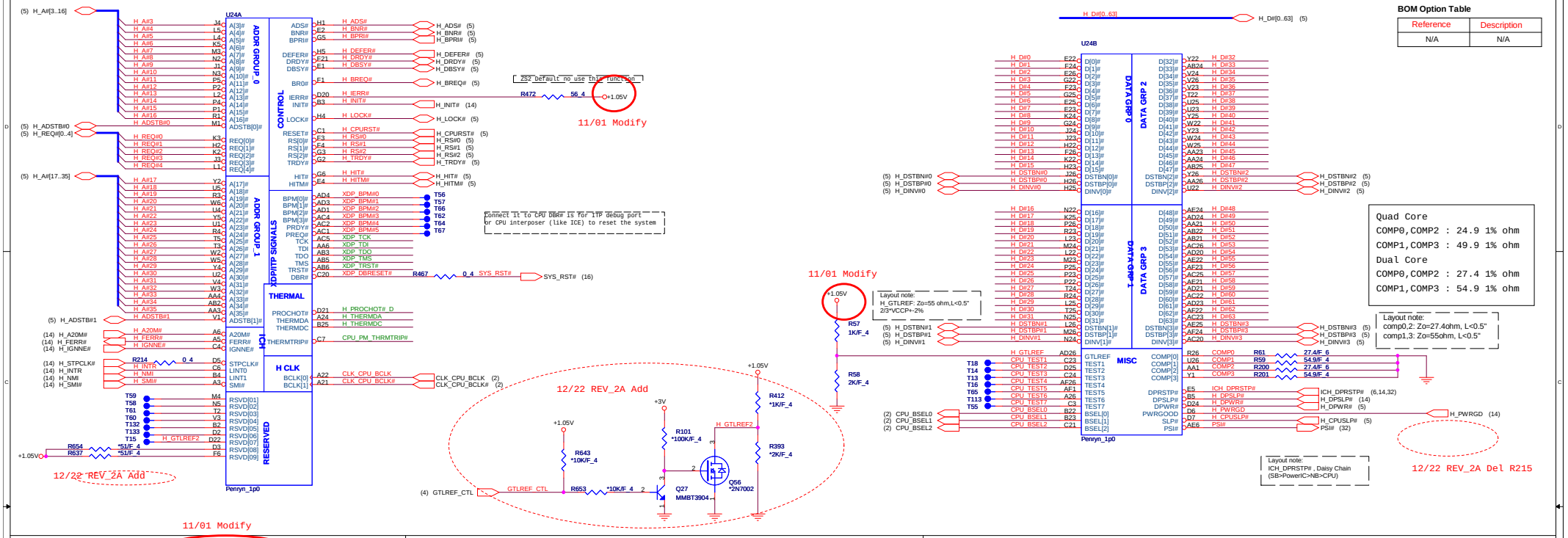
BOM Option Table
Reference
Description
N/A
N/A
U24A
U24B
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
Penryn_1p0
R472 56_4 +1.05V
11/01 Modify
2S2 Default no use this function
Connect it to CPU DBR# is for ITP debug port or CPU interposer (like ICE) to reset the system
R467 0_4 SYS_RST#
SYS_RST# (16)
12/22 REV_2A Add
12/22 REV_2A Del R215
Layout note: H_GTLREF: Zo=55 ohm,L<0.5" 2/3*VCCP+-2%
R57 1K/F_4
R58 2K/F_4
Quad Core
COMP0,COMP2 : 24.9 1% ohm
COMP1,COMP3 : 49.9 1% ohm
Dual Core
COMP0,COMP2 : 27.4 1% ohm
COMP1,COMP3 : 54.9 1% ohm
Layout note: comp0,2: Zo=27.4ohm, L<0.5" comp1,3: Zo=55ohm, L<0.5"
Layout note: ICH_DPRSTP# : Daisy Chain (SB>PowerIC>NB>CPU)
12/22 REV_2A Add
R643 *10K/F_4
R653 *10K/F_4
R101 *100K/F_4
R412 *1K/F_4
R393 *2K/F_4
Q27 MMBT3904
Q56 *2N7002
GTLREF_CTL
H_GTLREF2
Thermal Trip
11/01 Modify
Q41 FDV301N
R466 *10K_4
D30 *BAS316
R473 1K_4
R462 100K_6
R478 56.2/F_4
Q40 MMBT3904
10/23 Add
R475 *0_4 PM_THRMTRIP#
SYS_SHDN# (31)
PM_THRMTRIP# (6,14)
No use Thermal trip CPU side still PU 56ohm. Use Thermal trip can share PU at SB side
XDP
11/01 Modify
R213 *51/F_4
H_CPURST#
12/22 REV_2A Del R212
Reserve 1K for XDP function
XDP_TDO R199 *51/F_4
XDP_TDI R197 56_4
XDP_TMS R203 54.9/F_4
XDP_TCK R196 56_4
XDP_TRST# R202 56_4
CPU Thermal monitor
Q38 RHU002N06
Q37 RHU002N06
2ND_MBCLK#
2ND_MBDATA#
R446 10K_4
R444 10K_4
R456 200_6
C428 0.1u/10V_4
U22
*MAX6657
ADDRESS: 98H
C430 2200p/50V_4
H_THERMDA
H_THERMDC
NS LM95245 PU this pin
R442 10K_4
R443 *0_4
R453 10K_4
R451 330_4
THERM_ALERT#_R
THER_SHD#
Q39 MMBT3904
U21
LM95245
NS LM95245 : AL095245000
SCMC EMC1402 : AL001402000
CPU FAN CTRL
10/30 Add ESD solution.
10/14 Change reference to follow BL5S
U1 G995
C11 2.2u/6.3V_6
R7 0_4
C416 10u/10V_8
C417 0.01u/16V_4
C415 *0.01u/16V_4
D29 VPORT_6
D3 VPORT_6
*VPORT_6
D4
R435 10K_4
CN17 FAN_CON
TH_FAN_POWER
FANSIG
SYSFANON#
VFAN
12/18 REV_2A R415 DNI
Processor hot
11/01 Modify
R468 56_4
R465 *2.2K_4
R461 *0_4
H_PROCHOT#_D
H_PROCHOT# (32)
No use PROCHOT CPU side still PU 56ohm. Use PROCHOT to optional receiver CPU side PU 68ohm and through isolat 2.2K ohm to receiver side
Quanta Computer Inc.
PROJECT : BL5M Montevina
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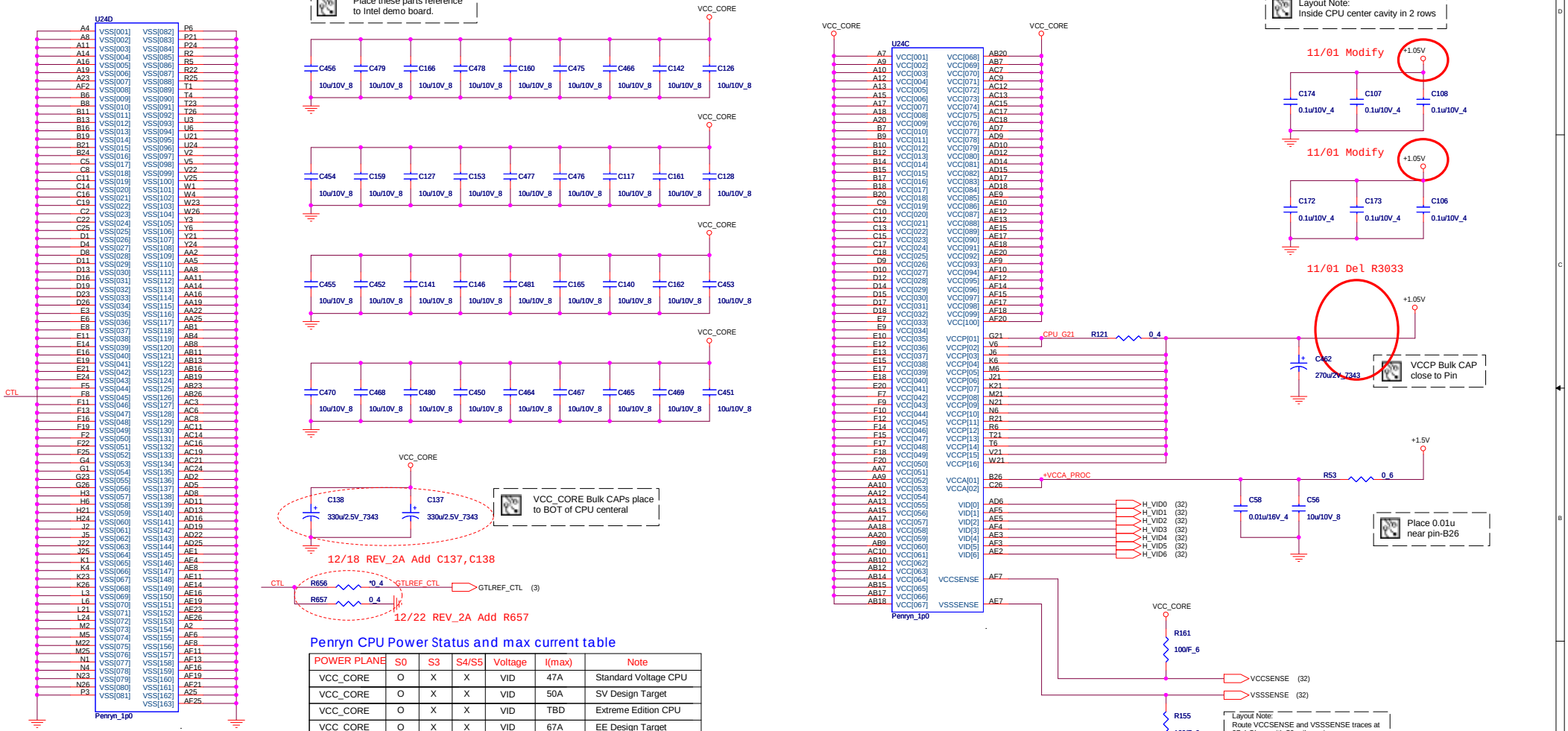
BOM Option Table

Reference	Description
N/A	N/A

Need NC 20PCS 10u before A1 BOM released(A0 all stuff)



Penryn CPU Power Status and max current table

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC_CORE	O	X	X	VID	47A	Standard Voltage CPU
VCC_CORE	O	X	X	VID	50A	SV Design Target
VCC_CORE	O	X	X	VID	TBD	Extreme Edition CPU
VCC_CORE	O	X	X	VID	67A	EE Design Target
VCCA	O	X	X	+1.5V	130mA	
VCCP	O	X	X	+1.05V	4.5A	Before VCC Stable
VCCP	O	X	X	+1.05V	2.5A	After VCC Stable

(See Penryn EMTS Rev:1.0 Table7,8 for voltage and current)

(See Penryn EMTS Rev:1.0 Table-3 for VID table)

Quanta Computer Inc.

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BOM Option Table

Reference	Description
N/A	N/A

11/01 Modify

+1.05V
R441 221/F_4
H_SWING
R440 100/F_4
C423 0.1u/10V_4
0.3125*VCCP
W:10,S:20 , L<0.5"

W:10,S:20 , L<0.5"
H_RCOMP
R45 24.9/F_4

11/01 Modify

+1.05V
R447 1K/F_4
H_AVREF
R448 2K/F_4
R449 0_4 H_DVREF
2/3*VCCP
W:10,S:20 , L<0.5"

U23A

(3) H_D#[63..0]

H_D#0	F2	H_D#_0
H_D#1	G8	H_D#_1
H_D#2	F8	H_D#_2
H_D#3	E6	H_D#_3
H_D#4	G2	H_D#_4
H_D#5	H6	H_D#_5
H_D#6	H2	H_D#_6
H_D#7	F6	H_D#_7
H_D#8	D4	H_D#_8
H_D#9	H3	H_D#_9
H_D#10	M9	H_D#_10
H_D#11	M11	H_D#_11
H_D#12	J1	H_D#_12
H_D#13	J2	H_D#_13
H_D#14	N12	H_D#_14
H_D#15	J6	H_D#_15
H_D#16	P2	H_D#_16
H_D#17	L2	H_D#_17
H_D#18	R2	H_D#_18
H_D#19	N9	H_D#_19
H_D#20	L6	H_D#_20
H_D#21	M5	H_D#_21
H_D#22	J3	H_D#_22
H_D#23	N2	H_D#_23
H_D#24	R1	H_D#_24
H_D#25	N5	H_D#_25
H_D#26	N6	H_D#_26
H_D#27	P13	H_D#_27
H_D#28	N8	H_D#_28
H_D#29	L7	H_D#_29
H_D#30	N10	H_D#_30
H_D#31	M3	H_D#_31
H_D#32	Y3	H_D#_32
H_D#33	AD14	H_D#_33
H_D#34	Y6	H_D#_34
H_D#35	Y10	H_D#_35
H_D#36	Y12	H_D#_36
H_D#37	Y14	H_D#_37
H_D#38	Y7	H_D#_38
H_D#39	W2	H_D#_39
H_D#40	AA8	H_D#_40
H_D#41	Y9	H_D#_41
H_D#42	AA13	H_D#_42
H_D#43	AA9	H_D#_43
H_D#44	AA11	H_D#_44
H_D#45	AD11	H_D#_45
H_D#46	AD10	H_D#_46
H_D#47	AD13	H_D#_47
H_D#48	AE12	H_D#_48
H_D#49	AE9	H_D#_49
H_D#50	AA2	H_D#_50
H_D#51	AD8	H_D#_51
H_D#52	AA3	H_D#_52
H_D#53	AD3	H_D#_53
H_D#54	AD7	H_D#_54
H_D#55	AE14	H_D#_55
H_D#56	AF3	H_D#_56
H_D#57	AC1	H_D#_57
H_D#58	AE3	H_D#_58
H_D#59	AC3	H_D#_59
H_D#60	AE11	H_D#_60
H_D#61	AE8	H_D#_61
H_D#62	AG2	H_D#_62
H_D#63	AD6	H_D#_63

H_SWING	C5	H_SWING
H_RCOMP	E3	H_RCOMP

(3) H_CPURST#
(3) H_CPUSLP#

H_CPURST#	C12	H_CPURST#
H_CPUSLP#	E11	H_CPUSLP#

H_AVREF	A11	H_AVREF
H_DVREF	B11	H_DVREF

HOST

CANTIGA_1p2

H_A#[35..3] (3)

H_A#_3	A14	H_A#3
H_A#_4	C15	H_A#4
H_A#_5	F16	H_A#5
H_A#_6	H13	H_A#6
H_A#_7	C18	H_A#7
H_A#_8	M16	H_A#8
H_A#_9	J13	H_A#9
H_A#_10	P16	H_A#10
H_A#_11	R16	H_A#11
H_A#_12	N17	H_A#12
H_A#_13	M13	H_A#13
H_A#_14	E17	H_A#14
H_A#_15	P17	H_A#15
H_A#_16	E17	H_A#16
H_A#_17	G20	H_A#17
H_A#_18	B19	H_A#18
H_A#_19	J16	H_A#19
H_A#_20	E20	H_A#20
H_A#_21	H16	H_A#21
H_A#_22	J20	H_A#22
H_A#_23	L17	H_A#23
H_A#_24	A17	H_A#24
H_A#_25	B17	H_A#25
H_A#_26	L16	H_A#26
H_A#_27	C21	H_A#27
H_A#_28	J17	H_A#28
H_A#_29	H20	H_A#29
H_A#_30	B18	H_A#30
H_A#_31	K17	H_A#31
H_A#_32	B20	H_A#32
H_A#_33	F21	H_A#33
H_A#_34	K21	H_A#34
H_A#_35	L20	H_A#35

H_ADS#	H12	H_ADS#	H_ADS# (3)
H_ADSTB#_0	B16	H_ADSTB#0	H_ADSTB#0 (3)
H_ADSTB#_1	G17	H_ADSTB#1	H_ADSTB#1 (3)
H_BNR#	A9	H_BNR#	H_BNR# (3)
H_BPRI#	F11	H_BPRI#	H_BPRI# (3)
H_BREQ#	G12	H_BREQ#	H_BREQ# (3)
H_DEFER#	E9	H_DEFER#	H_DEFER# (3)
H_DBSY#	B10	H_DBSY#	H_DBSY# (3)
HPLL_CLK	AH7	CLK_MCH_BCLK	CLK_MCH_BCLK (2)
HPLL_CLK#	AH6	CLK_MCH_BCLK#	CLK_MCH_BCLK# (2)
H_DPWR#	J11	H_DPWR#	H_DPWR# (3)
H_DRDY#	E9	H_DRDY#	H_DRDY# (3)
H_HIT#	H9	H_HIT#	H_HIT# (3)
H_HITM#	E12	H_HITM#	H_HITM# (3)
H_LOCK#	H11	H_LOCK#	H_LOCK# (3)
H_TRDY#	C9	H_TRDY#	H_TRDY# (3)

H_DINV#[3..0] (3)

H_DINV#_0	J8	H_DINV#0
H_DINV#_1	L3	H_DINV#1
H_DINV#_2	Y13	H_DINV#2
H_DINV#_3	Y1	H_DINV#3

H_DSTBN#[3..0] (3)

H_DSTBN#_0	L10	H_DSTBN#0
H_DSTBN#_1	M7	H_DSTBN#1
H_DSTBN#_2	AA5	H_DSTBN#2
H_DSTBN#_3	AE6	H_DSTBN#3

H_DSTBP#[3..0] (3)

H_DSTBP#_0	L9	H_DSTBP#0
H_DSTBP#_1	M8	H_DSTBP#1
H_DSTBP#_2	AA6	H_DSTBP#2
H_DSTBP#_3	AE5	H_DSTBP#3

H_REQ#[4..0] (3)

H_REQ#_0	B15	H_REQ#0
H_REQ#_1	K13	H_REQ#1
H_REQ#_2	F13	H_REQ#2
H_REQ#_3	B13	H_REQ#3
H_REQ#_4	B14	H_REQ#4

H_RS#[2..0] (3)

H_RS#_0	B6	H_RS#0
H_RS#_1	F12	H_RS#1
H_RS#_2	C8	H_RS#2

Quanta Computer Inc.
PROJECT : BL5M Montevina

Size	Document Number	Rev
	CLK. GEN./ CK505	1A

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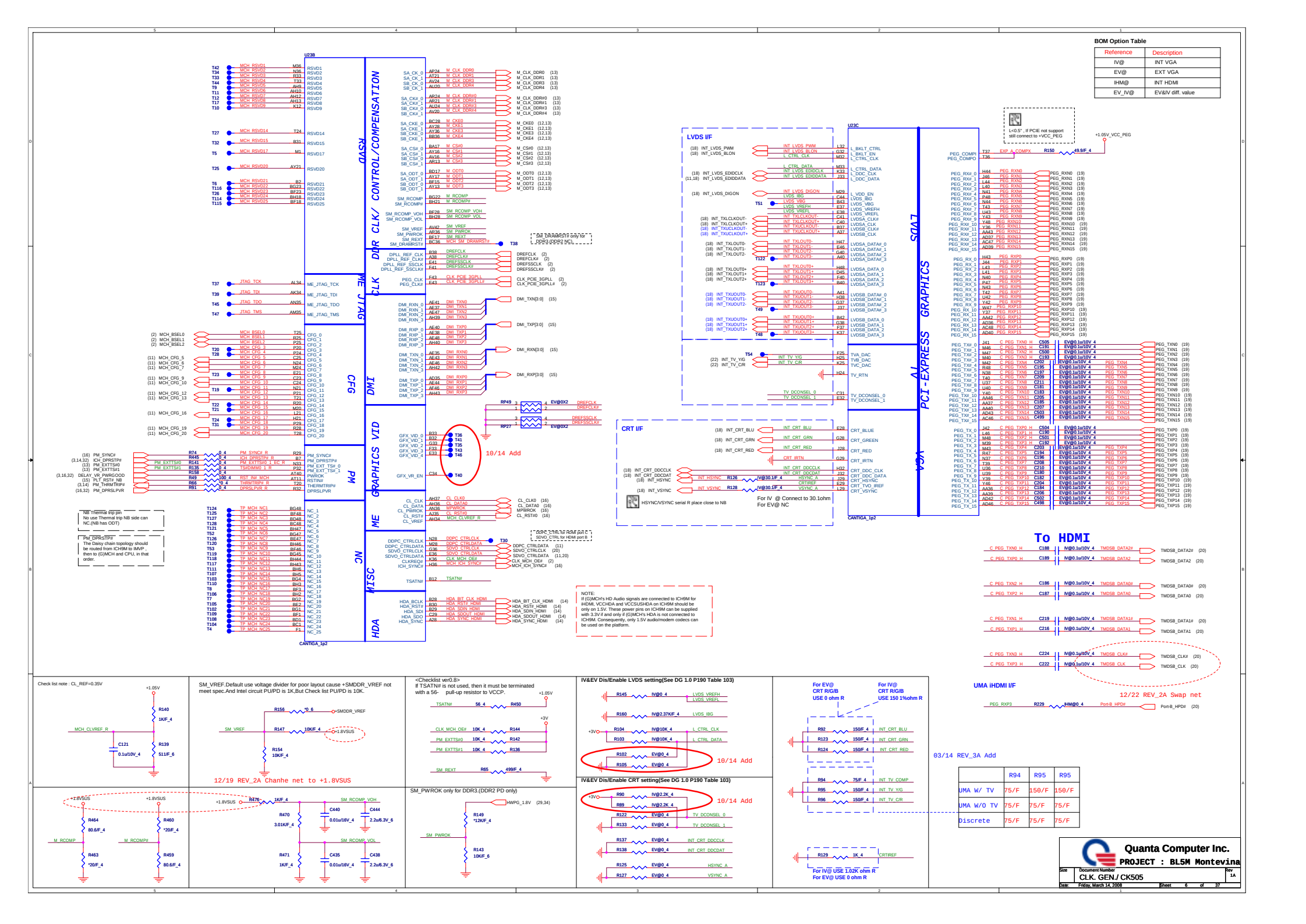
BOM Option Table

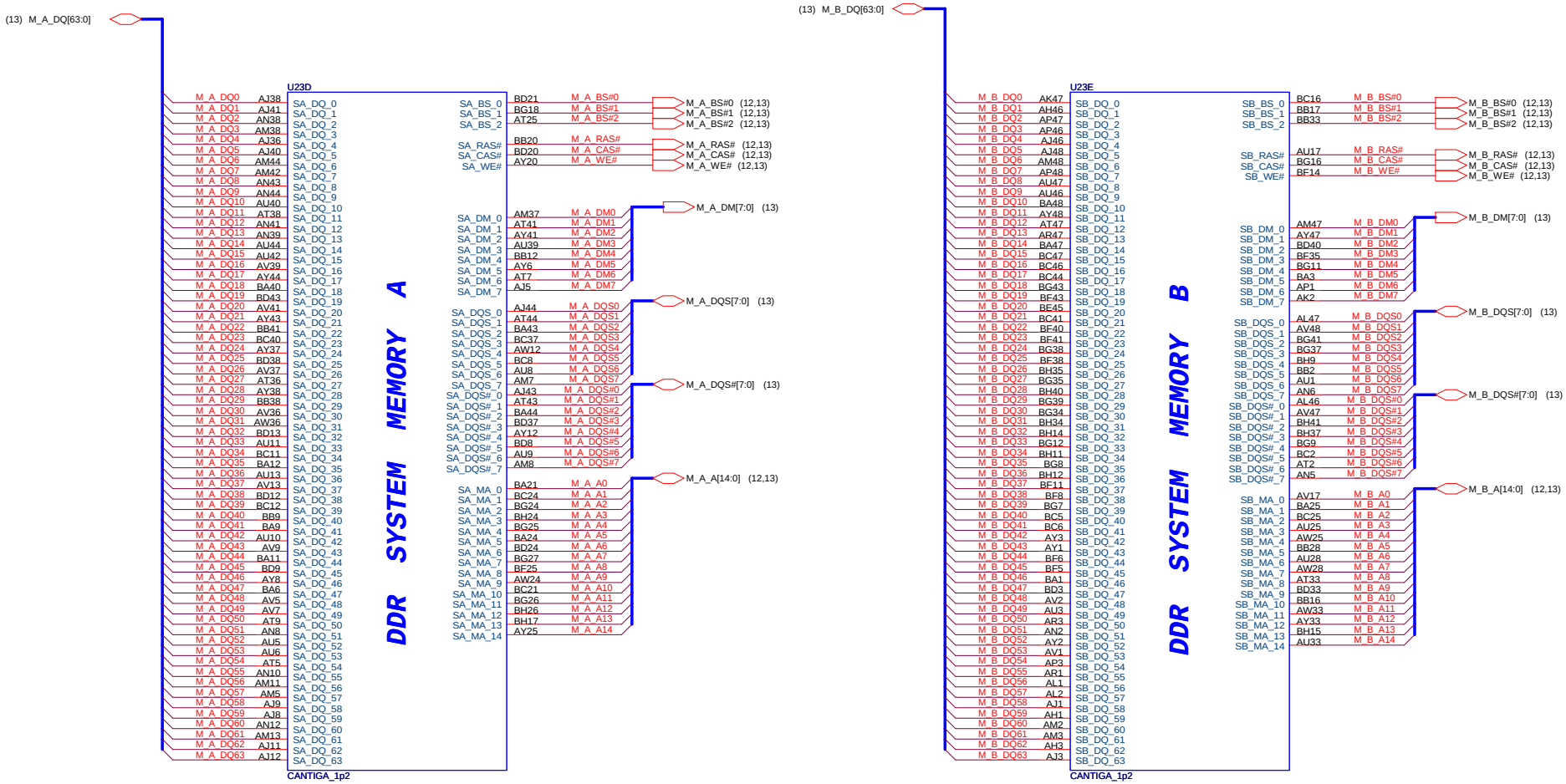
Reference	Description
IV@	INT VGA
EV@	EXT VGA
IHM@	INT HDMI
EV_IV@	EV&IV diff. value



	R94	R95	R95
UMA W/ TV	75/F	150/F	150/F
UMA W/O TV	75/F	75/F	75/F
Discrete	75/F	75/F	75/F

BOM Option Table

Reference	Description
N/A	N/A



Quanta Computer Inc.

PROJECT : BL5M Montevina

Size	Document Number	Rev
	CLK. GEN./ CK505	1A

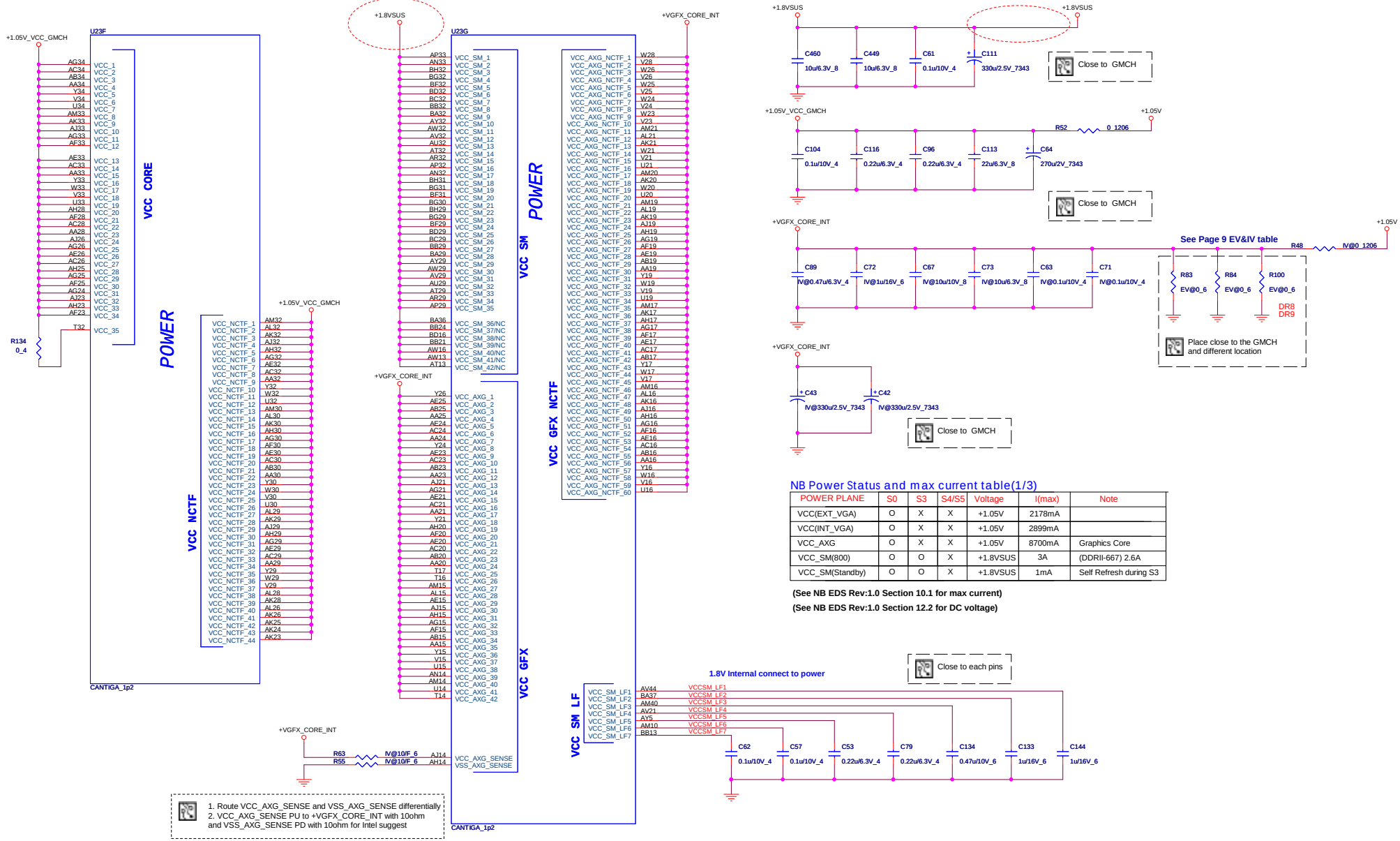
Date: Monday, March 10, 2008 Sheet 7 of 37

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA

12/19 REV_2A Chanhe net to +1.8VSUS

12/19 REV_2A Del R101



NB Power Status and max current table(1/3)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC(EXT_VGA)	O	X	X	+1.05V	2178mA	
VCC(INT_VGA)	O	X	X	+1.05V	2899mA	
VCC_AXG	O	X	X	+1.05V	8700mA	Graphics Core
VCC_SM(800)	O	O	X	+1.8VSUS	3A	(DDRII-667) 2.6A
VCC_SM(Standby)	O	O	X	+1.8VSUS	1mA	Self Refresh during S3

(See NB EDS Rev:1.0 Section 10.1 for max current)

(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

Quanta Computer Inc.

PROJECT : BL5M Montevina

Size	Document Number	Rev
	CLK. GEN./ CK505	1A

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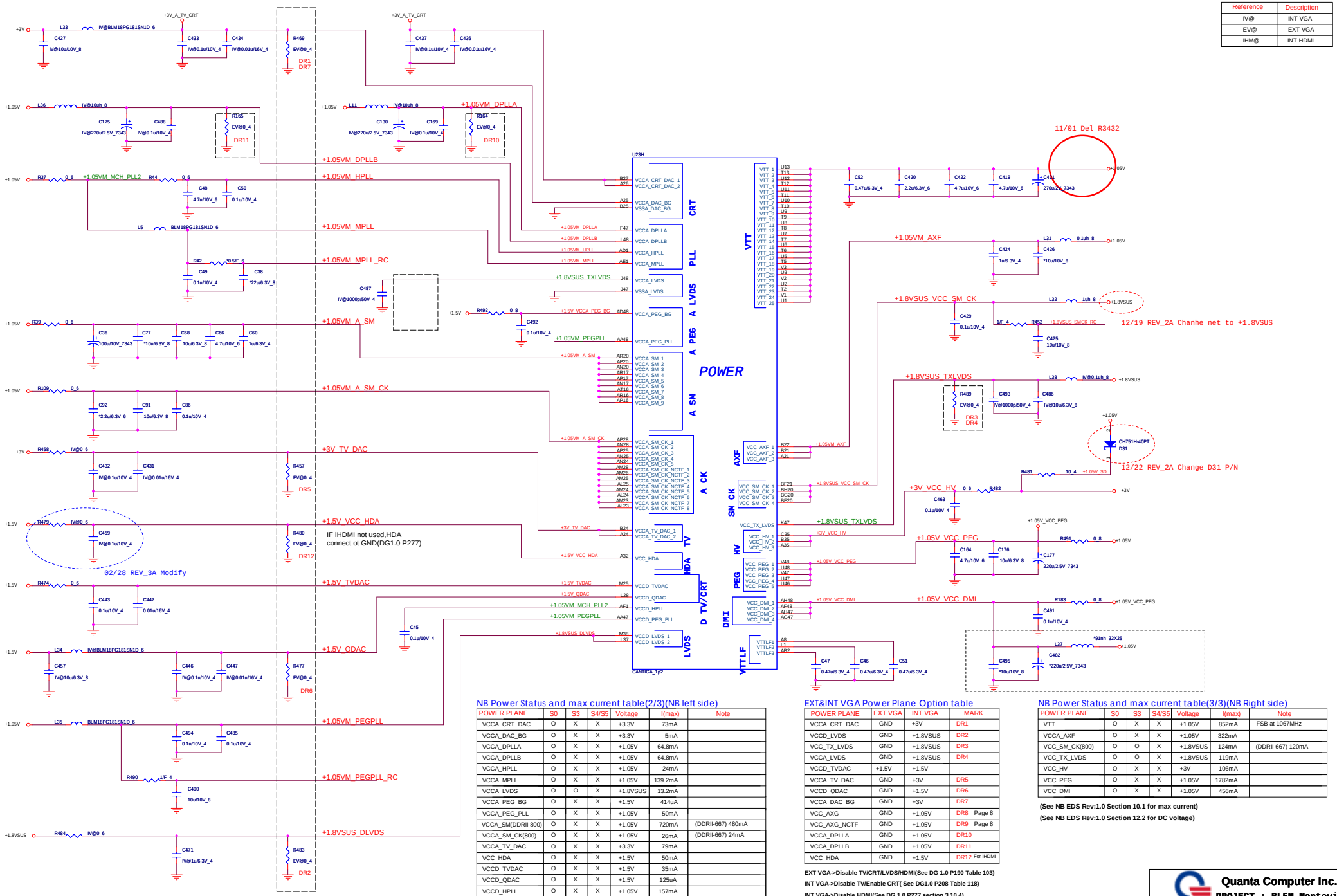

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA
IHM@	INT HDMI

NB Power Status and max current table(2/3)(NB left side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCCA_CRT_DAC	O	X	X	+3.3V	73mA	
VCCA_DAC_BG	O	X	X	+3.3V	5mA	
VCCA_DPLLA	O	X	X	+1.05V	64.8mA	
VCCA_DPLLB	O	X	X	+1.05V	64.8mA	
VCCA_HPLL	O	X	X	+1.05V	24mA	
VCCA_MPLL	O	X	X	+1.05V	139.2mA	
VCCA_LVDS	O	O	X	+1.8VSUS	13.2mA	
VCCA_PEG_BG	O	X	X	+1.5V	414uA	
VCCA_PEG_PLL	O	X	X	+1.05V	50mA	
VCCA_SM(DDRII-800)	O	X	X	+1.05V	720mA	(DDRII-667) 480mA
VCCA_SM_CK(800)	O	X	X	+1.05V	26mA	(DDRII-667) 24mA
VCCA_TV_DAC	O	X	X	+3.3V	79mA	
VCC_HDA	O	X	X	+1.5V	50mA	
VCCD_TVDAC	O	X	X	+1.5V	35mA	
VCCD_QDAC	O	X	X	+1.5V	125uA	
VCCD_HPLL	O	X	X	+1.05V	157mA	
VCCD_PEG_PLL	O	X	X	+1.05V	50mA	
VCCD_LVDS	O	O	X	+1.8VSUS	60mA	

EXT&INT VGA Power Plane Option table

POWER PLANE	EXT VGA	INT VGA	MARK
VCCA_CRT_DAC	GND	+3V	DR1
VCCD_LVDS	GND	+1.8VSUS	DR2
VCC_TX_LVDS	GND	+1.8VSUS	DR3
VCCA_LVDS	GND	+1.8VSUS	DR4
VCCD_TVDAC	+1.5V	+1.5V	
VCCA_TV_DAC	GND	+3V	DR5
VCCD_QDAC	GND	+1.5V	DR6
VCCA_DAC_BG	GND	+3V	DR7
VCC_AXG	GND	+1.05V	DR8 Page 8
VCC_AXG_NCTF	GND	+1.05V	DR9 Page 8
VCCA_DPLLA	GND	+1.05V	DR10
VCCA_DPLLB	GND	+1.05V	DR11
VCC_HDA	GND	+1.5V	DR12 For iHDMI

EXT VGA->Disable TV/CRT/LVDS/HDMI(See DG 1.0 P190 Table 103)

INT VGA->Disable TV/Enable CRT(See DG1.0 P208 Table 118)

INT VGA->Disable HDMI(See DG 1.0 P277 section 3.10.4)

NB Power Status and max current table(3/3)(NB Right side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VTT	O	X	X	+1.05V	852mA	FSB at 1067MHz
VCCA_AXF	O	X	X	+1.05V	322mA	
VCC_SM_CK(800)	O	O	X	+1.8VSUS	124mA	(DDRII-667) 120mA
VCC_TX_LVDS	O	O	X	+1.8VSUS	119mA	
VCC_HV	O	X	X	+3V	106mA	
VCC_PEG	O	X	X	+1.05V	1782mA	
VCC_DMI	O	X	X	+1.05V	456mA	

(See NB EDS Rev:1.0 Section 10.1 for max current)

(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

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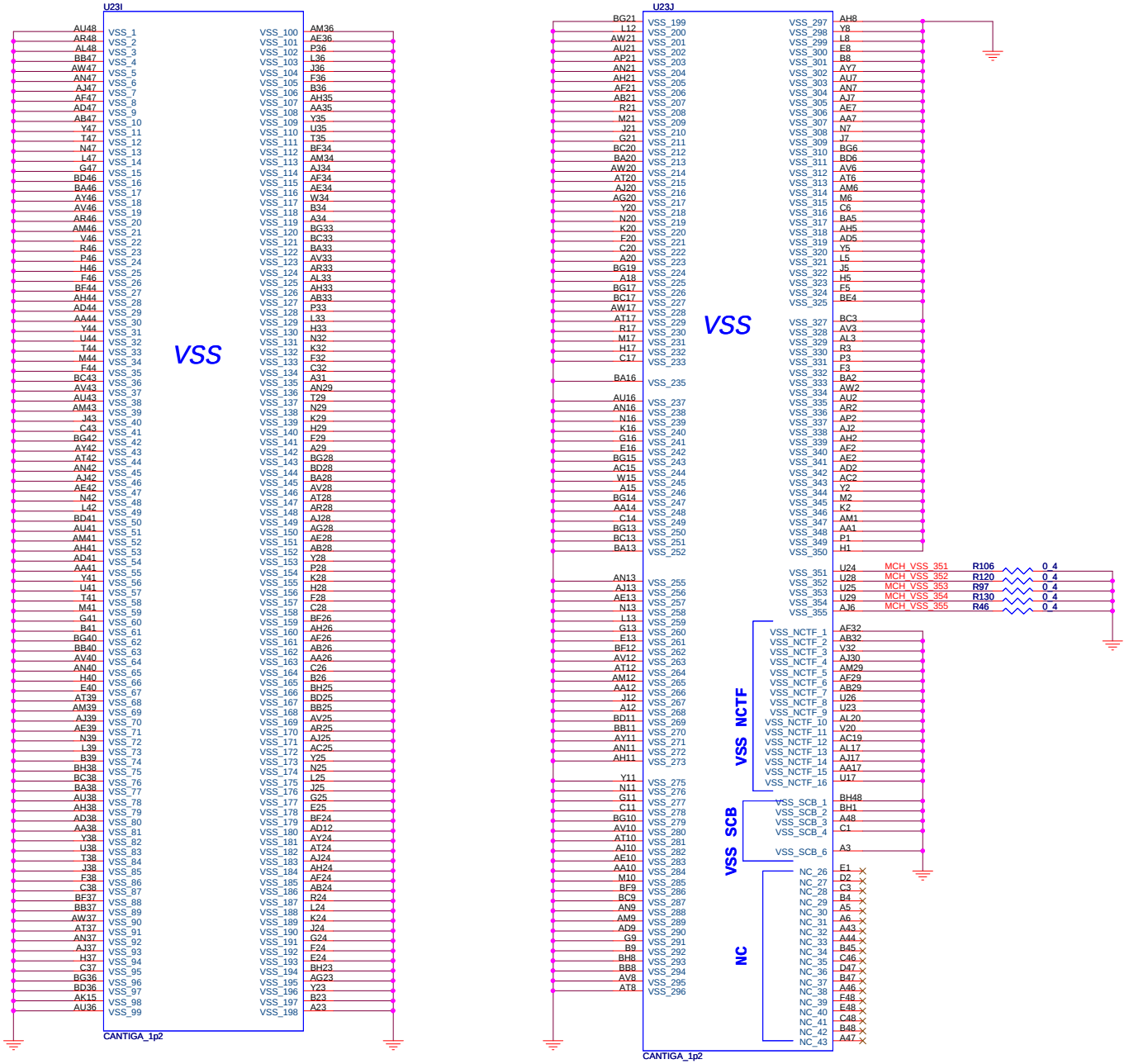
BOM Option Table

Reference	Description
N/A	N/A



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North Bridge Strap Pin Configuration Table

(See DG 1.0 P295 Table 184)
(See NB EDS 1.0 P187 Table 74)

BOM Option Table

Reference	Description
N/A	N/A

Pin Name	Strap description	Configuration	PU<4.02K> PD <2.21K>	Note
CFG[2:0]	FSB Frequency Select	[000]= FSB 1066MHz [010] = FSB 800MHz [011] = FSB 667MHz	See Page 2 FSB selection table	
CFG[4:3]	Reserved			
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)	(6) MCH_CFG_5 — R93 *4.02K/F_4 — GND	
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)	(6) MCH_CFG_6 — R99 *10K/F_4 — GND	
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)	(6) MCH_CFG_7 — R98 *4.02K/F_4 — GND	
CFG8	Reserved			
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)	(6) MCH_CFG_9 — R454 *4.02K/F_4 — GND	
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)	(6) MCH_CFG_10 — R455 *4.02K/F_4 — GND	
CFG11	Reserved			
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)	(6) MCH_CFG_12 — R76 *4.02K/F_4 — GND	
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)	(6) MCH_CFG_13 — R77 *4.02K/F_4 — GND	
CFG[15:14]	Reserved			
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)	(6) MCH_CFG_16 — R75 *4.02K/F_4 — GND	
CFG[18:17]	Reserved			
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed	(6) MCH_CFG_19 — R72 *4.02K/F_4 — +3V	
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port	(6) MCH_CFG_20 — R73 *4.02K/F_4 — +3V	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI/DP Device Present(Default) 1 = SDVO/HDMI/DP Device present	(6,20) SDVO_CTRLDATA — R146 *2.2K/F_4 — +3V	
L_DDC_DATA	Local Flat Panel(LFP) Present	0 = LFP Disable(Default) 1 = LFP Card Present;PCIE disable	(6,18) INT_LVDS_EDIDDATA — R166 *2.2K/F_4 — +3V	
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present	(6) DDPC_CTRLDATA — R71 *2.2K/F_4 — +3V	

Enable iTPM Table

PAGE	Net Name	PU & PD	NOTE
11	MCH_CFG_6	PD 10K to GND	NB Strap pin
13	SPI_MOSI	PU 20K to +3V_S5	SB Strap pin
14	CLGPIO5	PU 10K to +3V_S5	SB Strap pin

DDR2 Dual channel A/B PU

M_A_A[13..0] → M_A_A[13..0] (7,13)

M_B_A[13..0] → M_B_A[13..0] (7,13)

DDRII A CHANNEL

+SMDDR_VTERM

C83 0.1u/10V_4, C131 0.1u/10V_4, C90 0.1u/10V_4, C168 0.1u/10V_4, C125 0.1u/10V_4, C150 0.1u/10V_4, C85 0.1u/10V_4, C94 0.1u/10V_4, C135 0.1u/10V_4, C156 0.1u/10V_4, C84 0.1u/10V_4, C157 0.1u/10V_4, C87 0.1u/10V_4

DDRII B CHANNEL

+SMDDR_VTERM

C167 0.1u/10V_4, C143 0.1u/10V_4, C88 0.1u/10V_4, C102 0.1u/10V_4, C93 0.1u/10V_4, C152 0.1u/10V_4, C163 0.1u/10V_4, C171 0.1u/10V_4, C124 0.1u/10V_4, C101 0.1u/10V_4, C147 0.1u/10V_4, C158 0.1u/10V_4, C122 0.1u/10V_4

RP17: M_A_A3, M_A_A1 → +SMDDR_VTERM
RP22: M_A_A9, M_A_A8
RP20: M_A_A2, M_A_A4
RP29: (6,13) M_CKE1, M_A_A6
RP25: (7,13) M_A_BS#2, M_A_A5
RP30: M_A_A12, (6,13) M_CKE0
RP15: M_A_A0, (7,13) M_A_BS#1

RP14: M_B_A10, (7,13) M_B_BS#0 → +SMDDR_VTERM
RP19: M_B_A3, M_B_A5
RP13: (7,13) M_B_BS#1, M_B_A0
RP21: M_B_A7, M_B_A11
RP24: M_B_A8, M_B_A1
RP18: M_B_A4, M_B_A2
RP26: (7,13) M_B_BS#2, M_B_A12

R151, R148: 56_4 — (7,13) M_A_A14, (7,13) M_B_A14 → +SMDDR_VTERM

RP23: M_A_A7, M_A_A11 → +SMDDR_VTERM
RP31: M_B_A9, (6,13) M_CKE3
RP6: (6,13) M_ODT1, (6,13) M_CS#1
RP7: (6,13) M_ODT3, (6,13) M_CS#3
RP16: (7,13) M_A_BS#0, M_A_A10
RP12: (7,13) M_A_WE#, (7,13) M_A_CAS#
RP11: (6,13) M_CS#0, (7,13) M_A_RAS#
RP10: (7,13) M_B_WE#, (7,13) M_B_CAS#
RP28: (6,13) M_CKE4, M_B_A6
RP9: (6,13) M_ODT2, (7,13) M_B_RAS#
RP5: M_A_A13, (6,13) M_ODT0
RP8: (6,13) M_CS#2, M_B_A13

All RP: 56X2

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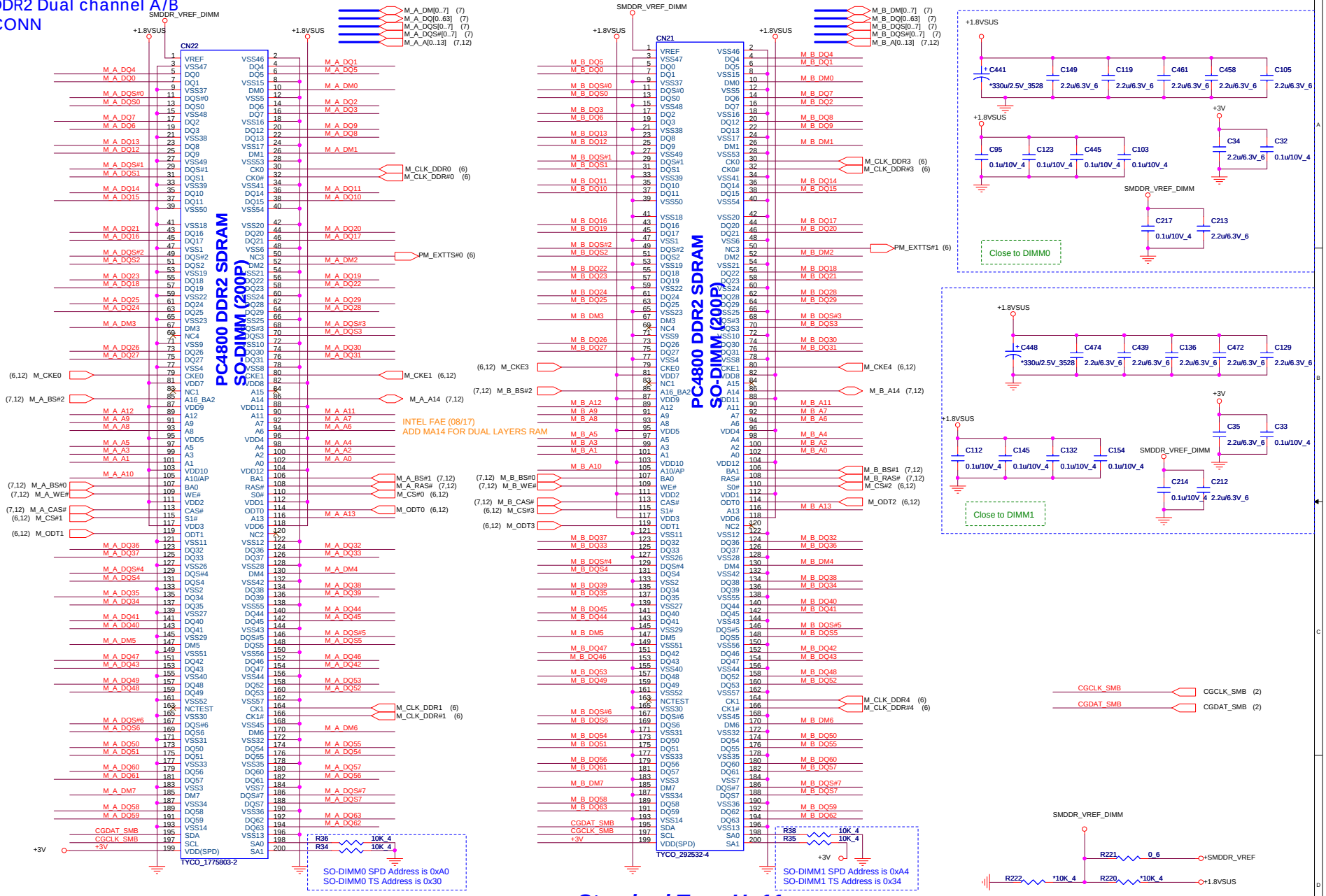
DDR2 Dual channel A/B CONN



Standard Type H: 6.5mm

CLOCK 0,1
CKE 0,1

Standard Type H: 11mm

CLOCK 3,4
CKE 2,3

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RTC CRYSTAL

C248 10p/50V_4 — CLK_32KX1
32.768KHZ Y2
R288 10M_6
C235 10p/50V_4 — CLK_32KX2

RESET JUMP

VCCRTC
An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided.
R527 20K_6 — RTC_RST#
C520 1u/6.3V_4
G2 *SHORT_PAD

VCCRTC
R250 20K_6 — SRTC_RST#
C233 1u/6.3V_4
G1 *SHORT_PAD

VCCRTC
R530 1M_4 — SM_INTRUDER#
R262 332K/F_4 — ICH_INTVRMEN
(DG 1.0 Table-292)
Internal VRM enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05.

+3V_SS
R525 10K_4 — ICH_GPIO56

+1.5V_PCIE_ICH
R293 24.9/F_4 — GLAN_COMP
24.9 Ohm pull up to 1.5V for GLAN_COMPIO is required, no matter intel LAN is used or not.

LDRQ0/1# : Internal PU

Layout note:
DPRSTP# , Daisy Chain
(SB>Power>NB>CPU)

BOM Option Table

Reference	Description
IHM@	INT HDMI

U35A

RTC / LPC
CLK_32KX1 C23 — RTCX1
CLK_32KX2 C24 — RTCX2
RTC_RST# A25 — RTCRST#
SRTC_RST# F20 — SRTCRST#
SM_INTRUDER# C22 — INTRUDER#
ICH_INTVRMEN B22 — INTVRMEN
A22 — LAN100_SLP

FWH0/LAD0 K5 — LAD0 — LAD0 (25,29)
FWH1/LAD1 K4 — LAD1 — LAD1 (25,29)
FWH2/LAD2 L6 — LAD2 — LAD2 (25,29)
FWH3/LAD3 K2 — LAD3 — LAD3 (25,29)
FWH4/LFRAME# K3 — LFRAME# — LFRAME# (25,29)
LDRQ0# J3 — LDRQ#0 — T88
LDRQ1#/GPIO23 J1 — LDRQ#1 — LDRQ#1 (25)

LAN / GLAN
E25 — GLAN_CLK
C13 — LAN_RSTSYNC
F14 — LAN_RXD0
G13 — LAN_RXD1
D14 — LAN_RXD2
D13 — LAN_TXD0
D12 — LAN_TXD1
E13 — LAN_TXD2

CPU
A20GATE N7 — GATEA20 — GATEA20 (29)
A20M# AJ27 — H_A20M# — H_A20M# (3)
DPRSTP# AJ25 — H_DPRSTP#_R — R588 0_4 — H_DPRSTP# (3,6,32)
DPSLP# AF23 — H_DPSLP#_R — R367 0_4 — H_DPSLP# (3)
FERR# AJ26 — H_FERR#_R — R587 56_4 — H_FERR# — H_FERR# (3)
CPUPWRGD AD22 — H_PWRGD — H_PWRGD (3)
IGNNE# AF25 — H_IGNNE# — H_IGNNE# (3)
INIT# AE22 — H_INIT# — H_INIT# (3)
INTR AG25 — H_INTR — H_INTR (3)
RCIN# L3 — RCIN# — RCIN# (29)
NMI AF23 — H_NMI — H_NMI (3) — R370 0_4 — H_SMI# — H_SMI# (3)
SMI# AF24 — H_SMI#_R
STPCLK# AH27 — H_STPCLK# — H_STPCLK# (3)
THRMTRIP# AG26 — H_THERMTRIP_R — R586 56_4 — H_THERMTRIP_RR — R585 *0_4 — PM_THRMTRIP# — PM_THRMTRIP# (3,6)
TP12 AG27 — ICH_TP12 — T150

+1.05V_ICH_IO
R608 *56_4
R378 *56_4
ICH_DPRSTP# (3,6,32)
H_DPSLP# (3)
+1.05V_ICH_IO
R607 56_4
H_FERR# — H_FERR# (3)
+1.05V_ICH_IO
R606 56_4
+3V
GATEA20 R329 8.2K_4
RCIN# R545 10K_4

Layout note:
PU R needs to placed within 2" of ICH9-M, series R must be placed within 2"of PU R w/o stub.

IHDA
ICH_GPIO56 B10 — GPIO56
GLAN_COMP B28 — GLAN_COMPI
B27 — GLAN_COMPO
HDA_BIT_CLK_R AF6 — HDA_BIT_CLK
HDA_SYNC_R AH4 — HDA_SYNC
HDA_RST#_R AE7 — HDA_RST#
(26) ACZ_SDIN0 — ACZ_SDIN0 AF4 — HDA_SDIN0
HDA_SDIN1 AG4 — HDA_SDIN1
HDA_SDIN2 AH3 — HDA_SDIN2
HDA_SDIN3 AE5 — HDA_SDIN3
T95
HDA_SDOUT_R AG5 — HDA_SDOUT
ICH_GPIO33 AG7 — HDA_DOCK_EN#/GPIO33
ICH_GPIO34 AE8 — HDA_DOCK_RST#/GPIO34
T146
T93
(22) SATA_LED# — SATA_LED# AG8 — SATALED#

SATA
SATA4RXN AH11 — SATA_RXN4_C
SATA4RXP AJ11 — SATA_RXP4_C
SATA4TXN AG12 — SATA_TXN4_C
SATA4TXP AF12 — SATA_TXP4_C
SATA5RXN AH9 — SATA_RXN5_C
SATA5RXP AJ9 — SATA_RXP5_C
SATA5TXN AE10 — SATA_TXN5_C
SATA5TXP AF10 — SATA_TXP5_C
SATA_CLKN AH18 — CLK_PCIE_SATA# — CLK_PCIE_SATA# (2)
SATA_CLKP AJ18 — CLK_PCIE_SATA — CLK_PCIE_SATA (2)
SATARBIAS# AJ7 — SATA_RBIAS_PN
SATARBIAS AH7
R596 24.9/F_4
SATA_RBIAS_PN<0.5" Avoid routing next to clock/high speed signals

SATA_RXN0_C AJ16 — SATA_RXP0_C AH16 — SATA_TXN0_C AF17 — SATA_TXP0_C AG17
SATA_RXN1_C AH13 — SATA_RXP1_C AJ13 — SATA_TXN1_C AG14 — SATA_TXP1_C AF14
SATA1RXN SATA1RXP SATA1TXN SATA1TXP

ICH9M REV 1.0

02/14 REV_3A Swap SATA chennal

SATA I/F

12/18 REV_2A Swap SATA chennal

To 2'nd SATA HDD
(22) SATA_RXN0 — SATA_RXP0 — SATA_TXN0 — SATA_TXP0
SATA_RXN0 C572 — SATA_RXP0 C571 — SATA_TXN0 C569 — SATA_TXP0 C570
3900p/25V_4 — SATA_RXN4_C
3900p/25V_4 — SATA_RXP4_C
3900p/25V_4 — SATA_TXN4_C
3900p/25V_4 — SATA_TXP4_C

To 1'st SATA HDD
(22) SATA_RXN1 — (22) SATA_RXP1 — (22) SATA_TXN1 — (22) SATA_TXP1
SATA_RXN1 C568 — SATA_RXP1 C567 — SATA_TXN1 C565 — SATA_TXP1 C566
3900p/25V_4 — SATA_RXN0_C
3900p/25V_4 — SATA_RXP0_C
3900p/25V_4 — SATA_TXN0_C
3900p/25V_4 — SATA_TXP0_C

To SATA ODD
(22) SATA_RXN4 — (22) SATA_RXP4 — (22) SATA_TXN4 — (22) SATA_TXP4
SATA_RXN4 C348 — SATA_RXP4 C347 — SATA_TXN4 C365 — SATA_TXP4 C366
3900p/25V_4 — SATA_RXN1_C
3900p/25V_4 — SATA_RXP1_C
3900p/25V_4 — SATA_TXN1_C
3900p/25V_4 — SATA_TXP1_C

To E-SATA
(19) SATA_RXN5 — (19) SATA_RXP5 — (19) SATA_TXN5 — (19) SATA_TXP5
SATA_RXN5 C350 — SATA_RXP5 C349 — SATA_TXN5 C352 — SATA_TXP5 C351
3900p/25V_4 — SATA_RXN5_C
3900p/25V_4 — SATA_RXP5_C
3900p/25V_4 — SATA_TXN5_C
3900p/25V_4 — SATA_TXP5_C

HD Audio I/F(CODEC& iHDMI)

HDA_SDIN2 R575 IHM@*0_4
HDA_SDIN1 R576 IHM@0_4 — HDA_SDIN_HDMI (6)
R597 IHM@33_4 — HDA_RST#_HDMI (6)
HDA_RST#_R R598 33_4 — ACZ_RST#_AUDIO (26)

HDA_SDOUT_R R602 IHM@33_4 — HDA_SDOUT_HDMI (6)
R604 33_4 — ACZ_SDOUT_AUDIO (26)
HDA_SYNC_R R599 IHM@33_4 — HDA_SYNC_HDMI (6)
R600 33_4 — ACZ_SYNC_AUDIO (26)
HDA_BIT_CLK_R R611 IHM@33_4 — HDA_BIT_CLK_HDMI (6)
R610 33_4 — BIT_CLK_AUDIO (26)

HDA_BIT_CLK_HDMI — R369 *22_4 — C353 *22p/50V_4
BIT_CLK_AUDIO — R368 *22_4 — C354 *22p/50V_4
10/14 Add

RTC BATTERY

+3VPCU — D33 RB500V — VCCRTC
R_3VRTC — D32 RB500V — VCCRTC
C522 1u/10V_6
02/12 REV_3A Change R528,R529,R532 value
R533 1K_4
RTC_N02
Q44 MMBT3904
R528 2K/F_4 — R529 2K/F_4
R532 6.8K/F_4
+5VPCU
CN28 RTC CONN
RTC_N03 — R535 15K_4

South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 0 HDA_SDOUT 0 — RSVD ICH_TP3 0 HDA_SDOUT 1 — Enter XOR Chain	(16) ICH_TP3 — ICH_TP3 R264 *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	ICH_TP3 1 HDA_SDOUT 0 — Normal opration(Default) ICH_TP3 1 HDA_SDOUT 1 — Set PCIE port config bit 1	HDA_SDOUT_R R582 *1K_4 +3V_HDA_IO_ICH PU +1.5V

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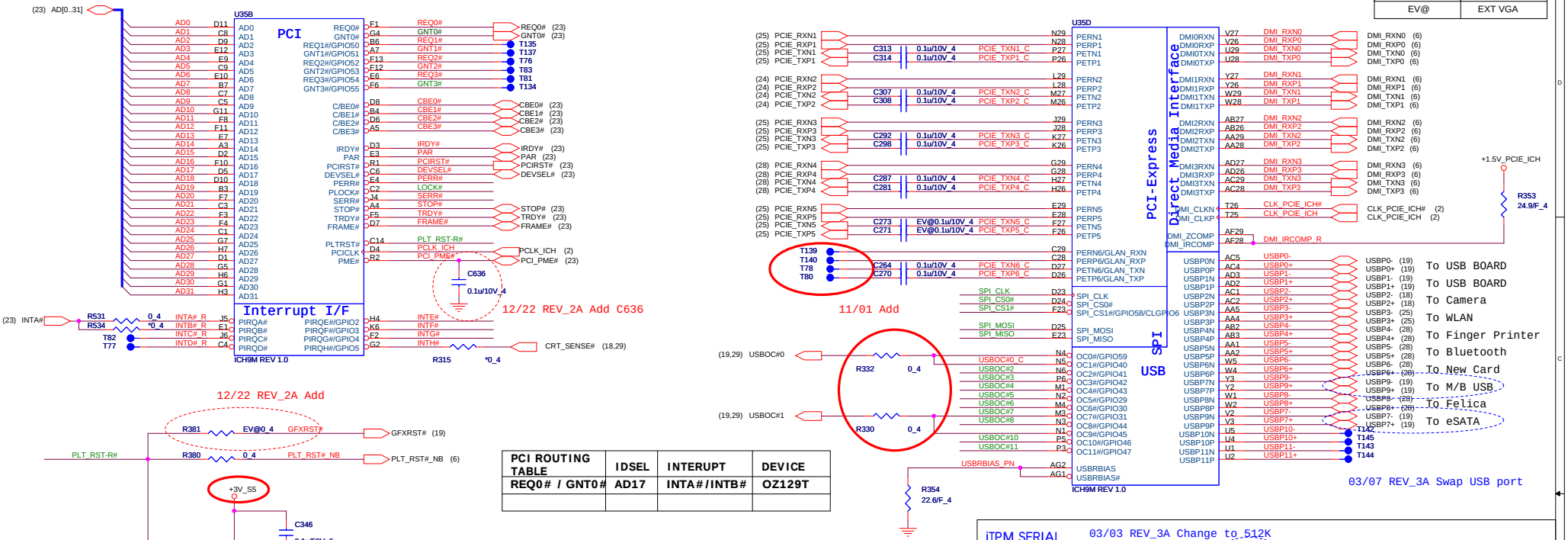
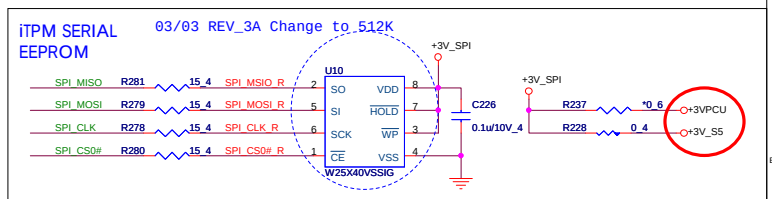
PCI/PCI-E/USB/DMI/SPI

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#/INTB#	OZ129T

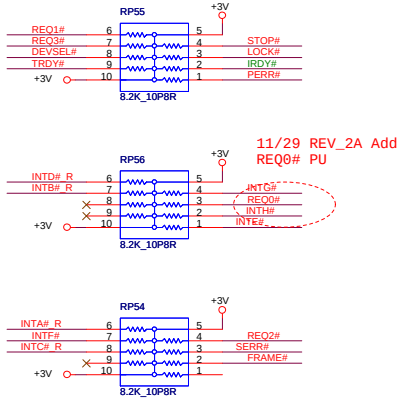


South Bridge Strap Pin (2/3)

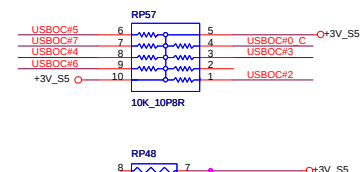
Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R511 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	Enable iTPM SPI_MOSI R295 *20K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK		GNT0# R304 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# R314 *1K_4

PCI_GNT#0	SPI_CS#1	Boot Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

PCI PULL-UP



USBOC# PULL-UP



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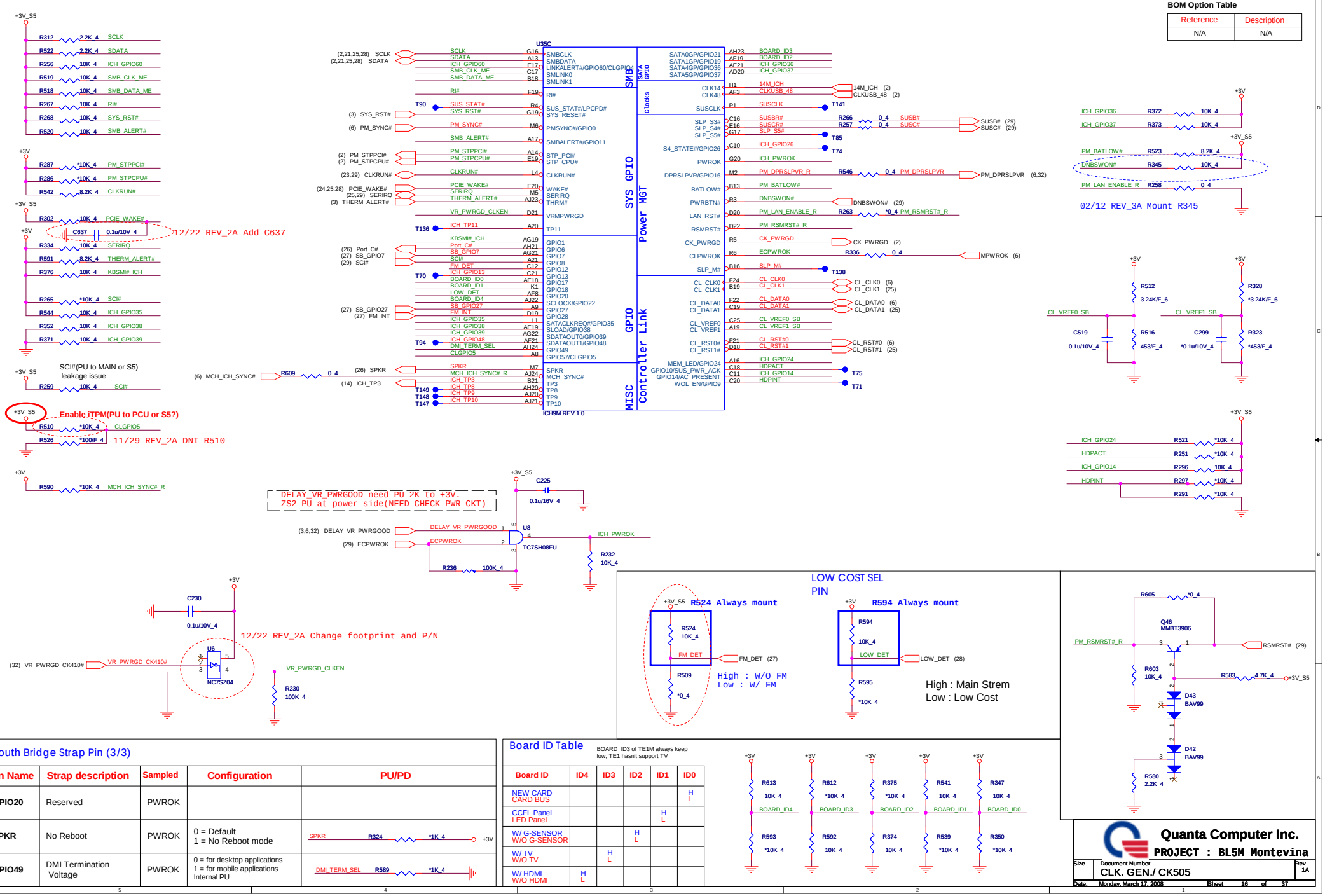
BOM Option Table

Reference	Description
N/A	N/A



South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	SPKR R324 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R589 *1K_4

Board ID Table

BOARD_ID3 of TE1M always keep low, TE1 hasn't support TV

Board ID	ID4	ID3	ID2	ID1	ID0
NEW CARD CARD BUS					H L
CCFL Panel LED Panel				H L	
W/ G-SENSOR W/O G-SENSOR			H L		
W/ TV W/O TV		H L			
W/ HDMI W/O HDMI	H L				

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Size	Document Number	Rev
	CLK. GEN./ CK505	1A

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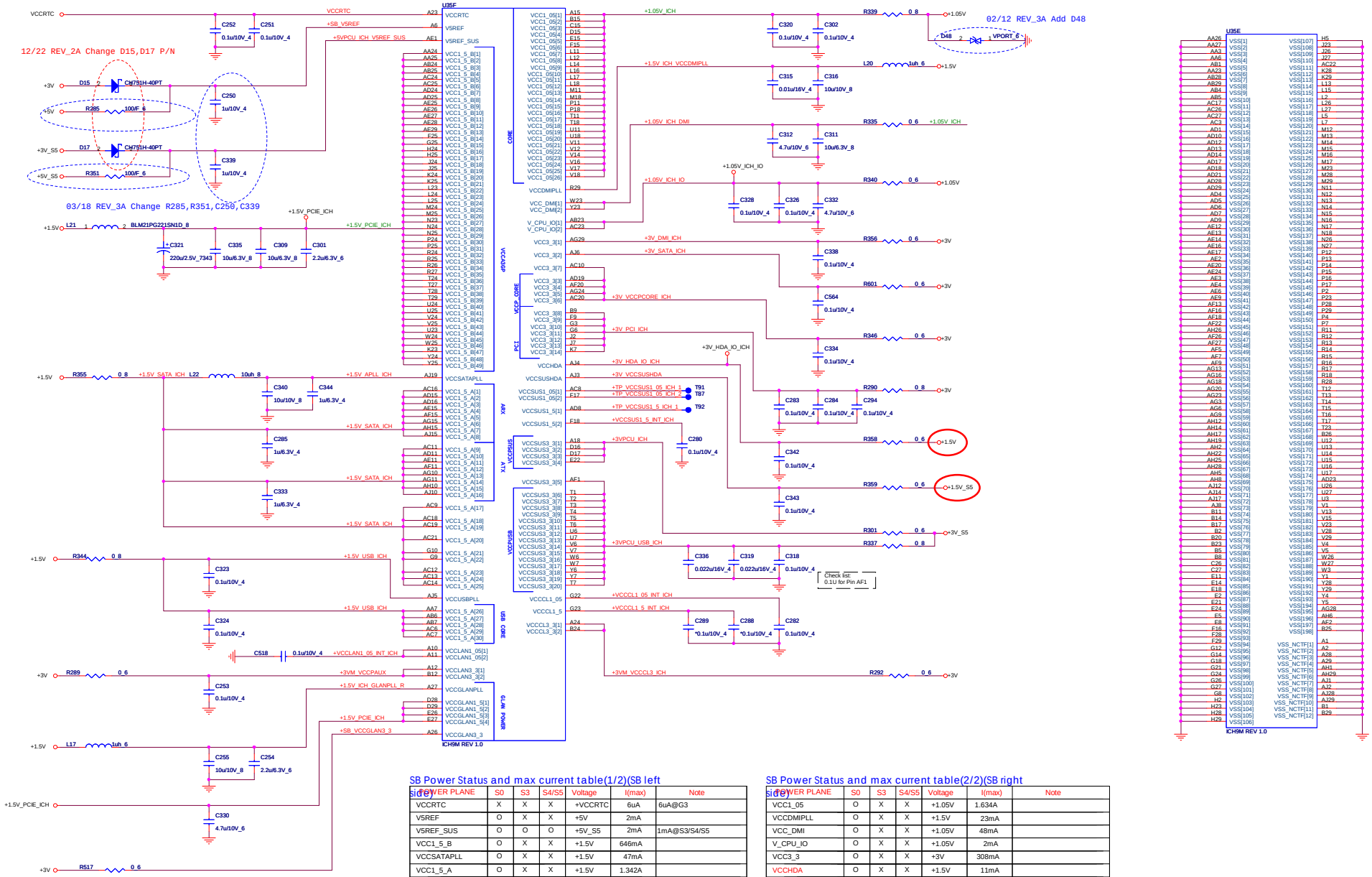

BOM Option Table

Reference	Description
N/A	N/A

SB Power Status and max current table(1/2)(SB left side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCCRTC	X	X	X	+VCCRTC	6uA	6uA@G3
V5REF	O	X	X	+5V	2mA	
V5REF_SUS	O	O	O	+5V_S5	2mA	1mA@S3/S4/S5
VCC1_5_B	O	X	X	+1.5V	646mA	
VCCSATAPLL	O	X	X	+1.5V	47mA	
VCC1_5_A	O	X	X	+1.5V	1.342A	
VCCUSBPLL	O	X	X	+1.5V	11mA	
VCCLAN1_05	O	X	X	+1.05V	X	Powered by Vcc1_05 in S0
VCCLAN3_3	O	X	X	+3V	19mA	Tied to +3V,not +3VSUS
VCCGLANPLL	O	X	X	+1.5V	23mA	
VCCGLAN1_5	O	X	X	+1.5V	80mA	
VCCGLAN3_3	O	X	X	+3V	1mA	

SB Power Status and max current table(2/2)(SB right side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC1_05	O	X	X	+1.05V	1.634A	
VCCDMIPLL	O	X	X	+1.5V	23mA	
VCC_DMI	O	X	X	+1.05V	48mA	
V_CPU_IO	O	X	X	+1.05V	2mA	
VCC3_3	O	X	X	+3V	308mA	
VCCHDA	O	X	X	+1.5V	11mA	
VCCSUSHDA	O	O	O	+1.5V_S5	11mA	1mA@S3/S4/S5
VCCSUS1_05	O	O	O	+1.05V	X	Powered by Vcc1_05 in S0
VCCSUS1_5	O	O	O	+1.5V	X	Powered by Vcc1_5_A in S0
VCCSUS3_3	O	O	O	+3VSUS	212mA	52mA@S3/S4/S5
VCCCL1_05	O	X	X	+1.05V	X	Powered by Vcc1_05 in S0
VCCCL1_5	O	X	X	+1.5V	X	Powered by Vcc1_5_A in S0
VCCCL3_3	O	X	X	+3V	19mA	Tied to +3V,not +3VSUS

Note:VCCSUS1_05 , VCCSUS1_5 are powered by VccSus3_3 in S3/S4/S5

Quanta Computer Inc.
PROJECT : BL5M Montevina
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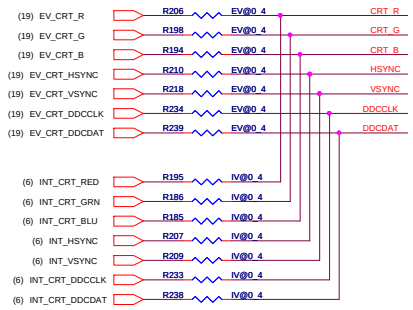
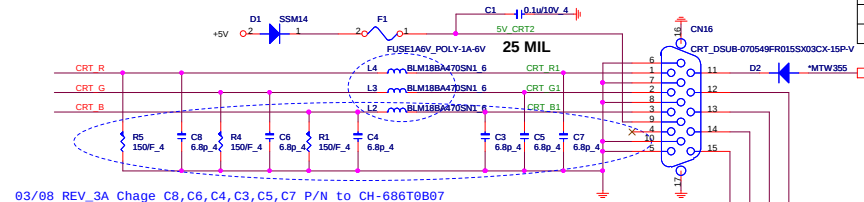
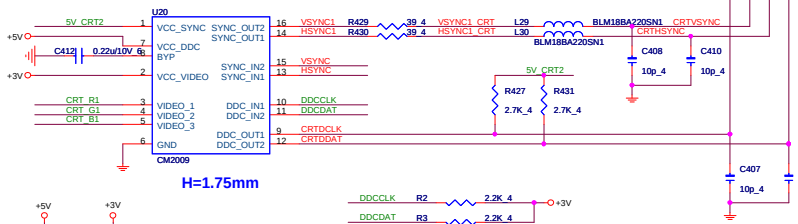
CRT PORT



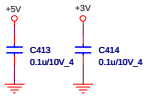
03/08 REV_3A Chage L2,L3,L4 P/N to CX8BA470003



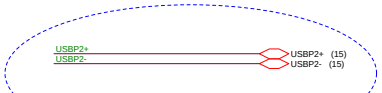
03/08 REV_3A Chage C8,C6,C4,C3,C5,C7 P/N to CH-686T0B07

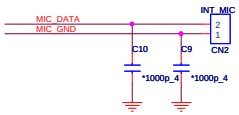


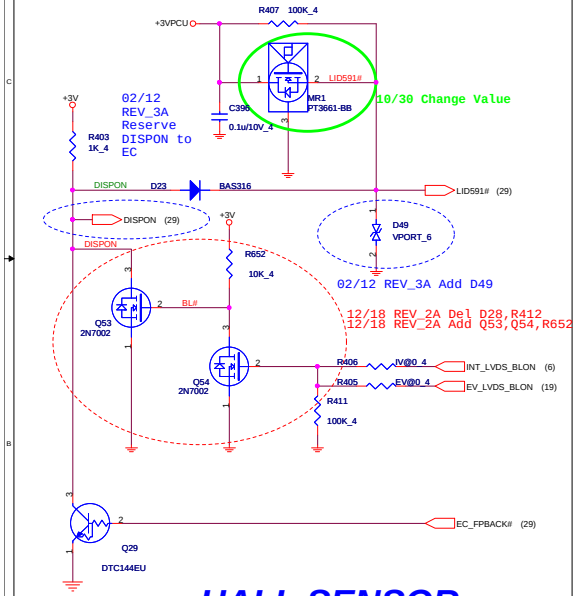
H=1.75mm



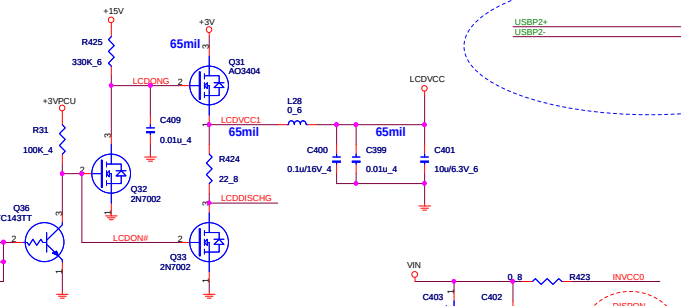
03/07 REV_3A Del RP1

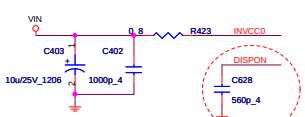






HALL SENSOR

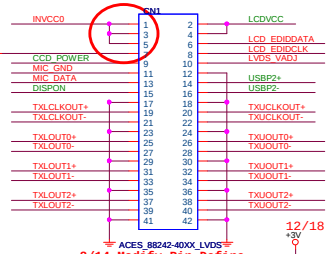




12/18 REV_2A Add C628

LCD PANEL MODULE

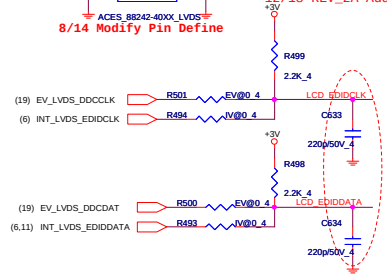
10/23 Add



8/14 Modify Pin Define

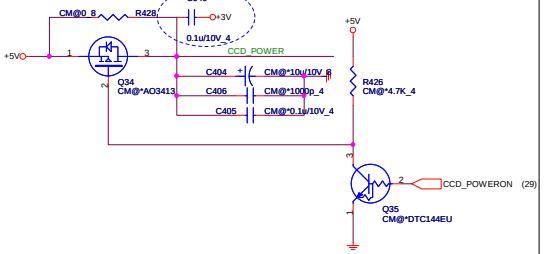
02/12 REV_3A Mount C14 for EMI

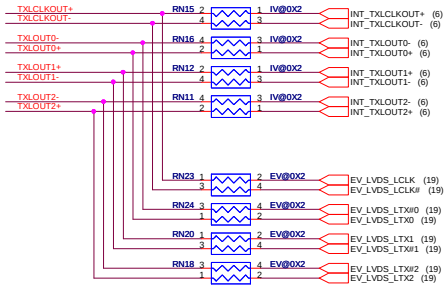
12/18 REV_2A Add

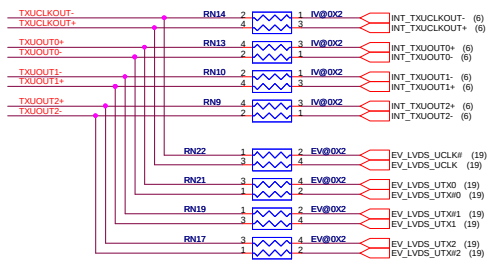


CAMERA MODULE

02/12 REV_3A Add C640 for EMI







BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA
IHM@	INT HDMI
EV_IV@	EV&IV diff. value

Quanta Computer Inc.
PROJECT : BL5M Montevina

Size	Document Number	Rev
	LCD/CRT/LID/CAMERA	1A
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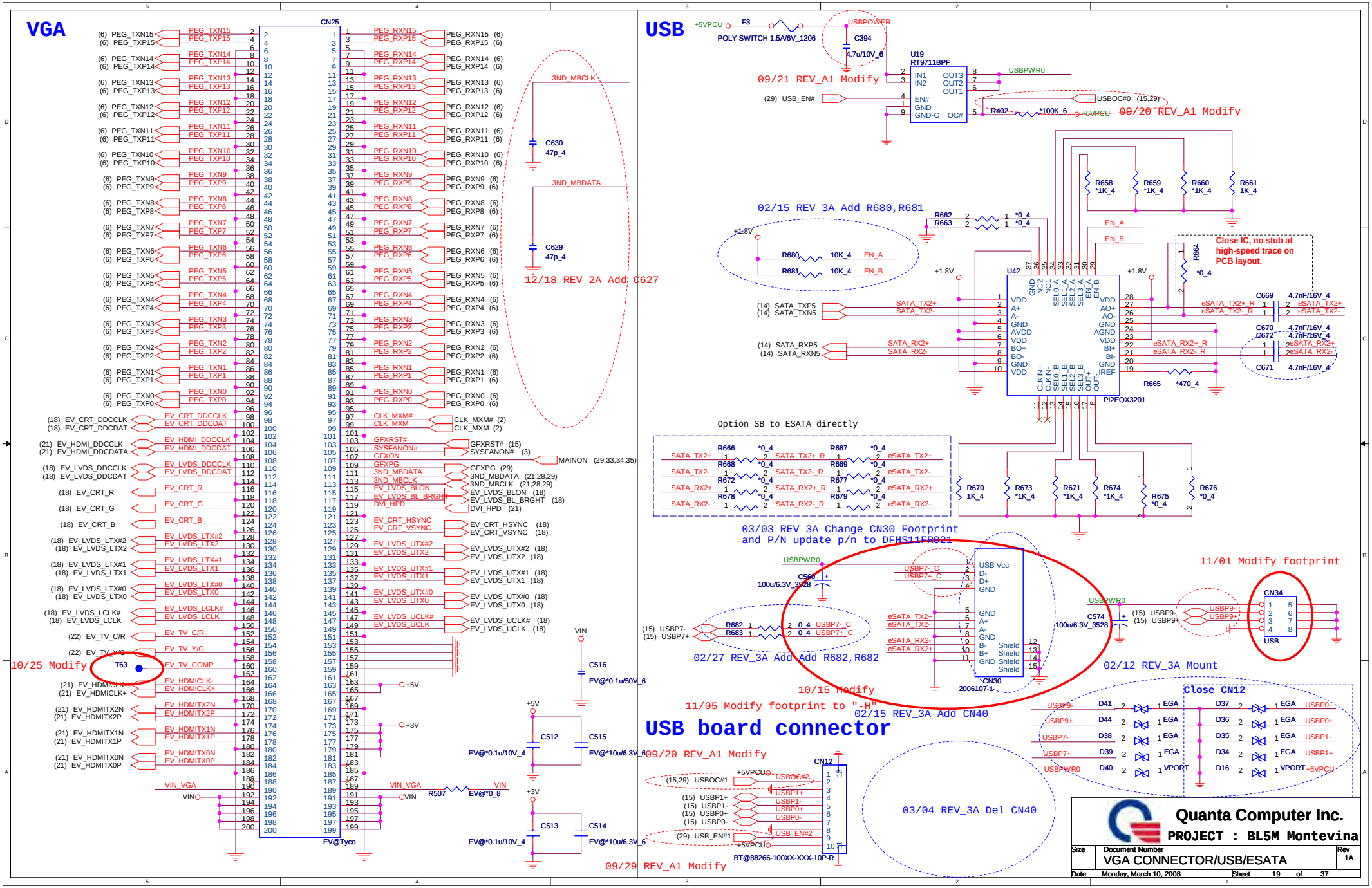
VGA
CN25
10/25 Modify
T63
12/18 REV_2A Add C627
09/29 REV_A1 Modify
USB
09/21 REV_A1 Modify
09/20 REV_A1 Modify
02/15 REV_3A Add R680,R681
Close IC, no stub at high-speed trace on PCB layout.
Option SB to ESATA directly
03/03 REV_3A Change CN30 Footprint and P/N update p/n to DFHS11FR021
11/01 Modify footprint
02/27 REV_3A Add Add R682,R682
10/15 Modify
02/12 REV_3A Mount
11/05 Modify footprint to "-H"
02/15 REV_3A Add CN40
USB board connector
09/20 REV_A1 Modify
03/04 REV_3A Del CN40
Close CN12
Quanta Computer Inc.
PROJECT : BL5M Montevina
VGA CONNECTOR/USB/ESATA
Monday, March 10, 2008
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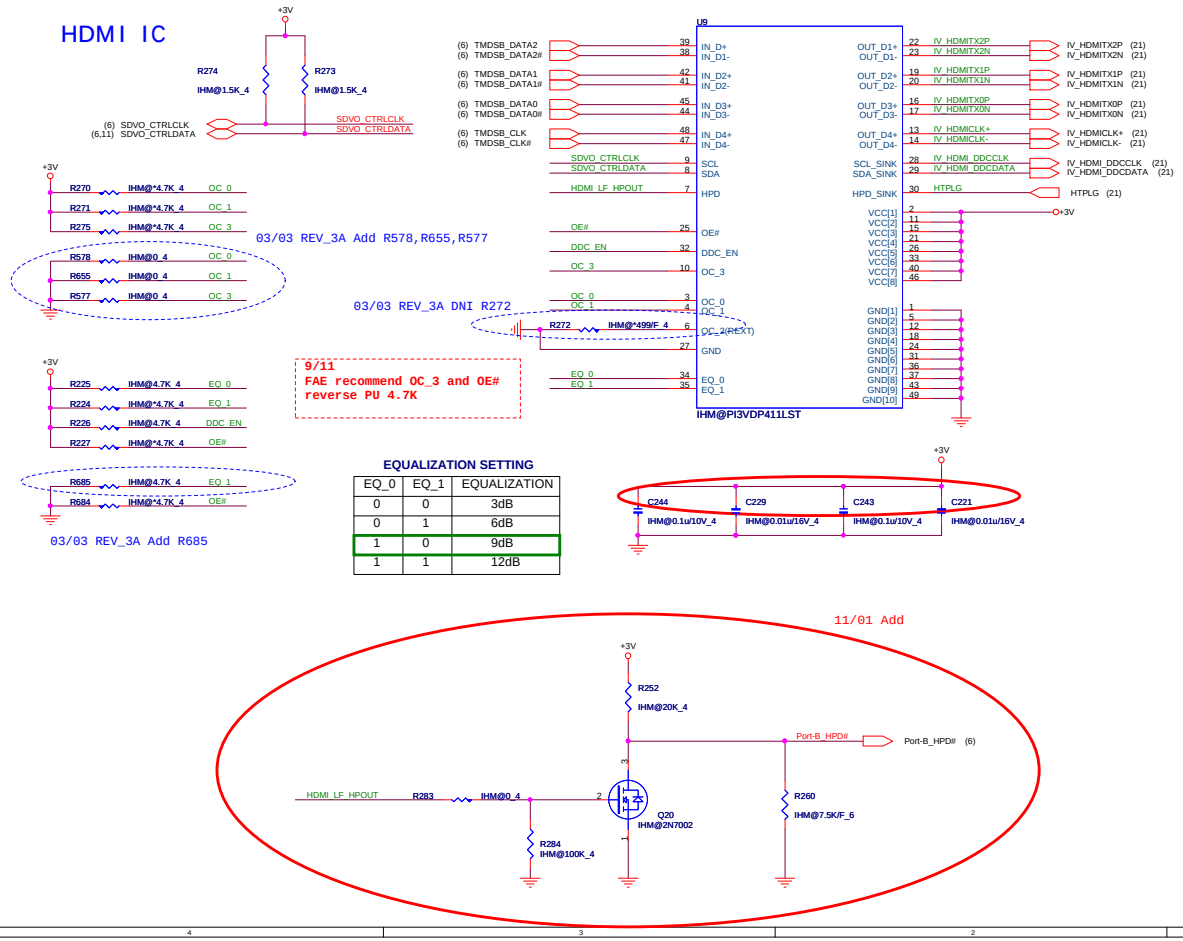
Only For UMA



EQ_0	EQ_1	EQUALIZATION
0	0	3dB
0	1	6dB
1	0	9dB
1	1	12dB

Quanta Computer Inc.
PROJECT : BL5M Montevina

Size	Document Number	Rev
	PI3VDP411LST(HDMI)	1A

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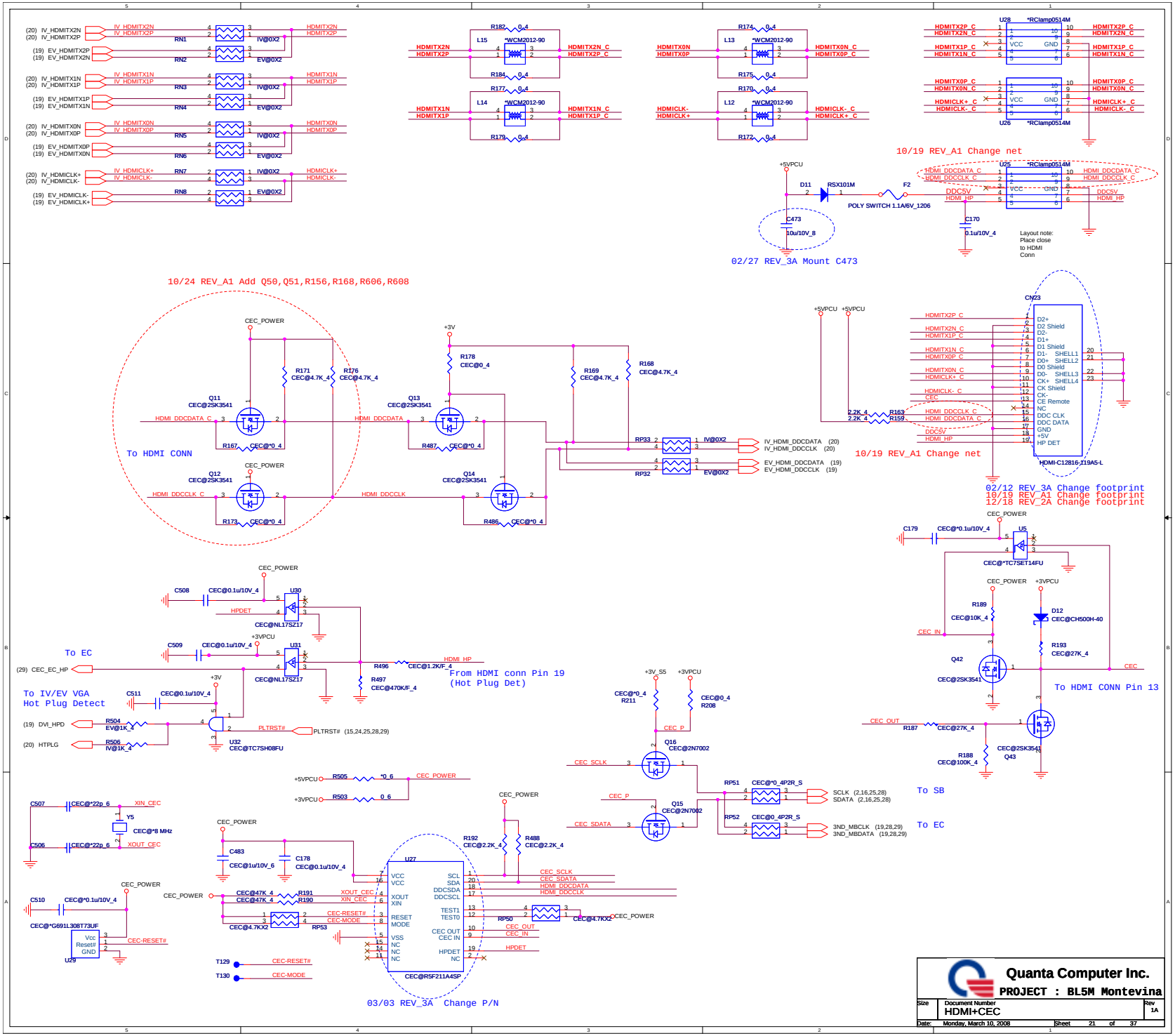
10/19 REV_A1 Change net
02/27 REV_3A Mount C473
10/24 REV_A1 Add Q50,Q51,R156,R168,R606,R608
To HDMI CONN
10/19 REV_A1 Change net
02/12 REV_3A Change footprint
10/19 REV_A1 Change net
12/18 REV_2A Change footprint
To EC
To IV/EV VGA
Hot Plug Detect
From HDMI conn Pin 19
(Hot Plug Det)
To HDMI CONN Pin 13
To SB
To EC
03/03 REV_3A Change P/N
Quanta Computer Inc.
PROJECT : BL5M Montevina
HDMI+CEC
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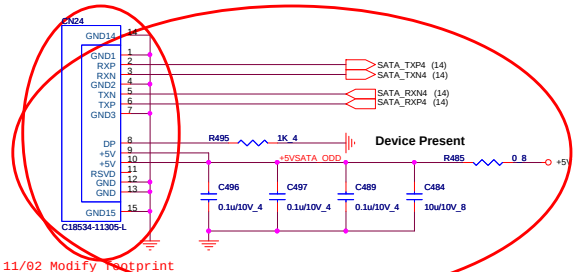
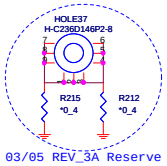
SATA ODD



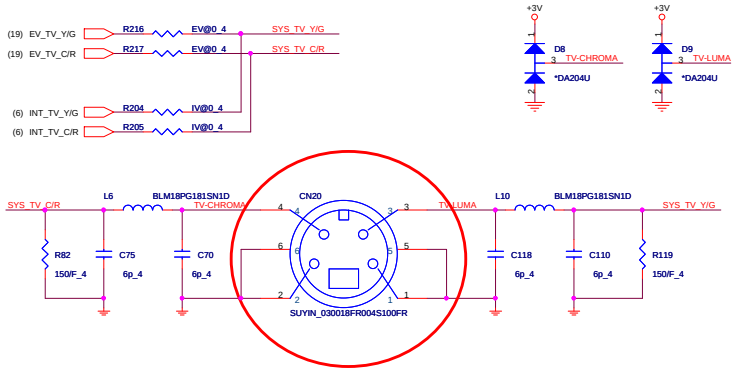
11/02 Modify footprint

10/15 Add



03/05 REV_3A Reserve R215,R212 fro EMI

TVOUT



10/25 Modify
11/01 Modify Footprint

CPU SINK

VGA SINK

MB SINK

10/23 REV_A1 Modify footprint

10/26 REV_A1 Modify footprint

02/12 REV_3A Modify HOLE32 to AGND

09/27 REV_A1 Modify Footprint

12/18 REV_2A Modify

10/26 REV_A1 Del HOLE34 for EXP

10/20 REV_A1 Add

10/22 REV_A1 Modify

MINI-1 SINK

MODEM

02/12 REV_3A Change footprint

MINI-2 SINK

LED / WLAN SW

02/12 REV_3A change LED4,LED3 footprint and P/N

10/26 REV_A1 Add

03/10 REV_3A Add

10/30 Copy from BL5S

12/18 REV_2A Add

11/05 Add

W-LAN&BT LED

Mainstream --> Orange
Low Cost --> Orange

WiMAX LED

10/25 Modify
03/07 REV_3A Mount R649

02/27 REV_3A Mount D24,D47

02/12 REV_3A Change R415,R414 value

10/25 Modify
12/18 REV_2A Change LED type

Mainstream --> White
Low Cost --> N/A

12/18 REV_2A Change P/N

03/09 REV_3A Del

09/20 REV_A1 Add HOLE32,HOLE33 for ESATA

09/20 REV_A1 Add HOLE30,HOLE31 for ESATA

2'nd SATA HDD

02/12 REV_3A Add for ESD

02/12 REV_3A Change footprint

SATA HDD

02/12 REV_3A Change footprint

Quanta Computer Inc. PROJECT : BL5M Montevina			
Size	Document Number PATA/ODD/TV/LED		Rev 1A
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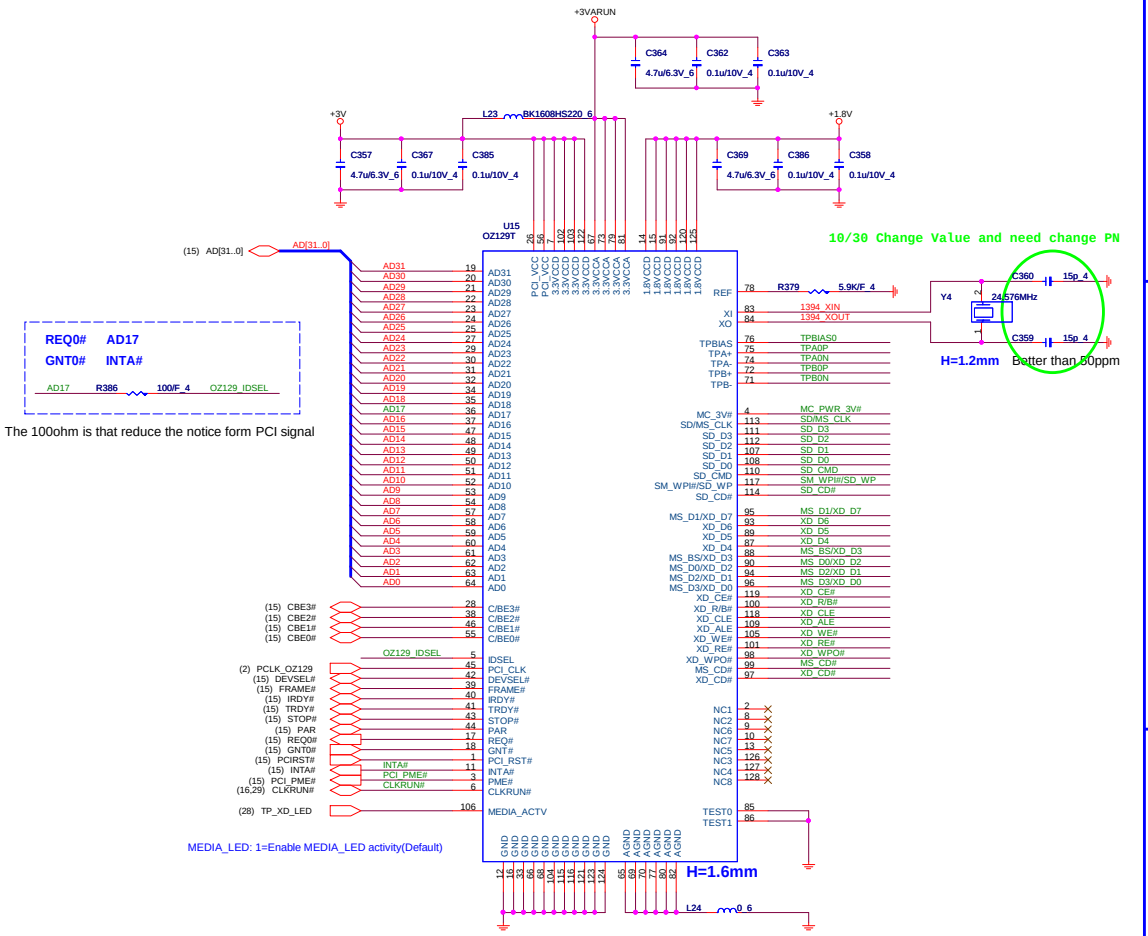
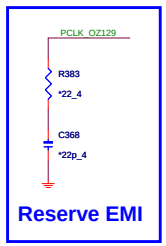
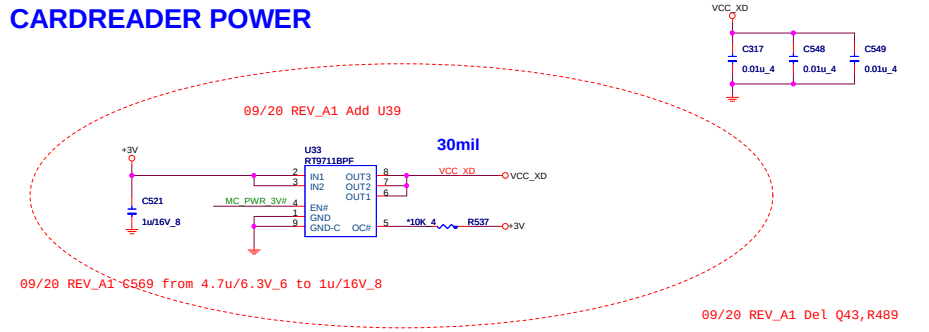


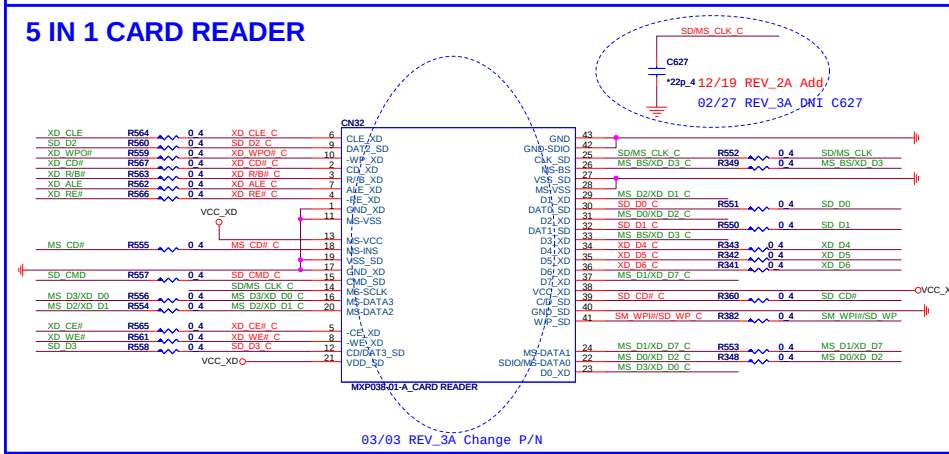


MMC

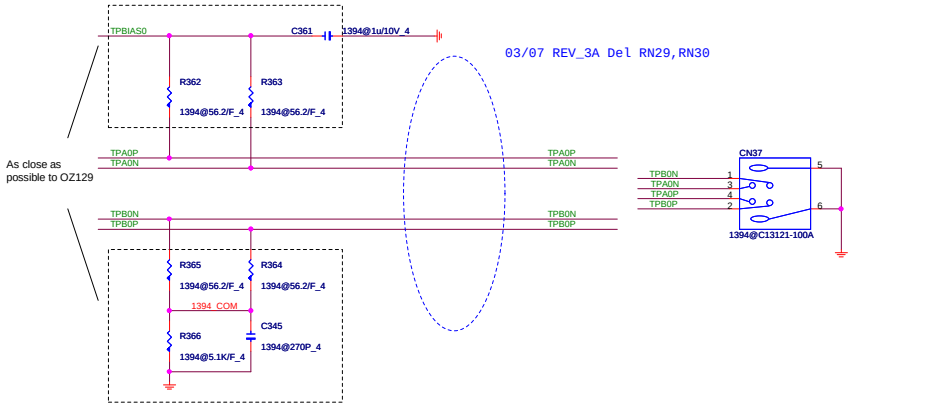
CARDREADER POWER



5 IN 1 CARD READER



1394



Quanta Computer Inc.
PROJECT : BL5M Montevina

Size	Document Number	Rev
	OZ129T (Card Reader/1394)	1A
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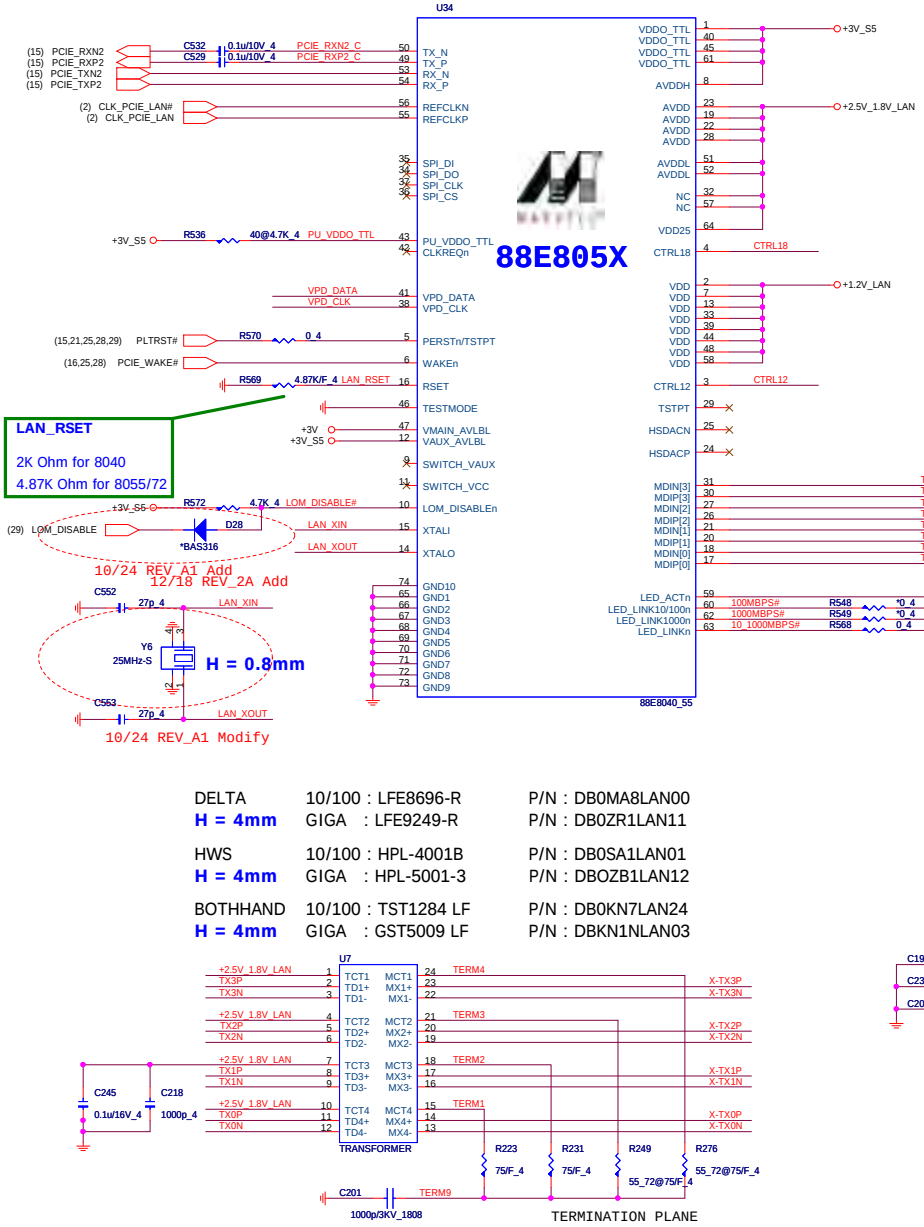
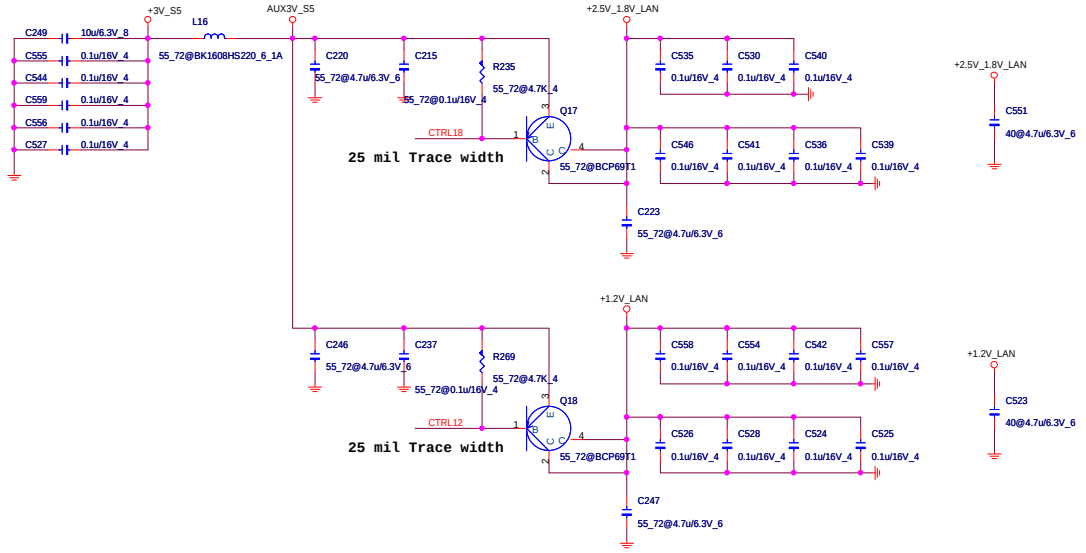
LAN_MARVELL_88E8040/88E8055

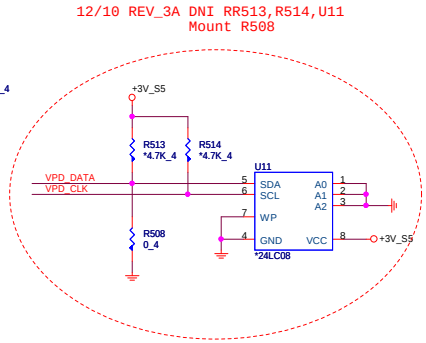
BOM Option Table

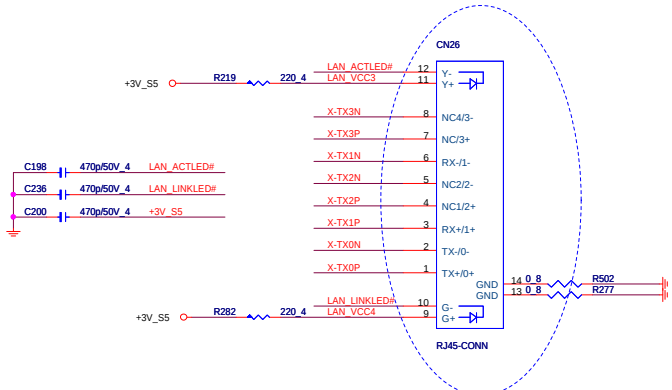
Reference	Description
40@	10/100 : 88E8040
55@	GIGA : 88E8055
55_72@	GIGA : 88E8072

10/100 : 88E8040 P/N : AL008040001
GIGA : 88E8055 P/N : AJ080550000
GIGA : 88E8072 P/N : AL008072000









DELTA 10/100 : LFE8696-R P/N : DB0MA8LAN00
H = 4mm GIGA : LFE9249-R P/N : DB0ZR1LAN11

HWS 10/100 : HPL-4001B P/N : DB0SA1LAN01
H = 4mm GIGA : HPL-5001-3 P/N : DBOZB1LAN12

BOTHHAND 10/100 : TST1284 LF P/N : DB0KN7LAN24
H = 4mm GIGA : GST5009 LF P/N : DBKN1NLAN03

Quanta Computer Inc.	
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Mini PCI-E Card
WLAN

MINI-Card I

09/28 REV_A1 Modify

03/14 REV_3A DNI

12/04 REV_2A Change to +3V_S5

12/04 REV_2A Change to +3V_S5

12/04 REV_2A Mount R24

10/30 Modify Wimax LED net.

12/04 REV_2A Change to +3V_S5

09/28 REV_A1 Modify

12/04 REV_2A Change to +3V_S5

12/13 REV_2A Add

03/03 REV_3A Add

To BT

MINI-Card II

09/20 REV_A1 Modify

12/23 REV_2A Change P/N

MINI-Card III

H= 8mm

EMI

12/20 REV_2A Add PAD

12/18 REV_2A Add C620~C626

12/18 REV_2A Add C618

Quanta Computer Inc.	
PROJECT : BL5M Montevina	
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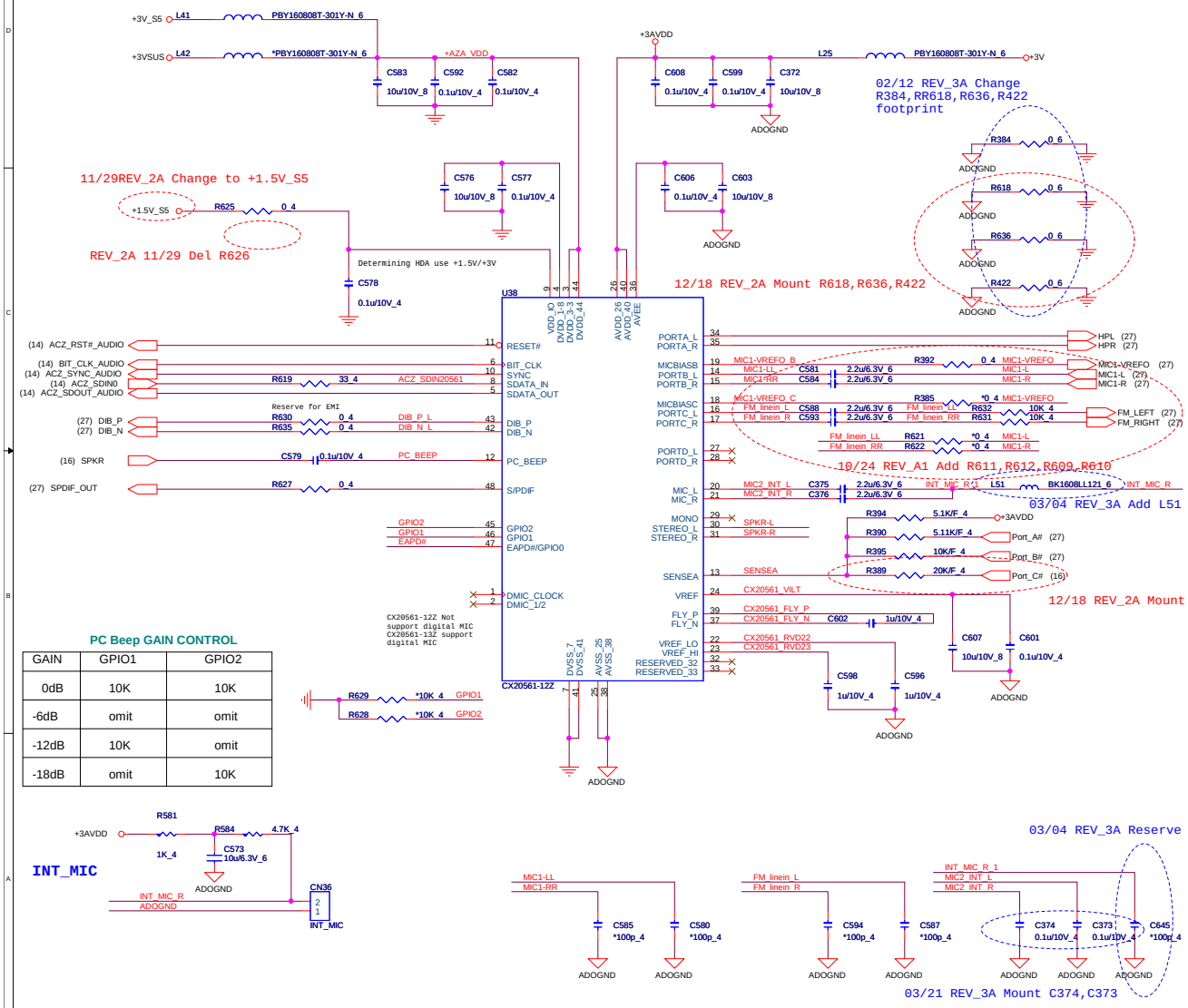
Codec(CX20561)

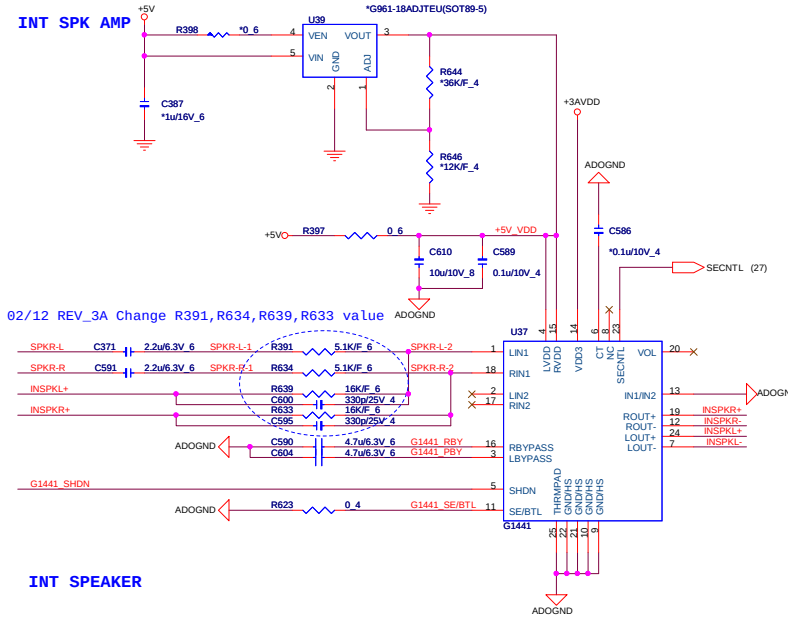


PC Beep GAIN CONTROL

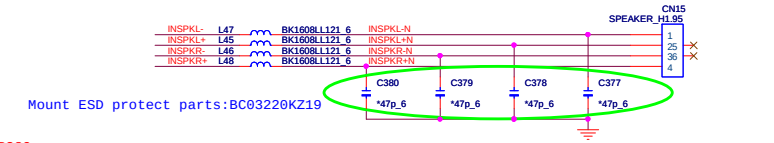
GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

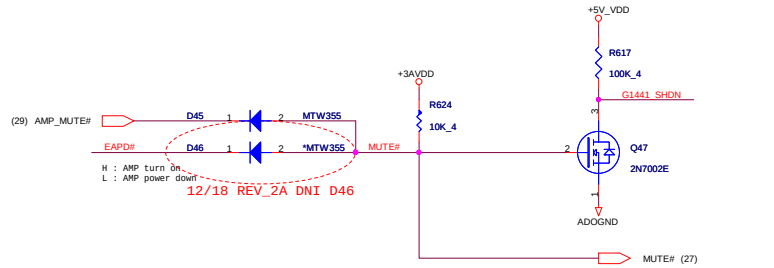
INT_MIC

INT SPK AMP



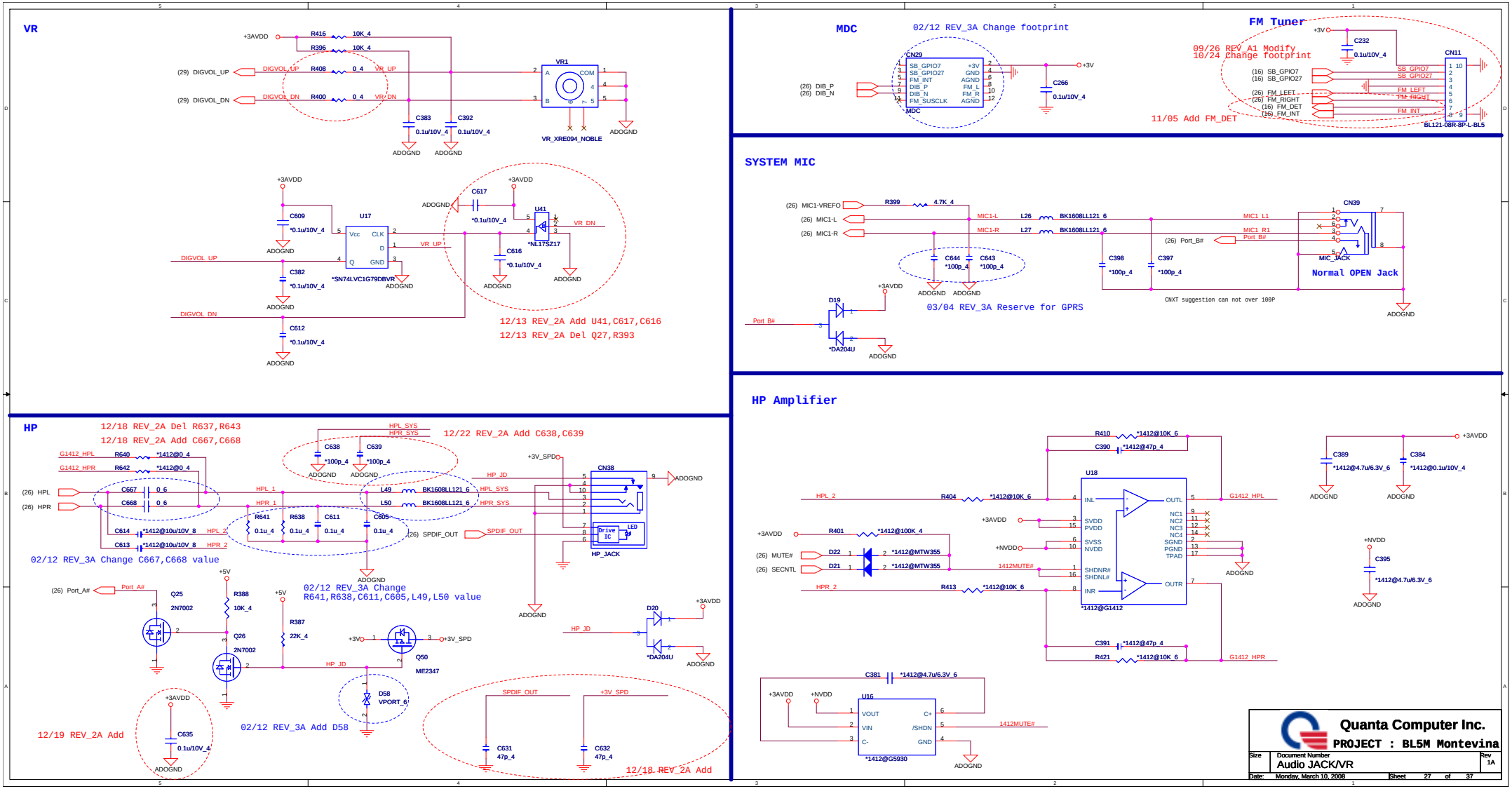
INT SPEAKER

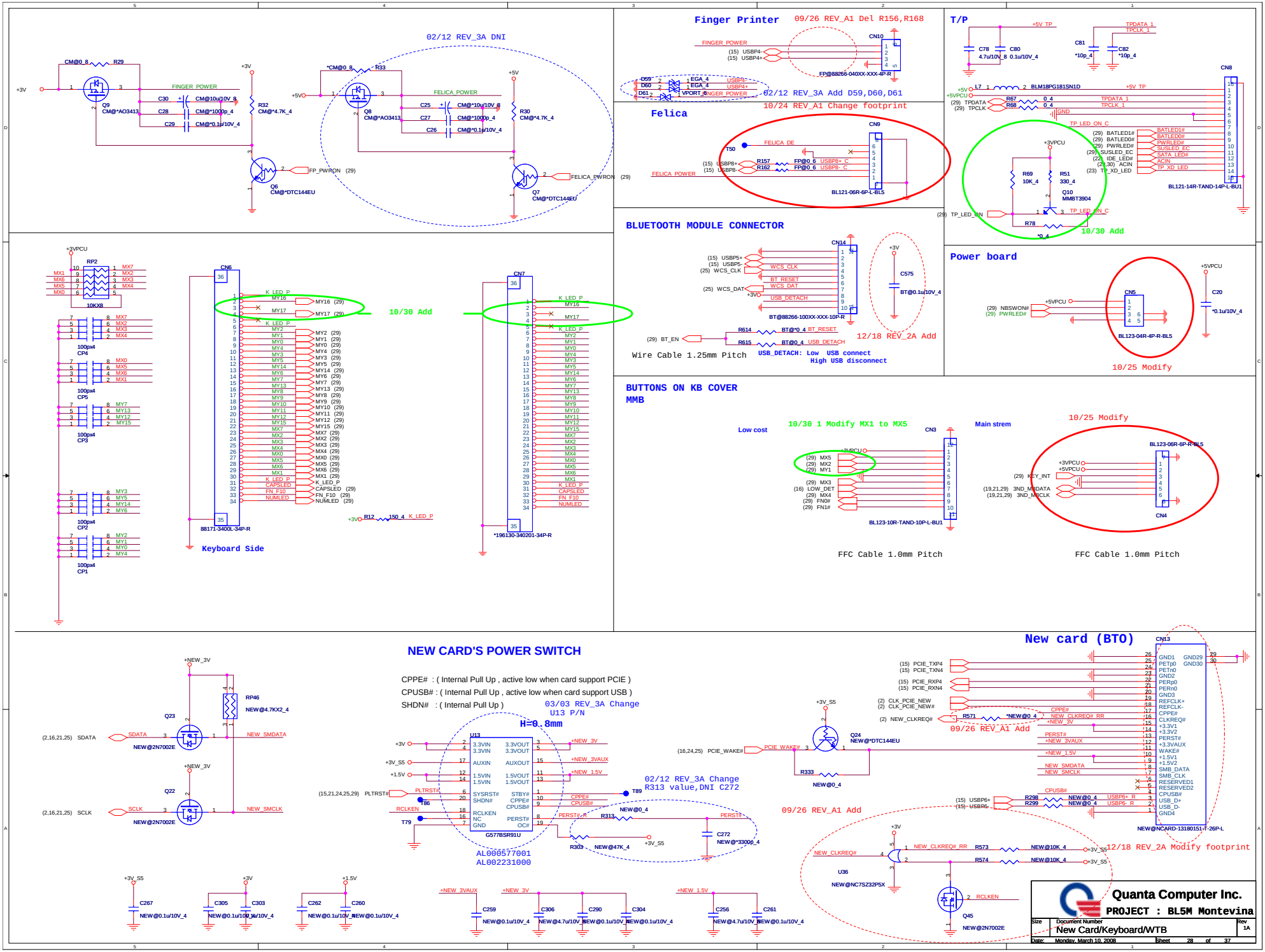




Quanta Computer Inc.
PROJECT : BL5M Montevina

Size	Document Number	Rev
	Conexant CX205601	1A
Date: Friday, March 21, 2008	Sheet 26 of 37	


VR
R416 10K_4
R396 10K_4
(29) DIGVOL_UP
DIGVOL_UP
R408 0_4
VR_UP
(29) DIGVOL_DN
DIGVOL_DN
R400 0_4
VR_DN
VR1
VR_XRE094_NOBLE
C383 0.1u/10V_4
C392 0.1u/10V_4
ADOGND
+3AVDD
C609 *0.1u/10V_4
U17
*SN74LVC1G79DBVR
C382 *0.1u/10V_4
C612 *0.1u/10V_4
C617 *0.1u/10V_4
U41
*NL17SZ17
C616 *0.1u/10V_4
12/13 REV_2A Add U41,C617,C616
12/13 REV_2A Del Q27,R393
MDC
02/12 REV_3A Change footprint
CN29
MDC
(26) DIB_P
(26) DIB_N
C266 0.1u/10V_4
FM Tuner
09/26 REV_A1 Modify
10/24 Change footprint
C232 0.1u/10V_4
CN11
BL121-08R-8P-L-BL5
(16) SB_GPIO7
(16) SB_GPIO27
(26) FM_LEFT
(26) FM_RIGHT
(16) FM_DET
(16) FM_INT
11/05 Add FM_DET
SYSTEM MIC
(26) MIC1-VREFO
(26) MIC1-L
(26) MIC1-R
R399 4.7K_4
L26 BK1608LL121_6
L27 BK1608LL121_6
C644 *100p_4
C643 *100p_4
C398 *100p_4
C397 *100p_4
CN39
MIC_JACK
Normal OPEN Jack
CNXT suggestion can not over 100P
03/04 REV_3A Reserve for GPRS
D19
*DA204U
HP
12/18 REV_2A Del R637,R643
12/18 REV_2A Add C667,C668
12/22 REV_2A Add C638,C639
G1412_HPL
G1412_HPR
R640 *1412@0_4
R642 *1412@0_4
(26) HPL
(26) HPR
C667 0_6
C668 0_6
C638 *100p_4
C639 *100p_4
L49 BK1608LL121_6
L50 BK1608LL121_6
R641 0.1u_4
R638 0.1u_4
C611 0.1u_4
C605 0.1u_4
C614 *1412@10u/10V_8
C613 *1412@10u/10V_8
CN38
HP_JACK
02/12 REV_3A Change C667,C668 value
02/12 REV_3A Change
R641,R638,C611,C605,L49,L50 value
Q25 2N7002
Q26 2N7002
R388 10K_4
R387 22K_4
Q50 ME2347
D20 *DA204U
D58 VPORT_6
02/12 REV_3A Add D58
12/19 REV_2A Add
C635 0.1u/10V_4
C631 47p_4
C632 47p_4
12/18 REV_2A Add
HP Amplifier
R410 *1412@10K_6
C390 *1412@47p_4
U18
*1412@G1412
R404 *1412@10K_6
R401 *1412@100K_4
D22 *1412@MTW355
D21 *1412@MTW355
R413 *1412@10K_6
C391 *1412@47p_4
R421 *1412@10K_6
C389 *1412@4.7u/6.3V_6
C384 *1412@0.1u/10V_4
C395 *1412@4.7u/6.3V_6
C381 *1412@4.7u/6.3V_6
U16
*1412@G5930
1412MUTE#
G1412_HPL
G1412_HPR
Quanta Computer Inc.
PROJECT : BL5M Montevina
Size
Document Number
Audio JACK/VR
Rev 1A
Date: Monday, March 10, 2008
Sheet 27 of 37


02/12 REV_3A DNI
CM@0_8
R29
+3V
FINGER_POWER
C30
CM@10u/10V_8
C28
CM@*1000p_4
C29
CM@*0.1u/10V_4
R32
CM@*4.7K_4
Q9
CM@*AO3413
Q6
CM@*DTC144EU
FP_PWRON (29)
*CM@0_8
R33
+5V
FELICA_POWER
C25
CM@*10u/10V_8
C27
CM@*1000p_4
C26
CM@*0.1u/10V_4
R30
CM@*4.7K_4
Q8
CM@*AO3413
Q7
CM@*DTC144EU
FELICA_PWRON (29)
Finger Printer
09/26 REV_A1 Del R156,R168
CN10
FINGER_POWER
(15) USBP4-
(15) USBP4+
FP@88266-040XX-XXX-4P-R
D59
D60
D61
EGA_4
VPORT_6
02/12 REV_3A Add D59,D60,D61
10/24 REV_A1 Change footprint
Felica
CN9
FELICA_DE
T50
FELICA_POWER
(15) USBP8+
(15) USBP8-
R157
R162
FP@0_6 USBP8+_C
FP@0_6 USBP8-_C
BL121-06R-6P-L-BL5
T/P
+5V_TP
C78
4.7u/10V_8
C80
0.1u/10V_4
C81
*10p_4
C82
*10p_4
TPDATA_1
TPCLK_1
CN8
L7
BLM18PG181SN1D
+5VPCU
(29) TPDATA
(29) TPCLK
R67
R68
0_4
GND
TP_LED_ON_C
(29) BATLED1#
(29) BATLED0#
(29) PWRLED#
(29) SUSLED_EC
(22) IDE_LED#
(24,30) ACIN
(23) TP_XD_LED
BATLED1#
BATLED0#
PWRLED#
SUSLED_EC
SATA_LED#
ACIN
TP_XD_LED
BL121-14R-TAND-14P-L-BU1
+3VPCU
R69
10K_4
R51
330_4
Q10
MMBT3904
(29) TP_LED_ON
R78
*0_4
10/30 Add
BLUETOOTH MODULE CONNECTOR
CN14
(15) USBP5+
(15) USBP5-
(25) WCS_CLK
(25) WCS_DAT
BT_RESET
WCS_DAT
USB_DETACH
BT@88266-100XX-XXX-10P-R
C575
BT@0.1u/10V_4
(29) BT_EN
R614
BT@*0_4 BT_RESET
R615
BT@0_4 USB_DETACH
12/18 REV_2A Add
Wire Cable 1.25mm Pitch
USB_DETACH: Low USB connect
High USB disconnect
Power board
CN5
(29) NBSWON#
(29) PWRLED#
C20
*0.1u/10V_4
BL123-04R-4P-R-BL5
10/25 Modify
RP2
10K8
MX1
MX6
MX5
MX0
100px4
CP4
CP5
CP3
CP2
CP1
CN6
K_LED_P
MY16 (29)
MY17 (29)
MY2 (29)
MY1 (29)
MY0 (29)
MY4 (29)
MY3 (29)
MY5 (29)
MY14 (29)
MY6 (29)
MY7 (29)
MY13 (29)
MY8 (29)
MY9 (29)
MY10 (29)
MY11 (29)
MY12 (29)
MY15 (29)
MX7 (29)
MX2 (29)
MX3 (29)
MX4 (29)
MX0 (29)
MX5 (29)
MX6 (29)
MX1 (29)
CAPSLED (29)
FN_F10 (29)
NUMLED (29)
88171-3400L-34P-R
Keyboard Side
10/30 Add
R12
150_4
CN7
*196130-340201-34P-R
BUTTONS ON KB COVER
MMB
Low cost
10/30 1 Modify MX1 to MX5
CN3
(29) MX5
(29) MX2
(29) MY1
(29) MY3
(16) LOW_DET
(29) MX4
(29) FN0#
(29) FN1#
BL123-10R-TAND-10P-L-BU1
FFC Cable 1.0mm Pitch
Main strem
10/25 Modify
BL123-06R-6P-R-BL5
+3VPCU
(29) KEY_INT
(19,21,29) 3ND_MSDATA
(19,21,29) 3ND_MSCLK
CN4
FFC Cable 1.0mm Pitch
NEW CARD'S POWER SWITCH
CPPE# : (Internal Pull Up , active low when card support PCIE)
CPUSB# : (Internal Pull Up , active low when card support USB)
SHDN# : (Internal Pull Up)
03/03 REV_3A Change
U13 P/N
H=0.8mm
+NEW_3V
Q23
RP46
NEW@4.7KX2_4
(2,16,21,25) SDATA
NEW@2N7002E
NEW_SMDATA
Q22
(2,16,21,25) SCLK
NEW_SMCLK
U13
G577BSR91U
+3V
+3V_S5
+1.5V
(15,21,24,25,29) PLTRST#
RCLKEN
T86
T79
T89
+NEW_3VAUX
+NEW_1.5V
CPPE#
CPUSB#
PERST#
R313
R303
NEW@47K_4
C272
NEW@*3300p_4
02/12 REV_3A Change
R313 value,DNI C272
AL000577001
AL002231000
09/26 REV_A1 Add
Q24
NEW@*DTC144EU
(16,24,25) PCIE_WAKE#
R333
NEW@0_4
New card (BTO)
CN13
(15) PCIE_TXP4
(15) PCIE_TXN4
(15) PCIE_RXP4
(15) PCIE_RXN4
(2) CLK_PCIE_NEW
(2) CLK_PCIE_NEW#
(2) NEW_CLKREQ#
R571
*NEW@0_4
CPPE#
NEW_CLKREQ# RR
PERST#
WAKE#
+3.3V1
+3.3V2
CLKREQ#
+1.5V1
+1.5V2
SMB_DATA
SMB_CLK
RESERVED1
RESERVED2
CPUSB#
USB_D+
USB_D-
GND4
(15) USBP6+
(15) USBP6-
R298
R299
USBP6+_R
USBP6-_R
NEW@NCARD-13180151-T-26P-L
12/18 REV_2A Modify footprint
U36
NEW@NC7SZ32P5X
R573
R574
NEW@10K_4
Q45
NEW@2N7002E
C267
C305
C303
C262
C260
C259
C306
C290
C304
C256
C261
NEW@0.1u/10V_4
NEW@4.7u/10V_4
Quanta Computer Inc.
PROJECT : BL5M Montevina
Size
Document Number
New Card/Keyboard/WTB
Rev
1A
Date: Monday, March 10, 2008
Sheet 28 of 37

Page 29 copy from BL5S

10/26 REV_A1 Add R64,R73,R176

09/20 REV_A1 Modify

09/29 REV_A1 Modify

10/26 REV_A1 Modify

10/22 REV_A1 Modify

03/03 REV_3A Add WMAX_P net

02/12 REV_3A Add to control MMB LED

10/22 REV_A1 Modify

10/24 REV_A1 Add

10/22 REV_A1 Modify

09/20 REV_A1 Modify

11/05 Add

11/01 Del D12

SMBUS Table

SMBUS	Devices
1	Battery
2	CPU Thermal Sensor 3D Sensor EC EEPROM
3	VGA Board Thermal Sensor Touch Sensor

SM BUS PU

I/O Base Address

BADDR1-0	I/O Address	
	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

12/18 REV_2A R54 DNI,R56 mount

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID

H=1.75mm

ADDRESS: A0H

SPI FLASH

H=2.16mm

INTERNAL KEYBOARD STRIP SET

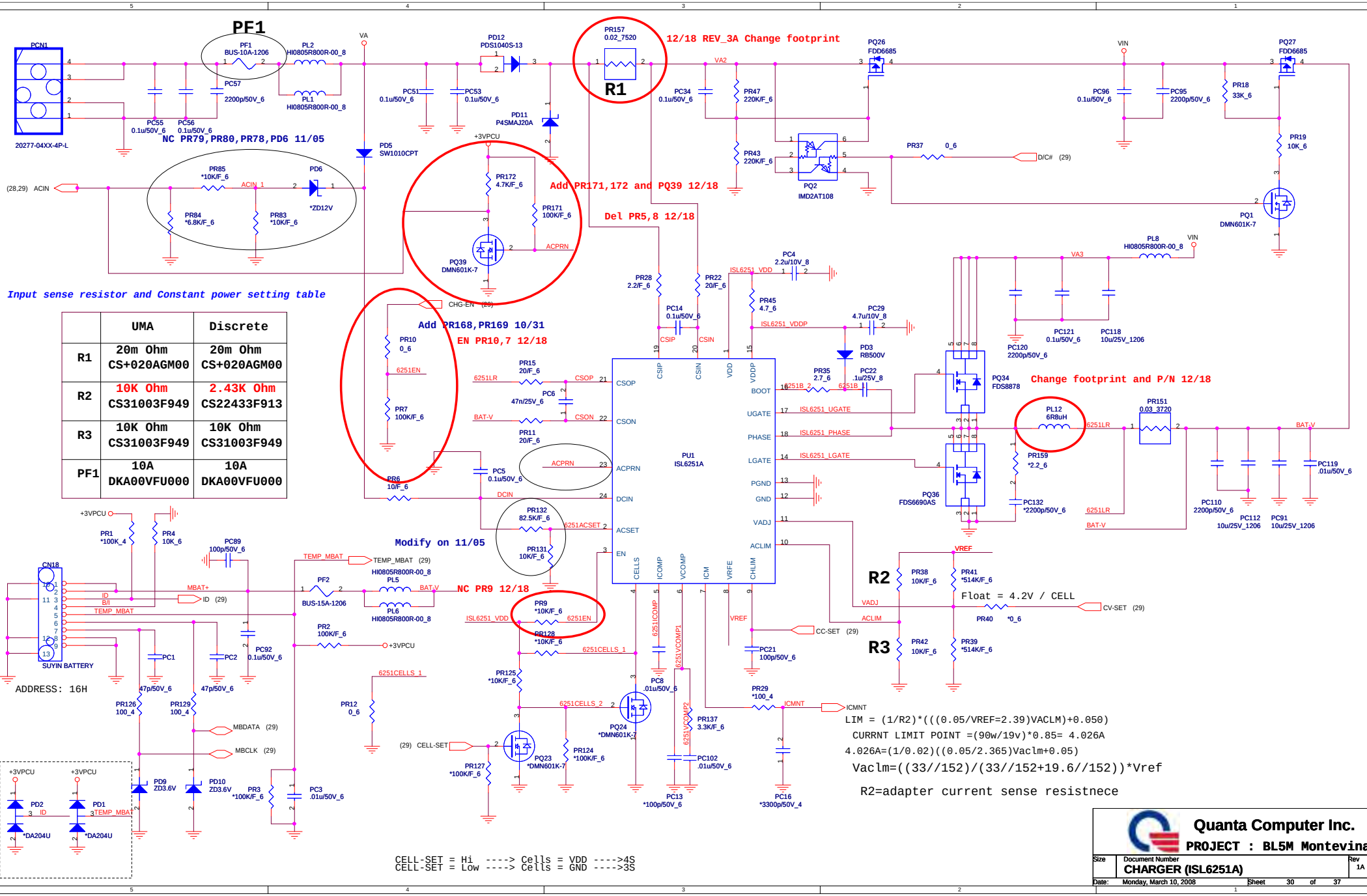
CIR (Copy from PB2A)

Only for 8769/775C

10/19 REV_A1 Change footprint
10/21 REV_A1 Change pin define

H=1.6mm

Quanta Computer Inc.	
PROJECT : BL5M Montevina	
Size	Document Number: EC-WPCE775C — Rev: 1A
Date: Monday, March 10, 2008	Sheet 29 of 37

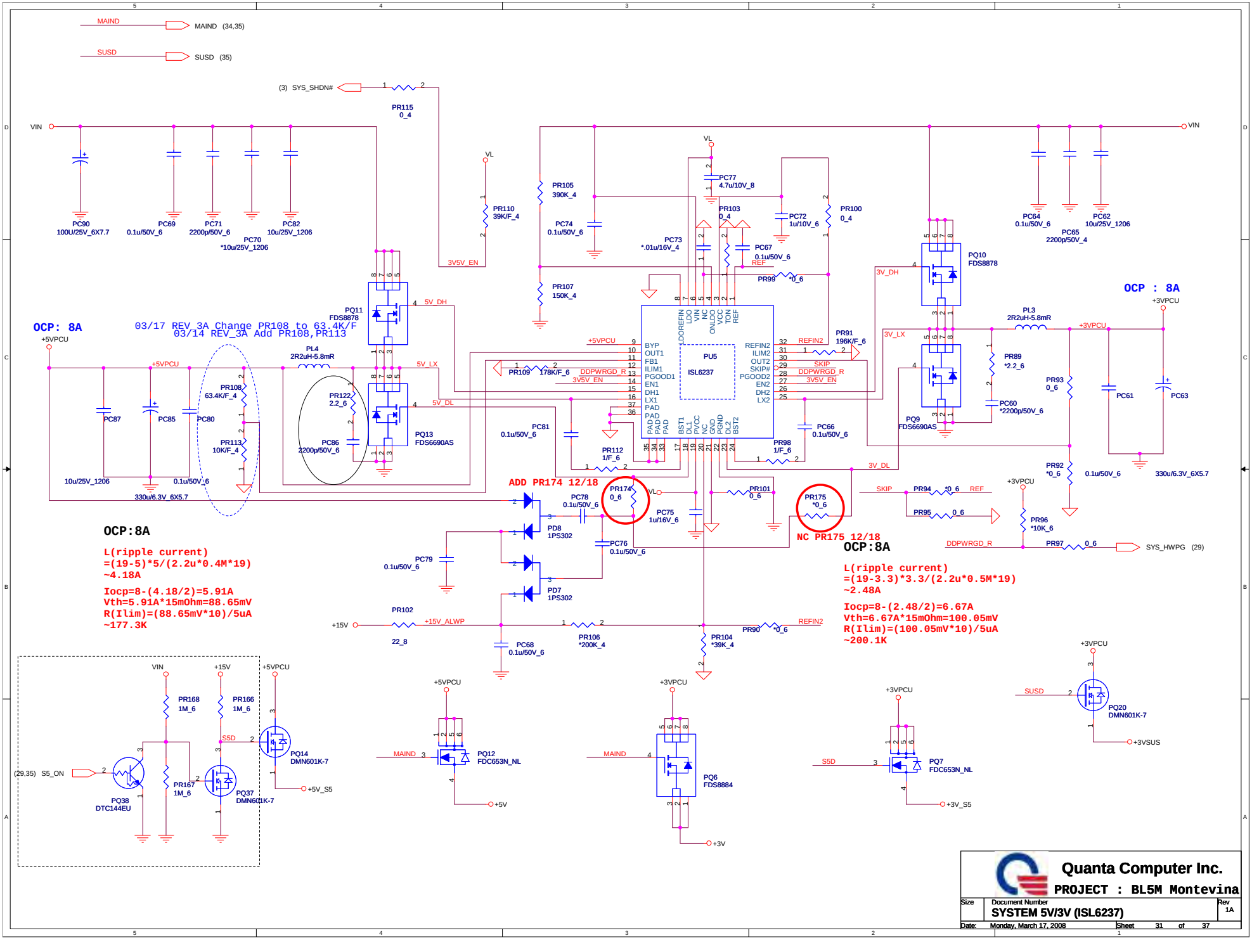


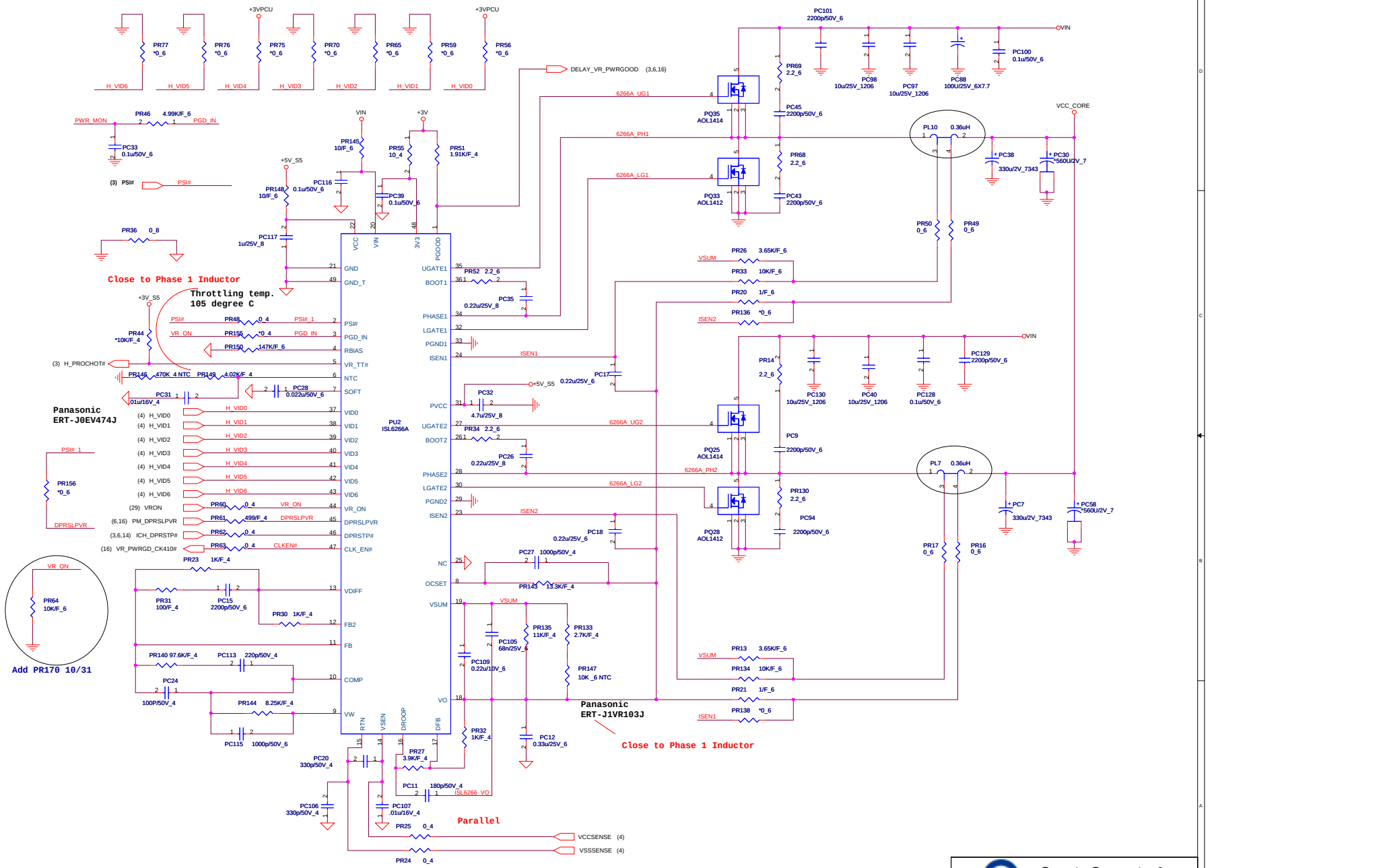
	UMA	Discrete
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	10K Ohm CS31003F949	2.43K Ohm CS22433F913
R3	10K Ohm CS31003F949	10K Ohm CS31003F949
PF1	10A DKA00VFU000	10A DKA00VFU000

Quanta Computer Inc.
PROJECT : BL5M Montevina

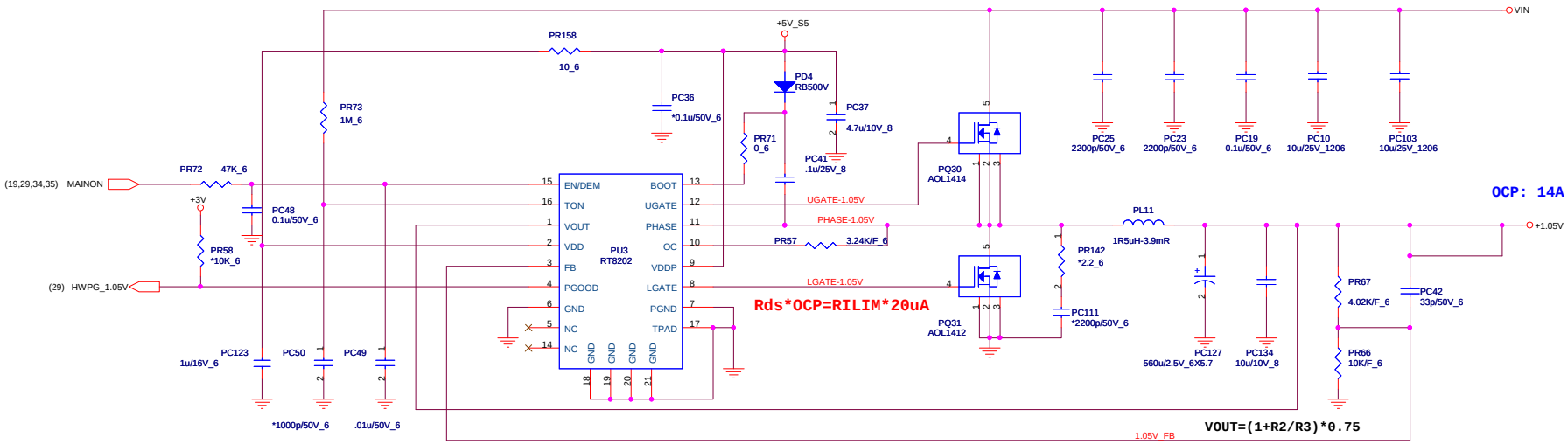
Size	Document Number	Rev
	CHARGER (ISL6251A)	1A

Date: Monday, March 10, 2008 Sheet 30 of 37


MAIND
MAIND (34,35)
SUSD
SUSD (35)
(3) SYS_SHDN#
PR115 0_4
VIN
PC90 100U/25V_6X7.7
PC69 0.1u/50V_6
PC71 2200p/50V_6
PC70 *10u/25V_1206
PC82 10u/25V_1206
VL
PR110 39K/F_4
3V5V_EN
PR105 390K_4
PC74 0.1u/50V_6
PR107 150K_4
PC77 4.7u/10V_8
PR103 0_4
PC72 1u/10V_6
PR100 0_4
PC73 *.01u/16V_4
PC67 0.1u/50V_6
REF
PR99 *0_6
PC64 0.1u/50V_6
PC65 2200p/50V_4
PC62 10u/25V_1206
OCP: 8A
03/17 REV_3A Change PR108 to 63.4K/F
03/14 REV_3A Add PR108,PR113
+5VPCU
PL4 2R2uH-5.8mR
5V_LX
5V_DH
5V_DL
PQ11 FDS8878
PQ13 FDS6690AS
PR108 63.4K/F_4
PR113 10K/F_4
PR122 2.2_6
PC86 2200p/50V_6
PC87
PC85
PC80
10u/25V_1206
0.1u/50V_6
330u/6.3V_6X5.7
PR109 178K/F_6
DDPWRGD_R
PC81 0.1u/50V_6
PR112 1/F_6
PU5 ISL6237
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
LDOREFIN
LDO
VIN
NC
ONLDO
VCC
TON
REF
BST1
DL1
PVCC
NC
GND
PGND
DL2
BST2
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
PR91 196K/F_6
PC66 0.1u/50V_6
PR98 1/F_6
3V_DL
ADD PR174 12/18
PR174 0_6
PC78 0.1u/50V_6
PD8 1PS302
PC76 0.1u/50V_6
PC79 0.1u/50V_6
PD7 1PS302
PC75 1u/16V_6
PR101 0_6
PR175 *0_6
NC PR175 12/18
SKIP
PR94 *0_6
PR95 0_6
REF
PR96 *10K_6
PR97 0_6
SYS_HWPG (29)
PR92 *0_6
0.1u/50V_6
330u/6.3V_6X5.7
PC61
PC63
PR89 *2.2_6
PC60 *2200p/50V_6
PR93 0_6
PQ10 FDS8878
PQ9 FDS6690AS
3V_DH
3V_LX
PL3 2R2uH-5.8mR
OCP : 8A
OCP:8A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=8-(4.18/2)=5.91A
Vth=5.91A*15mOhm=88.65mV
R(Ilim)=(88.65mV*10)/5uA
~177.3K
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=100.05mV
R(Ilim)=(100.05mV*10)/5uA
~200.1K
+15V
+15V_ALWP
PR102 22_8
PC68 0.1u/50V_6
PR106 *200K_4
PR104 *39K_4
PR90 *0_6
REFIN2
VIN
+15V
+5VPCU
PR168 1M_6
PR166 1M_6
S5D
PQ14 DMN601K-7
+5V_S5
(29,35) S5_ON
PR167 1M_6
PQ38 DTC144EU
PQ37 DMN601K-7
+5VPCU
MAIND
PQ12 FDC653N_NL
+5V
+3VPCU
MAIND
PQ6 FDS8884
+3V
+3VPCU
S5D
PQ7 FDC653N_NL
+3V_S5
+3VPCU
SUSD
PQ20 DMN601K-7
+3VSUS
Quanta Computer Inc.
PROJECT : BL5M Montevina
Size
Document Number
SYSTEM 5V/3V (ISL6237)
Rev 1A
Date: Monday, March 17, 2008
Sheet 31 of 37



Quanta Computer Inc.		
PROJECT : BL5M Montevina		
Size	Document Number: CPU CORE(ISL6266A)	Rev: 1A
Date: Monday, March 10, 2008	Sheet 32 of 37	

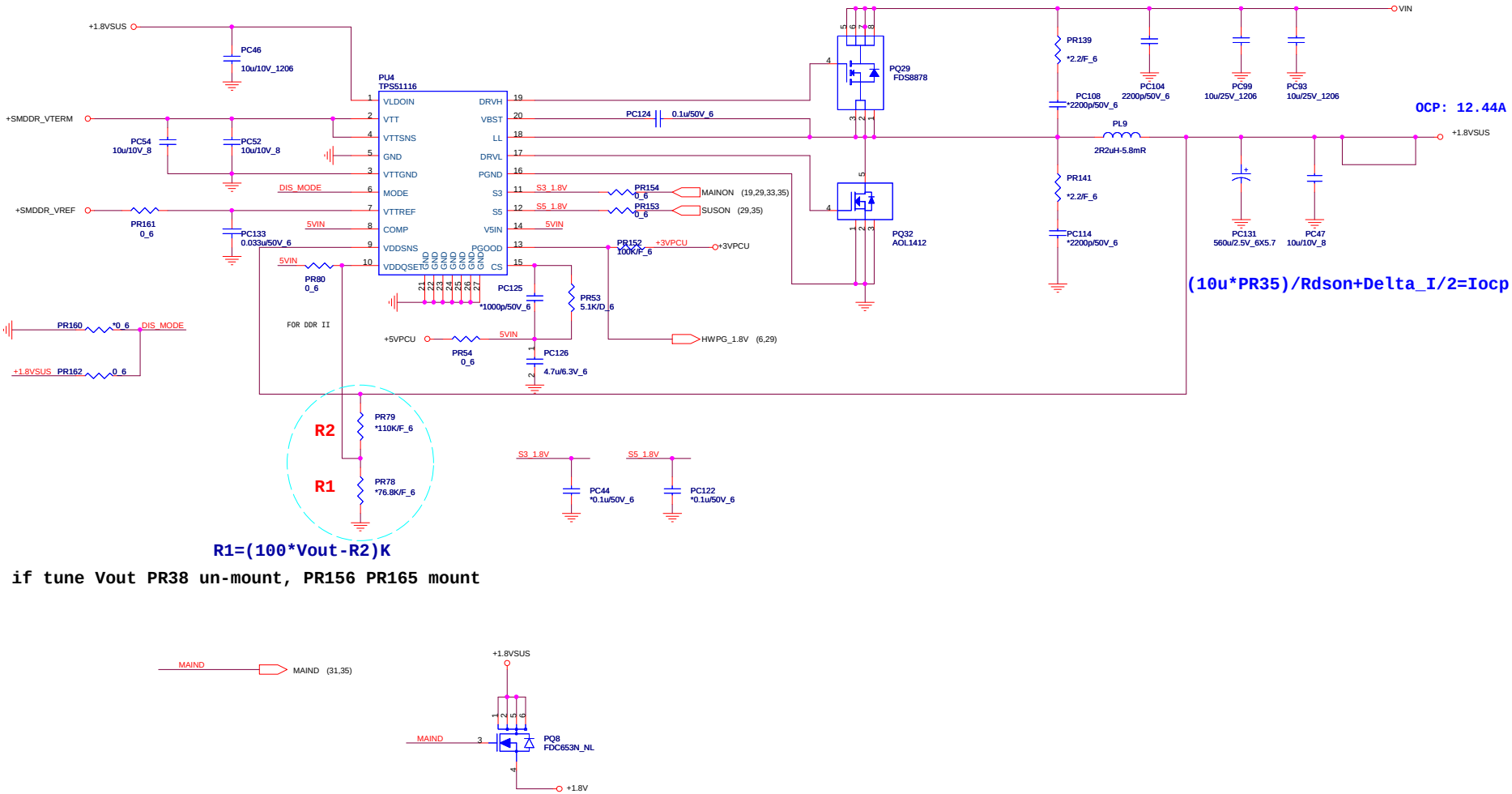


TON=3.85p*RTON*Vout/(Vin-0.5)

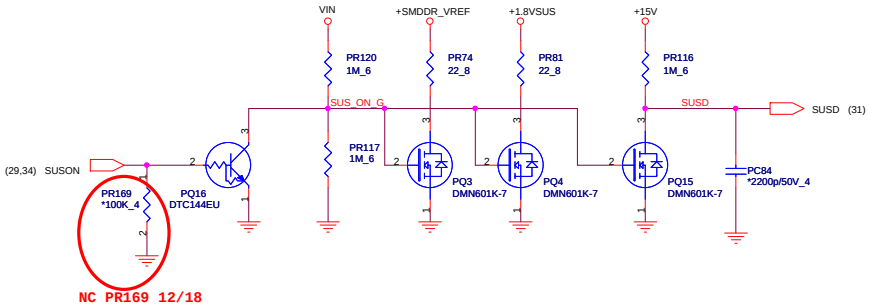
Frequency=Vout/(Vin*TON)

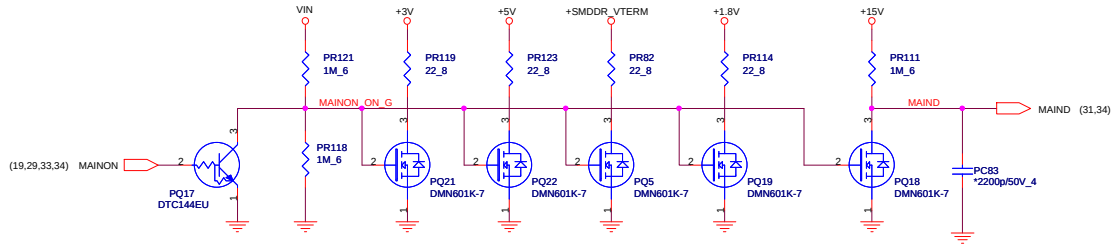
AOL1412 Rds=4.6mOhm
14A OCP --- OC=3.22K

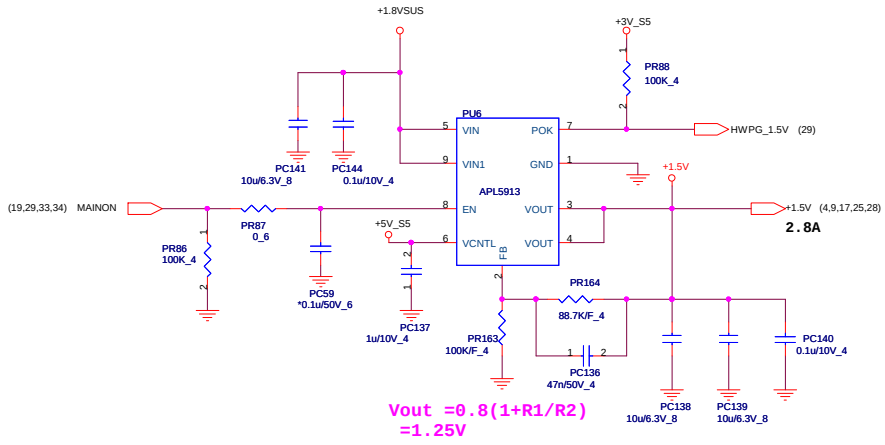
Quanta Computer Inc.		
PROJECT : BL5M Montevina		
Size	Document Number: VTT 1.05V (RT8202)	Rev: 1A
Date: Monday, March 10, 2008	Sheet 33 of 37	

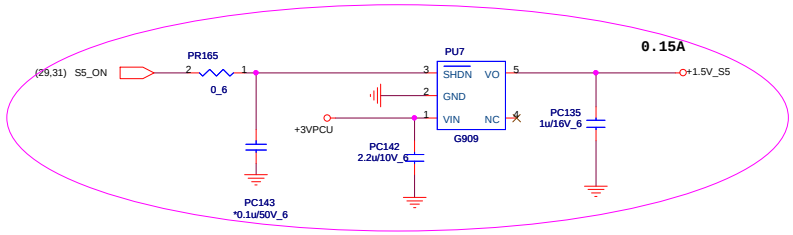


Quanta Computer Inc.		
PROJECT : BL5M Montevina		
Size	Document Number: DDR 1.8V(TPS51116)	Rev: 1A
Date: Monday, March 10, 2008	Sheet 34 of 37	









Quanta Computer Inc.

PROJECT : BL5M Montevina

Size	Document Number	Rev
	Discharge (1.25V/1.5V)	1A

Date: Monday, March 10, 2008 Sheet 35 of 37

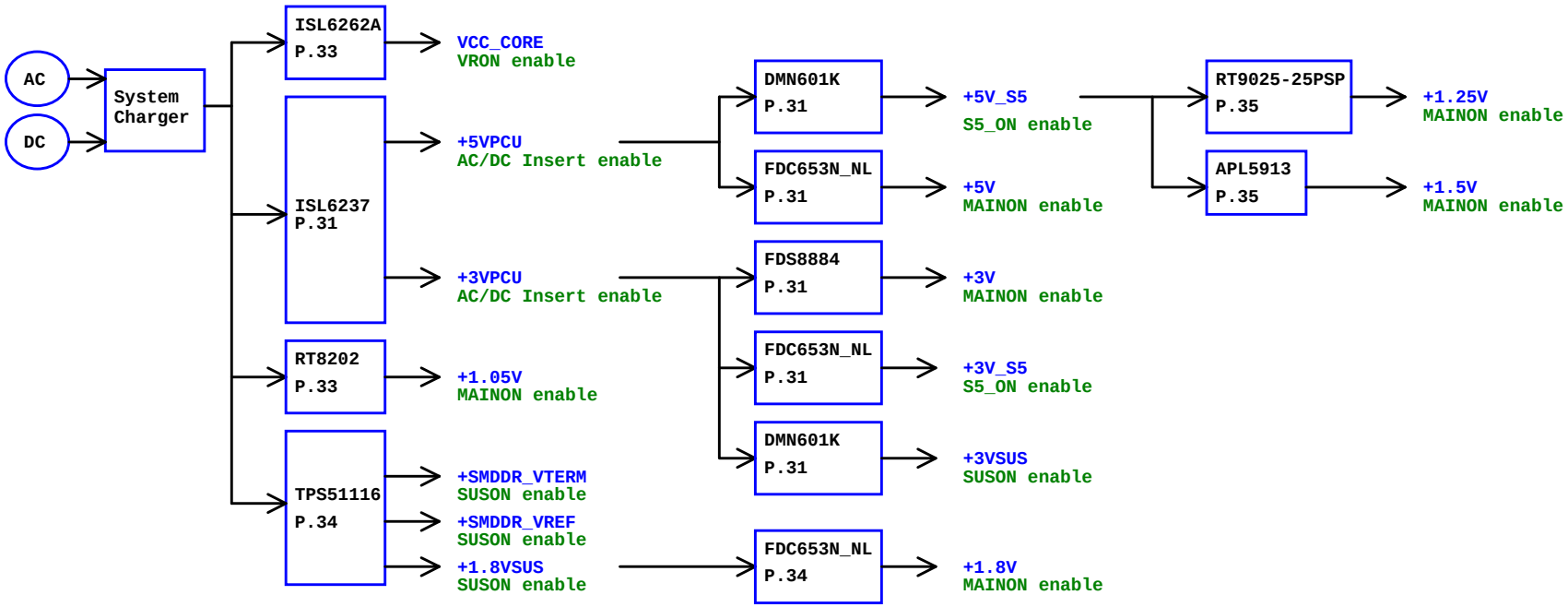
Model	REV	DATE	CHANGE LIST	NOTE
BL5S	00	20070824	FIRST RELEASED : 20070824	
	1A	20070914	FIRST RELEASED : E200709-2519	

Quanta Computer Inc.

PROJECT : BL5M Montevina

Size	Document Number	Rev
	Change List	1A

Date: Tuesday, March 04, 2008 Sheet 36 of 37



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+1.8VSUS	GMCH, DDR
+SMDDR_VREF	GMCH, DDR
+SMDDR_VTERM	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T) Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	HDMI, Cardreader (OZ129T)
+1.25V	CLK, GMCH, ICH8M