

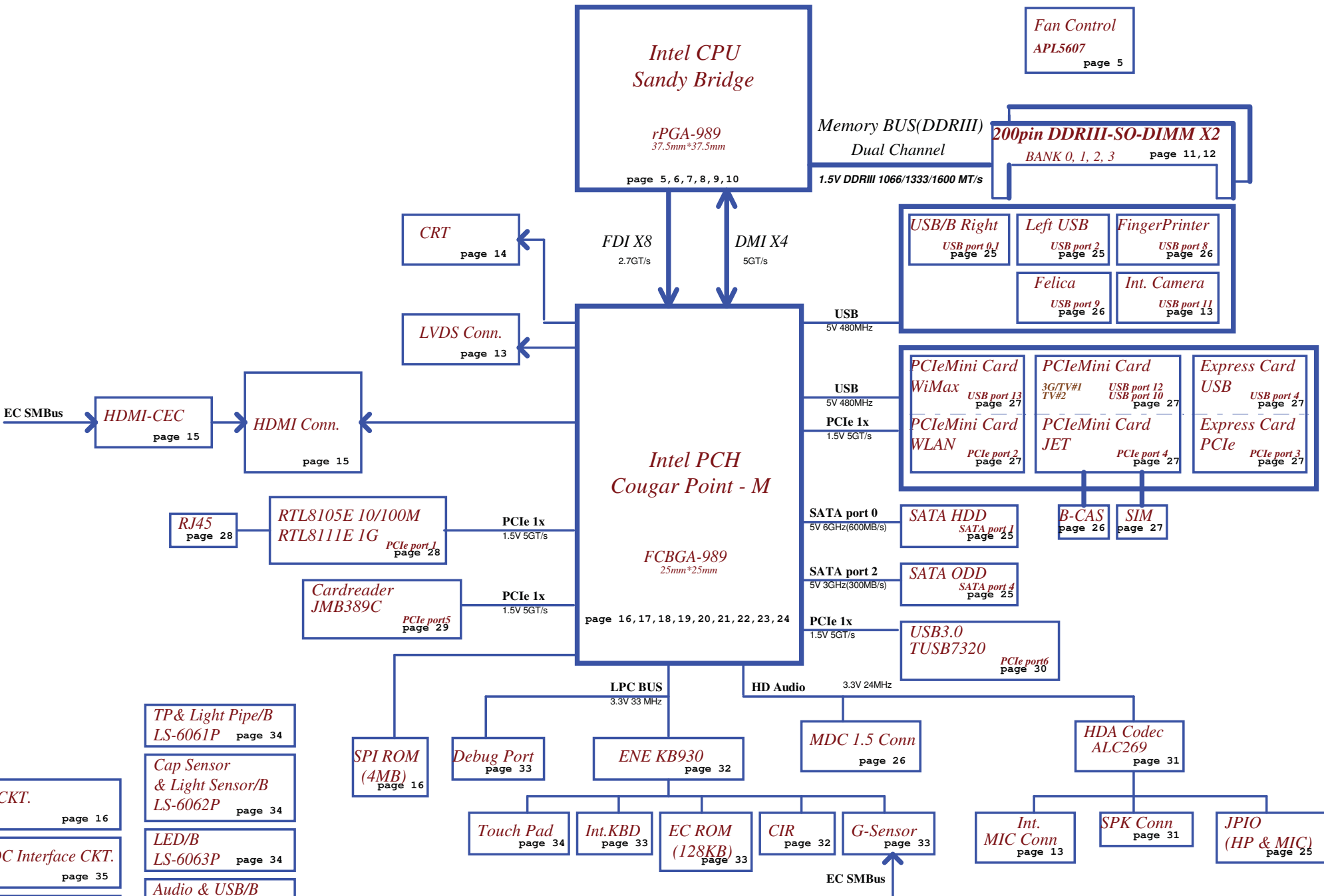
PHQAA

Marseille 10R/10RG

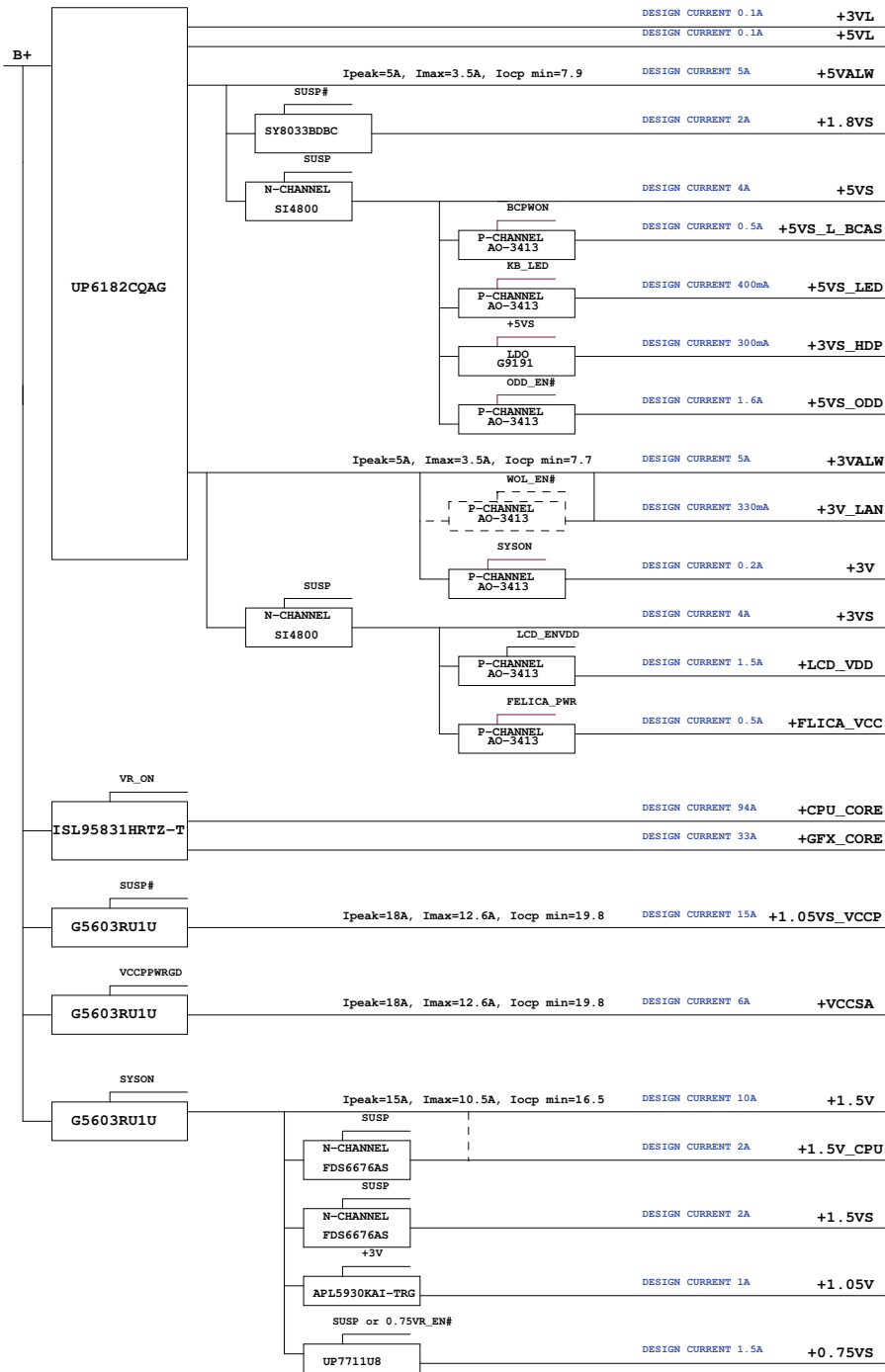
LA-6832P REV 0.2 Schematic

Intel Processor(Sandy Bridge) / PCH(Cougar Point)
2010-09-03 Rev 0.1

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				Cover Page	
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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b
Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9A H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	Light Sensor	52 H	0101 0010 b

BTO Option Table

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/ Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	MDC@	CIR@	KBL@

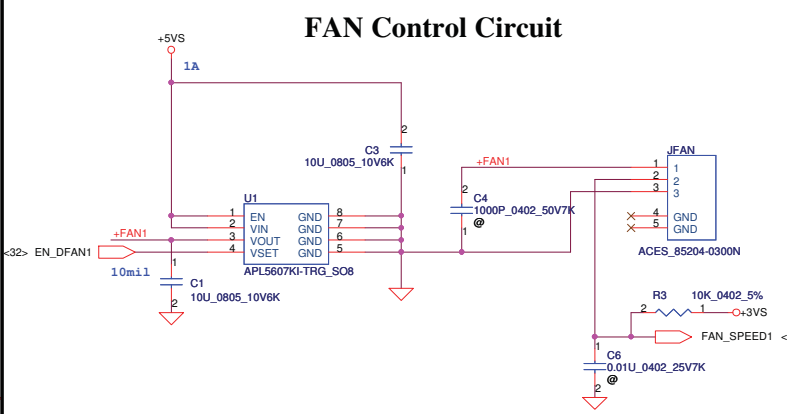
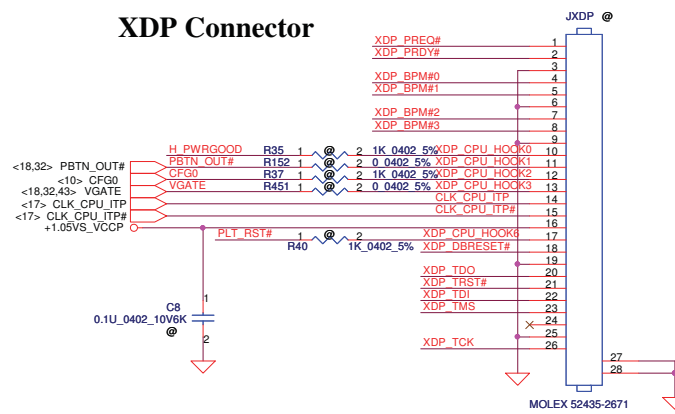
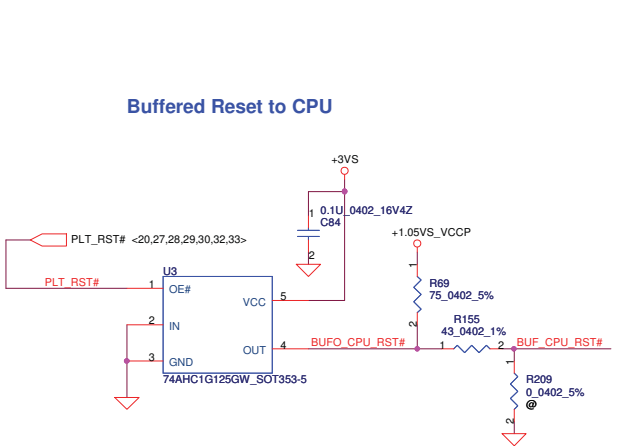
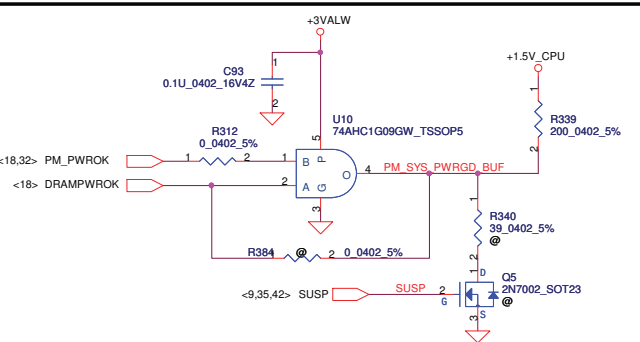
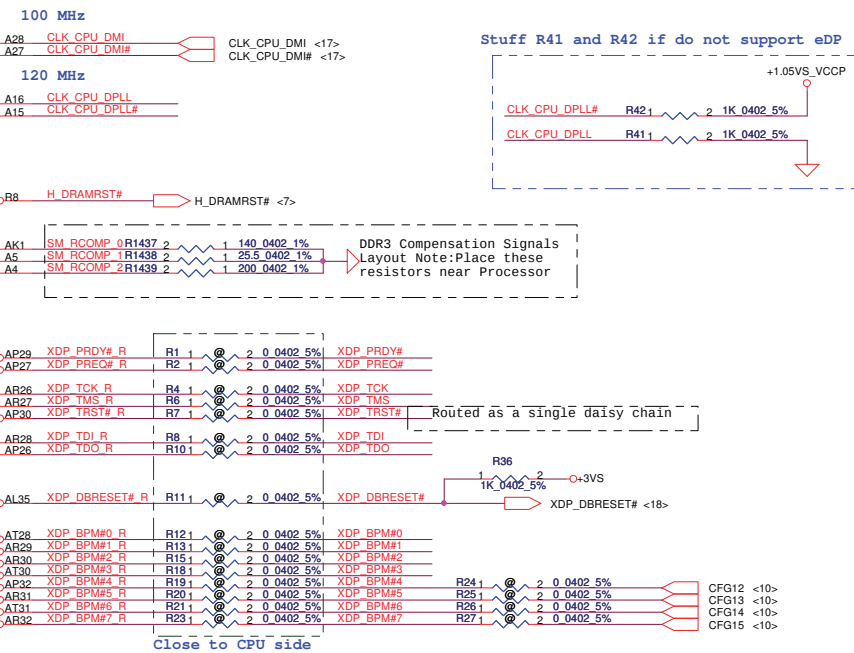
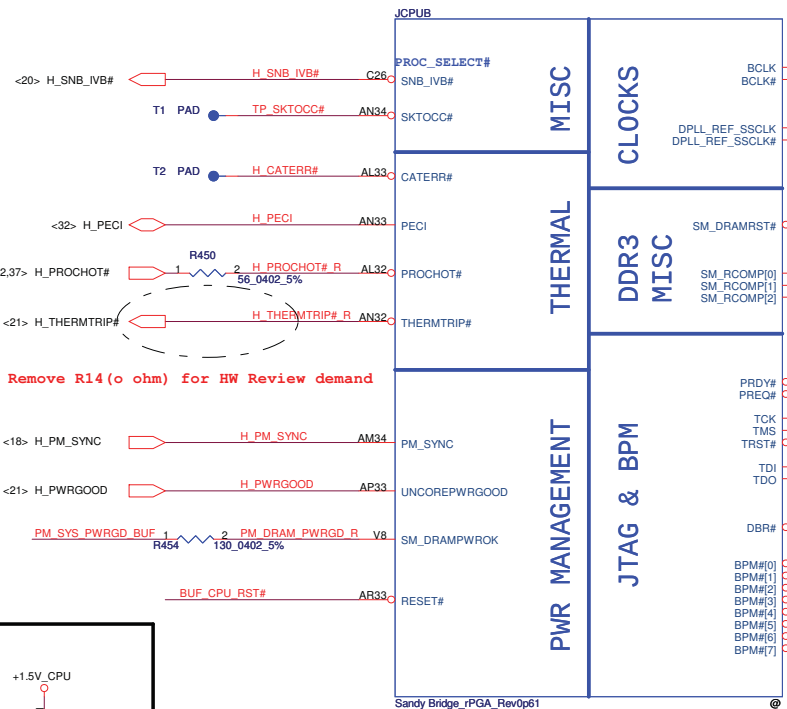
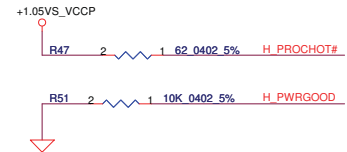
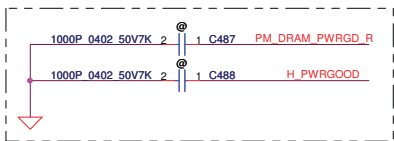
Function	Felica	BLUE TOOTH	G-SENSOR	SKU		LVDS		Camera & Mic	
description	Felica	BLUE TOOTH	G-SENSOR	SKU		3D Panel		Camera & Mic	
explain	Felica	BLUE TOOTH	G-SENSOR	Discrete	Optimus	Discrete		Optimus	Camera & Mic
BTO	FELICA@	BT@	GSENSOR@	DIS@	OPT@	3D@	NO3D@	OPTFH@	CAM@

Function	S3 Power Saving		GPU					
description	S3 Power Saving		N11P & N11E			N11M		
explain	No Power Saving	Power Saving	VRAM	N11P	N11E	N11M-GE1	N11M-GE2	N11M-OP1
BTO	NOPS@	PS@	8PCS@	N11P@	N11E@	N11MGE1@	N11MGE2@	N11MOP@

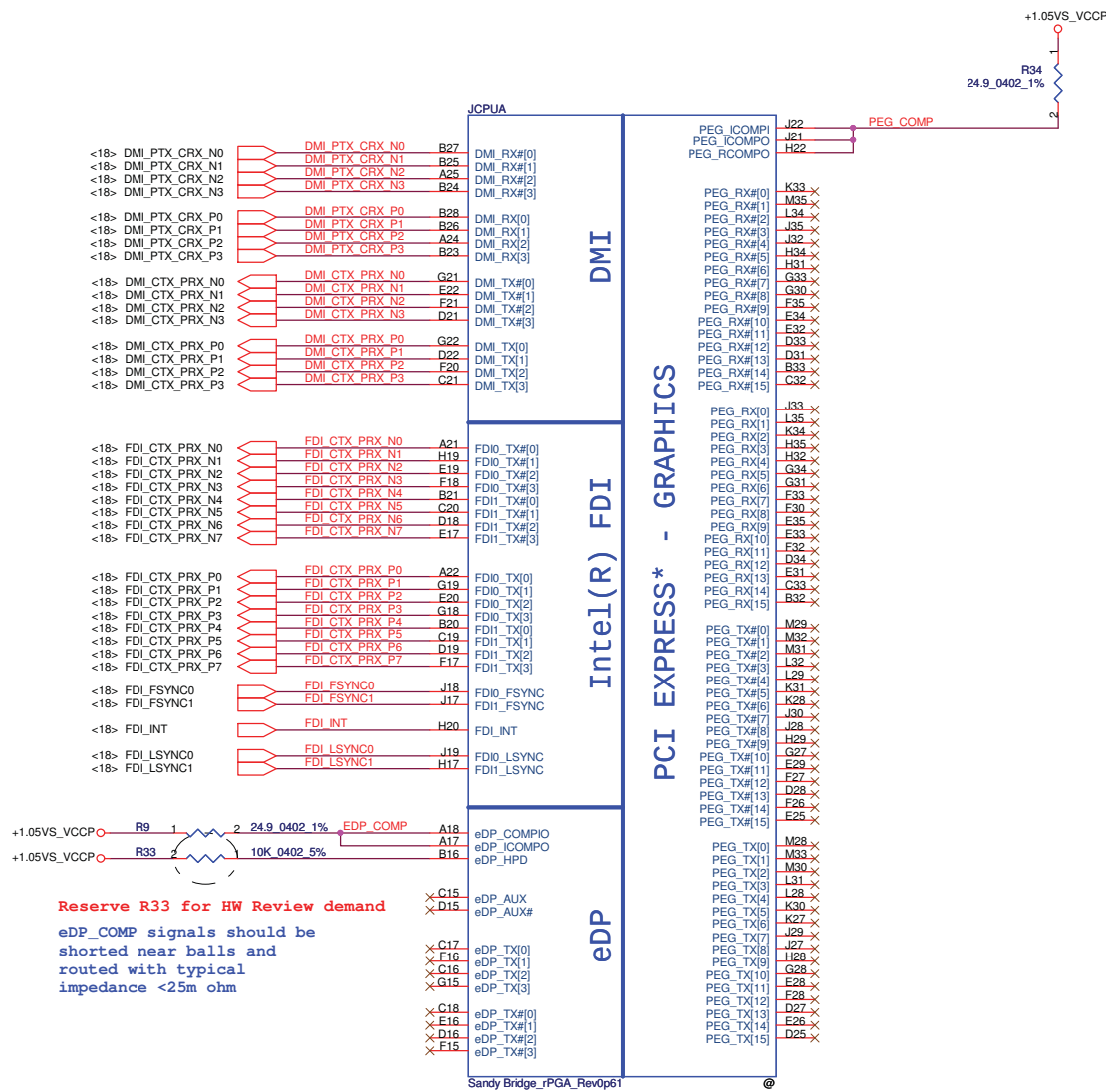
Function	Card reader		New Card
description	JMB385C/389C		New Card
explain	JMB385C	JMB389C	New Card
BTO	JMB385@	JMB389@	NEW@

STATE SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

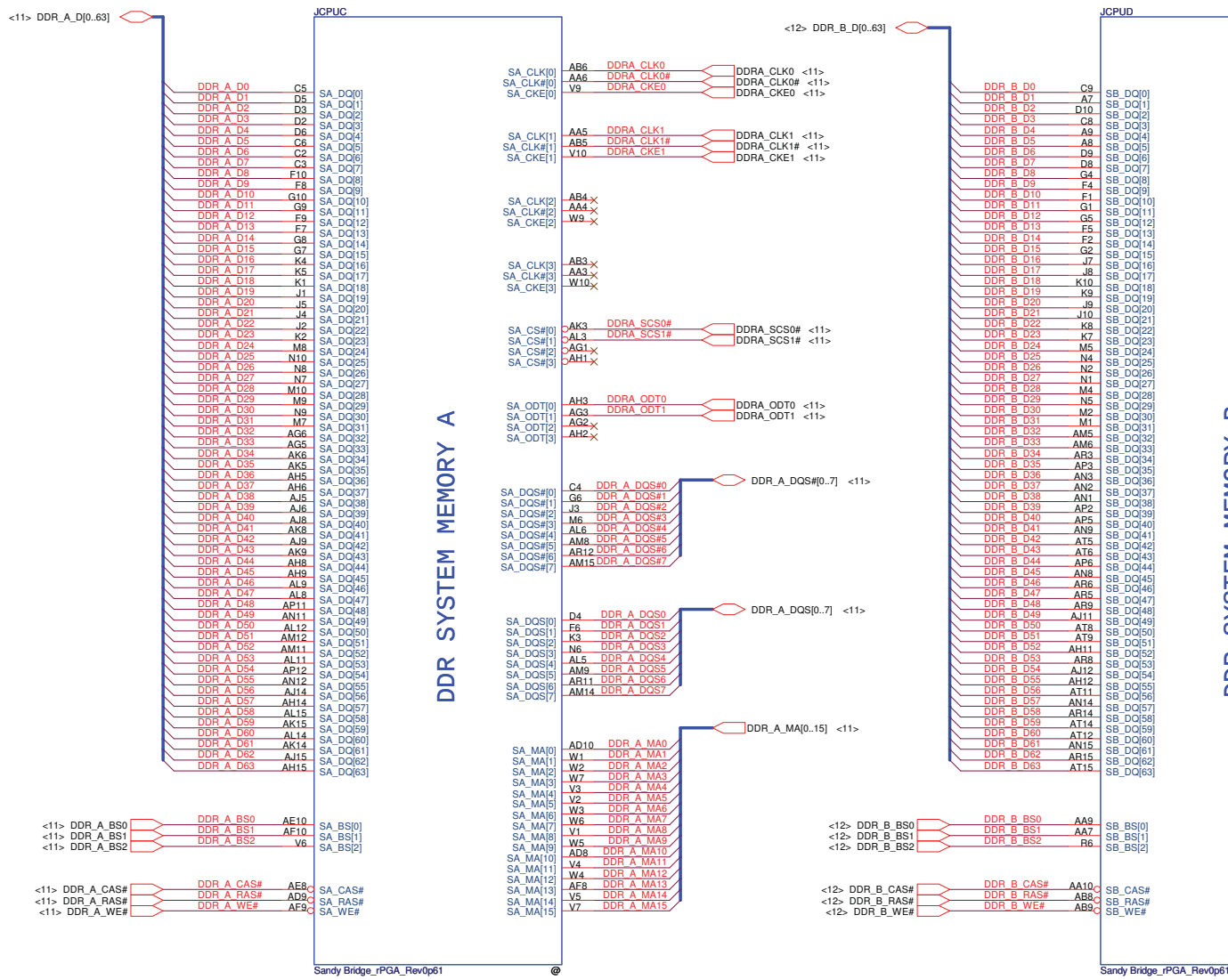
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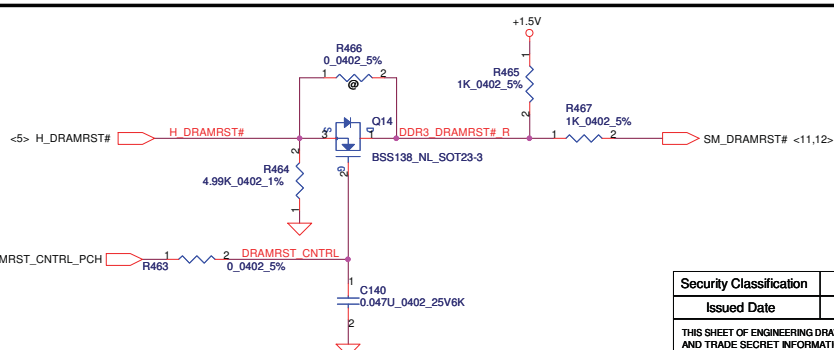
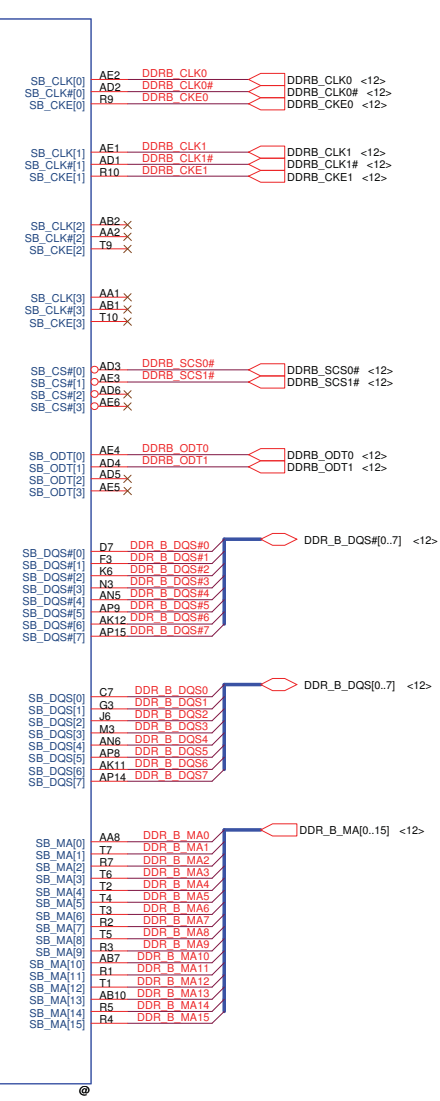
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DDR SYSTEM MEMORY B



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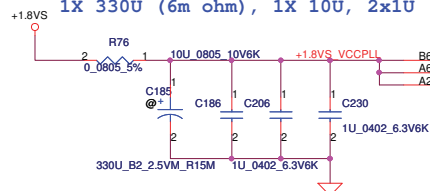
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+GFX_CORE

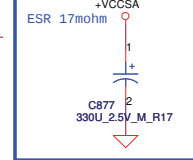
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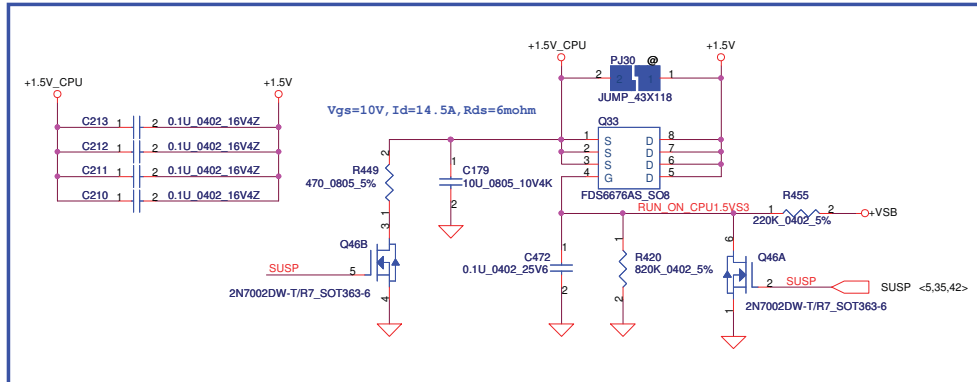
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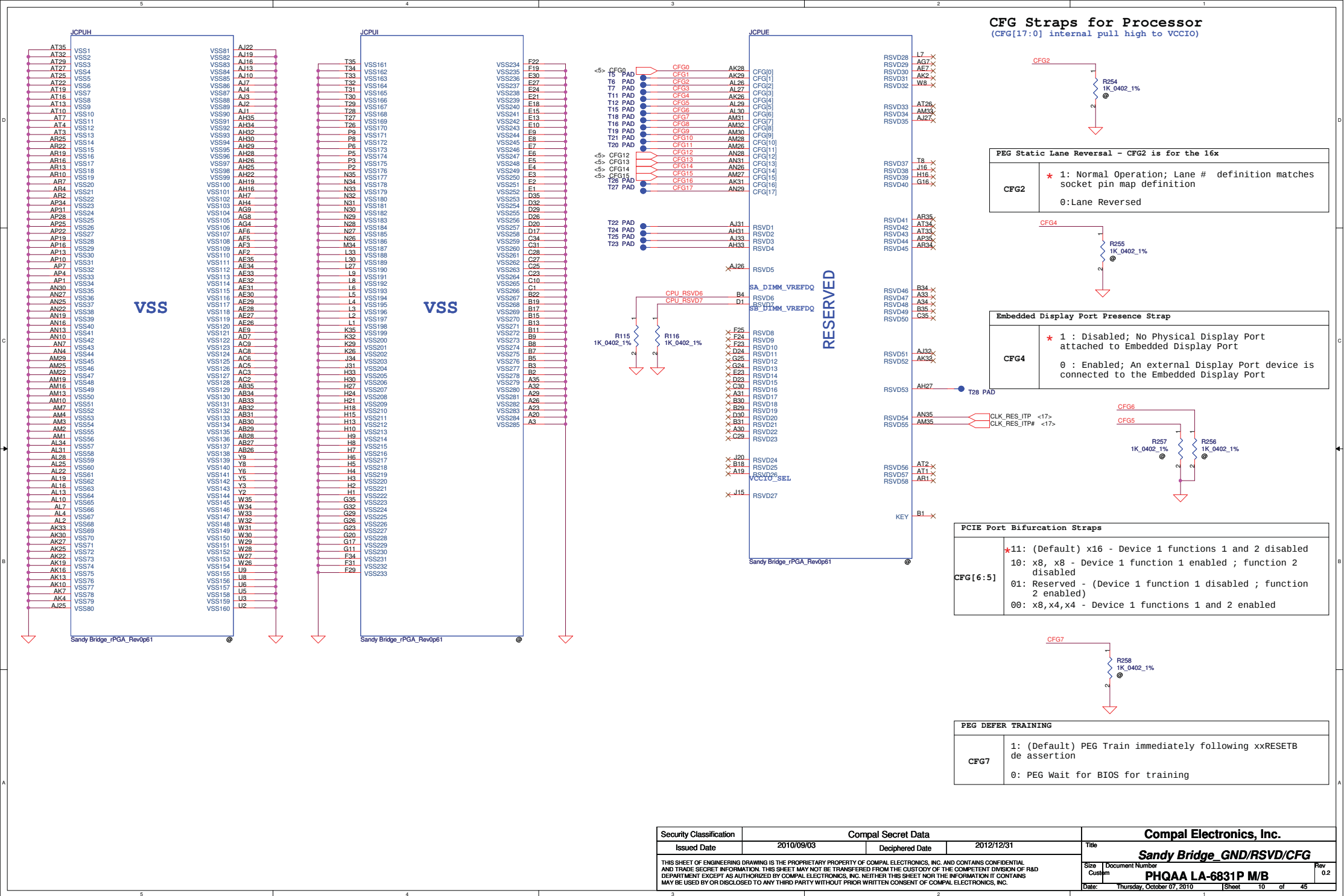
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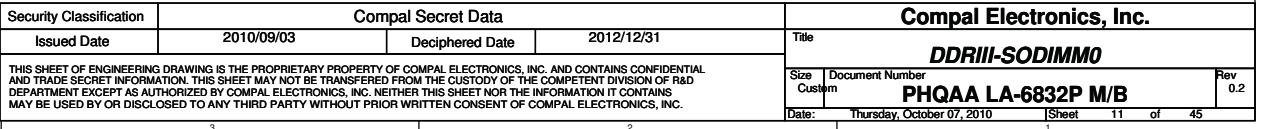
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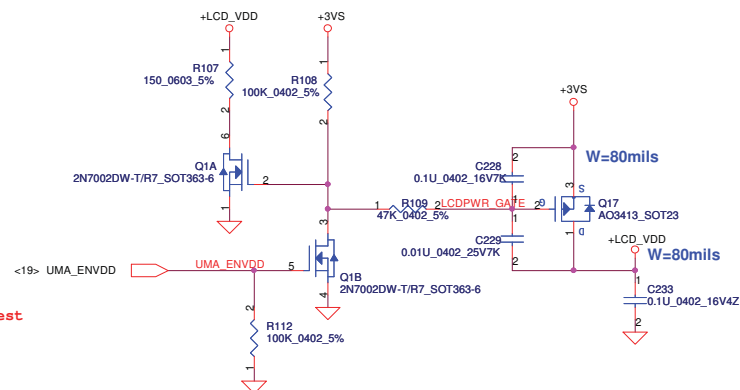
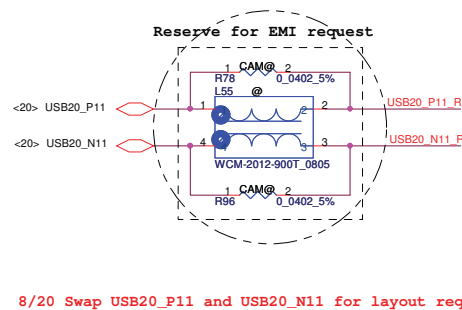


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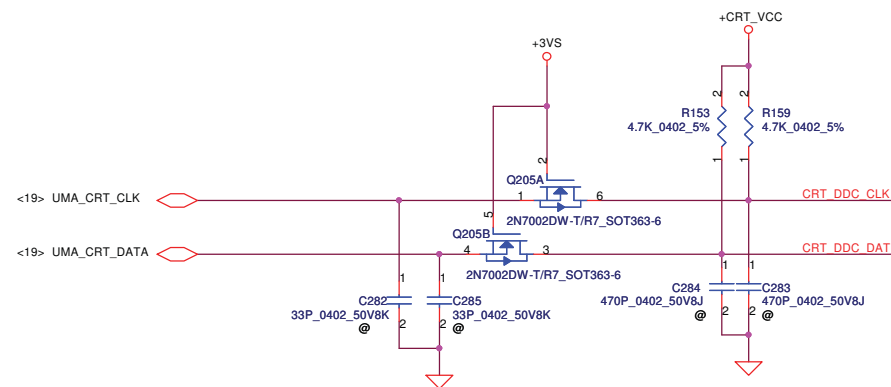
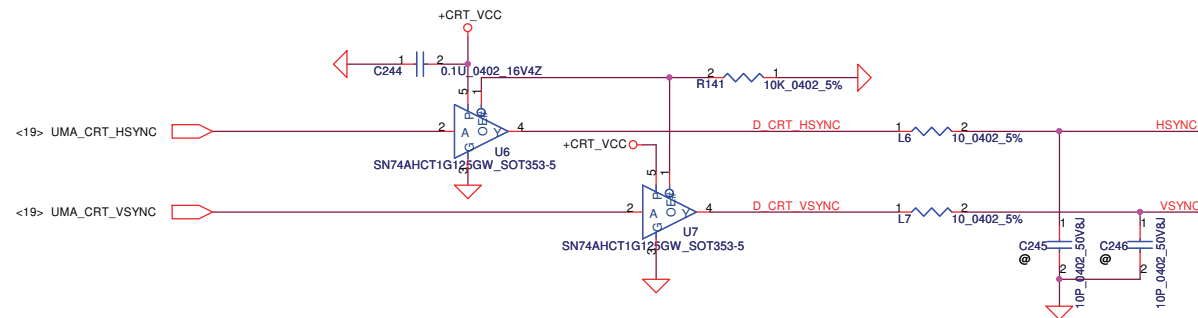
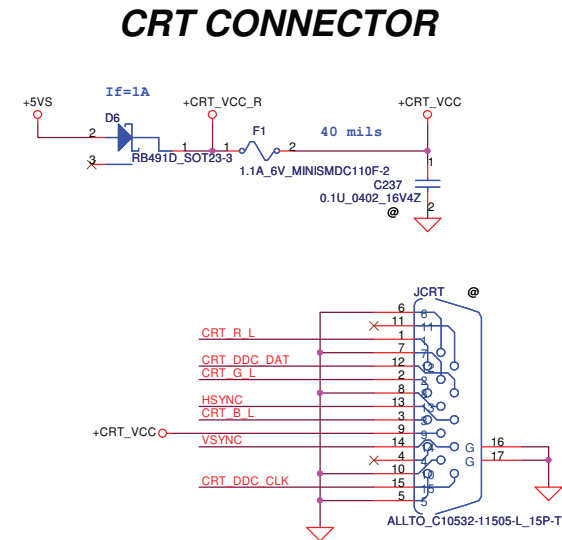
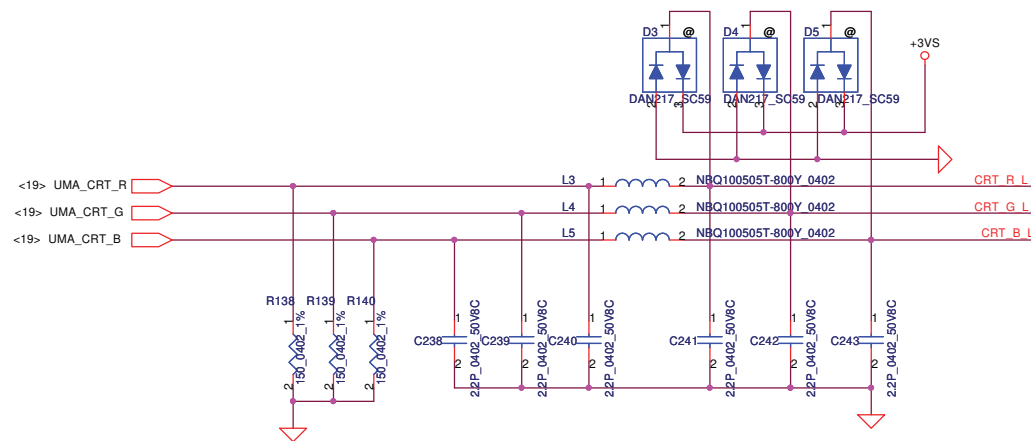


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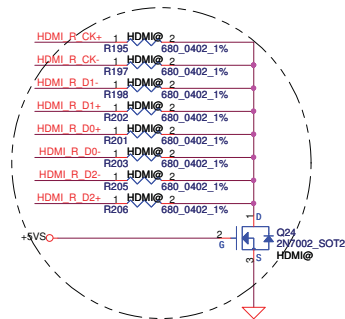
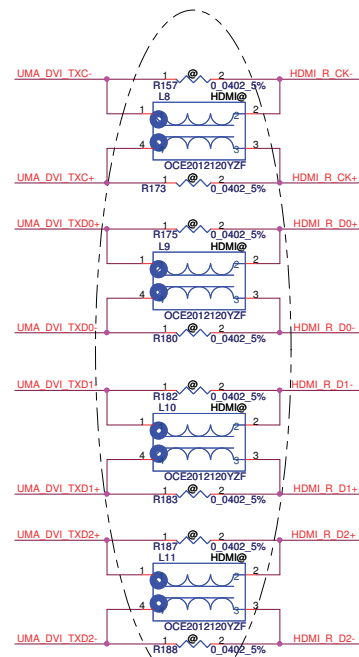
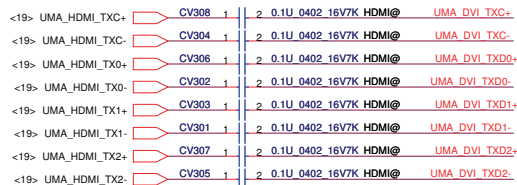
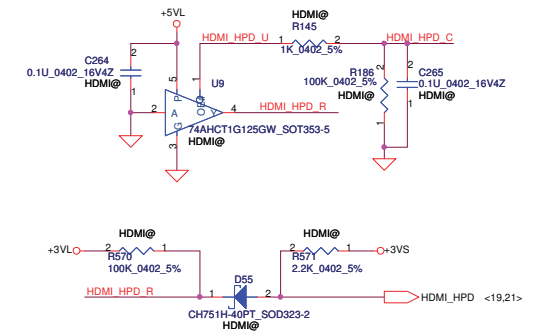
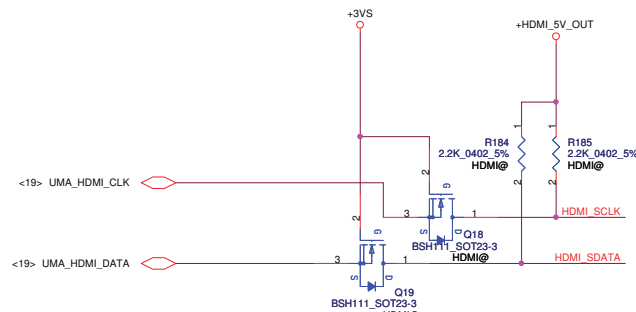
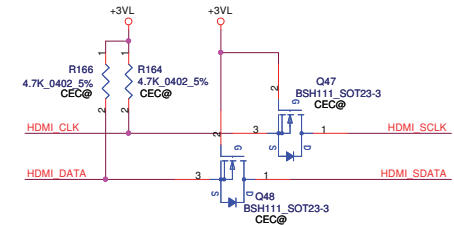
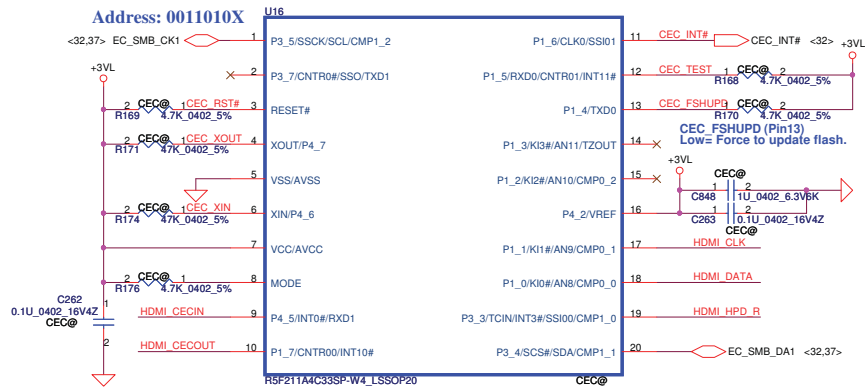
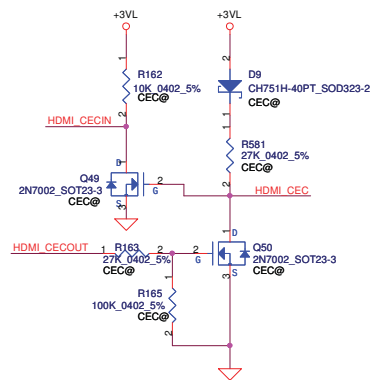
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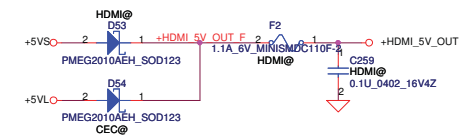


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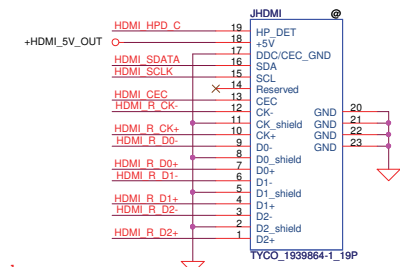
HDMI CEC Controller



08/18 Change R195, R197, R198, R202,
R201, R203, R205, R206 to SD028680080 for UMA request.

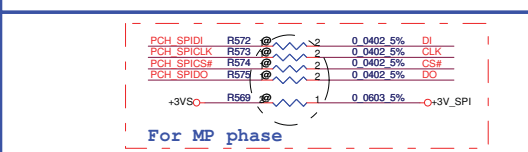
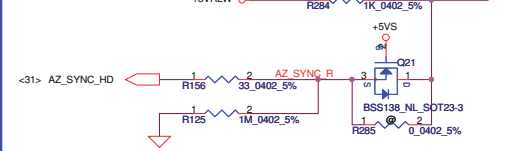
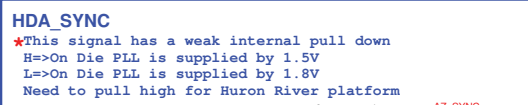
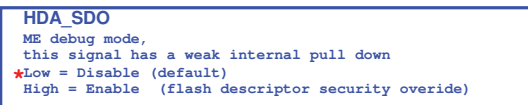
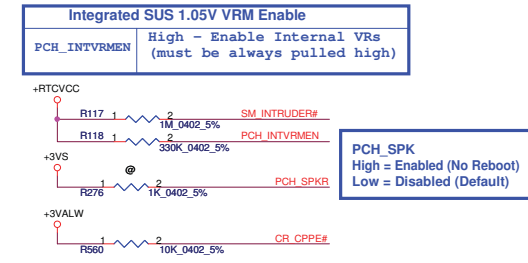
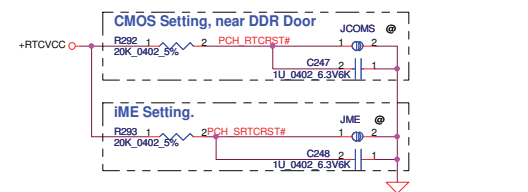


HDMI Connector

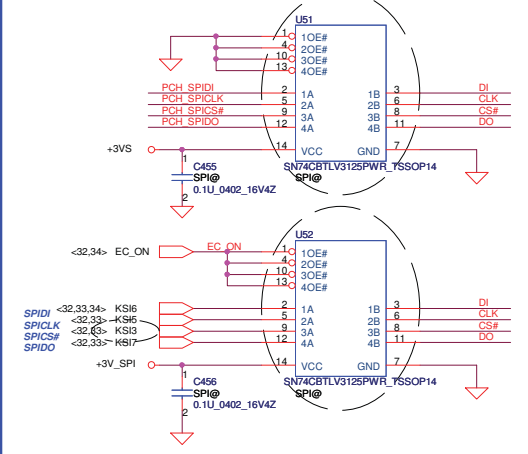


08/13 Change L8, L9 L10, L11 from SM070001600 to SM070001310 by EMI demand

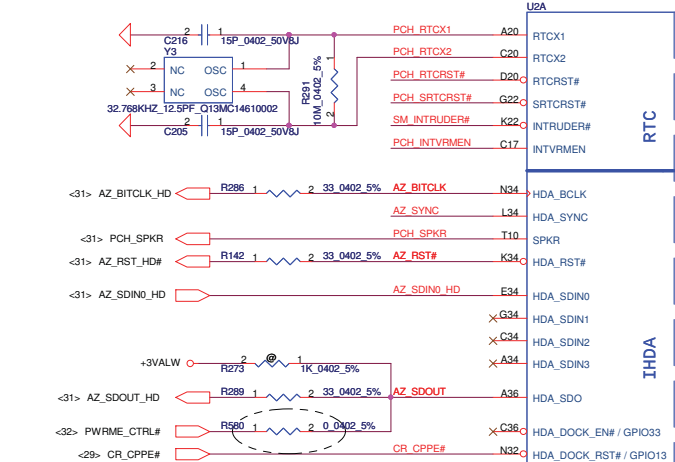
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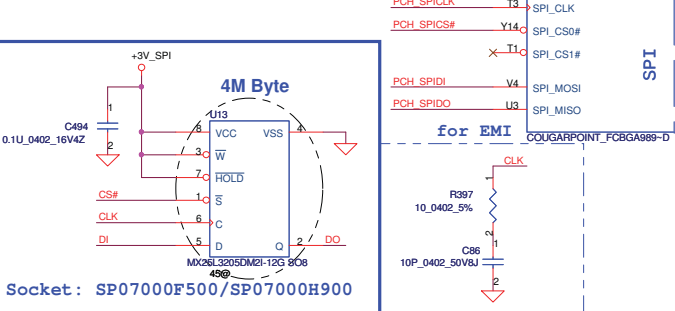
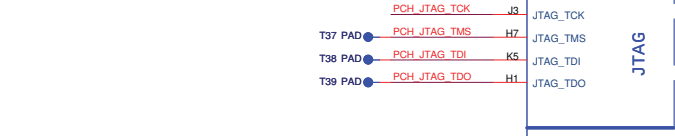
8/ 12 Change R572, R573, R574, R575, R569 from @ to mount



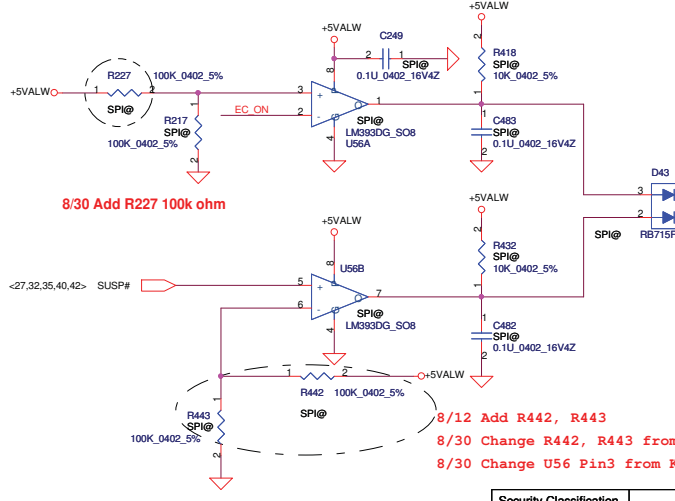
8/12 Change U51, U53 P/N form SA00000BJ20 to SA00000CA00
8/30 Change U53 PIN 9 from KS14 to KS13



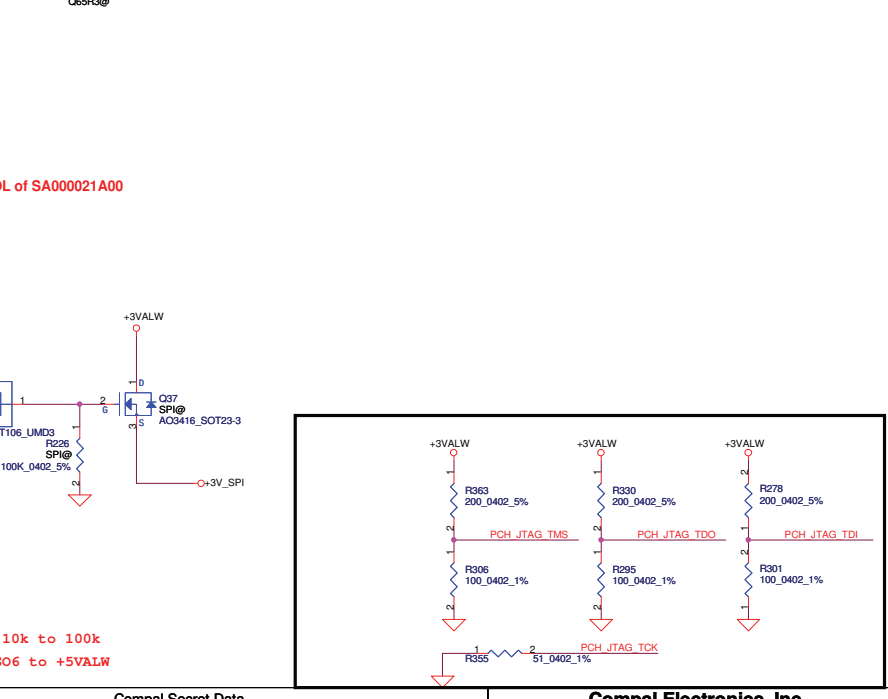
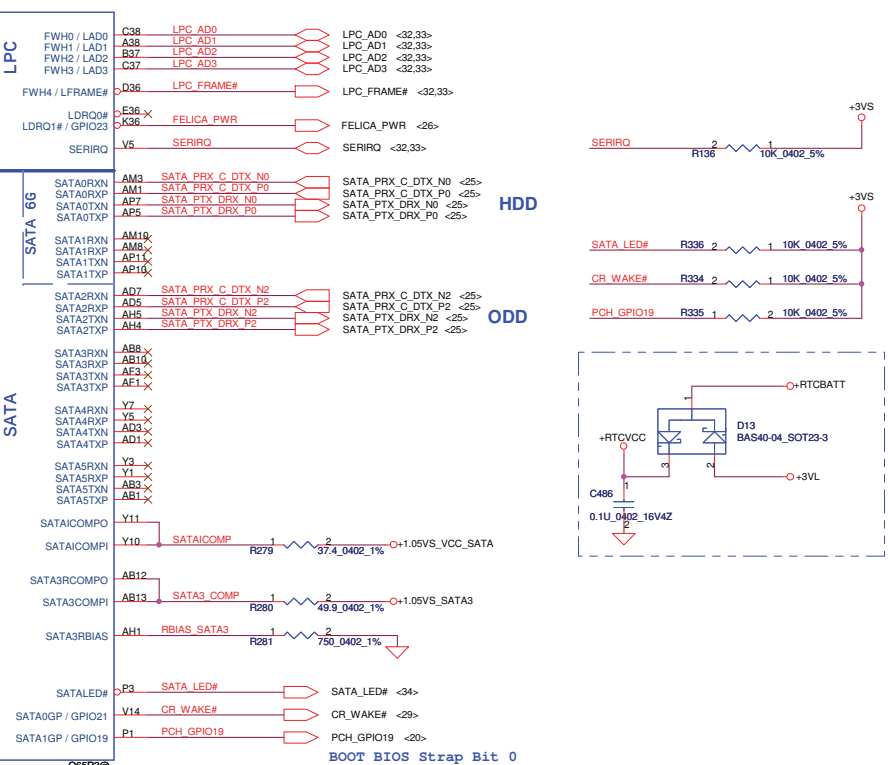
8/30 Change PWRME_CTRL# to HDA_SDO by PCH EDS



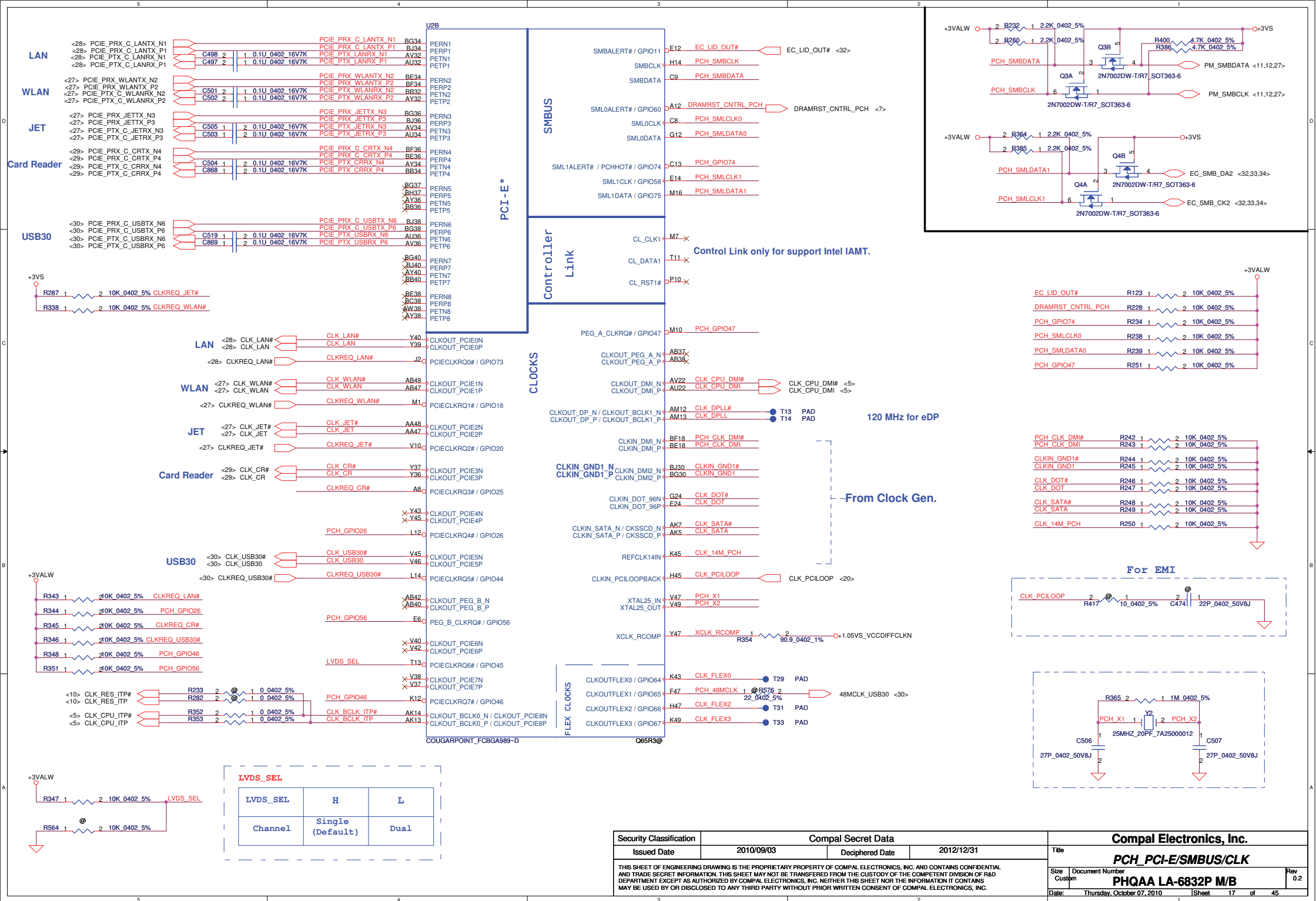
Please close to U2 PCH 8/30 Change U13 from SA000021A00 to SA000031N00 due to EOL of SA000021A00

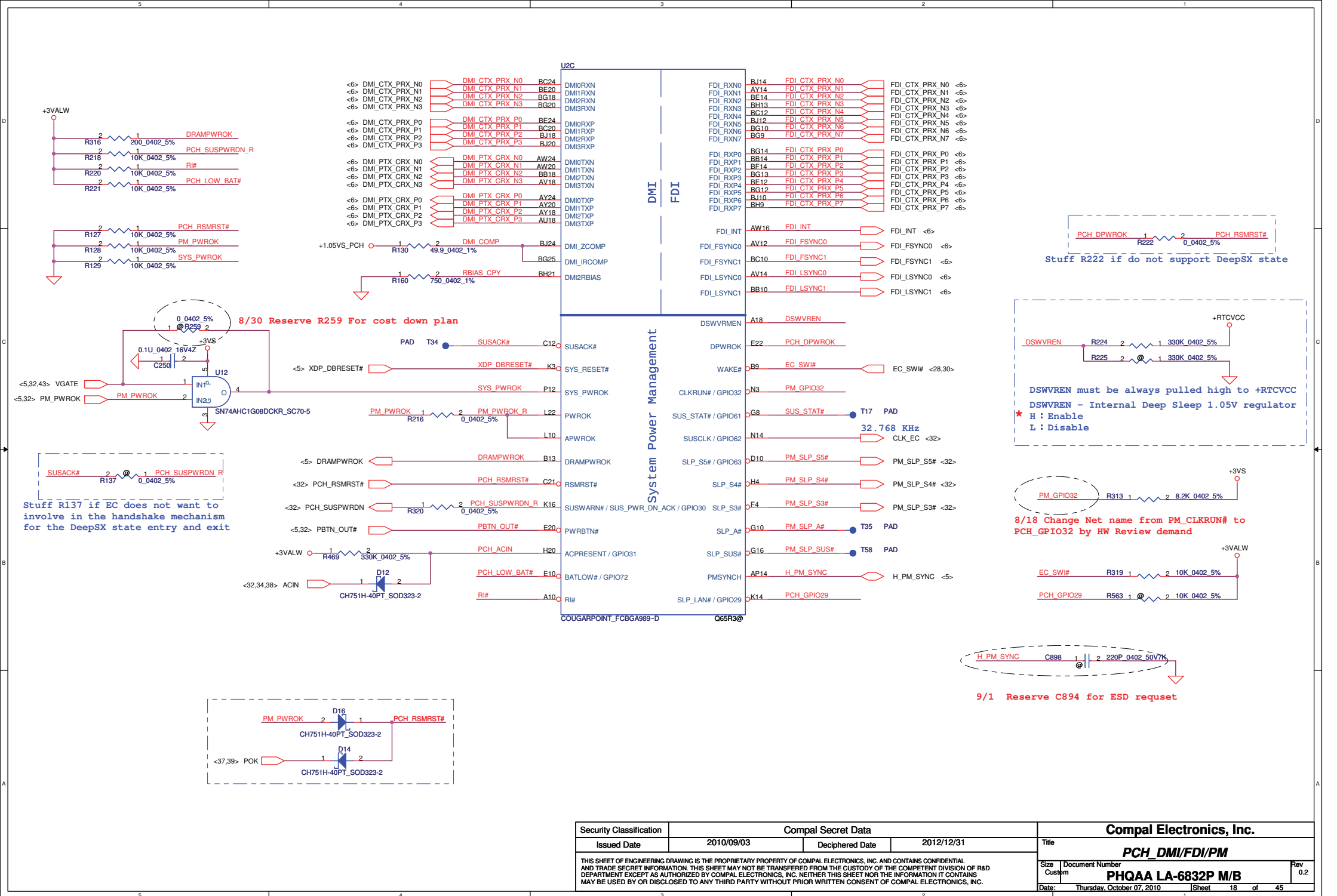


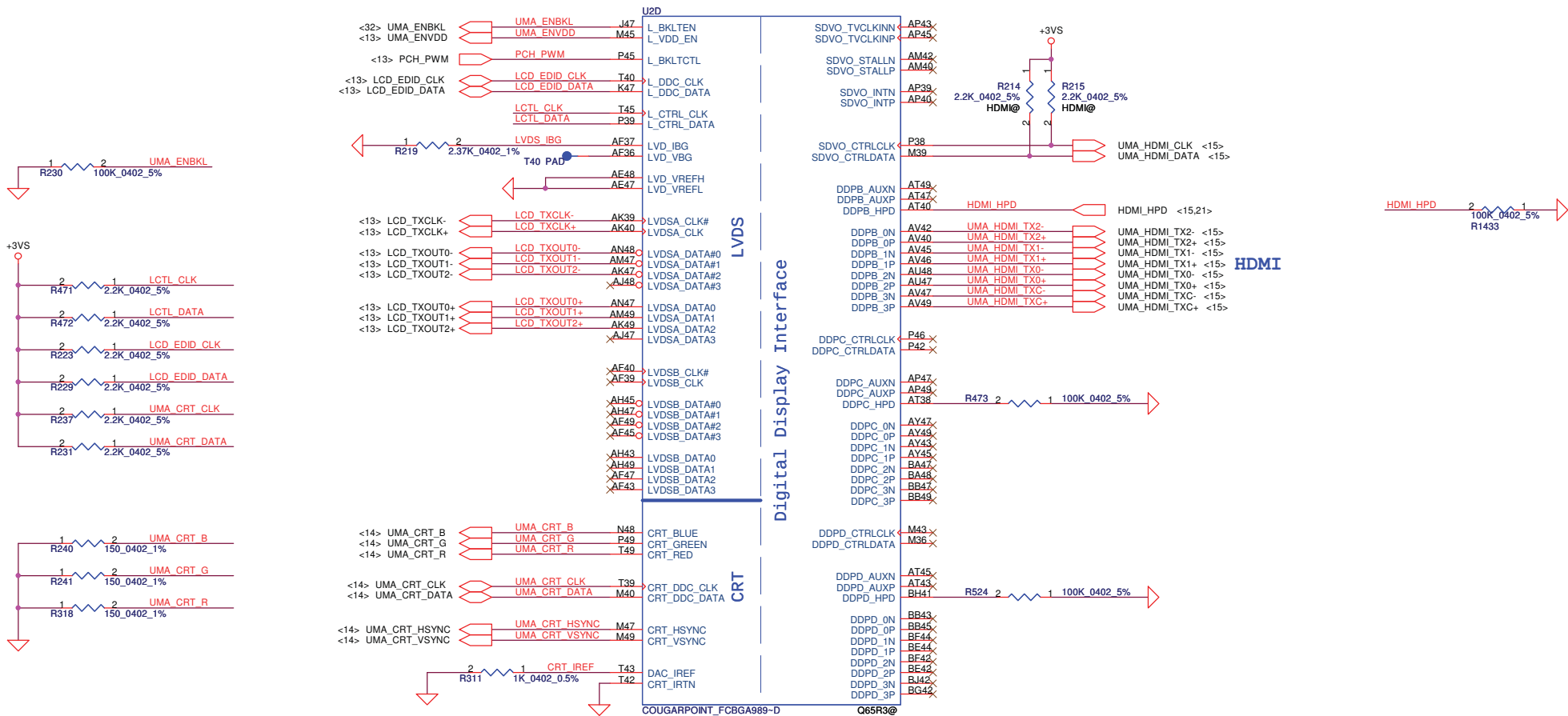
Please close to U2 PCH, and between U2 & U13



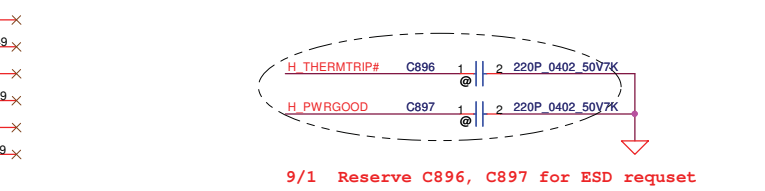
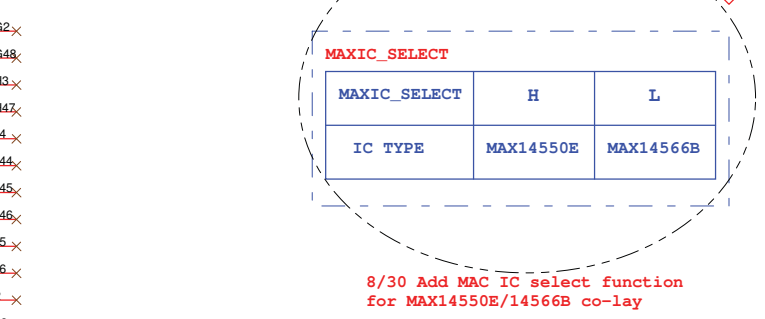
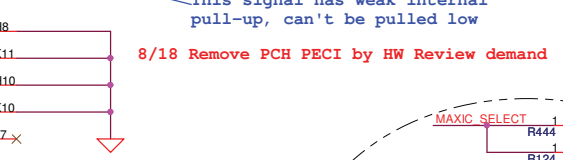
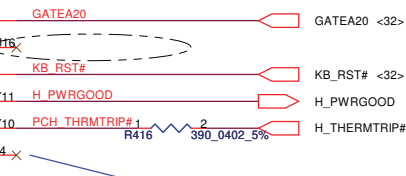
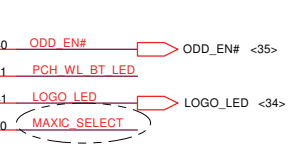
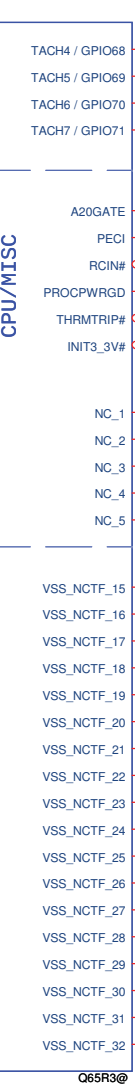
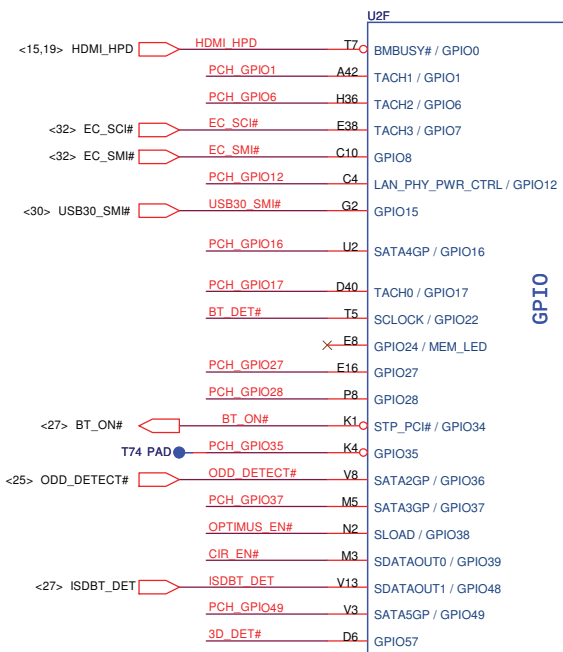
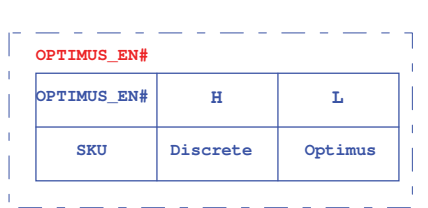
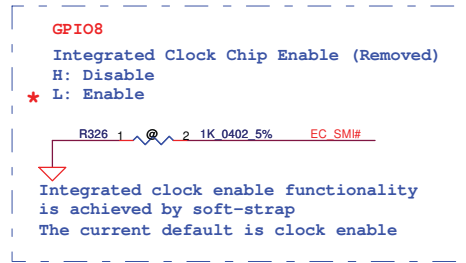
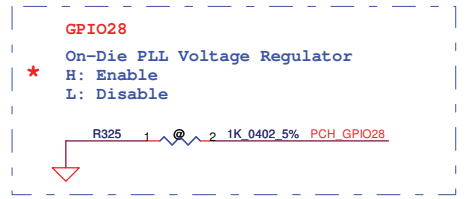
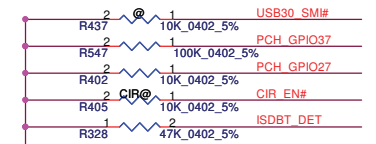
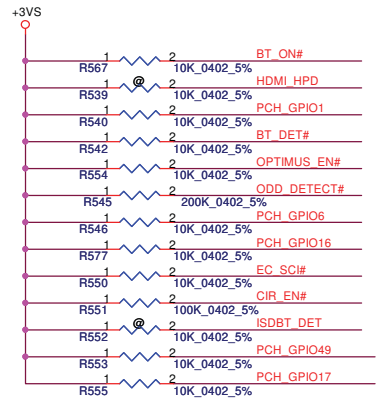
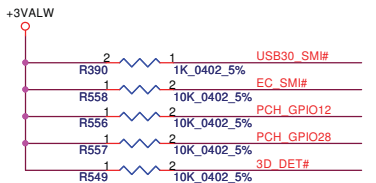
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				Sheet	16 of 45

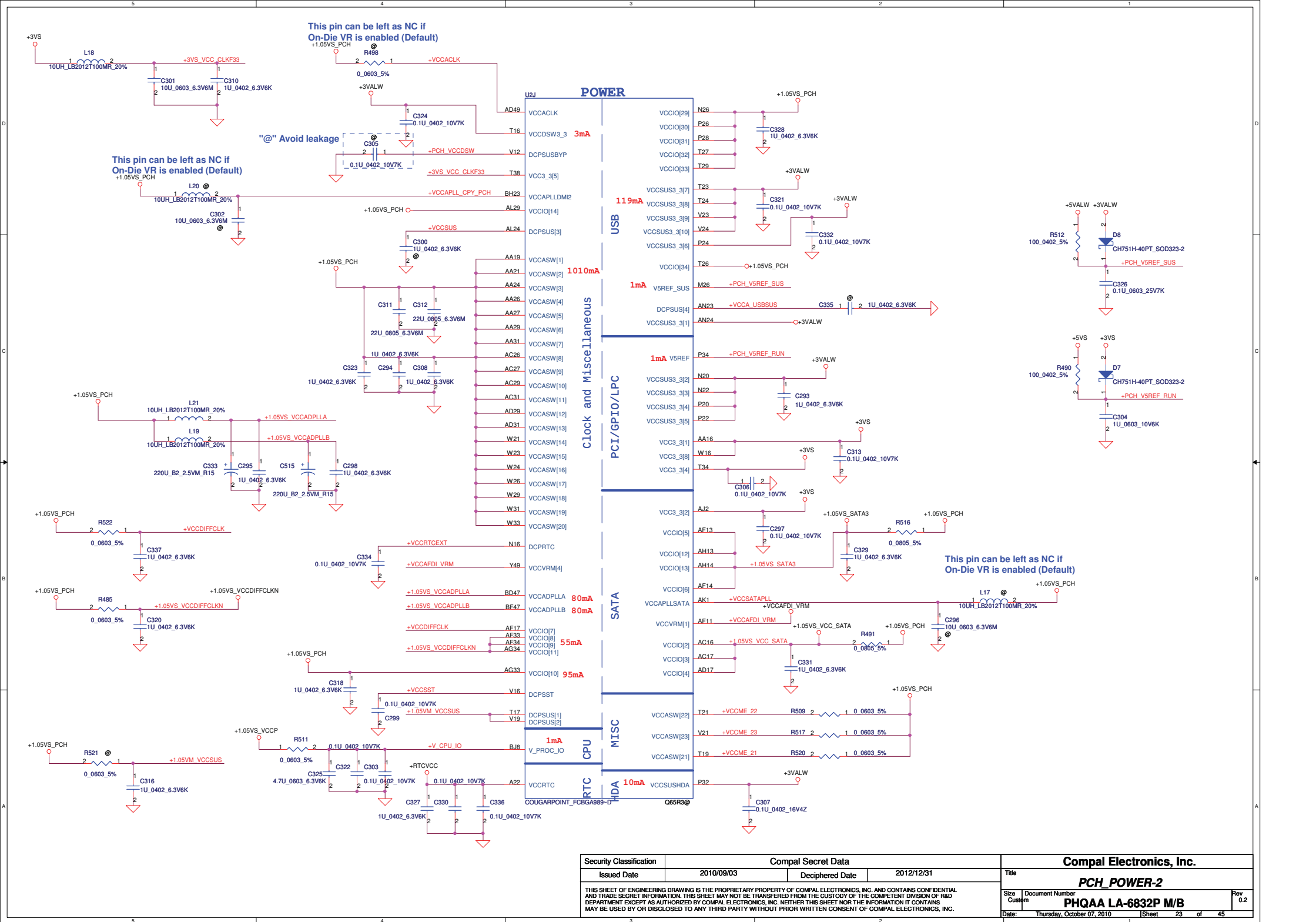


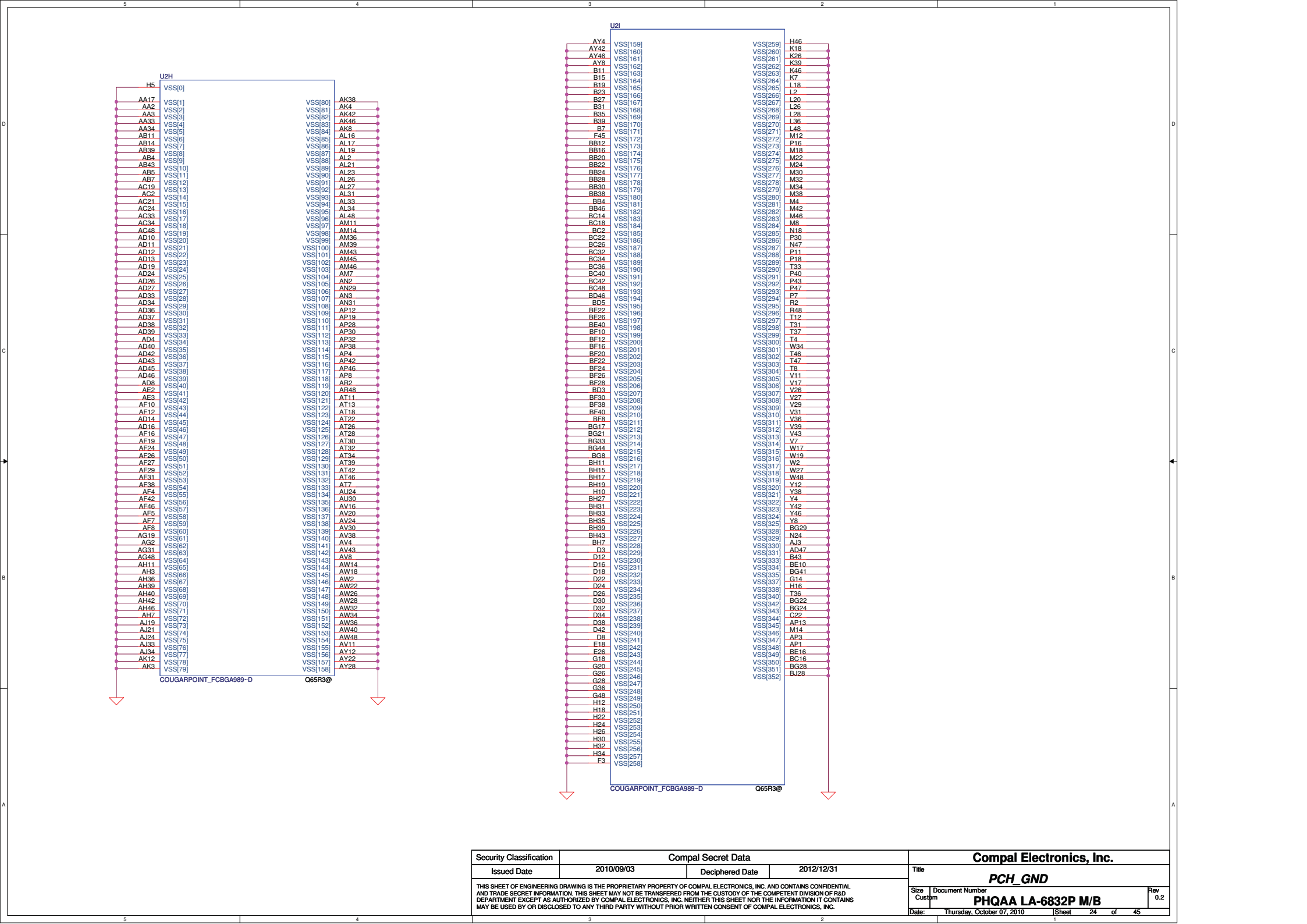




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				Sheet	19 of 45
				Rev	0.2

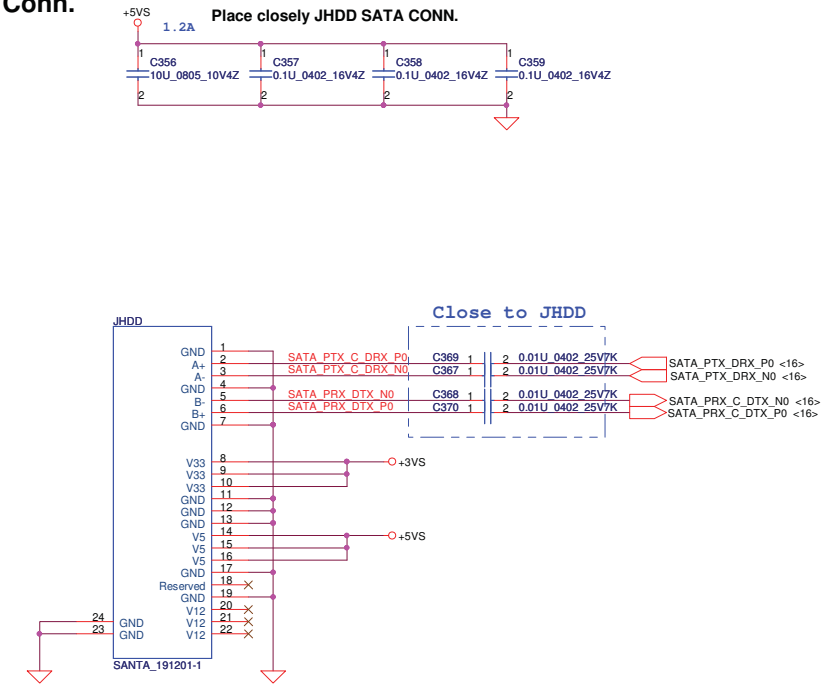




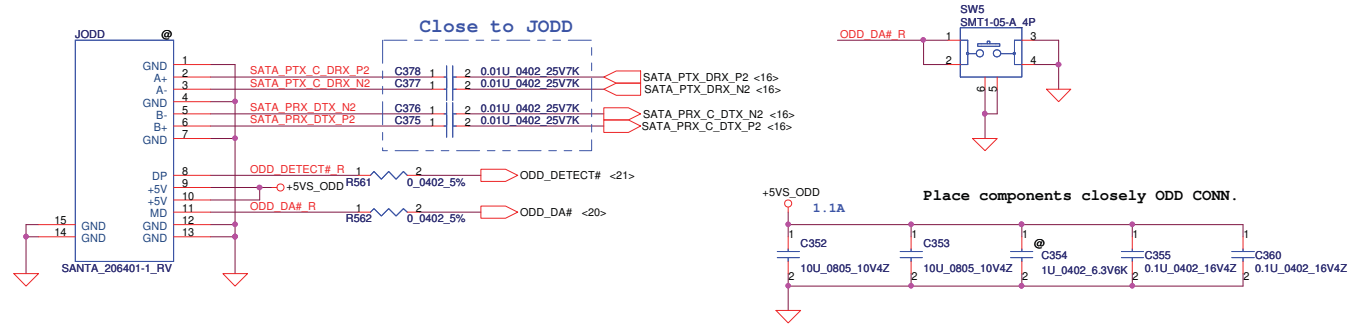


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Size		Document Number		Rev	
Custom		PHQAA LA-6832P M/B		0.2	
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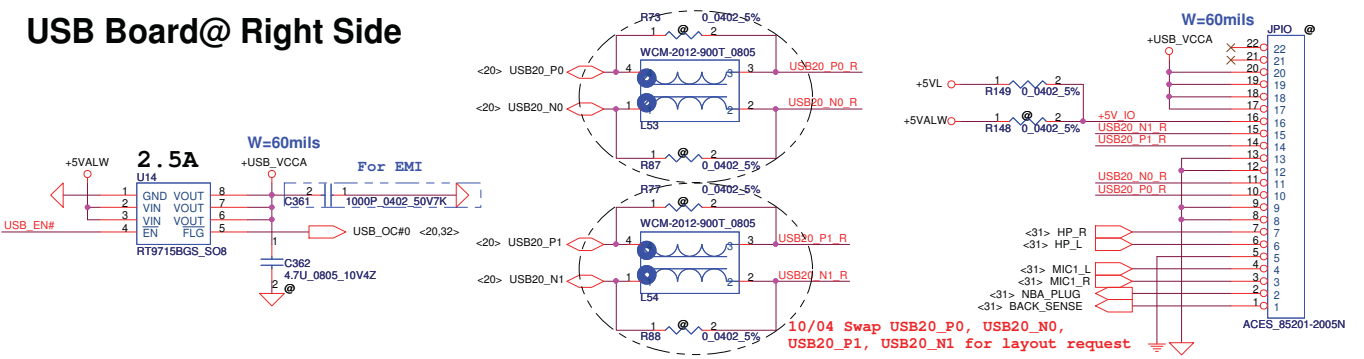
SATA HDD Conn.



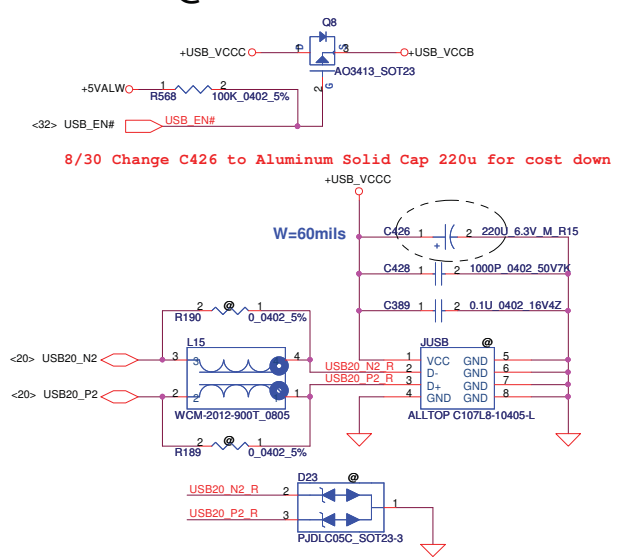
SATA ODD Conn



USB Board@ Right Side

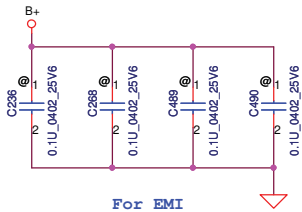


USB Board@ Left Side

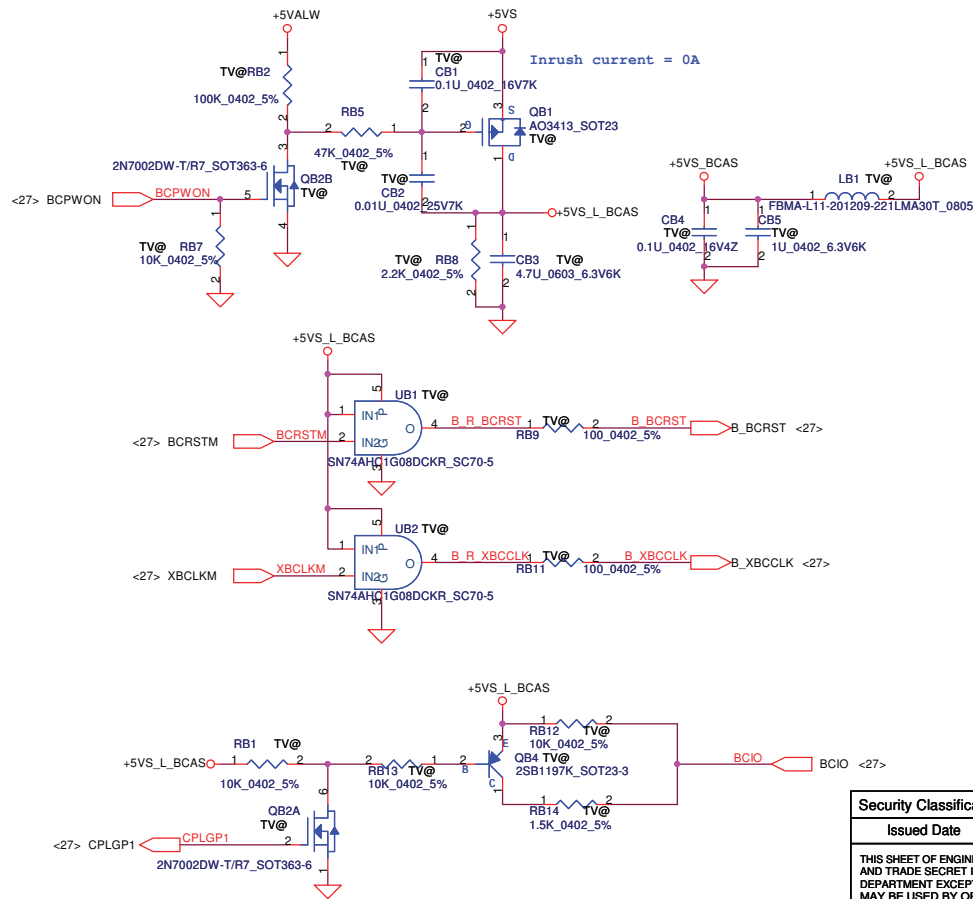


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Screw cap for ESD request

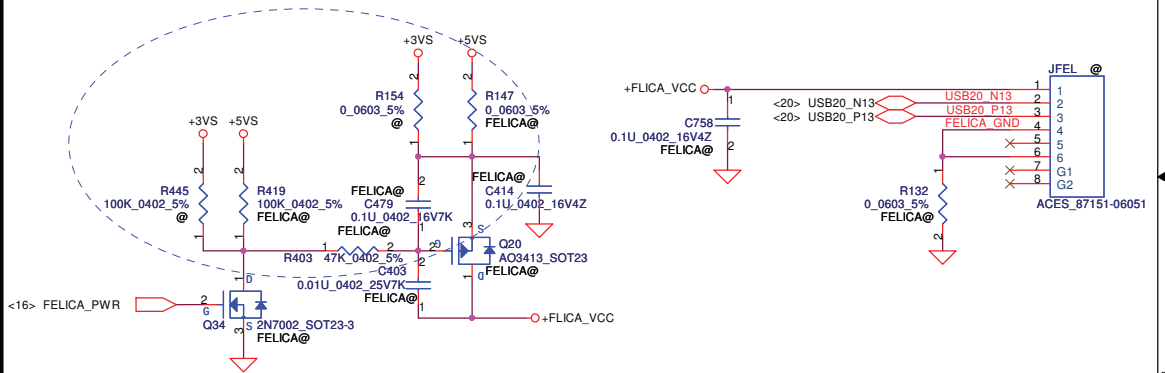


B-CAS Circuit

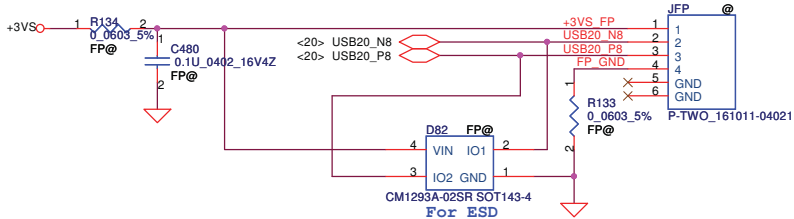


Felica

Reserve +3VS Felica by Customer demand.
2010/09/27

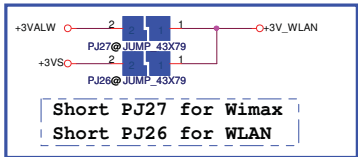


Finger printer



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								Size	Document Number	Rev
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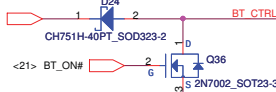
Slot 1 Half PCIe Mini Card-WLAN/ WiMax



WLAN+BT Combo module circuits

	BT on module	BT on module
BT_CTRL	Enable	Disable
BT_ON#	L	H

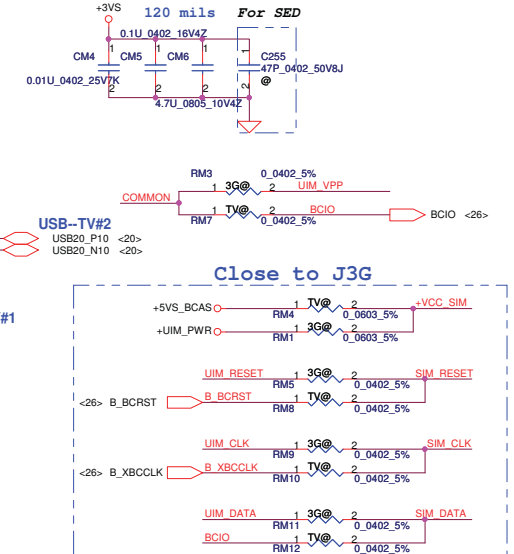
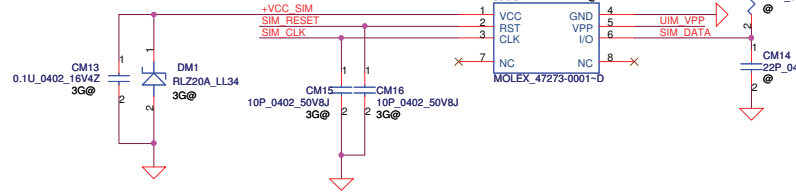
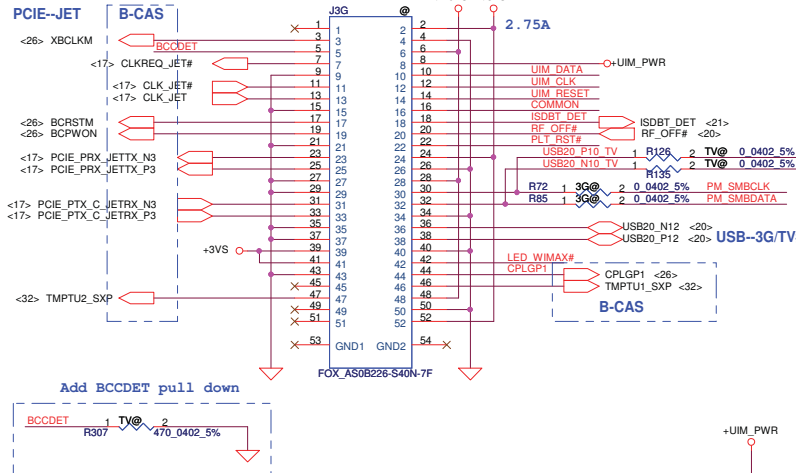
**If +3V_WLAN is +3VS, please remove D24



For isolate Intel Rainbow Peak and Compal Debug Card.

8/30 Reserve R1443 for WLAN Mini PCIe Card Pin5

Slot 2 Full PCIe Mini Card- 3G/ TV Tuner Half PCIe Mini Card- JET

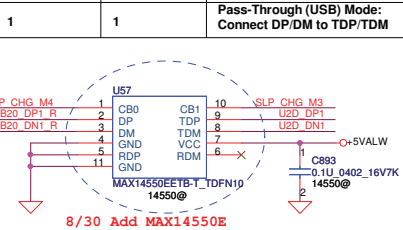
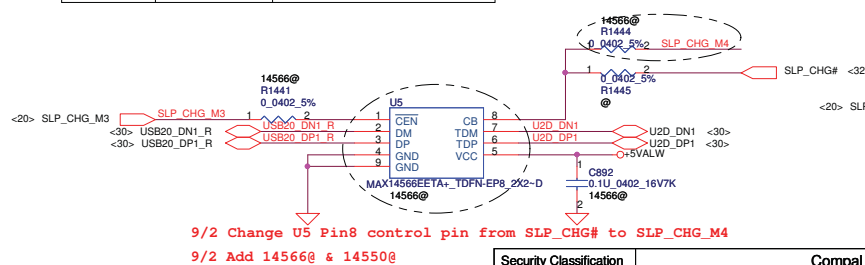
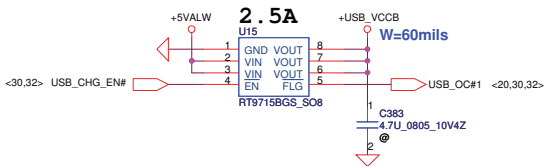


USB Sleep & Charge Auto-Mode Mode3/Mode4

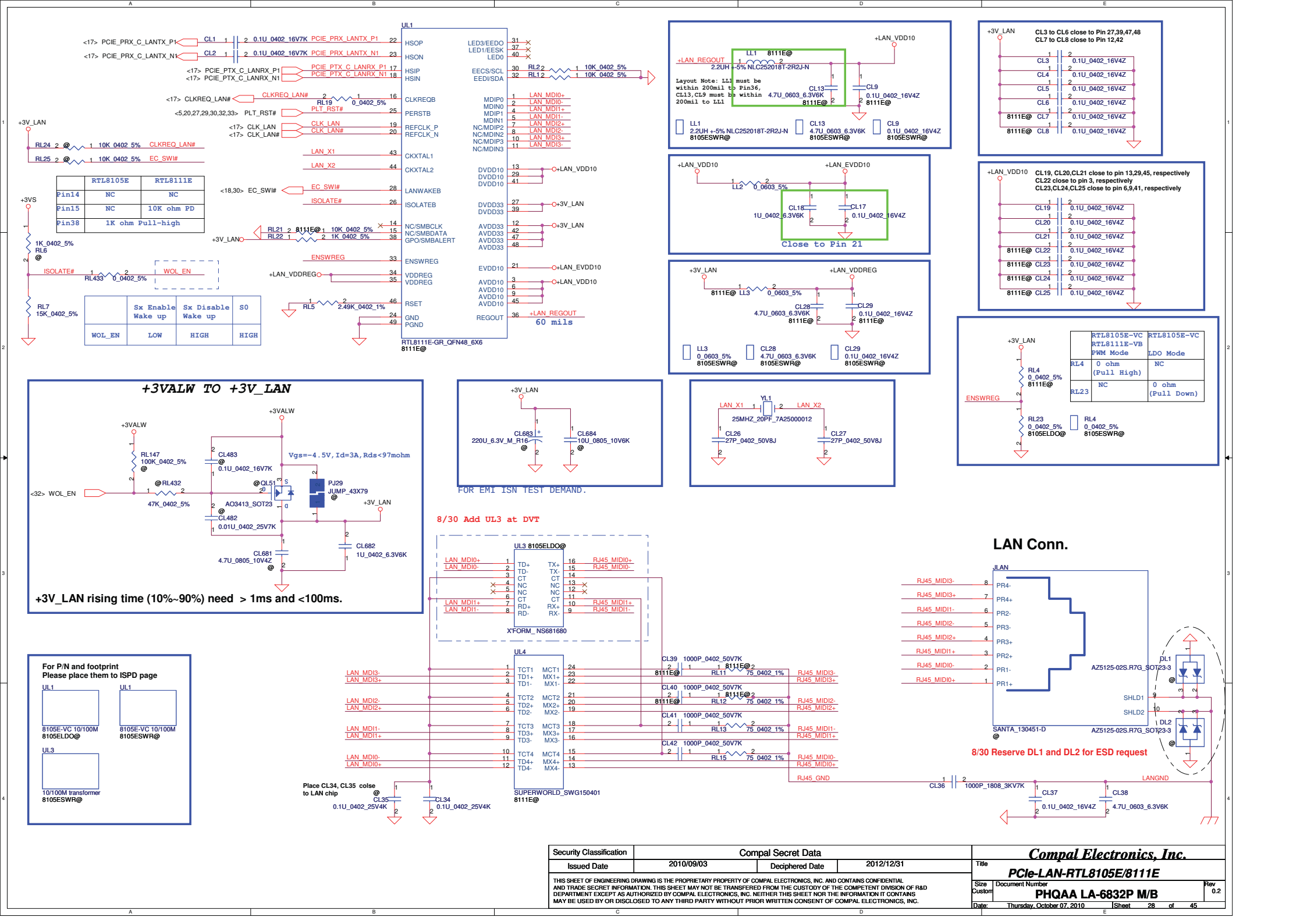
MAX14566B		
CB0 SLP_CHG#	CB1 (CEN#) SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

MAX14566E	
CB: SLP_CHG#	STATUS
0	AUTO MODE
1	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

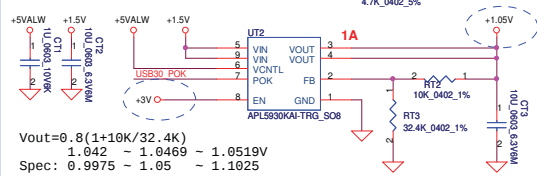
MAX14550E		
CB0 SLP_CHG_M4	CB1 SLP_CHG_M4	STATUS
0	0	AUTO MODE
0	1	MODE3
1	0	MODE4
1	1	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM



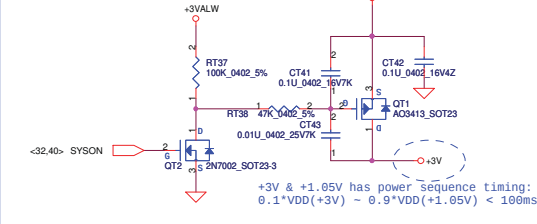
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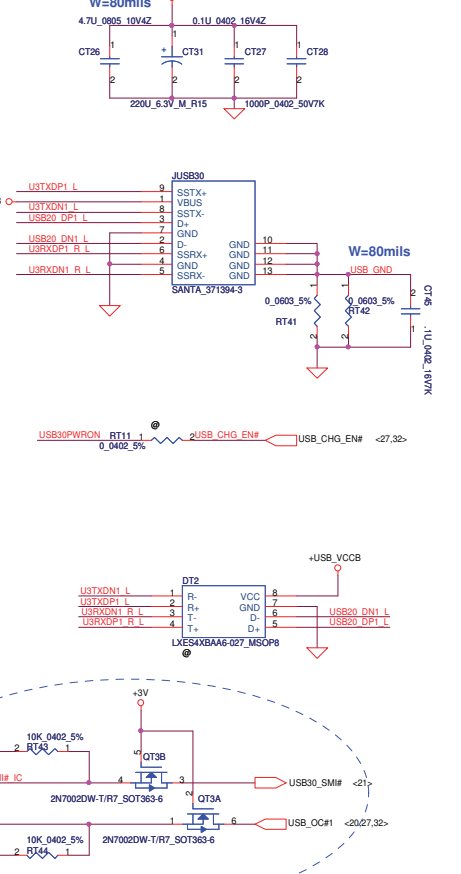
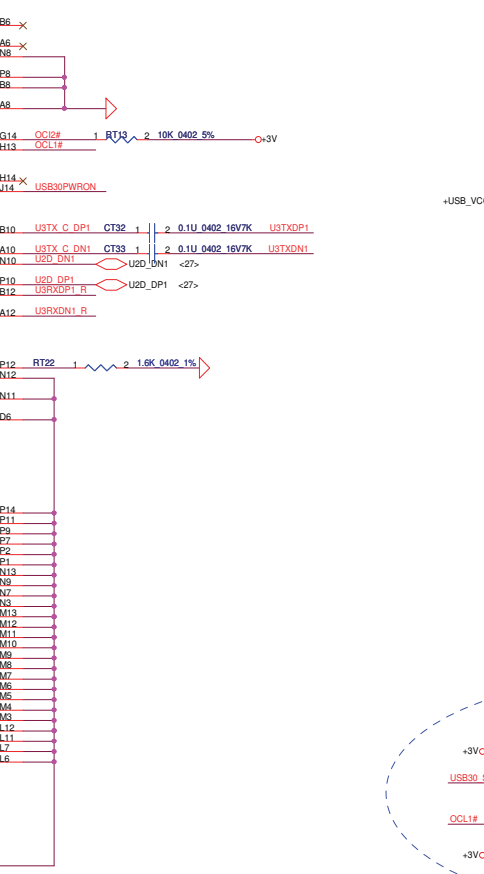
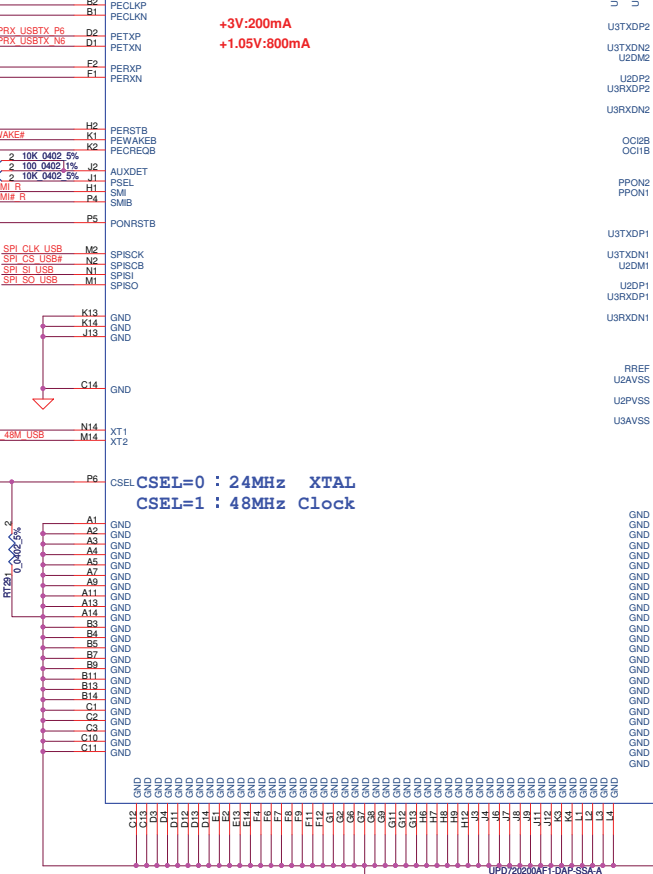
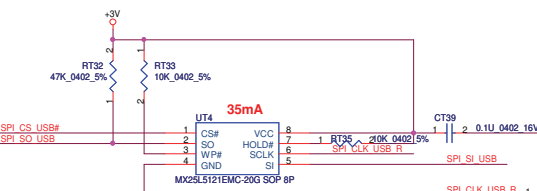
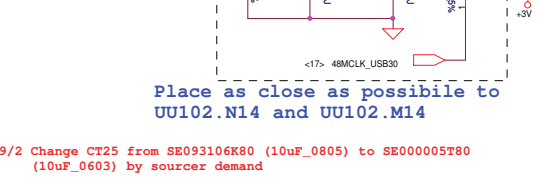
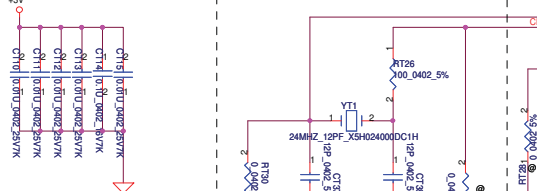
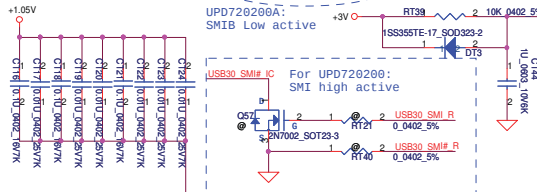
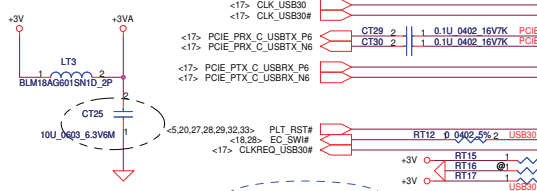
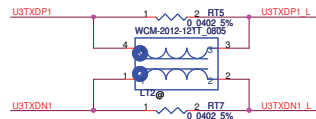
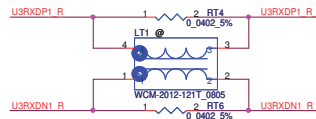
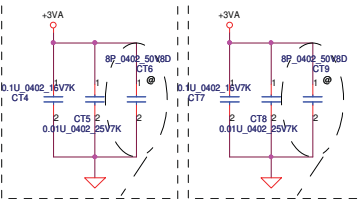
+1.5V to +1.05V Transfer



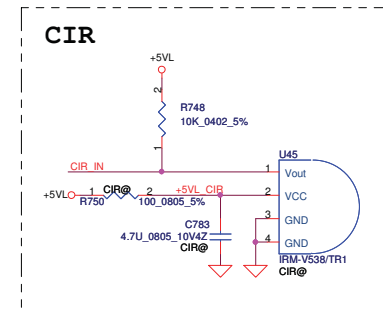
+3VALW to +3V Transfer



Close to U102.D7



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					PHQAA LA-6832P M/B			0.2	
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9/03 Change U22 change to SA00003FL10

The diagram shows the H7 microcontroller with the following connections:

- Pin 6:** Connected to +3V3.
- Pin 7:** Connected to SERIRQ through a 22k resistor (R392).
- Pin 8:** Connected to LPC_AD3.
- Pin 9:** Connected to LPC_AD1.
- Pin 10:** Connected to LPC_FRAME#.
- Pin 5:** Connected to PLT_RST#.
- Pin 4:** Connected to LPC_AD2.
- Pin 3:** Connected to LPC_AD0.
- Pin 2:** Connected to LPC_AD0.
- Pin 1:** Connected to CLK_PCI_DDR.
- Pin 0:** Labeled as DEBUG_PAD.

A dashed box labeled "For EMI" contains a 22pF capacitor (C457) connected to the CLK_PCI_DDR signal line (Pin 1) and ground.

Keyboard LED

Keyboard LED

The schematic diagram shows the internal circuitry of a keyboard LED. It features a +5V input connected to a 10K resistor (R587). The other end of the resistor is connected to the emitter of a PNP transistor (Q38, AO3413_SOT23-3). The base of Q38 is connected to a +5V input through a 47K resistor. The collector of Q38 is connected to a +5V input through a 10K resistor. The emitter of Q38 is connected to the base of an NPN transistor (Q52, 2N7002_SOT23-3). The collector of Q52 is connected to a +5V input through a 10K resistor. The emitter of Q52 is connected to ground. The output of the circuit is connected to a JBLG connector.

JBLG Pin Connections:

Pin	Signal
1	+5V_LED
2	X
3	X
4	X
5	X
6	X
GND	X

ACES_85201-0405N

For EMI

Close to JKB

Signal	Pin	Value
KSO16	C401	100P_0402_50V8J
KSO17	C402	100P_0402_50V8J
KSO2	C404	100P_0402_50V8J
KSO1	C405	100P_0402_50V8J

Pinout diagram for the ACES_88170-3400 connector. The diagram shows two rows of pins, 1 through 34, with their corresponding signal names and electrical characteristics.

Top Row (Pins 1-17):

- Pin 1: KSJ[0..7] <16,32,34>
- Pin 2: KSO[0..17] <32,34>
- Pin 3: KSO16
- Pin 4: KSO17
- Pin 5: KSO2
- Pin 6: KSO1
- Pin 7: KSO0
- Pin 8: KSO4
- Pin 9: KSO3
- Pin 10: KSO5
- Pin 11: KSO14
- Pin 12: KSO6
- Pin 13: KSO7
- Pin 14: KSO13
- Pin 15: KSO8
- Pin 16: KSO9
- Pin 17: KSO10

Bottom Row (Pins 18-34):

- Pin 18: KSO11
- Pin 19: KSO12
- Pin 20: KSO15
- Pin 21: KSI7
- Pin 22: KSI2
- Pin 23: KSI3
- Pin 24: KSI4
- Pin 25: KSI0
- Pin 26: KSI5
- Pin 27: KSI6
- Pin 28: KSI1
- Pin 29: CAPS_LED#
- Pin 30: NUM_LED#
- Pin 31: KSO16
- Pin 32: KSO17
- Pin 33: KSO2
- Pin 34: KSO1

Electrical Characteristics:

- 3V5: Connected to pins 1 and 18.
- Ground: Connected to pins 2 and 19.
- KSJ[0..7]: <16,32,34>
- KSO[0..17]: <32,34>
- KSO16: <32,34>
- KSO17: <32,34>
- KSO2: <32,34>
- KSO1: <32,34>
- KSO0: <32,34>
- KSO4: <32,34>
- KSO3: <32,34>
- KSO5: <32,34>
- KSO14: <32,34>
- KSO6: <32,34>
- KSO7: <32,34>
- KSO13: <32,34>
- KSO8: <32,34>
- KSO9: <32,34>
- KSO10: <32,34>
- KSO11: <32,34>
- KSO12: <32,34>
- KSO15: <32,34>
- KSI7: <32,34>
- KSI2: <32,34>
- KSI3: <32,34>
- KSI4: <32,34>
- KSI0: <32,34>
- KSI5: <32,34>
- KSI6: <32,34>
- KSI1: <32,34>
- CAPS_LED#: <32,34>
- NUM_LED#: <32,34>

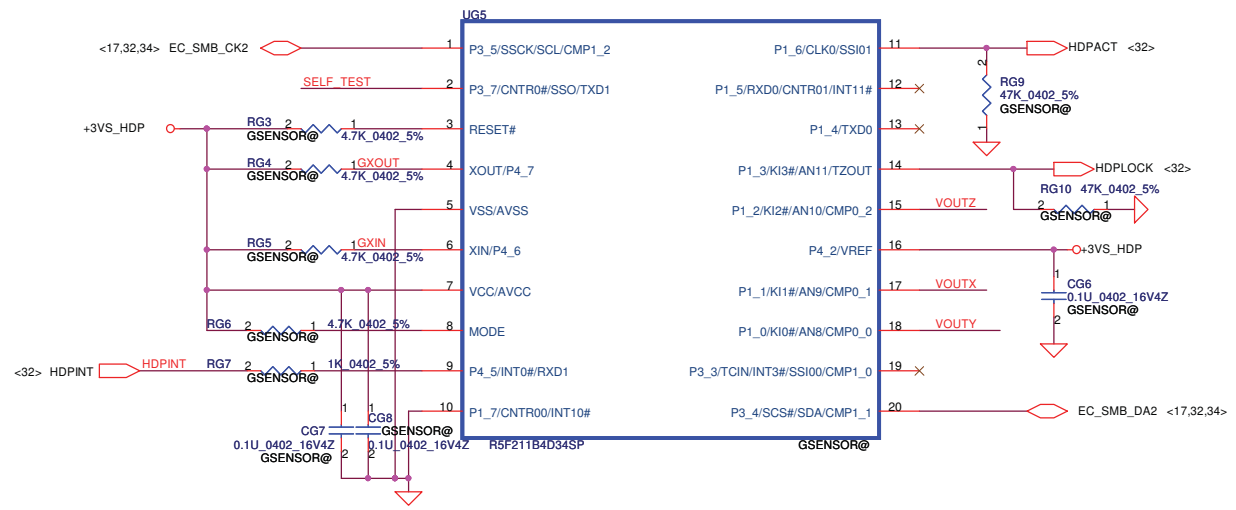
Top Layer Connections:

- Power and Ground:**
 - +5VS:** Connected to DG1, CG12, and the VIN pin of the GSENSOR.
 - +3VS:** Connected to the SHDN# pin of the GSENSOR.
 - +3VS_HDP:** Connected to the HDP pin of the GSENSOR and the VDD pin of the MMA7360LR2.
 - GND:** Connected to the GND pin of the GSENSOR and the GND pin of the MMA7360LR2.
- Signal and Control:**
 - ST (Sleep Test):** Connected to the ST pin of the MMA7360LR2.
 - Q-SELECT:** Connected to the Q-SELECT pin of the MMA7360LR2.
 - SLEEP#:** Connected to the SLEEP# pin of the MMA7360LR2.
 - 0G-DET:** Connected to the 0G-DET pin of the MMA7360LR2.
- Other Components:**
 - Resistors:** RG2 (0.0603 5%), CG10 (0.1U 0402 16V4Z), CG11 (0.1U 0402 16V4Z), CG14 (0.22U 0402 10V4Z).
 - Capacitors:** CG12 (1U 0402 6.3V6K), CG13 (1U 0402 6.3V6K).
 - Microcontroller:** MMA7360LR2_LGA14.

Reserve for 2nd Source:

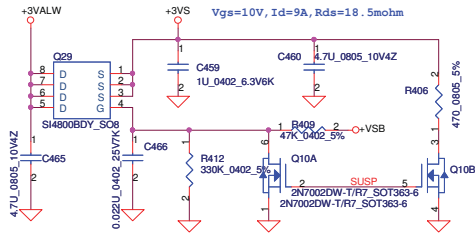
- CG9:** 0.1U 0402 16V4Z
- UG4:** 1VOUT2
- CG10:** 0.1U 0402 16V4Z
- UG4:** 1VOUT3
- CG11:** 0.1U 0402 16V4Z
- UG4:** 1VOUT4

Place UG1 and UG4 on TOP Layer

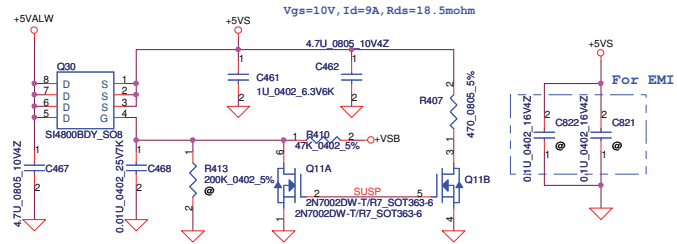


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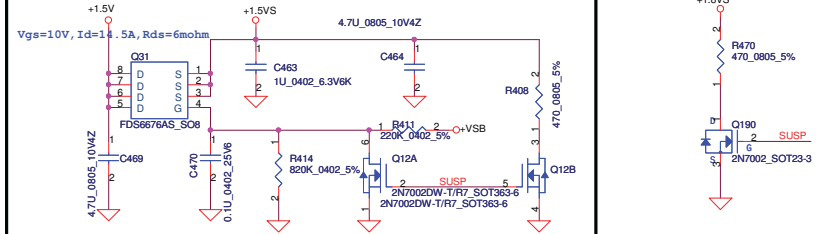
+3VALW TO +3VS



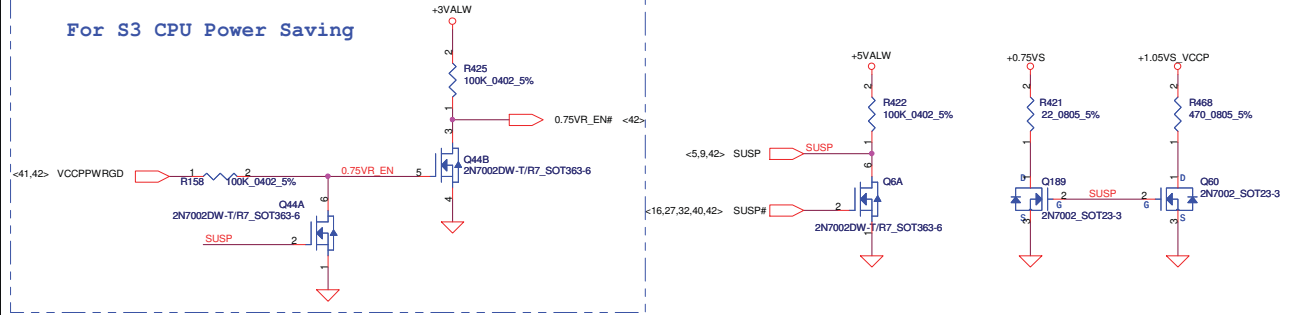
+5VALW TO +5VS



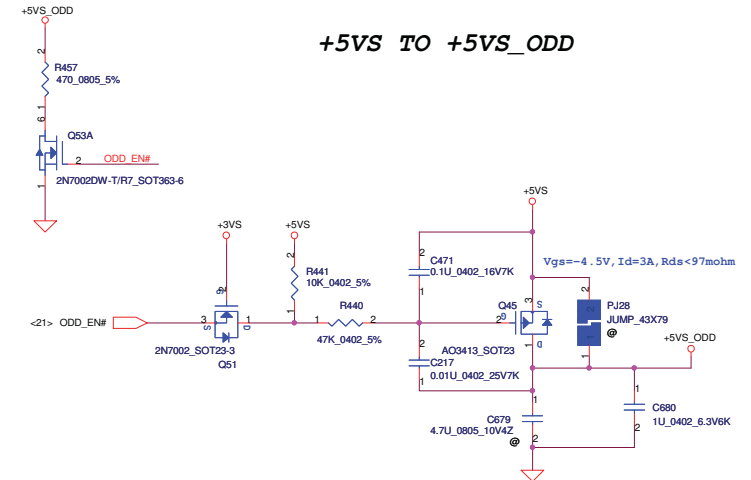
+1.5V to +1.5VS



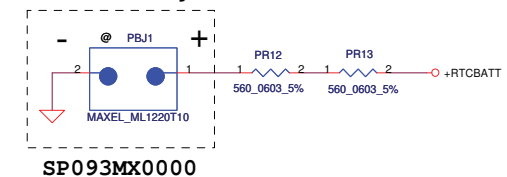
For S3 CPU Power Saving

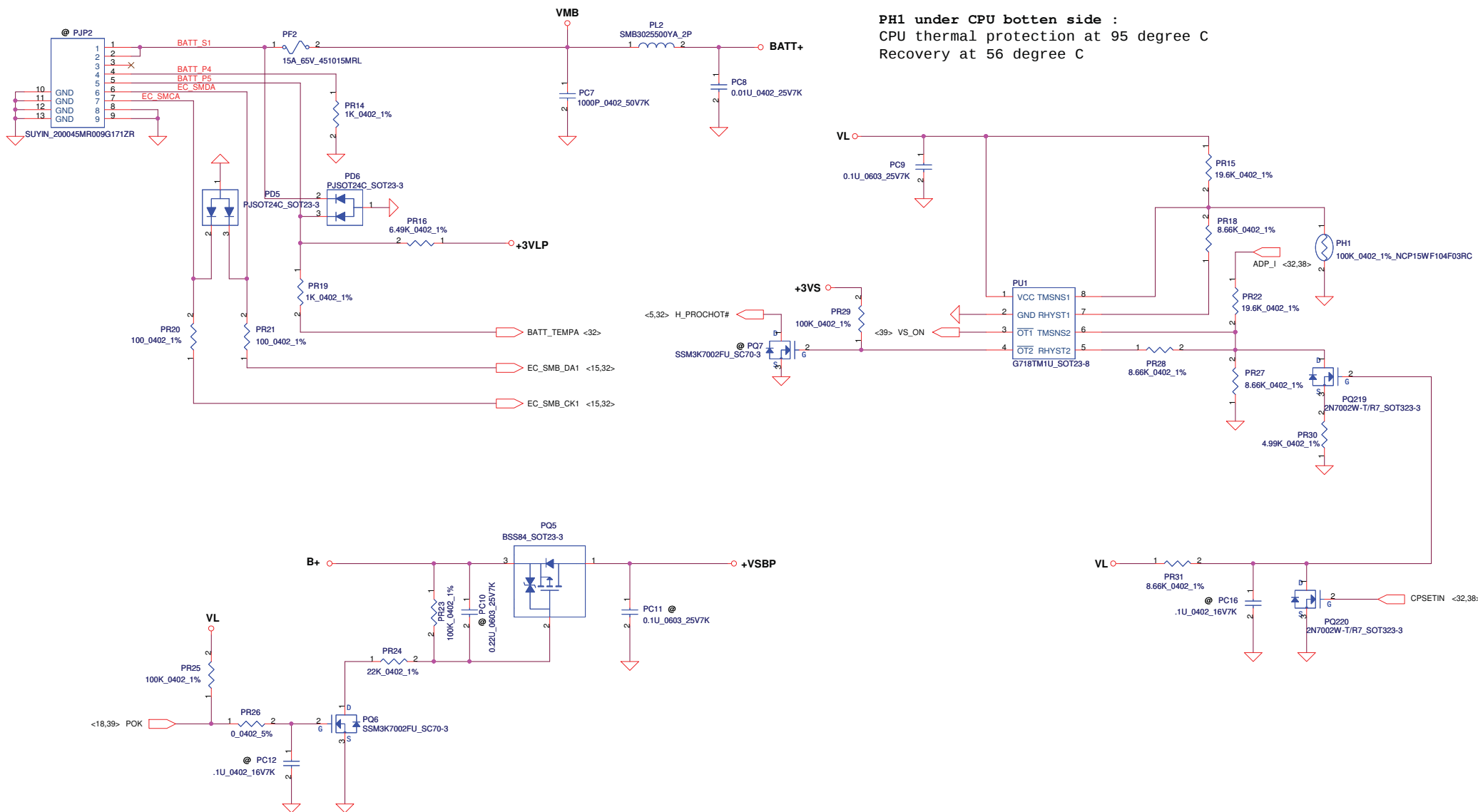


+5VS TO +5VS_ODD

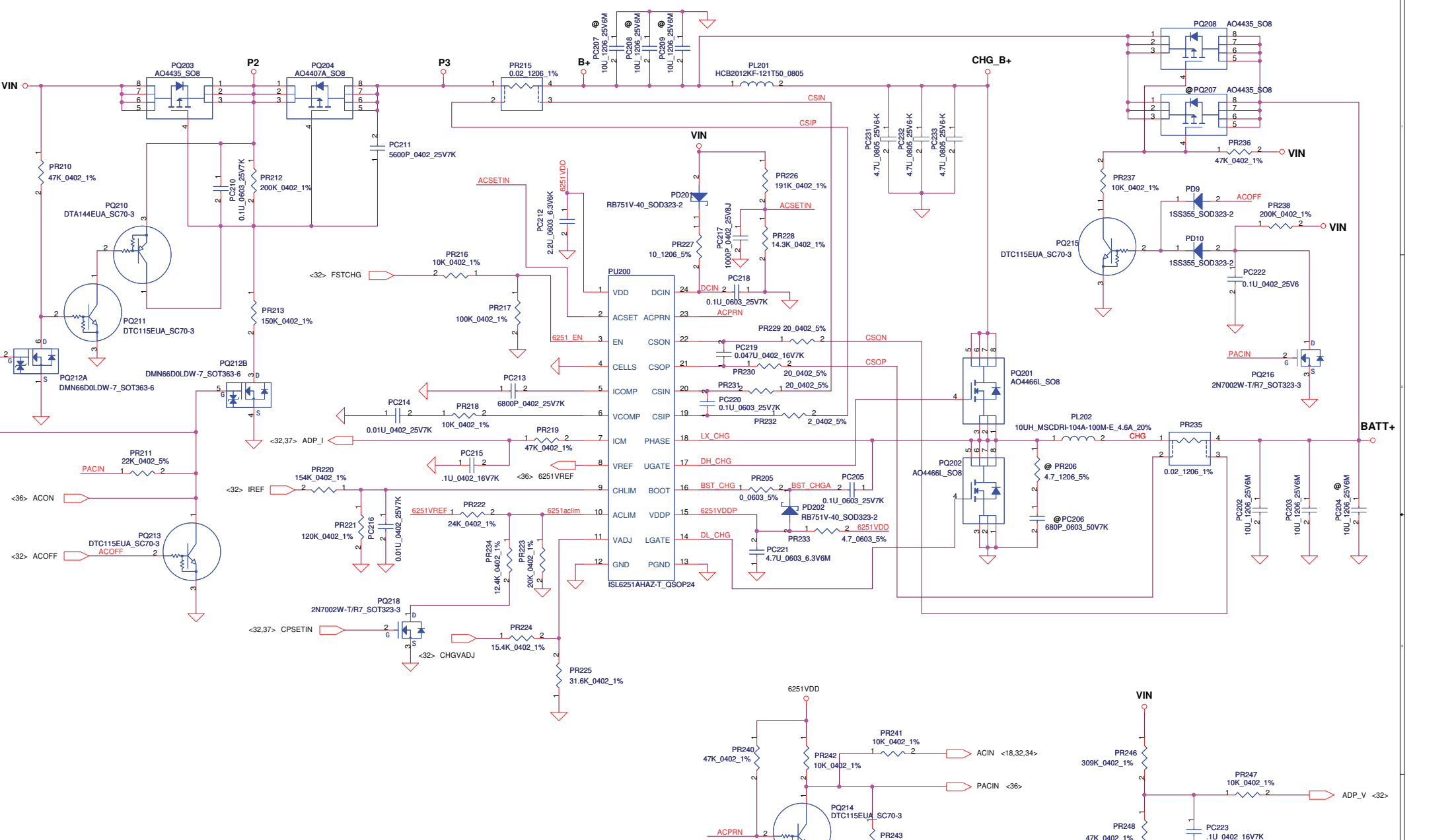


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CP mode

I _{ada} =0~3.42A (65W)	CP= 92%*I _{ada} ; CP=3.147A
V _{ac1im} =1.08V (65W)	PR222=75k PR223=20k PR45=0.02
I _{ada} =0~3.947A (75W)	CP= 92%*I _{ada} ; CP=3.63A
V _{ac1im} =0.736V (75W)	PR222=24k PR223=20k PR45=0.02
I _{ada} =0~4.737A (90W)	CP= 92%*I _{ada} ; CP=4.36A
V _{ac1im} =0.736V (90W)	PR222=53.6k PR223=20k PR45=0.015
I _{ada} =0~6.316A (120W)	CP= 92%*I _{ada} ; CP=5.81A
V _{ac1im} =0.736V (120W)	PR222=8.25k PR223=26.7k PR45=0.015

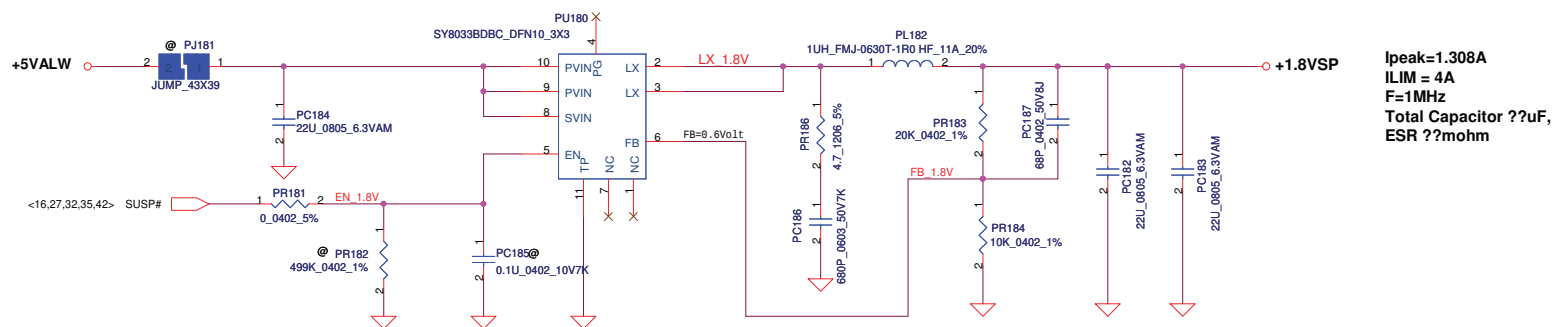
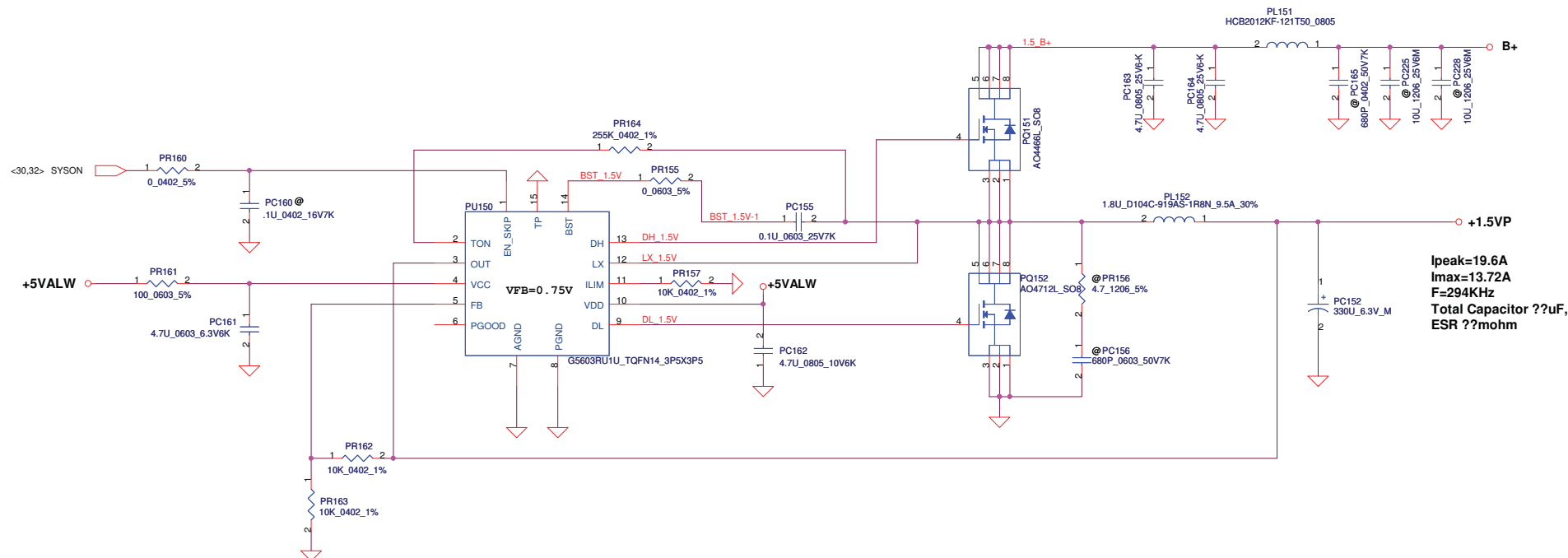
CC=0.25A~3A
IREF=1.016*I_{charge}
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(V _{cell} -4)*9.445	
V _{cell}	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

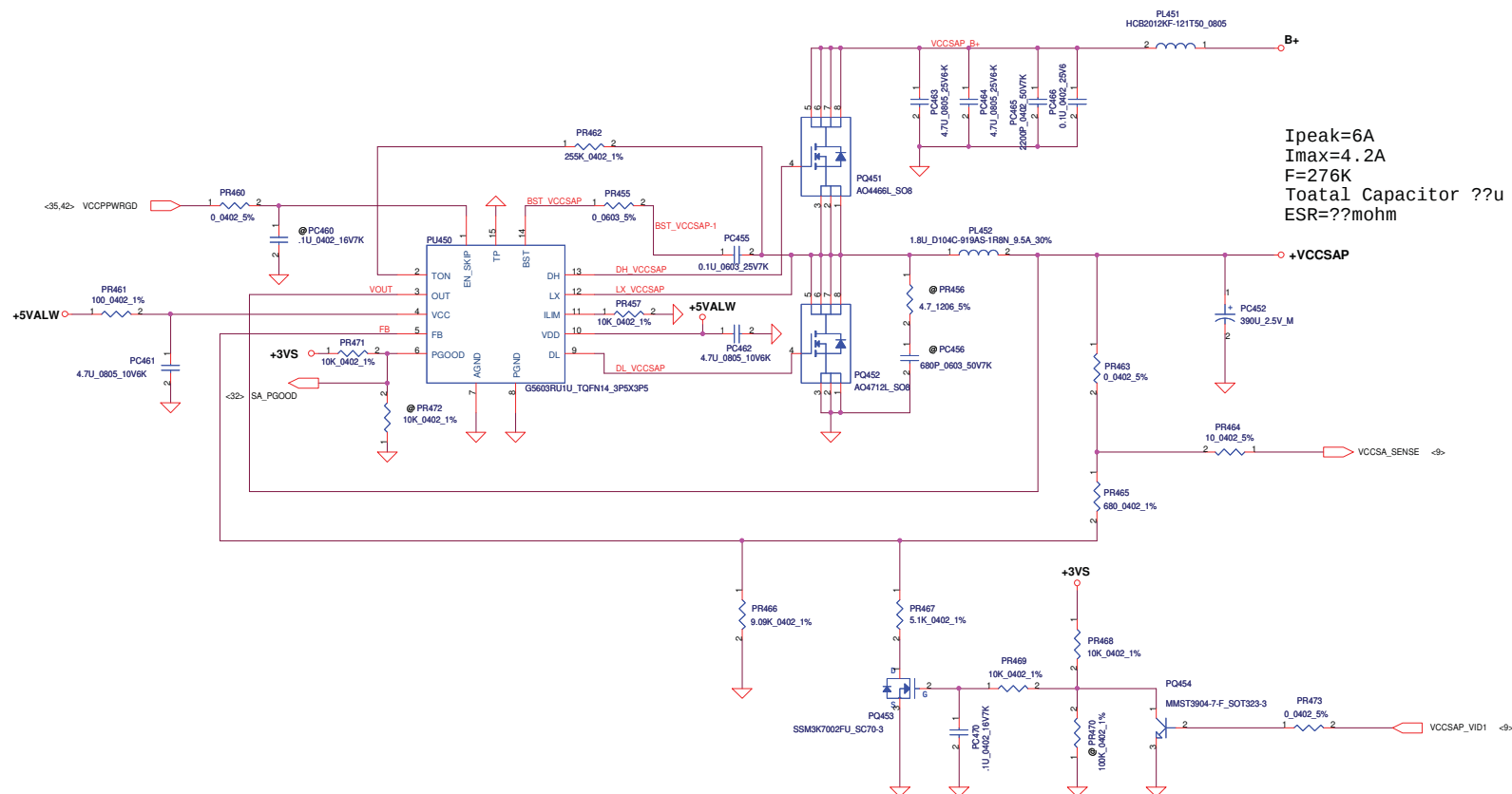
Vin Detector

High	18.089V
Low	17.44V

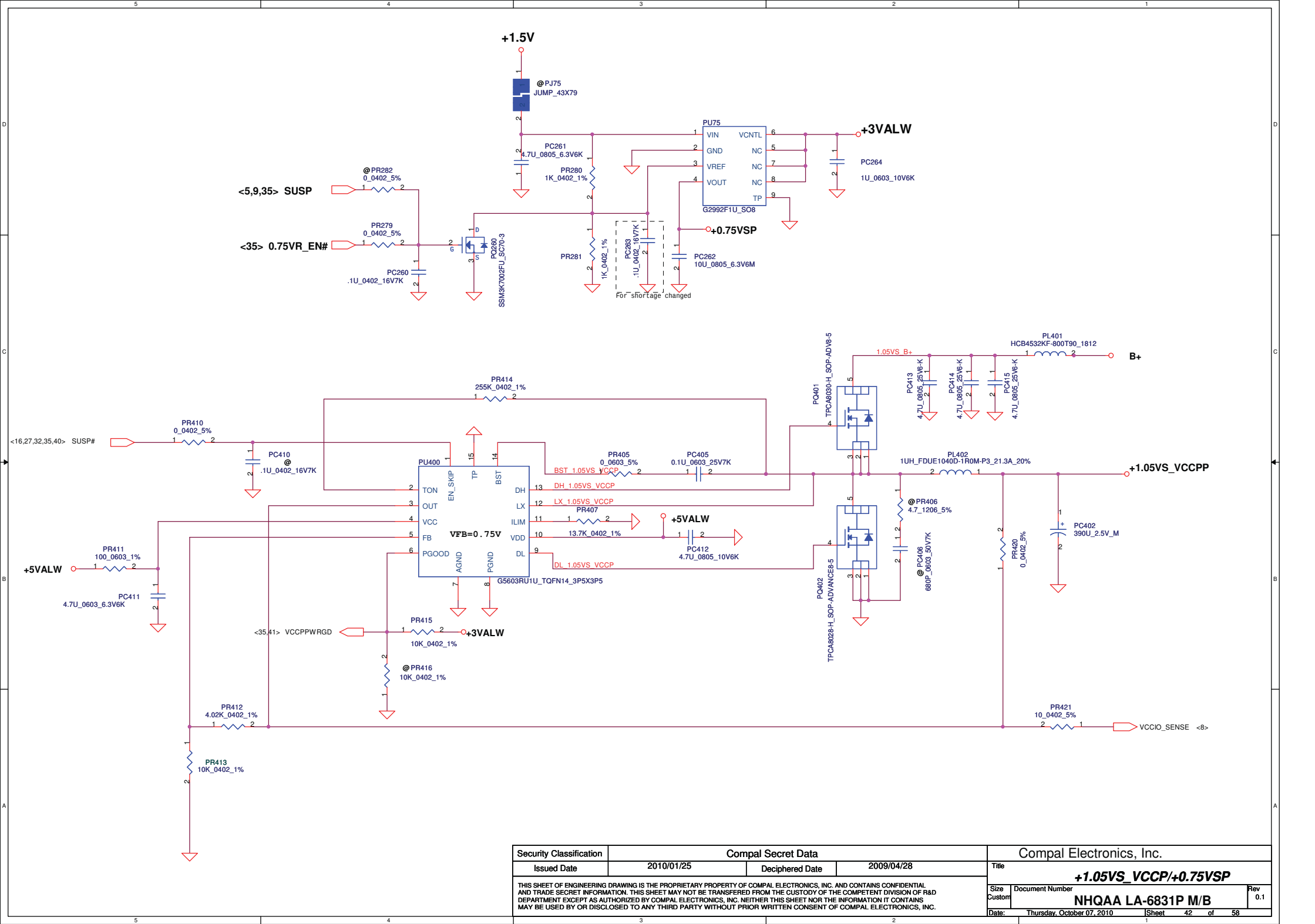
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				Rev	0.1

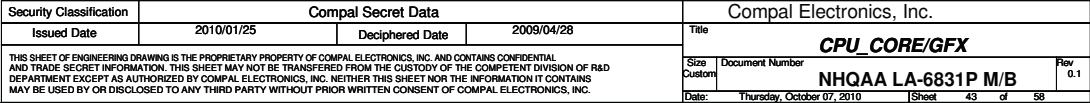


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Custom					0.1
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VID1	+VCCSAP
1	0.8V
0	0.9V





NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	2010/09/07	P37-PWR_BATTERY CONN / OTP	Remove PQ7 SSM3K7002FU	Adapter protect circuit not ready
2.	2010/09/07	P40-PWR-+1.5VP/+1.8VSP	Change PQ152 to A04712L	Use same part number
3.	2010/09/07	P41-PWR_+VCCSAP	Change PQ452 to A04712L	Use same part number
4.	2010/09/07	P40-PWR-+1.5VP/+1.8VSP	Change PQ151 to A0446L	Use same part number
5.	2010/09/07	P53-PWR_+VCCSAP	Change PQ451 to A0446L	Use same part number
6.	2010/09/07	P50-PWR-CHARGER	Change PQ201,PQ202 to A04466L	Use same part number
7.	2010/09/07	P50-PWR-CHARGER	Change PQ203 to A04435L and remove PQ207	For UMA SKU
8.	2010/09/07	P50-PWR-CHARGER	Add PR234 12.4k	For DC and QC CP setting
9.	2010/09/07	P55-PWR-CPU_CORE/GFX	Add PR560 0 Ohm	Set CPU VB00T to 0V
10.	2010/09/07	P50-PWR-CHARGER	Add PR222 24k and PR223 20k	For CP setting
11.	2010/09/07	P55-PWR-CPU_CORE/GFX	Add PR544 3.83k,PR545 27.4k,PH502 470k	Add CPU NTC NET
12.	2010/09/07	P55-PWR-CPU_CORE/GFX	Change PR551 from 3.83k to 3.65k	For CPU_CORE load line
12.	2010/09/07	P55-PWR-CPU_CORE/GFX	Change PC550 0.33u to 0.22u and add PC551 0.1u	For shortage issue

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				Power PIR	
				Size	Rev
				Document Number	
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HW PIR (Product Improve Record)

NWQAA LA-6832P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1

GERBER-OUT DATE: 2010/09/03

NO DATE PAGE MODIFICATION LIST

				PURPOSE	
Item	Date	Page	Component	Solution	Request
1)	07/21		Delete	30g,DHDMIg,DI8g,EDPg,NO3Dg,OPTg,UMAg	For low cost Huron River
2)	08/11		Update room		
3)	08/11	09	Change	R119 change to g	
4)	08/12	16	Add	R442, R443	For SPI debug circuit
5)	08/12	16	Change	R572, R573, R574, R575, R569 from g to mount	For SPI debug circuit
6)	08/12	20	Remove	USB20_P3/N3 from PCH	Don't need USB20/30 BTO
7)	08/12	30	Remove	DT1, USB20, RT14, RT20, RT23, RT24	Don't need USB20/30 BTO
8)	08/12	32	Change	C449, C450, Y4 from g to mount	
9)	08/13	15	Change	L8, L9 L10, L11 from SM070001600 to SM070001310	For EMI demand
10)	08/13	30	Change	RT11 to g	
11)	08/13	30	Change	RT19 to USB30g	
12)	08/13	30	Change	CT3 from SE0000005TN0 to SE0000005T80	
13)	08/13	30	Remove	RT25, RT27	Don't need USB20/30 BTO
14)	08/17	5	Remove	R14	For HW Review demand
15)	08/18	6	Reserve	R33	For HW Review demand
16)	08/18	9	Reserve	R119	To follow CRB 1.0
17)	08/18	11	Remove	R32, R89	For HW Review demand
18)	08/18	12	Remove	R35, R97	For HW Review demand
19)	08/18	26	Reserve	C236, C268, C490	For HW Review demand
20)	08/18	15	Remove	R435, R438, R453(0 ohm)	
21)	08/18	15	Change	R195, R197, R198, R202, R201, R203, R205, R206 to SD028680080	
22)	08/18	15	Remove	R207	For HW Review demand
23)	08/18	18	Change	Net name from PM_CLKRUN# to PCH_GPI032	For HW Review demand
24)	08/18	20	Change	R324 From 1K to 2.2K	For Intel check list demand
25)	08/18	21	Remove	PCH PECl signal	By HW Review demand
26)	08/18	25	Remove	C363, C364, C365, C366	By HW Review demand
27)	08/18	30	Change	U74 to SA00004600	For CIC demand
28)	08/18	30	Change	USB30g to always mount	Due to no BTO USB20/30.
29)	08/18	27	Remove	all new card function	
30)	08/20	9	Add	PJ32	For Cost down +1.5V to +1.5V_CPU
31)	08/20	13	Swap	USB20_P11 and USB20_N11	For layout request
32)	08/20	25	Swap	USB20_P0, USB20_N0, USB20_P1, USB20_N1	For layout request
33)	08/23		Update Power schematic		
34)	08/23	20	Swap	PCI_PIRQC#, PCH_GPI04, PCH_GPI02, PCI_PIRQA#	For layout request
35)	08/23	20	Swap	SLP_CHG_M3, SLP_CHG_M4, USB_OC#0	For layout request
36)	08/30	18	Reserve	R259	For cost down plan
37)	08/30		Change	USB3.0 Connector	For ME demand
38)	08/30	21	Add	USB Sleep & Charge MAXIC_Select pin in GPIO71(Remove T73)	For MAX14550E/14566B co-lay
39)	08/30	25	Change	C426 to Aluminum Solid Cap 220u	For cost down
40)	08/30	27	Add	USB Sleep & Charge IC: MAX14550E	
41)	08/30	28	Add	16pin X'form for cost down, and P/N is SP050006E00	For cost down
42)	08/30	28	Change	PWRME_CTRL# from PCH_GPI033 to HDA_SDO	By Intel spec
43)	08/30	16	Change	U53 PIN 9 from KS14 to KS13	
44)	08/30	16	Change	R442, R443 from 10k to 100K	
45)	08/30	16	Change	U56 Pin3 from KSO6 to +5VALW	
46)	08/30	16	Add	R227 100k ohm	
47)	08/30	28	Reserve	D85 and D86	For ESD request
48)	08/30	30	Swap	U3RXDN1_R, U3RXDN1_R_L, U3RXDP1_R, U3RXDP1_R_L	For layout request
49)	08/30	16	Change	U13 from SA000021A00 to SA000031N00	Due to EOL of SA000021A00
50)	08/30	27	Reserve	R1443 for WLAN Mini PCIE Card Pin5	
51)	08/30	33	Change	U22 From SA00003GK00 to SA00003GM10	Due to EOL of SA00003GK00
52)	08/30	34	Change	SW1, SW4 to SN100002Y00	
53)	09/01	28	Add	LL5 for ISN Test	For EMI demand
54)	09/01	31	Change	RA12 from 10k to 4.7kohm and CA18 from 0.1uF to 100pF	For Beep by A51 demand.
55)	09/01	32	Add	CPSETIN to power	For 65W/75W select
56)	09/01	18,20,21	Reserve	C894, C895, C896, C897	For ESD request
57)	09/02	08	Remove, add	C126, C131 and add C898 3Pin Bulk Cap	By Power Demand
58)	09/02	27	Add	14566g & 14550g	
59)	09/02	27	Change	U5 Pin8 control pin from SLP_CHG# to SLP_CHG_M4	
60)	09/02	33	Change	EC ROM size from 256KB(SA00003GM10) to 128KB(SA00003FL10)	
61)	09/02	11	Change	C165,C166,C168,C171,C174,C176,C178 from SE093106M80 to SE0000005T80	For sourcer demand
62)	09/02	12	Change	C191,C192,C194,C197,C200,C202,C204 from SE093106M80 to SE0000005T80	For sourcer demand
63)	09/02		Change	CT25 from SE093106K80 (10uF_0805) to SE0000005T80 (10uF_0603)	For sourcer demand
64)	09/03	08	Change	C890, C891, C894 from SGA000005R00 to SGA00004X80	For Power demand
65)	09/06	33	Change	U22 change to SA00003FL10	
66)	09/06	28	Delete	U14 8105ELDOg and 8105ESWRg	

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