

Sakhir 10, 10C, 10G

LA-2491 Schematics Document

Intel Dothan / Alviso GM(PM) / DDR-1 / ICH6-M / Fix Bay
(nVIDIA NV43M / NV44M / ATi M22 / M24)

2004 / 11 / 28

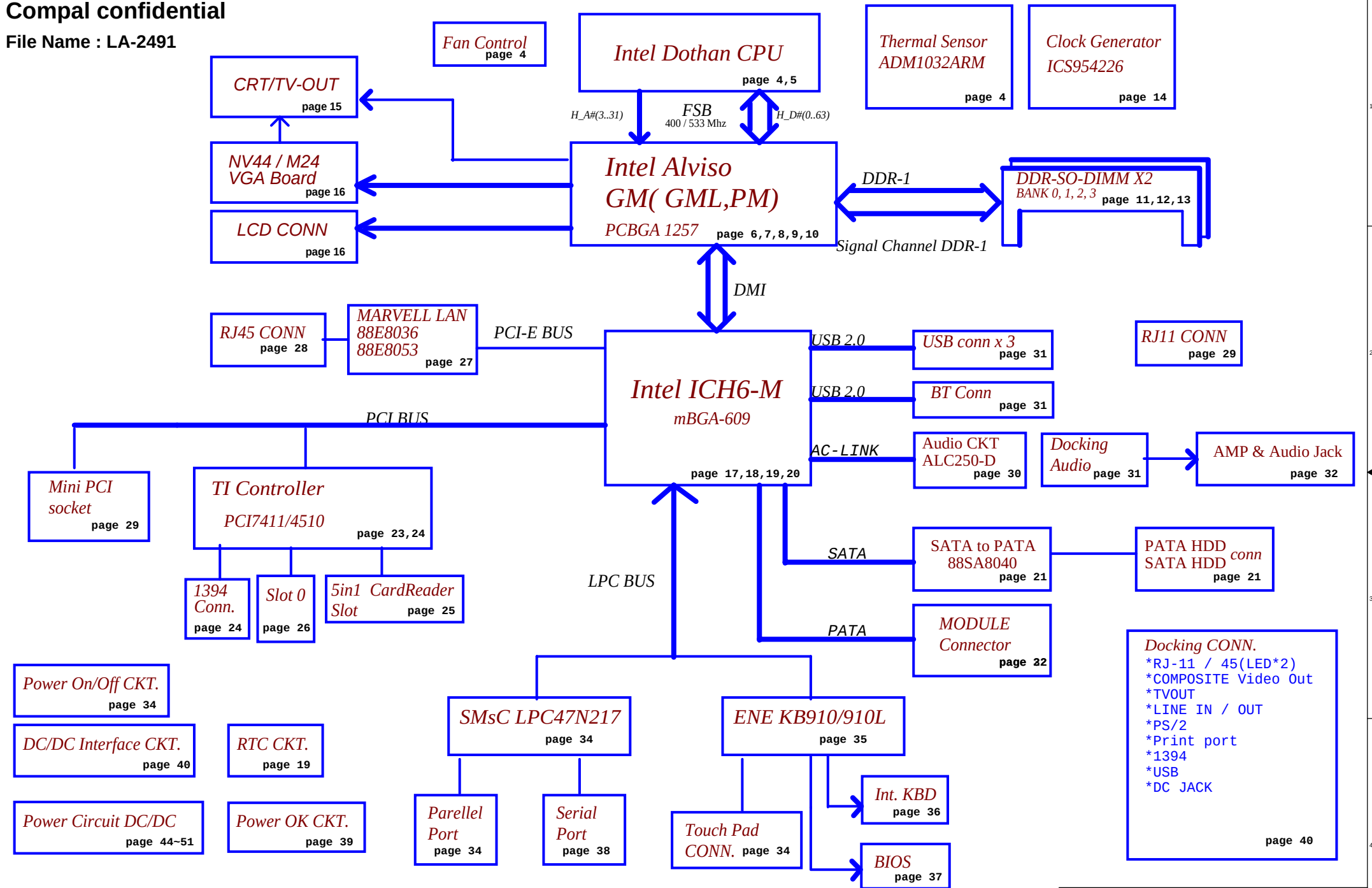
Rev:1.0

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Compal Electronics, Inc.	
Title	Cover Sheet
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Compal confidential

File Name : LA-2491



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+DDRVTT	1.25V switched power rail for DDR terminator	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+DDRVCC	2.5V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5VCD	5V switched power rail for Direct CD	ON	OFF	OFF
+5VMOD	5V switched power rail for Module Bay	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB
1394	AD20	2	PIRQA/PIRQB
SD	AD20	2	PIRQA/PIRQB
Mini-PCI	AD18	1	PIRQG/PIRQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b	2'nd Battery	1001 011X b
(24C04)	1011 000Xb	Docking	1010 000X b

ICH6M SM Bus address

Device	Address
Clock Generator (ICS 952623)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 001Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

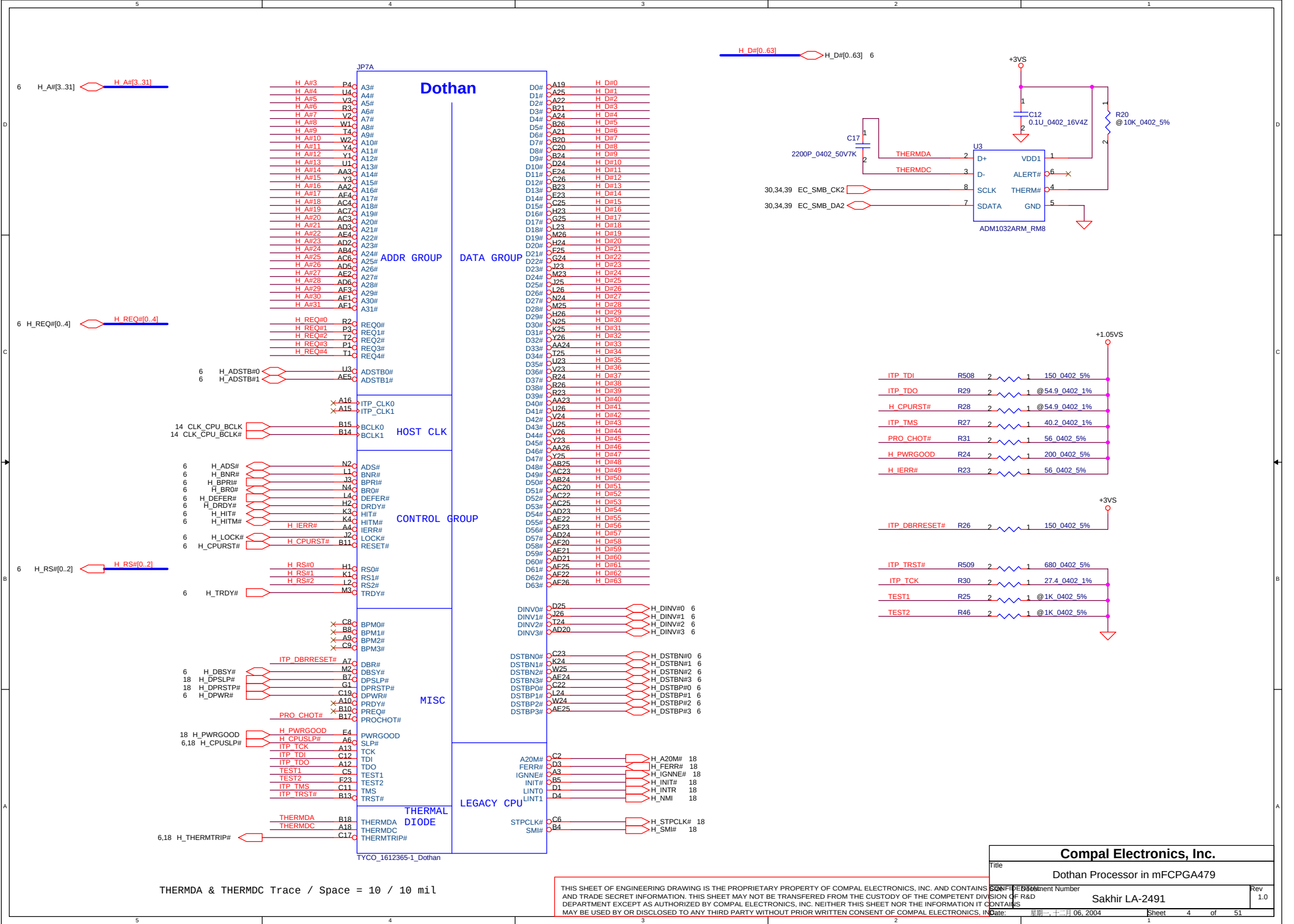
Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

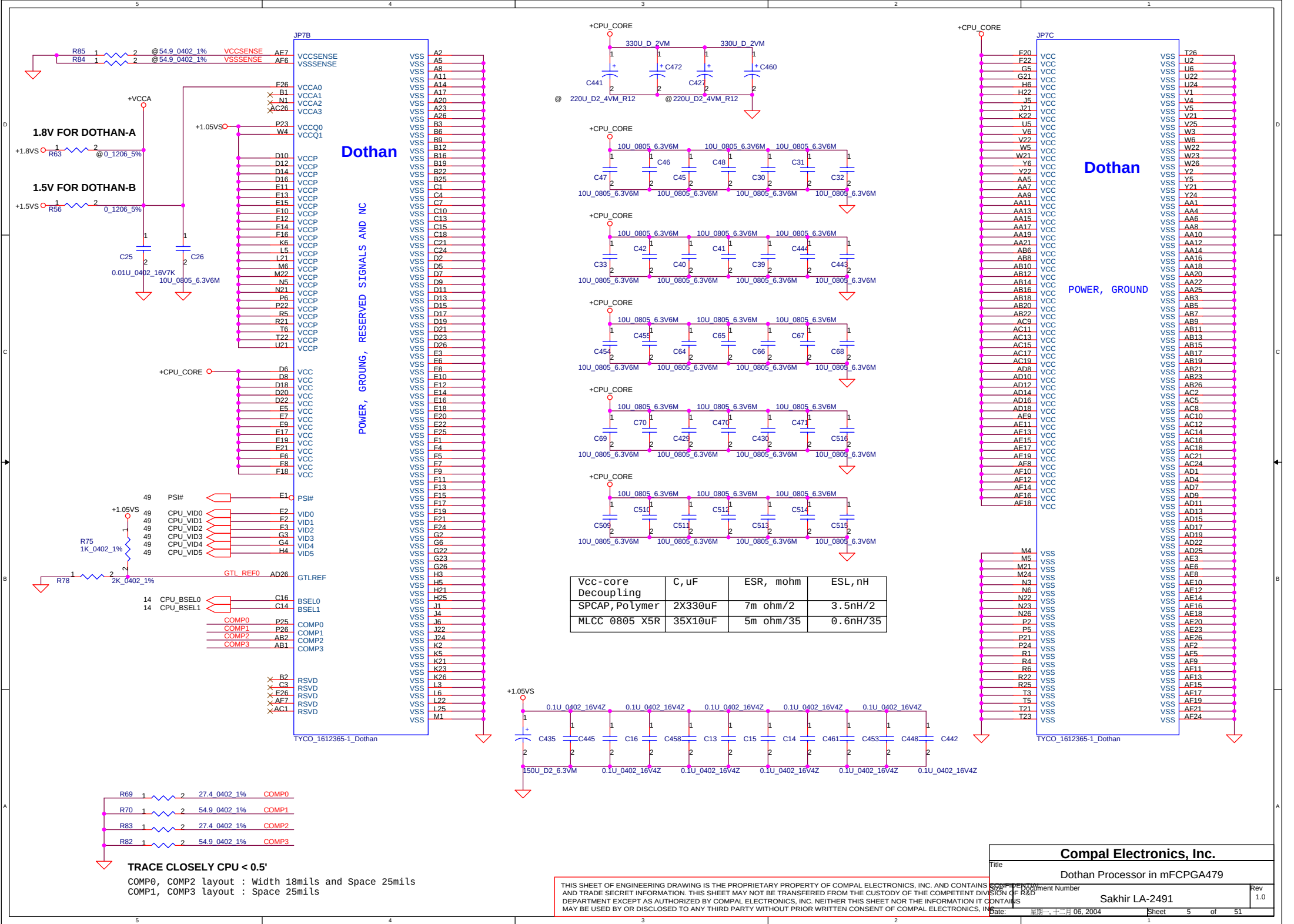
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

SKU ID Table

	SKU_ID_CHECK_1	7	6	5
SKU_ID_CHECK_0		1-Button	3-Buttons	7-Buttons
0	10	1		0
1	10C	3	12	2
2	10G	5		4
3	10GC	7	13	6
4	10J	11		10
5				
6				



THERMDA & THERMDC Trace / Space = 10 / 10 mil



D

C

B

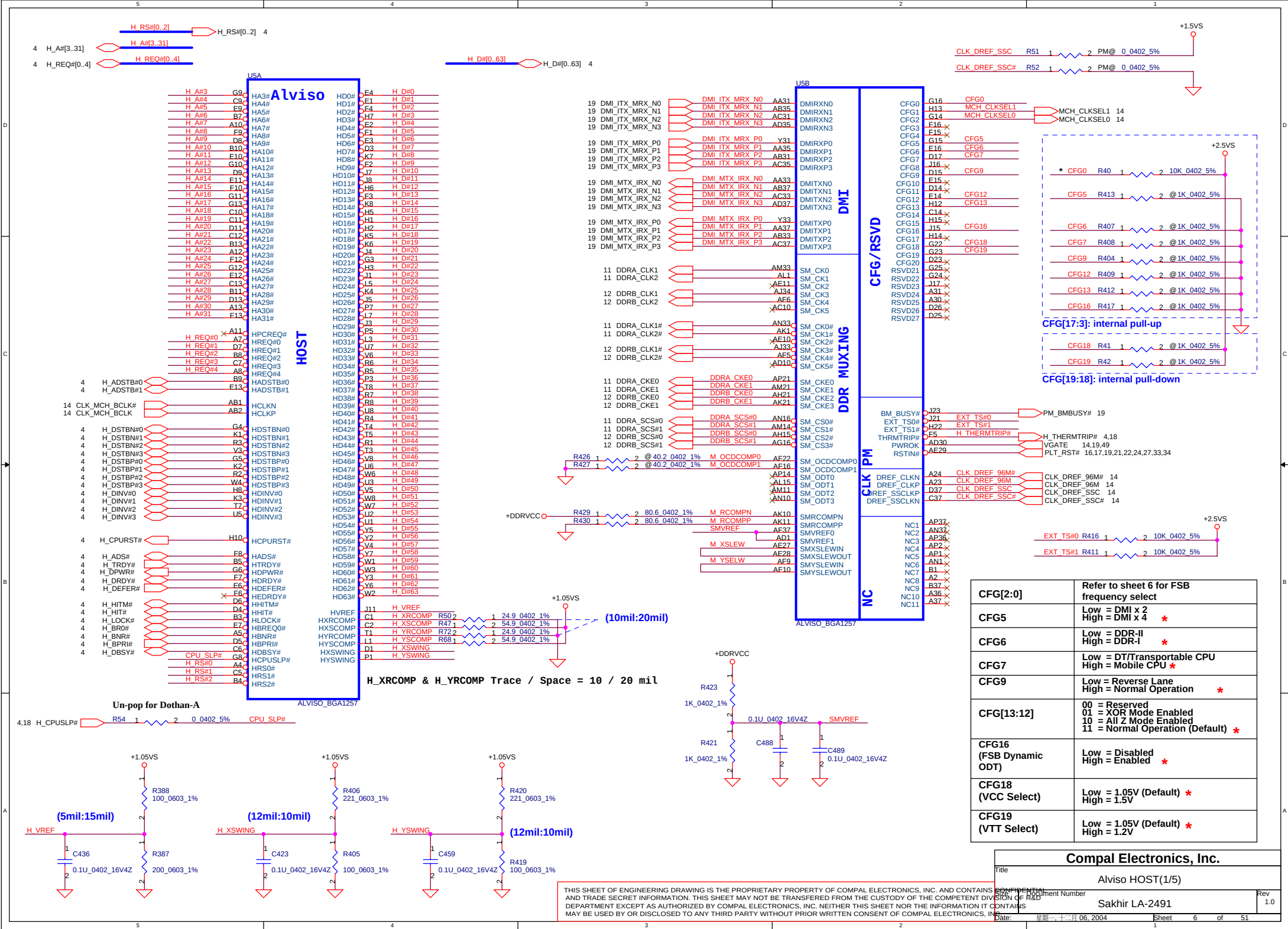
A

D

C

B

A



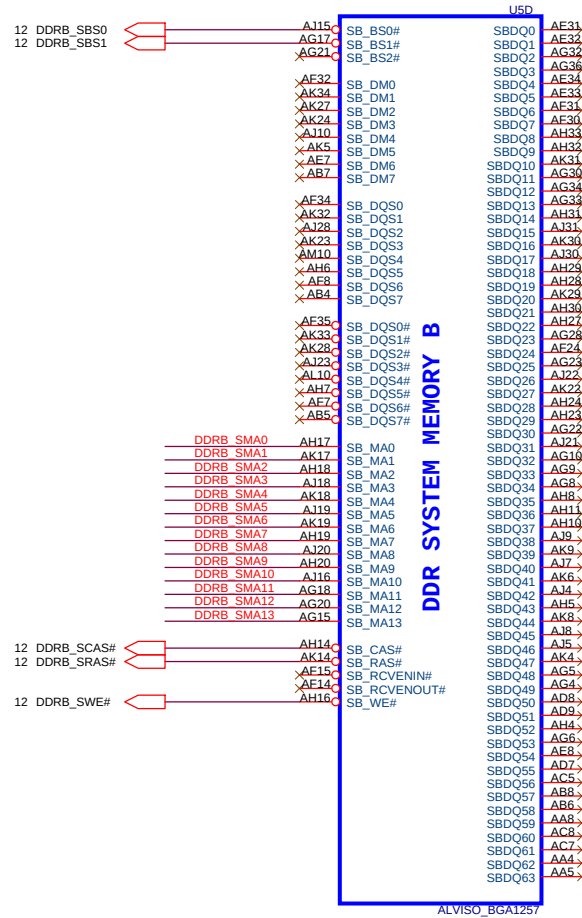
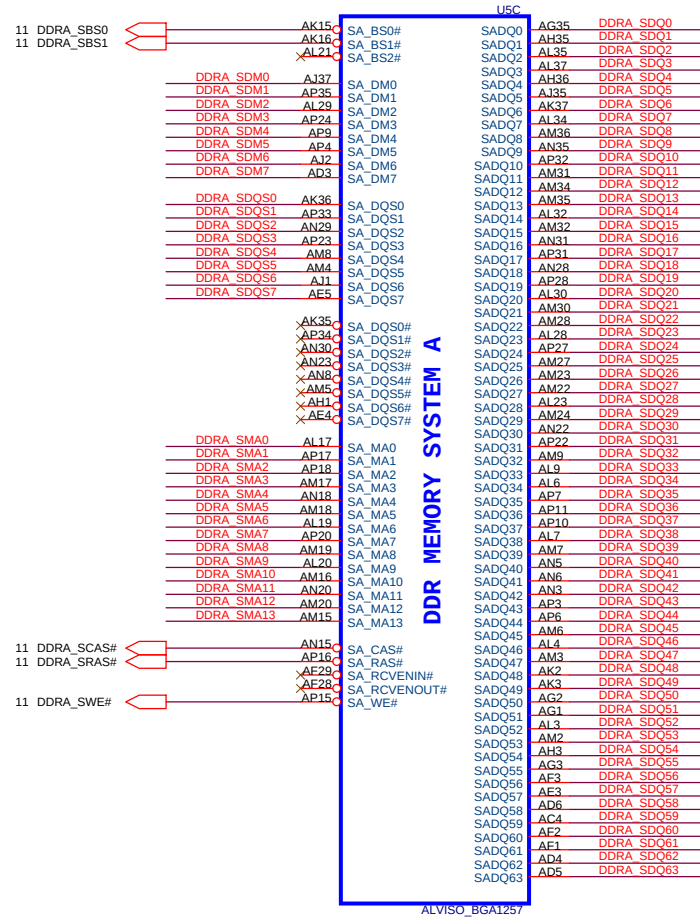
CFG[2:0]	Refer to sheet 6 for FSB frequency select
CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = DDR-II High = DDR-I *
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All 2 Mode Enabled 11 = Normal Operation (Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V

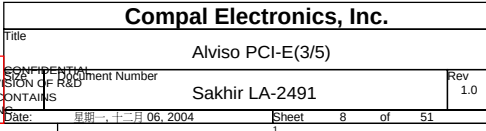
Compal Electronics, Inc.	
Title	Alviso HOST (1/5)
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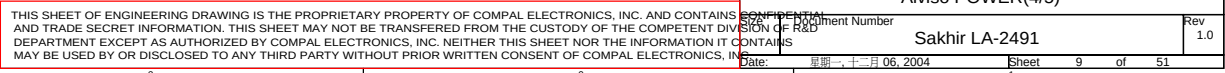
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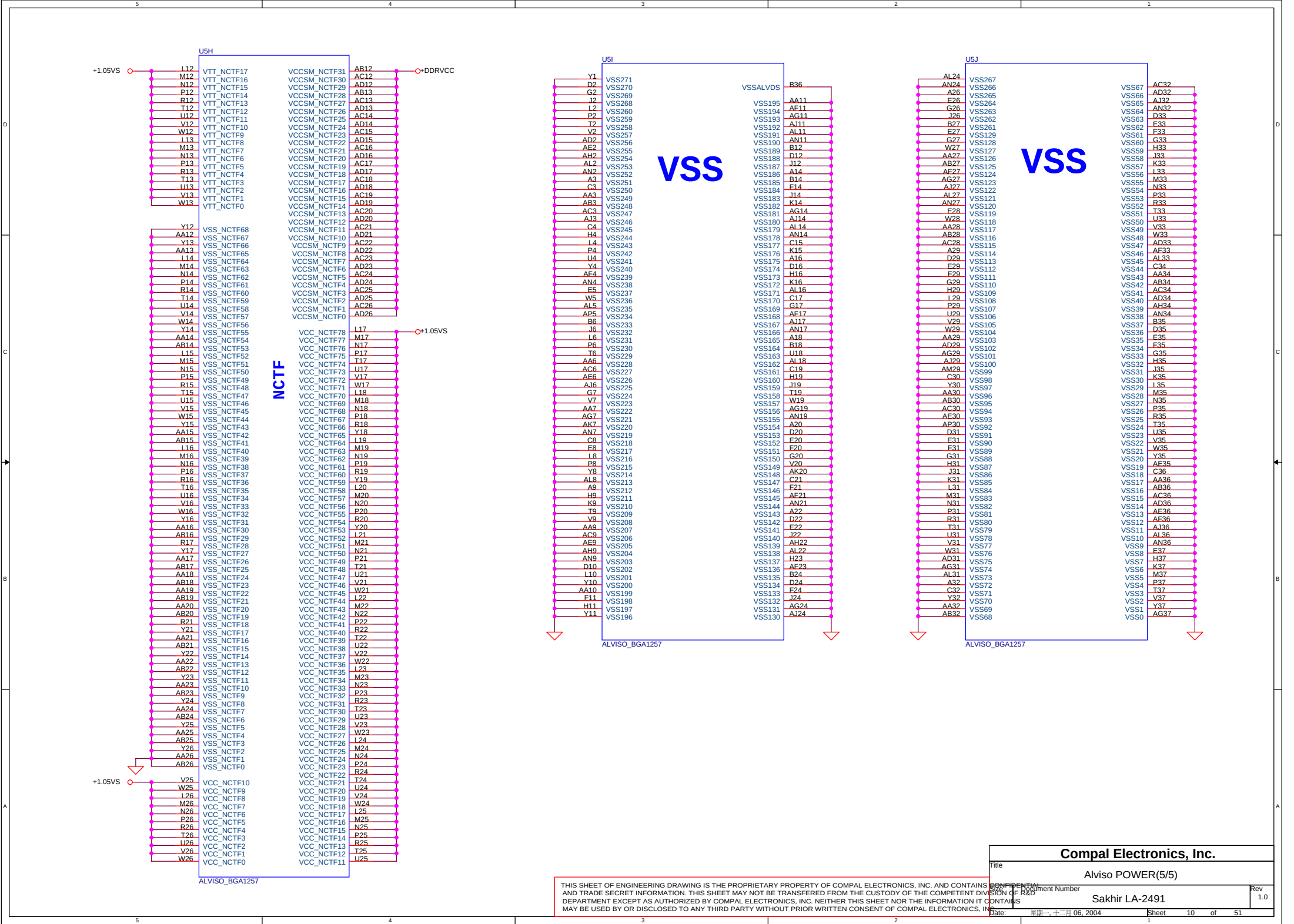
11 DDRA_SDQ[0..63] < DDRA_SDQ[0..63]
11 DDRA_SDM[0..7] < DDRA_SDM[0..7]
11 DDRA_SDQS[0..7] < DDRA_SDQS[0..7]
11 DDRA_SMA[0..13] < DDRA_SMA[0..13]

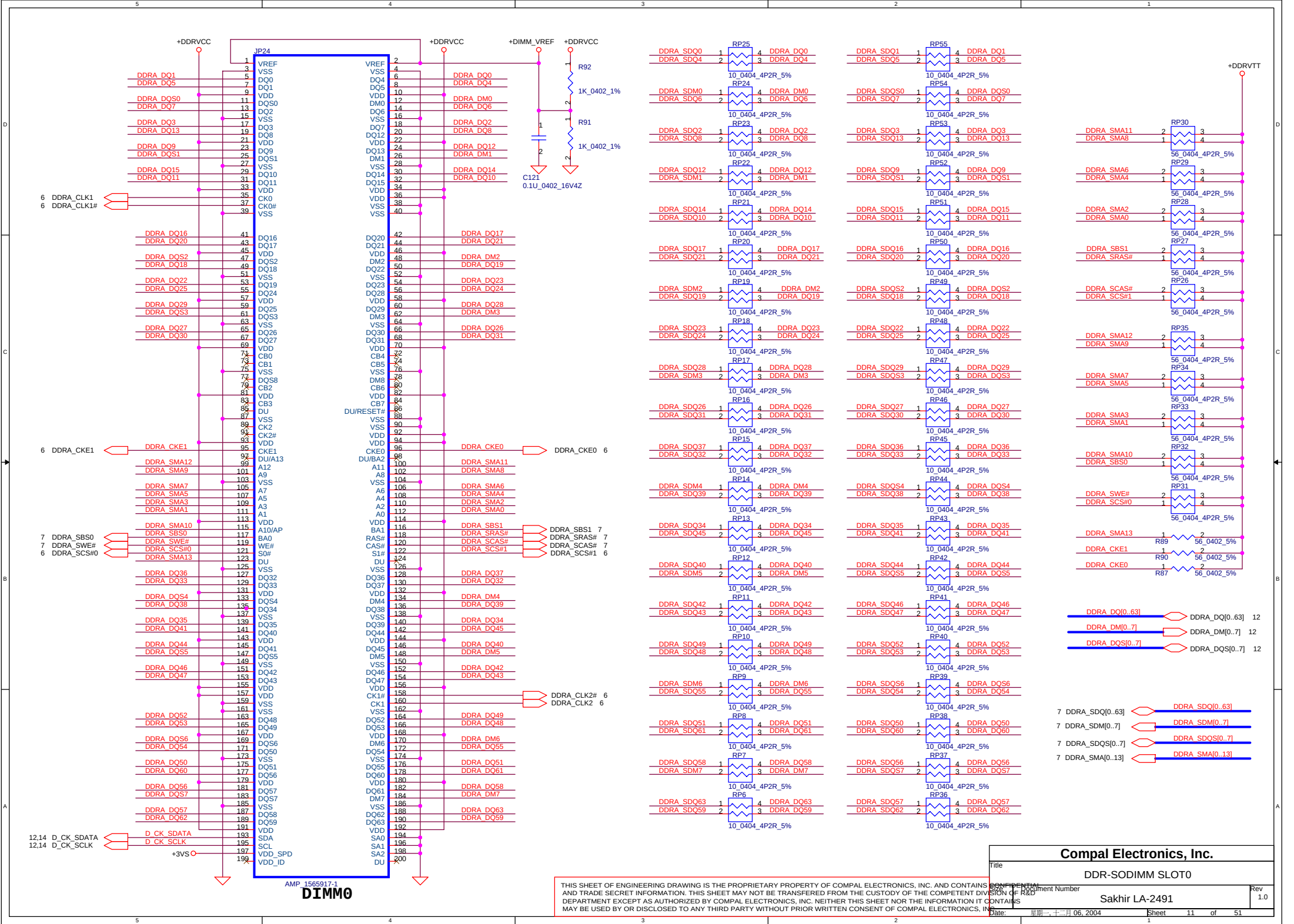
12 DDRB_SMA[0..13] < DDRB_SMA[0..13]





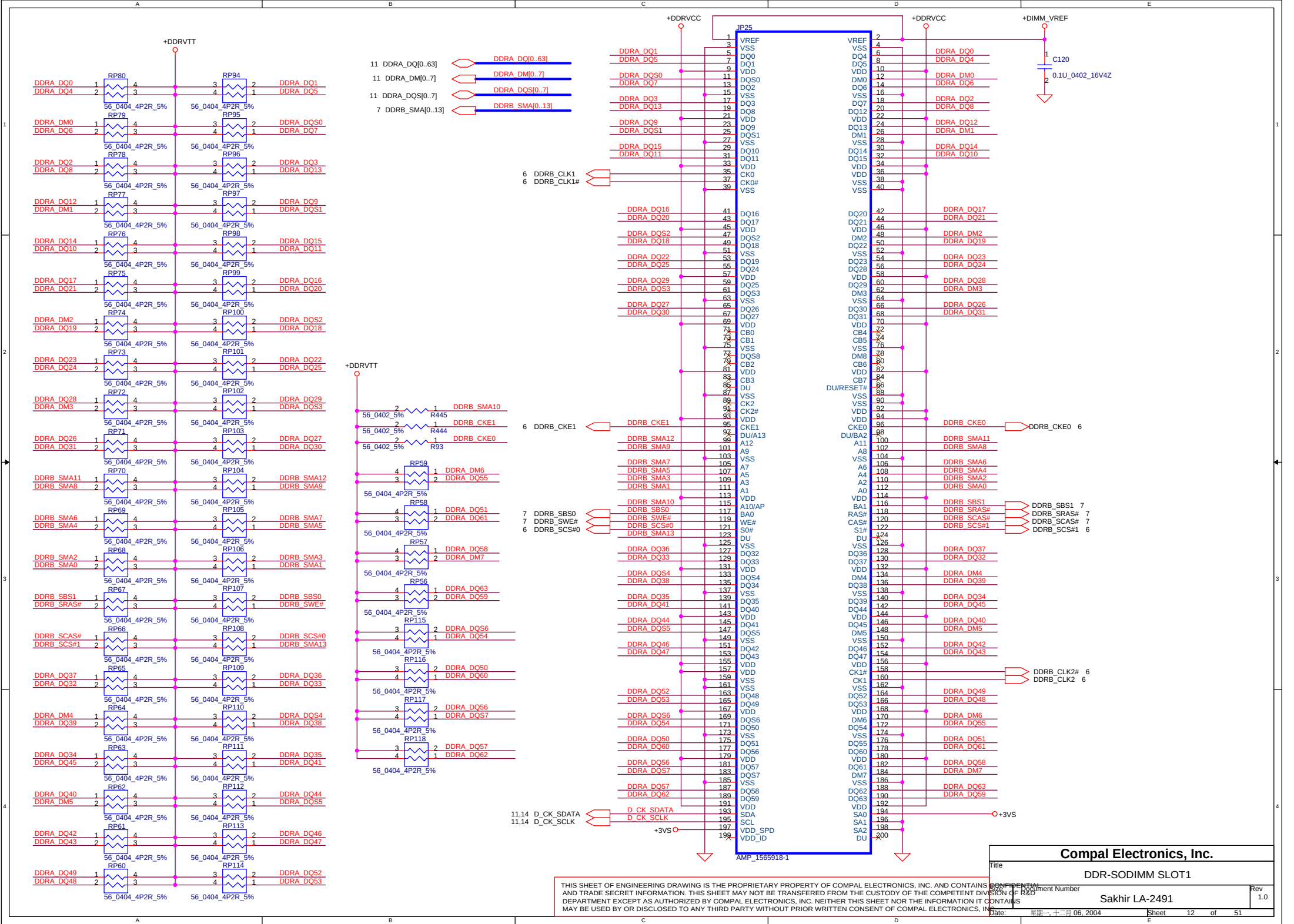






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Compal Electronics, Inc.

DDR-SODIMM SLOT1

Sakhir LA-2491

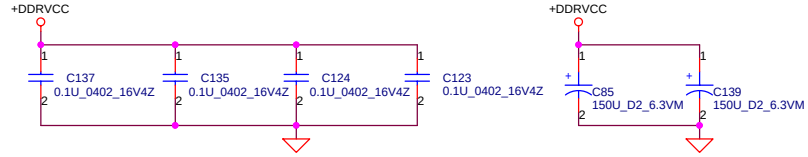
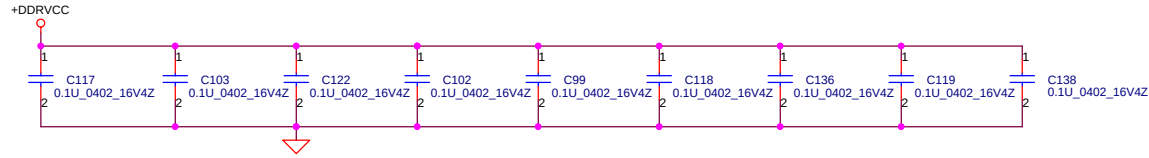
Rev 1.0

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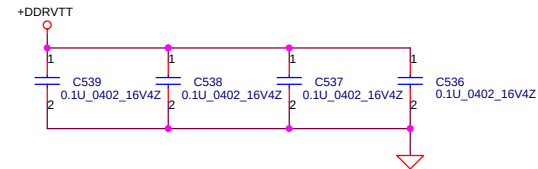
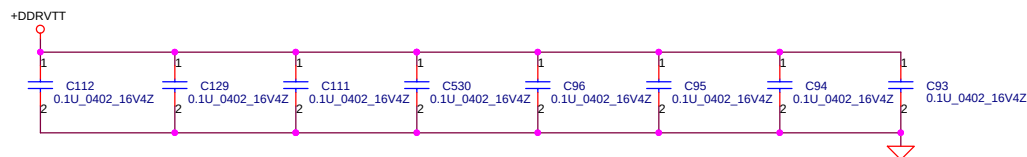
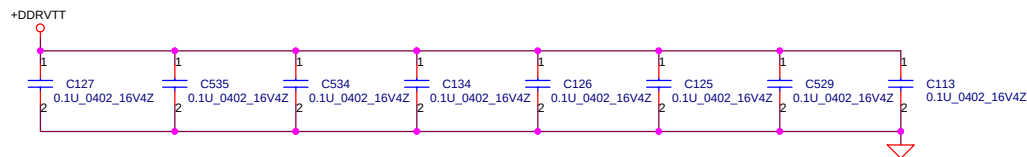
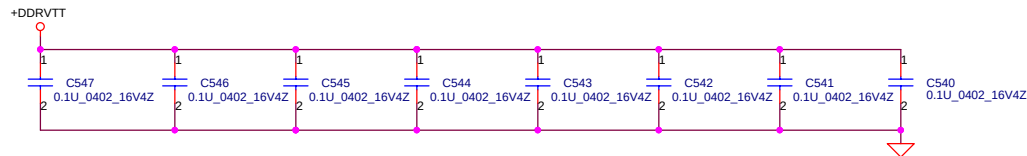
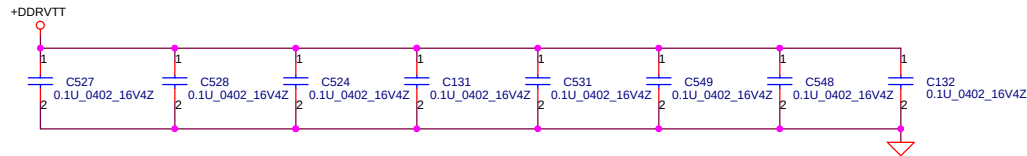
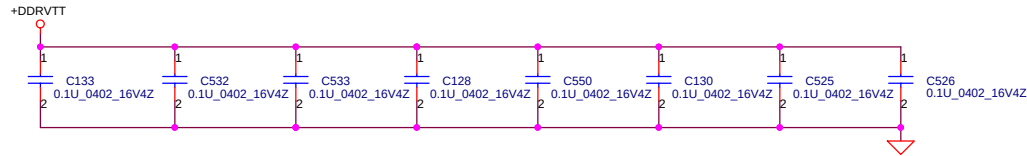
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Layout note :
Distribute as close as possible
to DDR-SODIMM.



Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25V



CRT Connector

Pop with No-Docking

TV-OUT Conn.

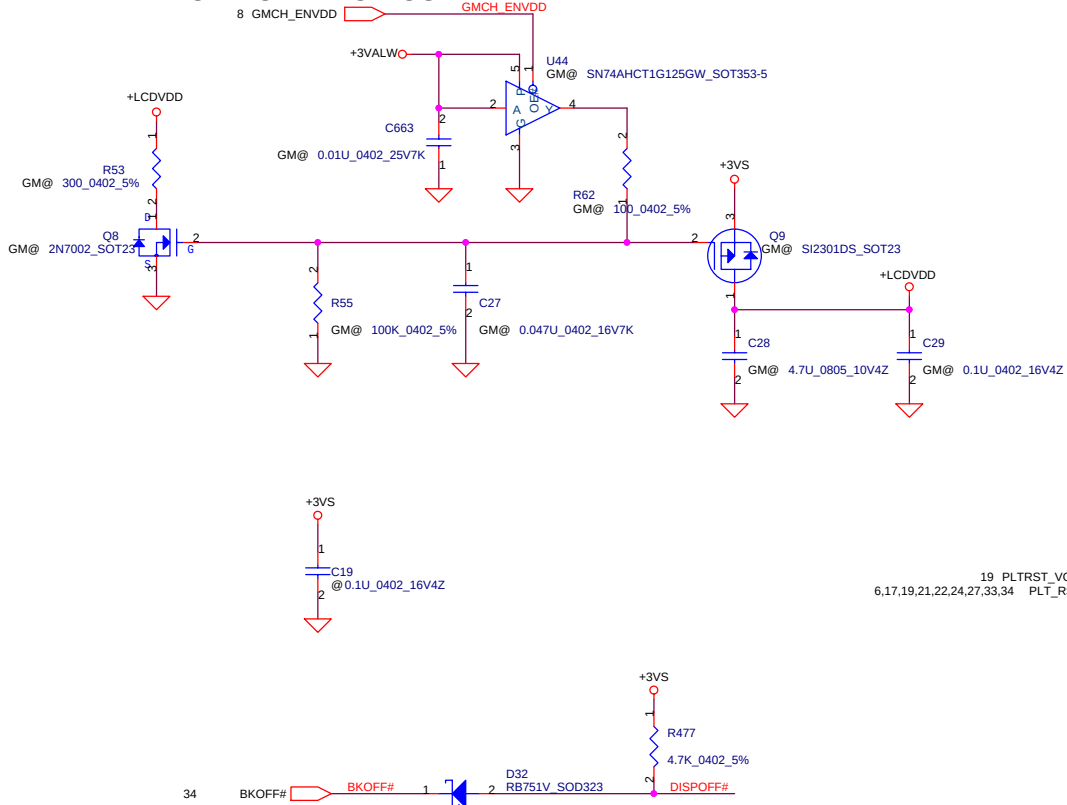
Legend:

- 1. Y ground
- 2. C ground
- 3. Y (luminance+sync)
- 4. C (chrominance)

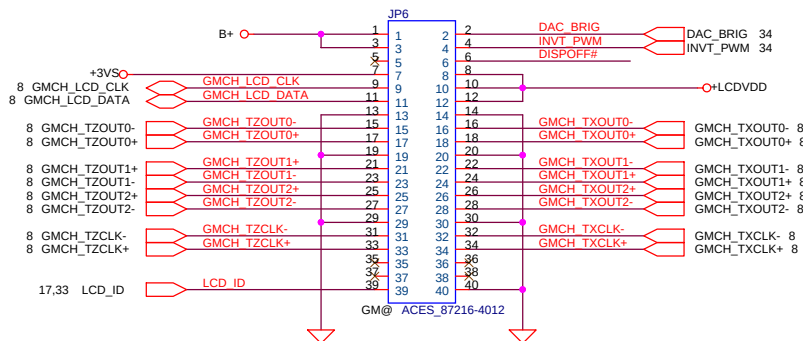
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CRT & TVout Connector
Sakhir LA-2491
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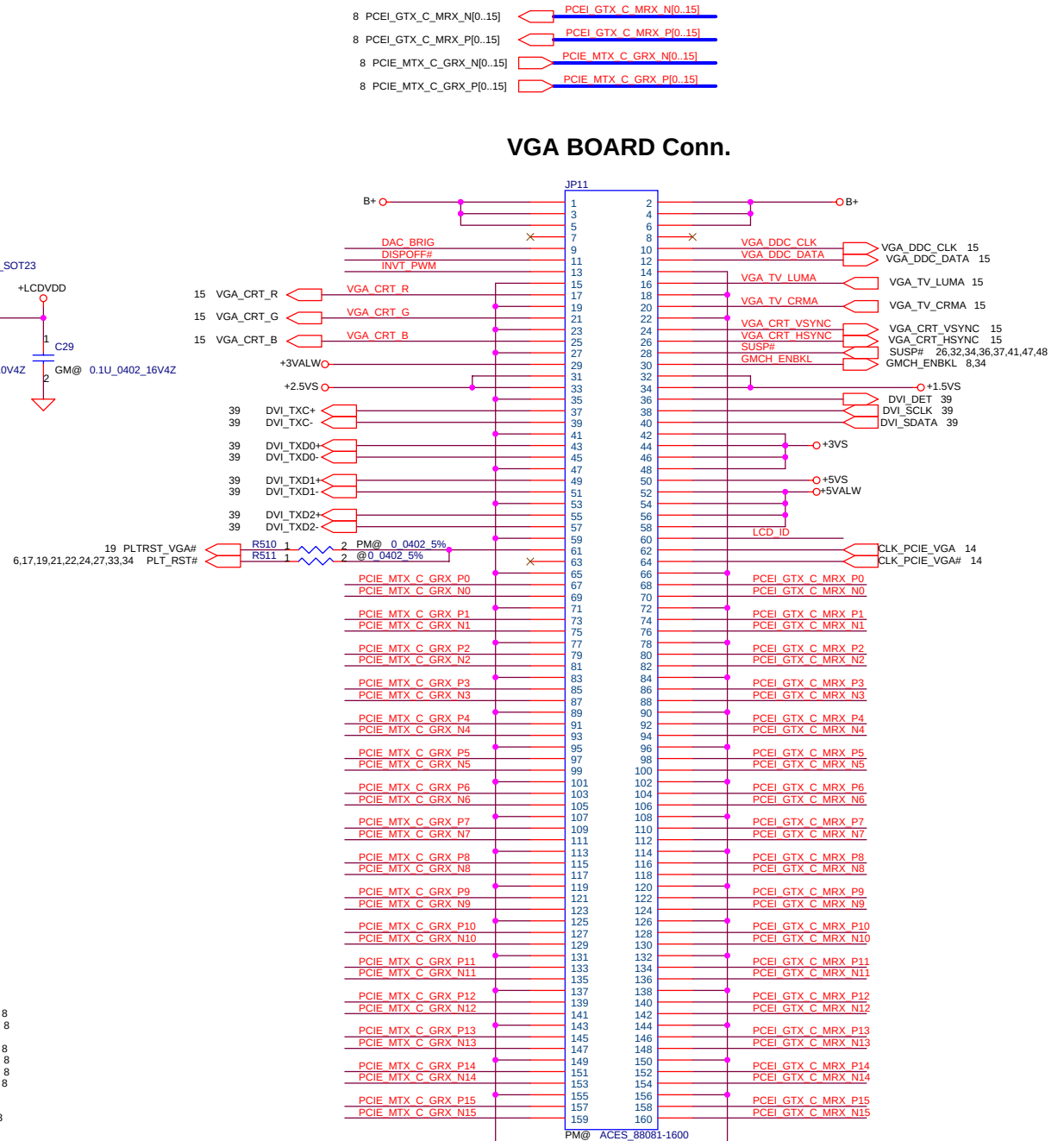
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.

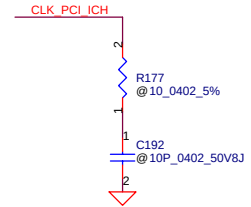
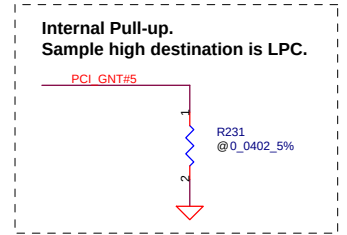
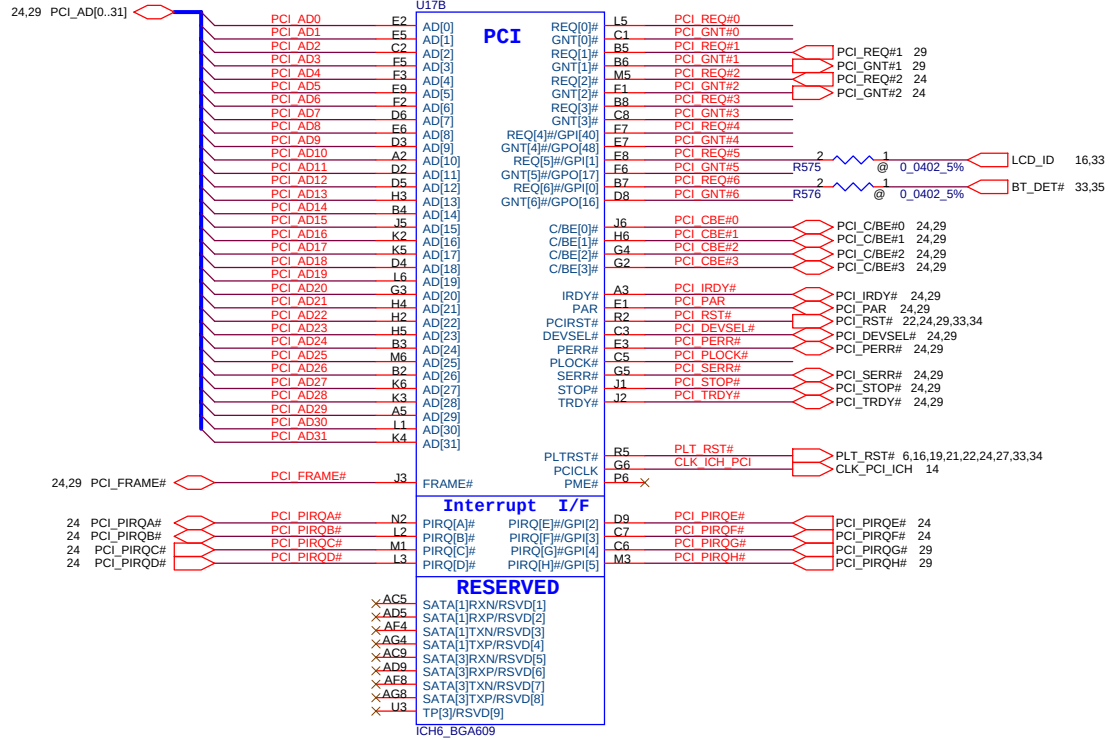
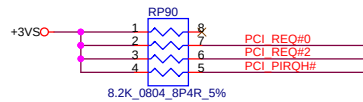
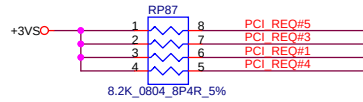
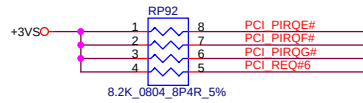
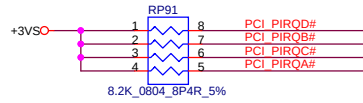
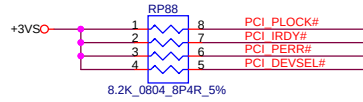
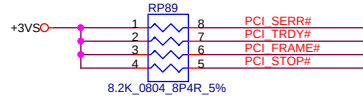


VGA BOARD Conn.

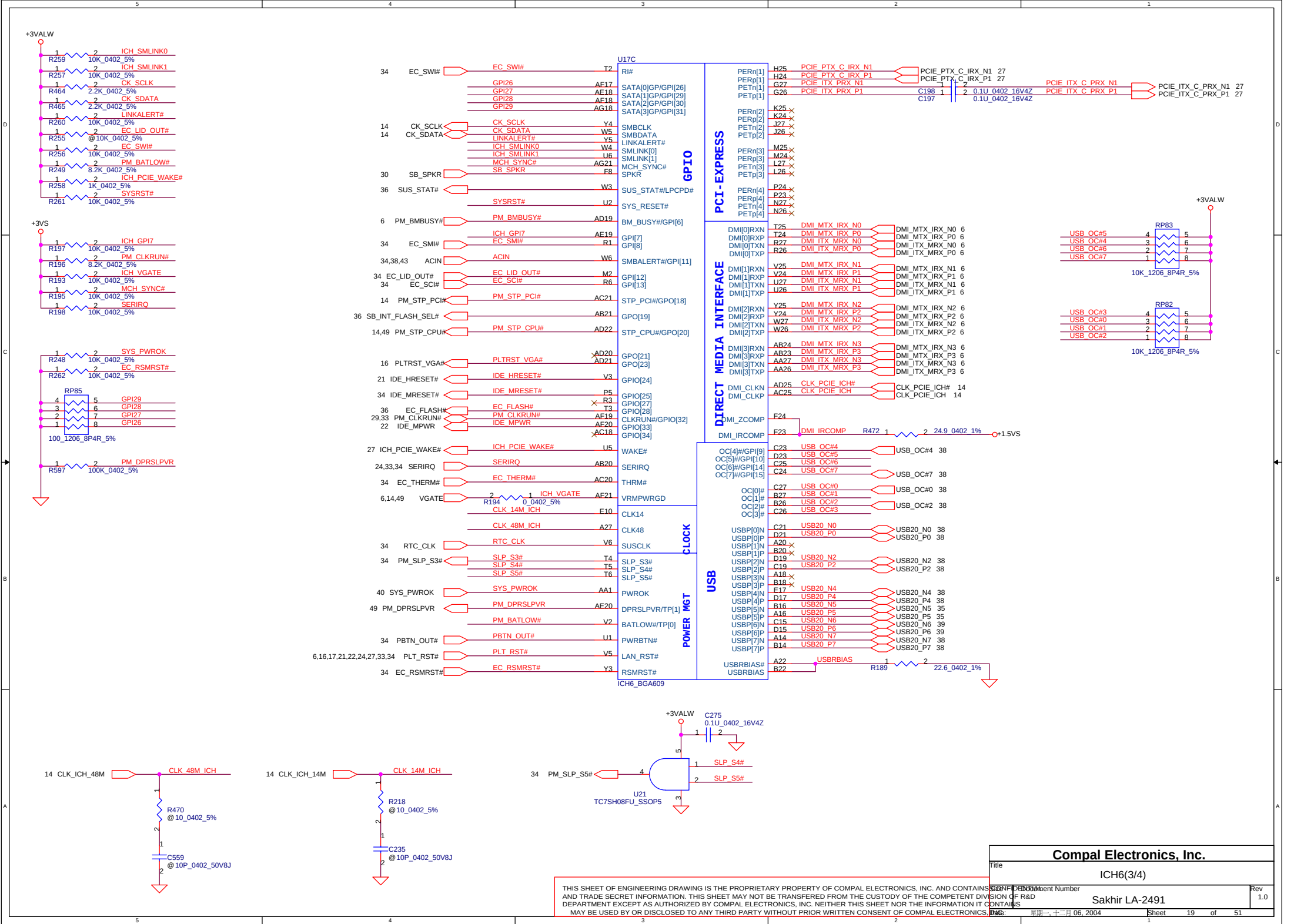


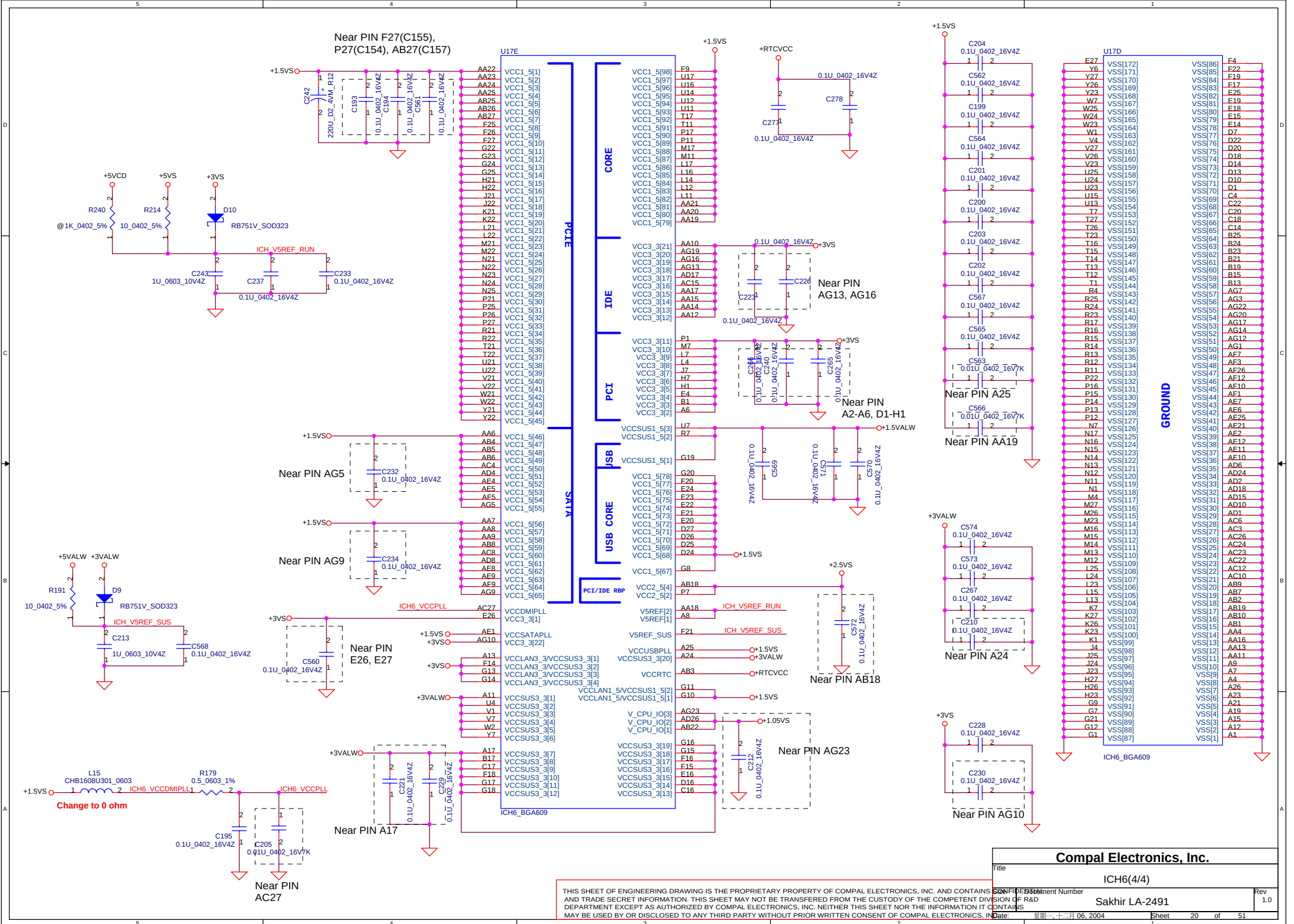
Compal Electronics, Inc.	
Title	VGA / LCD CONN.
Rev	1.0
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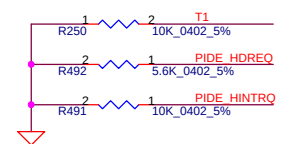
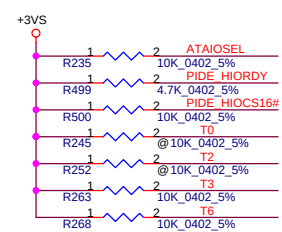
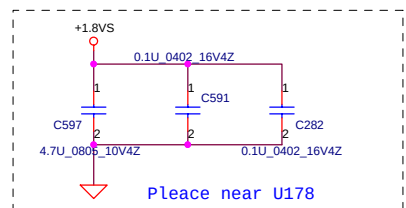
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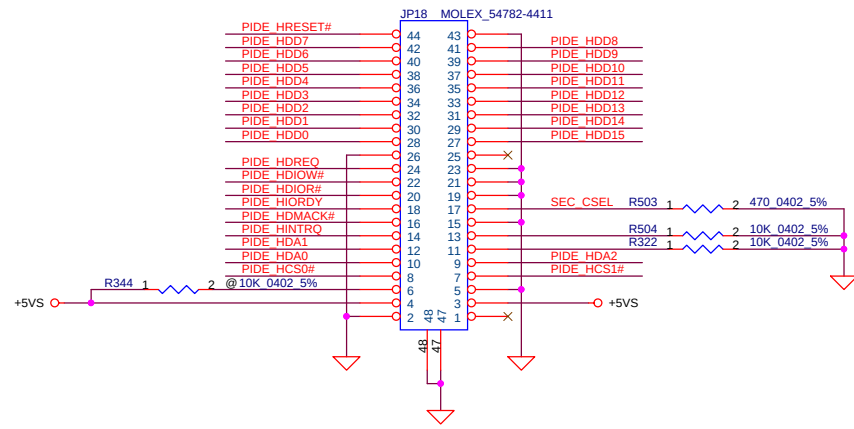
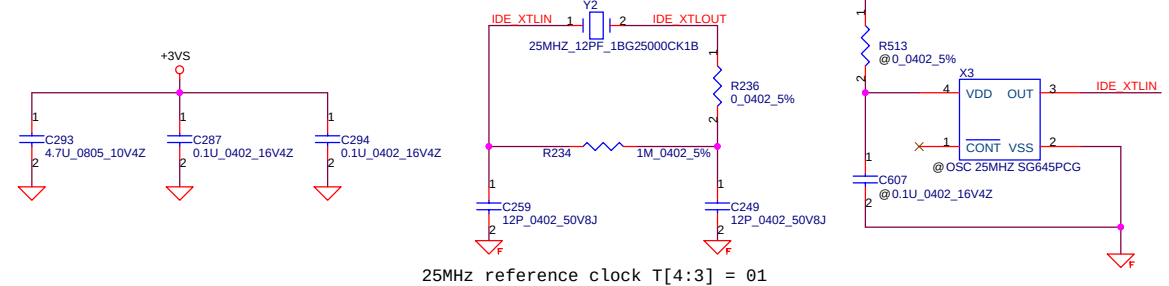
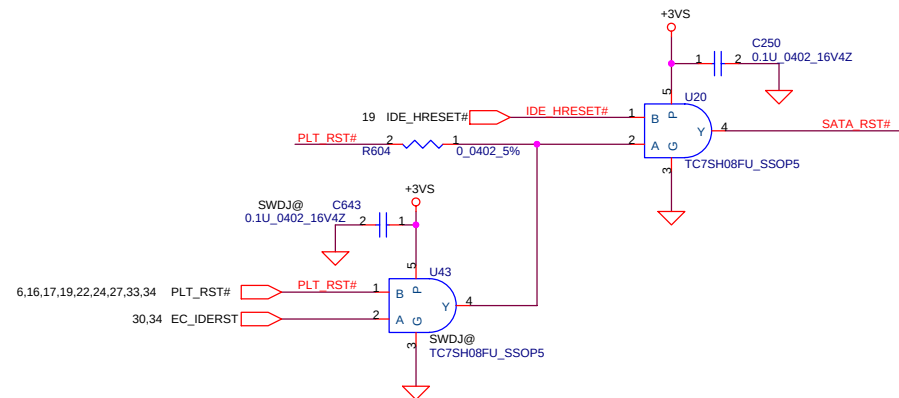
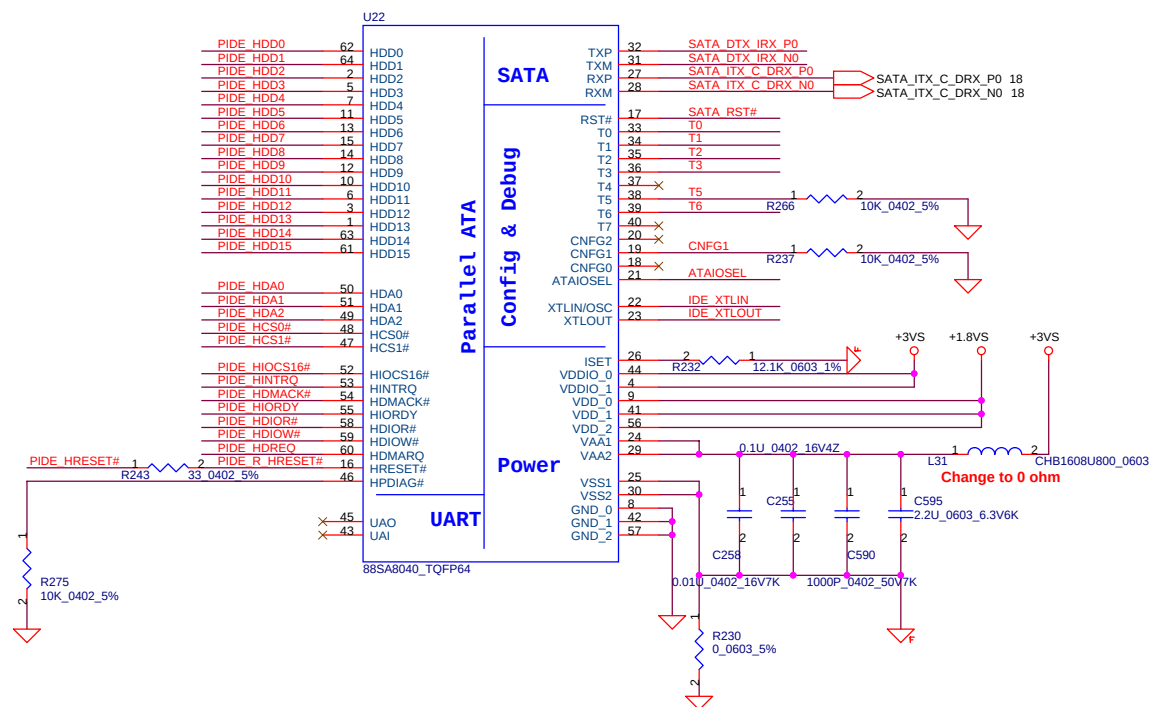
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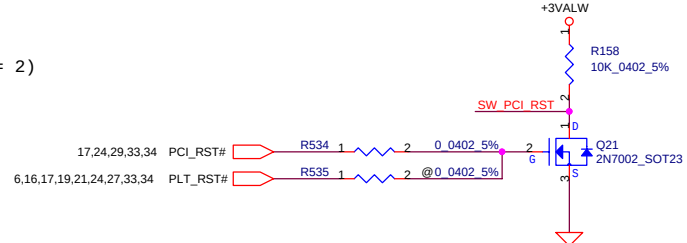
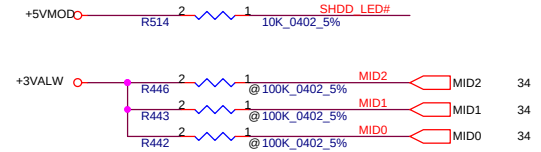
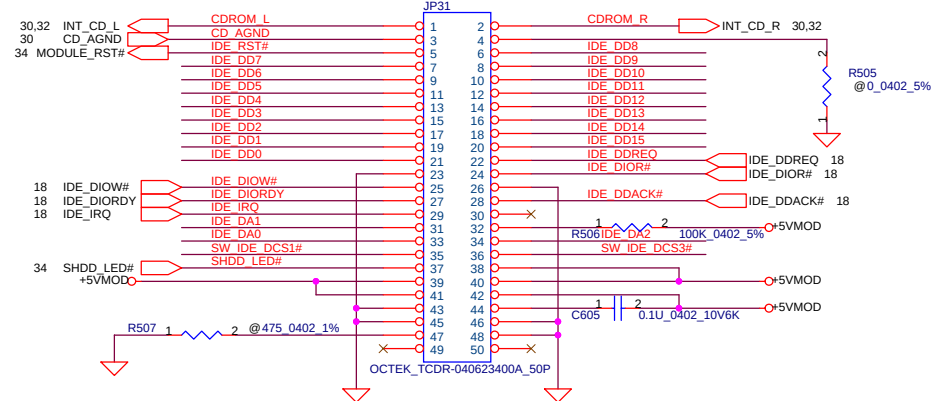
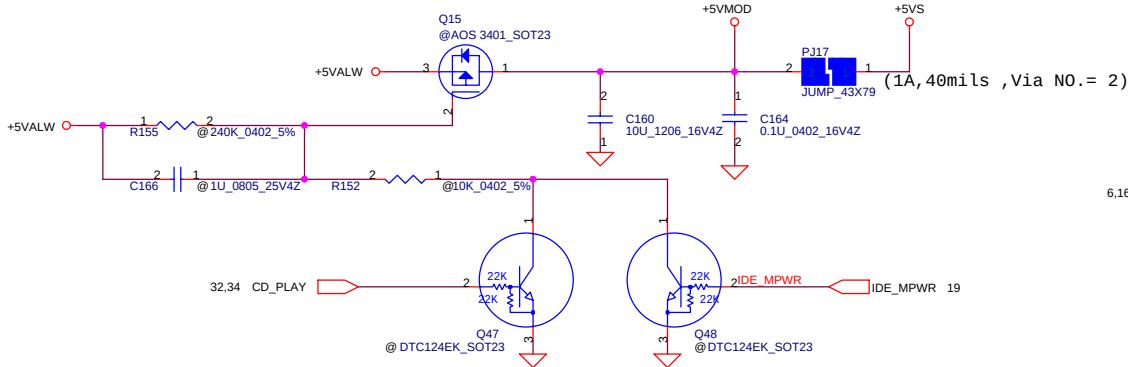
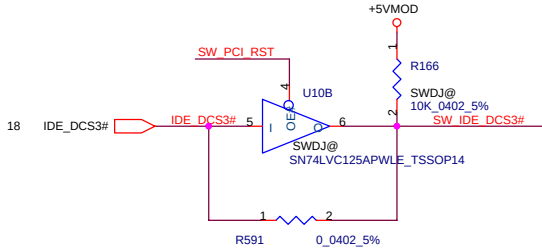
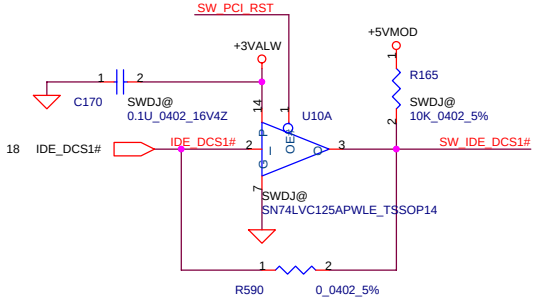
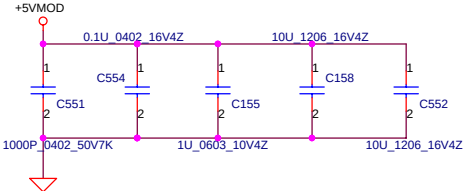




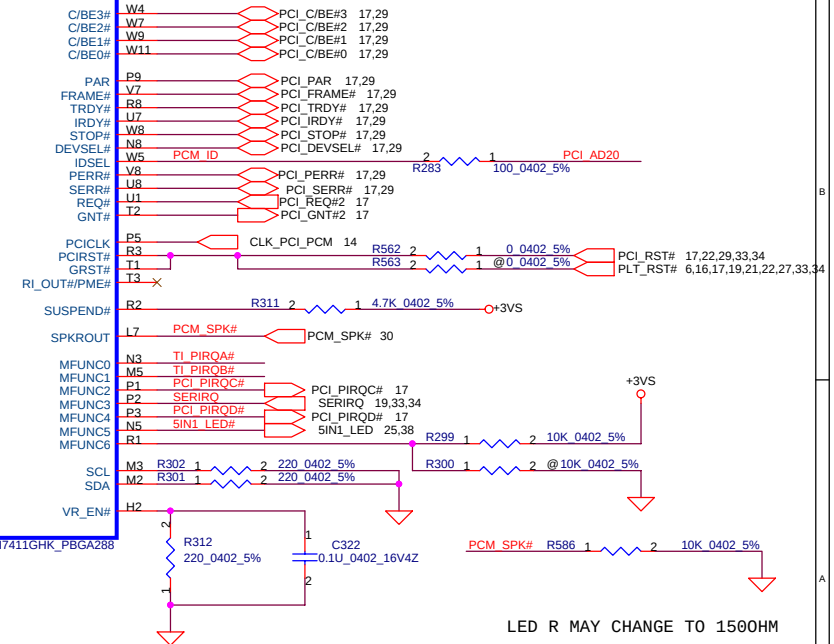
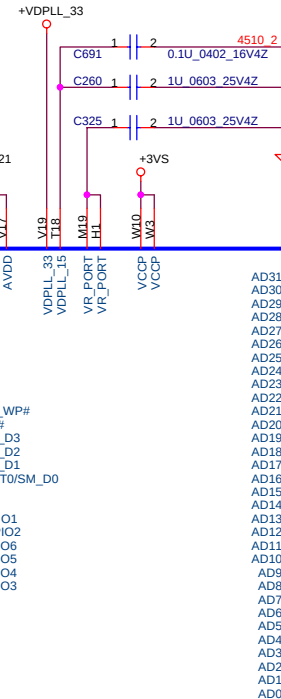
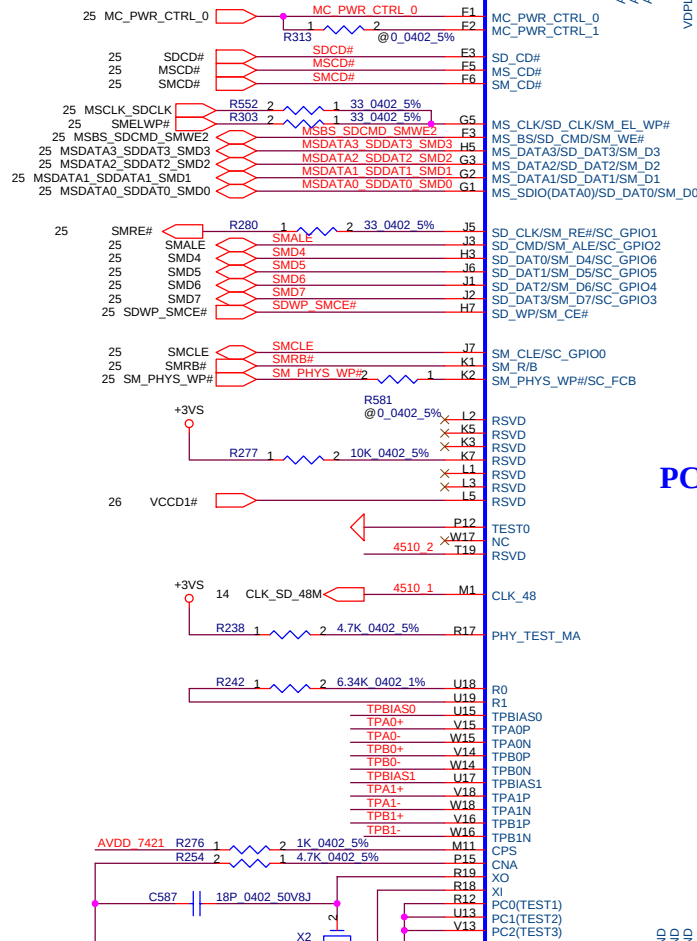
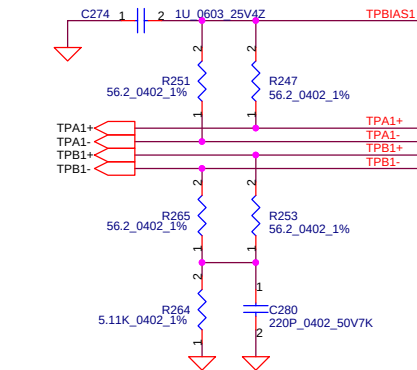
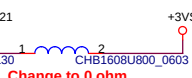
CNF62 INT PD	CNF61	CNF60 INT PD	NOTE
0	0	0	Device Mode 100MB/s
0	0	1	Device Mode 133MB/s
0	1	0	Device Mode 150MB/s
1	0	0	Host Mode 100MB/s
1	0	1	Host Mode 133MB/s
1	1	0	Host Mode 150MB/s
0	1	1	Reserved
1	1	1	Reserved



Place caps. near ODD CONN.



Module Conn.

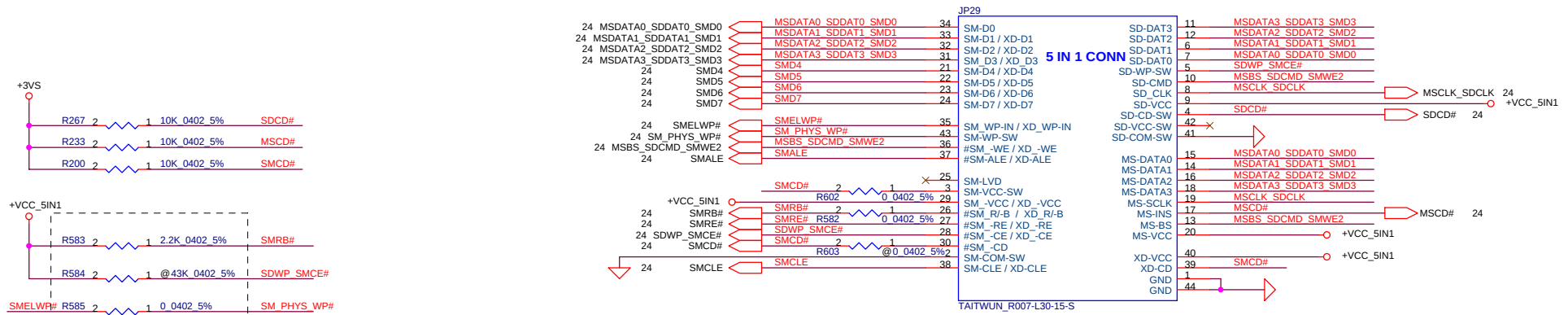


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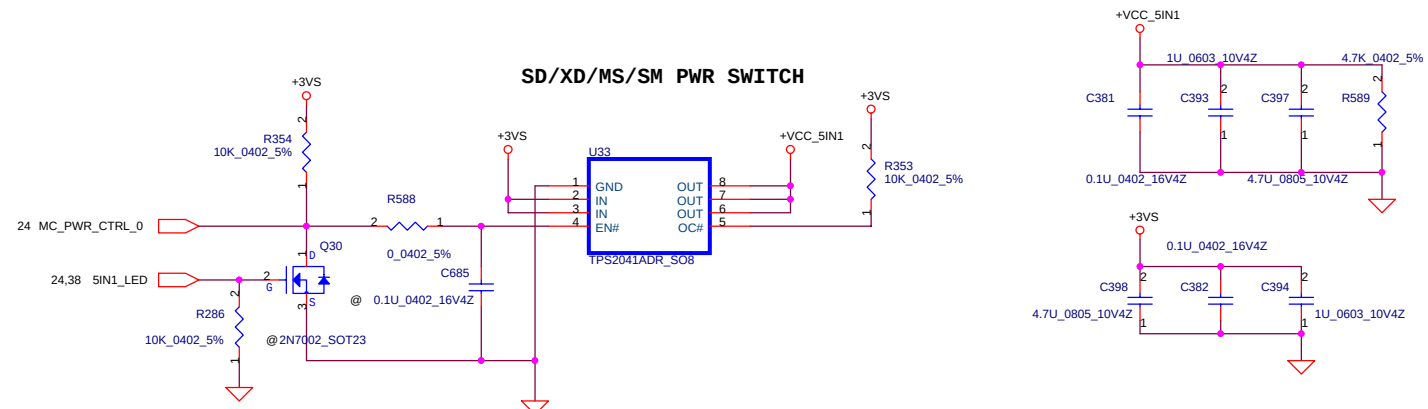
Title		PCI7421(2/2)	
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5 in 1 CardReader Conn.



TI Workaround need check



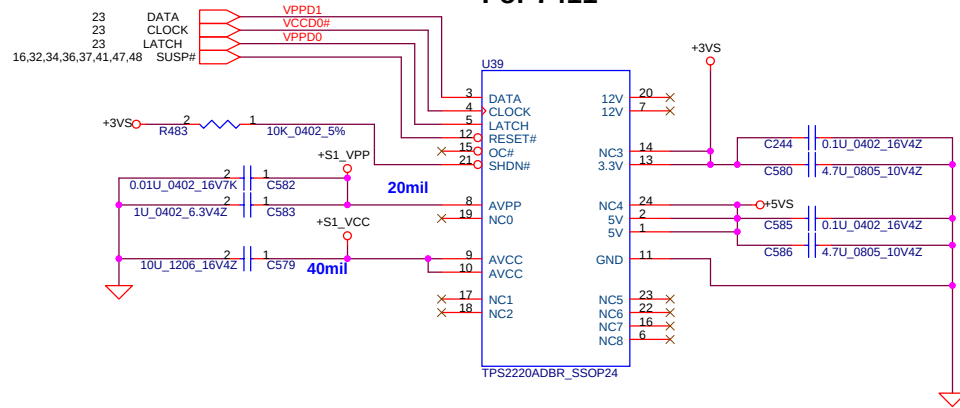
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Title	5 IN 1 Stocket
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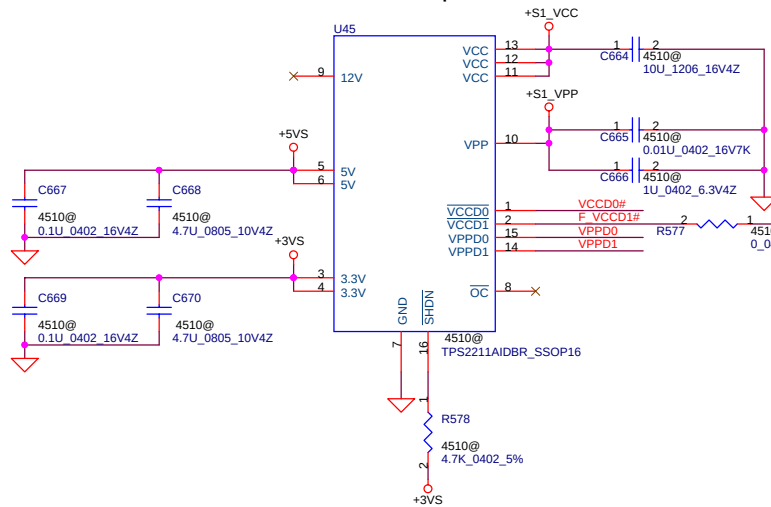
Power Switch for PCMCIA

For 7411

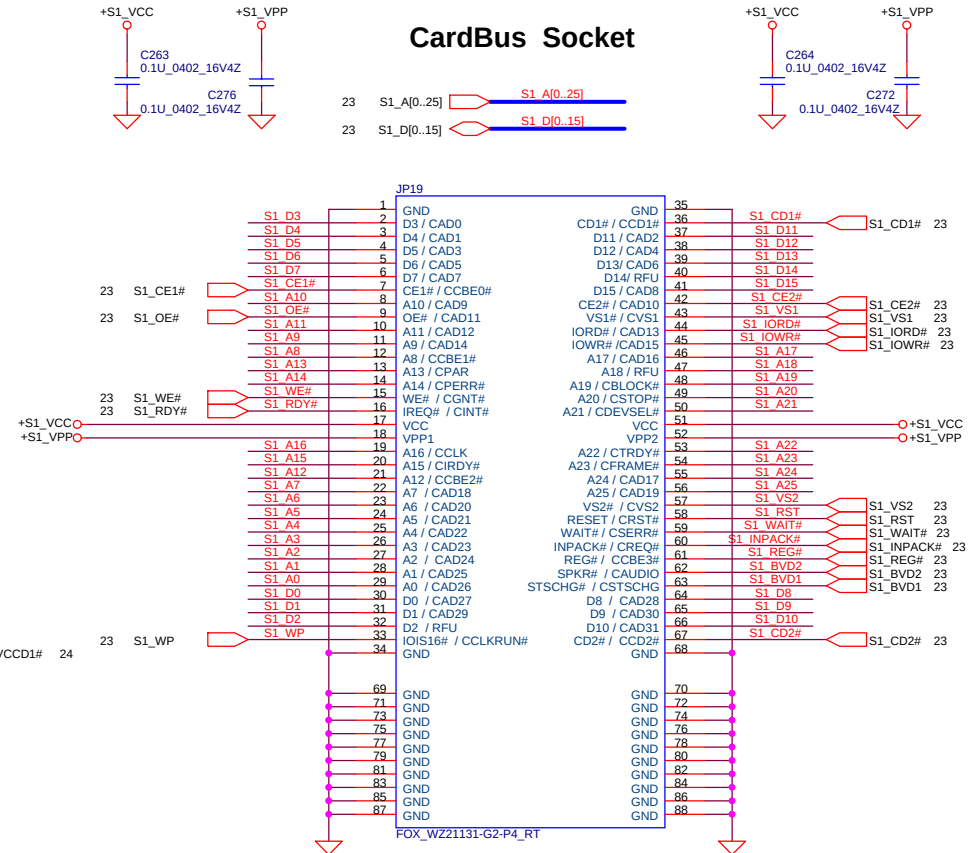


For 4510

use U4 footprint



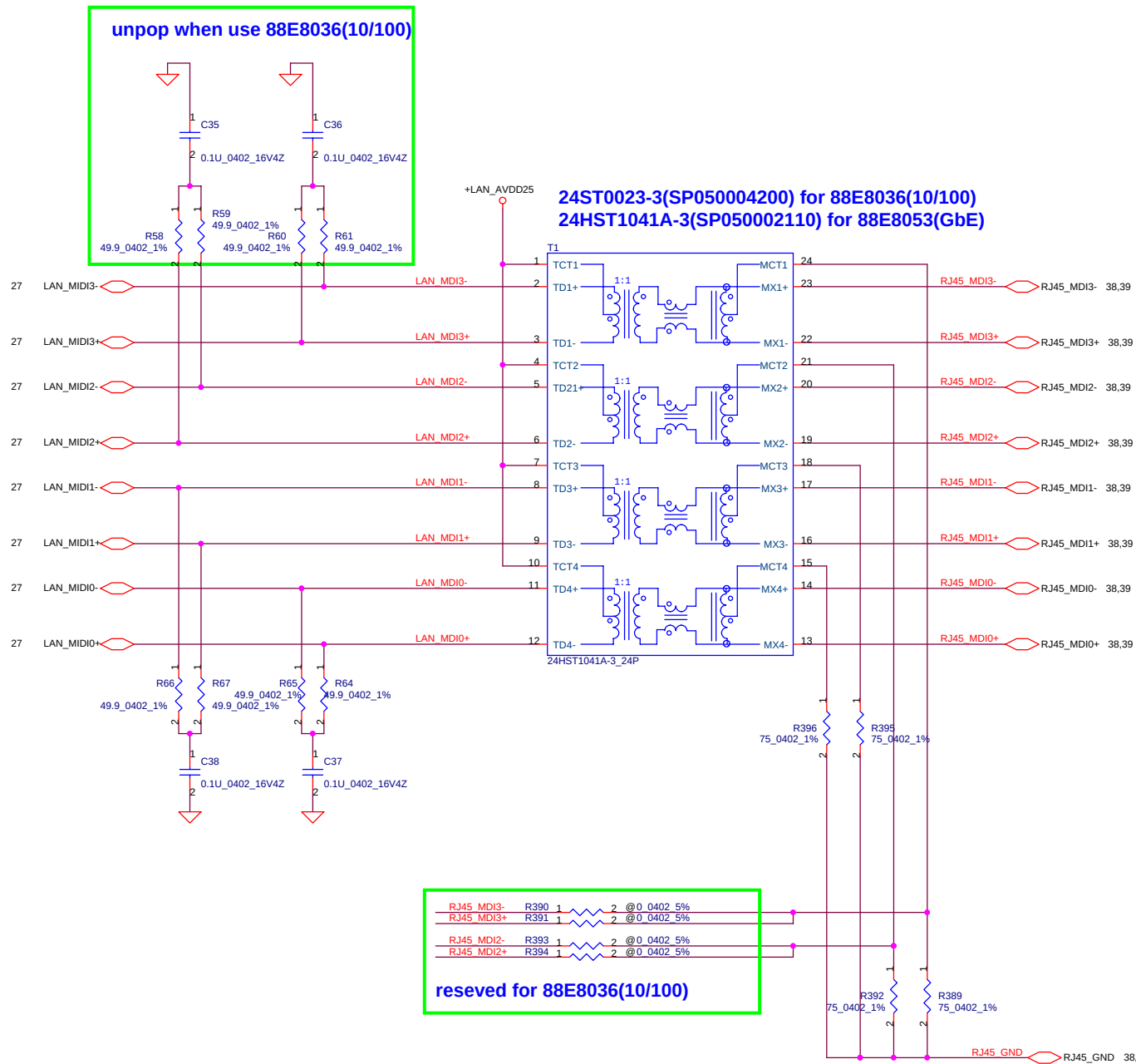
CardBus Socket



Compal Electronics, Inc.

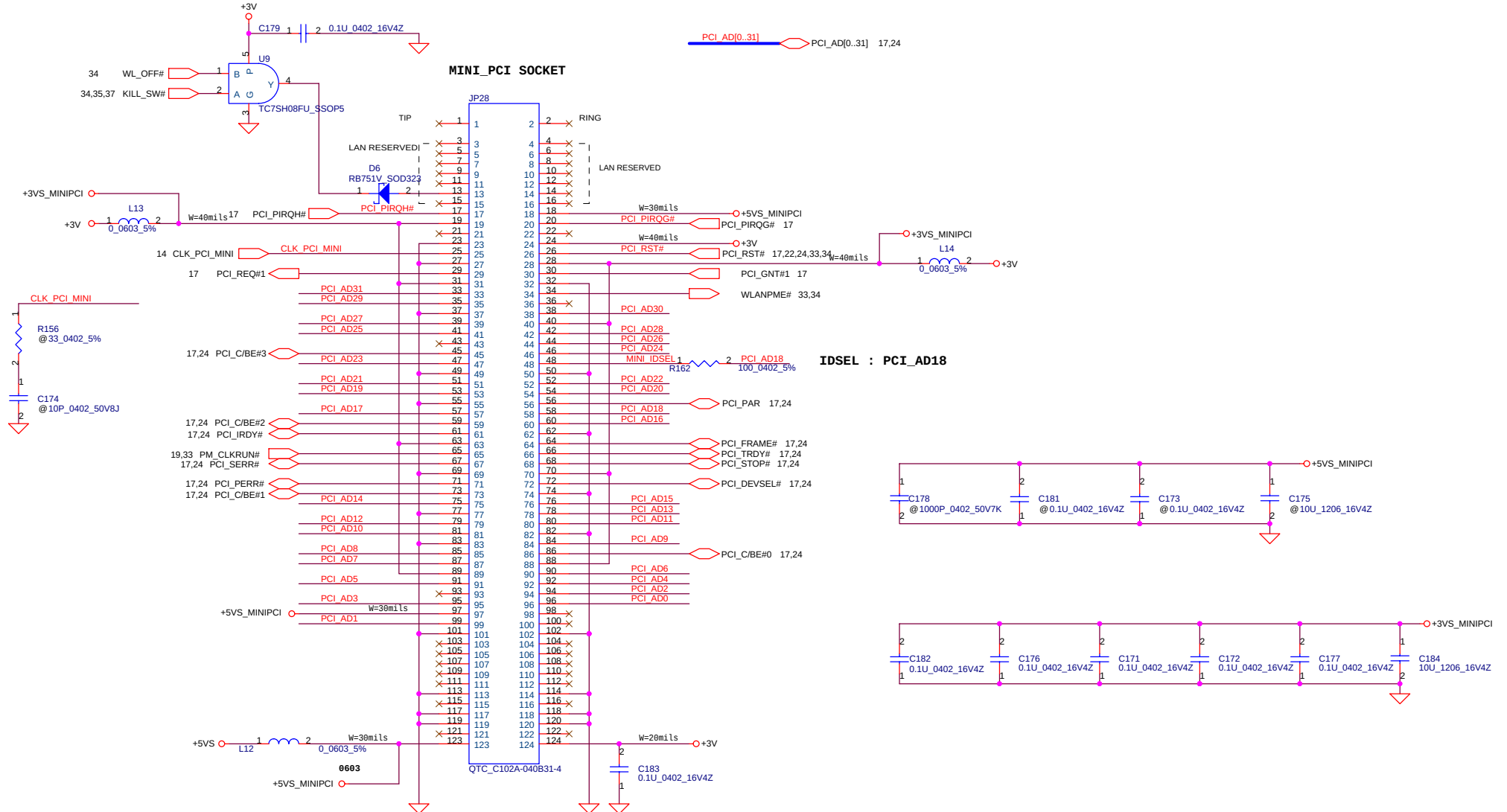
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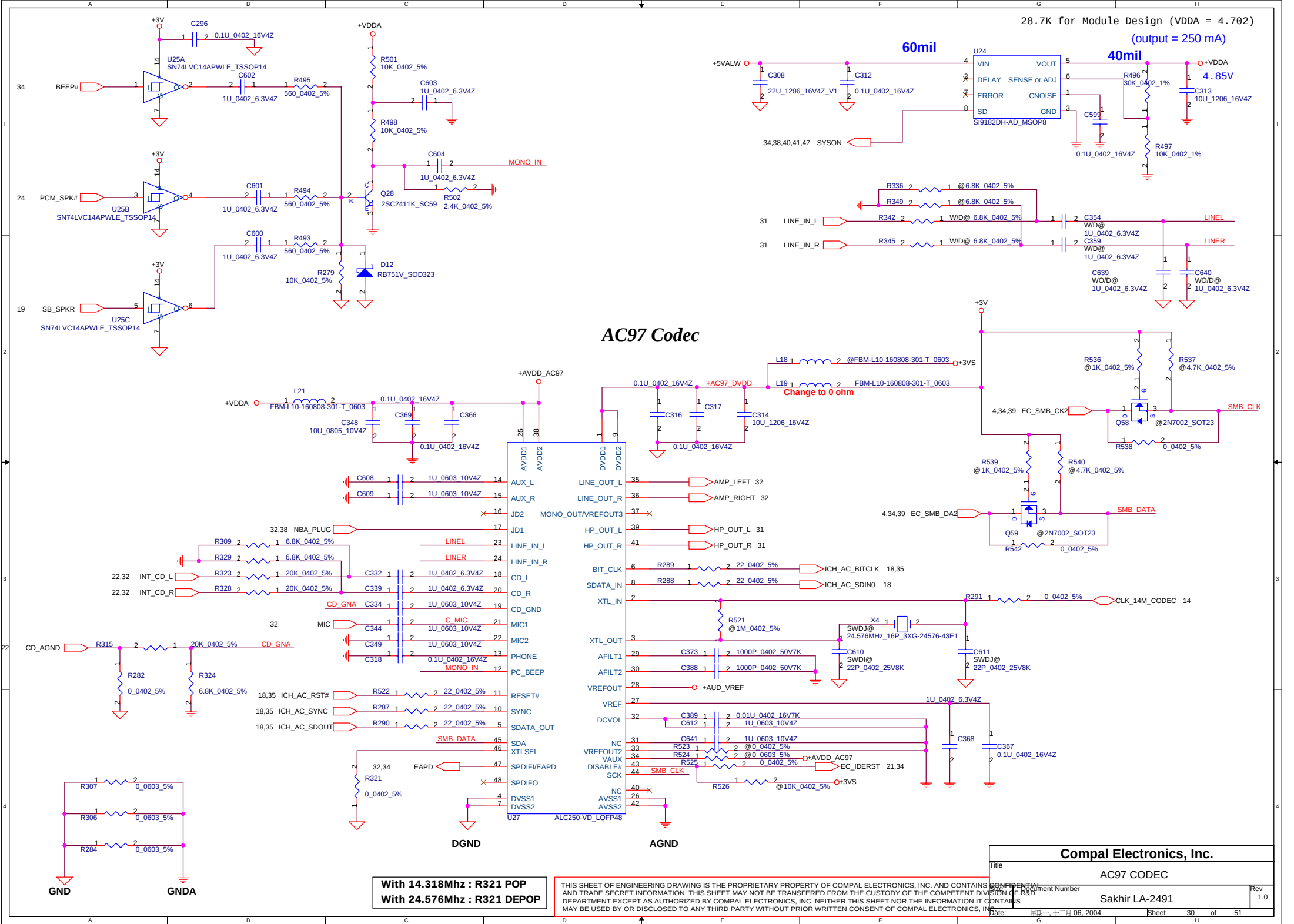
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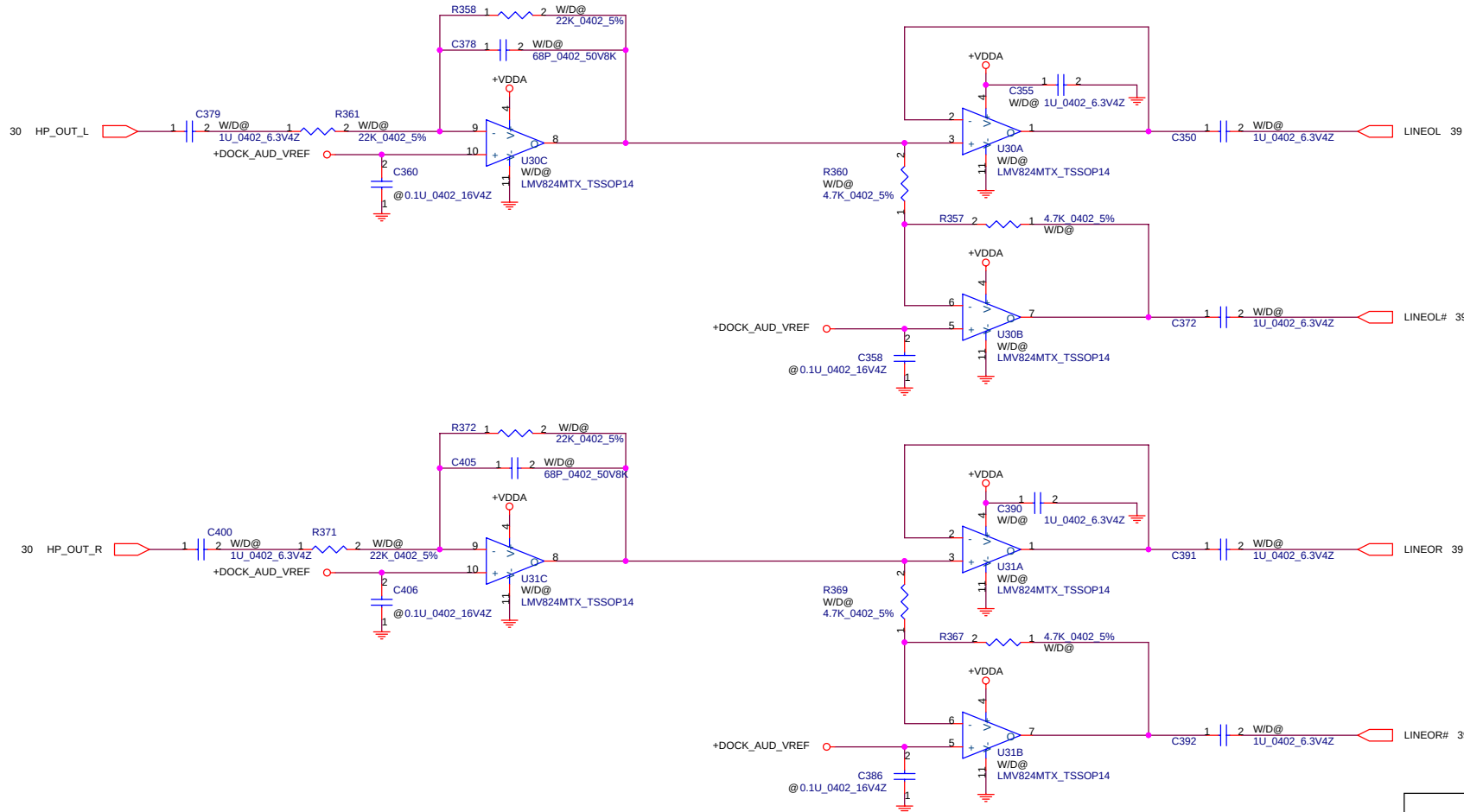
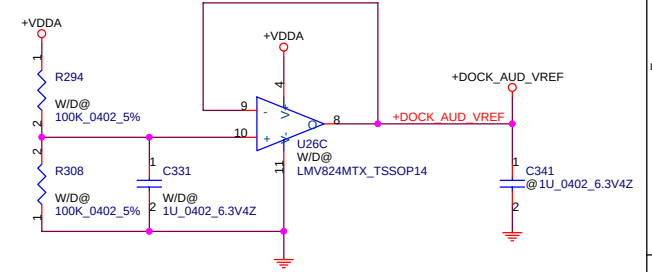
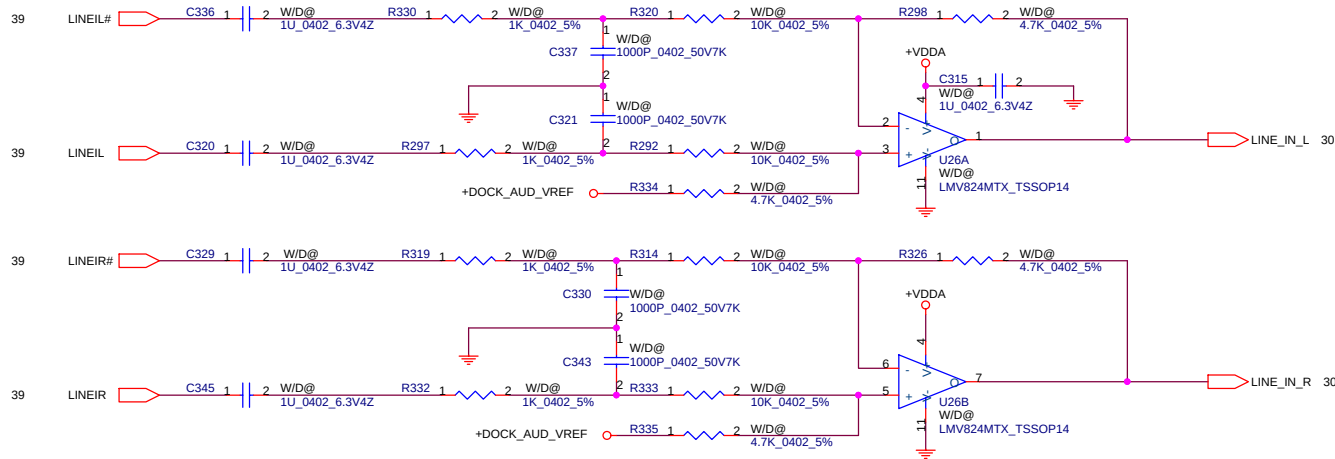


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Title	LAN Conn.		
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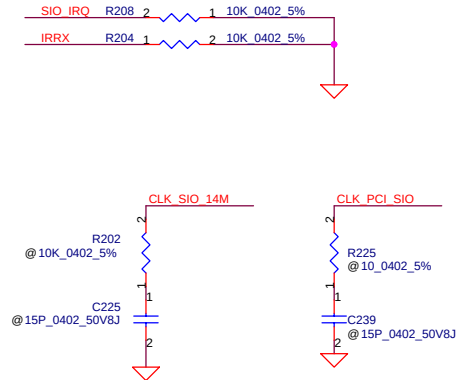
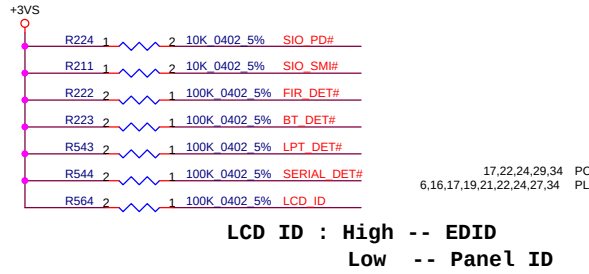




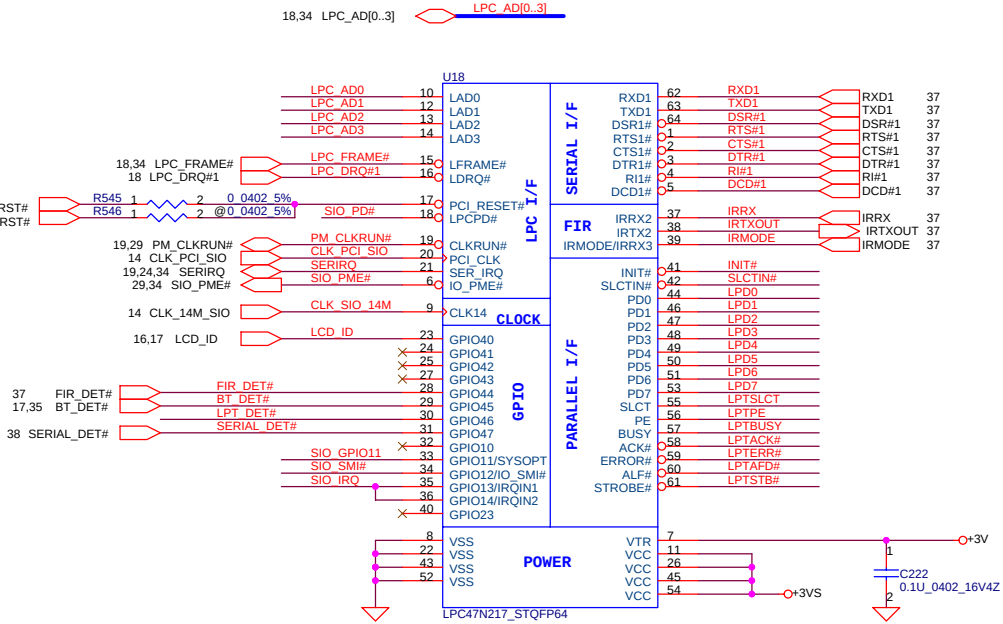
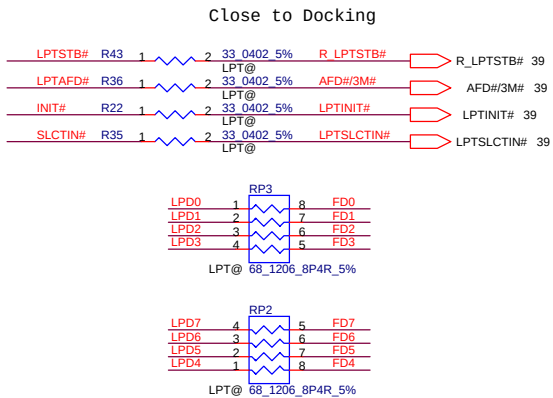
Compal Electronics, Inc.			
Title		Docking Audio	
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SUPER I/O SMsC LPC47N217

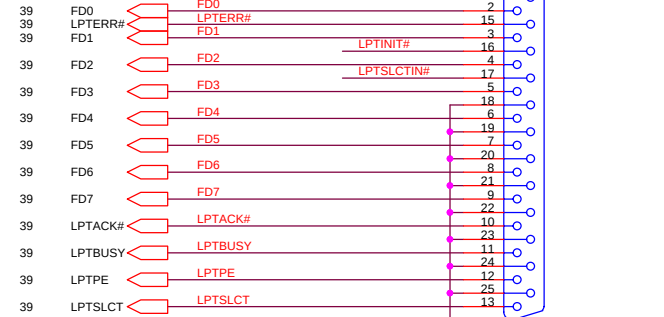
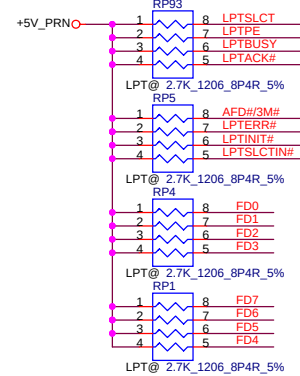
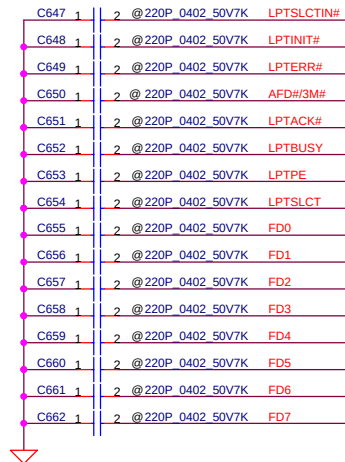
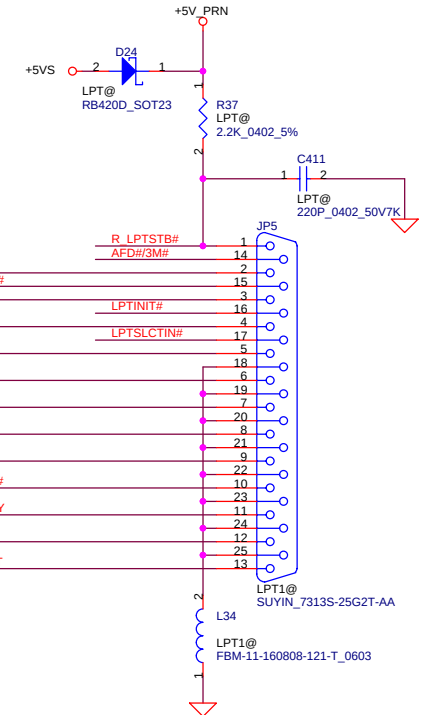
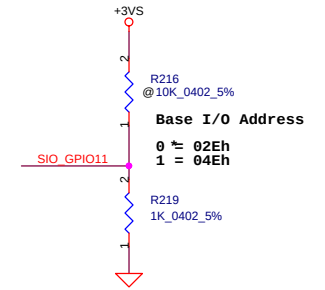
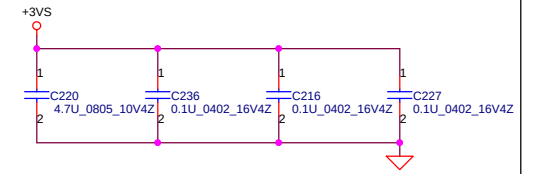
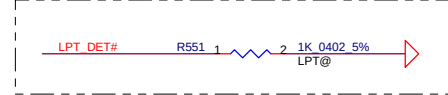


No Docking and Parallel Port ----->Del



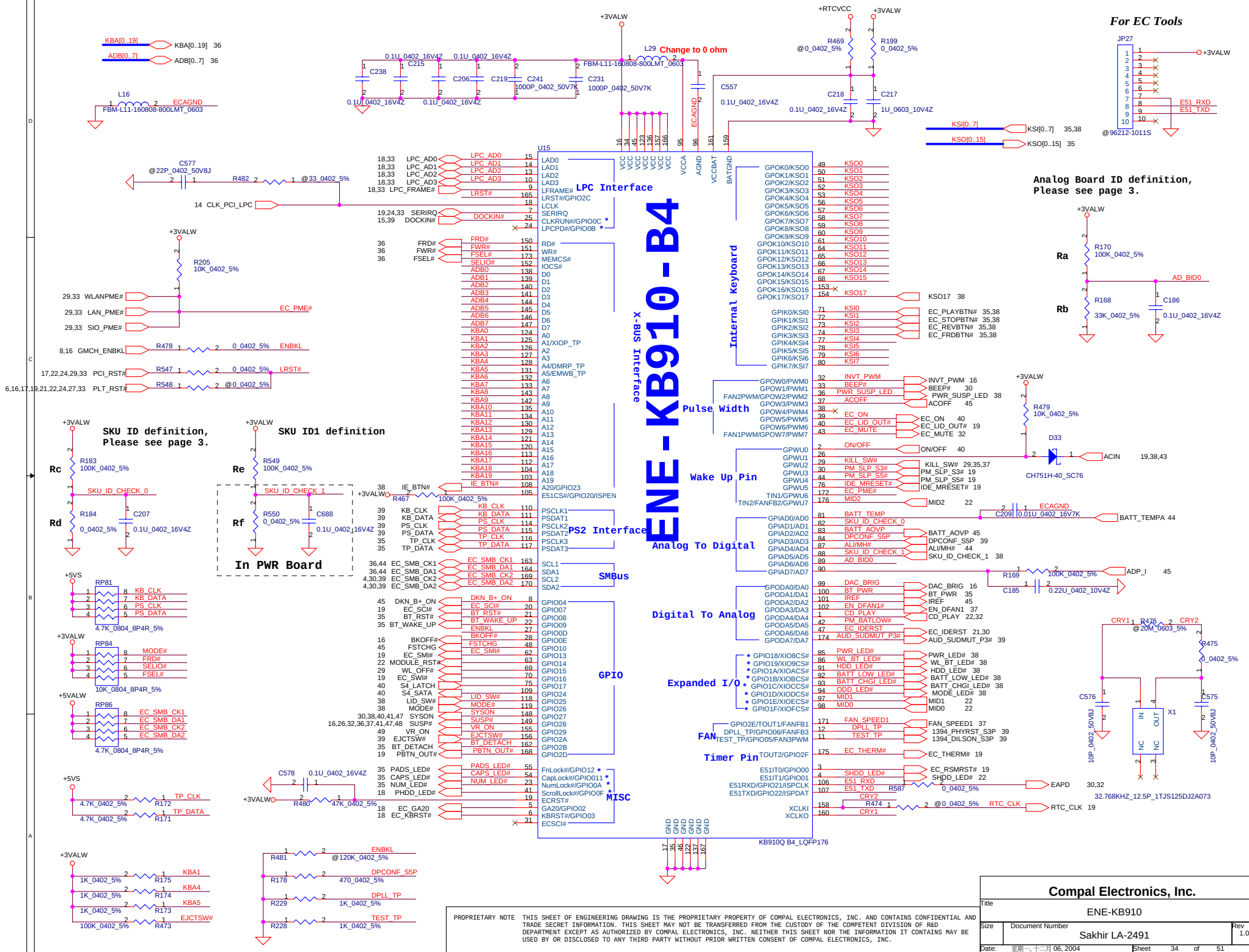
Parallel Port

LPT Module L: R POP LPT Enable
 H: R De-POP LPT Disable



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For EC Tools

Analog Board ID definition, Please see page 3.

SKU ID definition, Please see page 3.

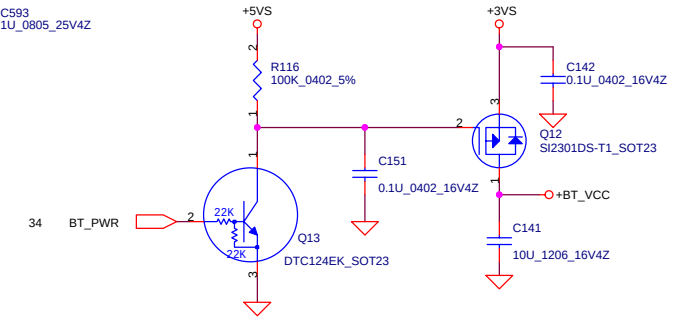
SKU ID1 definition

In PWR Board

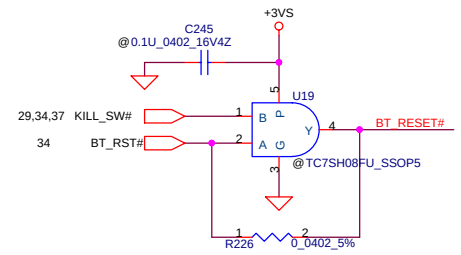
Compal Electronics, Inc.				
ENE-KB910				
Title	Document Number	Sakhir LA-2491		Rev 1.0
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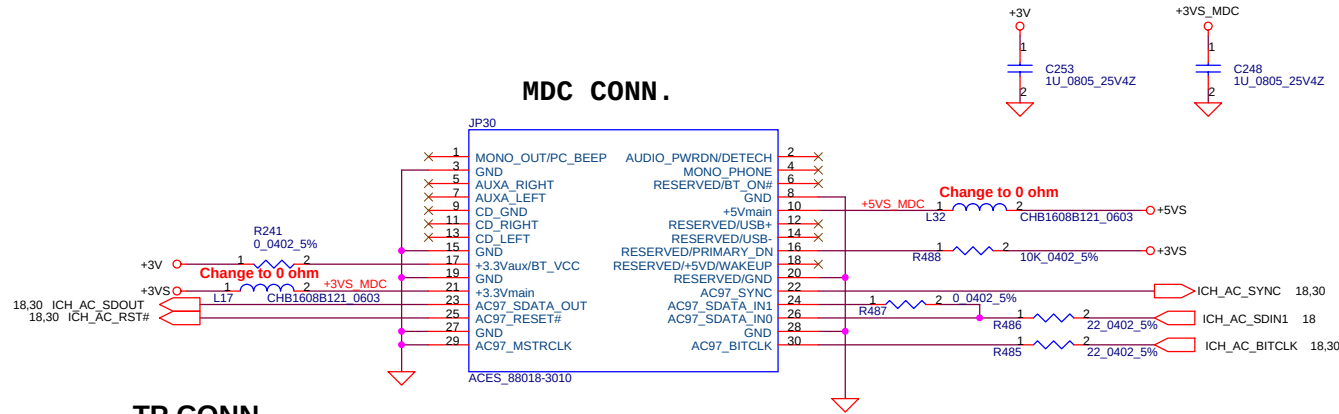
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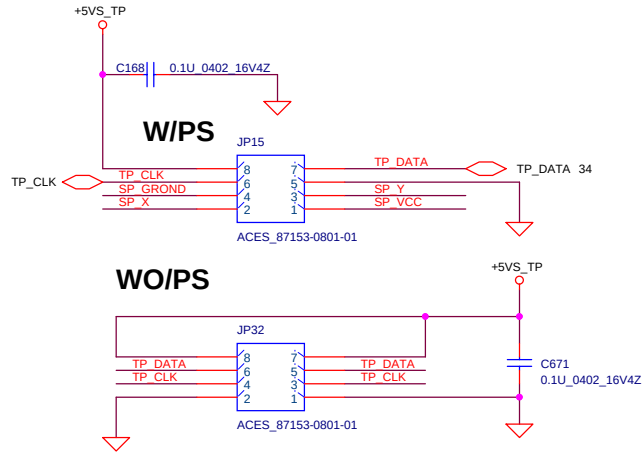
Module ID
Indication for polarity of reset
Reset input High Active -> Low
Reset input Low Active -> Open



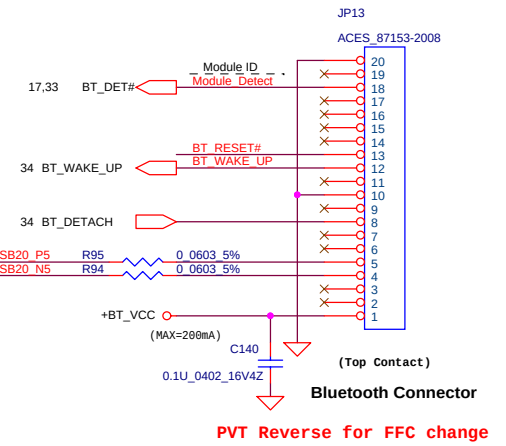
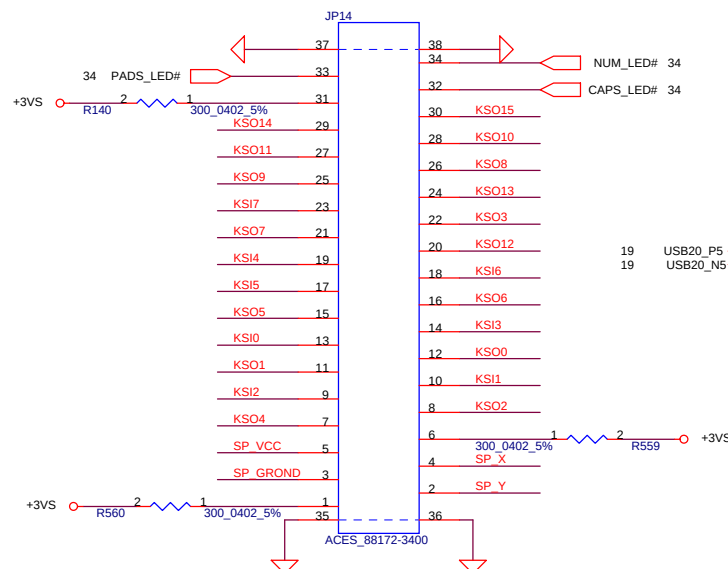
MDC CONN.



TP CONN.



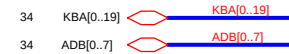
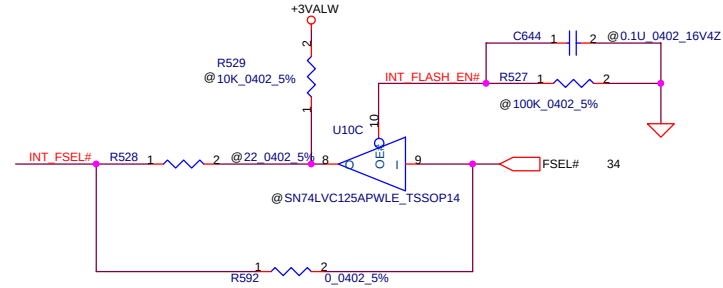
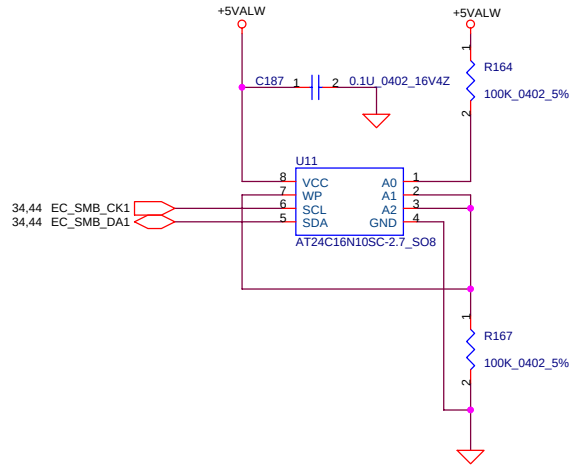
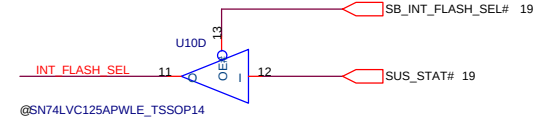
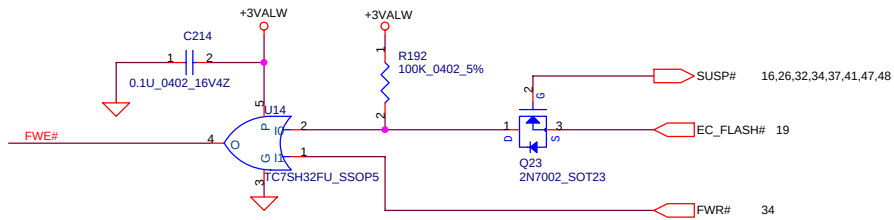
INT_KBD CONN.



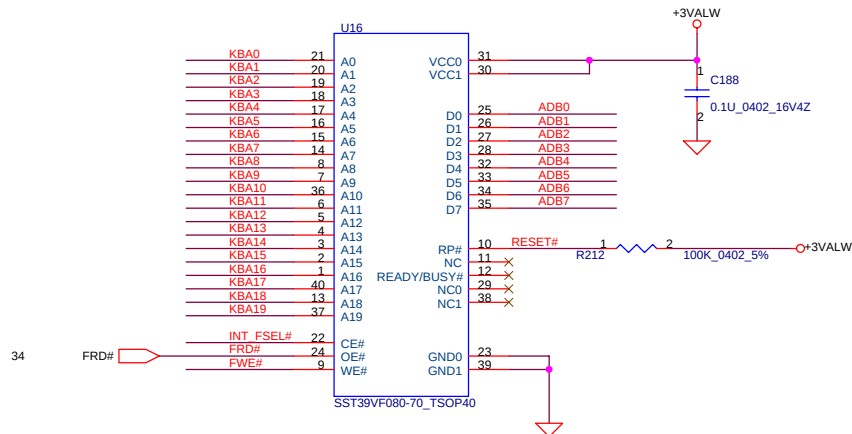
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MDC / BT / KBD / TP		
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Date	星期一, 十二月 06, 2004	Sheet 35 of 51

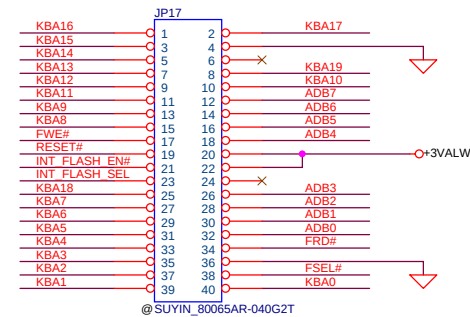
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1MB Flash ROM



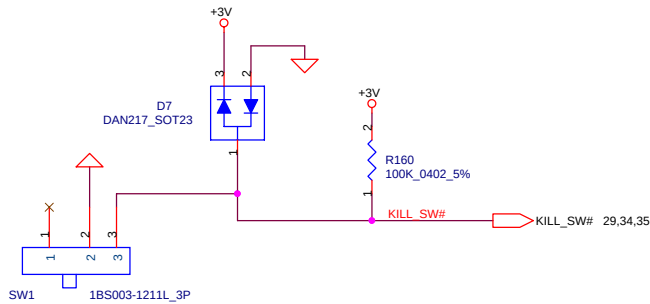
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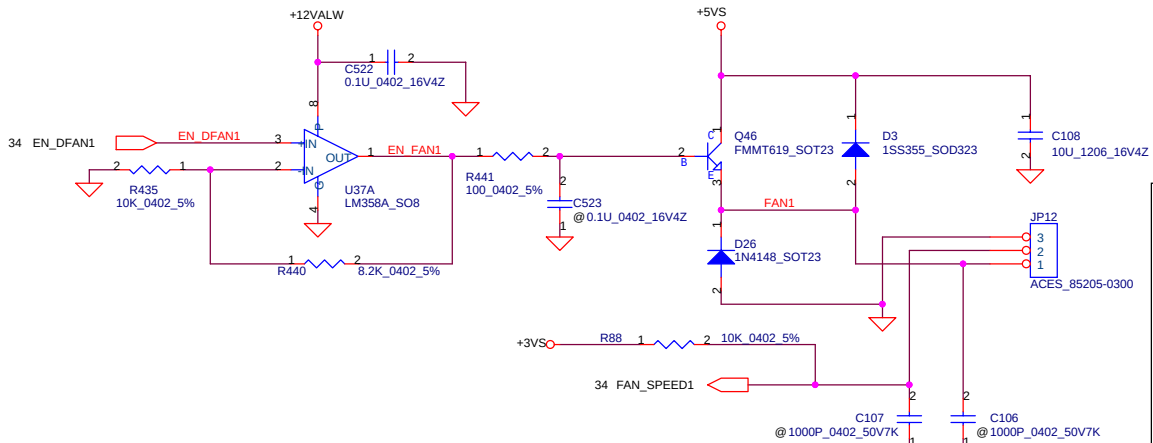
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Title		BIOS & EXT. I/O PORT	
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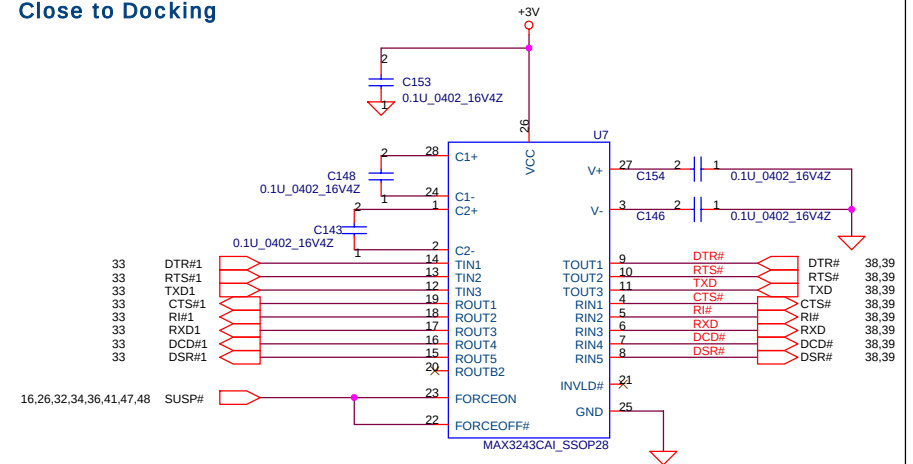
Kill SWITCH



FAN Conn



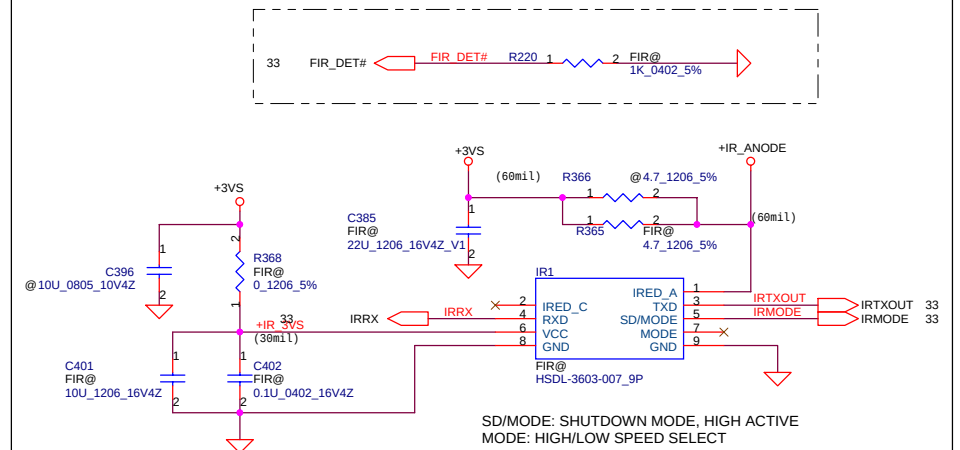
Close to Docking



No Docking and Serial Port ----->Del

FIR Module

L: R POP; FIR Enable
H: R De-POPFIR Disable



Compal Electronics, Inc.

FAN1 / FIR / Kill

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R3457 Serial Board Conn.

Pinout diagram for the R3457 Serial Board Conn. showing connections for USB20, DTR, RTS, TXD, CTS, RI#, RXD, DCD#, DSR#, USB_OC#7, SERIAL_DET#, LAN_ACTIVITY#, LAN_LINK#, R345_GND, R345_MDI3+, R345_MDI3-, R345_MDI2+, R345_MDI2-, R345_GND, R345_MDI1+, R345_MDI1-, R345_GND, R345_MDI0+, and R345_MDI0-.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
19	USB20_N7	30	USB20_N7	15	LAN_ACTIVITY#	27	LAN_ACTIVITY#
19	USB20_P7	29	USB20_P7	14	LAN_LINK#	27	LAN_LINK#
37	DTR#	28	DTR#	13			
37	RTS#	27	RTS#	12	R345_GND	28	R345_GND
37	TXD	26	TXD	11	R345_MDI3+	28	R345_MDI3+
37	CTS#	25	CTS#	10	R345_MDI3-	28	R345_MDI3-
37	RI#	24	RI#	9	R345_GND	28	R345_GND
37	RXD	23	RXD	8	R345_MDI2+	28	R345_MDI2+
37	DCD#	22	DCD#	7	R345_MDI2-	28	R345_MDI2-
37	DSR#	21	DSR#	6	R345_GND	28	R345_GND
19	USB_OC#7	20	USB_OC#7	5	R345_MDI1+	28	R345_MDI1+
33	SERIAL_DET#	19		4	R345_MDI1-	28	R345_MDI1-
		18		3	R345_GND	28	R345_GND
		17		2	R345_MDI0+	28	R345_MDI0+
		16		1	R345_MDI0-	28	R345_MDI0-

ACES_87216-3002

[illegible]

Timing diagram for PWR_SUSPLD_1# showing a transition from high to low at D35, labeled HT-191UD_AMBER_0603.

The diagram shows the AC IN LED circuit. It starts with a +5VALW supply connected to a resistor R364. The other end of R364 is connected to the anode of a blue LED D18 (HT-191NB_BLUE_0603). The cathode of D18 is connected to the anode of a MOSFET Q40 (2N7002_SOT23). The gate of Q40 is connected to the ACIN signal. The drain of Q40 is connected to the +5VALW supply, and the source is connected to ground. The LED is labeled AC IN LED.

Schematic diagram of the BATT_LOWLED# and BATT_CHGLED# signals. A +5VALW supply is connected to a network of resistors (R374, R561) and capacitors (120_0402, 5%) leading to a D16 decoder. The decoder outputs are connected to BATT_LOWLED# (pin 1) and BATT_CHGLED# (pin 4). The component HT-297UD/NB_BLUE/AMB_0603 is noted.

HDD LED

5V

R375

1

2

120_0402_5%

D20

HT-191NB BLUE 0603

HDD_LED# 34

MODE

+5VS

R376

1 2

@120_0402_5%

D19

@HT-191NB_BLUE_0603

1

MODE_LED# 34

47 +3VALW

R370 1 2 300_0402_5% 2 1 D15 HT-110UD_1204 WL_BT_LED# 34

The diagram shows the pin configuration for the ACES_87216-3002 component. The pins are numbered 1 through 30. The connections are as follows:

- +5VALW**: Connected to Pin 1.
- JP16**: A header connector spanning pins 1 through 15.
- SYSON#**: Connected to Pin 6.
- USB_OC#0**: Connected to Pin 8.
- USB_OC#2**: Connected to Pin 9.
- USB_OC#4**: Connected to Pin 10.
- NBA_PLUG**: Connected to Pin 11.
- VOL_AMP**: Connected to Pin 12.
- USB20_N0**: Connected to Pin 16.
- USB20_P0**: Connected to Pin 17.
- USB20_N2**: Connected to Pin 19.
- USB20_P2**: Connected to Pin 20.
- USB20_N4**: Connected to Pin 22.
- USB20_P4**: Connected to Pin 23.
- LID**: Connected to Pin 24.
- RTCTVREF**: Connected to Pin 27.
- +5VCD**: Connected to Pin 29.
- ACES_87216-3002**: The component name at the bottom.

Pin 1 connection diagram for D31 DAN202U_SC70. Pin 1 is labeled MODEBTN#. It connects to pin 2 (MODE#) and pin 3 (51ON#) of the component. Pin 2 is connected to MODE# (34) and pin 3 is connected to 51ON# (40,43). The component is labeled D31 DAN202U_SC70.

Schematic diagram of the IEBT pin connection for the DAN202U_SC70 component. The IEBT# pin (pin 1) is connected to the +3VALW supply through a 100K resistor (R531). The IE_BTN# pin (pin 3) is connected to the 510N# signal line. The component is labeled D30 DAN202U_SC70.

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The diagram illustrates the electrical connections for a docking connector, specifically focusing on the JP23A and JP23B headers. It shows a complex network of signals including power (+3VALW, +5VS), data (DKN_B+, PS_CLK, KB_CLK, DDC, CRT, DVI), and control (DOCKIN#, DOCKOUT#, DOCKIN#). The connections are organized into two main sections, JP23A and JP23B, with a central area for power and ground connections. The diagram includes labels for components like resistors (R13, R17, R574), capacitors (C11), and integrated circuits (U2, TC7SH32FU_SSOP5). It also shows signal names such as +DC_IN_S1, DKN_B+, PS_CLK, KB_CLK, and various data lines like DDC, CRT, and DVI. The diagram is organized into two main sections, JP23A and JP23B, with a central area for power and ground connections.

MDC to Docking Conn.

4

MDC1_RING

MDC2_TIP

JP2

1

2

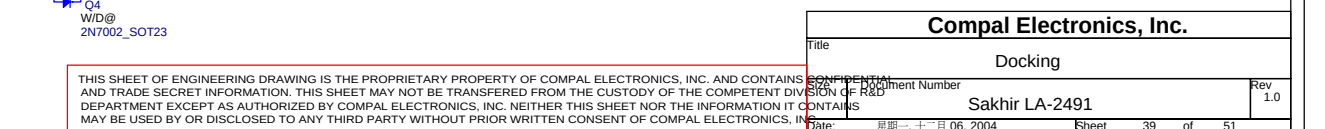
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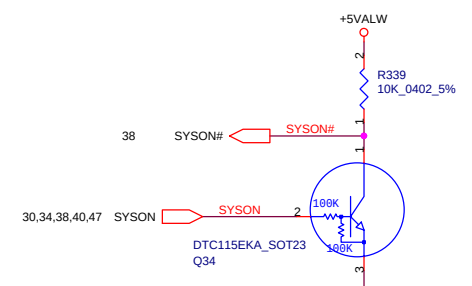
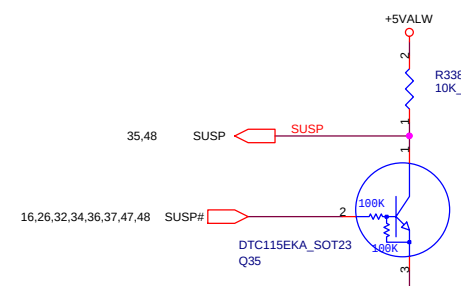
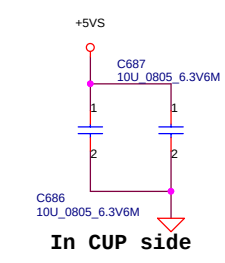
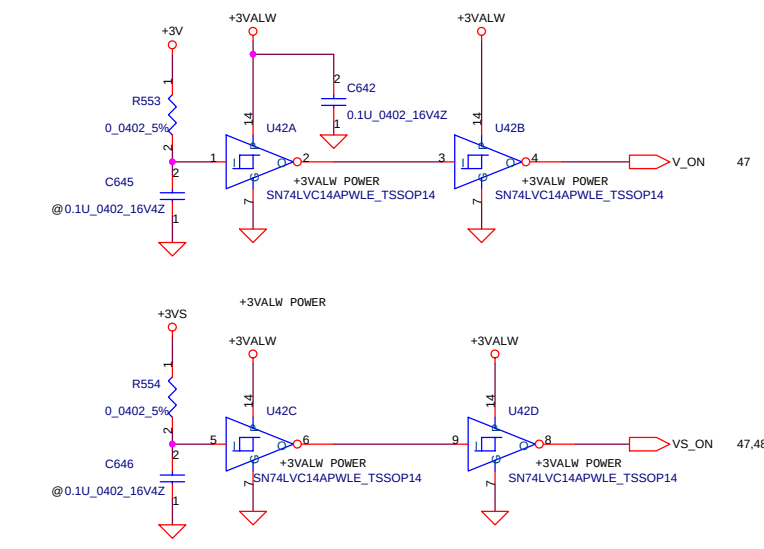
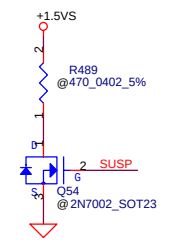
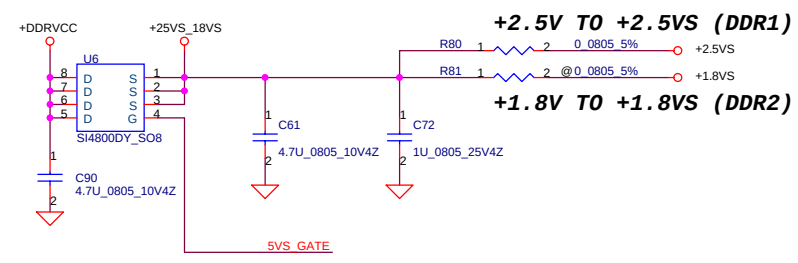
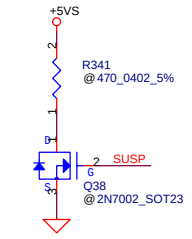
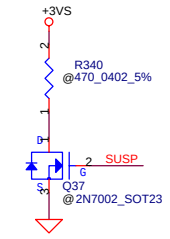
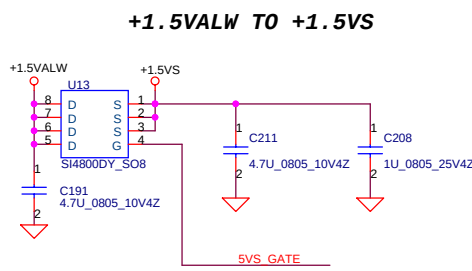
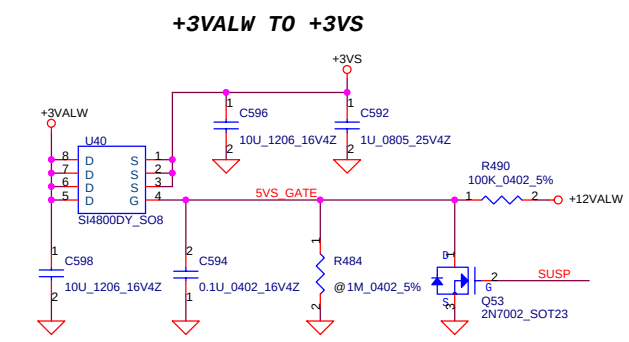
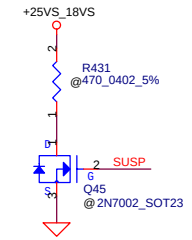
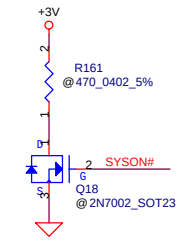
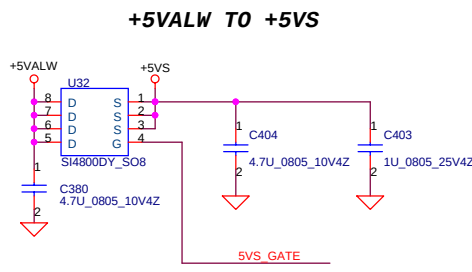
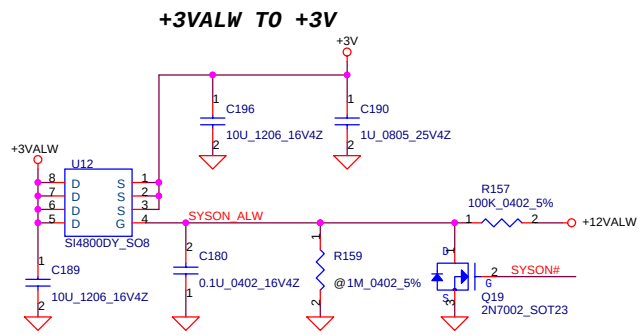
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W/D@

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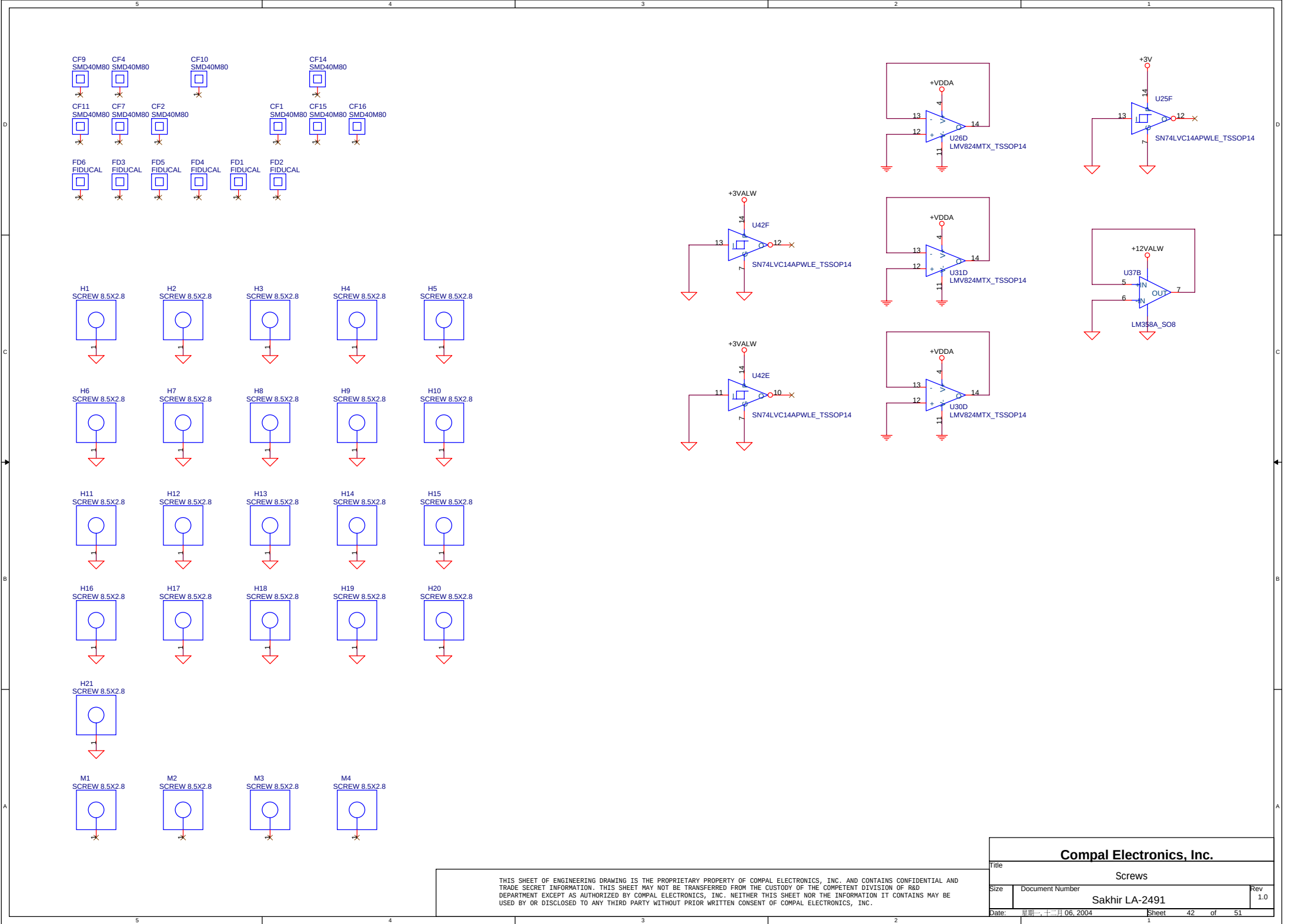
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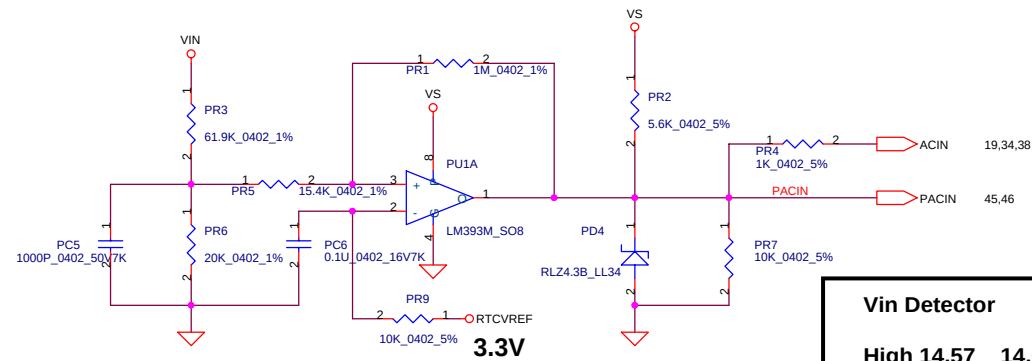
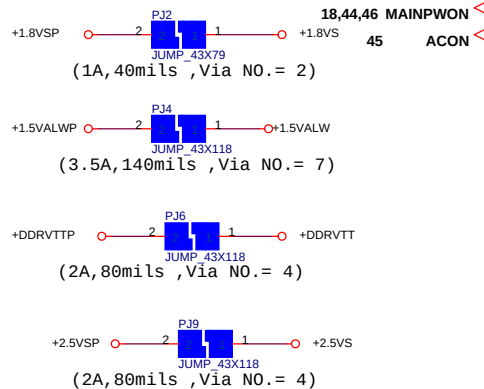
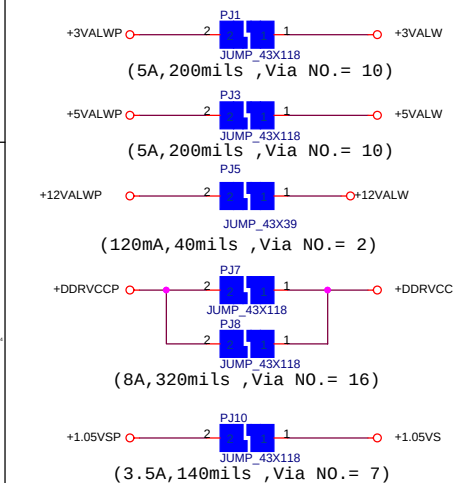
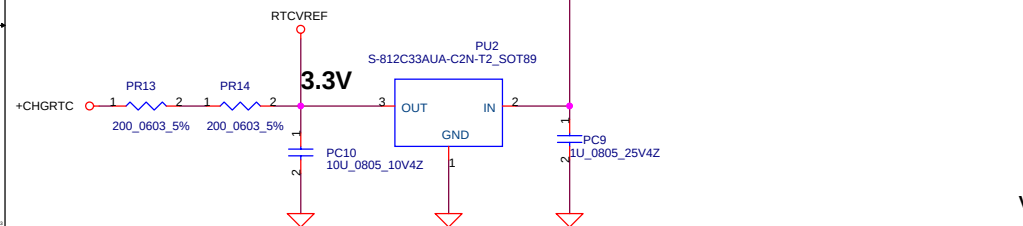
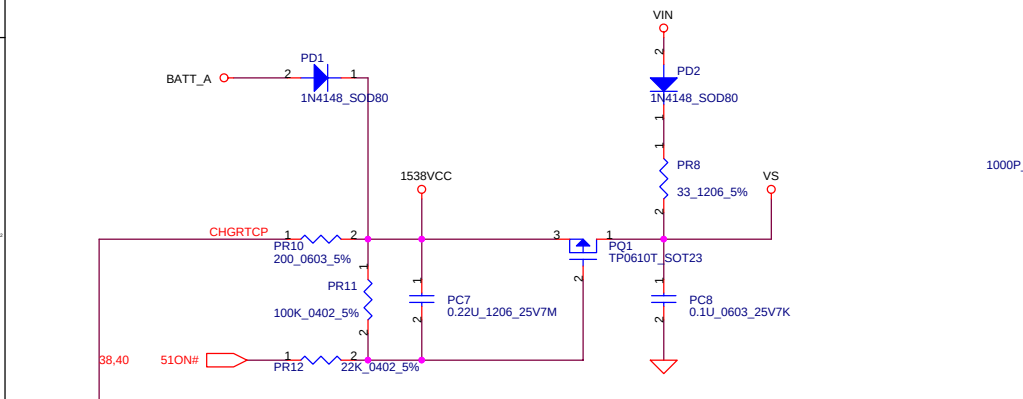
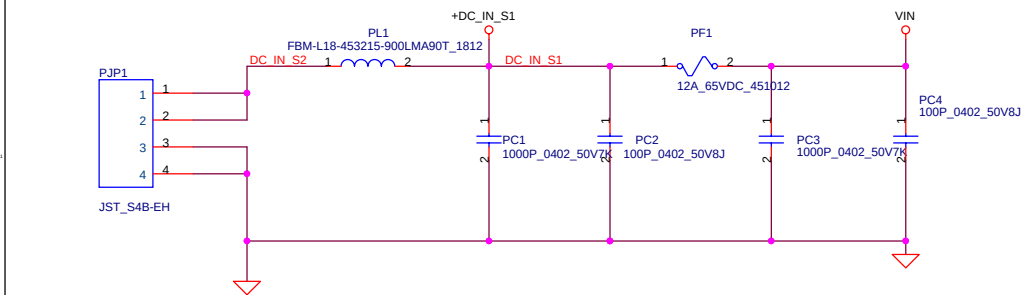
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POWER CONTROL CKT			
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Date	星期二, 十二月 06, 2004	Sheet	41 of 51

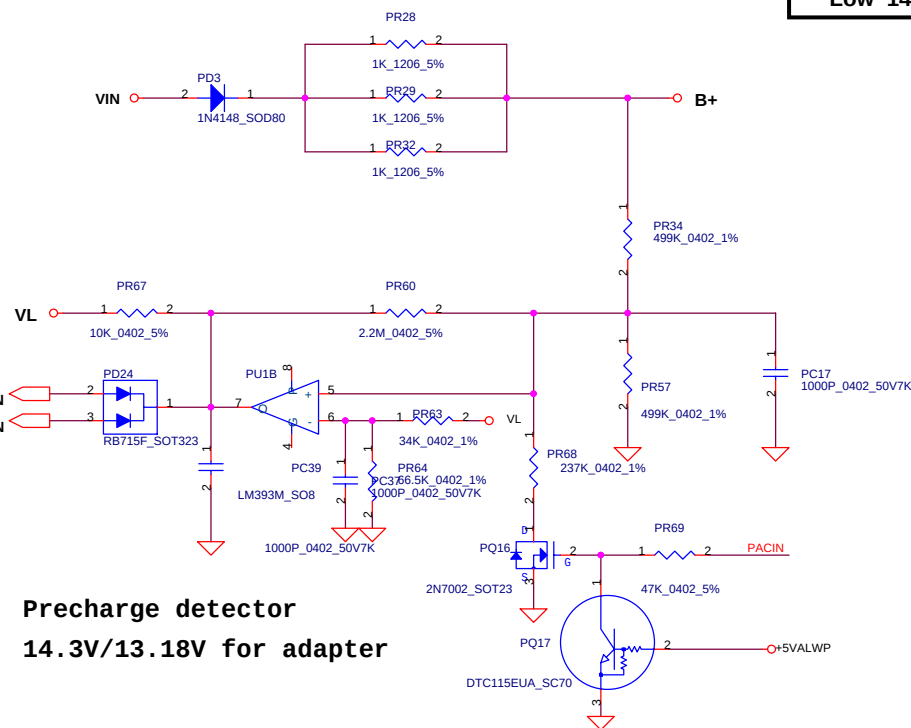


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Title				
Screws				
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Vin Detector				
High	14.57	14.01	13.46	
Low	14.06	13.51	12.98	

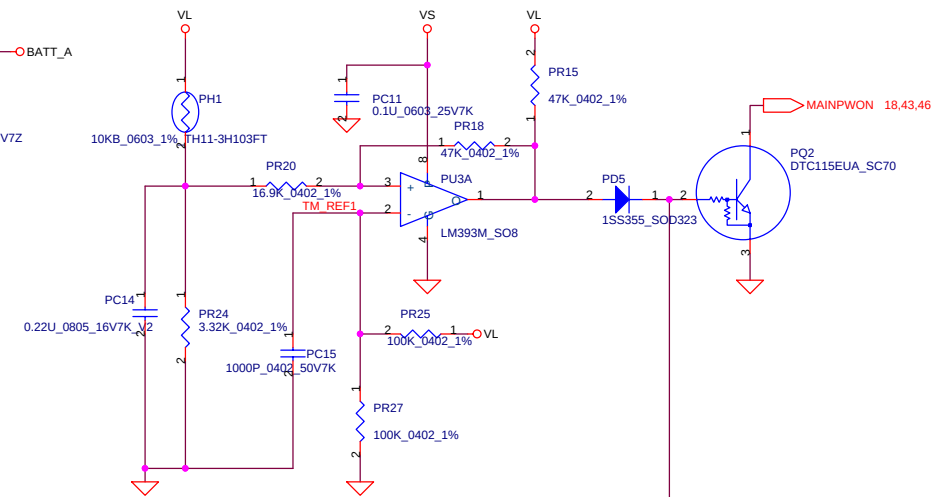
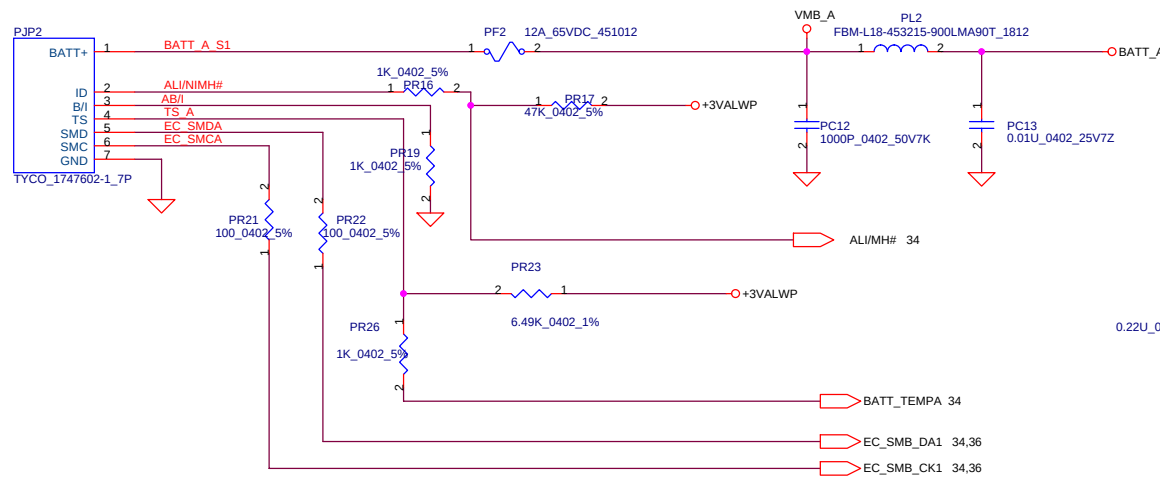


Precharge detector
14.3V/13.18V for adapter

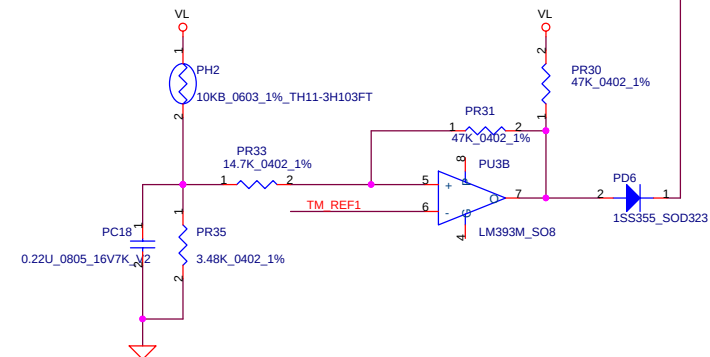
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Compal Electronics, Inc.				
Title DCIN & DETECTOR				
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PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C



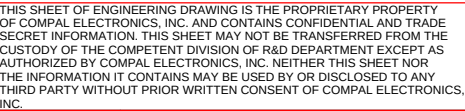
PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C

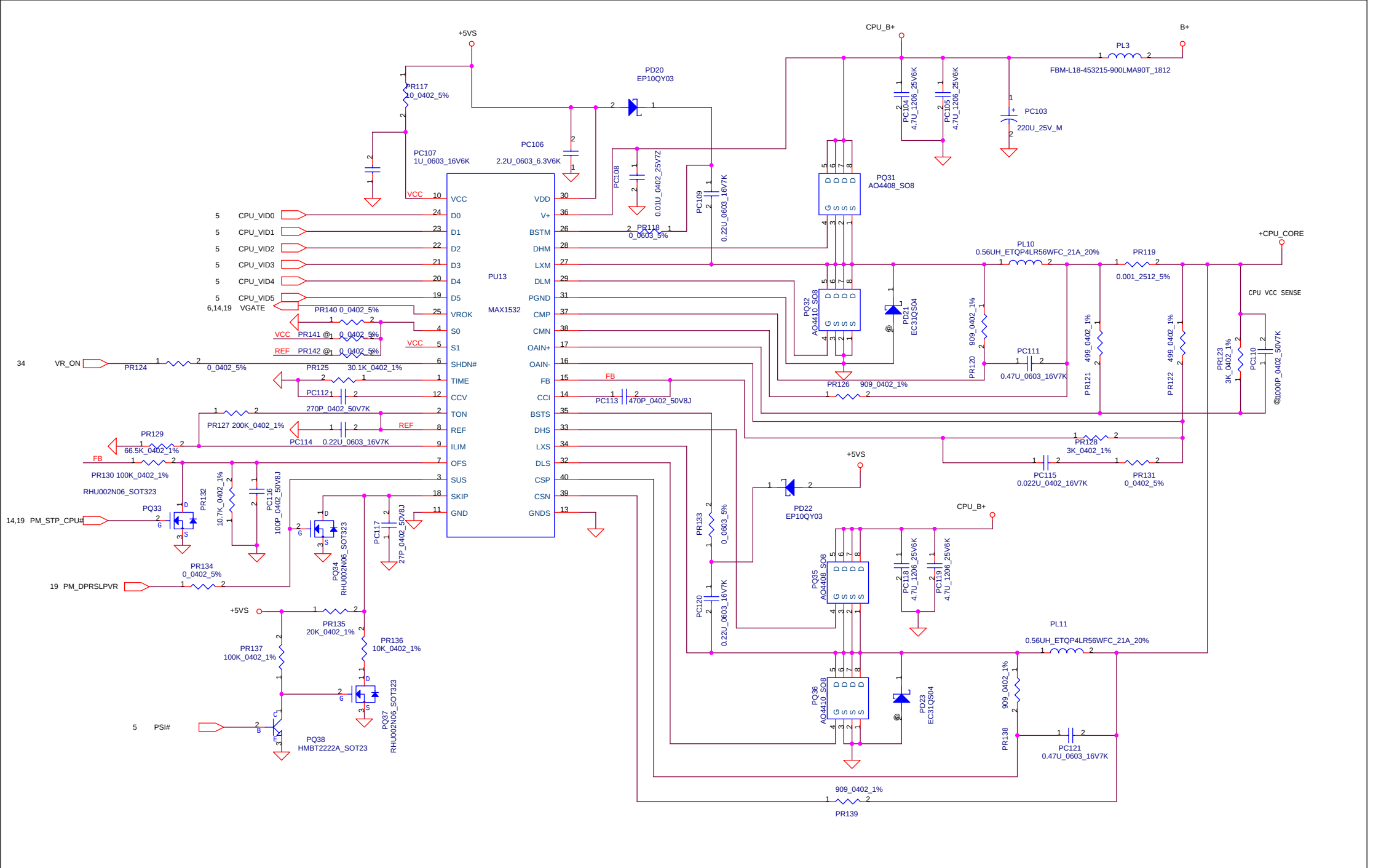


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Title			
BATTERY CONN / OTP			
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EAT10 PIR List

***** Rev:0.2 PIR List 2004/08/10 Writer by Jason *****

***** Rev:0.3 PIR List 2004/10/26 Writer by Sam Tsai *****

P05:Add @ in R63
Del @ in R56

P06:Del @ in R54
Del JP9

P08:Q6, Q43, Q44 Horizontally
"GMCH_TXCLK-, GMCH_TXCLK+" Swap

P12:+3VS change from JP25.194 to JP25.196

P15:Update U4 CIS Lib

P16:Del JP9
New add Q56

P21:New add R513
New add X3
New add C607

P22:New add R514, R534, @R535

P30:New add C639, C640
Change U27 to ALC2500
New add @R539, @R540, @R542, @Q59
New add @R536, @R537, @R538, @R541, @Q58
New add C608, C609, R522, R521, R526, C610, C611, C612, C641, X4
New add @R523, @R524, @R525
Del R295, R296, R310, R327, L20, @C311, C374

P33:New add R543, R544

P34:Del @ in R478
New add R547, @R548, R549, R550

P35:Del CP2, CP3, CP4, CP5, CP6, CP7
Modify JP14 Pin Define
New add C613, C614, C615, C616, C617
New add C618, C619, C620, C621, C622
New add C623, C624, C625, C626, C627
New add C628, C629, C630, C631, C632
New add C633, C634, C635, C636

P36:Del @U42, @C608
New add U43, U44, U45
New add C637, C638
New add R527, R528, R529

P37:Swap JP12.1, JP12.3
Swap SW1.1, SW1.3

P38:Q52 change from 2N7002 to DTA114
New add R530, R531, R532, R533, Q57

P04:Add @ in R28 Intel Recommend

P06:Add @ in C441, C427
Del J209 C460 Change Value from 220U to 330U Power Team testing OK

P12:+3VS change from JP25.196 to JP25.194 Intel Recommend

P15:New add R570, R571 & R572
New add L33
Del D2 & D25 RGB without Docking
EMI

P16:Change U44 from 7404 to 74125 LCDVDD Soft-Start

P18:New add R573
R439 Change Value from 100K to 20K
C271 Change Value from 0.1U to 1U Intel Recommend
Intel Recommend

P20:R214 Change Value from 1K to 10ohm Intel Recommend

P22:New add @R , @R& Q SWDJ testing

P24:New add R586
New add @R581 TI Recommend

P25:New add R582, R583, @R584, R585, R588, R589 & @C685 TI Recommend

P27:R73 Change Value from 4.99K to 4.7K Marvwl Recomm

P31:R361 & R371 Change Value from 47K to 22K Design Change

P33:New add R543, R544 Design Change

P32:Modify C399 Net to SPKL+

P33:New add L34
add@ in C647 ~ C662 EMI

P34:New add R587 Design Change

P35:New add JP32 & C671
New add C682 ~ C684
JP13 reverse Design Change
EMI

P36:New add SWDJ testing

P37:SW1 change to 1BS003-1211L_3P Design Change

P38:Q52.3 change from +3VALW to +3V Design Change
Q57.3 change from +5VALW to +5VS
Lid Switch IC Power change from JP16.26 +3VALW to JP16.27 RTCVREF
EMI

P39:New add R574 Design Change

P40:Del D11 Design Change

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Title			
Changed-List History-1			
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