IAYAA

LA-3391P REV 1.0 Schematic

UFC-PGA Yonah/ RC410MD(ME)/ SB450

2006-11-03 Rev. 1.0

Security Classification	Compal Secret Data		
Issued Date	2006/05/18	Deciphered Date	2007/10/25

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Title: Black Diagram

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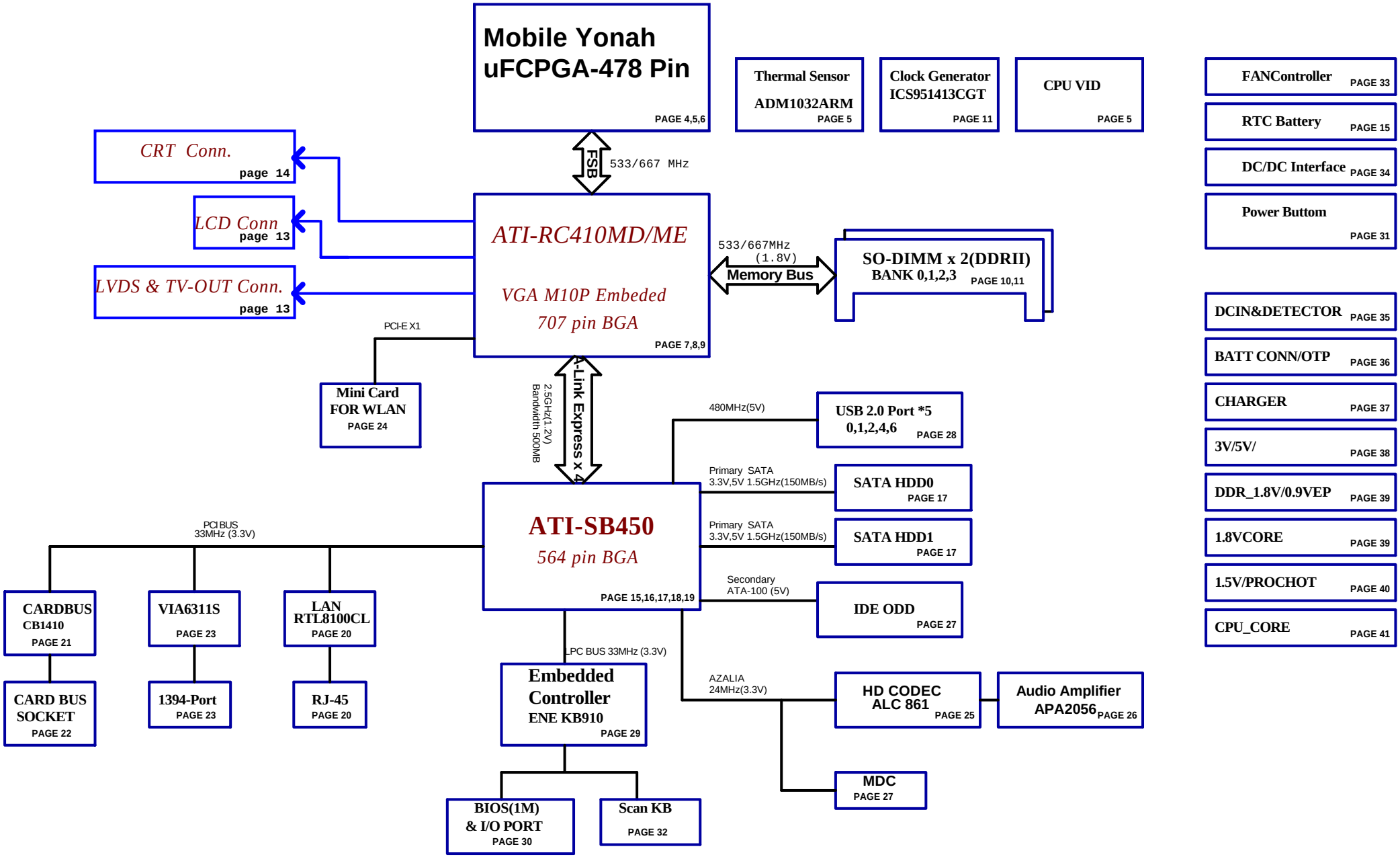
Date: Tuesday, November 07, 2006 | Sheet 1 of 48

IVYAA LA-3391P FUNCTION BLOCK DIAGRAM



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Title	Black Diagram	
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VGA_CORE	1.0V/1.2V switched power rail for VGA chip	ON	OFF	OFF
+1.2VS	1.2VS for PCI-Express	ON	OFF	OFF
+0.9VS	0.9V switched power rail	ON	OFF	OFF
+1.5VS	DOTHAN B	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8V	1.8V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Card Bus	AD20	2	PIRQB
LAN	AD22	1	PIRQG
1394	AD16	0	PIRQA

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
ADM1032	1001 100X b

SB450 SM Bus address

Device	Address	
Clock Generator (ICS951413CGLFT)	1101 001Xb	
DDR DIMM0	1010 0100b	A4
DDR DIMM1	1010 0110b	A6

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO	BOM STURCTURE
WIRELESS	WLAN@
1394	1394@
MIC	MIC@, 45 MIC@
Second HDD	2H@
NB Chipset	MD@, ME@
MDC	MDC@

SKU ID	BTN_ID
0	1 Buttons
1	
2	
3	
4	7 Buttons
5	
6	
7	

	SKU_ID
0	WW
1	
2	
3	
4	JP
5	
6	
7	

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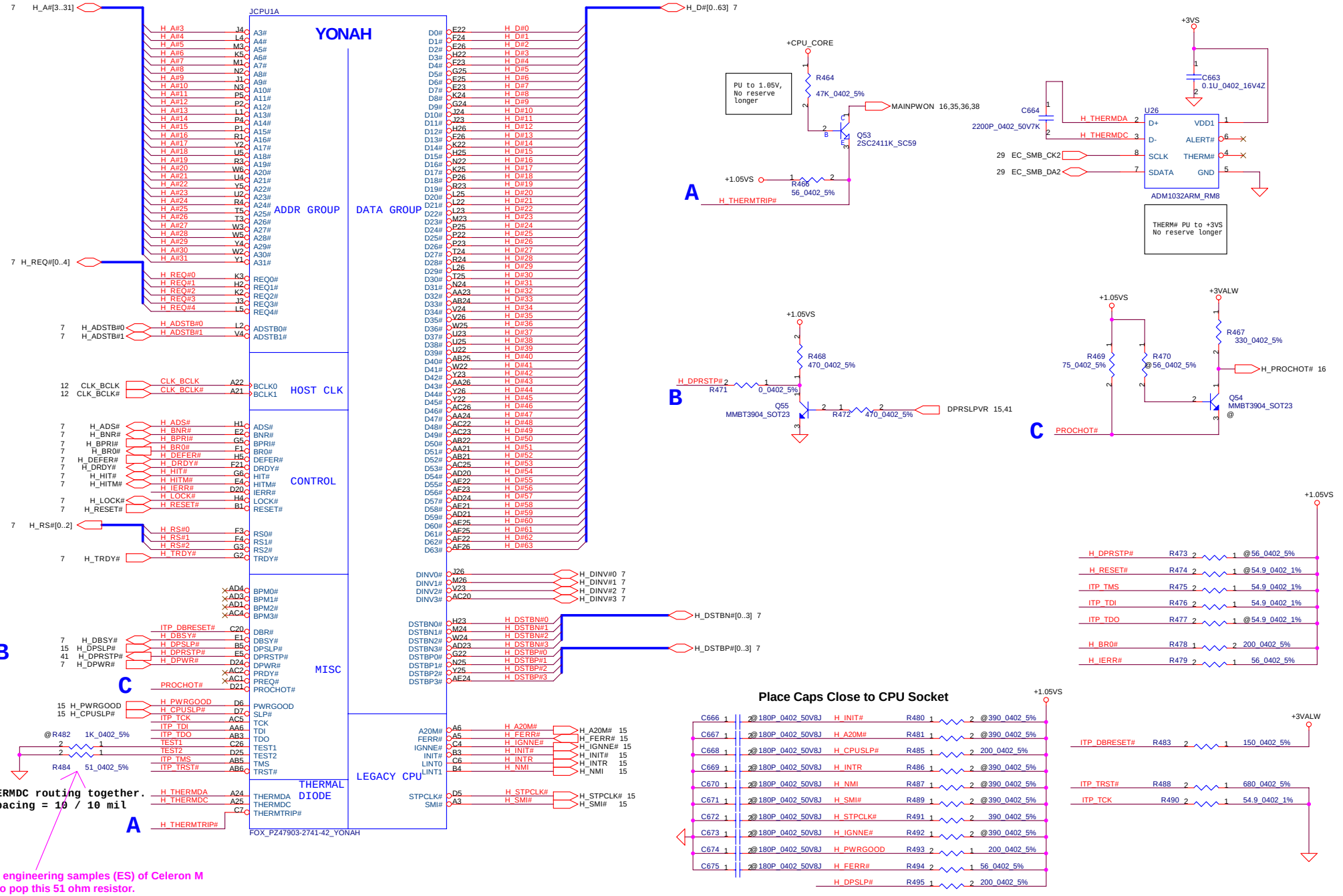

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Compal Electronics, Inc.

Title: Yonah(1/2)-GTLITP

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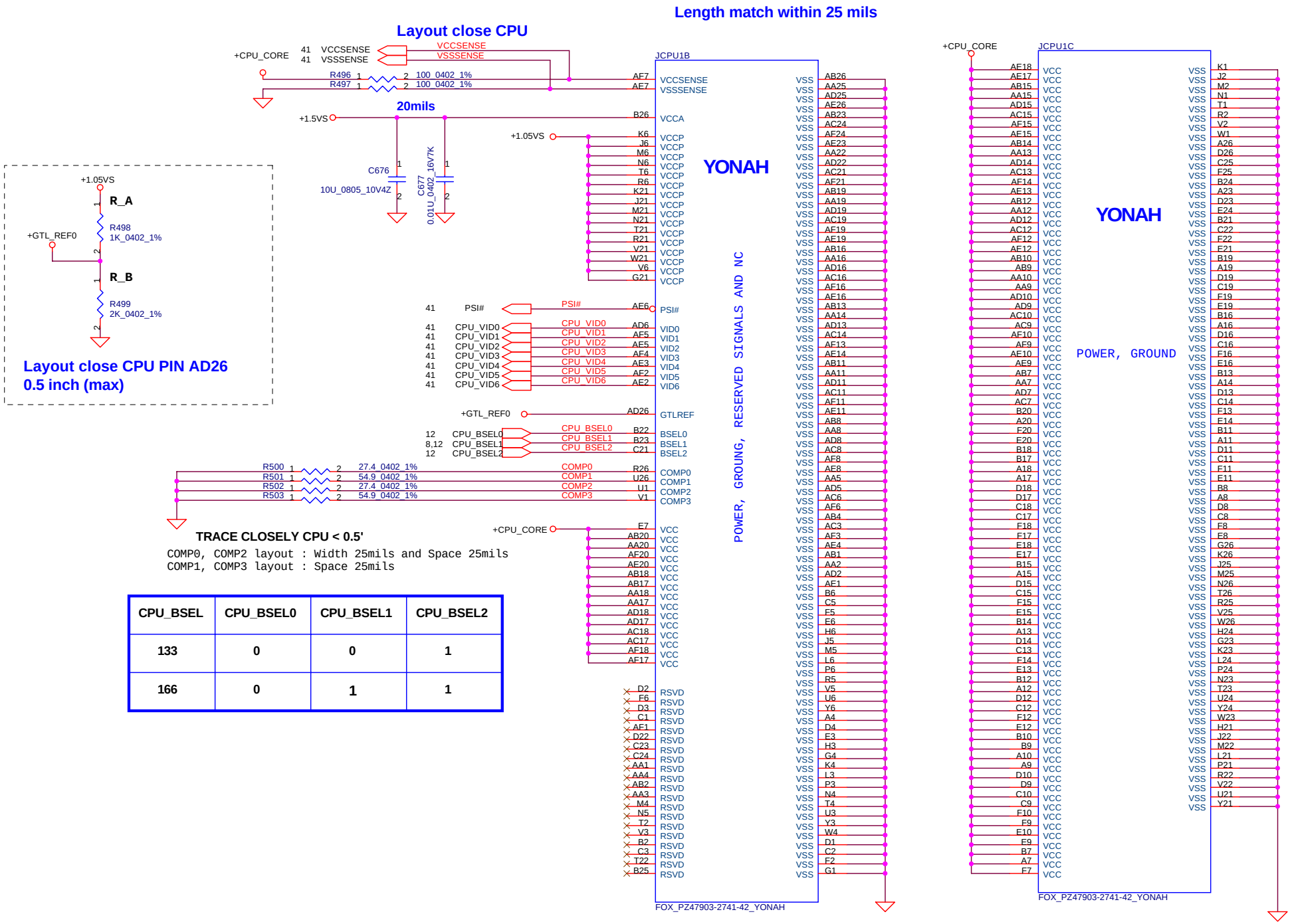

CPU_BSEL	CPU_BSEL0	CPU_BSEL1	CPU_BSEL2
133	0	0	1
166	0	1	1

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Compal Electronics, Inc.

Title: Yonah(2/2)-PWR/GND

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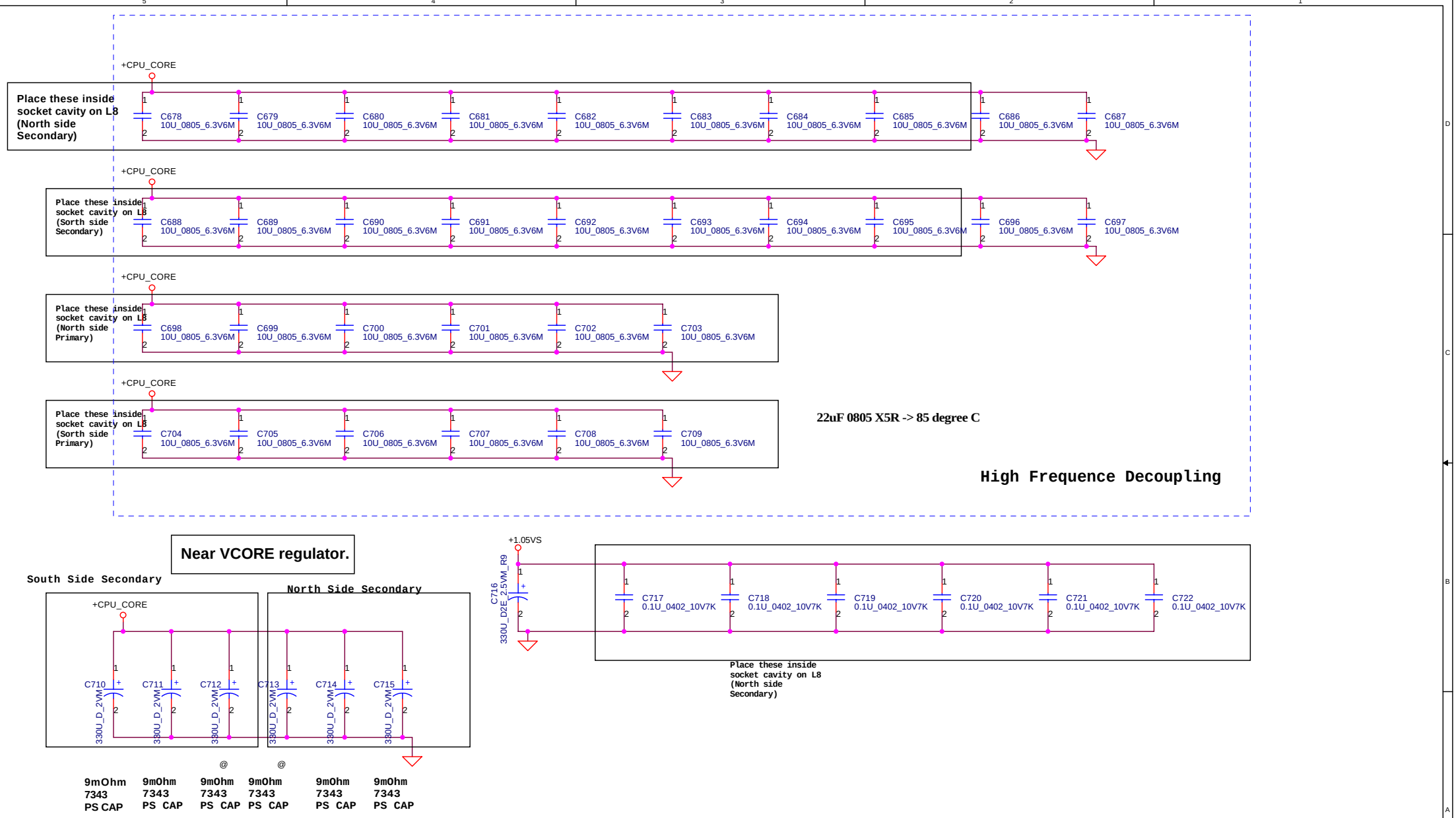

ESR <= 1.5m ohm
Capacitor > 1980uF

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Compal Electronics, Inc.

Title: Yonah Bypass

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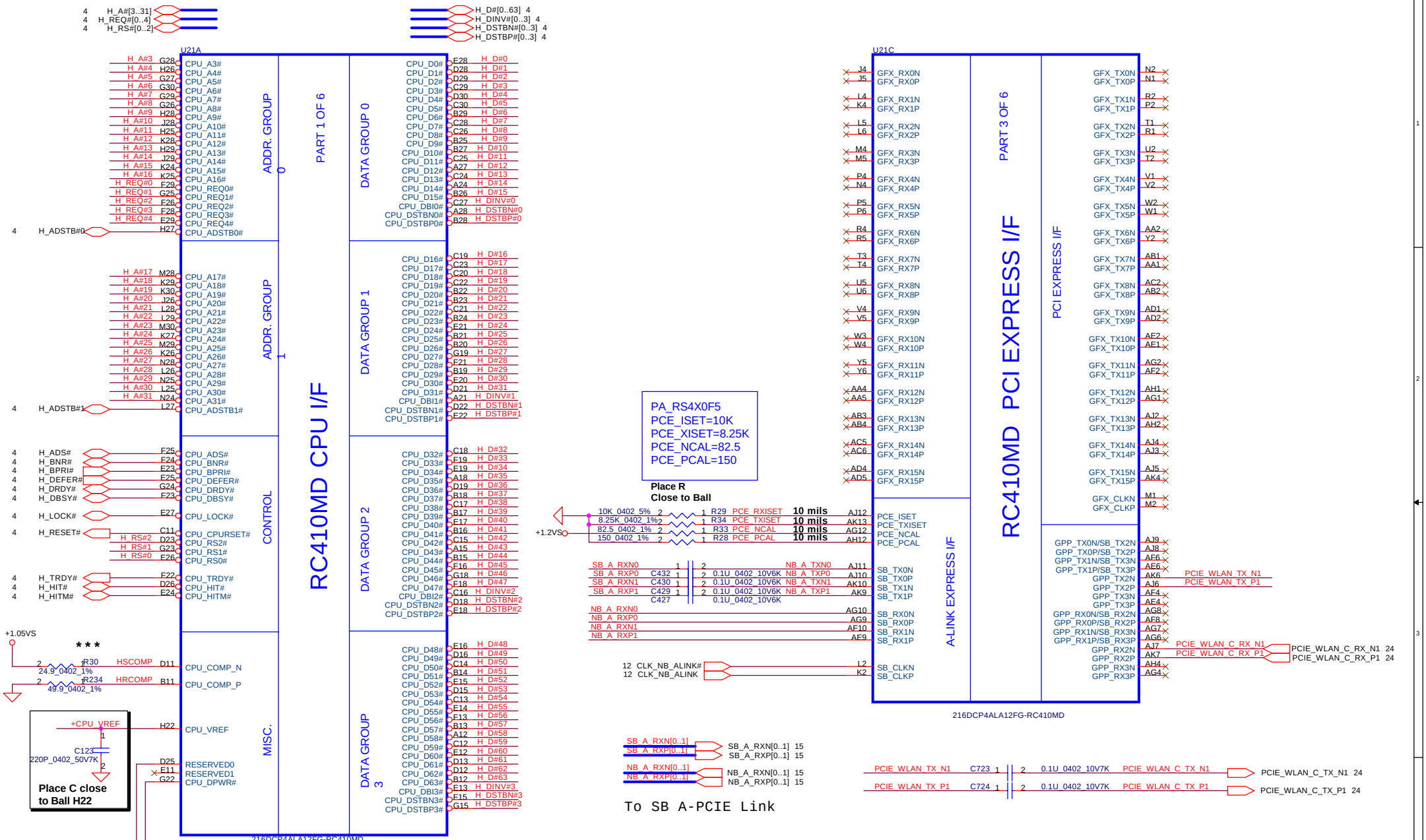

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Compal Electronics, Inc.

Title: RC410MD-FSB, PCIE,A-PCIE

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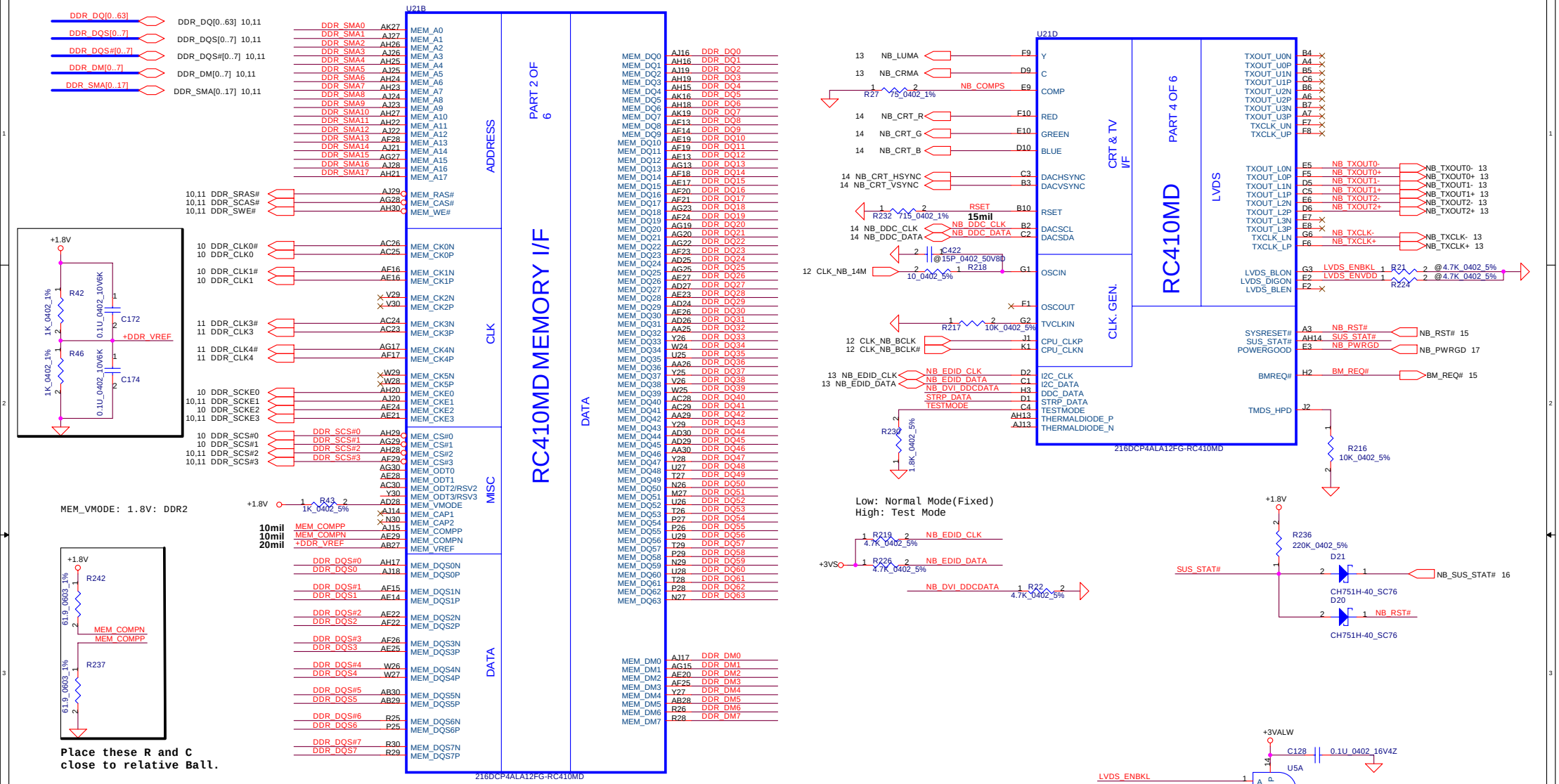
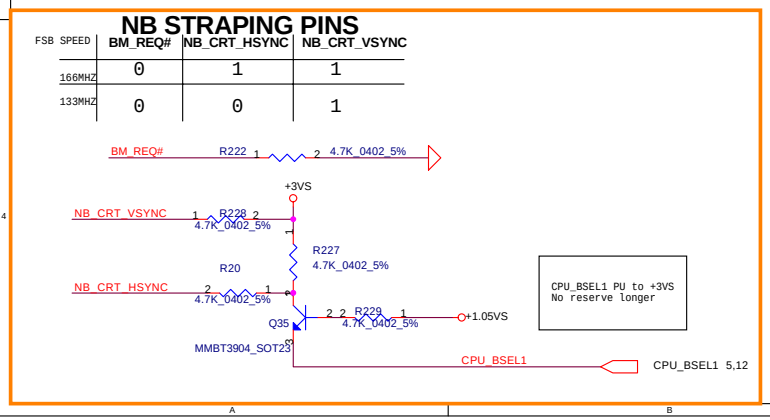
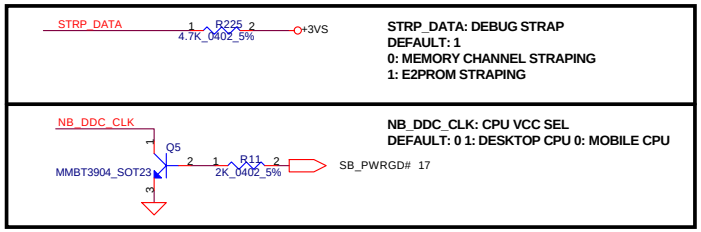


NB STRAPING PINS

FSB SPEED	BM_REQ#	NB_CRT_HSYNC	NB_CRT_VSYNC
166MHZ	0	1	1
133MHZ	0	0	1





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Compal Electronics, Inc.

Title: RC410MD-DDR/DISP/MISC

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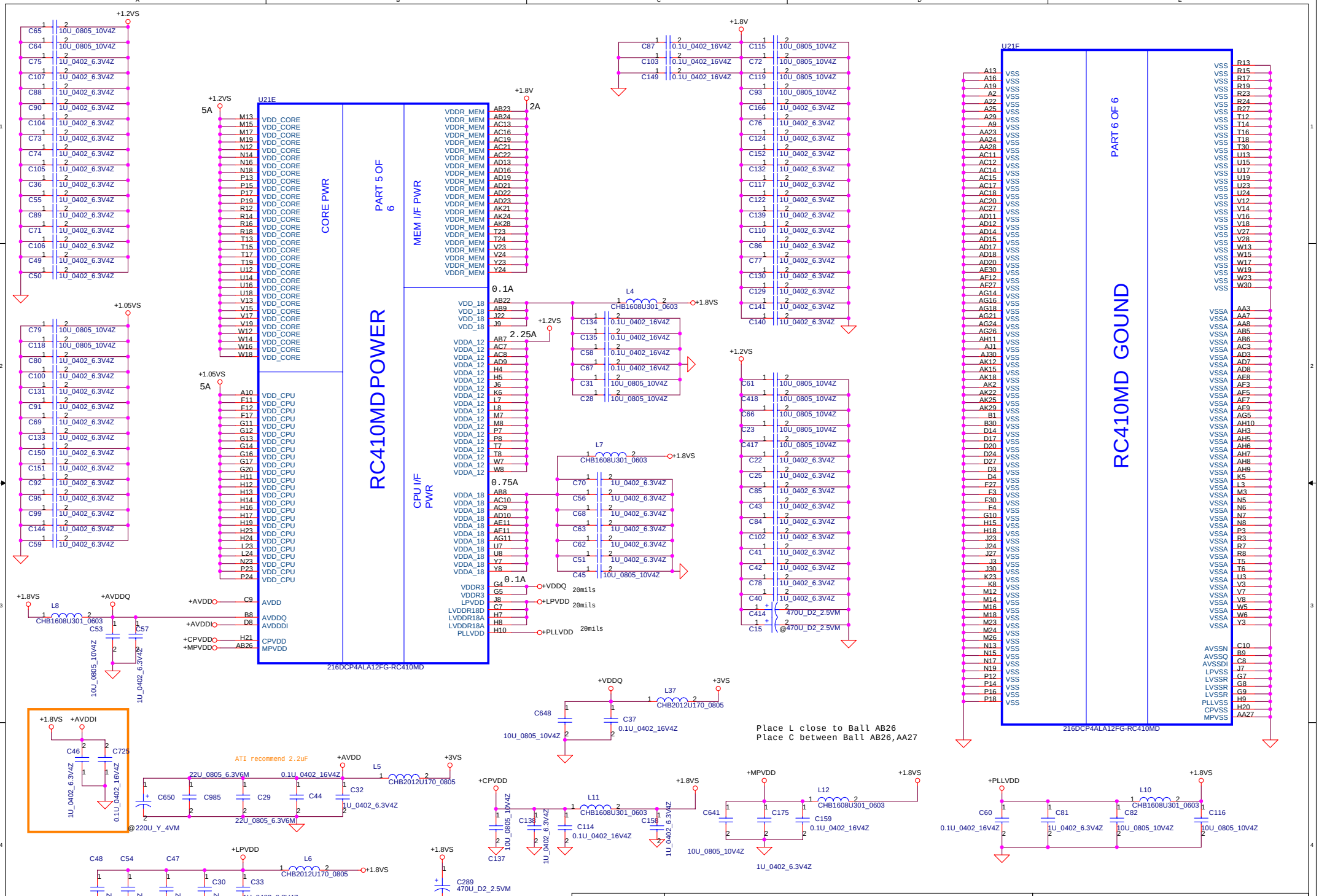

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Compal Electronics, Inc.

Title: RC410MD PWR/GND

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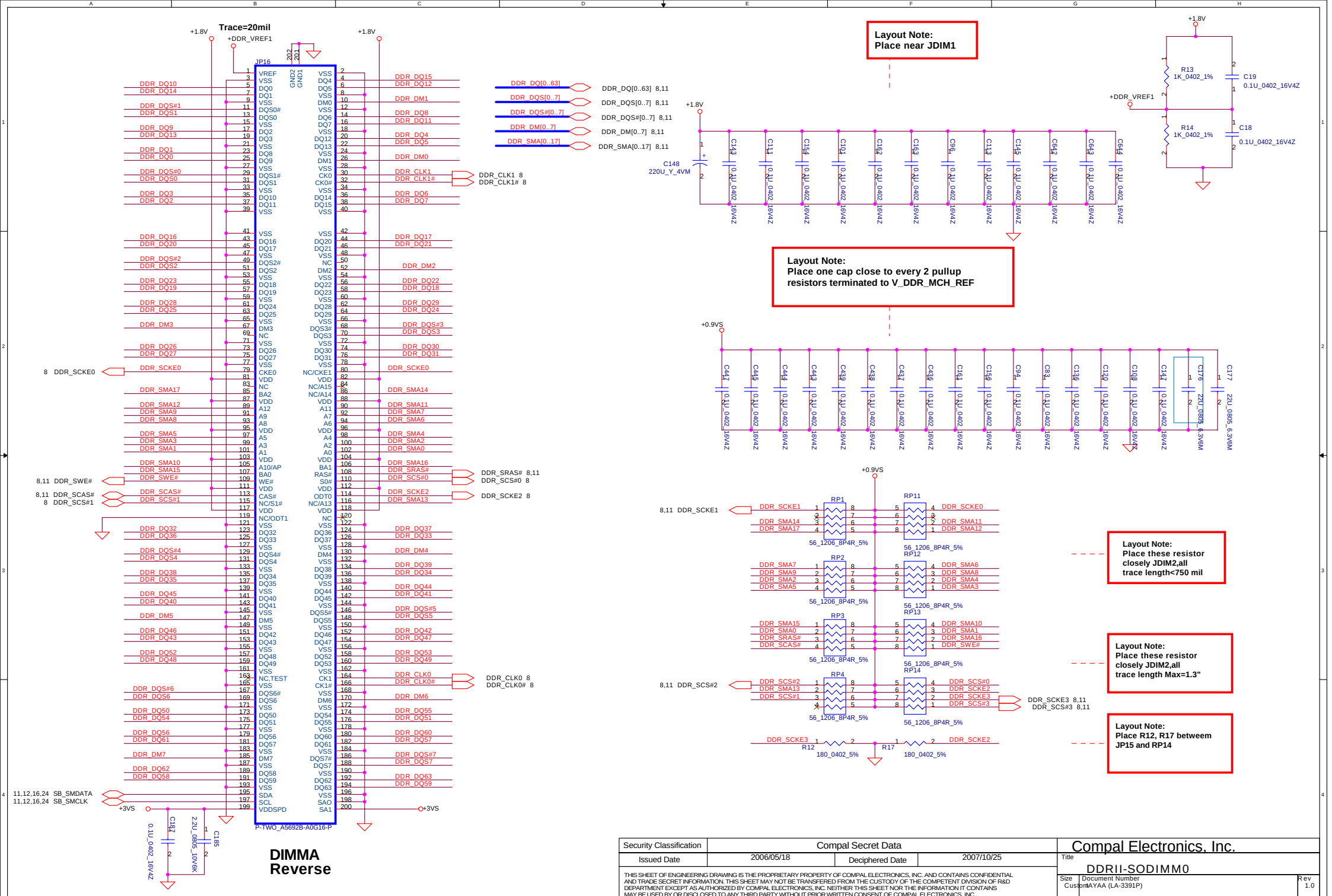

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Compal Electronics, Inc.

Title: DDRII-SODIMM0

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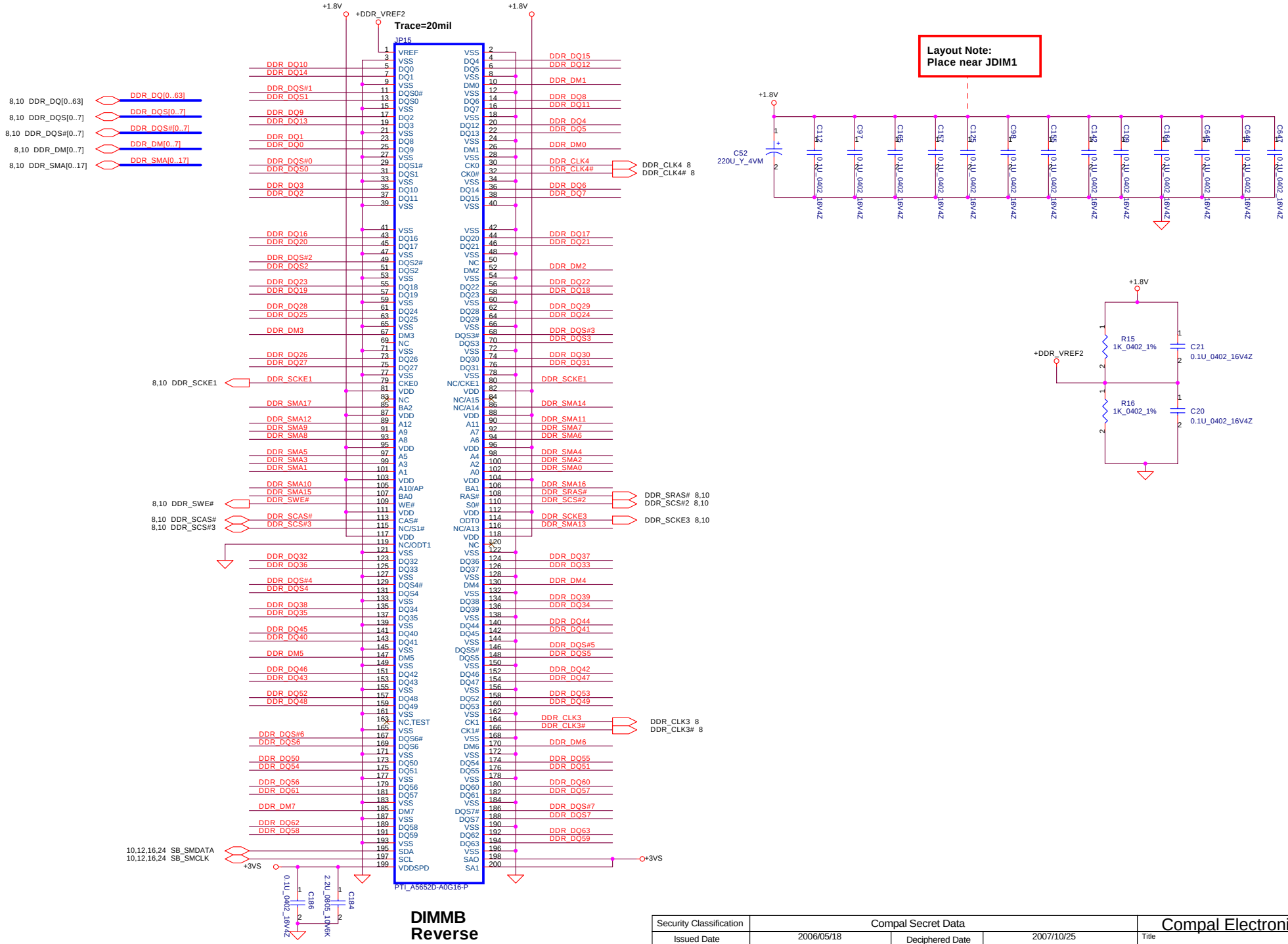

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Compal Electronics, Inc.

Title: DDR-II SODIMM1

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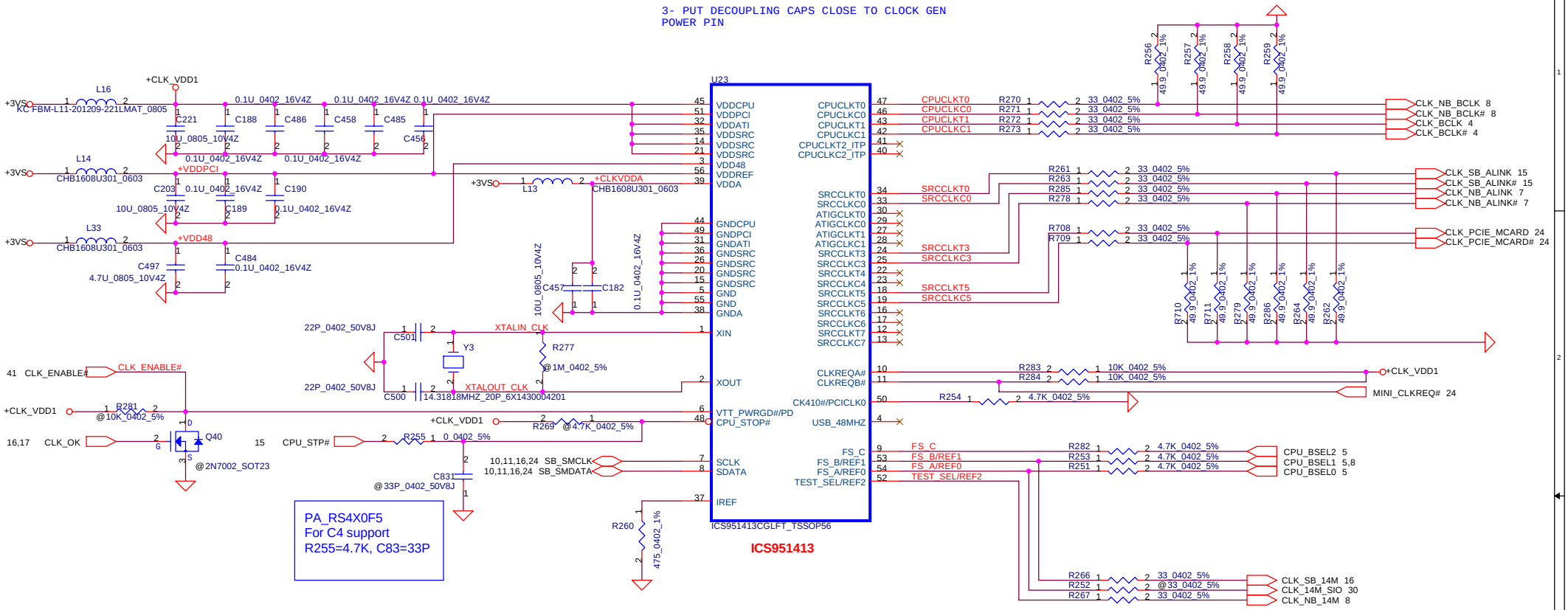
Clock Generator

1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLOCK GEN AS POSSIBLE

2- ROUTE ALL CPUCLK/#, NBCLK/#, ITPCLK/# AND SCR/# ,AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



PA_RS4X0F5
For C4 support
R255=4.7K, C83=33P

FS_C	FS_B	FS_A	CPU	SRC	PCI	REF	USB
1	0	1	100.00	100.00	33.33	14.318	48.000
0	0	1	133.33	100.00	33.33	14.318	48.000
0	1	1	166.66	100.00	33.33	14.318	48.000

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Compal Electronics, Inc.

Title: ClockGen ICS 951411

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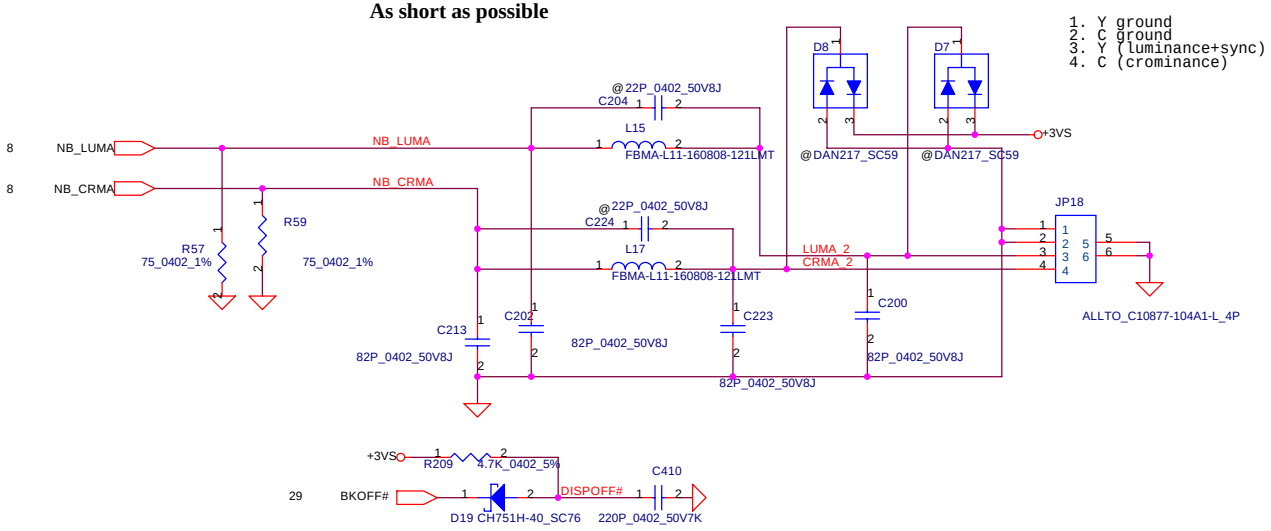
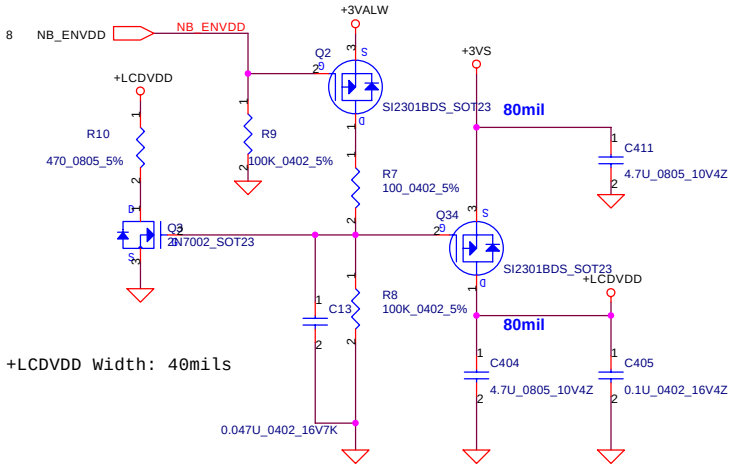
TV-OUT CONNECTOR

Reduce LUMA_1 and CRMA_1 length
As short as possible

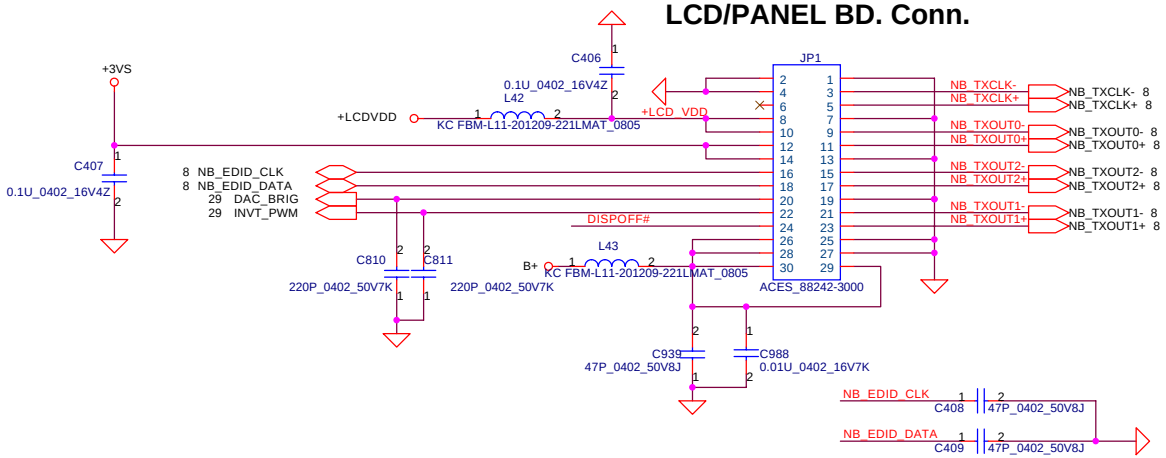


PANEL +LCDVDD CTRL CKT



+LCDVDD Width: 40mils

LCD/PANEL BD. Conn.



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Compal Electronics, Inc.

Title: TV-OUT, LVDS CONNECTOR

Size: B | Document Number: IAYAA (LA-3391P) | Rev: 1.0

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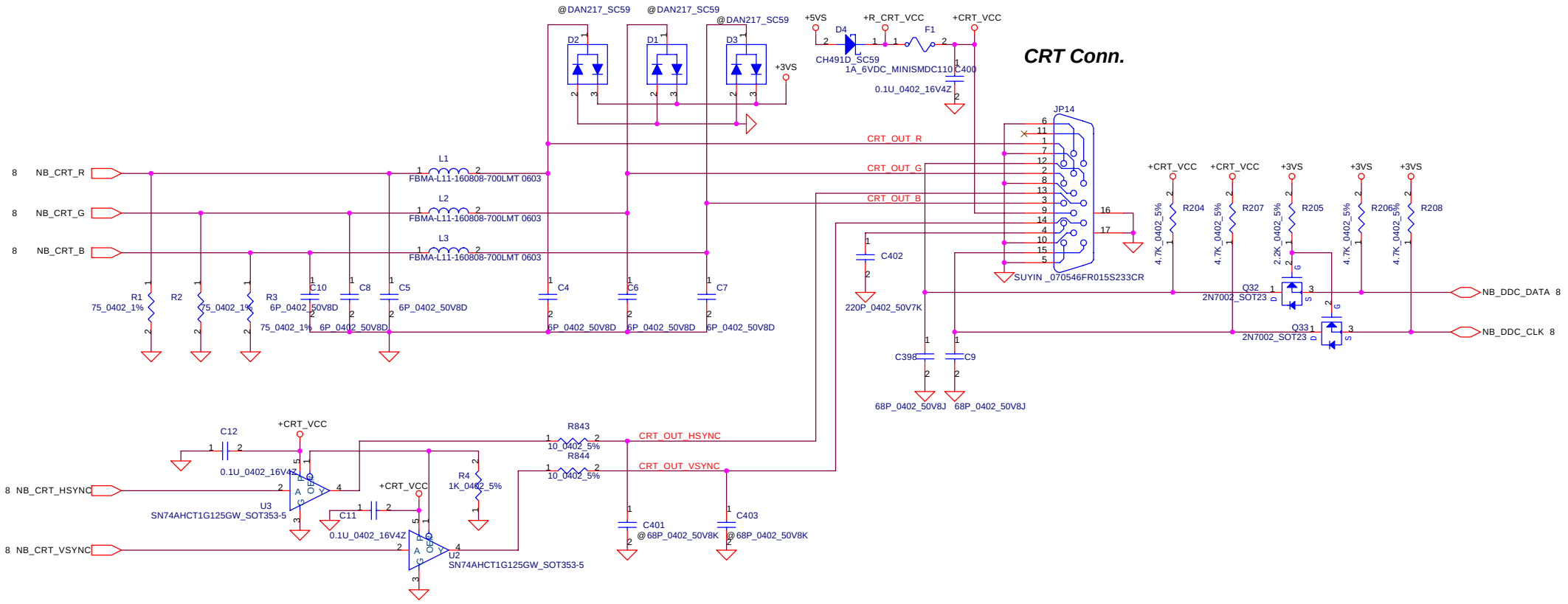
CRT CONNECTOR



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Compal Electronics, Inc.

Title: CRT CONNECTOR

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PA_IXP400AC16
C300, C305, C295, C298=10nF
A_RST#, PCIRST# 8.2K Pull down
BMREQ# add diode and RC

SB450 SB
Part 1 of 4

PCI EXPRESS INTERFACE
PCI CLKS
PCI INTERFACE
XTAL
CPU
LPC
RTC

Spread Spectrum

SS%	Deviation
1	0.5%
0	0.25%

Pull-high on CPU side

RTC Battery

Place JOPEN1 close to DDR-SODIMM

Consider --connect RTC_CLK to EC

PA_RS4X0F5
For C4 support

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Compal Electronics, Inc.

Title: PCI_EXP/LPC/RTC

Size: | Document Number: IAYAA (LA-3391P) | Rev: 1.0

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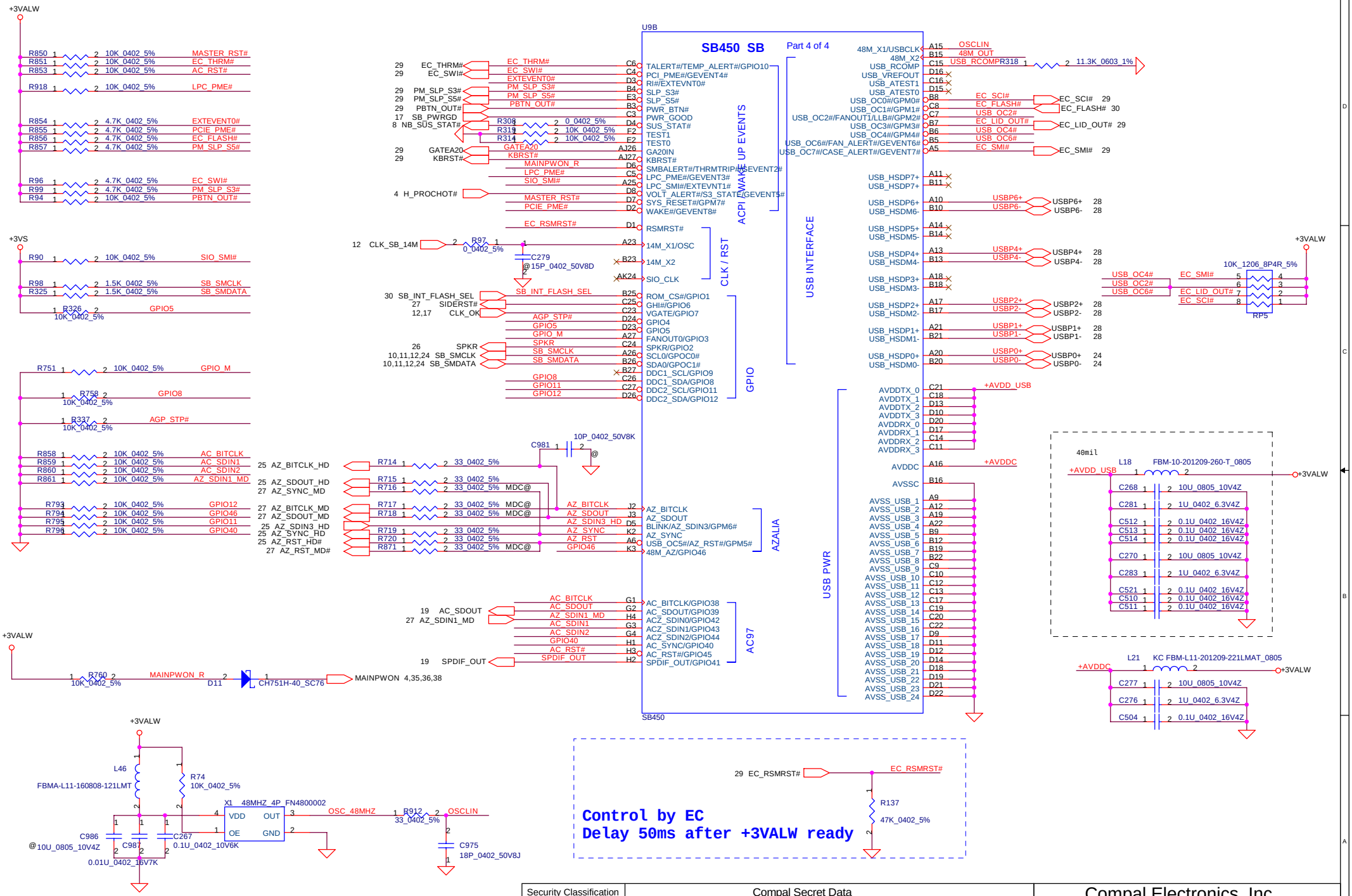

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Compal Electronics, Inc.

Title: SB450 USB/ACPI/AC97/GPIO

Size: Custom | Document Number: MAYAA (LA-3391P) | Rev: 1.0

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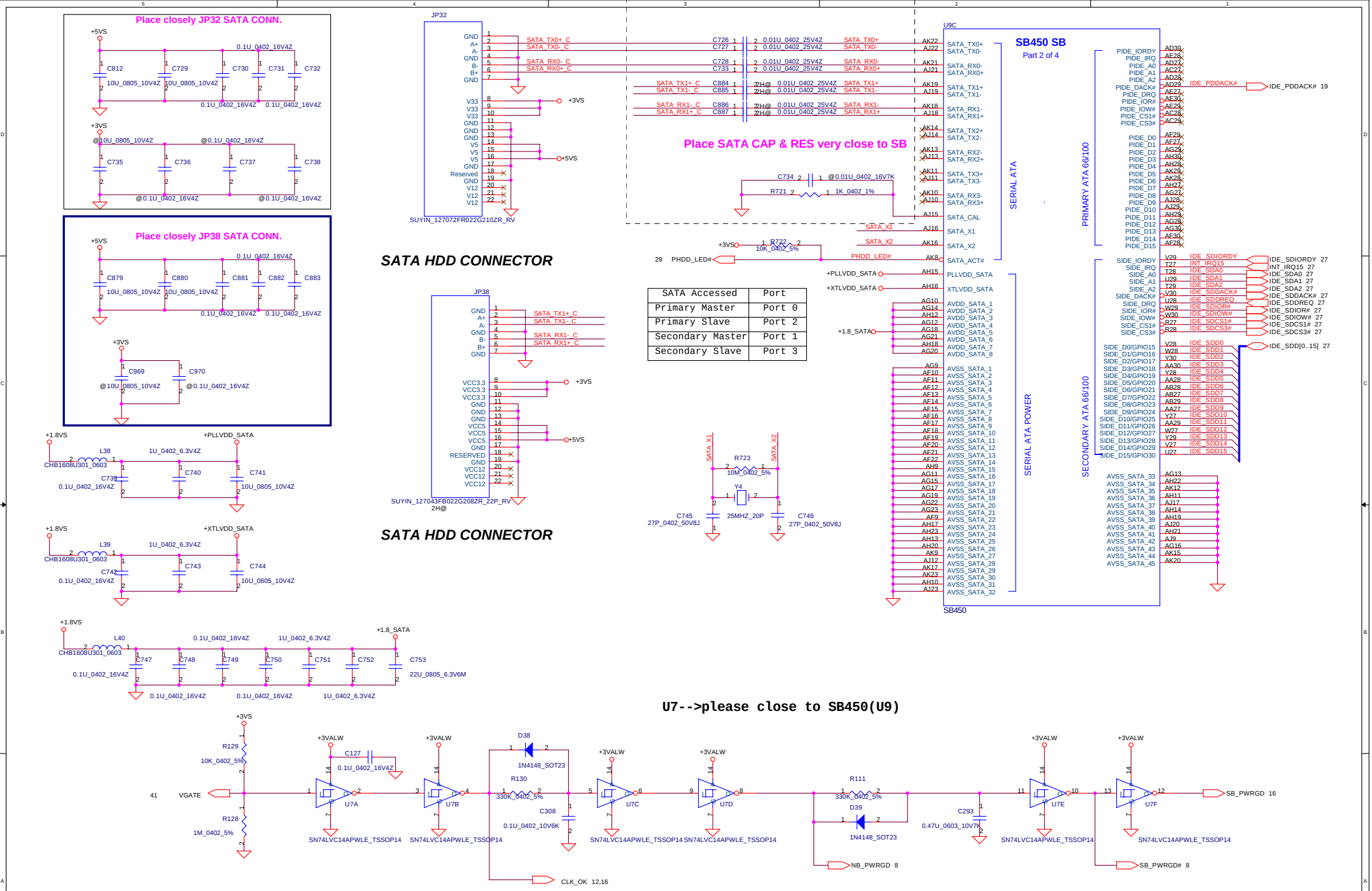

SATA Accessed	Port
Primary Master	Port 0
Primary Slave	Port 2
Secondary Master	Port 1
Secondary Slave	Port 3

Security Classification	Compal Secret Data		
Issued Date	2006/05/18	Deciphered Date	2007/10/25

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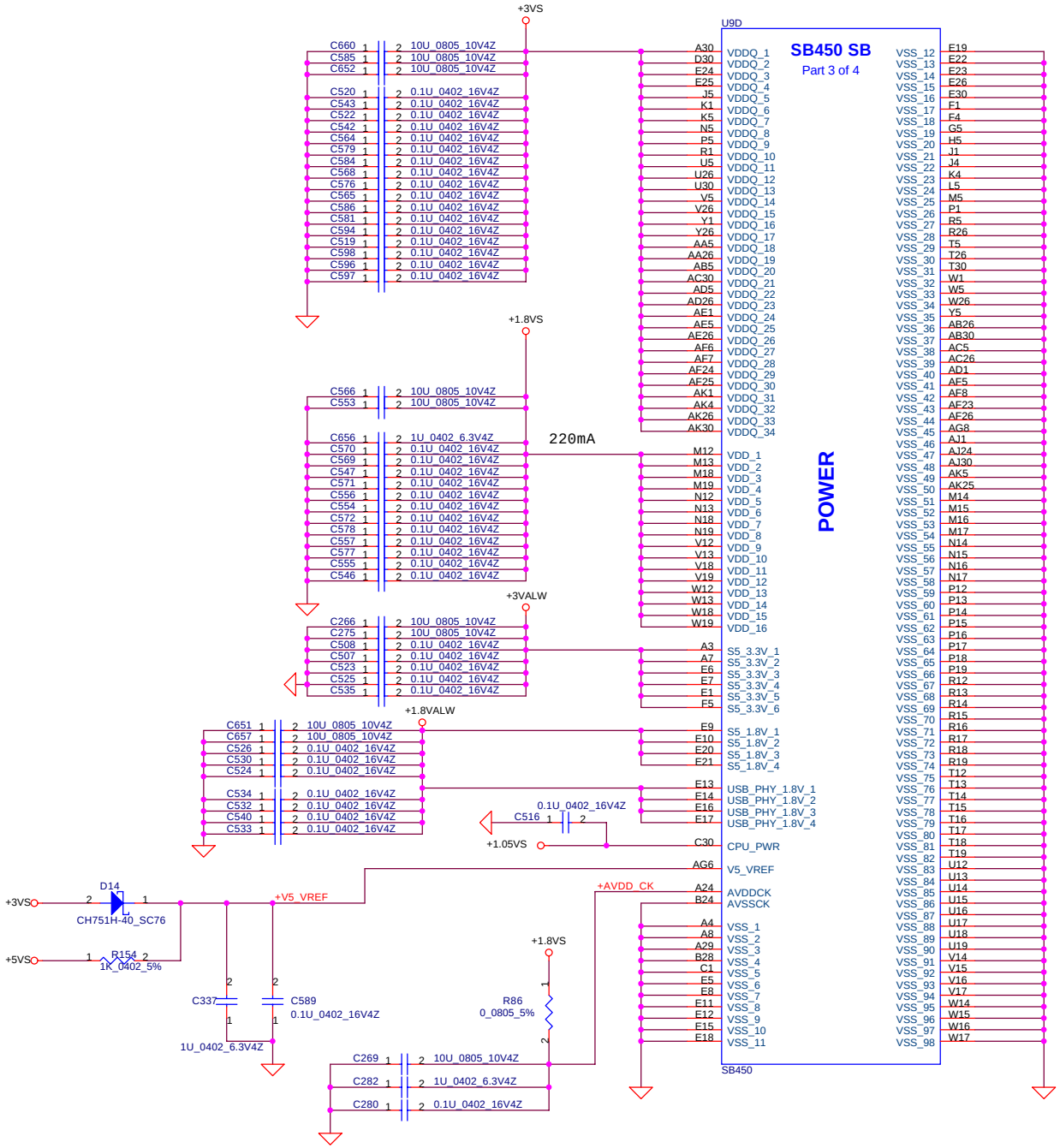
Compal Electronics, Inc.

Title: SB450 IDE/SATA

Size: Custom | Document Number: LAYAA (LA-3391P) | Rev: 1.0

Date: Friday, November 03, 2006 | Sheet 17 of 48



Security Classification	Compal Secret Data		
Issued Date	2006/05/18	Deciphered Date	2007/10/25

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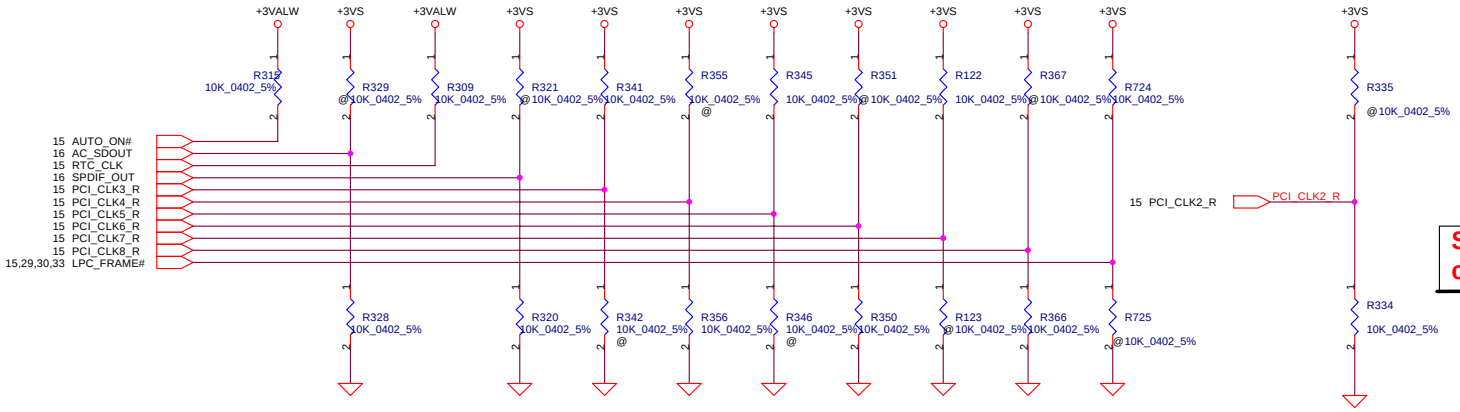
Compal Electronics, Inc.

Title: SB450/POWER/GND

Size: B | Document Number: IAYAA (LA-3391P) | Rev: 1.0

Date: Friday, November 03, 2006 | Sheet 18 of 48

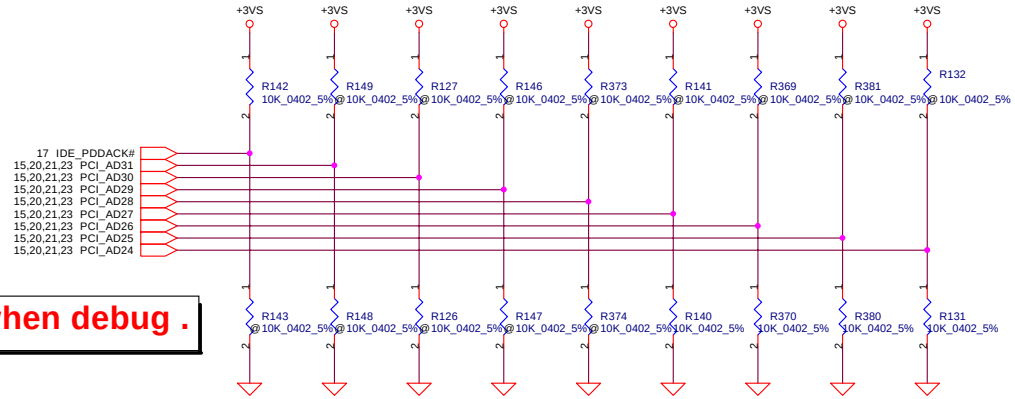


Selects type of 48MHz clock pad

ACPWRON

REQUIRED STRAPS

	AUTO_ON#	AC97_SDOUT	RTC_CLK	SPDIF_OUT	CLK_PCI3	CLK_PCI_LAN	CLK_PCI_LPC	PCI_CLK6	PCI_CLK7 PCI_CLK8	PCI_CLK2_R	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	USB PHY PWRDOWN DISABLE	Internal PLL	PCIE CM_SET low DEFAULT	CPU I/F = K8	ROM TYPE H,H = PCI ROM H,L = LPC ROM I L,H = LPC ROM II L,L = FWH ROM	Crytsal Pad	THERMTIP# ENABLE
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHZ DEFAULT	USB PHY PWRDOWN ENABLE DEFAULT	External Clock DEFAULT	PCIE CM_SET HIGH	CPU I/F = P4 DEFAULT		Clock input buffer DEFAULT	THERMTIP# DISENABLE



Pop R634 when debug .

DEBUG STRAPS

	IDE_PDDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT

```
AD23 strapping
No reserve longer
```

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Issued Date	2006/05/18	Deciphered Date	2007/10/25

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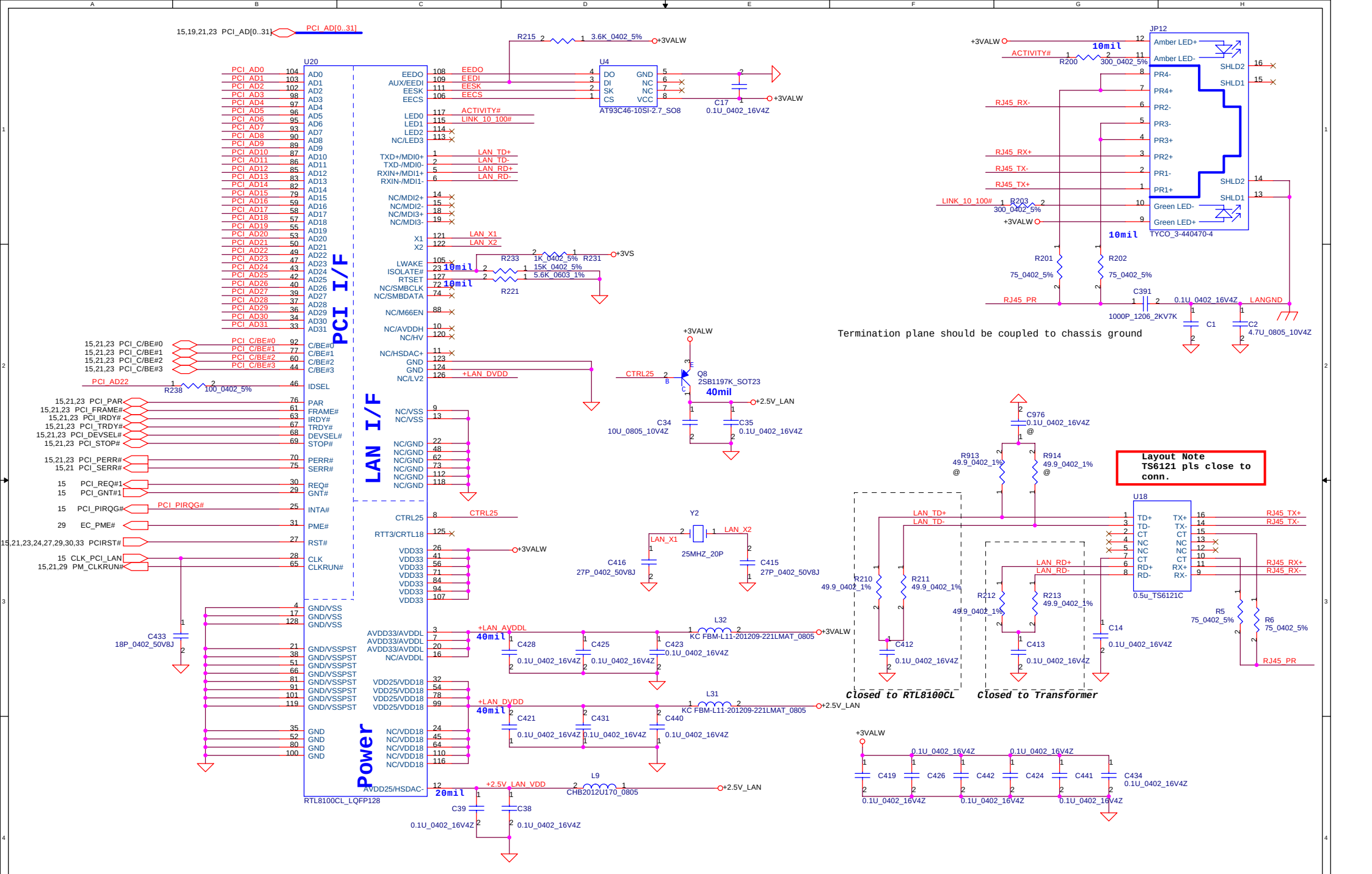
Compal Electronics, Inc.

Title: HARDWARE TRAP

Size: Custom | Document Number: MAYAA (LA-3391P) | Rev: 1.0

Date: Friday, November 03, 2006 | Sheet 19 of 48



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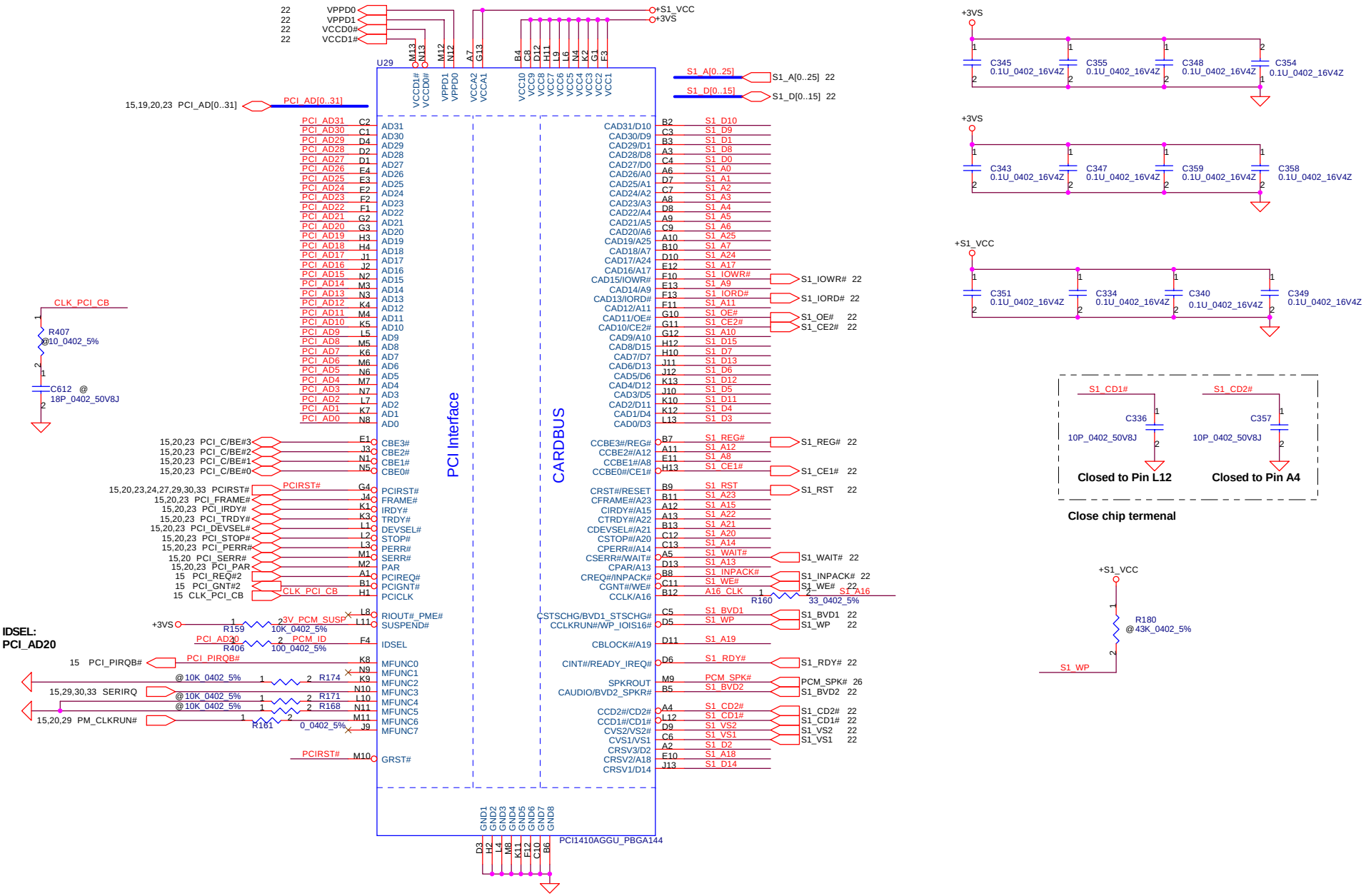
Compal Electronics, Inc.

Title: RTL8100CL

Size: B | Document Number: IAYAA (LA-3391P) | Rev: 1.0

Date: Friday, November 03, 2006 | Sheet 20 of 48



Security Classification	Compal Secret Data		
Issued Date	2006/05/18	Deciphered Date	2007/10/25

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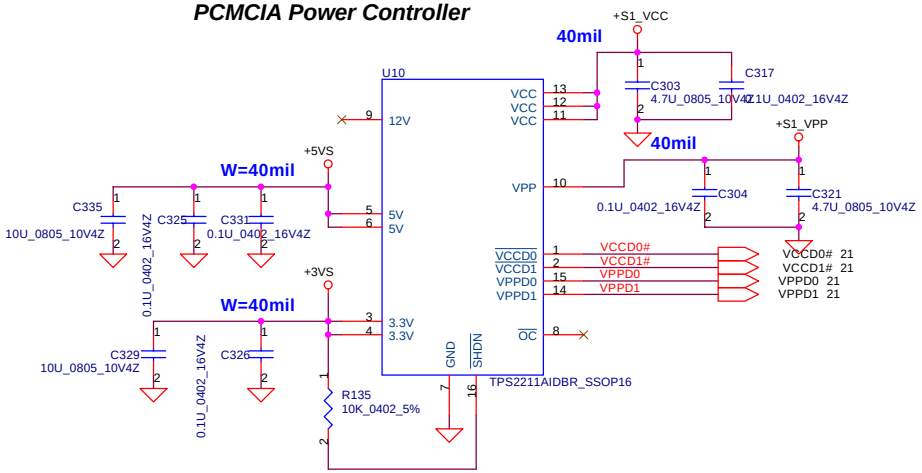
Compal Electronics, Inc.

Title: ENE-CB1410

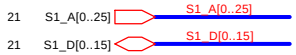
Size: B | Document Number: IAYAA (LA-3391P) | Rev: 1.0

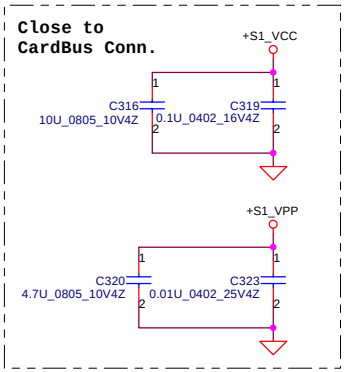
Date: Friday, November 03, 2006 | Sheet 21 of 48

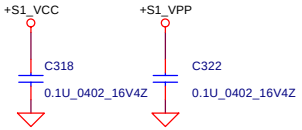
PCMCIA Power Controller

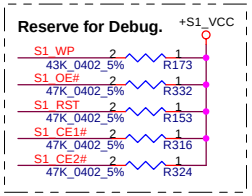


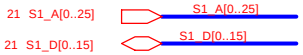
CardBus Socket



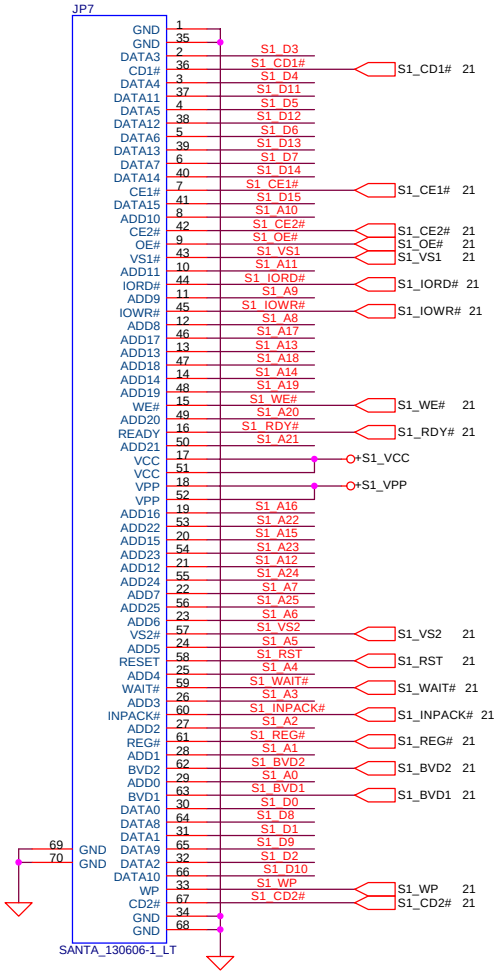








CardBus Socket



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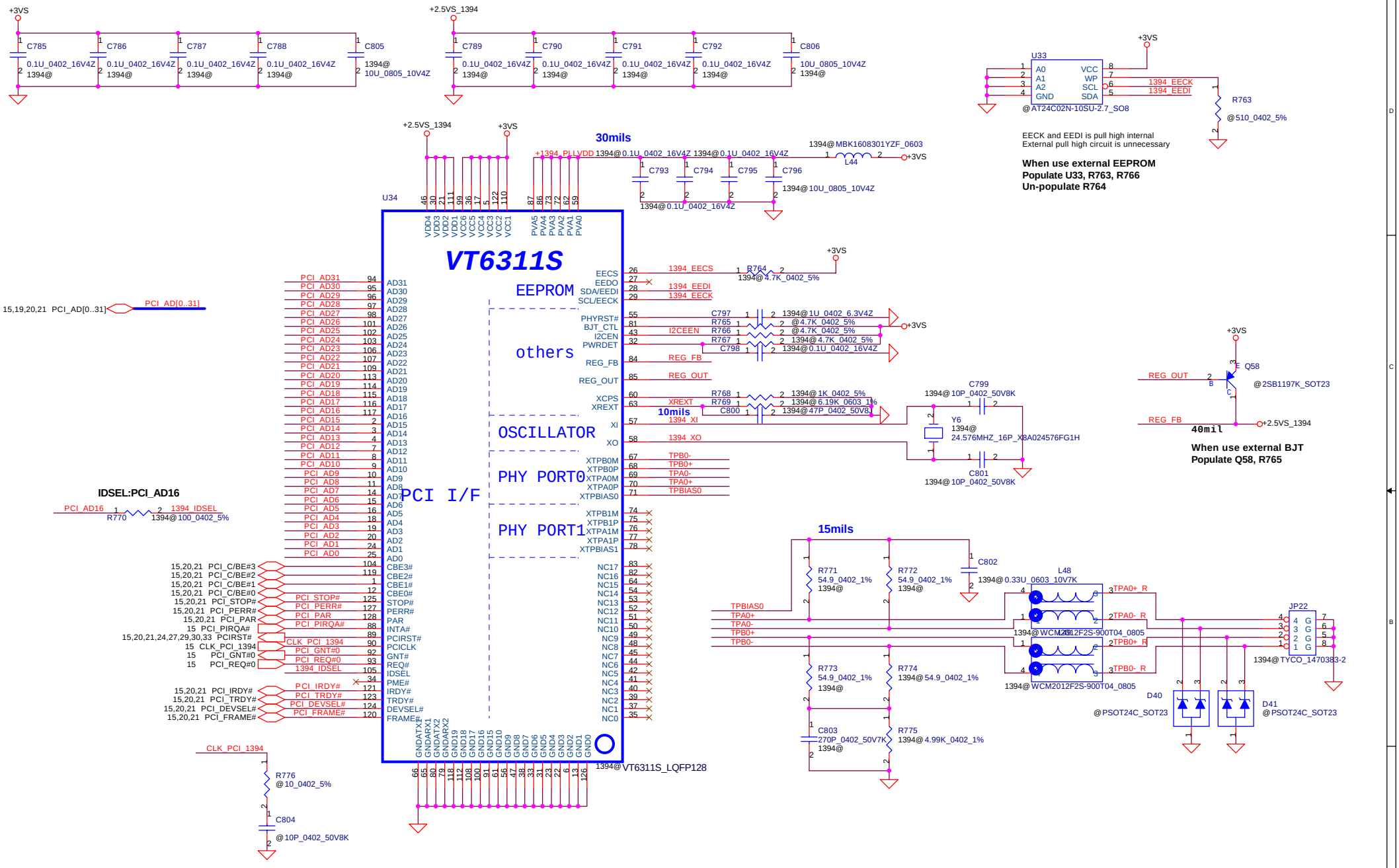
Compal Electronics, Inc.

Title: CARD BUS SOCKET

Size: B | Document Number: IAYAA (LA-3391P) | Rev: 1.0

Date: Friday, November 03, 2006 | Sheet 22 of 48



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Issued Date	2006/05/18	Deciphered Date	2007/10/25

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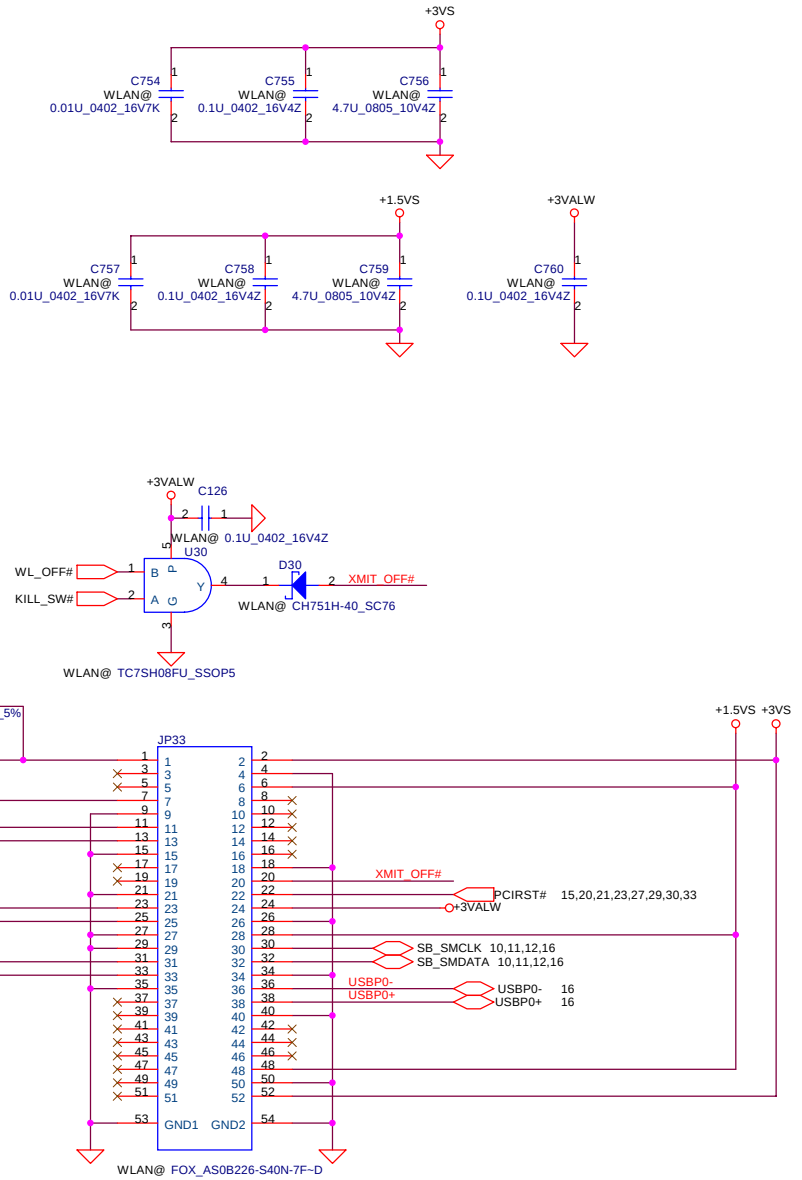
Compal Electronics, Inc.

Title: IEEE1394 VIA VT6311S

Size: B | Document Number: IAYAA (LA-3391P) | Rev: 1.0

Date: Friday, November 03, 2006 | Sheet 23 of 48



Mini-Express Card

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2006/05/18	Deciphered Date	2007/10/25	Title: MINI PCI SLOT
				Size: B; Document Number: IAYAA (LA-3391P); Rev: 1.0
				Date: Friday, November 03, 2006; Sheet 24 of 48

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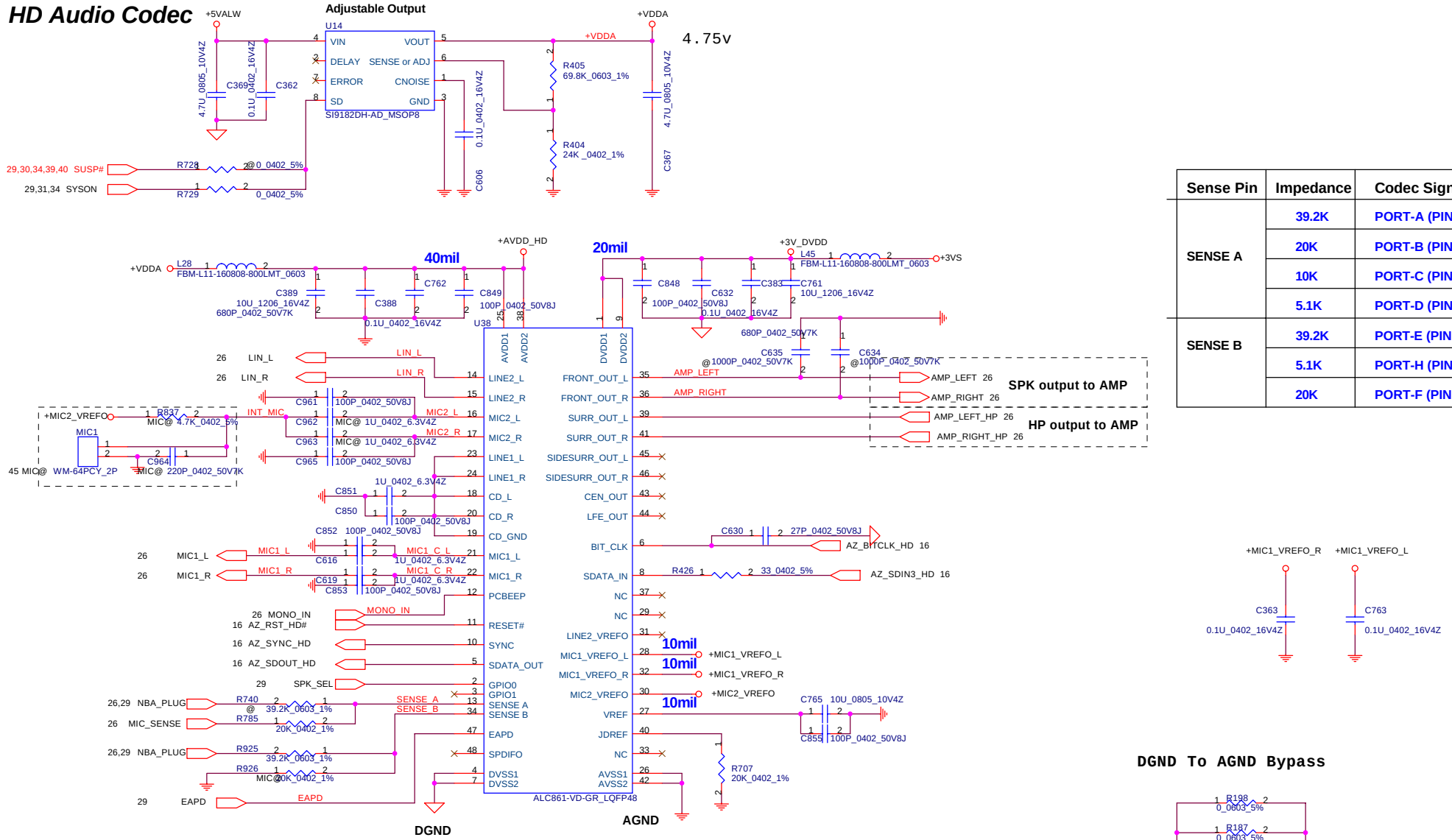
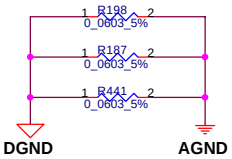
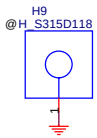
HD Audio Codec



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	5.1K	PORT-H (PIN 45, 46)
	20K	PORT-F (PIN 16, 17)

DGND To AGND Bypass





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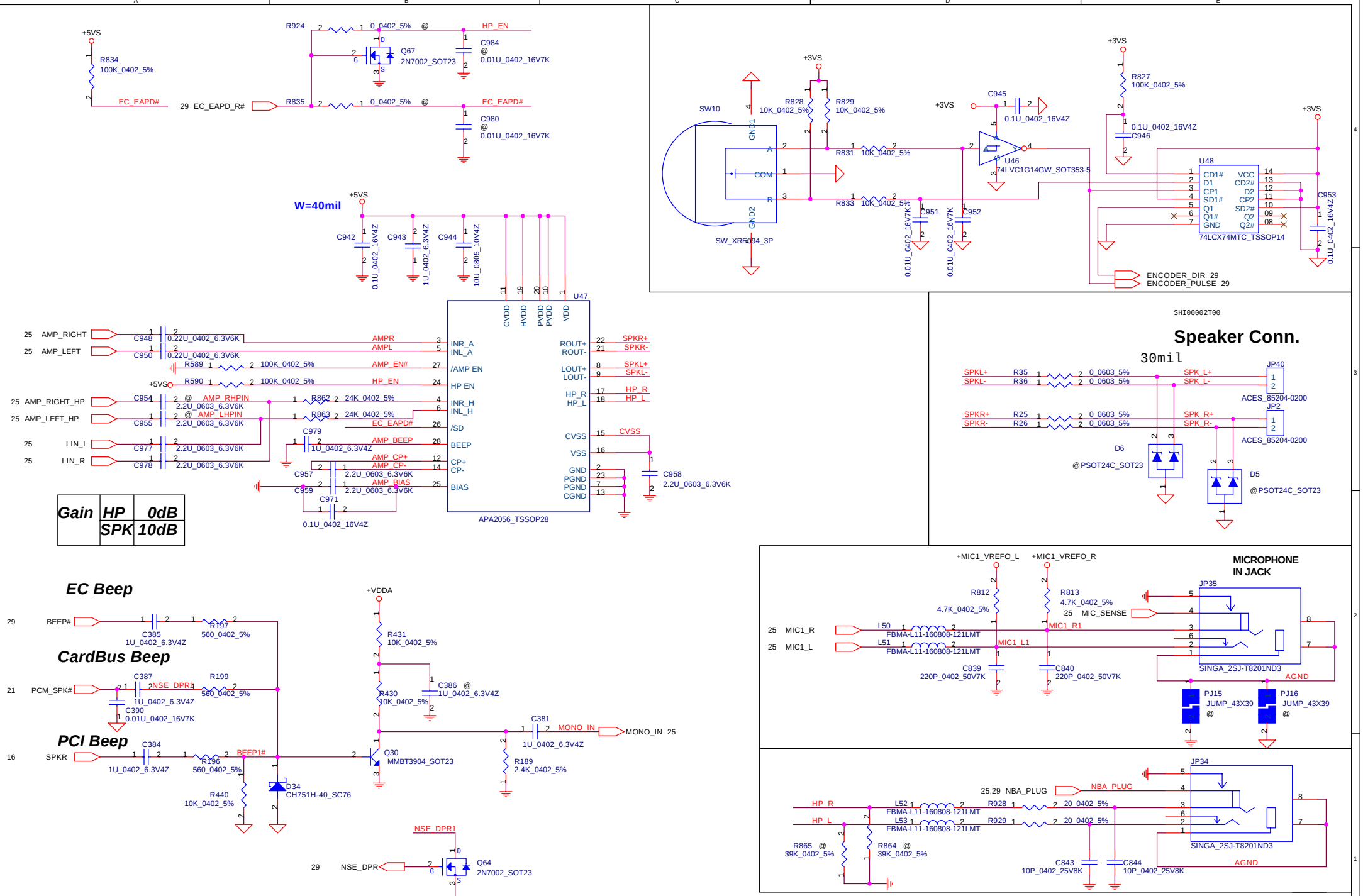
Compal Electronics, Inc.

Title: HD CODEC ALC861D

Size: B | Document Number: IAYAA (LA-3391P) | Rev: 1.0

Date: Friday, November 03, 2006 | Sheet 25 of 48



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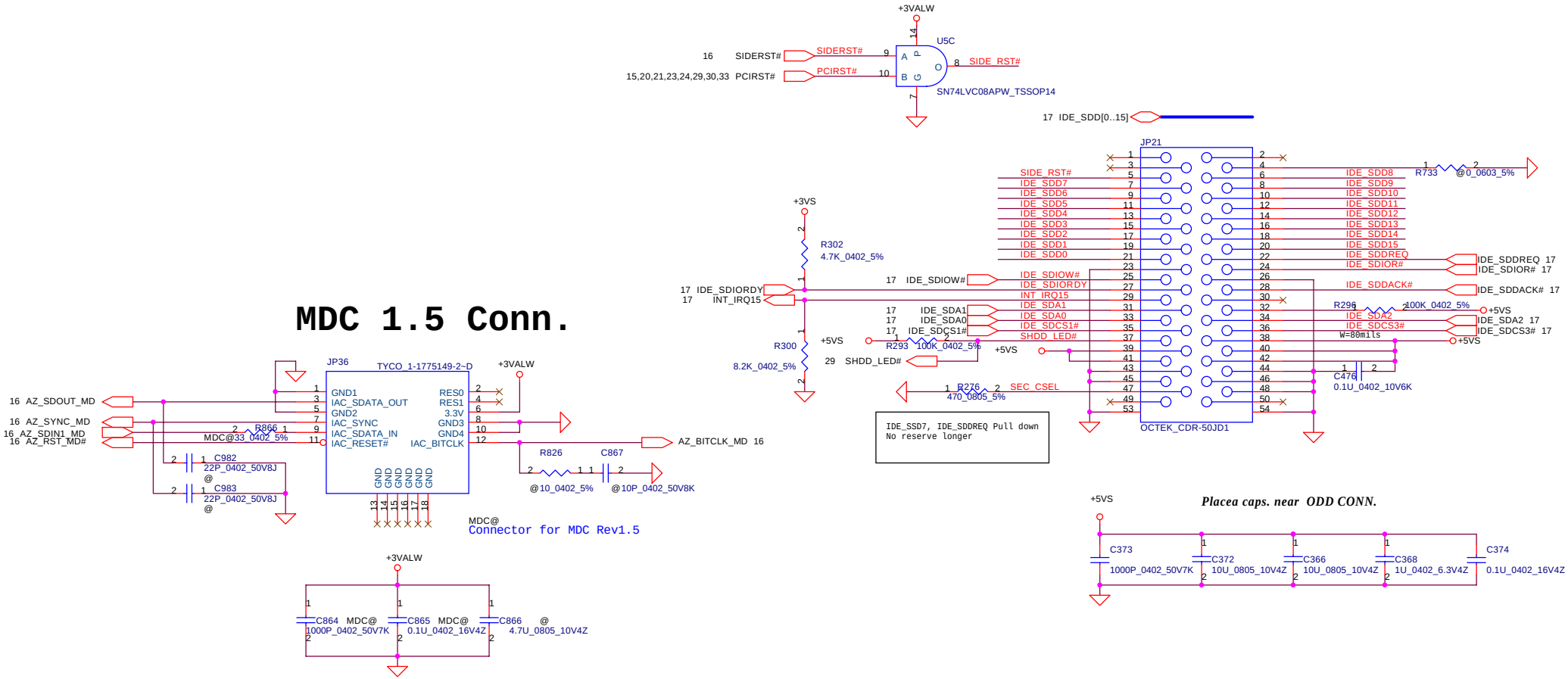
Compal Electronics, Inc.

Title: AMP&Audio Jack/MDC

Size: B | Document Number: IAYAA (LA-3391P) | Rev: 1.0

Date: Friday, November 03, 2006 | Sheet 26 of 48

MDC 1.5 Conn.



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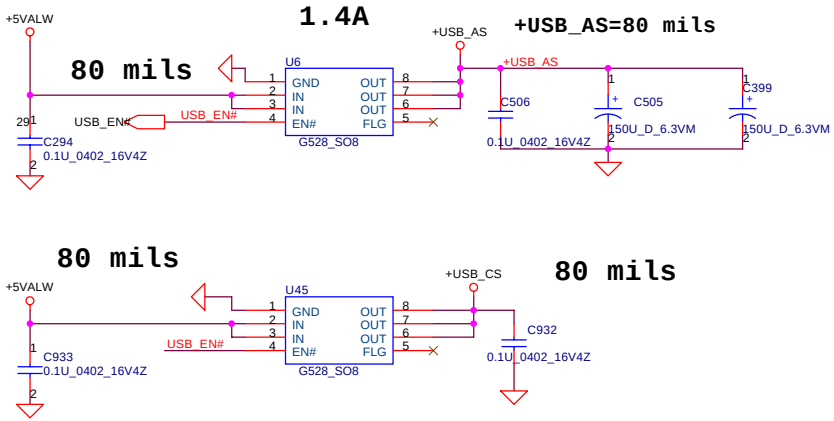
Compal Electronics, Inc.

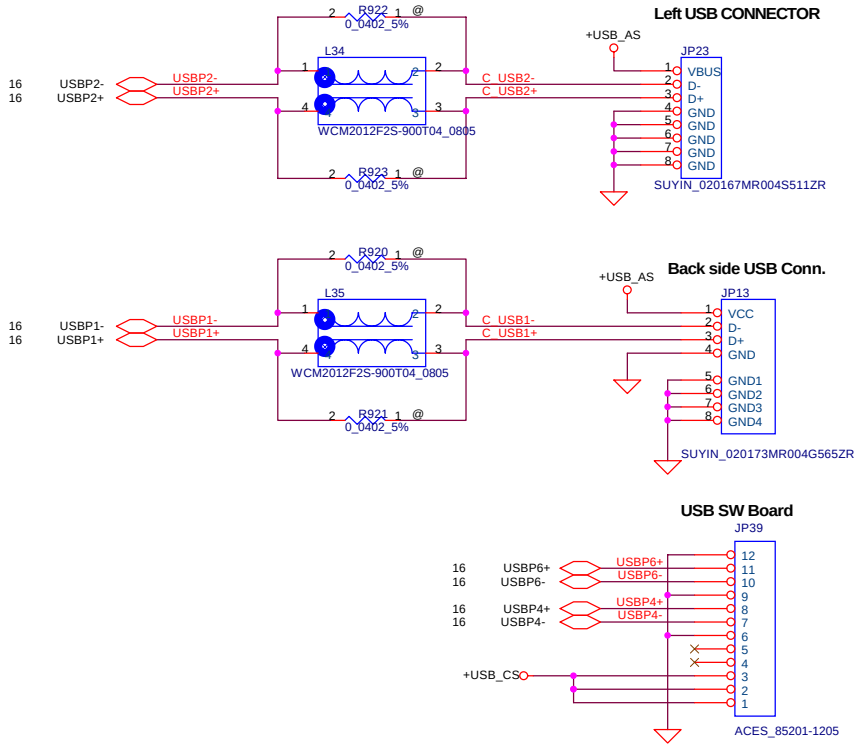
Title: TPM/ ODD CONNECTORS

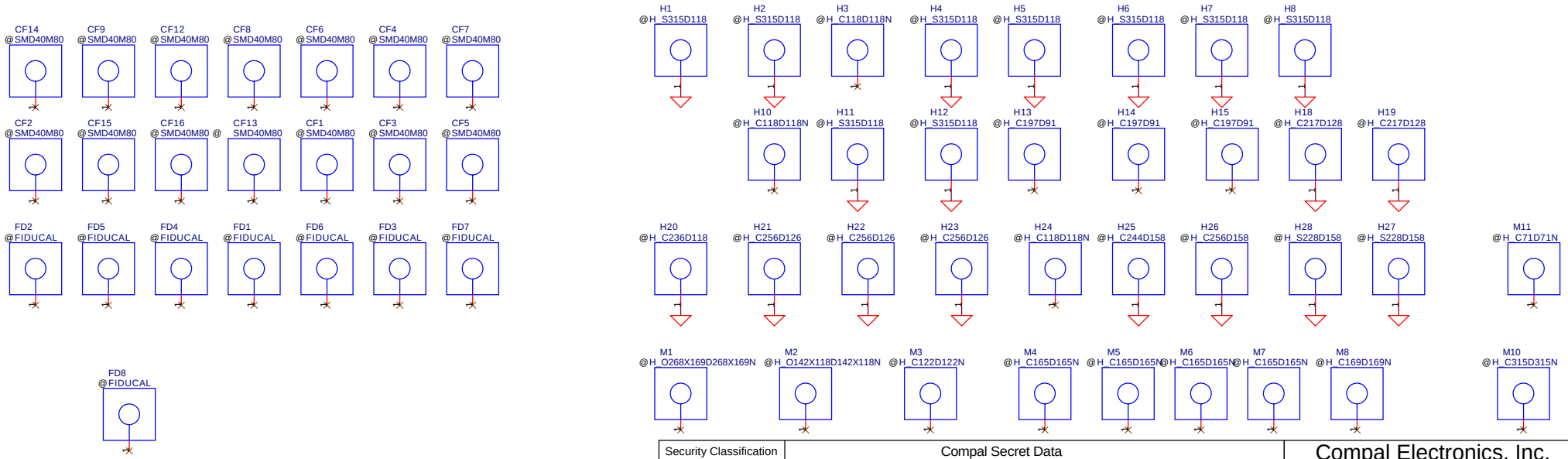
Size	Document Number	Rev
B	IAYAA (LA-3391P)	1.0

Date: Friday, November 03, 2006 | Sheet 27 of 48

Keep 20 mils minimum spacing between
USB signals and others signals







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Issued Date	2006/05/18	Deciphered Date	2007/10/25

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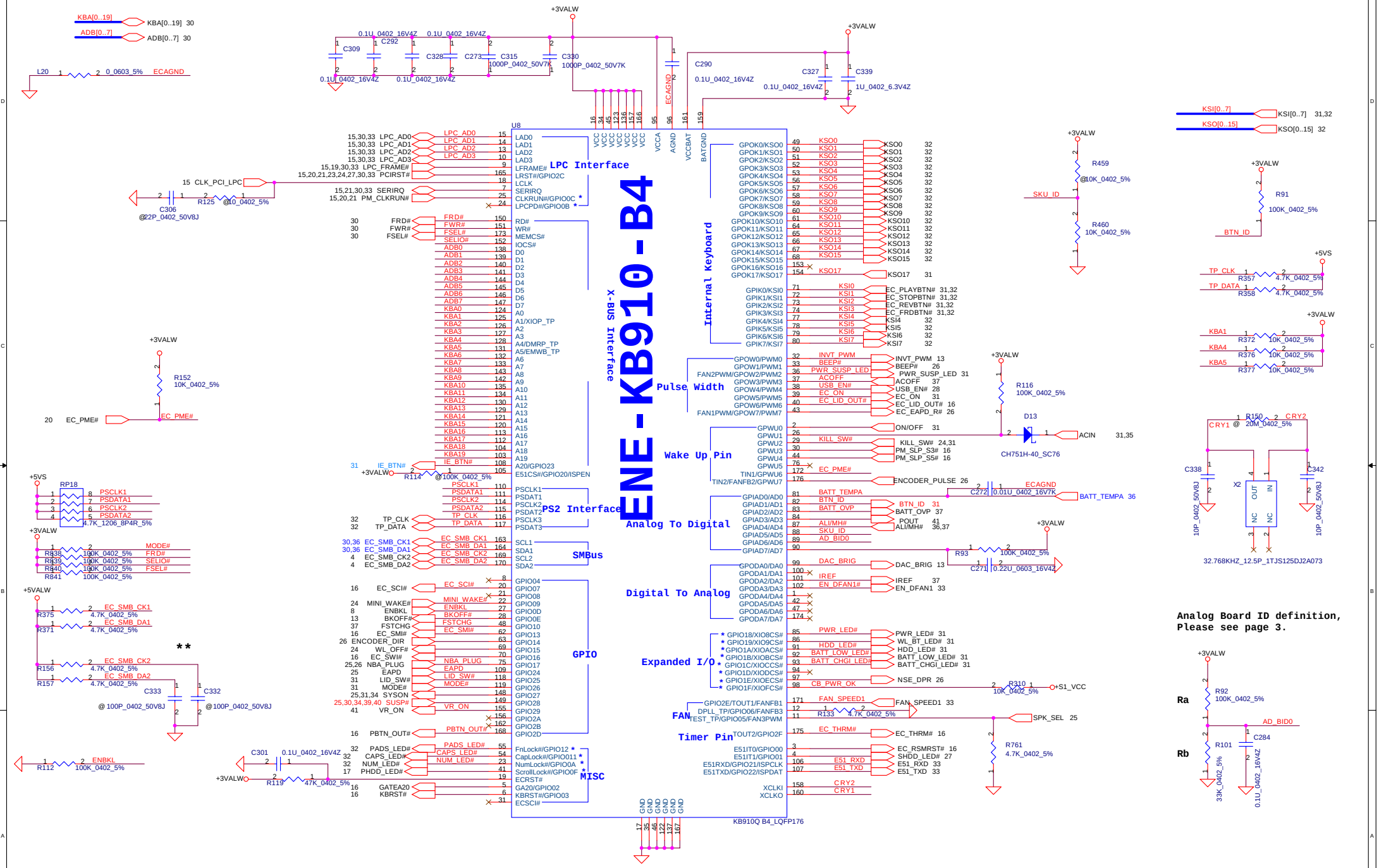
Compal Electronics, Inc.

Title: USB Conn.

Size	Document Number	Rev
B	IAYAA (LA-3391P)	1.0

Date: Friday, November 03, 2006 | Sheet 28 of 48


ENE-KB910-B4
U8
LPC Interface
X-BUS Interface
Internal Keyboard
Pulse Width
Wake Up Pin
Analog To Digital
PS2 Interface
SMBus
Digital To Analog
GPIO
Expanded I/O
FAN
Timer Pin
MISC
KB910Q B4_LQFP176
KBA[0..19]
ADB[0..7]
KSI[0..7]
KSO[0..15]
+3VALW
+5VS
ECAGND
Analog Board ID definition,
Please see page 3.
Ra
Rb
Security Classification
Compal Secret Data
Issued Date
2006/05/18
Deciphered Date
2007/10/25
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Title
ENE-KB910
Size
Custom
Document Number
MAYAA (LA-3391P)
Rev
1.0
Date:
Friday, November 03, 2006
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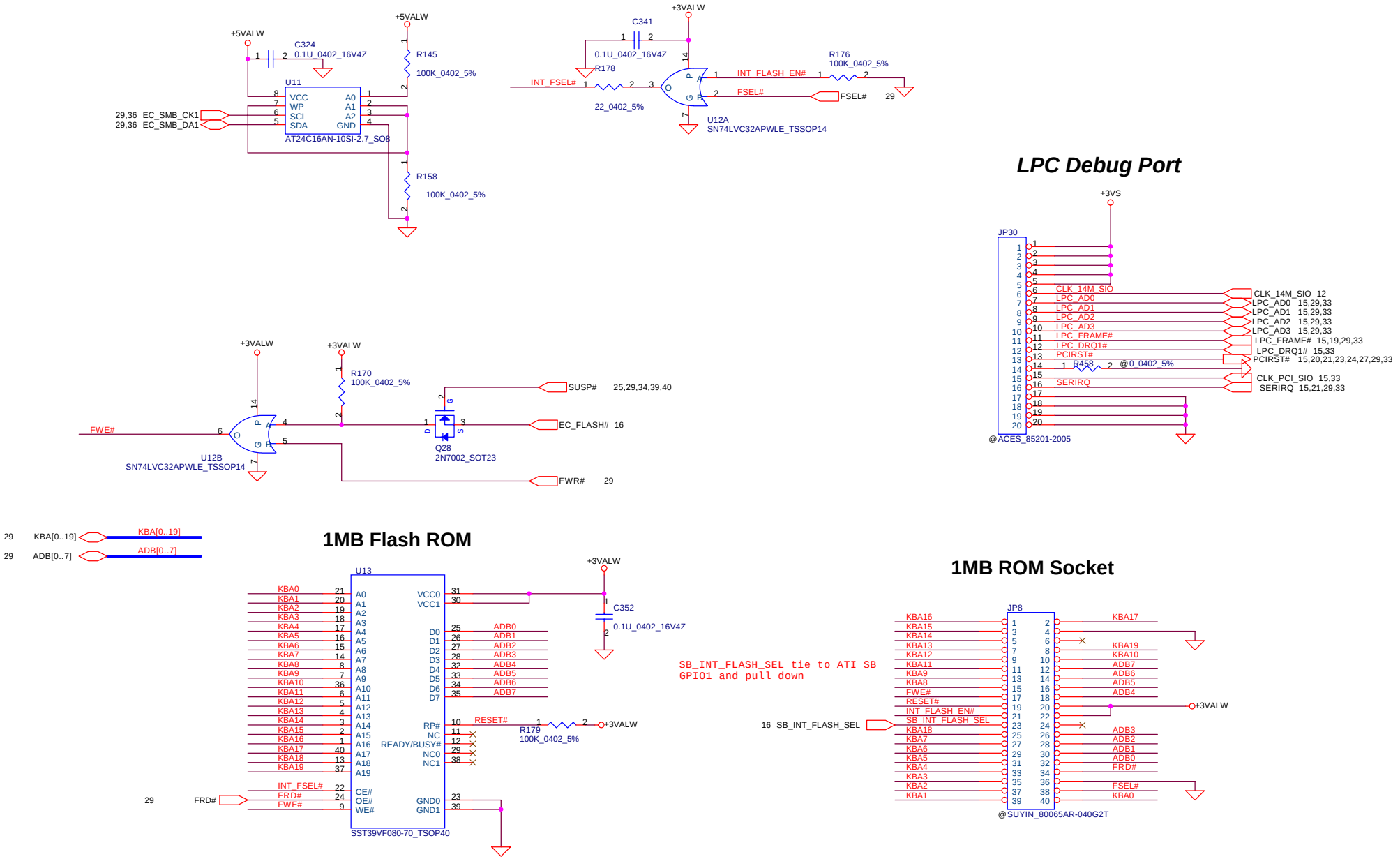
29
of
48



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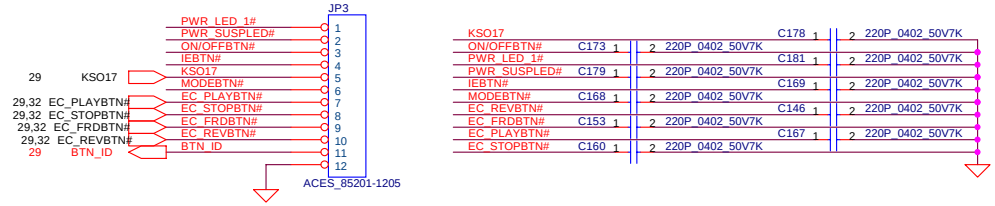
Compal Electronics, Inc.

Title: BIOS& I/O PORT

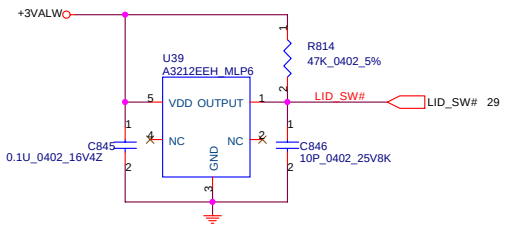
Size: B | Document Number: IAYAA (LA-3391P) | Rev: 1.0

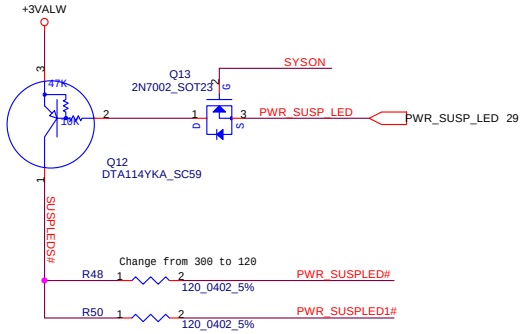
Date: Friday, November 03, 2006 | Sheet 30 of 48

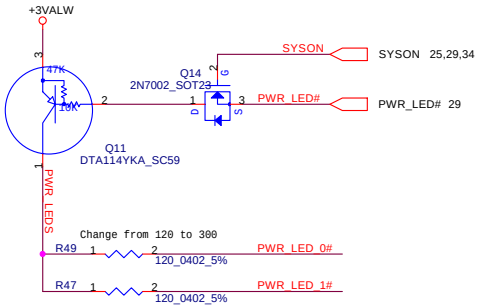
Switch Board Conn.



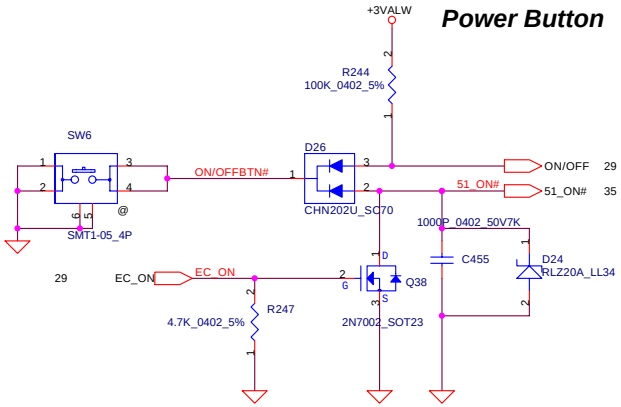
LID Switch

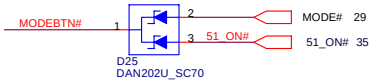


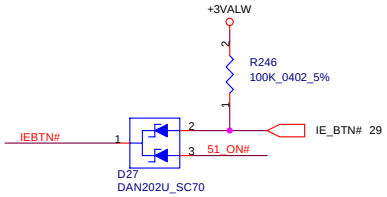




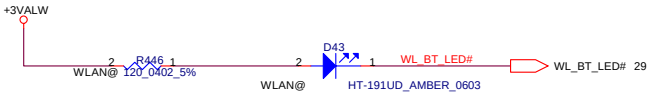
Power Button



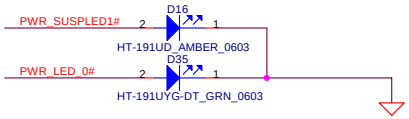




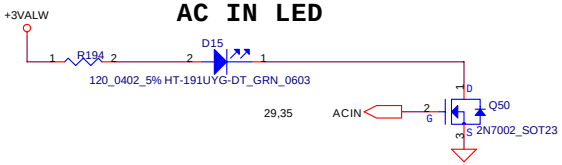
WL&BT LED



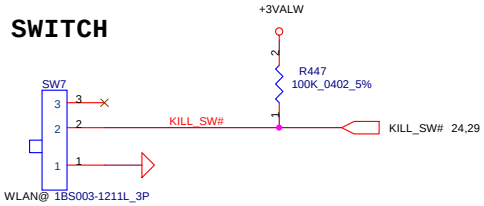
POWER/ON LED



AC IN LED



Kill SWITCH



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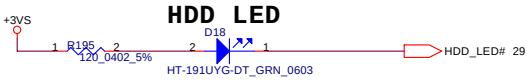

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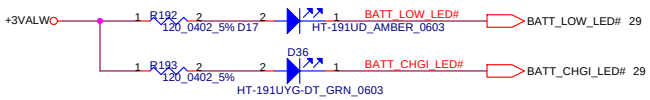

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Issued Date	2006/05/18	Deciphered Date	2007/10/25

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Compal Electronics, Inc.

Title: Kill SW/ Sub Conn./LEDS

Size: Custom | Document Number: AYAA (LA-3391P) | Rev: 1.0

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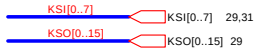
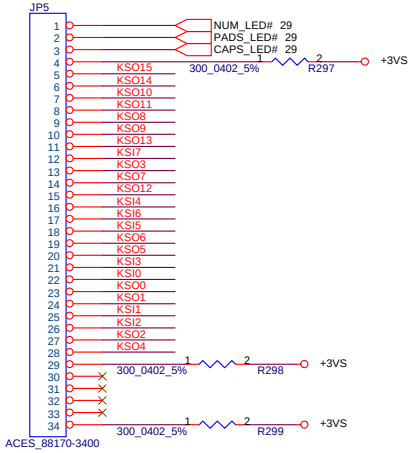
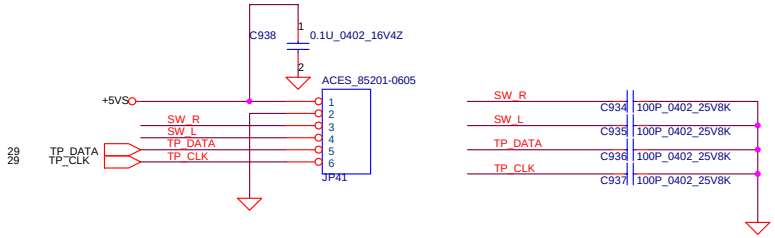


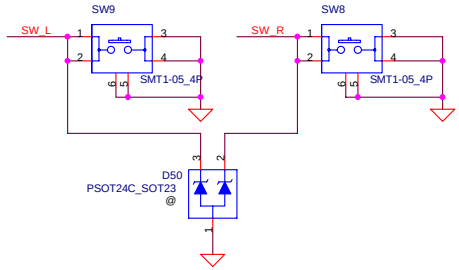
INT_KBD CONN.

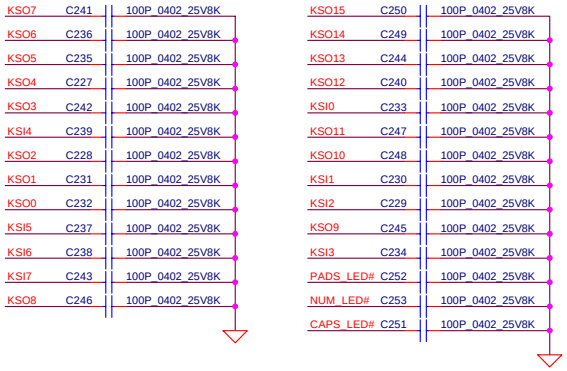


TP Conn.



T/P Button





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Issued Date	2006/05/18	Deciphered Date	2007/10/25

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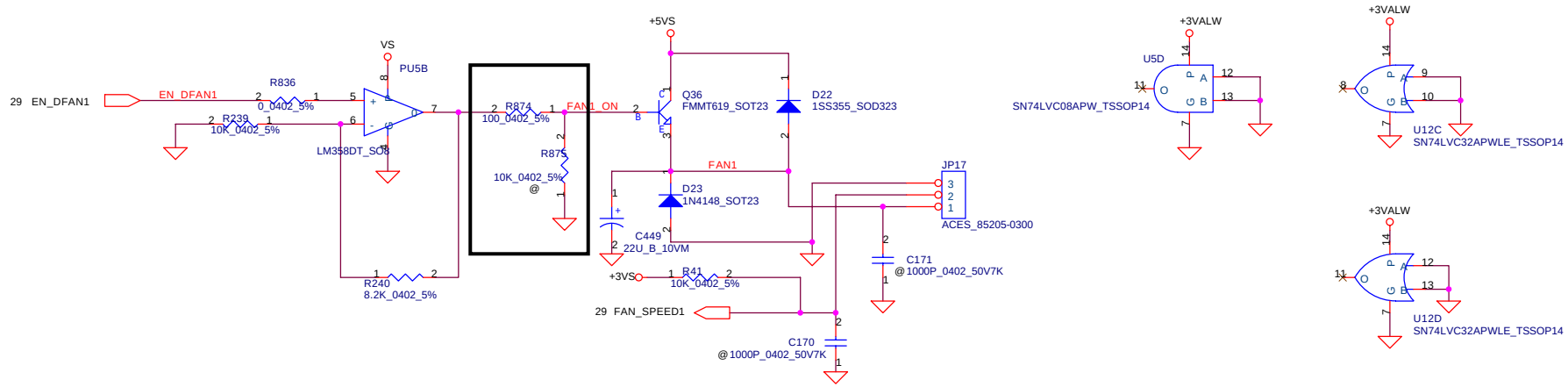
Compal Electronics, Inc.

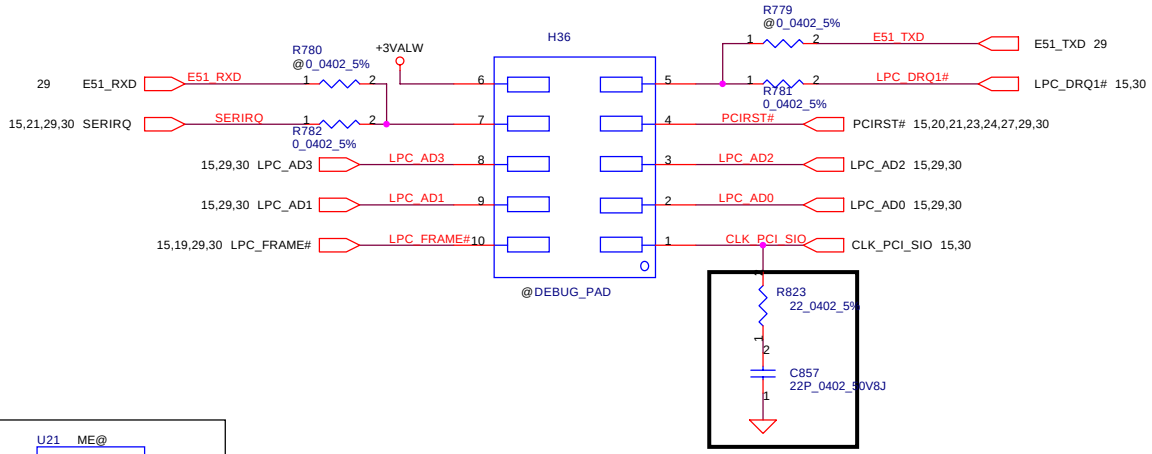
Title: KB/Touch Pad& hibernation

Size: Custom | Document Number: IAYAA (LA-3391P) | Rev: 1.0

Date: Friday, November 03, 2006 | Sheet 32 of 48

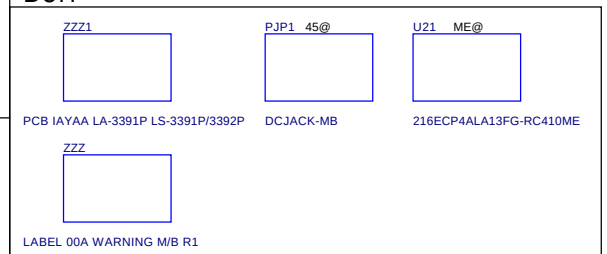
FAN Conn





LPC Debug card

BOM



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Compal Electronics, Inc.

Title: FAN & MDC

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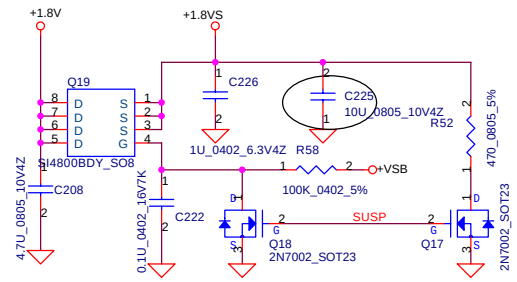
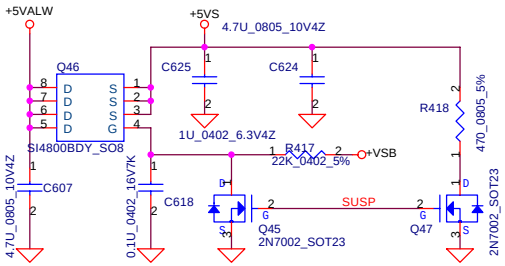
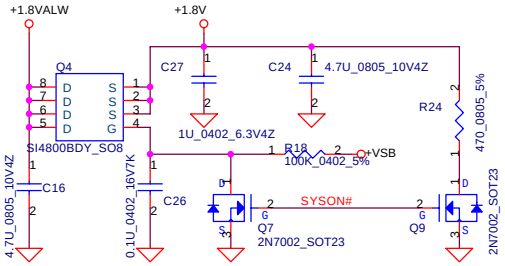
+1.8V TO +1.8VS

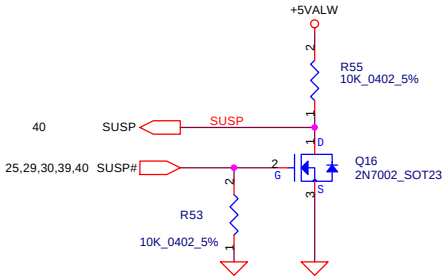


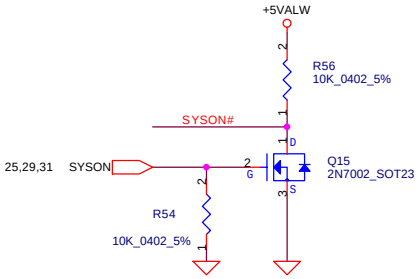
+5VALW TO +5VS



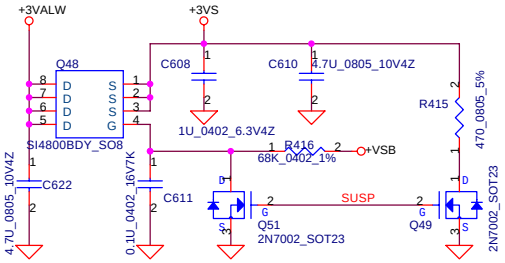
+1.8VALW TO +1.8V

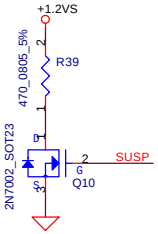


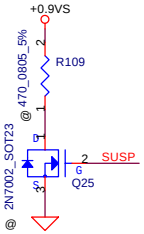




+3VALW TO +3VS







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Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size: B | Document Number: IAYAA (LA-3391P) | Rev: 1.0

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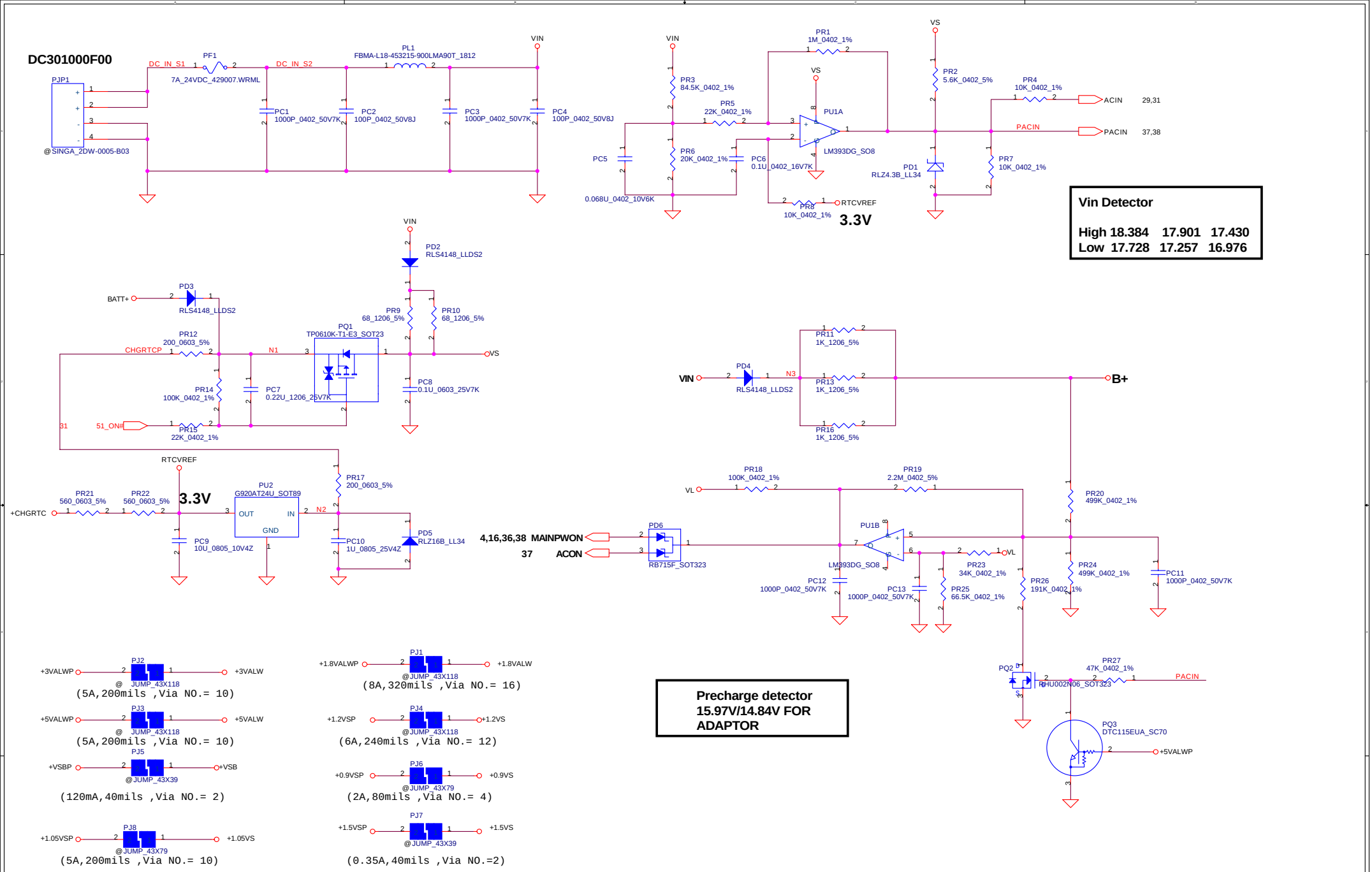

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Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size | Document Number | Rev 1.0

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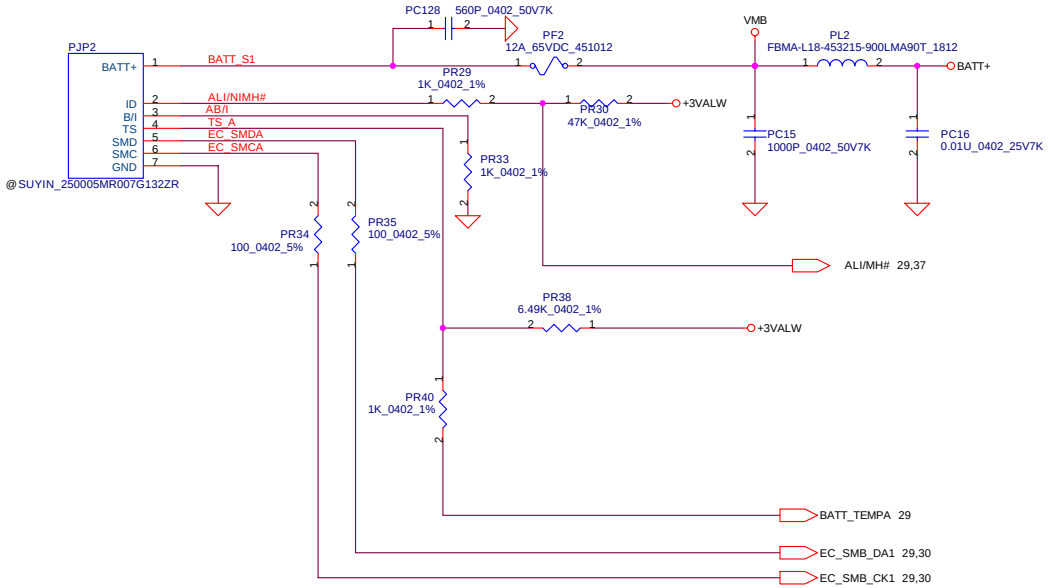
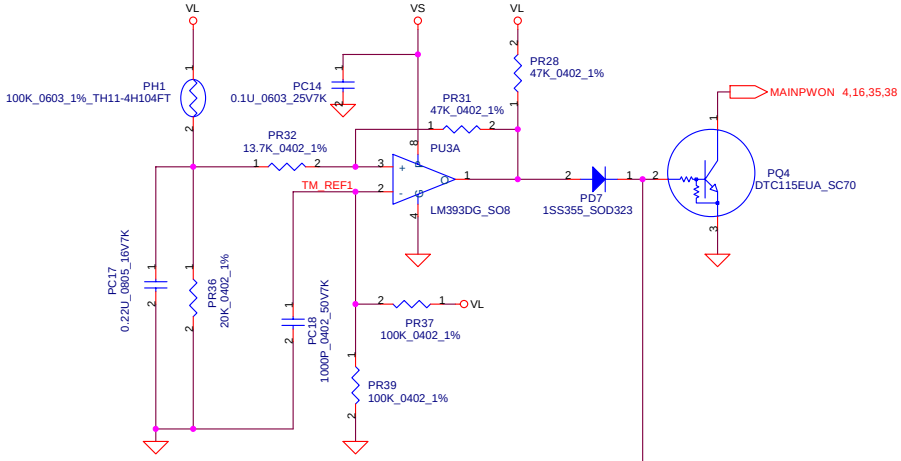
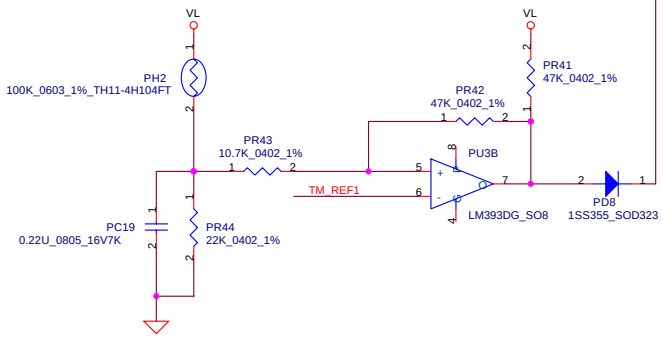
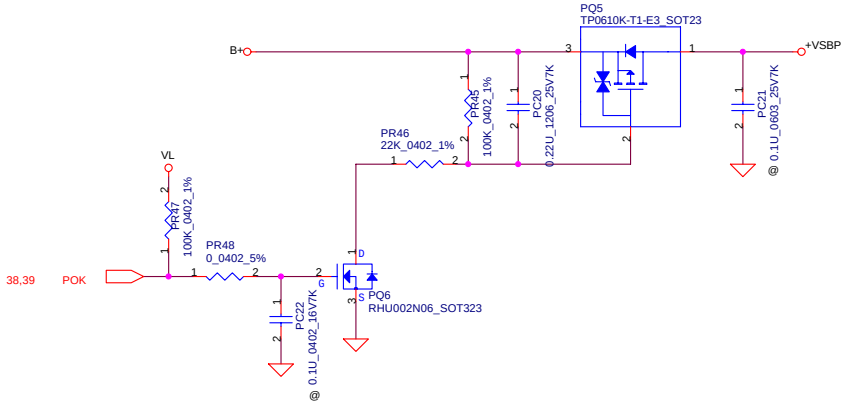
PH1 under CPU botten side :
CPU thermal protection at 87 degree C
Recovery at 48 degree C





PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C





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Compal Electronics, Inc.

Title: BATTERY CONN / OTP

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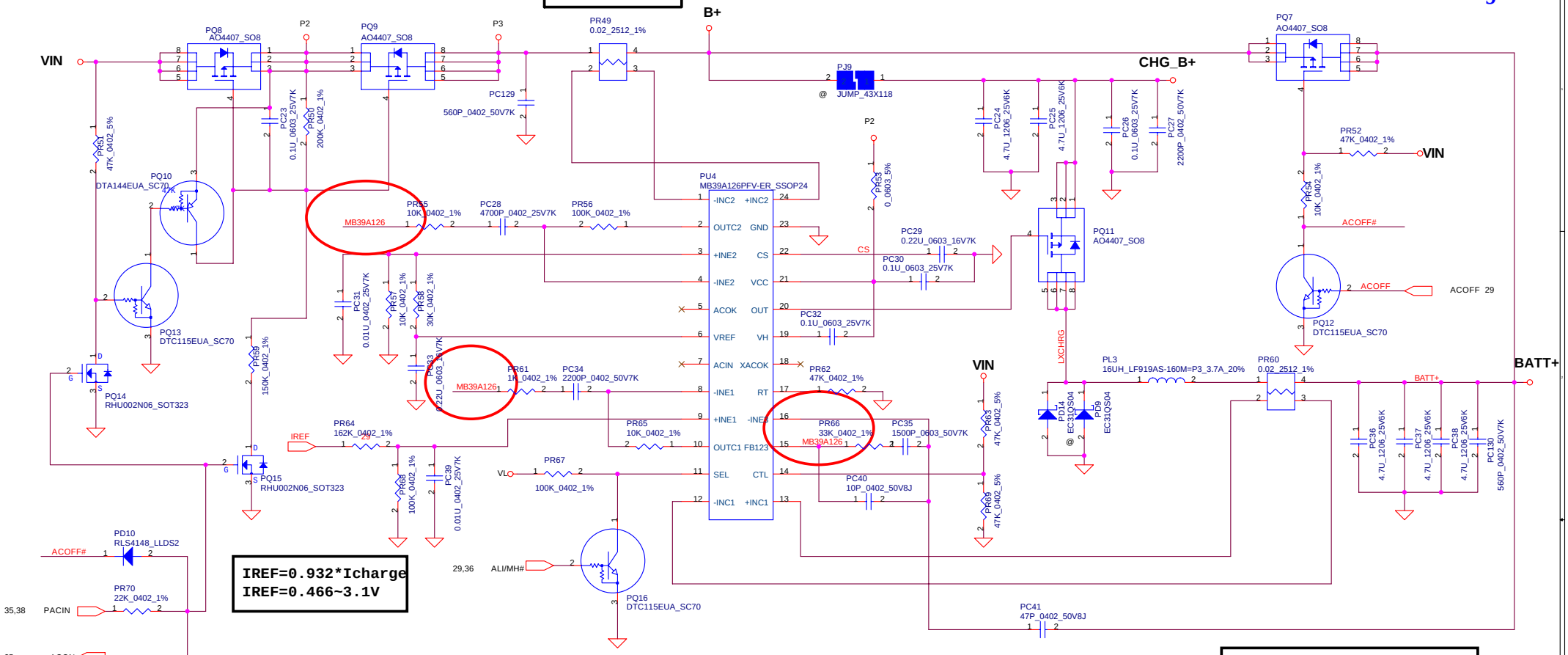
Date: Friday, November 03, 2006 | Sheet 36 of 48

Charger

Iadp=0~3.125A

Fosc=14100/Rt=14100/47=300KHz



IREF=0.932*Icharge
IREF=0.466~3.1V

Charge voltage
3S CC-CV MODE : 12.6V (SEL=L , ALI/MH#=3.3V)
4S CC-CV MODE : 16.8V (SEL=H , ALI/MH#=0V)

CC=3A , IREF=3.144V
(100K/(100K+162K))*3.144V=1.2V
1.2/(20*0.02)=3A

CP Point=3.125A
5V*(10K/(30k+10k))=1.25V
1.25V/(20*0.02)=3.125A

LI-3S :13.5V----BATT-OVP=1.5V
LI-4S :18V----BATT-OVP=2V
BATT-OVP=0.111*BATT+

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Compal Electronics, Inc.

Title: CHARGER

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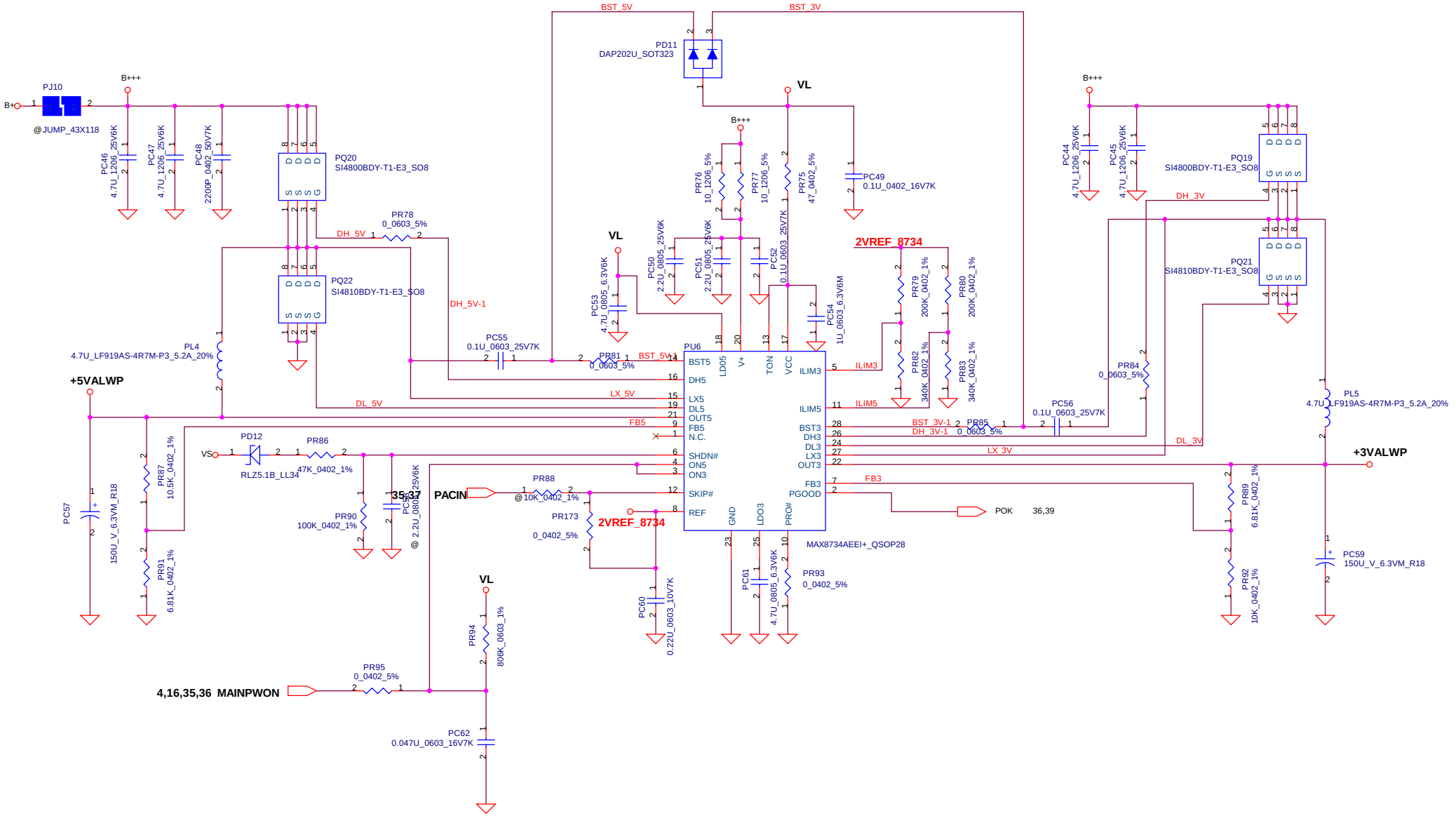
Date: Friday, November 03, 2006 | Sheet 37 of 48

+3.3VALWP/+5VALWP



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Compal Electronics, Inc.

Title: +5V/+3V

Size: Custom | Document Number: IAYAA (LA-3391P) | Rev: 1.0

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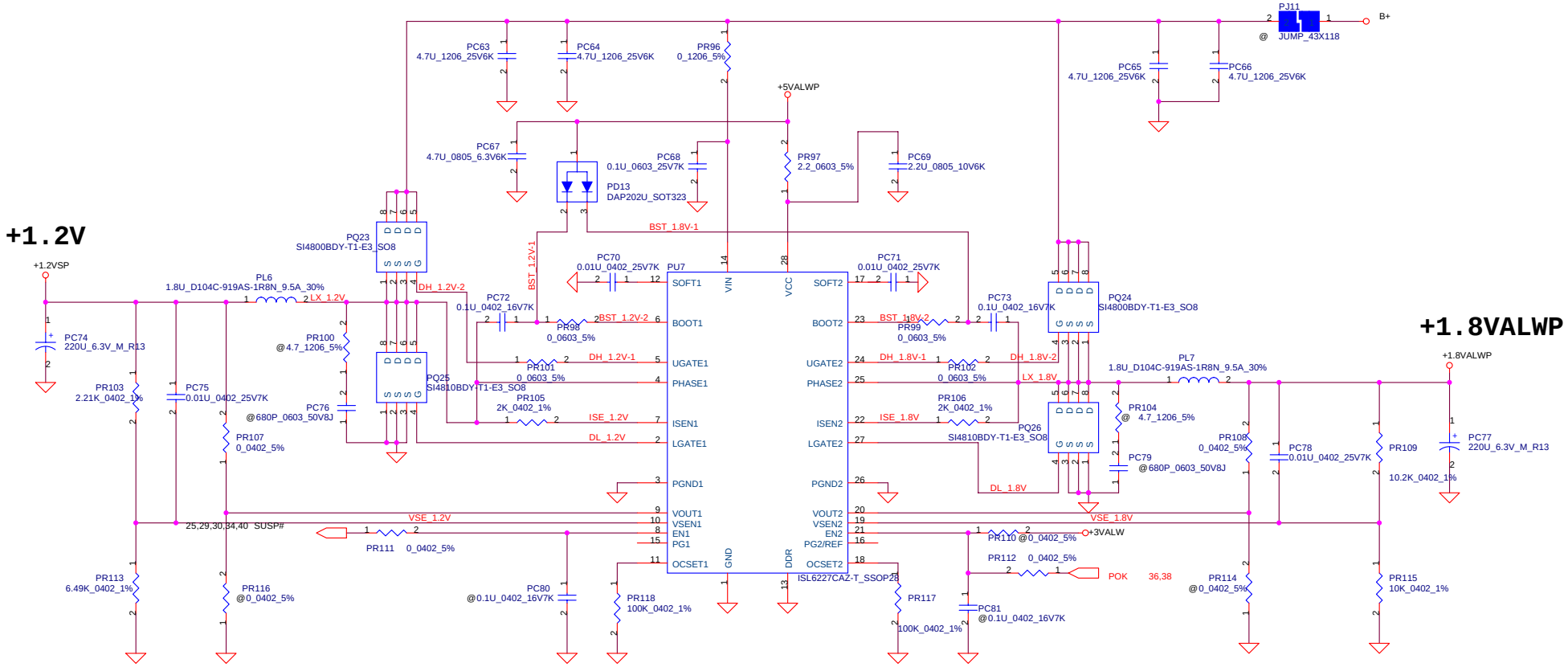

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Compal Electronics, Inc.

Title: 1.8V / 1.2V

Size | Document Number | Rev 1.0

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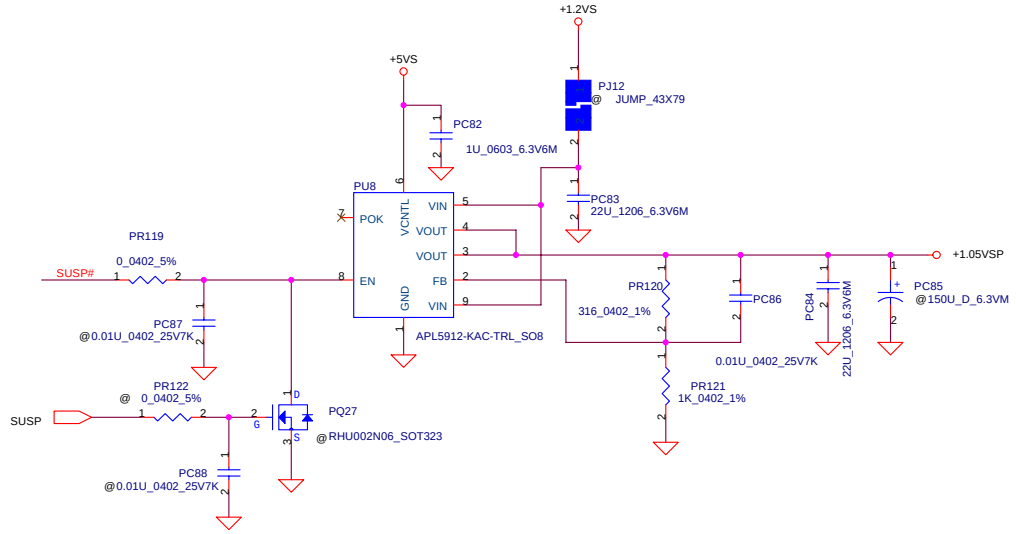

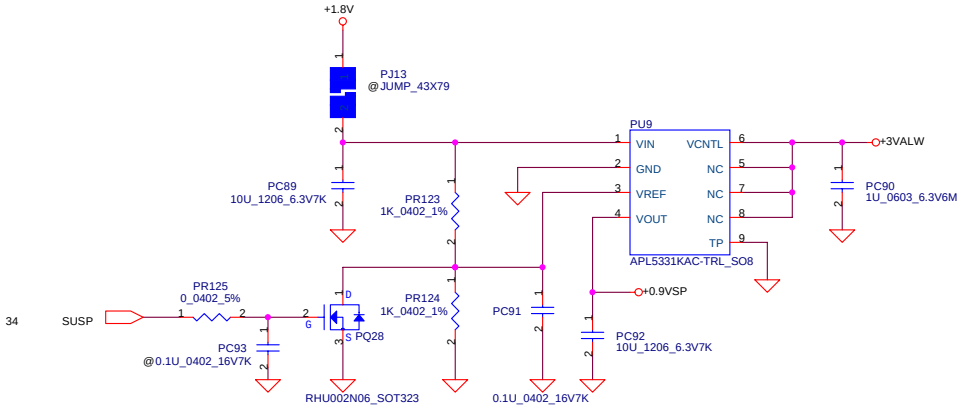

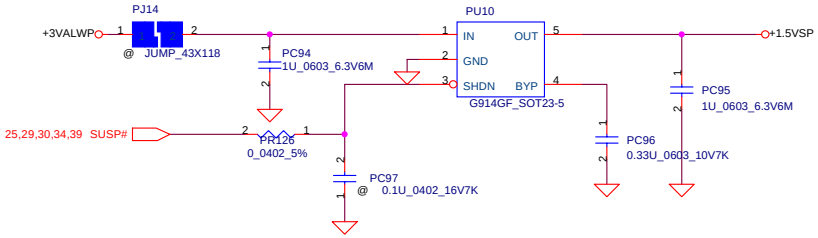

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Compal Electronics, Inc.

Title: 1.05V / 0.9V / 1.5V

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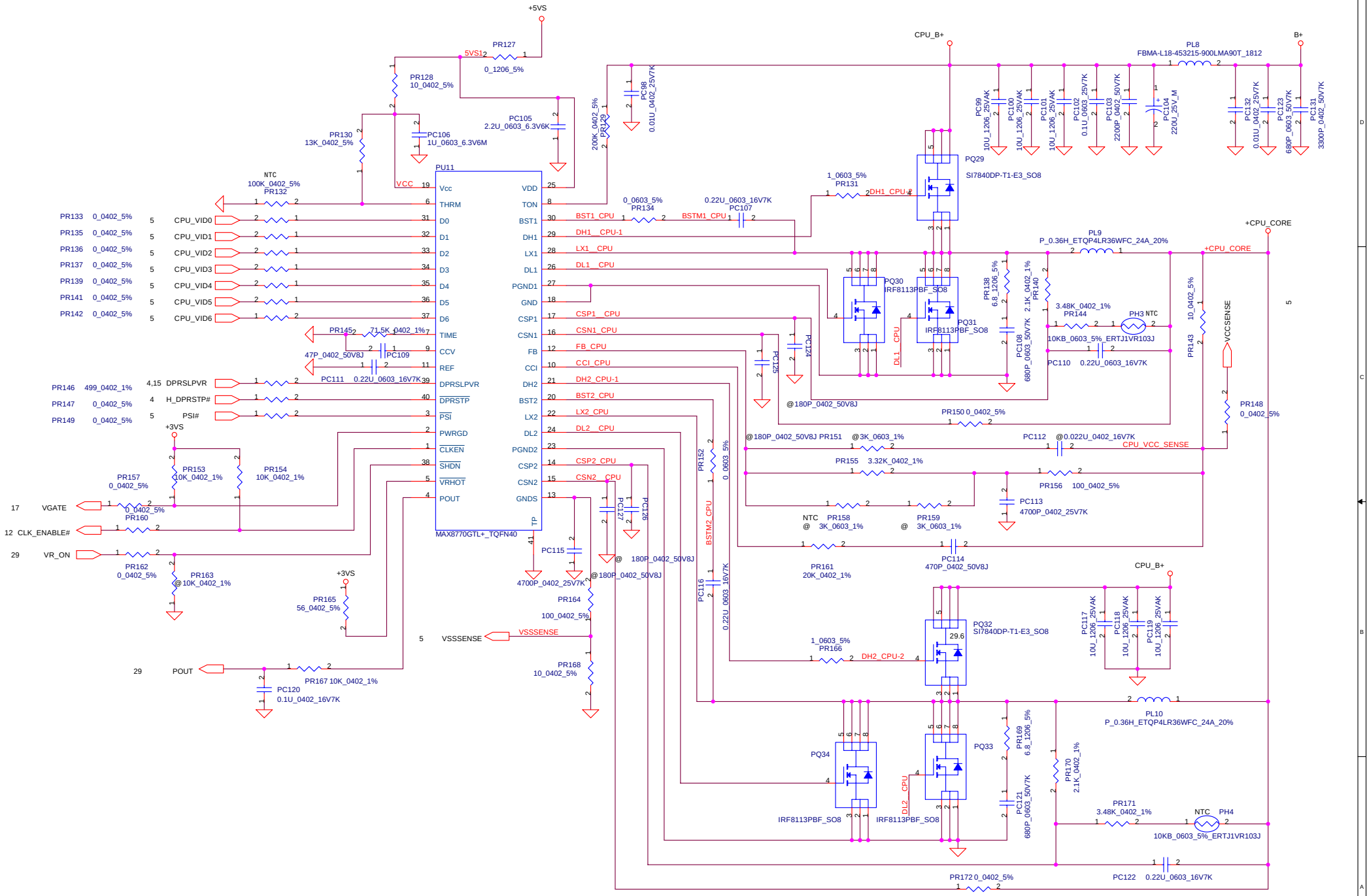

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Compal Electronics, Inc.

Title: **+CPU_CORE**

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Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
8	Net connection	U21.AG30 (MEM_ODT0)	DDR_ODT0	NC	DDR 667 workaround, ATI recommend (PA_RS400R2)	0.2	
		U21.AE28 (MEM_ODT1)	DDR_ODT1	NC			
		U21.AC30 (MEM_ODT2)	DDR_ODT2	NC			
		U21.Y30 (MEM_ODT3)	DDR_ODT3	NC			
10	Net connection	JP16.80 (DIMMA_CKE1)	DDR_SCKE1	DDR_SCKE0			
11	Net connection	JP15.79 (DIMMB_CKE0)	DDR_SCKE2	DDR_SCKE1			
		JP15.79 (DIMMB_CKE1)	DDR_SCKE3	DDR_SCKE1			
10	Net connection	JP16.114 (DIMMA_ODT0)	DDR_ODT0	DDR_SCKE2			
		JP16.119 (DIMMA_ODT1)	DDR_ODT2	GND			
		JP15.114 (DIMMB_ODT0)	DDR_ODT1	DDR_SCKE3			
		JP16.119 (DIMMB_ODT1)	DDR_ODT3	GND			
		RP1.4 (CKE3 PU)	DDR_SCKE3	NC			
		RP1.1 (CKE2 PU)	DDR_SCKE2	NC			
		RP4.4 (ODT3 PU)	DDR_ODT3	NC			
		RP14.3 (ODT0 PU)	DDR_ODT0	DDR_SCKE2			
		RP14.2 (ODT1 PU)	DDR_ODT1	DDR_SCKE3			
	Del part	R40 (ODT2 PU)	56_0402_5%	_____			
	Add part	R12 (CKE2 PD)	_____	180_0402_5%			
		R17 (CKE3 PD)	_____	180_0402_5%			
9	Change part	C70, C68, C63, C62, C51	0.1U_0402_6.3V4Z	1U_0402_6.3V4Z	VDDA_18 decoupling, ATI recommend	0.2	
15	Change part	C295, C298, C300, C305	0.1U_0402_6.3V4Z	0.01U_0402_16V7K	ALINK coupling cap for differential signal, ATI recommend	0.2	
16	Net connection	U9.A21(USB_HSDP1+)	USBP1-	USBP1+	Fix USB function fail	0.2	
		U9.B21(USB_HSDM1-)	USBP1+	USBP1-			
16	Net connection	R760.1 (MAINPWONR PU)	+3VS	+3VALW	For SB mainpwron (Gevent) is S5 power pin	0.2	
25	Net connection	R740.2 (PH sensor)	N17081292	NBA_PLUG	For audio jack change to normal open	0.2	
		R785 (Mic sensor)	N16810569	MIC_SENSE			
	Del part	R872, R873	0_0402_5%(@)	_____			
		R786, R842	100K_0402_5%	_____			
		Q59, Q67	2N7002_SOT23	_____			
	Change part	JP34, JP35	FOX_JA6033L-B5S3-7F	FOX_JA6333L-B3T0-7F			
26	Net connection	U47.16 (VSS)	GND	CVSS	Fix audio left channel no function	0.2	
29	Change part	R116	10K_0402_5%	100K_0402_5%	Fix BATT charge LED always light, for power workaround	0.2	

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15	Add part	D28	————	CH751H-40_SC76	For C3 pop-up and C1e HW rework. ATI recommend (PA_IXP400AC16)	0.2	
		R899	————	10K_0402_5%			
		C972	————	15P_0402_50V8D			
	Net connection	U9.D27 (SB BMREQ#)	BM_REQ#	SB_BM_REQ#			
15	Change part	U36	TC7SH00FU_SSOP5	74LVC1G14GW_SOT353-5	C4 timing on Yonah-M platforms workaround, ATI recommend (PA_IXP400BR4)	0.2	
		R802	200K_0402_5%(@)	150K_0402_5%			
	Add part	R900, R901	————	10K_0402_5%			
		C973	————	330P_0402_50V7J			
		D29	————	CH751H-40_SC76			
		Q6	————	MMBT3904_SOT23			
		Q1	————	2N7002_SOT23			
		R902	————	0_0402_5%			
	Net connection	U9.E29 (SB STPCLK#)	H_STPCLK#	SB_STPCLK#			
	BOM Structure	Q62, U36, C832, C833, D42	@	————			
12	Change part	R255	0_0402_5%	4.7K_0402_5%			
	BOM Structure	C831	@	————			
7,8,9	Change part	U21	216CPP4AKA21HK RC410ME	216DCP4ALA12FG RC410MD	For Product spec	0.2	
9	Change part	C650	220U_D_6.3VM(@)	220U_Y_4VM(@)	For height limit, change to 2mm	0.2	
10		C148	220U_D2_4VM	220U_Y_4VM			
11		C52	220U_D2_4VM	220U_Y_4VM			
17	BOM Structure	C884, C885, C886, C887	————	2H@	For 2 HDD configuration	0.2	
26	Change part	SW10	EVQWA4001_6P	XRE094 2	For new digital VR	0.2	
26	Add part	C977, C978	————	1U_0402_6.3V4Z	Reserve for ALC861D/ ALC268 HP out, for Vista integrate driver	0.2	
	BOM Structure	C954, C955	————	@			
25	Net connection	U38.14 (LINE2_L)	NC	LIN_L			
		U38.15 (LINE2_R)	NC	LIN_R			
4	DEL PART	R463	47K_0402_5%(@)	————	Remove useless parts	0.2	
		R465	10K_0402_5%(@)	————			
8	DEL PART	R762	4.7K_0402_5%	————			
		R23	4.7K_0402_5%(@)	————			
19	DEL PART	R138, R139	10K_0402_5%(@)	————			

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27 4 12	Delete part	R305 R304 C665 R268	10K_0402_5%(@) 5.6K_0603_1%(@) 0.1U_0402_16V4Z(@) 4.7K_0402_5%(@)	——————— ——————— ——————— ———————	Remove useless parts	0.2	
14	Net rename	DVI_R DVI_G DVI_B DVI_HSYNC DVI_VSYNC	DVI_R DVI_G DVI_B DVI_HSYNC DVI_VSYNC	CRT_OUT_R CRT_OUT_G CRT_OUT_B CRT_OUT_HSYNC CRT_OUT_VSYNC	For designer check	0.2	
29	Net connection	X2.1(X'tal X1) X2.2(X'tal X2)	CRY1 CRY2	CRY2 CRY1	For layout smooth	0.2	
16	Add part BOM structure	Y7 C974, C975 R910 R911, R912 L46, R74, C267, X1, R335 R334	——————— ——————— ——————— ——————— ——————— @	48MHZ 20PF X6G048000FK3H-H 20P_0402_50V8J 1M_0402_5% 0_0402_5% @ ———————	Chnage USB clock from osciallor to crystal	0.2	
16	Net connection	R326.1 (GPIO5 PU) R751.1 (GPIO_M PD)	GND +3VS	+3VS GND	For ATi requirement	0.2	
13	BOM structure	C406, C407, C810, C811	@	———————	EMI solution for LVDS	0.2	
14	Change Part BOM structure	L1, L2, L3 C1, C2, C3	FCM2012C-800_0805 @	BK1608LL121-T 0603 ———————	EMI solution for CRT	0.2	
14	Change Part	JP23	SUYIN 020133MR004S529ZL~N	SUYIN 020167MR004S511ZR	ME change	0.2	
20	Add part	R913, R914 C976	——————— ———————	49.9_0402_1%(@) 0.1U_0402_16V4Z(@)	For LAN reverse	0.2	
4	Change part	R475, R476 R490	40.2_0402_1% 150_0402_5% 27.4_0402_1%	54.9_0402_1% 54.9_0402_1% 54.9_0402_1%	For CPU ITP	0.2	
29	Change part	L20, L23	FBM-L11 160808-800LMT_0603	0_0603_5%	Change EC power sorce and gnd source	0.2	
23	Net rename	U34.26(EECS) U34.28(EEDI) U34.29(EECK)	EECS EEDI EECK	1394_EECS 1394_EEDI 1394_EECK	Name Name duplication	0.2	

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29	Del part Add part Net Rename	Q66 C980 EC_EAPD	2N7002 _____ EC_EAPD	_____ 0.01U_0402_16V7K(@) EC_EAPD_R#	For Audio EAPD	0.2	
29	Add part	C979 Q67 R915 R916 R917 R919		1U_0402_6.3V4Z(@) 2N7002_SOT23(@) 8.2K_0402_5%(@) 20K_0402_5%(@) 2.4K_0402_5%(@) 1K_0402_5%(@)	For POST BEEP no sound issue	0.2	
16	Del part	R384(GATE20 PU) R385(KBRST# PU)	10_0402_5% 10_0402_5%	_____ _____	No need external pull up	0.2	
16	Net connection Add part	U9.D6(LPC_PME#) R918	EC_PME# _____	LPC_PEM# 10K_0402_5%	Disconnect SB PME# to EC PME#	0.2	
16 27	Add part	C981 C982, C983	_____ _____	10P_0402_50V8K(@) 22P_0402_50V8J(@)	For EMI reserve	0.2	
12	Del part Net connector	R712 U23.11 (Clock REQ B)	0_0402_5%(@) N19175427	_____ MINI_CLKREQ#	For mini card clock request	0.2	
28	BOM Structure	C712, C715	_____	@	Transion test pass	0.2	
29	Change part	U46	NC7SZ14M5X_SOT23-5	74LVC1G14GW SOT353-5	Change package for logic IC standard	0.2	
29	Del part Net connection	R867, R868 R714.2 (BITCLK to HD) R715.2 (BITCLK to MDC)	0_0402_5% N52707434 N52707448	_____ AZ_BITCLK_HD AZ_BITCLK_MD	Azalia signal, no need two serial reisistor	0.2	
28	Add part	R920, R921, R922, R923	_____	0_0402_5%(@)	Reserve resistor for USB signal	0.2	
26	Add part	R924 C984	_____ _____	0_0402_5% (@) 0.01U_0402_16V7K(@)	Reserve function for EC control HP_EN	0.2	
26	BOM Structure	C406, C407, C810, C811	@	_____	For LVDS EMI solution	0.2	
29	Change part	R101	0_0402_5%	8.2K_0402_5%	Board ID change to 1 for Rev0.2	0.2	
25	Add part	R925	_____	39.2K_0603_5%	For ALC861 +Vista driver	0.3	
26	BOM Sturcture	C977, C978 C954, C955	@ _____	_____ @	For Vista intergated driver	0.3	

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HW4 Product Improvement Record (P.I.R.)

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26	Del part	R919 R916 R917 Q67	1K_0402_5%(@) 20K_0402_5%(@) 2.4K_0402_5%(@) 2N7002_SOT23(@)	——— ——— ——— ———	Remove POST BEEP no sound issue	0.3	
29	Change part	R101	8.2_0402_5%	18_0402_5%	PCB revision ID	0.3	
4 15	BOM Sturcture	R491 R167 R713	@ ——— @	——— @ ———	For C4 timing	0.3	
19	BOM Sturcture	R334 R335	@ ———	——— @	48M oscillator select	0.3	
20	Del part Change part	R235 C433	10_0402_5%(@) 22P_0402_50V8J(@)	——— 18P_0402_50V8J(@)	LAN PCI clock for EMI	0.3	
15	BOM Structure	C832, C833, C973, D29, D42, Q1, Q6, Q62, R802, R900, R901, U36 R713, R902	——— @	@ ———	No need C4 support	0.3	
12 15	Change part BOM Structure Add part	R255 C831 Q66 U49 R927	4.7K_0402_5% ——— ——— ——— ———	0_0402_5% @ 2N7002_SOT23(@) 74LVC1G14GW_SOT353-5(@) 10K_0402_5%(@)			
20	Add part	R926	———	20K_0402_1%(@)	Internal MIC sensor	0.3	
20	Change part	C286, C287	18P_0402_50v8D	12P_0402_50v8J	RTC timing	0.3	
20	Del part	L23	0__0603_5%	———	Component reduce (EC A-power)	0.3	
15	Del part	R317	0__0402_5%(@)	———	Layout reduce (SB H_RESET#)	0.3	
15	Change part	R318	11.8K_0603_1%	11.3K_0603_1%	USB adjust and EMI	0.3	
16 27	BOM Sturcture	R716, R717, R718, R871 R886, C864, C865, JP36	——— ———	MDC@ MDC@	MDC option	0.3	
26	Add part Change part	R928, R929 R862, R863	——— 39K_0402_5%	20_0402_5% 24K_0402_5%	HP serial resistor for AP2056 noise when use mono HP gain adjust	0.3	

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Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
16	Del part	C974	20P_0402_50V8J	_____	For USB logo and EMI	0.3	
		Y7	48MHZ_20PF_	_____			
		R910	1M_0402_5%	_____			
		R911	0_0402_5%	_____			
	Change part	C975	20P_0402_50V8J	12P_0402_50V8J			
		R912	0_0402_5%	30_0402_5%			
	Net connect	R912.1 (48MHz source)	48M_XTAL1	OSC_48MHZ			
		X1.3 (48MHz source)	48M_XTAL1	OSC_48MHZ			
		C975.2 (48MHz source)	48M_XTAL1	OSC_48MHZ			
	BOM Structure	L46, R74, C267, X1	@	_____			
26	Add part	Q67	_____	2N7002_SOT23	De- Bo noise		
26	Change part	C954, C955	1U_0603_6.3V4Z(@)	2.2U_0603_6.3V6K(@)	Audio precision	0.3	
		C977, C978	1U_0603_6.3V4Z	2.2U_0603_6.3V6K		0.3	
		C957 C958	1U_0603_16V6K	2.2U_0603_6.3V6K			
	Del part	R830, R832	1.5K_0402_5%	_____			
		C947, C949	1U_0402_6.3V4Z	_____			
	Change part	C948, C950	1U_0402_6.3V4Z	0.22U_0402_6.3V6K			
33	Change part	C449	10U 10V M A NOJ H1.6	22U 10V M B NOJ H1.9	For De-fan noise		
13	Net connect	JP1.29(LCD CONN)	GND	B+	For dual lamp LCD	0.3	
		JP1.26(LCD CONN)	_____				
33	Net connect	PU5.5 (OP+)	N19688420 (FAN FB)	N19688478 (EC_FANCTRL)	Update FAN control circuit	0.3	
		PU5.6 (OP-)	N19688478 (EC_FANCTRL)	N19688420 (FAN FB)			
		R240.2	FAN1	N19688714 (FAN FB)		0.3	
	Change part	R836	10K_0402_5%	0_0402_5%			
		R240	5.1K_0402_5%	8.2K_0402_5%			
		R874	5.1K_0402_5%	100_0402_5%			
		Q36	AOS 3401_SOT23	FMMT619_SOT23			
	BOM Structure	R875, C449	_____				
28	Change part	C979	0.47U_0402_6.3V6K	1U_0402_6.3V4Z	No use amplifier beep		
	Del part	R915	47K_0402_5%	@ _____			
	Net connect	C979.2 (AMP_BEEP)	BEEP_DIR	AMP_BEEP		0.3	

HW4 Product Improvement Record (P.I.R.)

Phase: C to PreMP | Date: 2006/10/25 | Writer: Timo Teng

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16	Add Part	C986	10uF_0805		For 48MHz harmonic noise issue		
		C987	0.01uF_0402				
13	Add Part	C988	0.01uF_0402		Solve inverter EMI noise issue		

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IAYAA POWER Product Improvement Record (P.I.R.)

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	0807	P.39	Change net susp# to pok and pok to susp#	
2.	0807	P.41	Add PC124,PC125,PC126,PC127	reserve for in-phase issue
3.	0929	P.36,37	Add PC128,PC129,PC130	For EMI solve 200MHz-300MHz Broad band
4.	0929	P.41	Add PC131	For EMI solve 80MHz-100MHz Broad band
5.	1024	P.36	Change PR36 from 22K to 20K_0402_1%	For thermal team request to modify OTP point
6.	1024	P.38	Add PR173 (0_0402_5%) and unpop PR88	Decrease the S5 power consumption
7.	1025	P.41	Add PC132	For EMI solution

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