

Compal confidential

Liverpool 10AR/10ARG

KSWAE LA-4971P Schematics Document

Mobile AMD S1G2 S1G3/
RS780MN & RS780MC & RX781 & RS880 /
SB700 & SB710

2009-02-09 Rev. 0.3

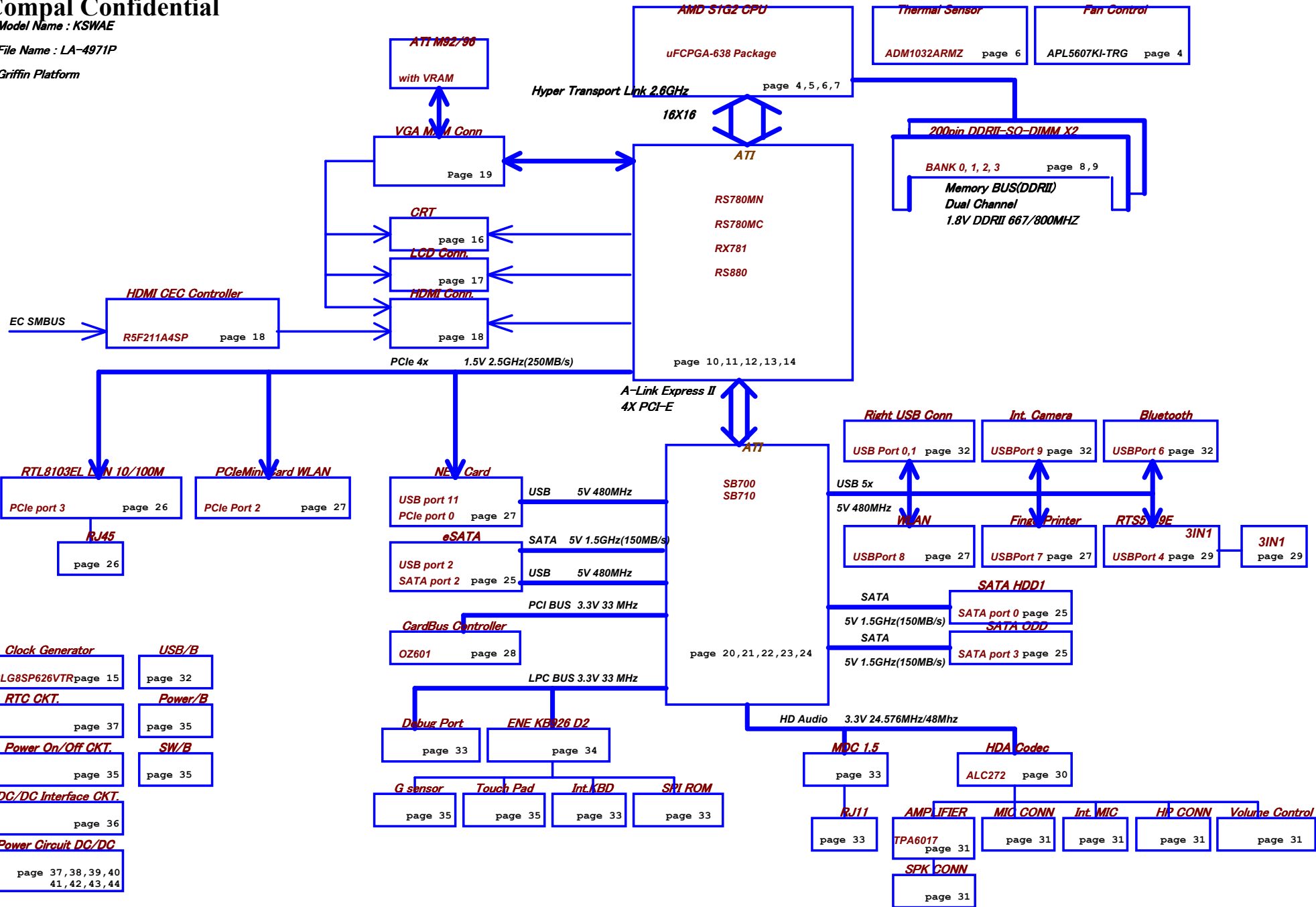
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Issued Date	2008-09-25	Deciphered Date	2009-09-25	Compal Electronics, Inc. Cover Sheet	
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Compal Confidential

Model Name : KSWAE

File Name : LA-4971P

Griffin Platform



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Voltage Rails

O : ON
X : OFF

power plane	+B	+5VALW	+1.8V	+5VS
State	+3VL	+3VALW	+0.9V	+3VS
	+5VL	+1.2VALW	+0.9V	+2.5VS
	+RTCVCC	+3V_LAN		+1.8VS
				+1.5VS
				+1.1VS
				+VGA_CORE
				+1.2V_HT
				+CPU_CORE_NB
				+CPU_CORE_0
				+CPU_CORE_1
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X b
HDMI-CEC	34H	0011 010X b
EC KB926D2		

EC SM Bus2 address

Device	HEX	Address
ADI1032-1 CPU	98H	1001 100X b
ADI1032-2 VGA	9AH	1001 101X b
EC KB926D2		
Ext. VGA/B		
CS/B		

Symbol Note :



@ : just reserve , no build

DEBUG@ : reserve for debug.



UMA@: means for RS780M.

BTO (Build-To-Order) Option Table

Function	Express card / PCMCIA	BLUE TOOTH	RJ11	SSD	SATA ODD	WiFi	G- sensor	3 in 1 card reader
Description	(E / A)	(B)	(R)	(S)		(H)		
Explain					16"	17"	Half - size	First Second RTS5159
BTO	EXPCARD@ / PCMCIA@	BT@	MDC@	SSD@	16inch@	17inch@	WLAN@ WIMAX@	G@ + G_1st@ G@ + G_2nd@ CARD@

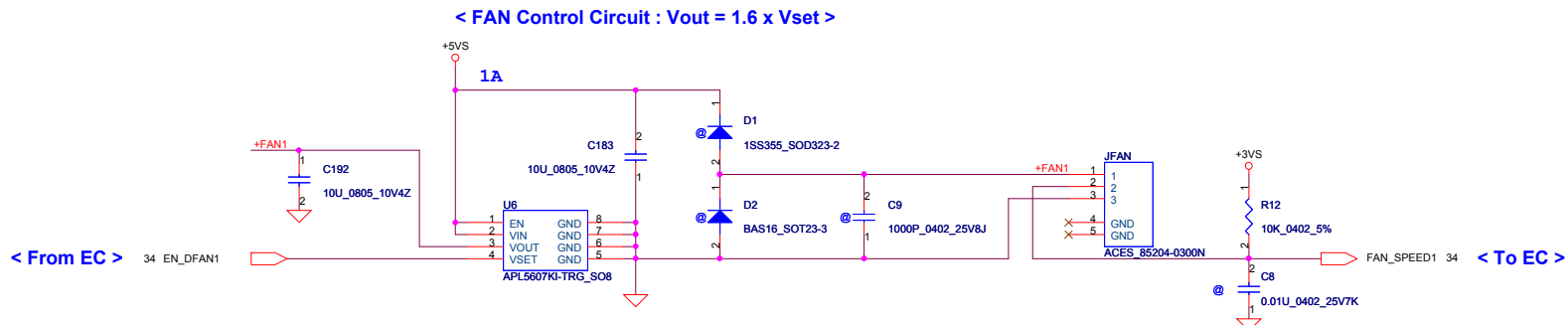
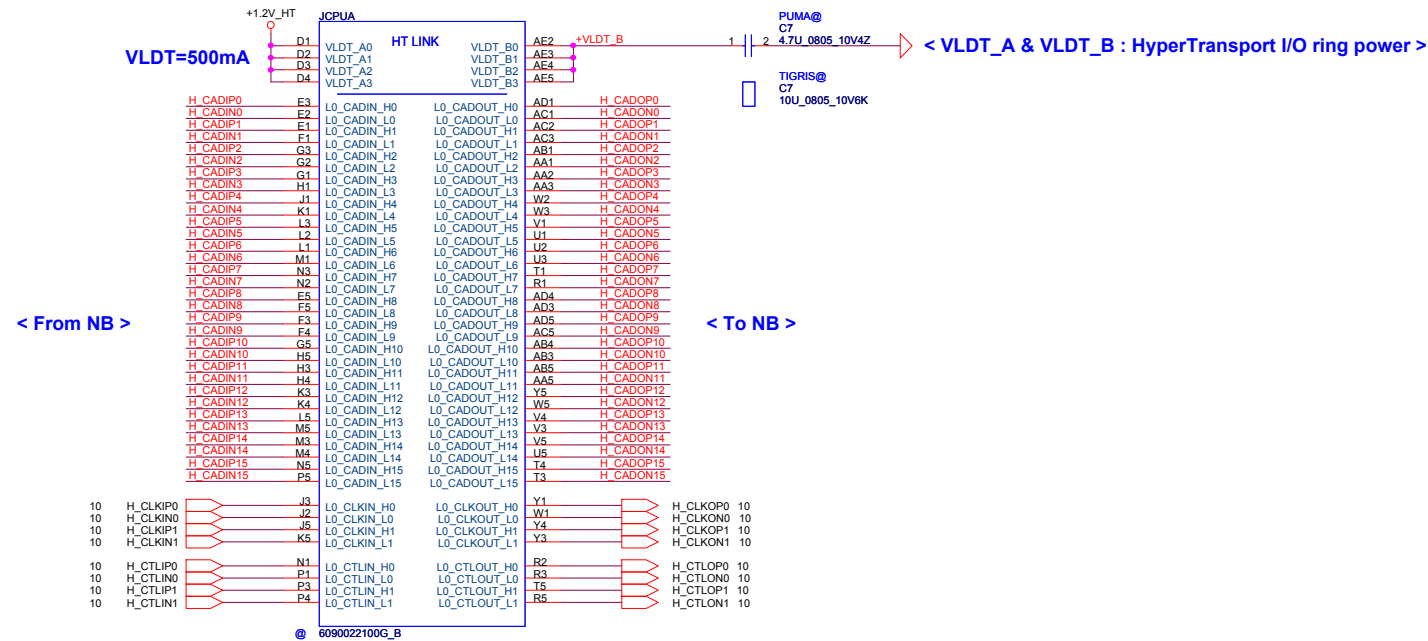
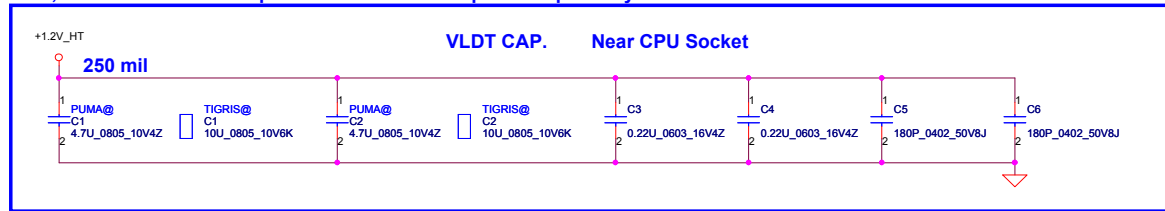
Function	FingerPrinter	CAMERA & MIC	HDMI	LVDS wireset	DC-IN	CHIPSET
Description	(F)	(X)	(Y)			
Explain		CAMERA MIC	AMD(UMA) ATI VGA/B COMMON	Cost down		
BTO	FP@	CAM@ MIC@	IHDMI@ HDMI@ H@	LVDSSET@	16inch_45@ 17inch_45@	PUMA@ TIGRIS@

SMBUS Control Table

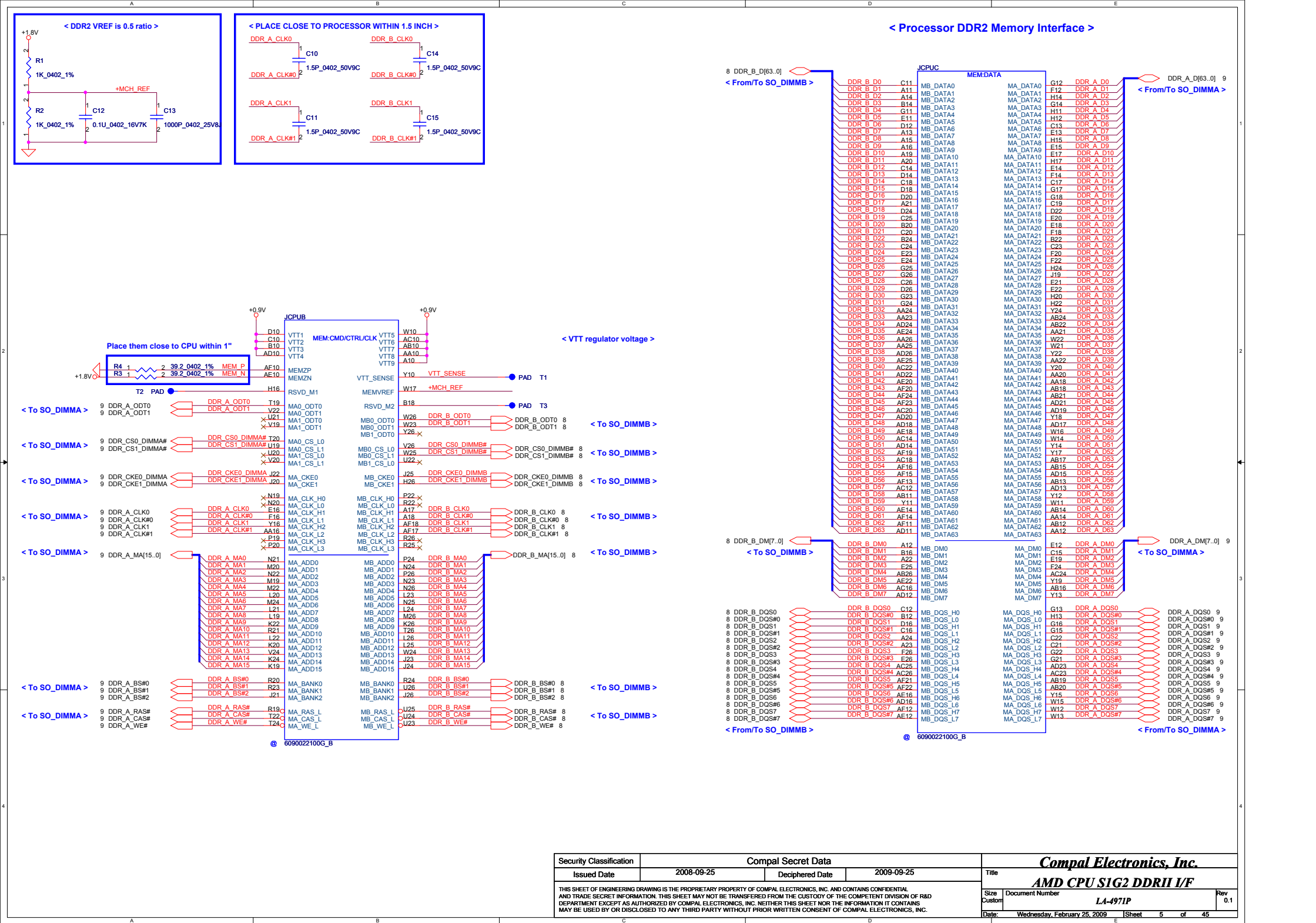
	SOURCE	INVERTER	BATT	HDMI CEC	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM	NEW CARD	MXM Thermal Sensor
EC_SMB_CK1 EC_SMB_DA1	KB926		V	V								
EC_SMB_CK2 EC_SMB_DA2	KB926				V							V
I2C_CLK I2C_DATA	RS780M								V			
DDC_CLK0 DDC_DATA0	RS780M									V		
DDC_CLK1 DDC_DATA1	RS780M											
SCL0 SDA0	SB700					V	V				V	
SCL1 SDA1	SB700							V				
SCL2 SDA2	SB700											
SCL3 SDA3	SB700											

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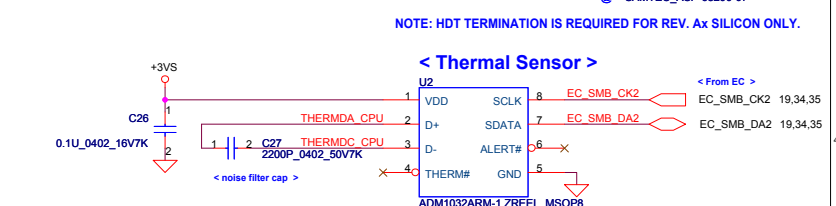
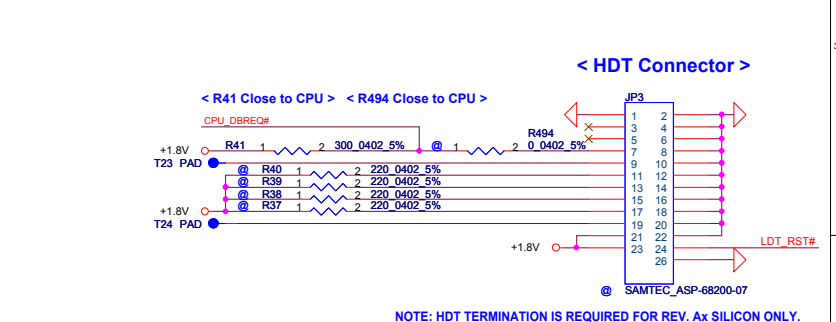
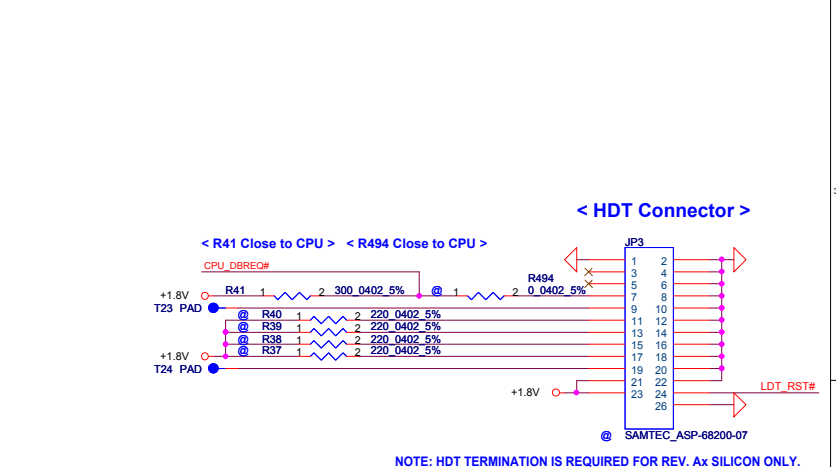
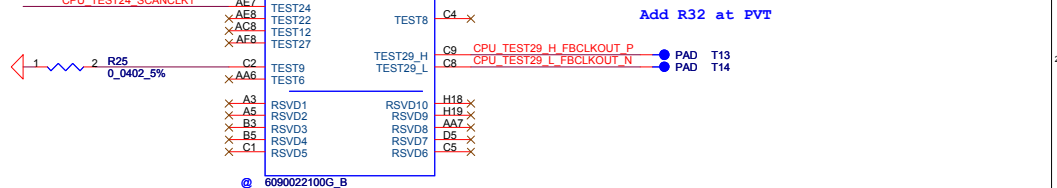
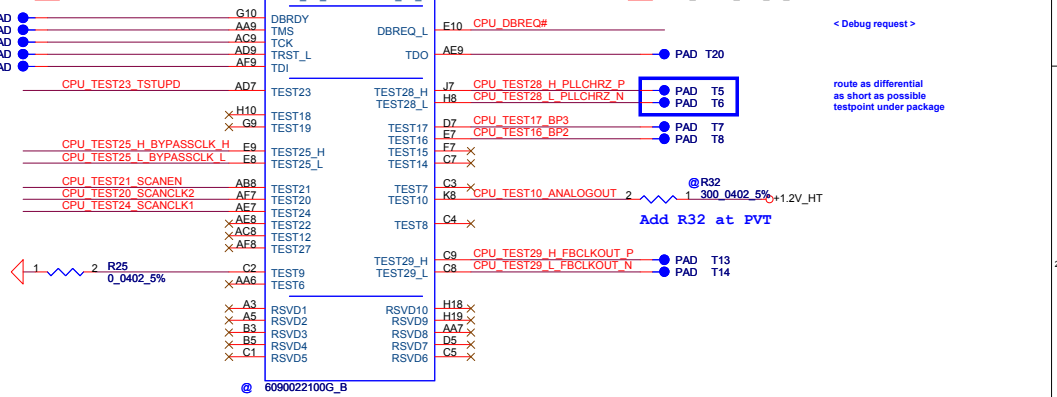
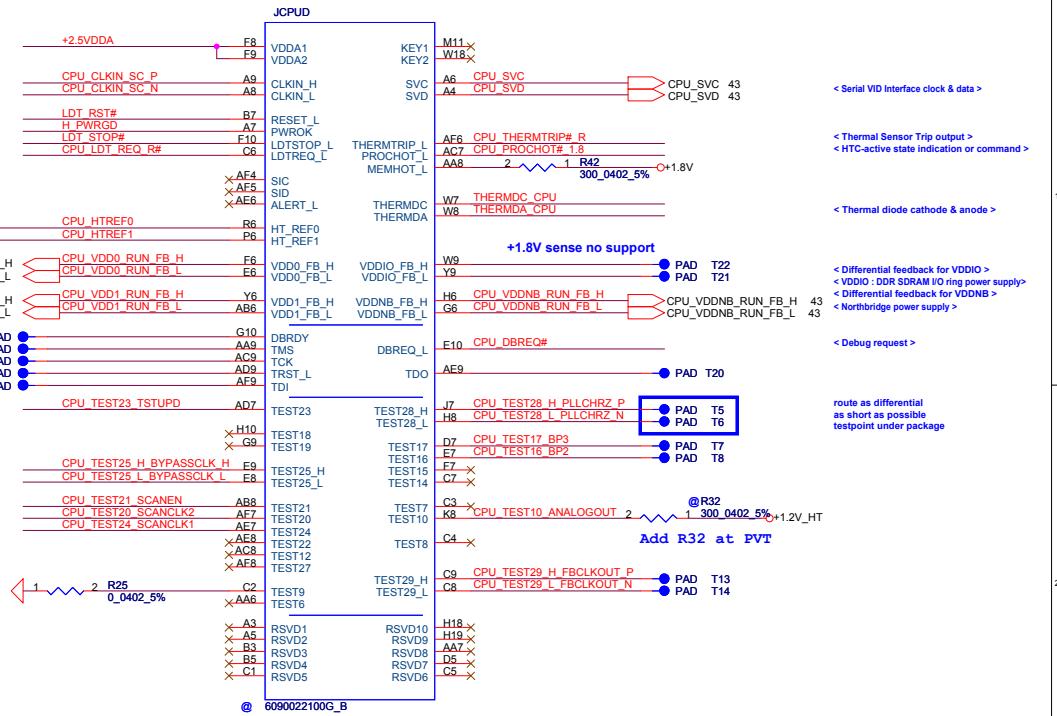
< C1, C2 and C7 must be replaced to 10-uF for Caspian compatibility >



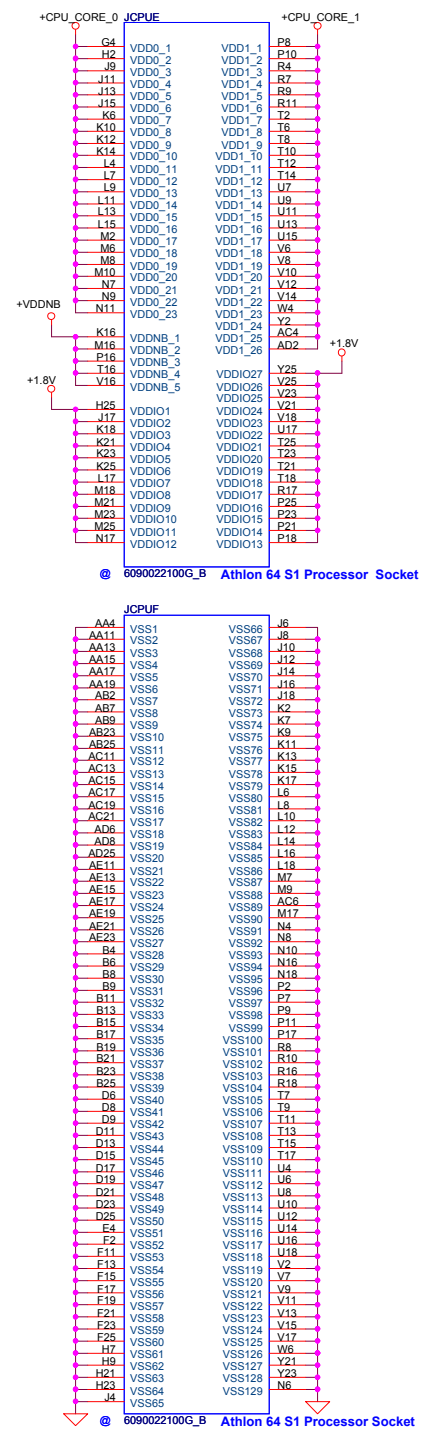
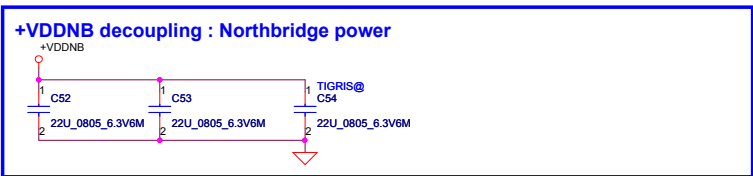
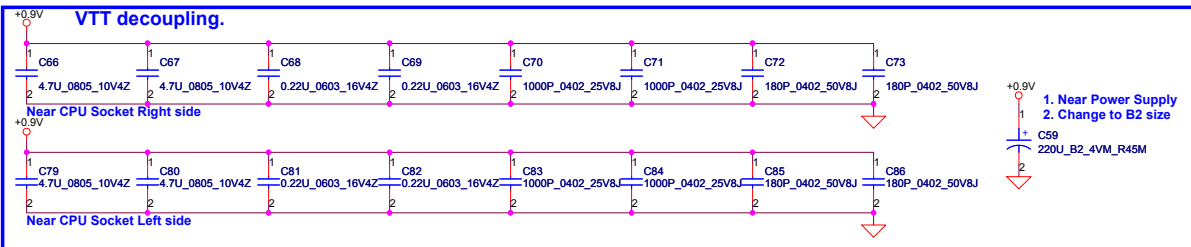
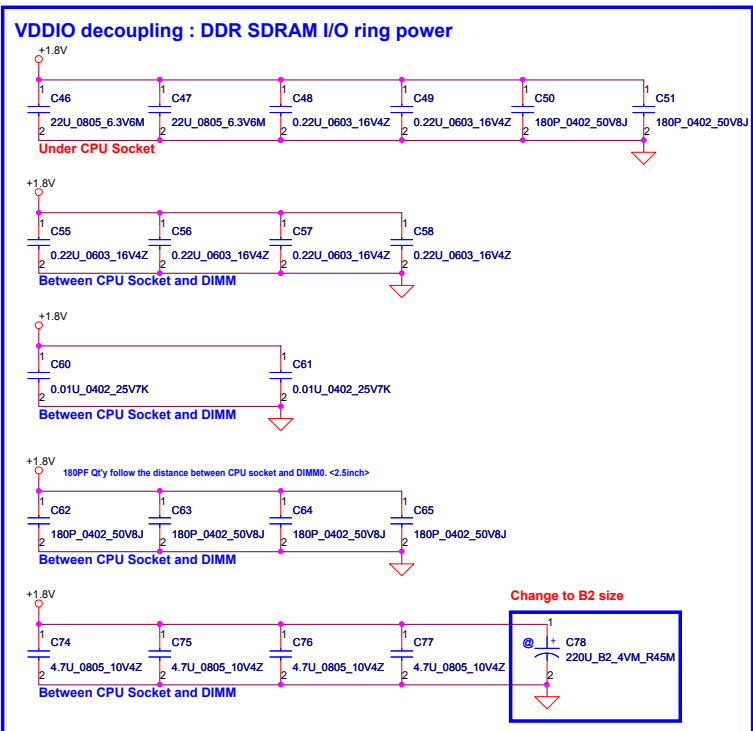
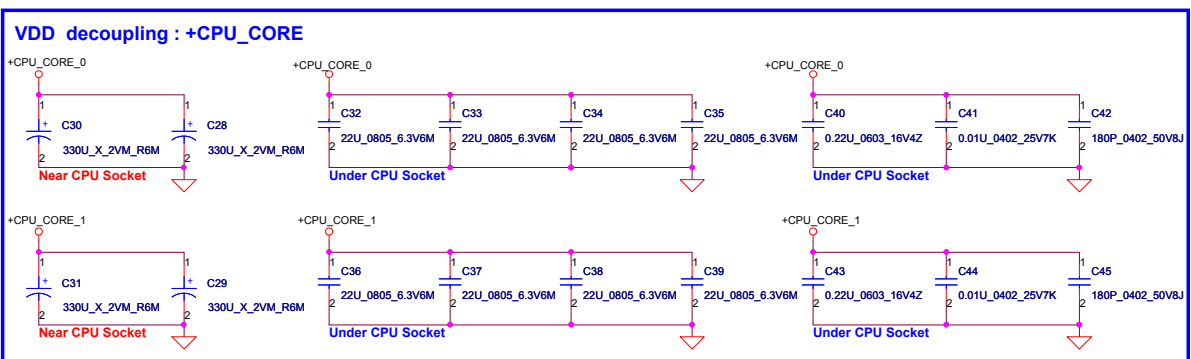
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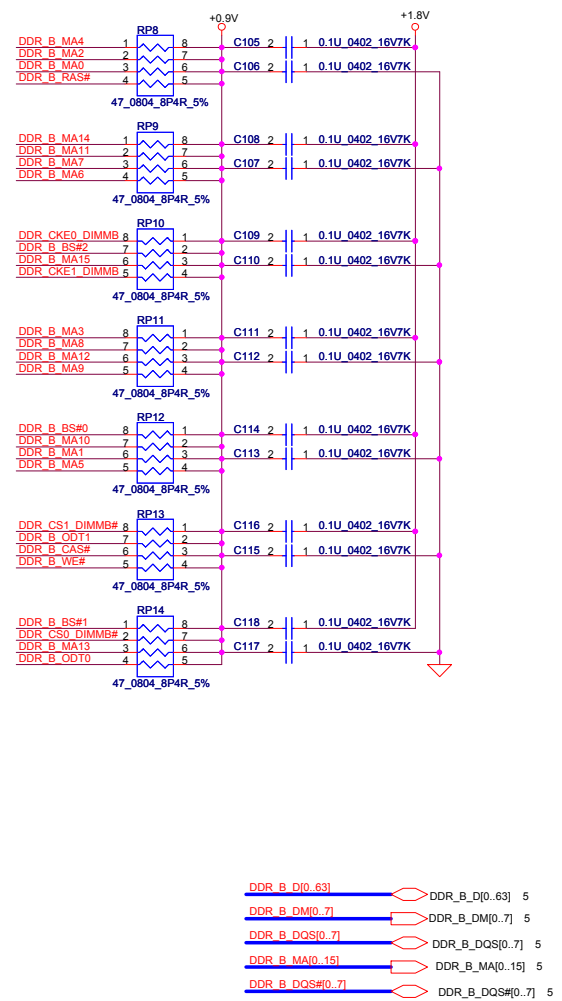
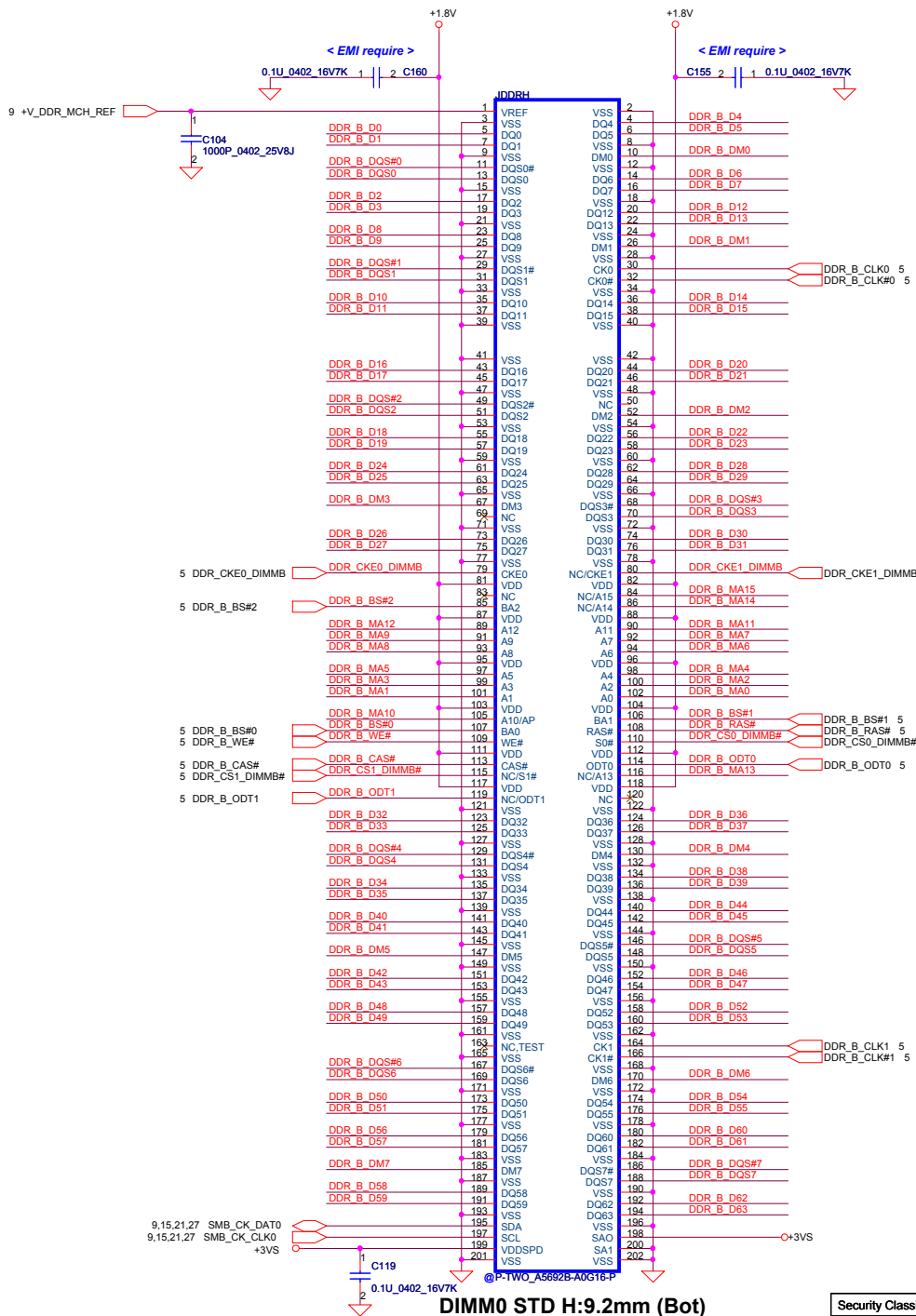


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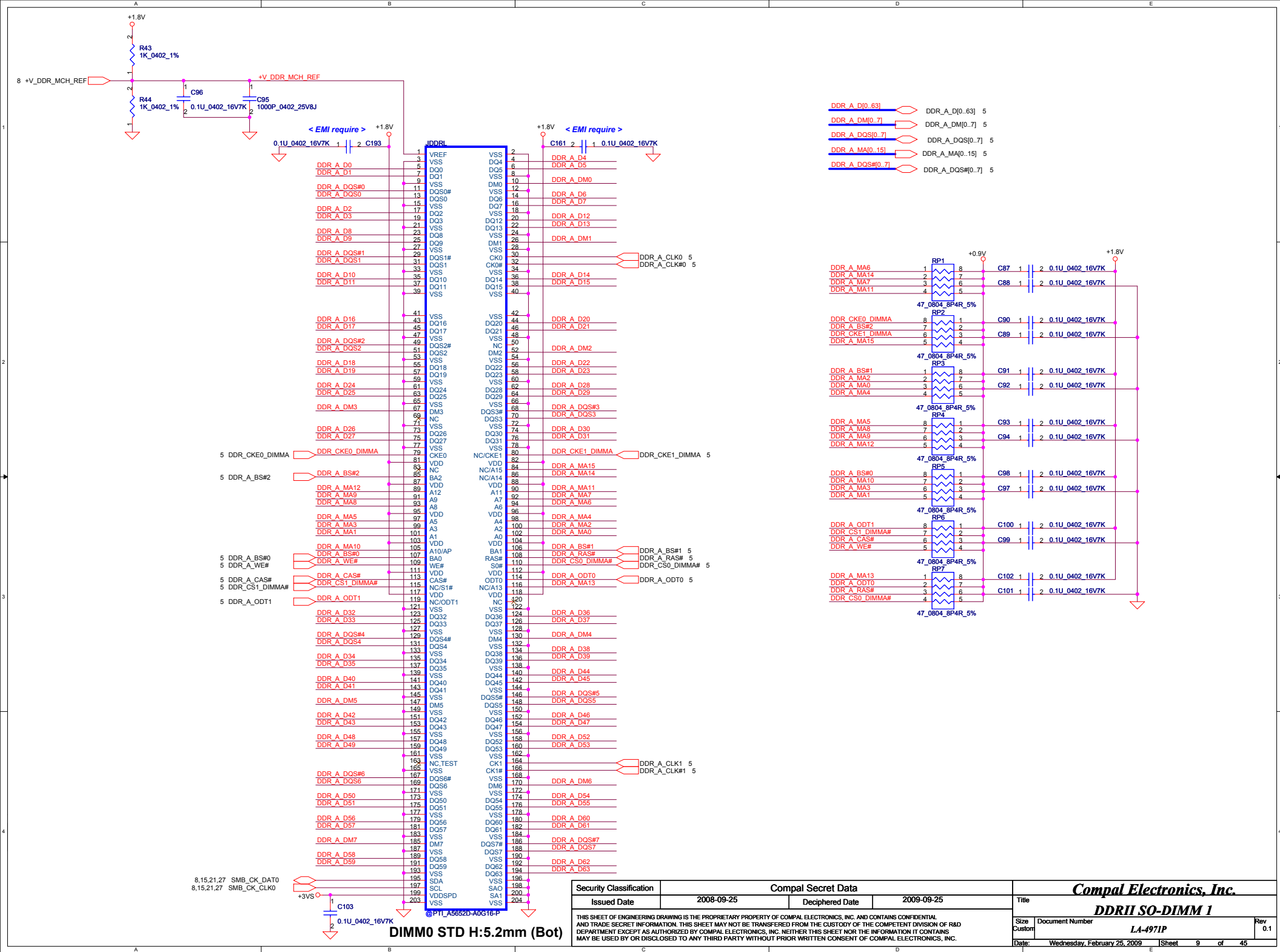
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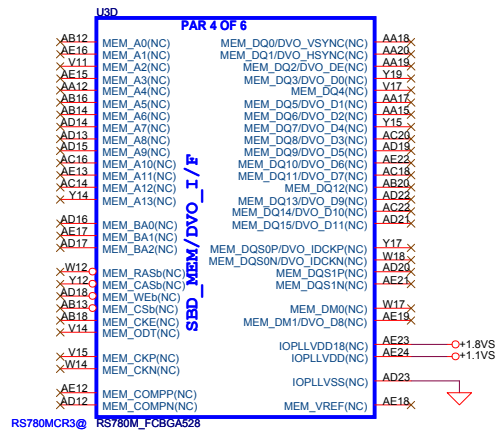
DIMM0 STD H:9.2mm (Bot)

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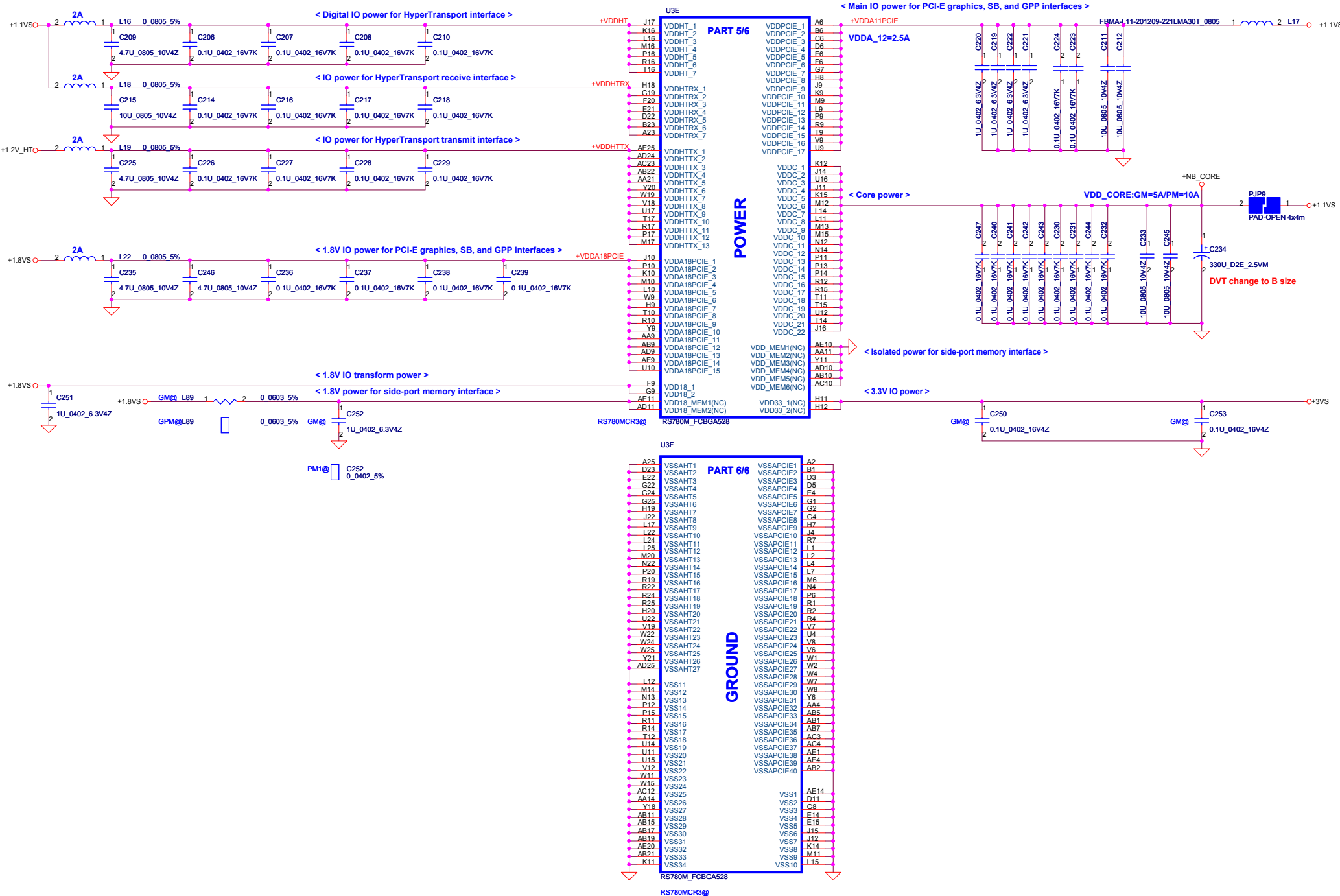


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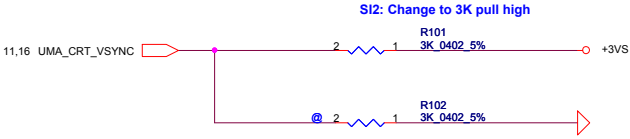
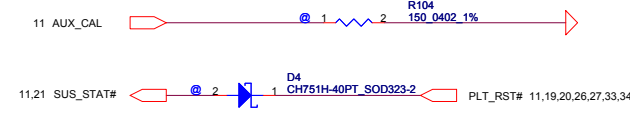
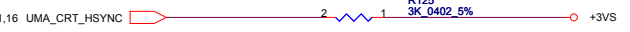
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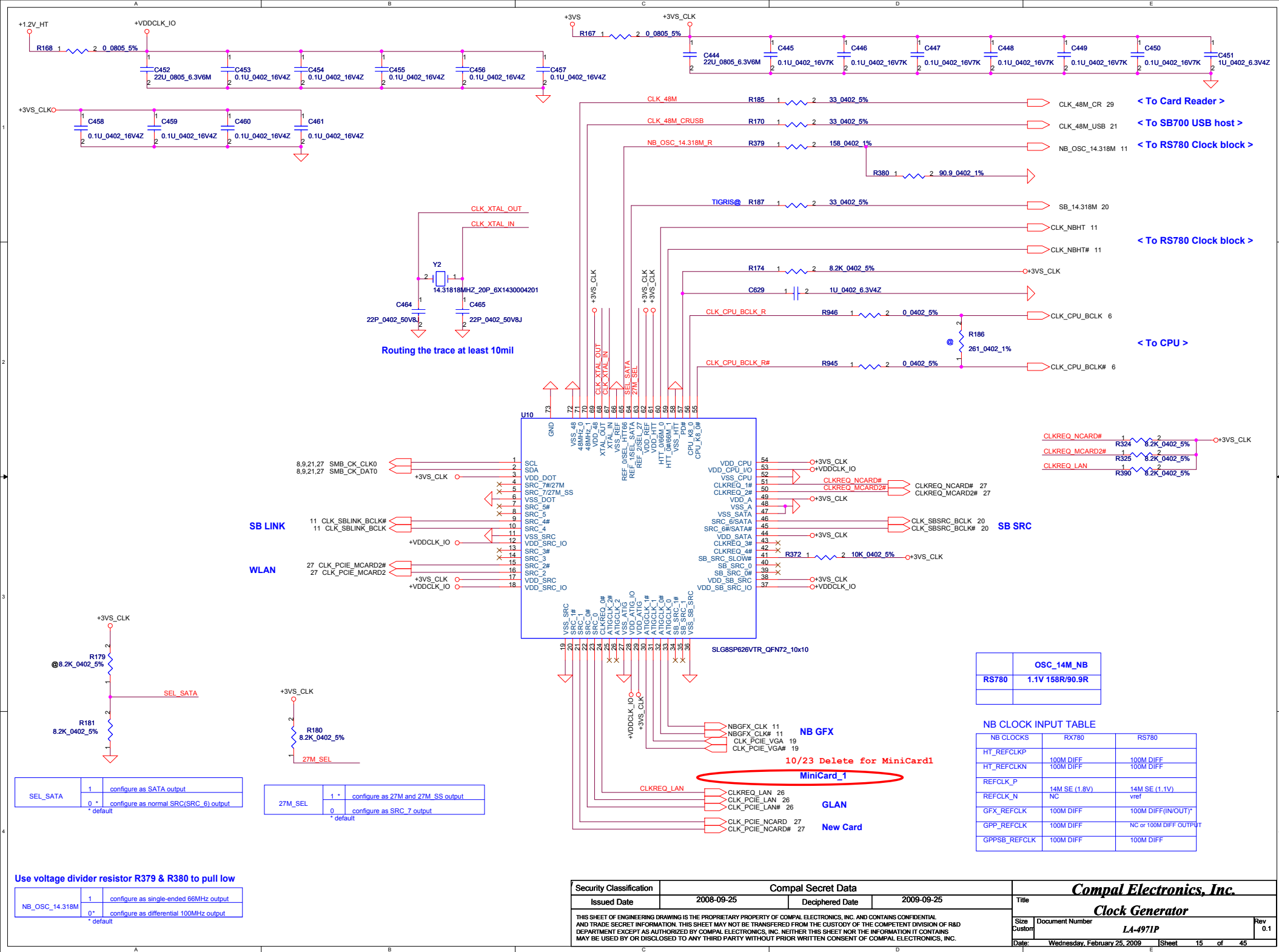
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< RS780 DFT_GPIO5 mux at CRT_VSYNC pull High to 3K > SI2: Change to 3K pull high 	< DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb > Enables the Test Debug Bus using GPIO. 1 : Enable (RX780, RS780) 0 : Disable (RX780, RS780) PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#
< RS780 use register to control PCI-E configure >	< DFT_GPIO[4:2] : STRAP_PCIE_GPP_CFG[2:0] > These pin straps are used to configure PCI-E GPP mode. 000 : 00001 001 : 00010 010 : 01011 011 : 00100 100 : 01010 101 : 01100 111 : 01011
< RS780 DFT_GPIO1 > 	< DFT_GPIO1 : LOAD_EEPROM_STRAPS > Selects Loading of STRAPS from EPROM 1 : Bypass the loading of EEPROM straps and use Hardware Default Values 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected RS740/RX780: DFT_GPIO1 RS780:SUS_STAT
< RS780 use HSYNC to enable SIDE PORT (internal pull high) > 	< DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb > RX780: Enables the Test Debug Bus using PCIE bus 1 : Disable (Can still be enabled using nbcfg register access) 0 : Enable RS780: Enables Side port memory (RS780 use HSYNC#) 1. Disable (RS780) 0 : Enable (RS780)

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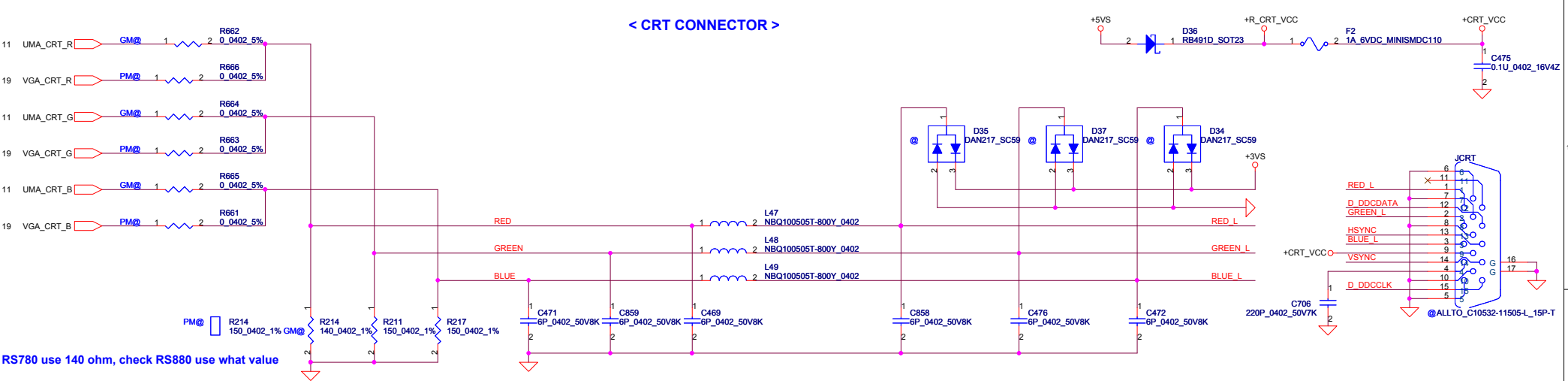
	OSC_14M_NB
RS780	1.1V 158R/90.9R

NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPSSB_REFCLK	100M DIFF	100M DIFF

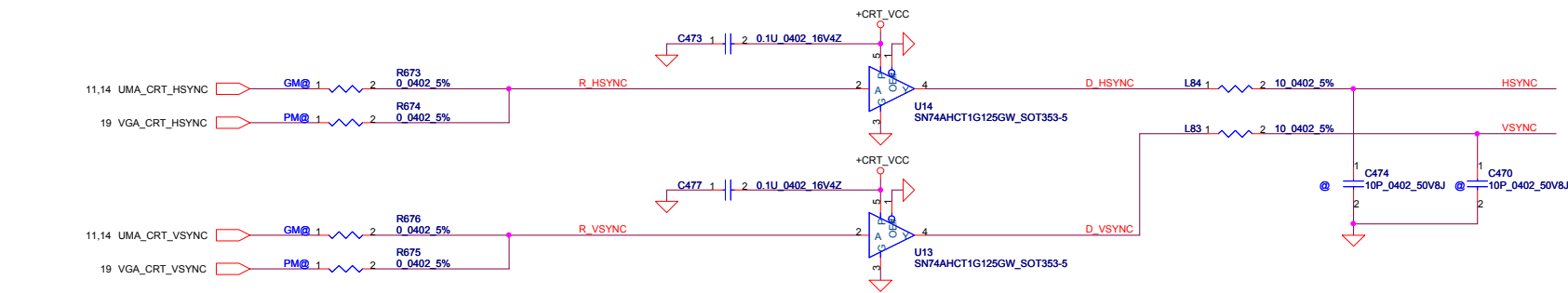
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< CRT CONNECTOR >

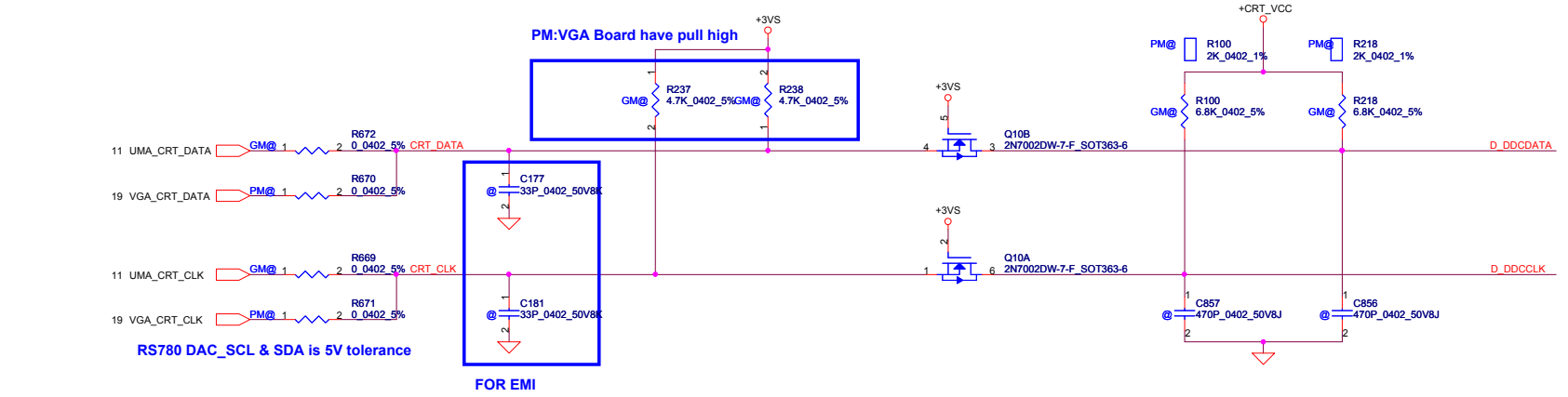


RS780 use 140 ohm, check RS880 use what value

< SYNC SIGNAL >



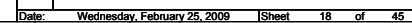
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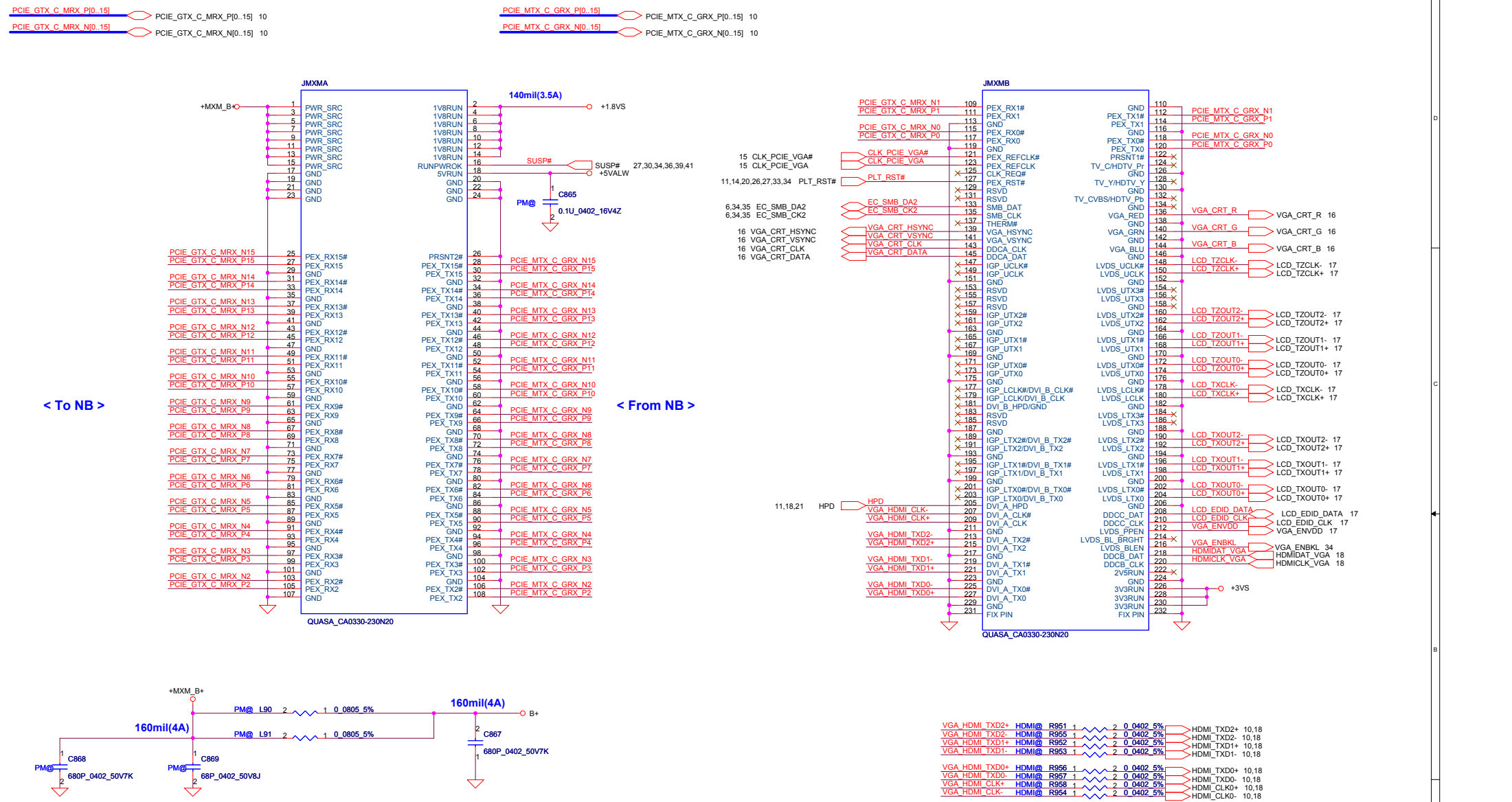


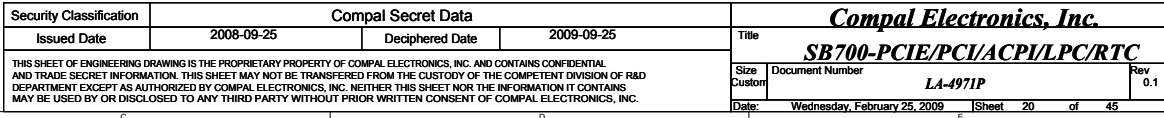
RS780 DAC_SCL & SDA is 5V tolerance

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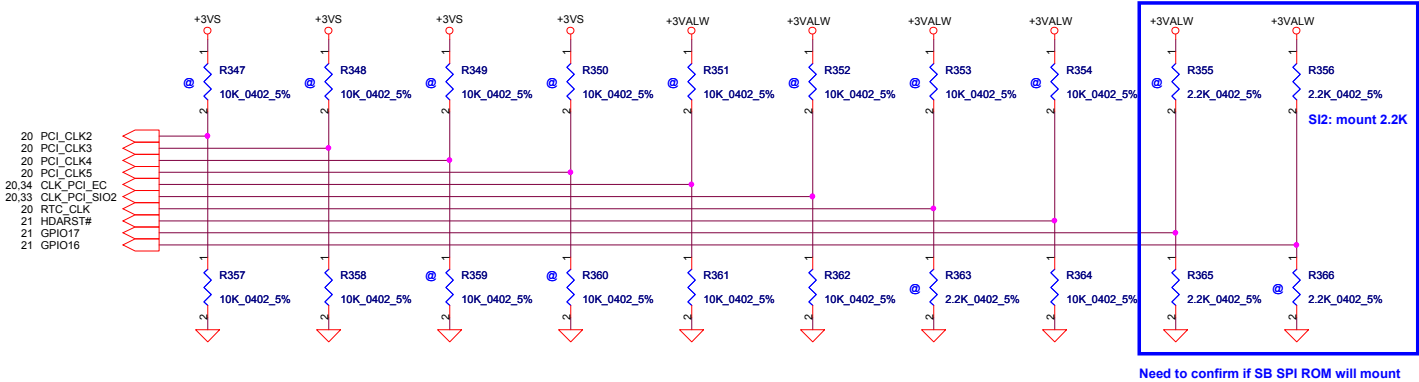




REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

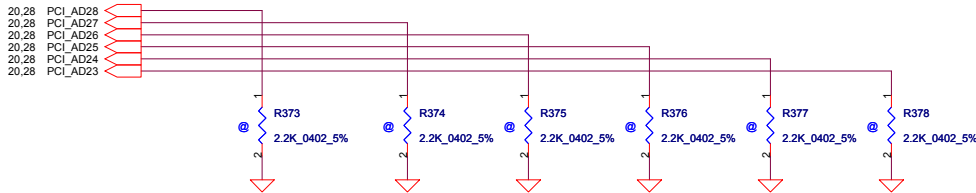
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default) L,L = FWH ROM



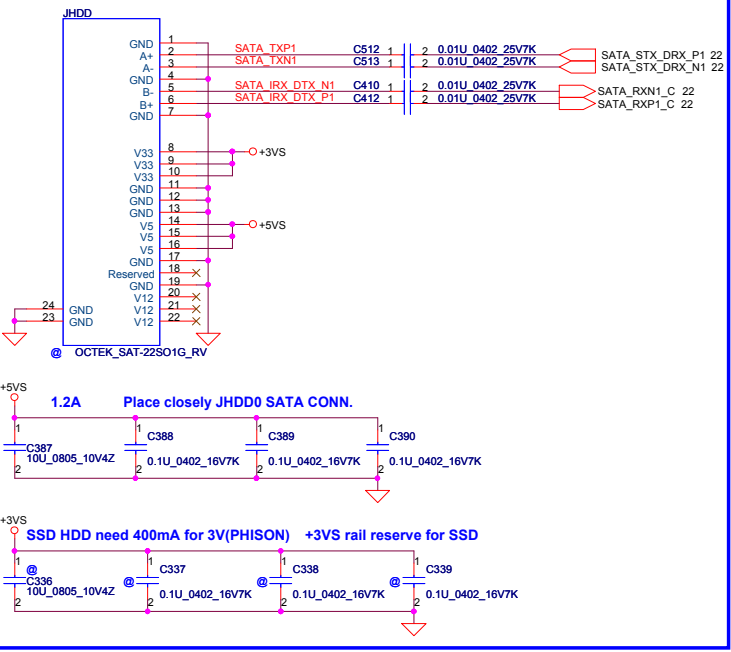
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

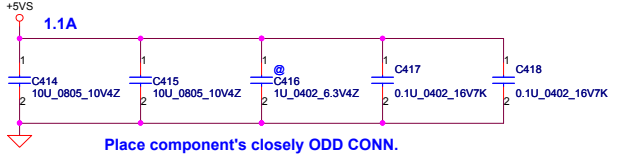
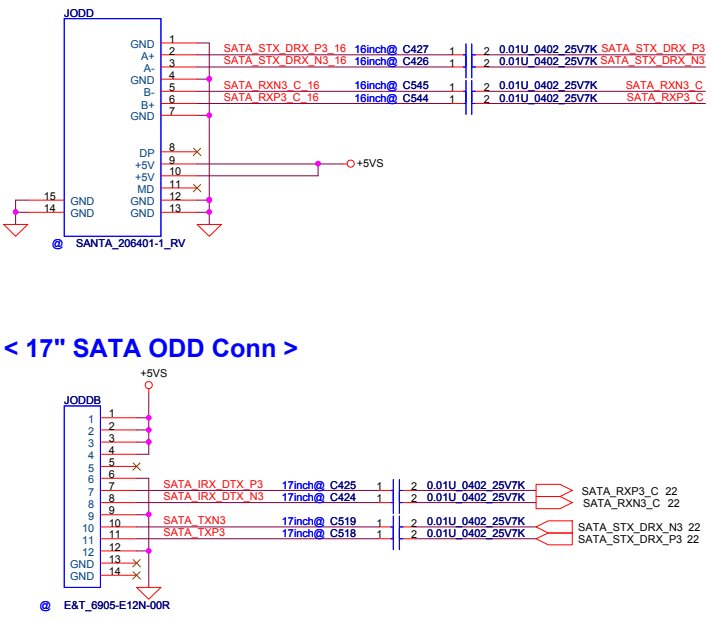
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



< SATA HDD1 Conn >

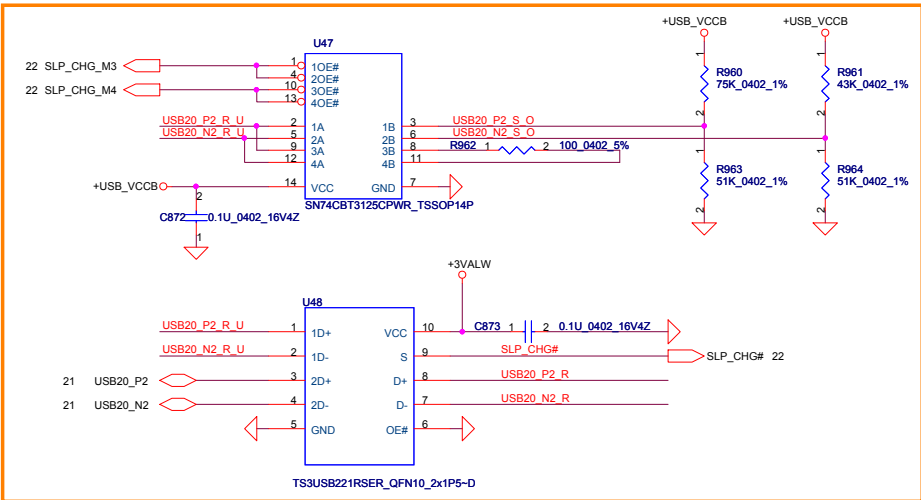


< 16" SATA ODD Conn >

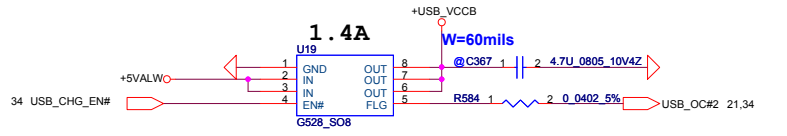
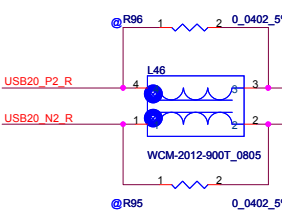


< eSATA/USB >

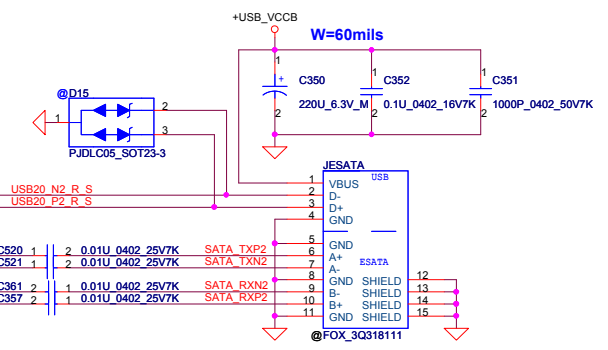
10/22 Add for USB Sleep & Charge M3/M4



Reserve for EMI request



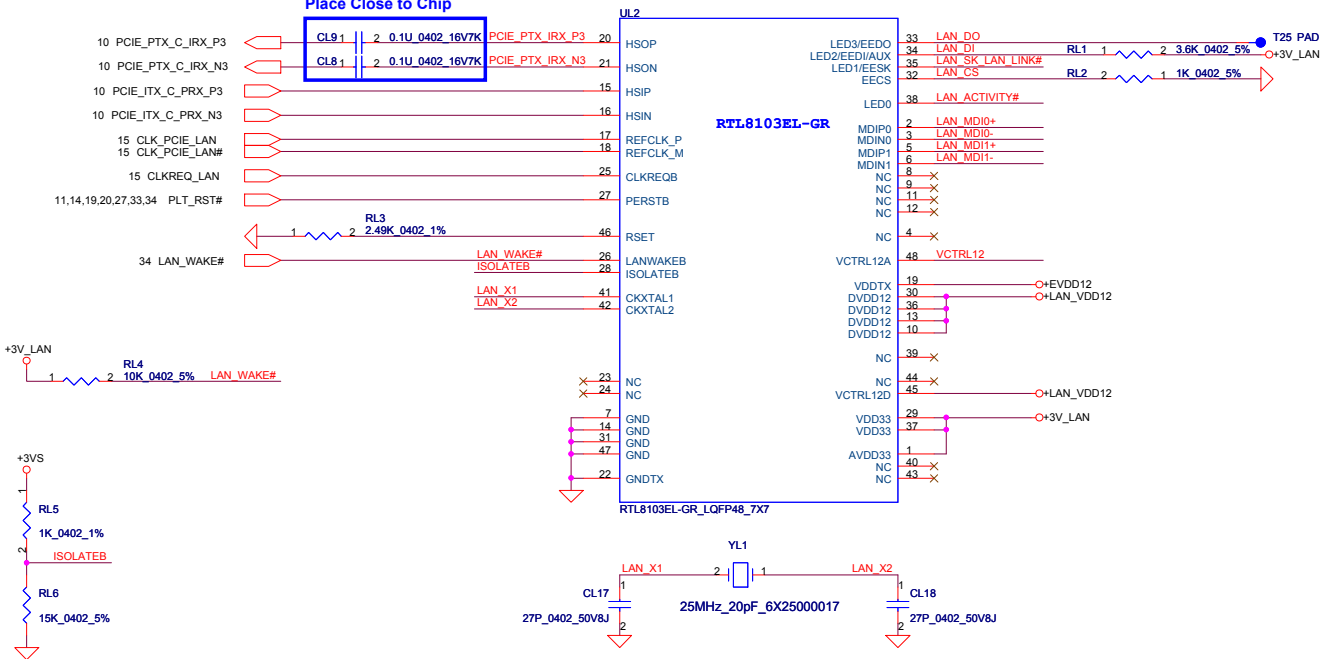
eSATA/USB Conn



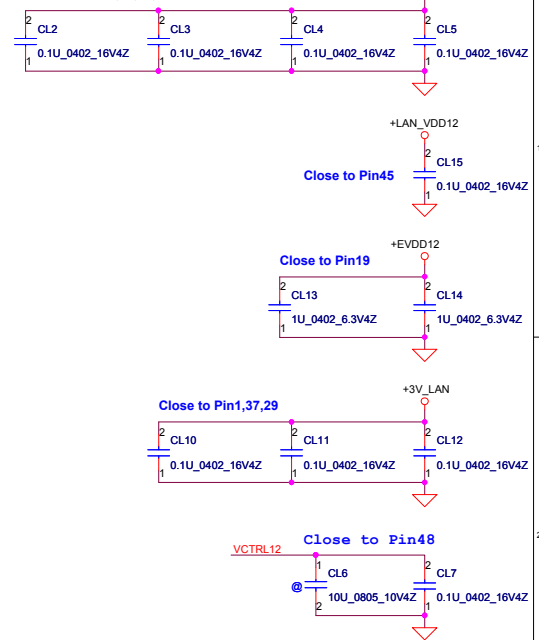
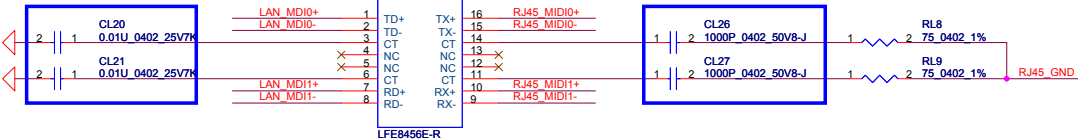
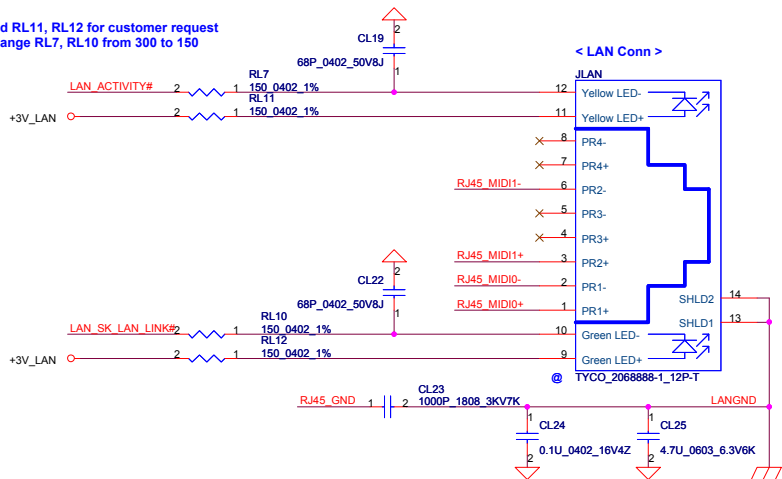
	SLP_CHG_M3	SLP_CHG_M4	SLP_CHG#	FUNCTION
Mode 3	HIGH	LOW	LOW	D=1D
Mode 4	LOW	HIGH	HIGH	D=2D

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Place Close to Chip

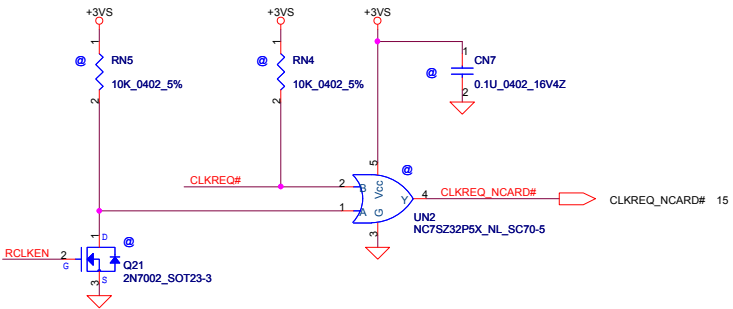
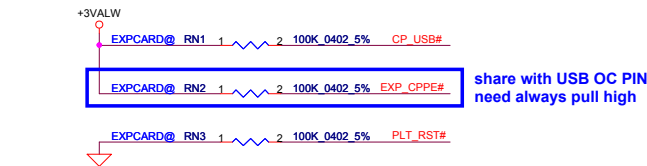
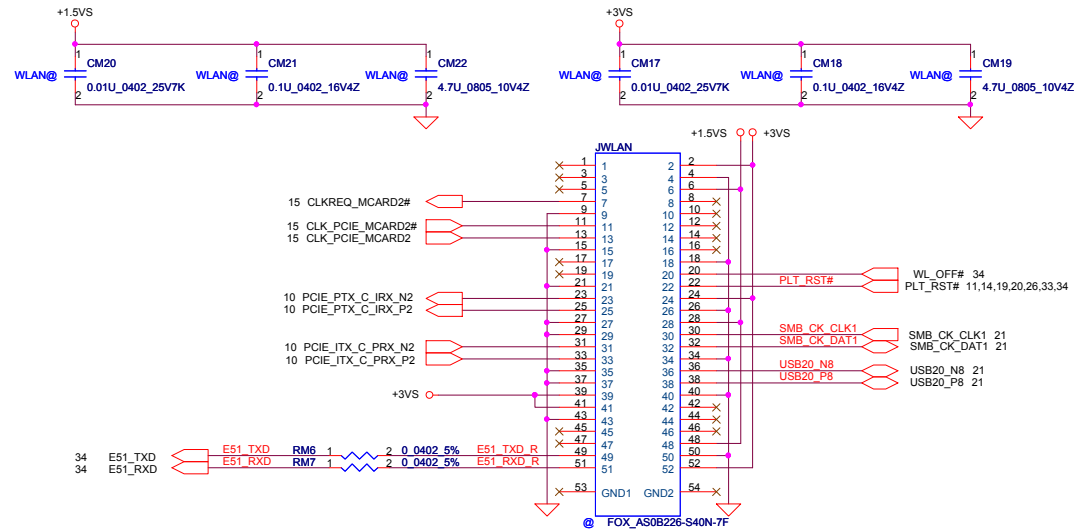


Close to Pin10,13,30,36

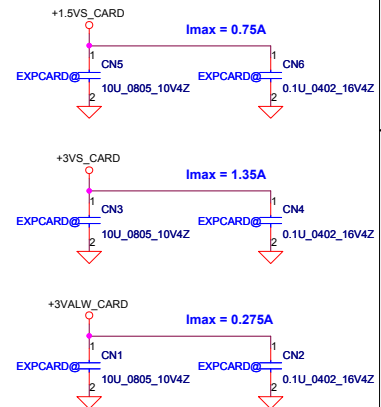
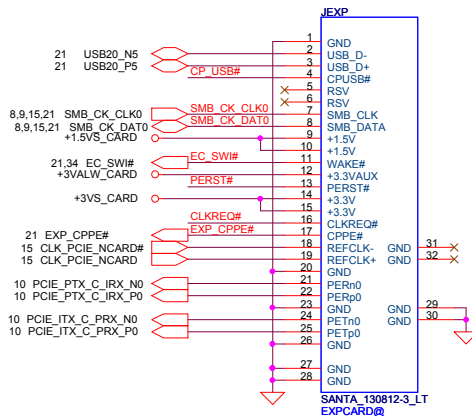
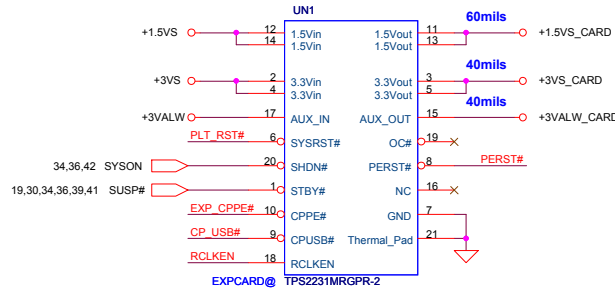
Place these components
colsed to LAN chipAdd RL11, RL12 for customer request
Change RL7, RL10 from 300 to 150

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< PCIe Mini Card for WLAN >

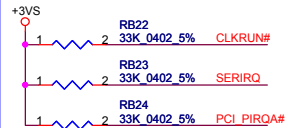


< Reserve for test >

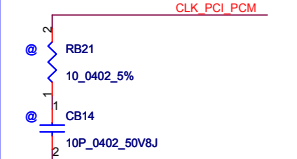


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22K TO 47K PULL-UPS MUST BE PLACED ON INTA#, PME#, SERIRQ# & CLKRUN#.



For EMI



NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME.

IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS.

THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

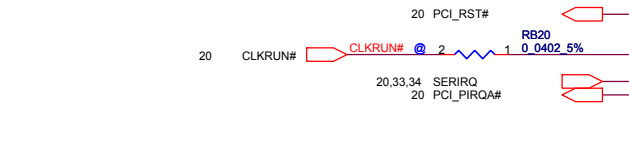
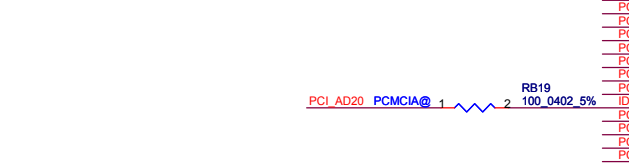
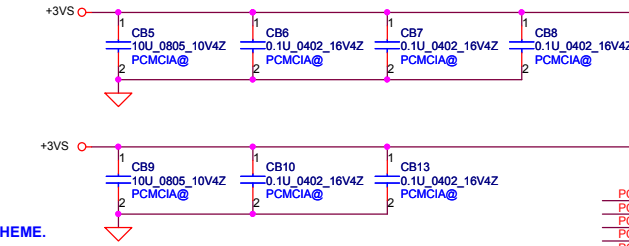
CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127 ball F4

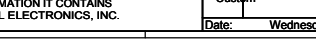
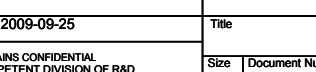
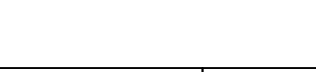
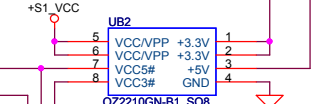
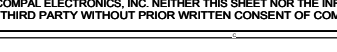
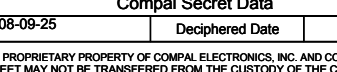
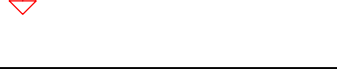
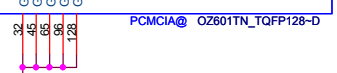
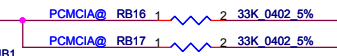
must check IDSEL, PCI_PIRQ#,

20,24 PCI_AD[0..31]

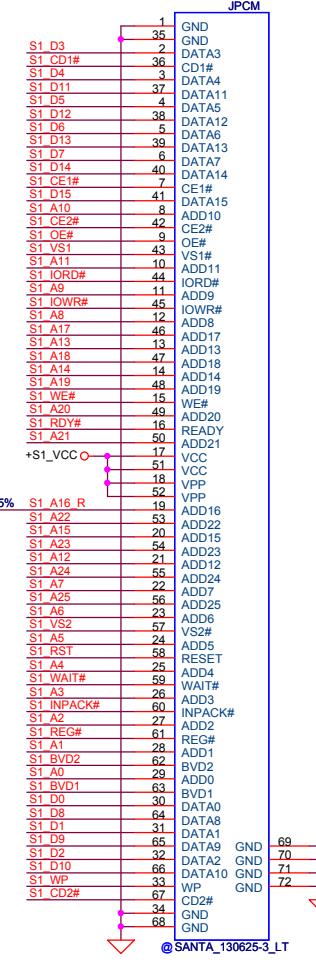
20 PCI_CBE#[0..3]

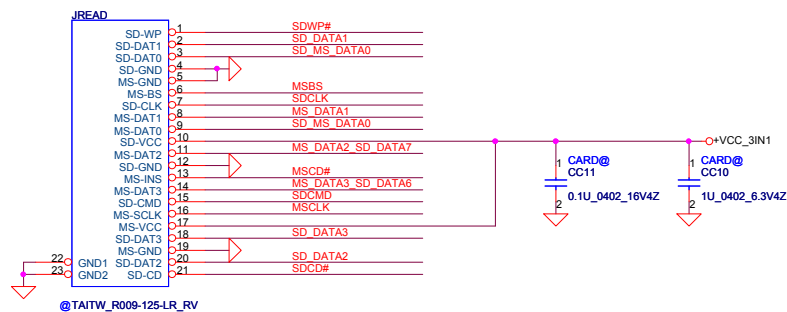
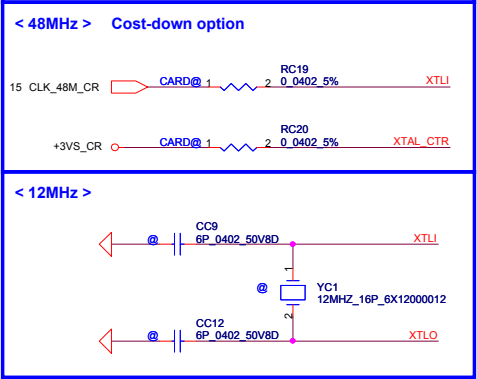


IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)

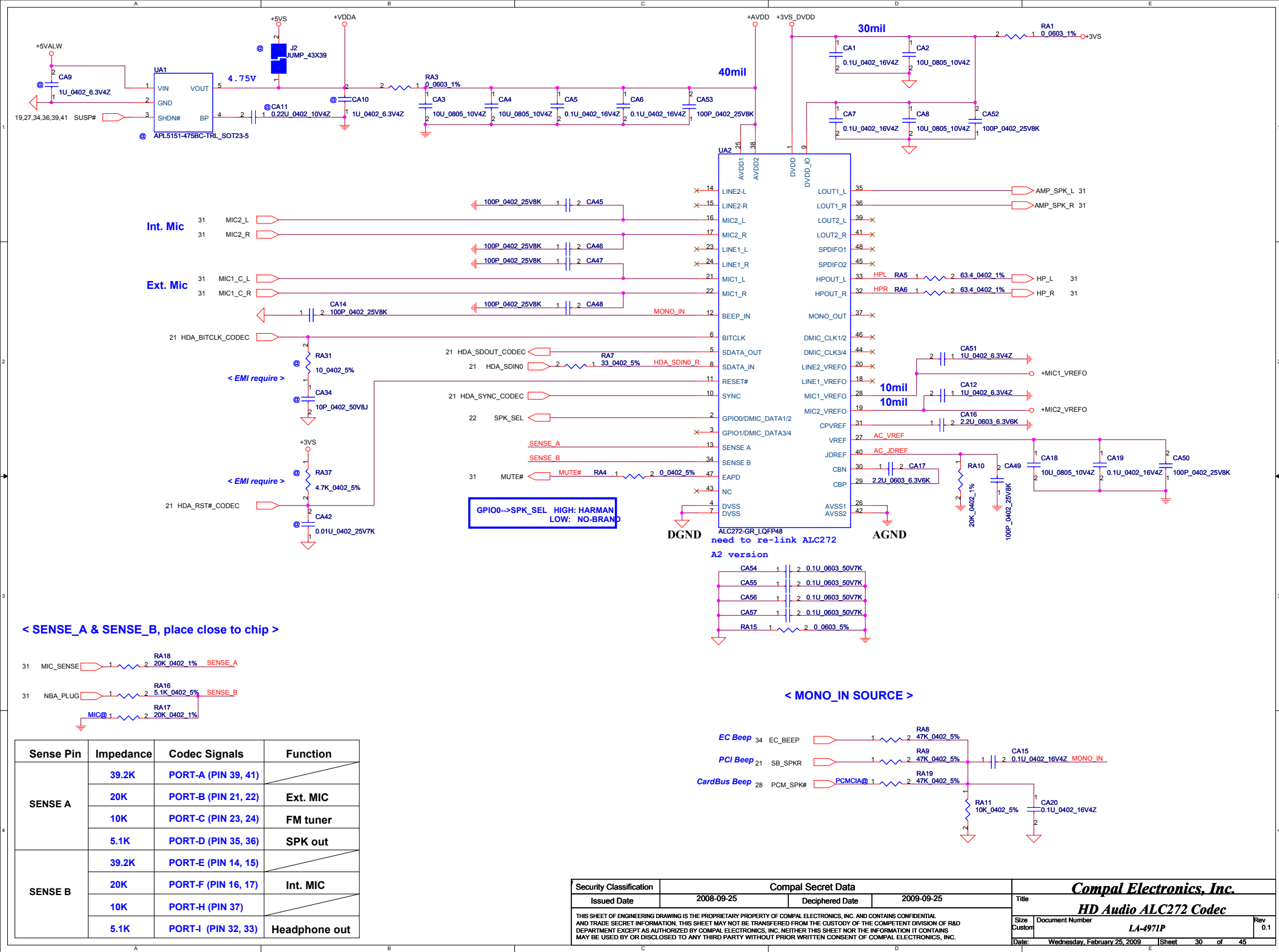


PCMCIA Socket





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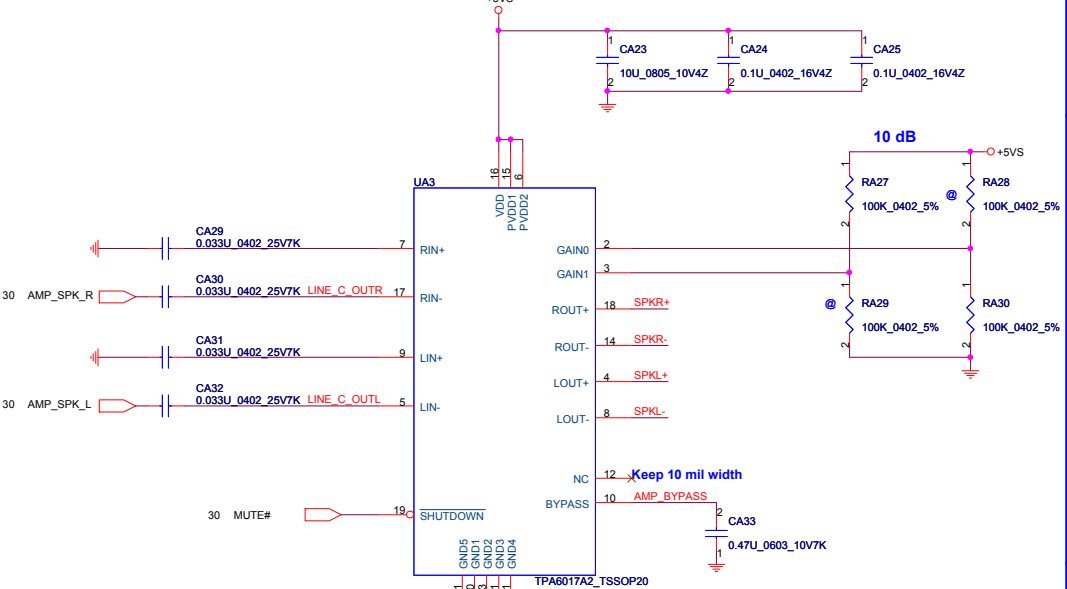


< SENSE_A & SENSE_B, place close to chip >

Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	Ext. MIC
	20K	PORT-B (PIN 21, 22)	
	10K	PORT-C (PIN 23, 24)	FM tuner
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	Int. MIC
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 37)	Headphone out
	5.1K	PORT-I (PIN 32, 33)	

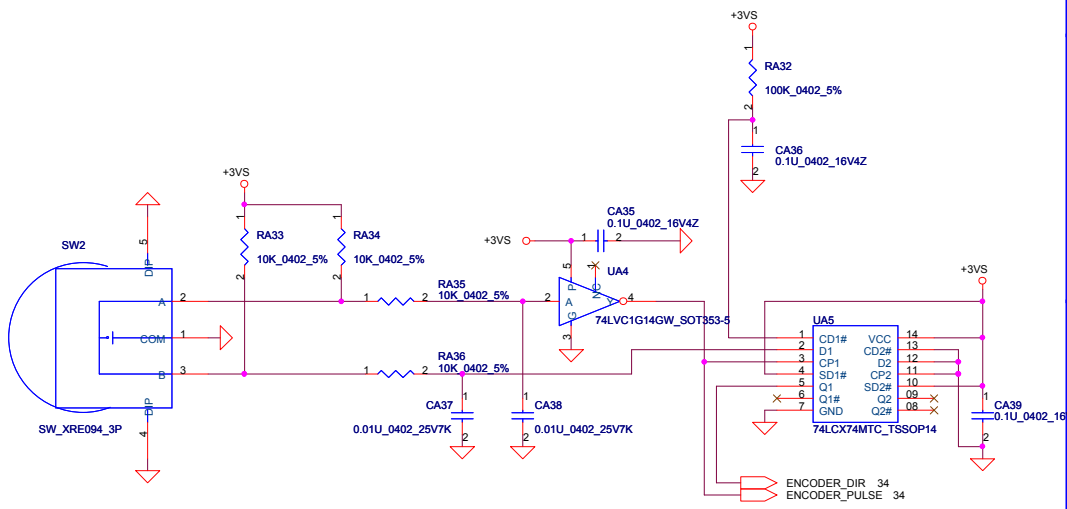
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< TPA6017 Medium Range Amplifier >

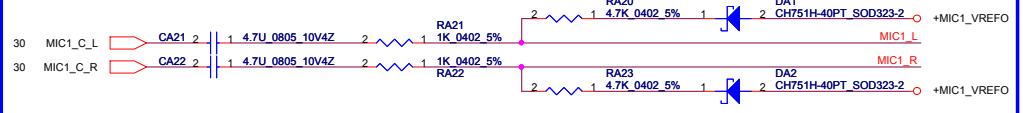


GAIN0	GAIN1	Av (db)	Rin (ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K

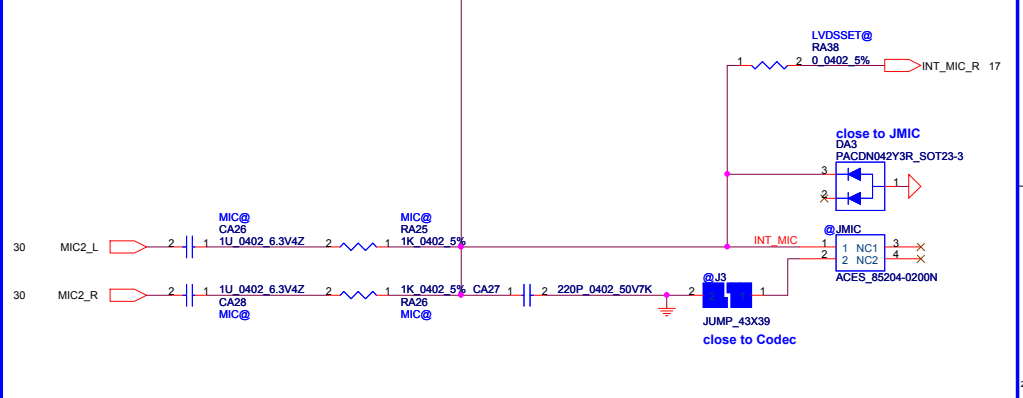
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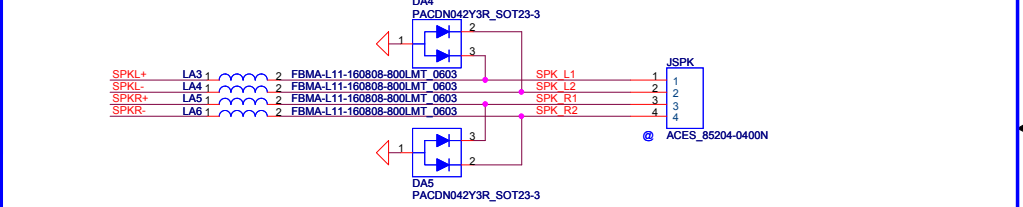
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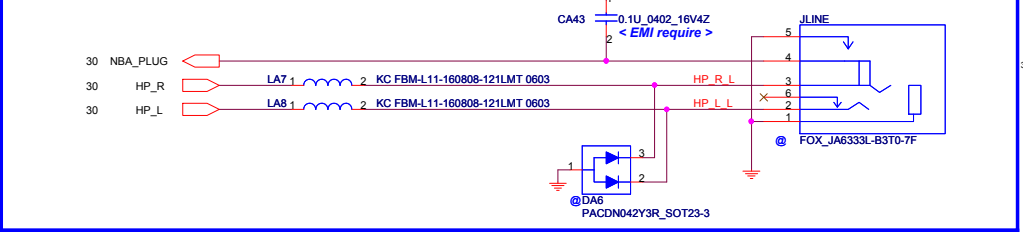
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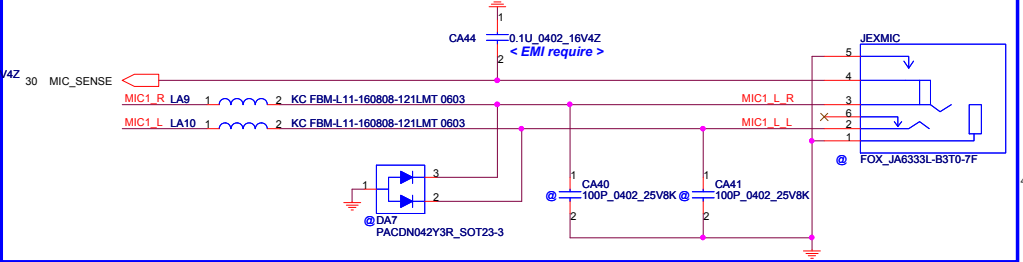
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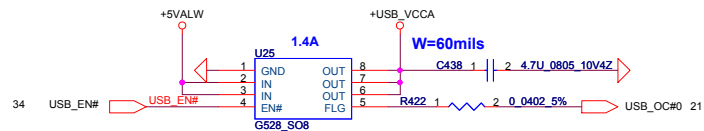
< HeadPhone JACK >



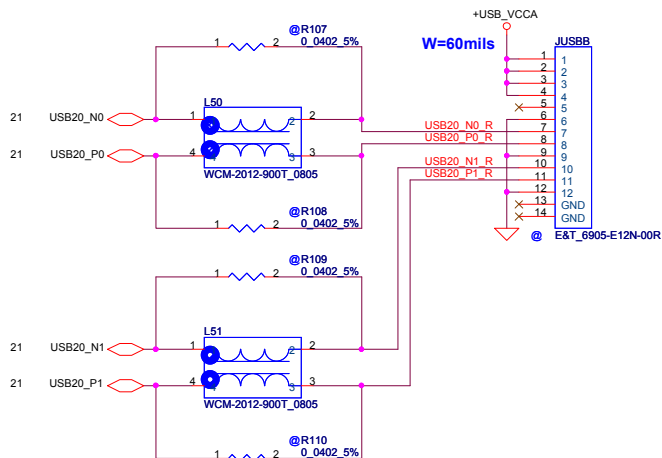
< Ext.MIC/LINE IN JACK >



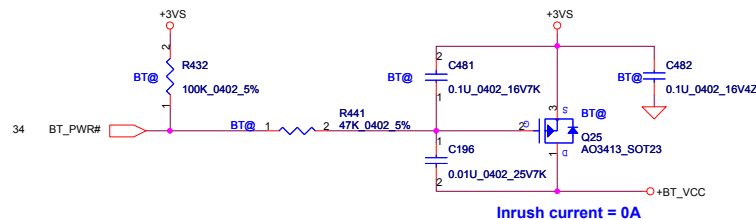
< USB Right-side Board, USB port 0,1 >



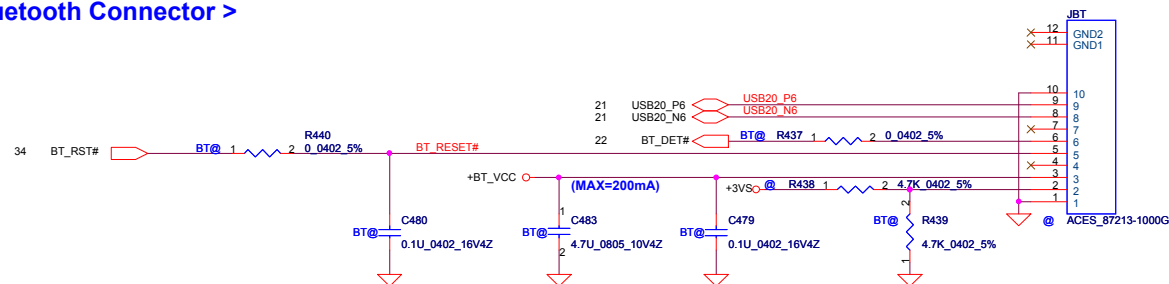
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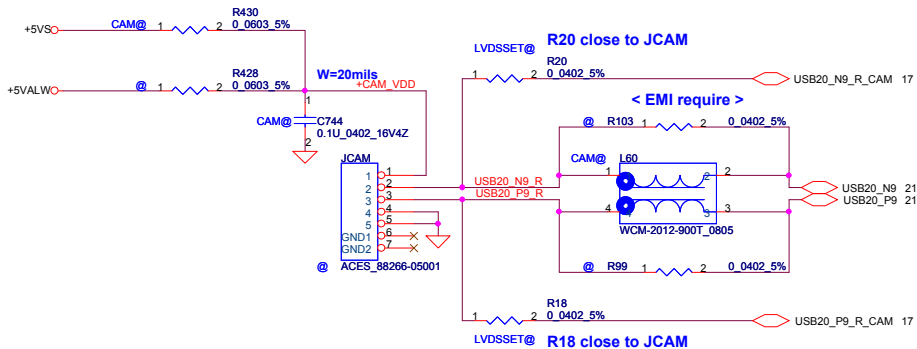
< BlueTooth Interface, USB port6 >



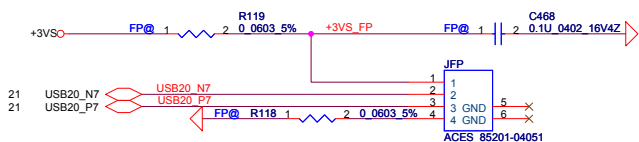
< Bluetooth Connector >



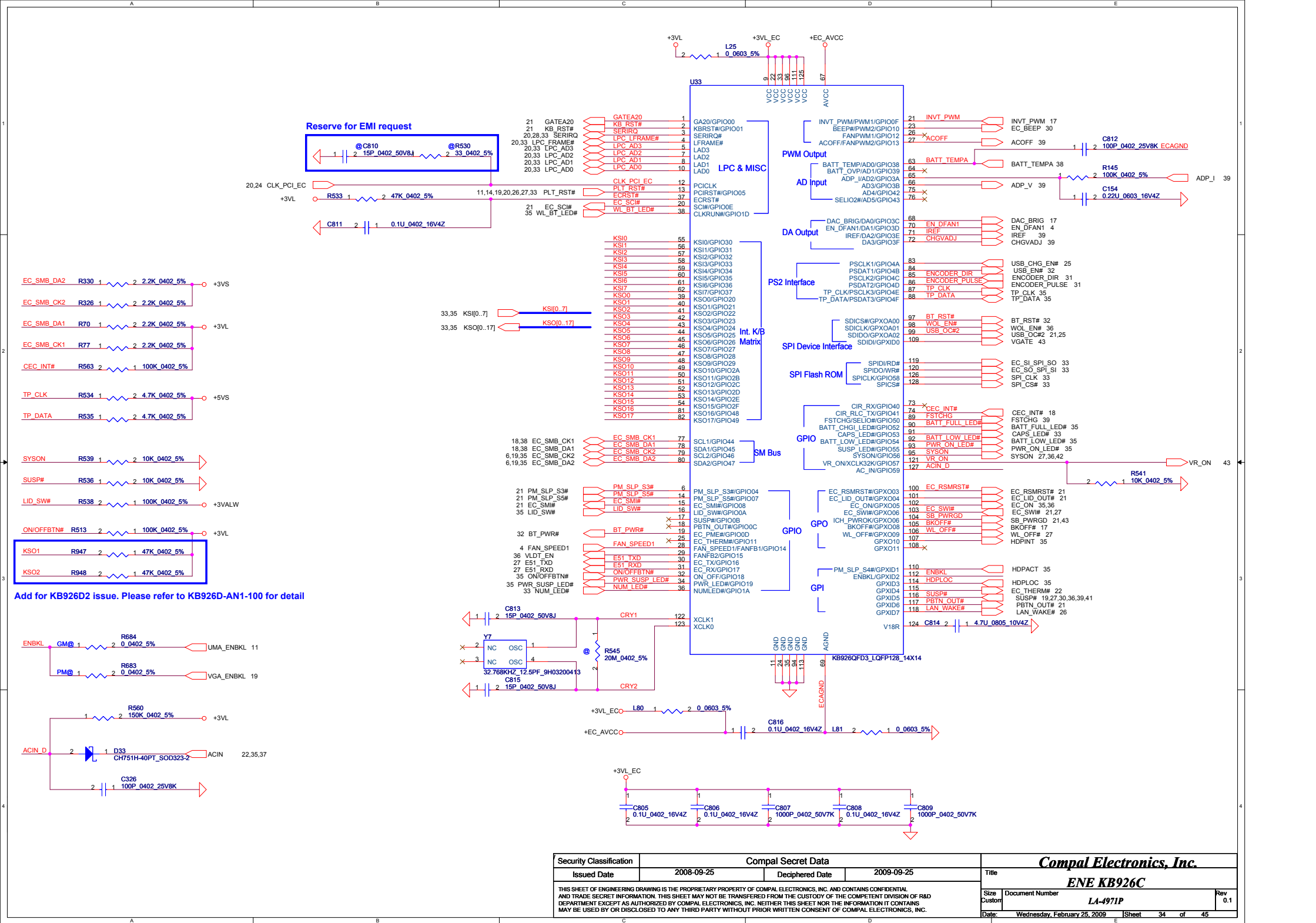
< Int. Camera, USB port 9 >



< Finger Printer, USB port 7 >

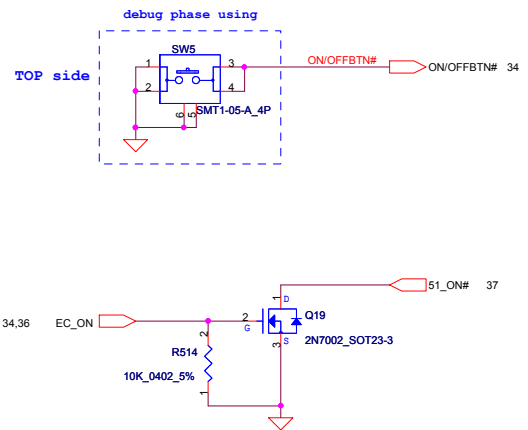


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								Rev			
								0.1			
								Date			
								Wednesday, February 25, 2009			
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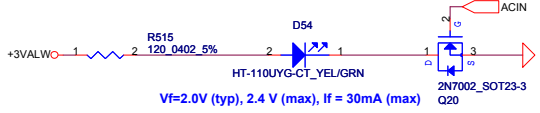


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< Power Button for Debug >

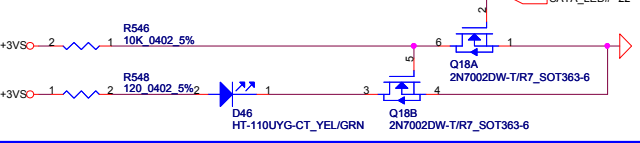


< DC-IN LED >



Remove WiMAX LED control circuit

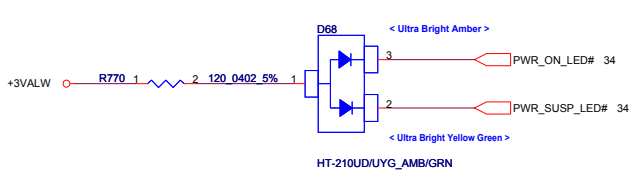
< HDD LED >



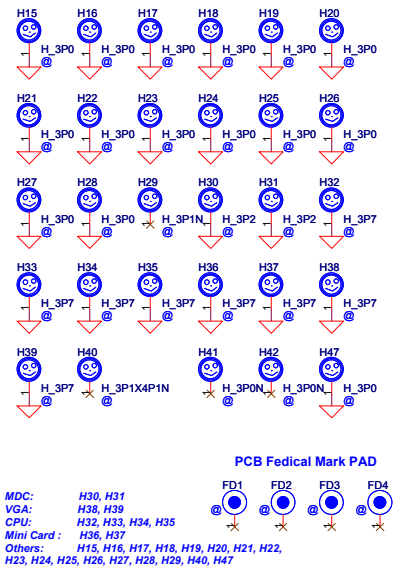
< WL&BT LED >



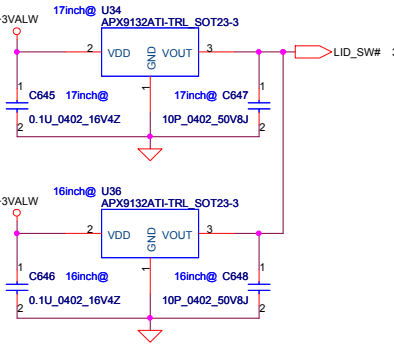
< POWER-ON & SUSPEND LED >



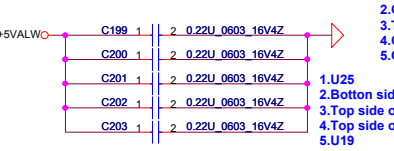
< Screw Hole >



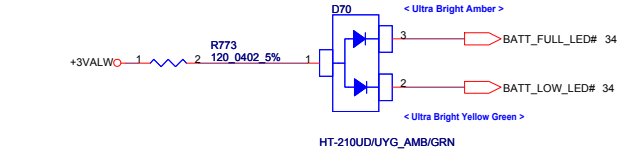
< LID Switch >



< EMI reserve >



< BATT CHARGE/FULL LED >

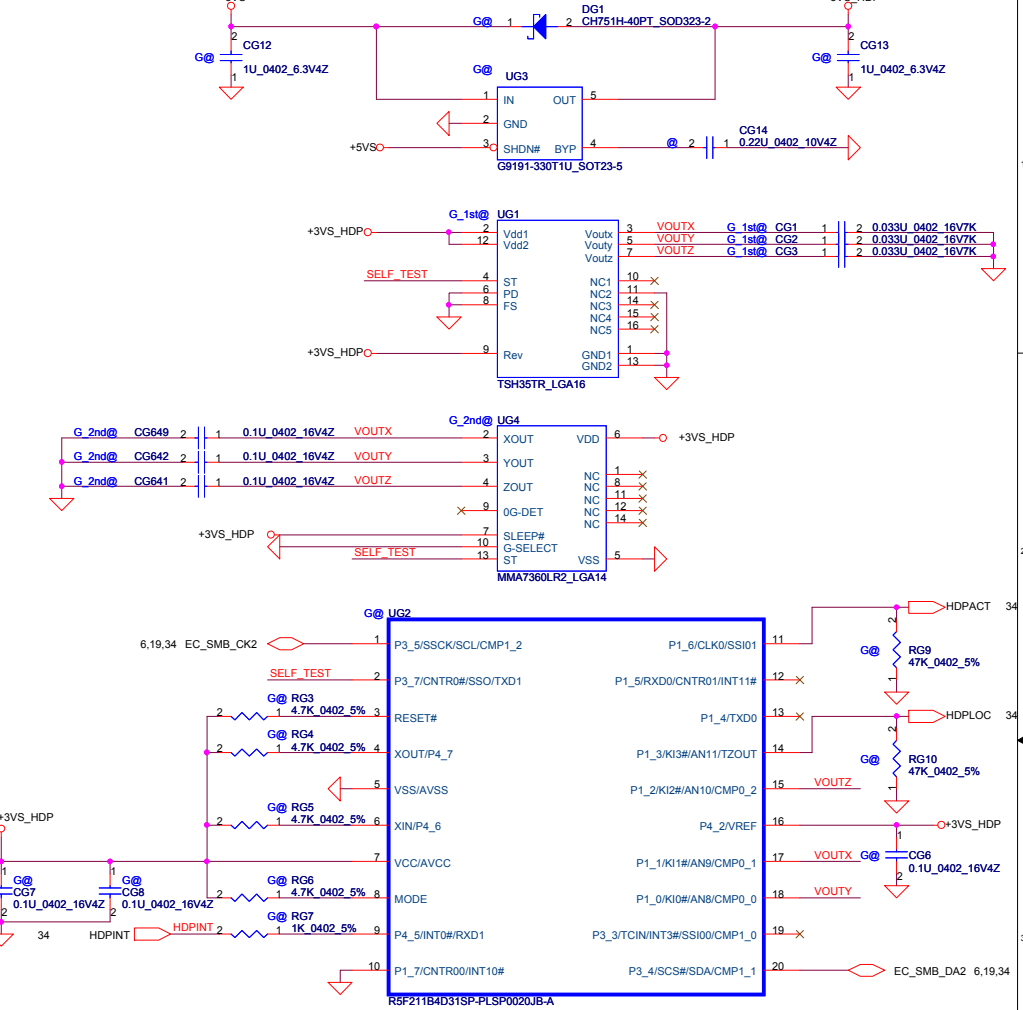


Vf=1.9V(typ),2.4V(max) for amber

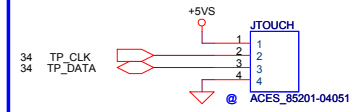
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If=30mA(max)

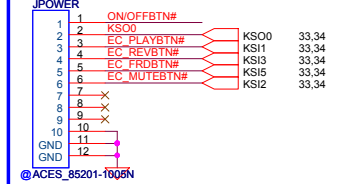
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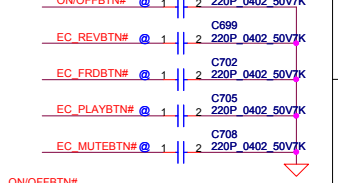
< Touch/B Connector >



< SW/B Connector >

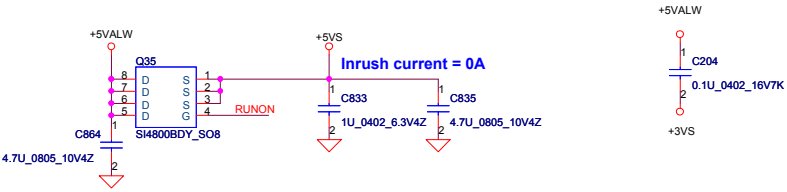


< For EMI >



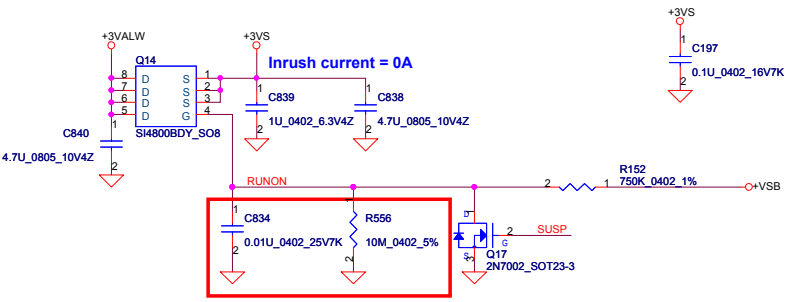
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< +5VALW TO +5VS >



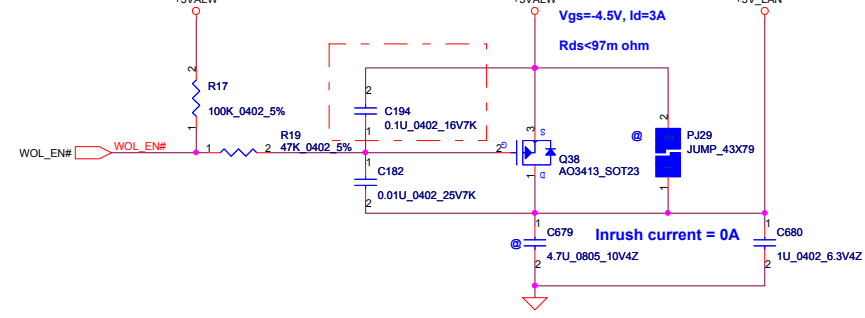
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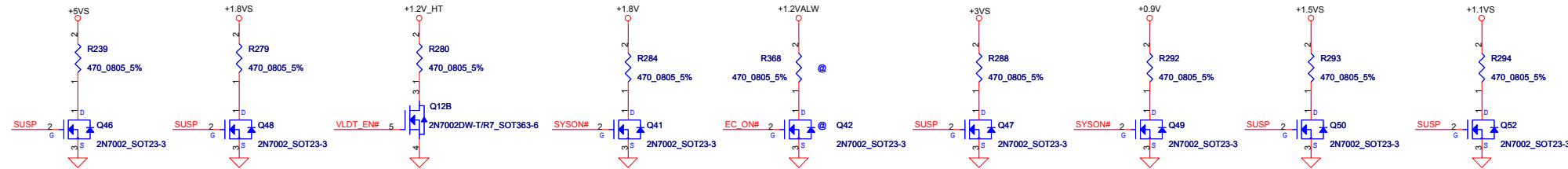


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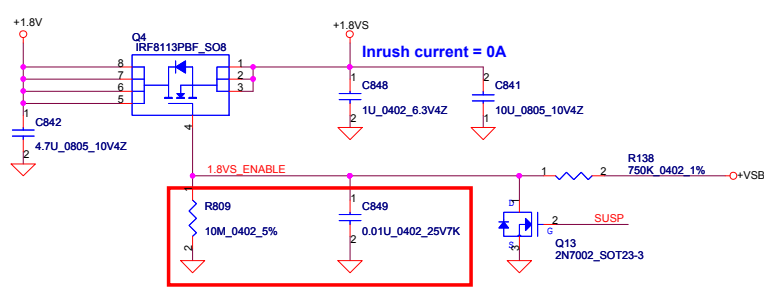
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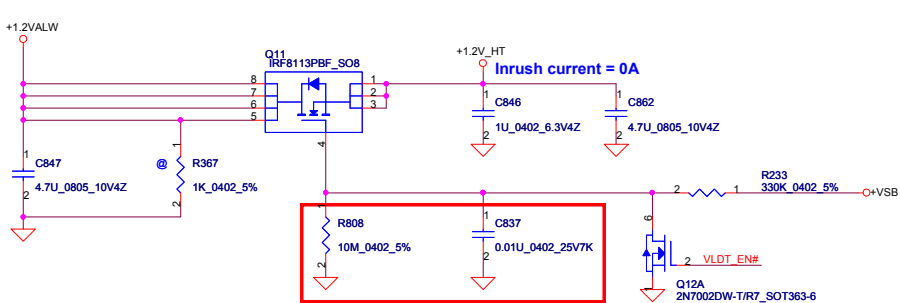
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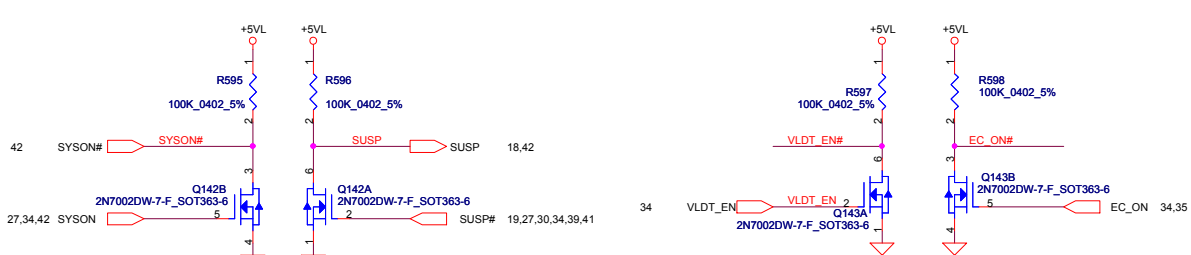
< +1.8V TO +1.8VS >



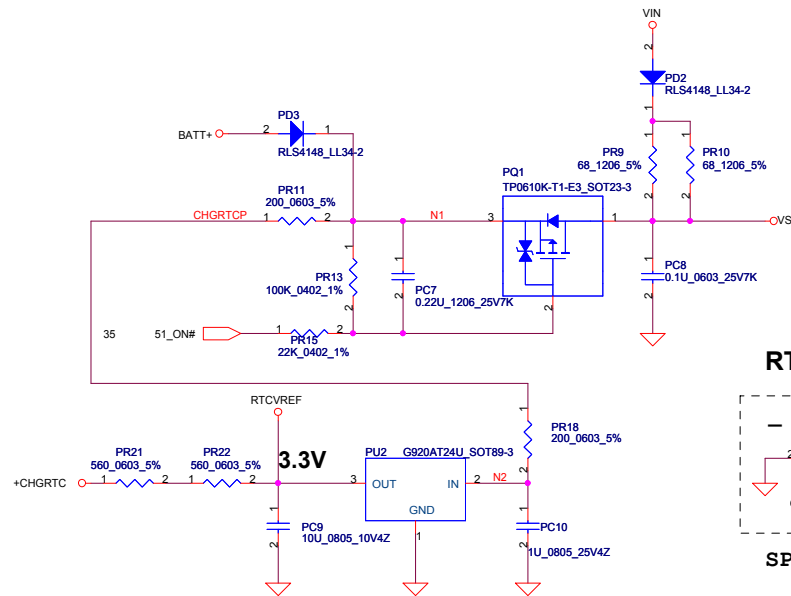
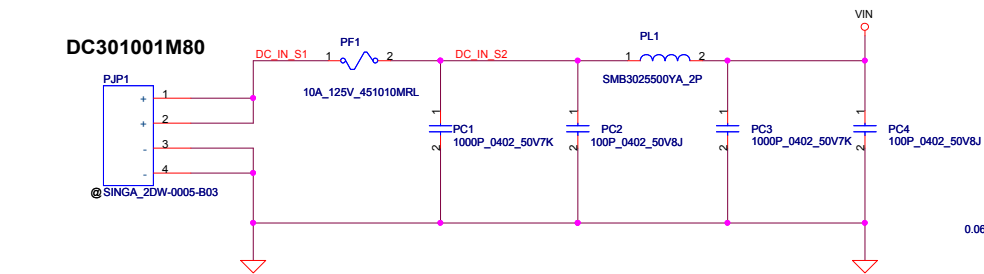
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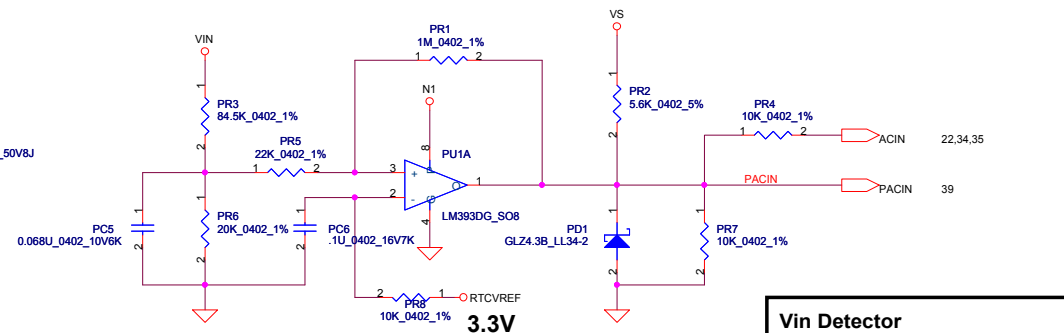
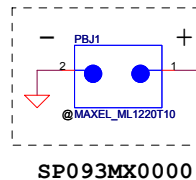
< Inversion of SYSON, SUSP#, VLDT_EN, EC_ON >



DC301001M80

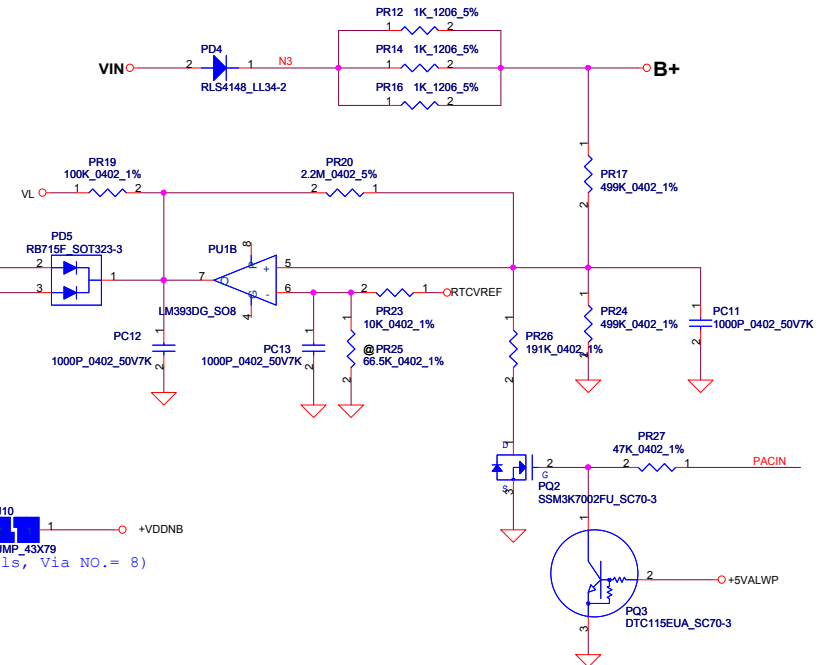


RTC Battery

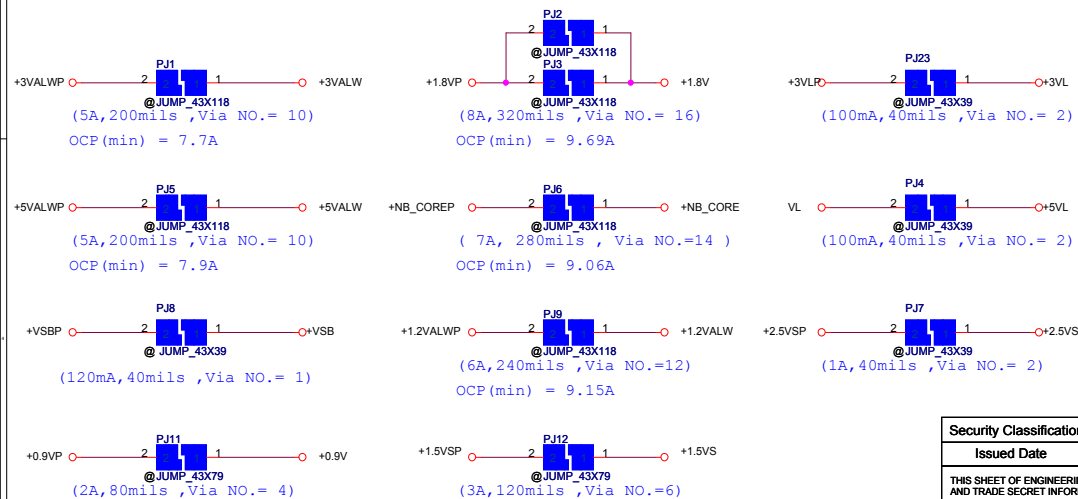


Vin Detector

High 18.384 17.901 17.430
 Low 17.728 17.257 16.976

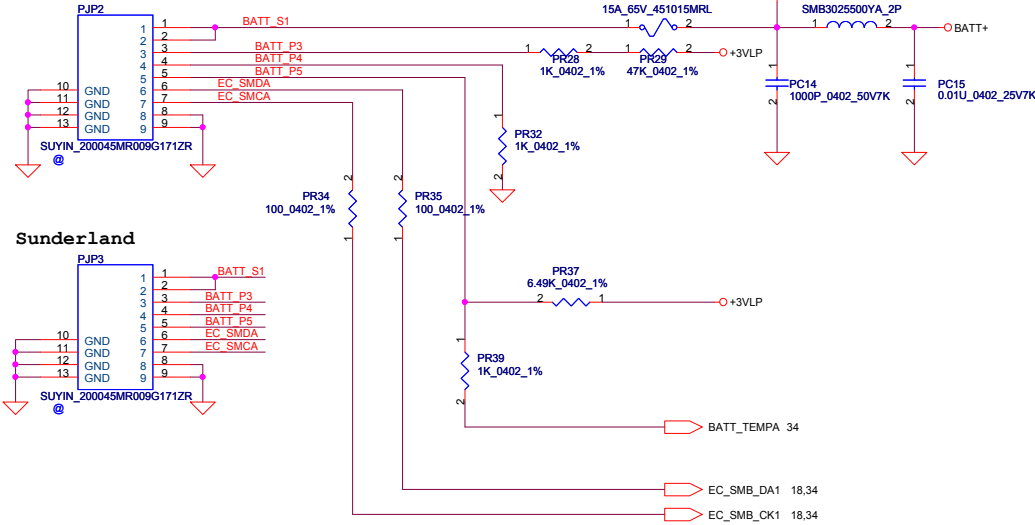


Precharge detector 15.97V/14.84V FOR ADAPTOR

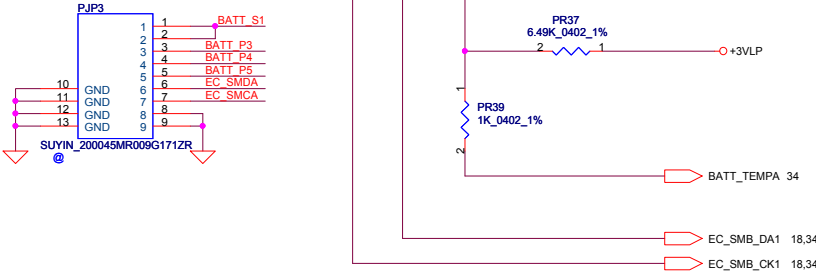


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Liverpool

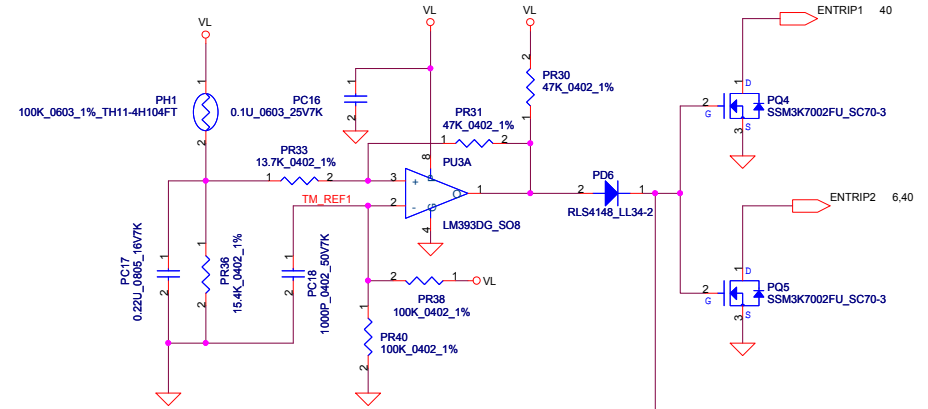


Sunderland



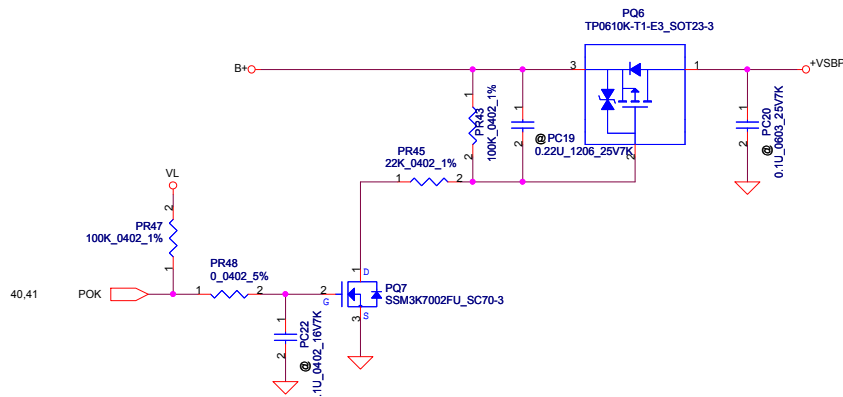
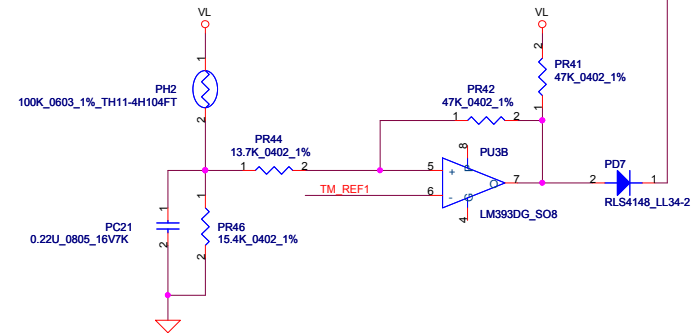
PH1 under CPU botten side :

CPU thermal protection at 92 degree C
Recovery at 56 degree C

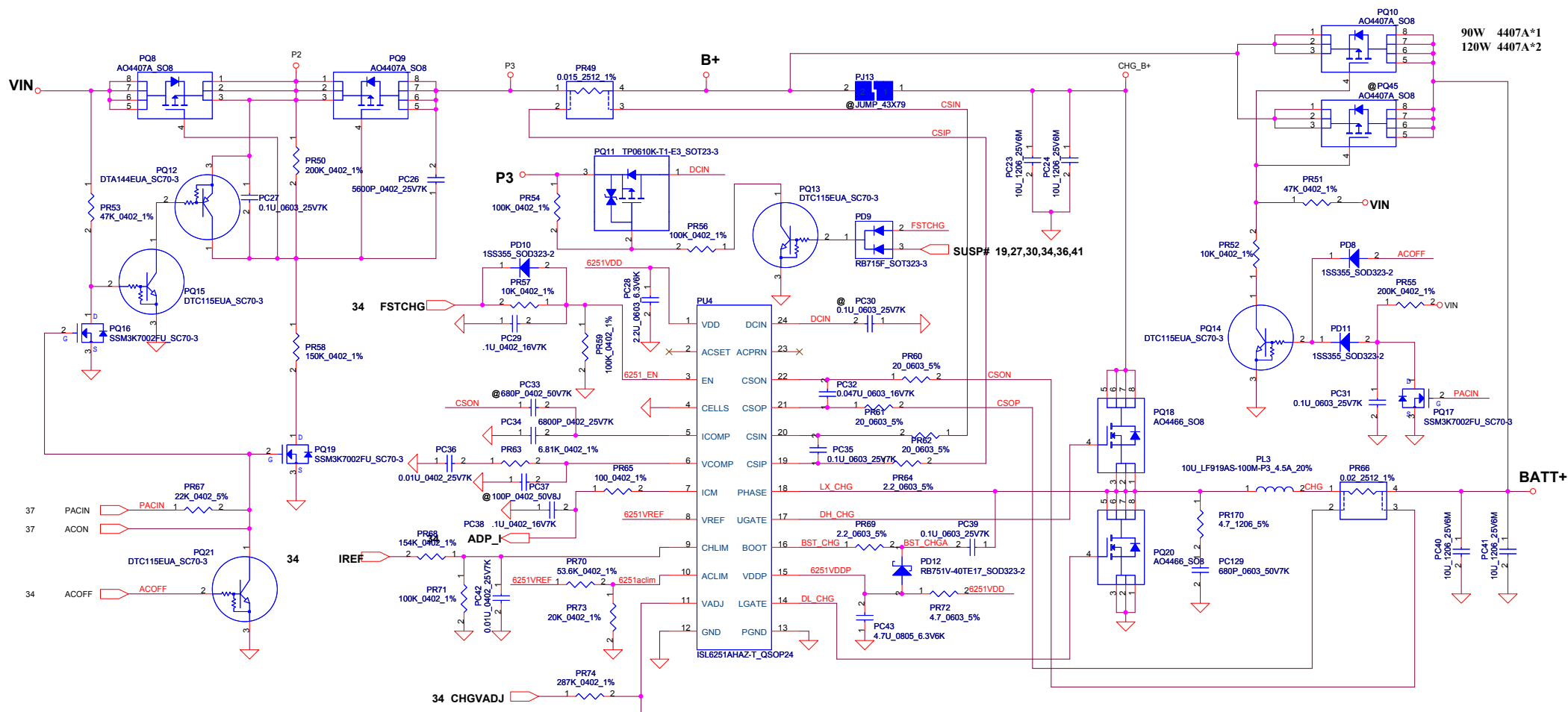


PH2 near main Battery CONN :

BAT. thermal protection at 92 degree C
Recovery at 56 degree C



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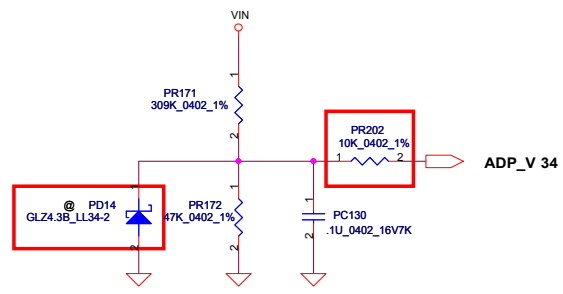
Iada=0~3.421A (65W) CP=3.15A PR49=0.02, PR70=75k, PR73=20k
 Iada=0~3.947A (75W) CP=3.63A PR49=0.02, PR70=24k, PR73=20k
 Iada=0~4.737A (90W) CP=4.36A PR49=0.015, PR70=53.6k, PR73=20k
 Iada=0~6.316A (120W) CP=5.81A PR49=0.015, PR70=8.25k, PR73=26.7k
 CP= 92%*Iada

CP mode
 $V_{ac1m} = 2.39 * (R_b / (152K) + (R_t / (152K + R_b) / 152K))$
 $I_{input} = (1 / PR49) * ((0.05 * V_{ac1m}) / (2.39 + 0.05))$
 where $V_{ac1m} = 1.09986V$, $I_{input} = 3.65A$
 $V_{ac1m} = 0.7717V$, $I_{input} = 4.41A$
 $V_{ac1m} = 0.4204V$, $I_{input} = 5.88A$

CC=0.25A~3A
 IREF=1.016*Icharge
 IREF=0.254V~3.048V
 VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CELLS	VDD	GND	Float
CELL number	4	3	2

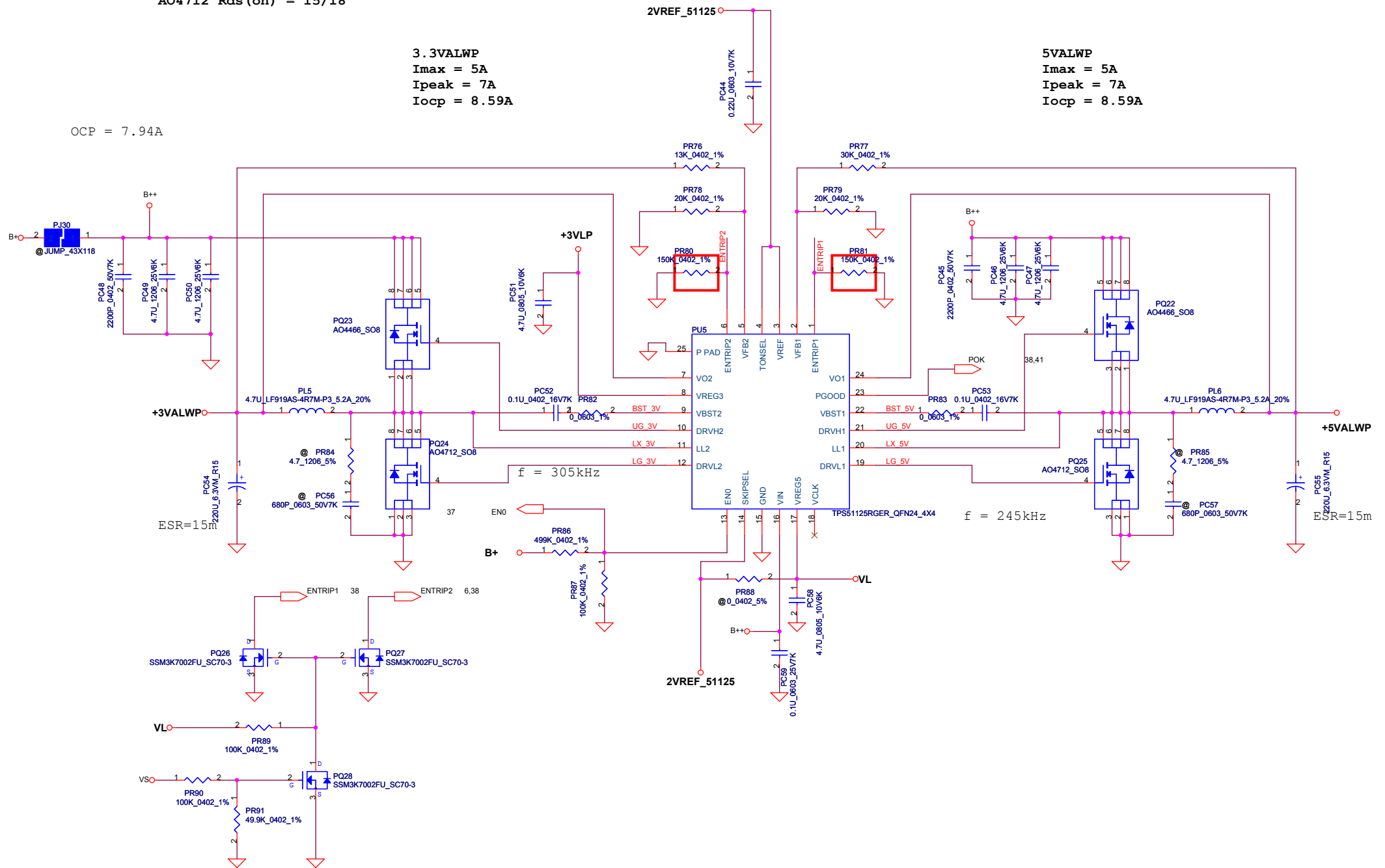


AO4712 Rds(on) = 15/18

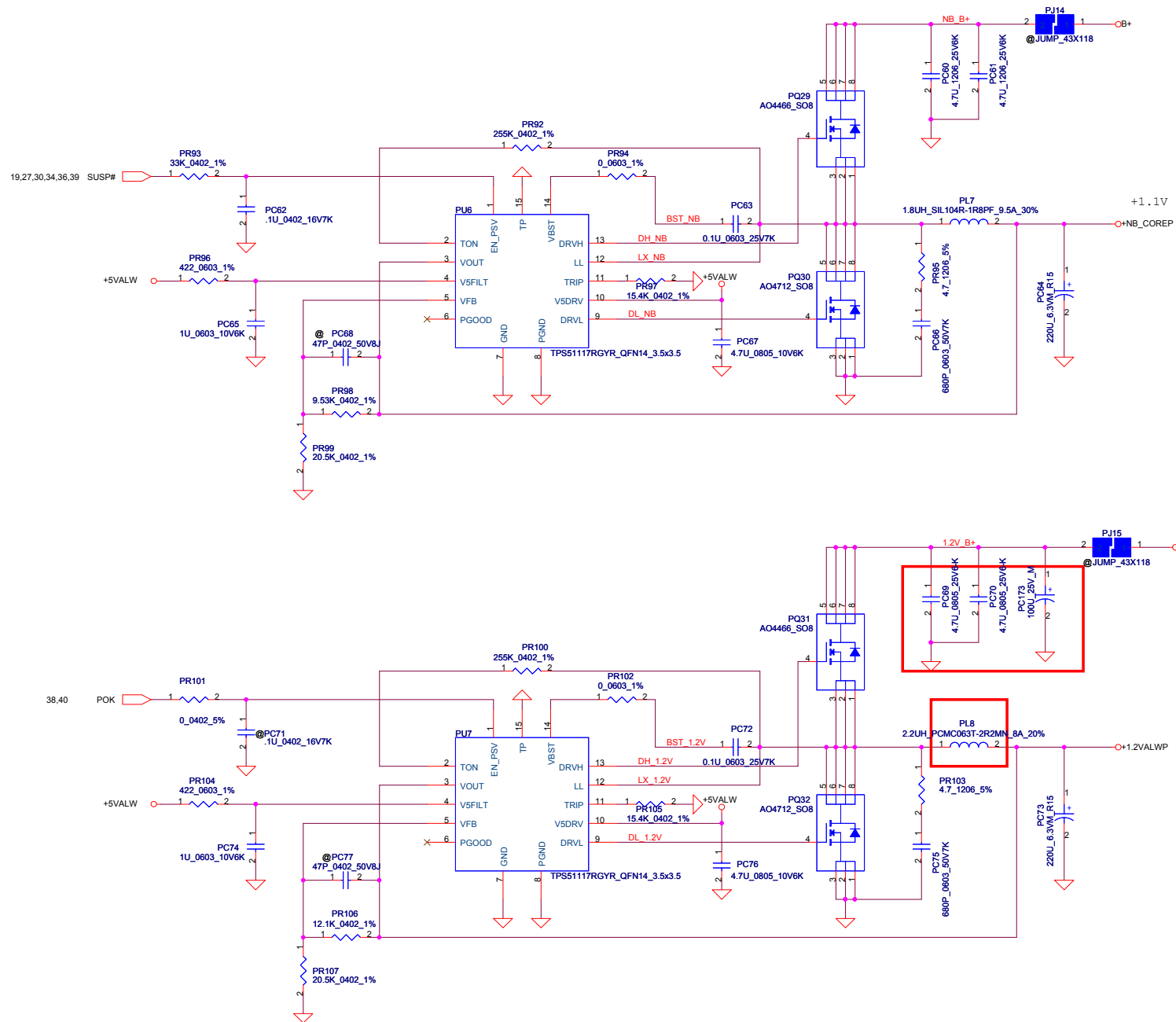
3.3VALWP
Imax = 5A
Ipeak = 7A
Iocp = 8.59A

OCP = 7.94A

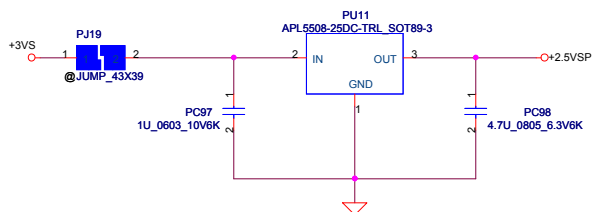
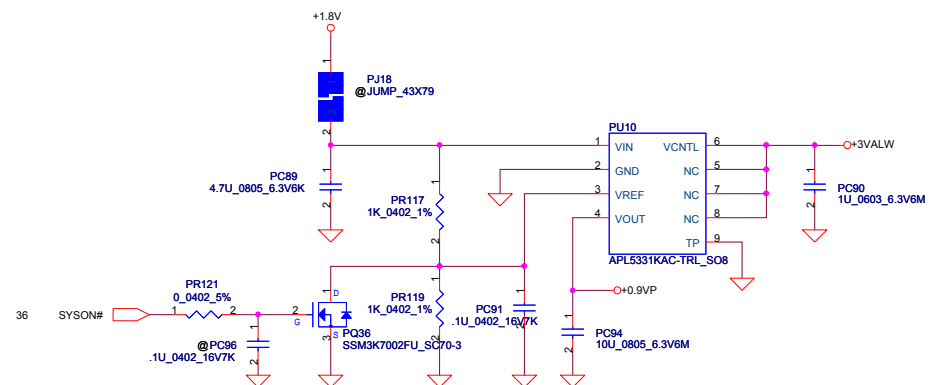
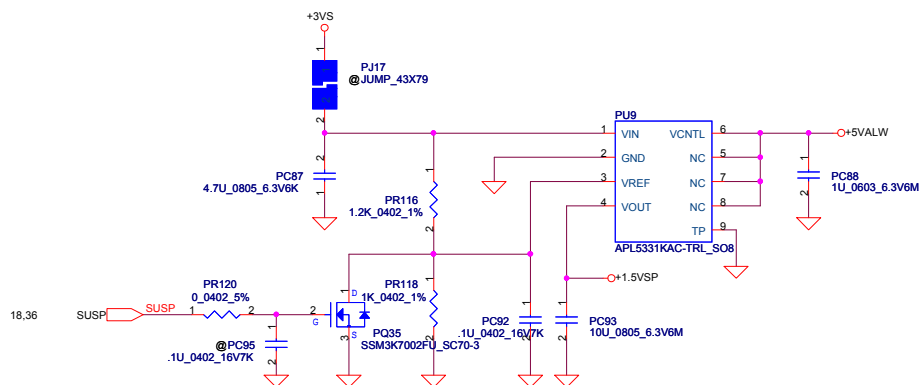
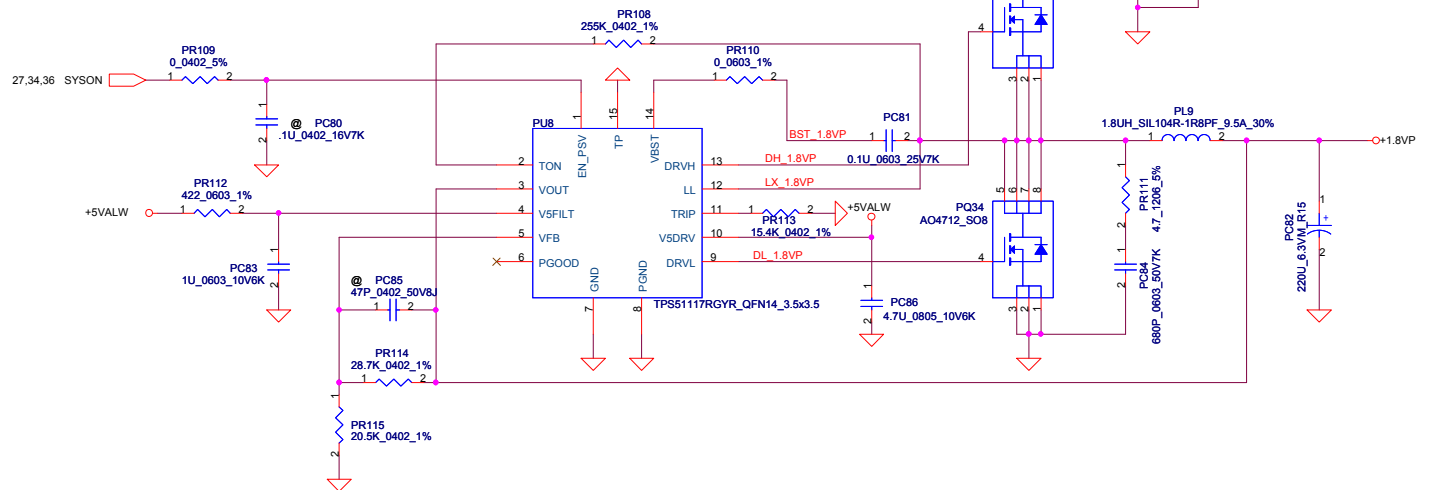
5VALWP
Imax = 5A
Ipeak = 7A
Iocp = 8.59A



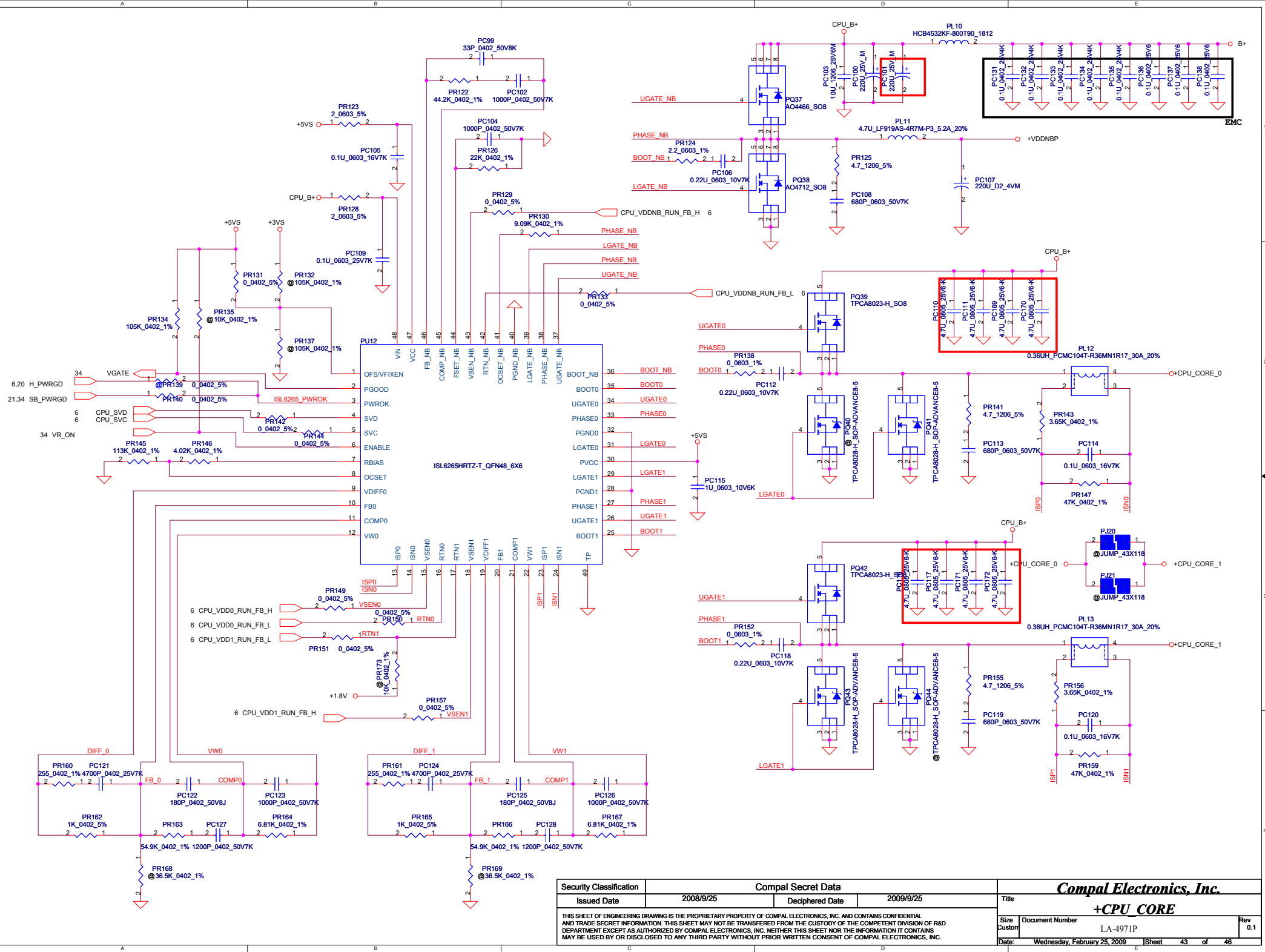
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Issued Date	2008/9/25	Deciphered Date	2009/9/25	1.8VP/0.9VP/1.5VSP2.5VSP	
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								+CPU CORE	
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						LA-4971P			
						Date:		Wednesday, February 25, 2009	

Compal Electronics, Inc.
+CPU CORE

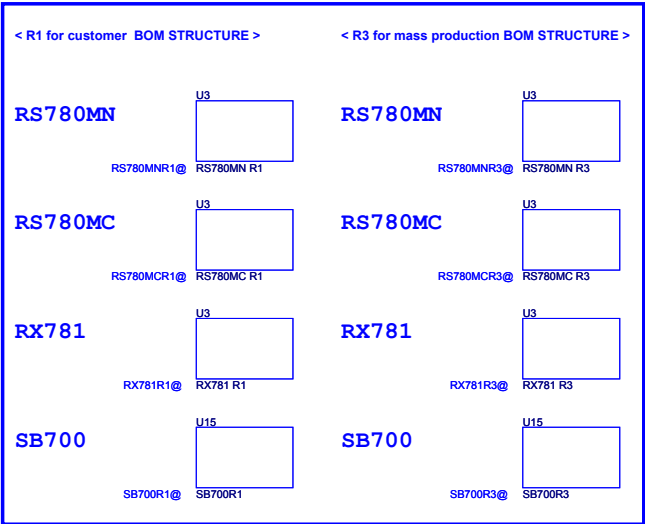
Version Change List (P. I. R, List) for Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1.	2008/11/29	--> change SLP_CHG to SLP_CHG#				57. 2009/02/09 --> change UG1's Value from TIS355AL3TR to TSH35TR	
2.	2008/12/29	--> change HDMI_SCLK and HDMI_SDATA path circuit (add two MOSFETs)				58. 2009/02/09 --> change UL3's P/N to SP050005V00	
3.	2008/12/29	--> connect HDPINT to pin 107 of EC, HDPACT to pin 110 of EC				59. 2009/02/09 --> change R489 & R488 BOM structure	
4.	2008/12/29	--> Change 2nd source of G-sensor to new part				60. 2009/02/09 --> change R142 from 300 ohm to 150 ohm	
5.	2008/12/29	--> Change +3VALW to +3V_LAN soft-start circuit (R=4.7K ohm, C= 0.1uF)				61. 2009/02/09 --> change R143 from 1M ohm to 100K ohm	
6.	2008/12/29	--> Change +BT_VCC circuit (change BT_PWR from high active to low active in pin19 of EC)				62. 2009/02/09 --> change JREAD footprint to TAITW_R009-125-LR_21P_RV-T	
7.	2008/12/29	--> Change +LCD_VDD circuit (change +3VALW to +3VS(R143) and add 0.1uF cap to +3VS)				63. 2009/02/09 --> change C867 from 0.1u_0603 to 680pF_0402	
8.	2008/12/29	--> add pull-down resistor R146 to BKOFF# to prevent backlight flash when power down				64. 2009/02/09 --> change +HDMI_5V_OUT circuit, add D18, R160, Q26, R557, C876 and change power	
9.	2008/12/29	--> connect SHDN# of UG3 to +5VS and remove EC_HDPPD				65. 2009/02/11 --> change UG1 P/N to SA000039900	
10.	2008/12/29	--> connect PD of UG1 to GND and remove EC_HDPPD				66. 2009/02/12 --> change CV2 to C706	
11.	2008/12/29	--> Let 0G-DET of UG4 float				67. 2009/02/12 --> change PCMCIA connector	
12.	2008/12/29	--> connect SLEEP# to +3VS_HDP and remove EC_HDPPD				68. 2009/02/12 --> remove WIMAX LED control circuit	
13.	2008/12/29	--> Connect G-SELECT to GND				69. 2009/02/17 --> remove Audio codec digital GND to analog GND net	
14.	2008/12/29	--> Connect pin10 of UG2 to GND and remove HDPPD				70. 2009/02/17 --> add NPTH Hole H41, H42	
15.	2008/12/29	--> Add HDPLOC to pin14 of UG2				71. 2009/02/17 --> change JTOUCH footprint	
16.	2008/12/29	--> Change pin99 of EC from EC_HDPPD to USB_OC#2 and remove EC_HDPPD				72. 2009/02/17 --> add CA12	
17.	2008/12/29	--> Change pin107 of EC to HDPINT				73. 2009/02/17 --> change Int MIC ground to AGND between CA27 and J3	
18.	2008/12/29	--> Change pin110 of EC to HDPACT				74. 2009/02/17 --> add JPOWER1 for co-lay	
19.	2008/12/29	--> Change pin114 of EC from USB_OC#2 to HDPLOC				75. 2009/02/17 --> change NEWCARD power switch (UN1) to TI SA00001SL20	
20.	2008/12/29	--> add R689				76. 2009/02/17 --> add CA45, CA46, CA47, CA48, CA49, CA50, CA51, CA52, CA53	
21.	2009/01/13	--> change the footprint of L47, L48 and L49 to R_0402				76. 2009/02/17 --> replace RA12, RA13, RA14 with CA54, CA55, CA56 and add CA57	
22.	2009/01/19	--> add differential clock name CLK_CPU_BCLK_R & CLK_CPU_BCLK_R#				77. 2009/02/17 --> change JPOWER1 to JPWR1	
23.	2009/01/19	--> change 3 in 1 card reader connector to push-pull type				78. 2009/02/23 --> change R70, R77 from 4.7K to 2.2K	
24.	2009/01/19	--> change the pin158 of MXM connector from GND to NC				79. 2009/02/23 --> change R178 from 4.7K to 47K	
25.	2009/01/19	--> add BOM structure of C1, C2 and C7 for Tigris				80. 2009/02/26 --> change SPI ROM from SST to MXIC	
26.	2009/01/19	--> add R486, R487, R488, R489 & R27 for Tigris					
27.	2009/01/19	--> add R497, R498, R499, R500 for tigris					
28.	2009/01/19	--> add R29, R31 & R32 for Tigris					
29.	2009/01/19	--> add C54 for Tigris					
30.	2009/01/19	--> add R187 for Tigris					
31.	2009/01/19	--> change RL2 from 10Kohm to 1Kohm suggested by vendor					
32.	2009/01/19	--> change CL14 from 0.1uF to 1uF suggested by vendor					
33.	2009/01/19	--> change RL4 from 100Kohm to 10Kohm suggested by vendor				Power circuit: 1. 2008/02/03 --> add +1.8V to CPU_VDD1_RUN_FB_L for Tigris platform add PR173 10K unmount	
34.	2009/01/19	--> remove kill switch and add R87					
35.	2009/01/21	--> add card reader BTO					
36.	2009/01/21	--> change Q33, Q34, Q139 & Q140 symbol				2. 2008/02/03 --> add jump PJ20, PJ21 to connect +CPU_CORE_0 and +CPU_CORE_1 for Tigris platform add PJ20, PJ21	
37.	2009/01/22	--> add +1.8V to CPU_VDD1_RUN_FB_L for Tigris platform (add PR173 10K unmount)					
38.	2009/01/22	--> add jump PJ20, PJ21 to connect +CPU_CORE_0 and +CPU_CORE_1 for Tigris platform (add PJ20, PJ21)				3. 2008/02/03 --> remove PR148, PR153, PR154, PR158, HW already reserves these components	
39.	2009/01/22	--> remove PR148, PR153, PR154, PR158, HW already reserves these components					
40.	2009/01/22	--> PU1 VCC issue, VCC later than input signals results in output pin drop (connect N1 to PU1 VCC)				4. 2008/02/03 --> PU1 VCC issue, VCC later than input signals results in output pin drop connect N1 to PU1 VCC	
41.	2009/02/02	--> add C182, C195, C196 for soft-start, change R441 to 47K ohm, change R19 to 47K ohm, change R140 to 47K ohm					
42.	2009/02/02	--> change BT PWR from +5VS to +3VS(R432)				5. 2008/02/04 --> shift PR173 to pin17	
43.	2009/02/02	--> remove kill SW component, delete KILL_SW# on EC, connect WL_OFF# to JWLAN pin20 directly.					
44.	2009/02/02	--> change +HDMI_5V_OUT circuit				6. 2009/02/17 --> modify ADP_V too low situation. Add PR202 and change PD14 to unpop.	
45.	2009/02/03	--> change DA3-DA7 to SCA00000G00					
46.	2009/02/03	--> change JREAD from TAITW_R009-135-LR_21P_RV-T to TAITW_R009-125-LR_RV				7. 2009/02/17 --> for noise solution : 1.change PL8 to 2.2uH molding. 2.change PC69, PC70 to 0805 size 4.7uF add PC173 100uF. 3.change PC110, PC111, PC116, PC117 to 0805 size 4.7uF. 4.add PC169, PC170, PC171, PC172 0805 size 4.7uF. 5.change PC101 to mount	
47.	2009/02/03	--> add J3 in int-MIC					
48.	2009/02/04	--> change USB port of New card from port11 to port5				8. 2009/02/17 --> for common circuit. change 3/5V trip resistor PR80, PR81 to 150K	
49.	2009/02/04	--> modify HDMI CEC power & related circuit.					
50.	2009/02/05	--> add 3PCS Cap.=0.1uF_0402 (PC136 to PC138) on B+					
51.	2009/02/05	--> add snubber circuit : PR155, PR141, PR111, PR103, PR95, PR170; PC119, PC113, PC84, PC75, PC66, PC129					
52.	2009/02/05	--> change PR74 to 287K, PR75 to 499K					
53.	2009/02/05	--> add C197 on +3VS and close to PQ20 (Place EMI confirm)					
54.	2009/02/05	--> add C204 between +3VS with +5VALW and close to PQ20 (Place EMI confirm)					
55.	2009/02/05	--> add D76, R966, R965 on LPC_FRAME#					
56.	2009/02/09	--> change UG3					

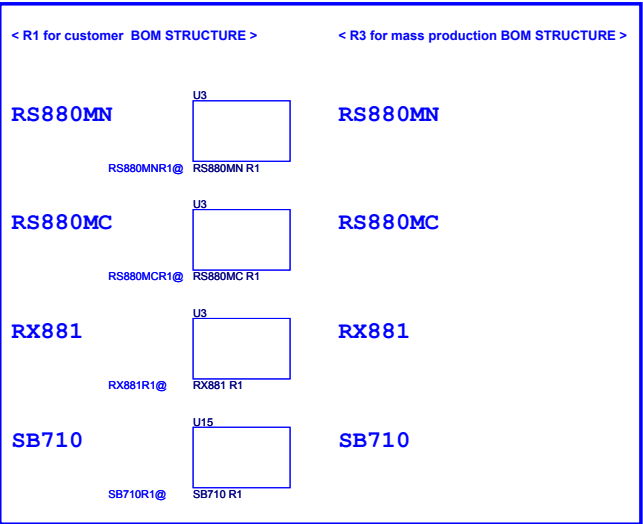
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HW4 Product Improvement Record (P.I.R.)

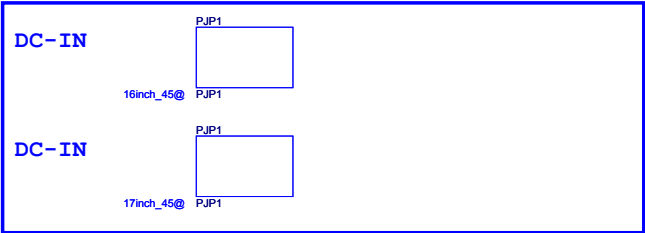
< Liverpool & Sunderland >



< Tigris >

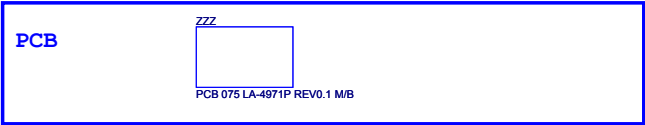


< DC Jack >



Use MEMO : change UG1 R5F211B4D31SP (SA000037Y60) to R5F211B4D34SP (SA00003A600)

< PCB >



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