

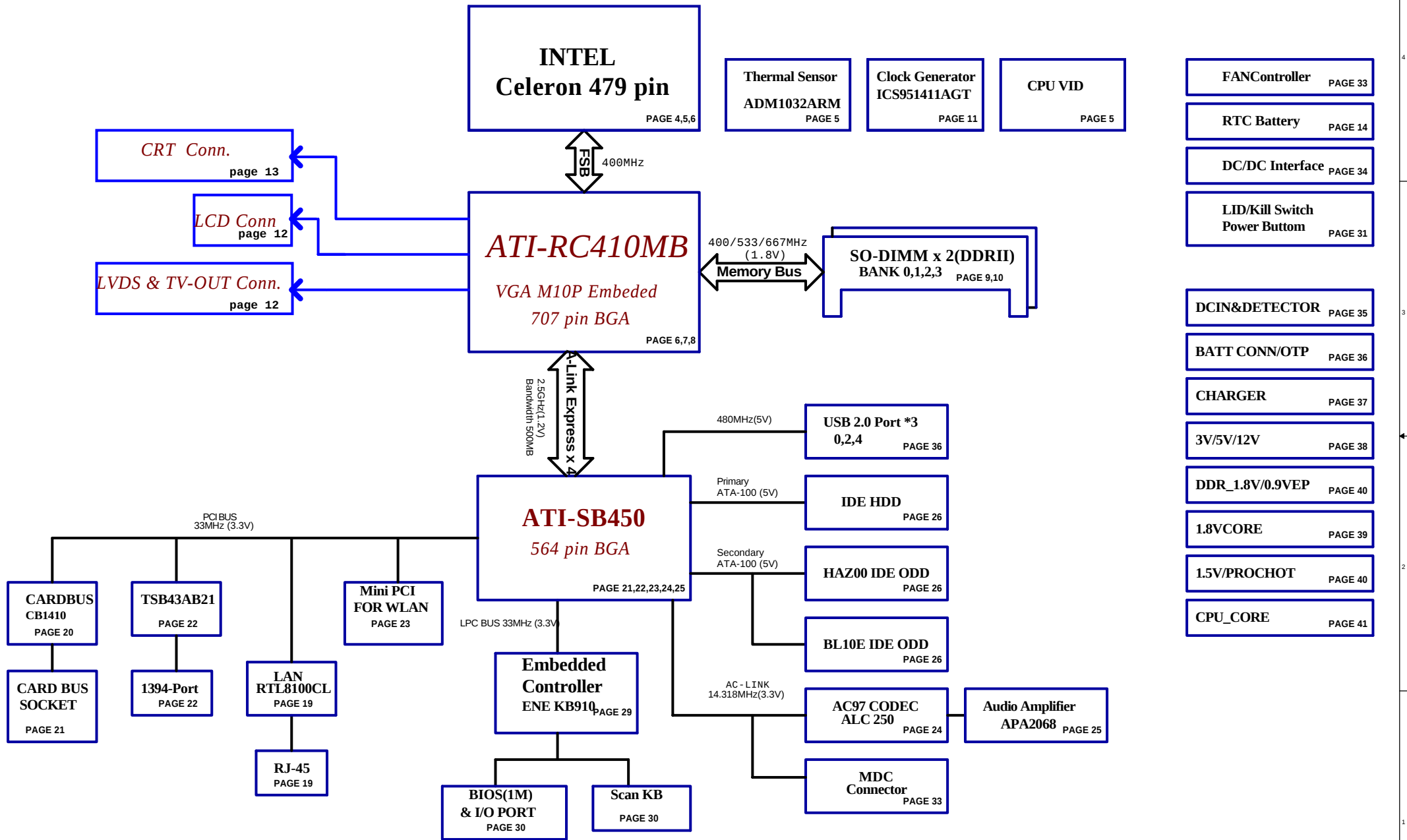
HAZ00/HTW01

LA-2861 REV 1.0 Schematic

UFC-PGA Dothan/ RC410MD(RC410MB)/ SB450
2005-07-11 Rev.1.0

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				Date: Thursday, August 04, 2005	Sheet 1 of 42
				Rev 1.0	

HAZ00 & HTW01 LA-2861 FUNCTION BLOCK DIAGRAM



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				Date	Thursday, August 04, 2005
				Sheet	2 of 42

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VGA_CORE	1.0V/1.2V switched power rail for VGA chip	ON	OFF	OFF
+1.2VS	1.2VS for PCI-Express	ON	OFF	OFF
+0.9VS	0.9V switched power rail	ON	OFF	OFF
+1.5VS	DOTHAN B	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8V	1.8V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
TI 1410	AD20	2	PIRQA/PIRQB
LAN	AD22	1	PIRQG
Mini-PCI(WLAN)	AD18	3	PIRQF/PIRQG
1394	AD16	0	PIRQA

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b

EC SM Bus2 address

SB450 SM Bus address

Device	Address
Clock Generator (ICS9514138GLFT)	1101 001Xb
DDR DIMM0	1010 0100b A4
DDR DIMM1	1010 0110b A6

STATE	SIGNAL					
	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

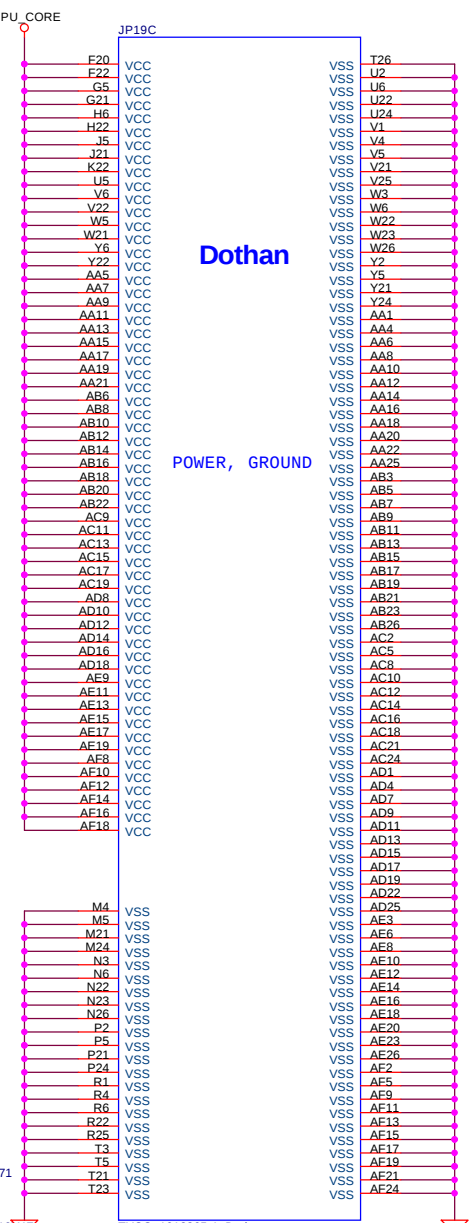
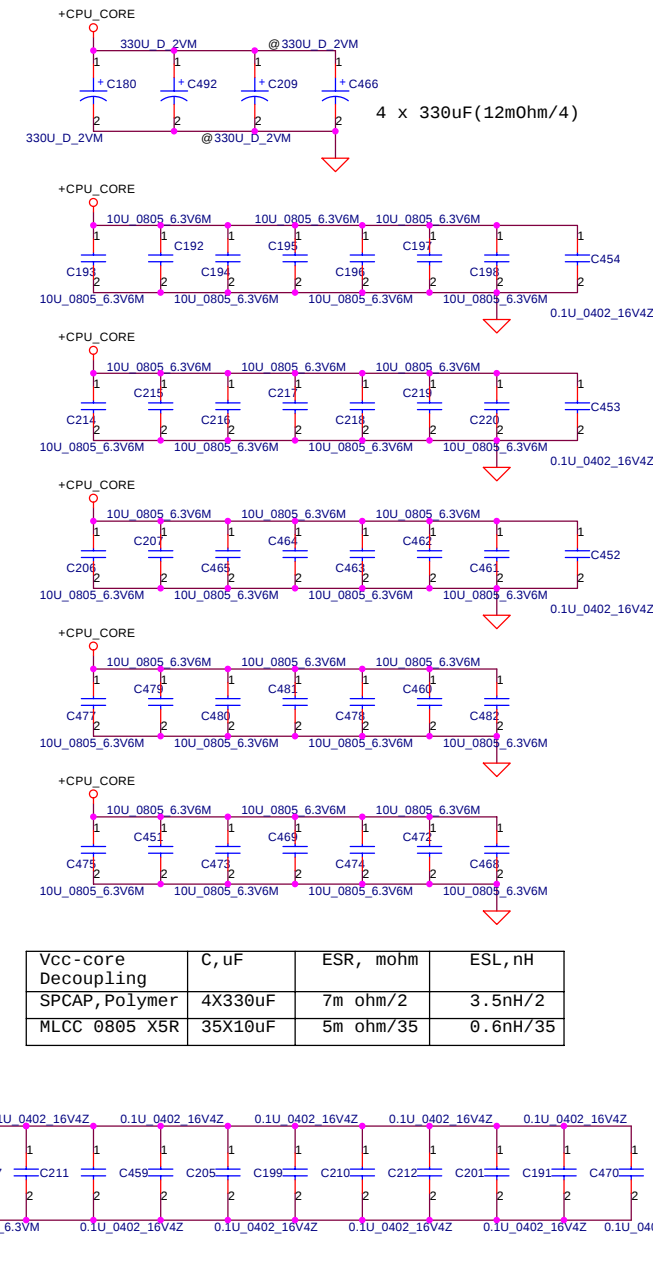
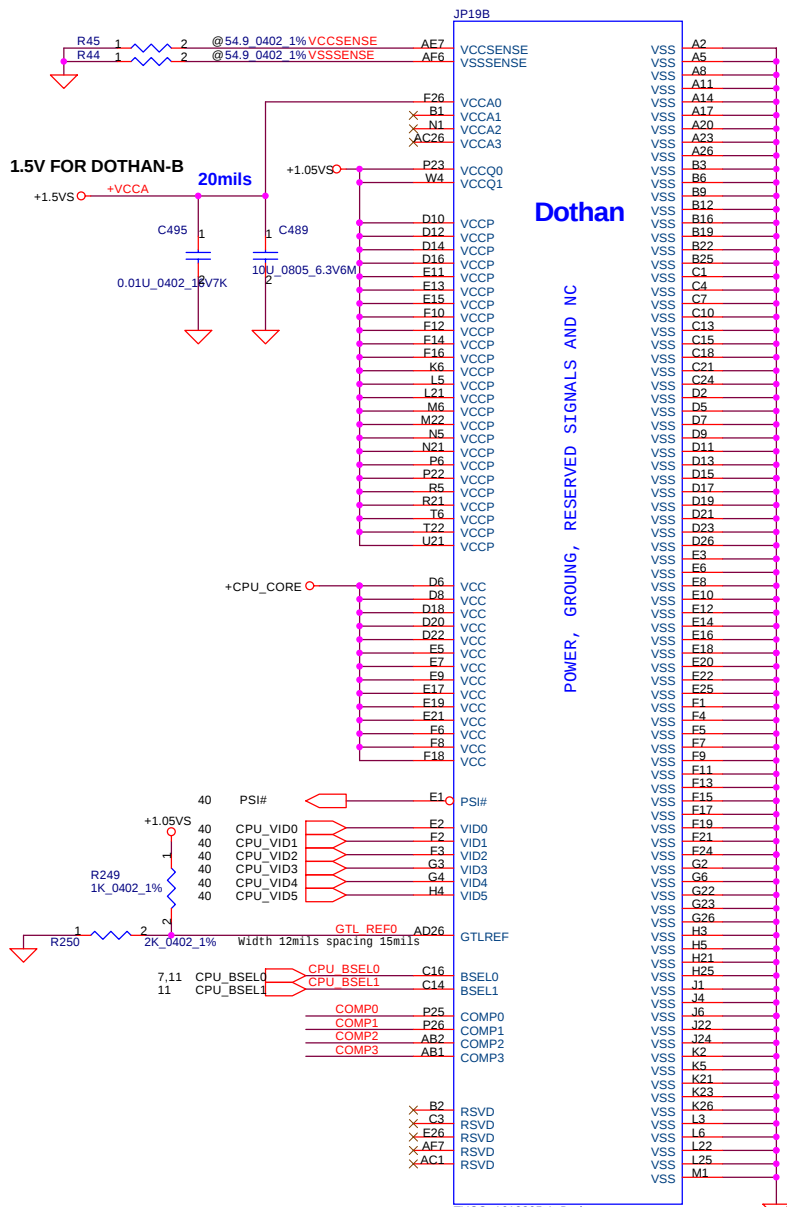
Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1, 0.2
1	0.3
2	1.0
3	
4	
5	
6	
7	

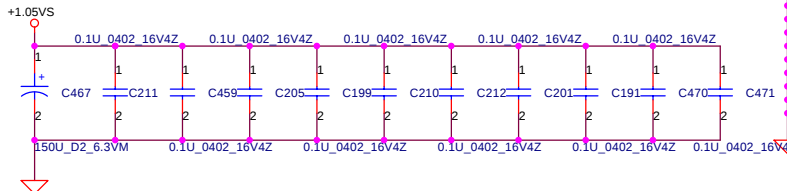
SKU ID	SKU Status
0	
1	
2	
3	
4	
5	1 Buttons
6	
7	7 Buttons

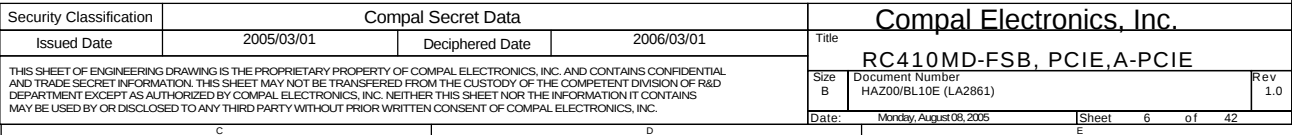
	HDD Password
0	NO
1	Yes

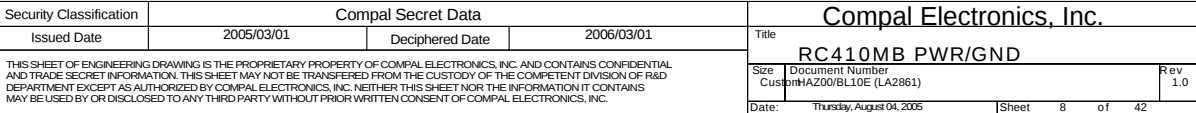
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				Date:	Thursday, August 04, 2005
				Sheet	3 of 42
				Rev	1.0

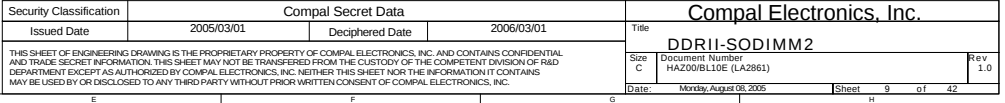


Vcc-core Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	4X330uF	7m ohm/2	3.5nH/2
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35



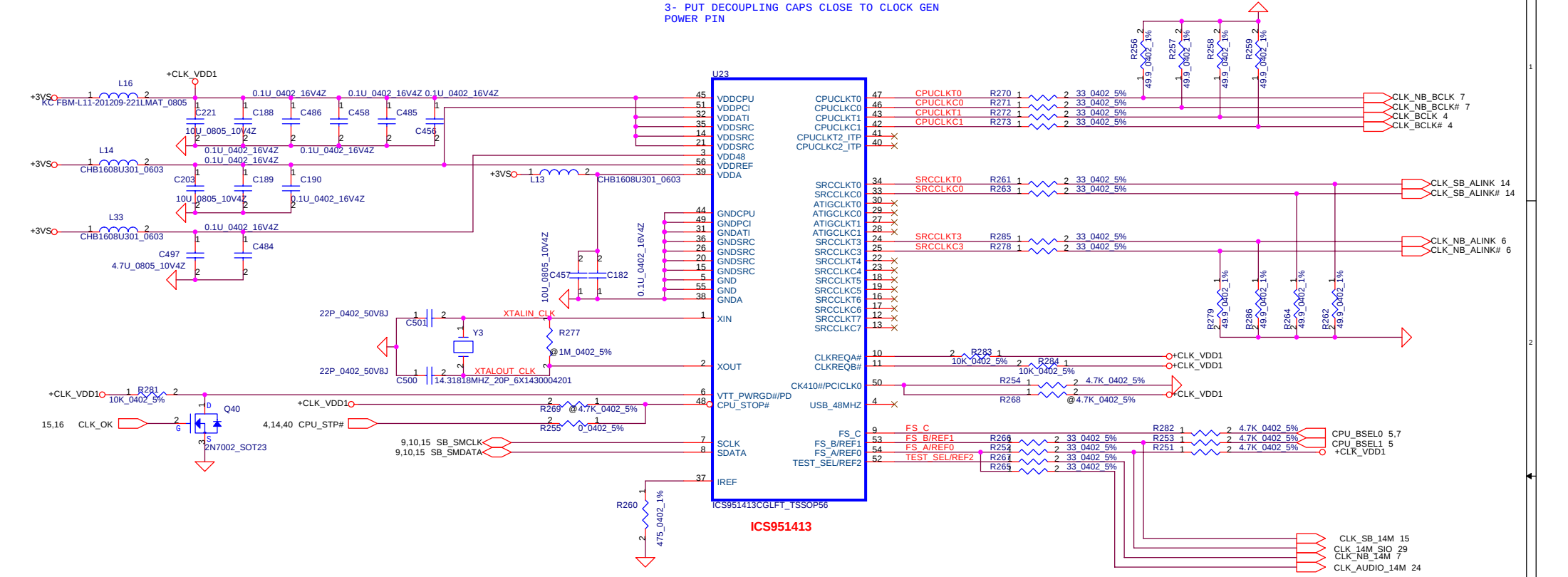






Clock Generator

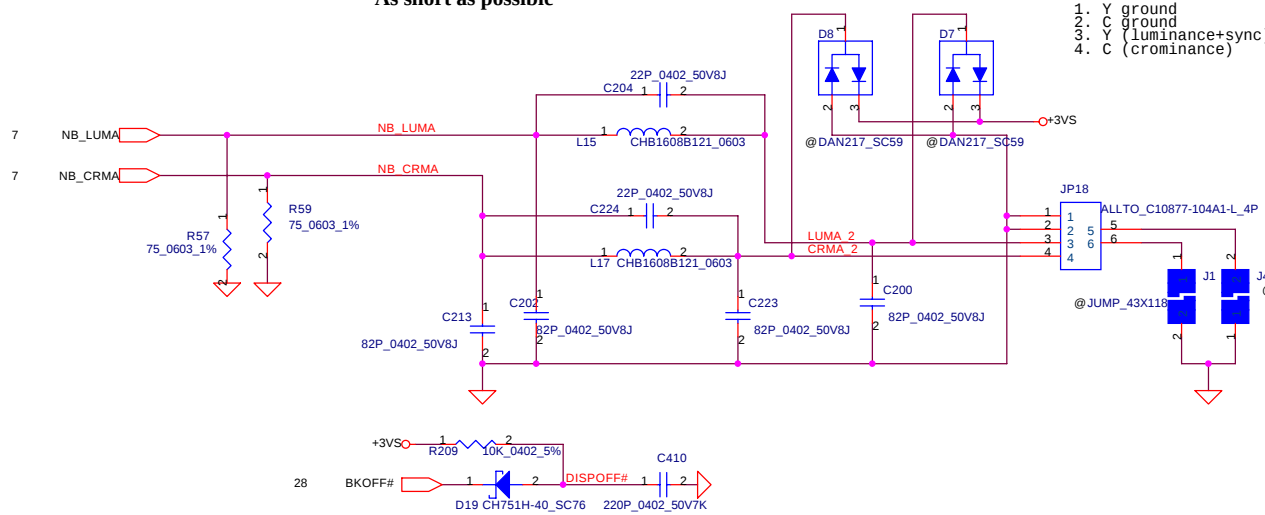
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLOCK GEN AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBCLK/#, ITPCLK/# AND SCR/# ,AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



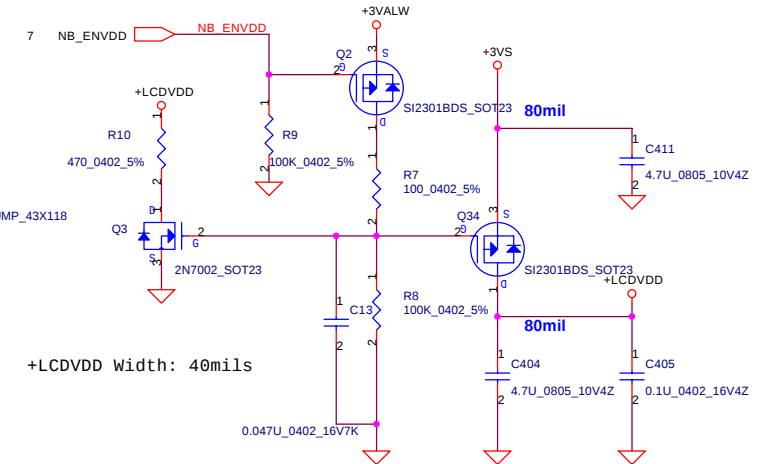
FS_C	FS_B	FS_A	CPU	SRC	PCI	REF	USB
1	0	1	100.00	100.00	33.33	14.318	48.000
0	0	1	133.33	100.00	33.33	14.318	48.000
1	1	1	---	---	---	---	---

TV-OUT CONNECTOR

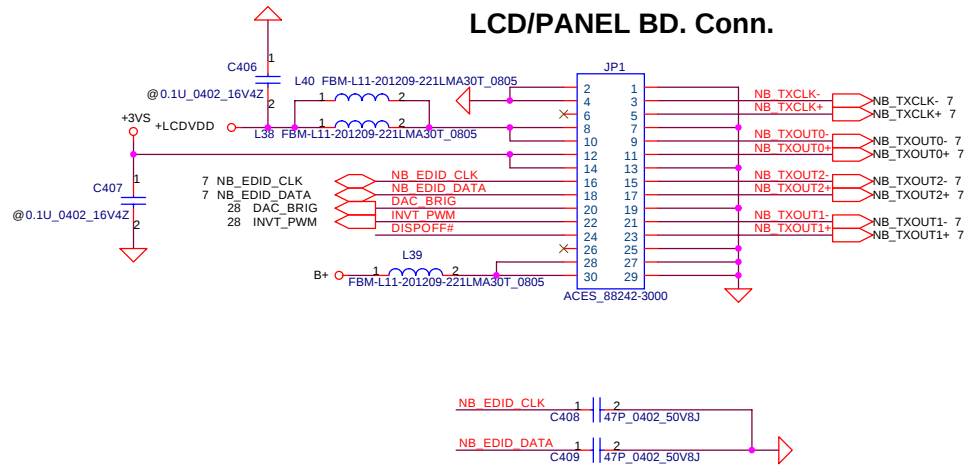
Reduce LUMA_1 and CRMA_1 length
As short as possible



PANEL +LCDVDD CTRL CKT

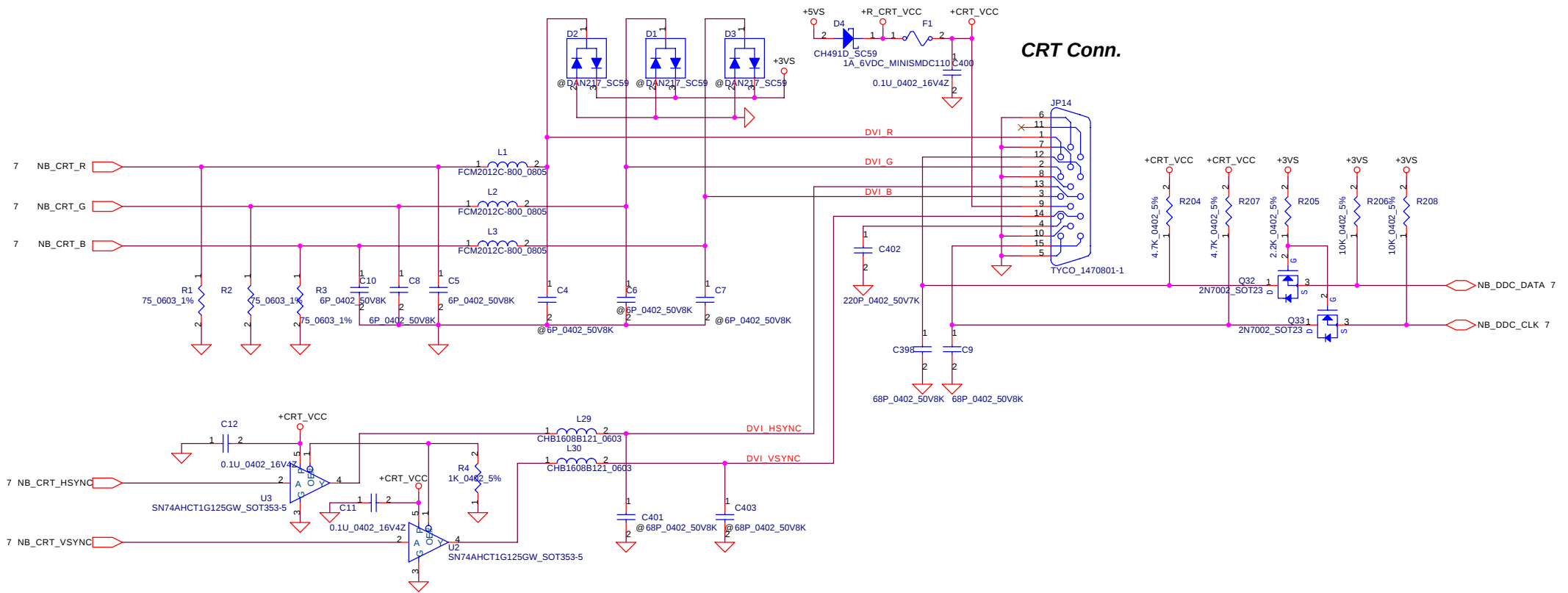


LCD/PANEL BD. Conn.

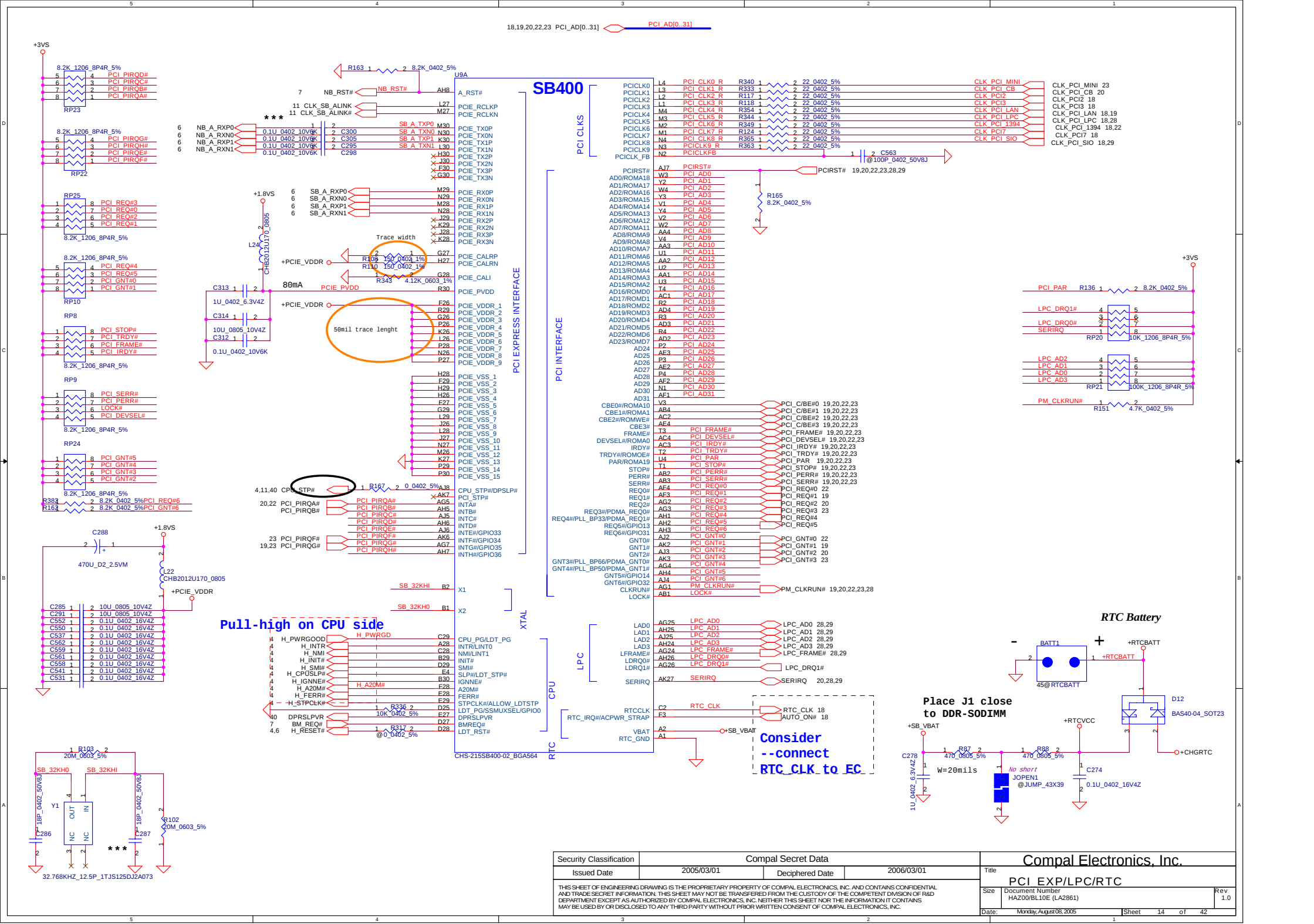


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				Date: Monday, August 08, 2005	Sheet 12 of 42
				Rev 1.0	

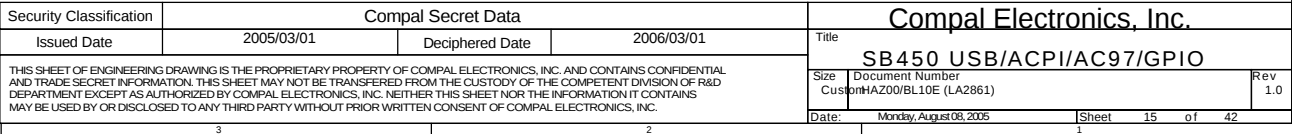
CRT CONNECTOR

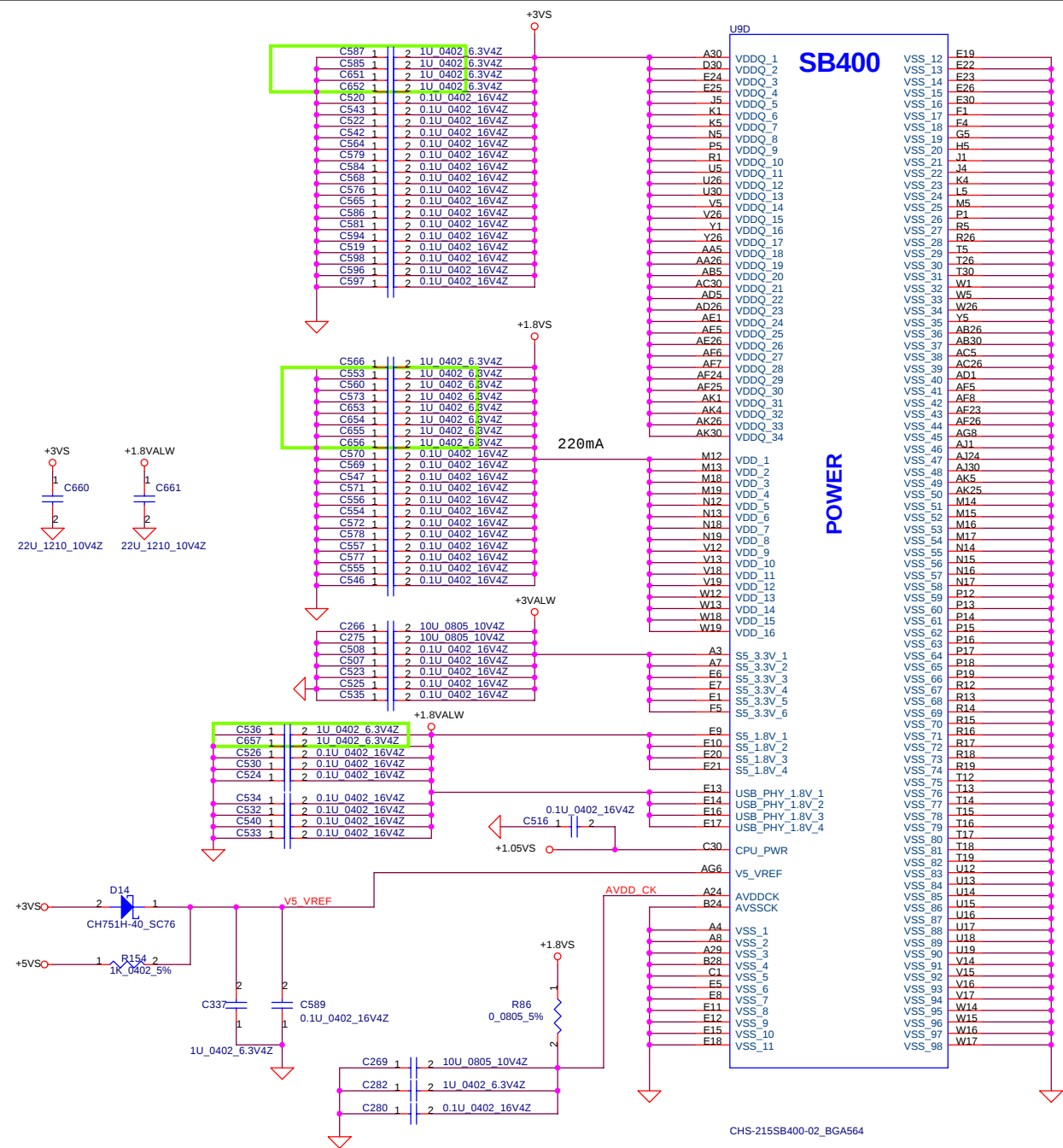


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Size B	Document Number HAZ00/BL10E (LA2861)			Rev	1.0
Date:	Thursday, August 04, 2005			Sheet	13 of 42



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Issued Date	2005/03/01	Deciphered Date	2006/03/01	Title	PCI EXP/LPC/RTC	
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					HAZ00/BL10E (LA2861)	1.0
				Date:	Monday, August 08, 2005	Sheet 14 of 42





CHS-215SB400-02_BGA564

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Size	Document Number			Rev	
B	HAZ00/BL10E (LA2861)			1.0	
Date:	Thursday, August 04, 2005	Sheet	17 of 42		

REQUIRED STRAPS

14 AUTO_ON#
15,24,32 AC_SDOUT
14 RTC_CLK
15 SPDIF_OUT
14 CLK_PCI3
14,19 CLK_PCI_LAN
14,28 CLK_PCI_LPC
14,22 CLK_PCI_1394
14 CLK_PCI7
14,29 CLK_PCI_SIO



	AUTO_ON#	AC97_SDOUT	RTC_CLK	SPDIF_OUT	CLK_PCI3	CLK_PCI_LAN	CLK_PCI_LPC	PCI_CLK6	PCI_CLK7	PCI_CLK8	CLK_PCI_MINI2
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	PU for 48Mhz XTAL mode DEFAULT	USB PHY PWRDOWN DISABLE	Internal PLL	PCIE CM_SET low DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = LPC ROM I		Clock input buffer DEFAULT
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	48M OSC mode DEFAULT	USB PHY PWRDOWN ENABLE DEFAULT	External Clock DEFAULT	PCIE CM_SET HIGH	CPU I/F = P4 DEFAULT	L,H = LPC ROM II L,L = FWH ROM		Crytsal Pad

Selects type of 48MHz clock pad

Pop R634 when debug .

DEBUG STRAPS

16,26 IDE_PDDACK#
14,19,20,22,23 PCI_AD31
14,19,20,22,23 PCI_AD30
14,19,20,22,23 PCI_AD29
14,19,20,22,23 PCI_AD28
14,19,20,22,23 PCI_AD27
14,19,20,22,23 PCI_AD26
14,19,20,22,23 PCI_AD25
14,19,20,22,23 PCI_AD24
14,19,20,22,23 PCI_AD23

	IDE_PDDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

14,18,20,22,23 PCI_AD[0..31]

PCI AD0	104	AD0
PCI AD1	103	AD1
PCI AD2	102	AD2
PCI AD3	98	AD3
PCI AD4	97	AD4
PCI AD5	96	AD5
PCI AD6	95	AD6
PCI AD7	93	AD7
PCI AD8	90	AD8
PCI AD9	89	AD9
PCI AD10	87	AD10
PCI AD11	86	AD11
PCI AD12	85	AD12
PCI AD13	83	AD13
PCI AD14	82	AD14
PCI AD15	79	AD15
PCI AD16	59	AD16
PCI AD17	58	AD17
PCI AD18	57	AD18
PCI AD19	55	AD19
PCI AD20	53	AD20
PCI AD21	50	AD21
PCI AD22	49	AD22
PCI AD23	47	AD23
PCI AD24	43	AD24
PCI AD25	42	AD25
PCI AD26	40	AD26
PCI AD27	39	AD27
PCI AD28	37	AD28
PCI AD29	36	AD29
PCI AD30	34	AD30
PCI AD31	33	AD31

14,20,22,23 PCI_C/BE#0	PCI_C/BE#0	92
14,20,22,23 PCI_C/BE#1	PCI_C/BE#1	77
14,20,22,23 PCI_C/BE#2	PCI_C/BE#2	60
14,20,22,23 PCI_C/BE#3	PCI_C/BE#3	44

PCI_AD22

14,20,22,23 PCI_PAR	76	PAR
14,20,22,23 PCI_FRAME#	61	FRAME#
14,20,22,23 PCI_IRDY#	63	IRDY#
14,20,22,23 PCI_TRDY#	67	TRDY#
14,20,22,23 PCI_DEVSEL#	68	DEVSEL#
14,20,22,23 PCI_STOP#	69	STOP#

14,20,22,23 PCI_PERR#	70	PERR#
14,20,22,23 PCI_SERR#	75	SERR#

14 PCI_REQ#1	30	REQ#
14 PCI_GNT#1	29	GNT#

14,23 PCI_PIRQG#	25	INTA#
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22,23,28 LAN_PME#	31	PME#
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14,20,22,23,28,29 PCIRST#	27	RST#
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14,18 CLK_PCI_LAN	28	CLK
14,20,22,23,28 PM_CLKRUN#	65	CLKRUN#

4	GND/VSS	128
17	GND/VSS	128
21	GND/VSSPST	38
38	GND/VSSPST	51
51	GND/VSSPST	66
66	GND/VSSPST	81
81	GND/VSSPST	91
91	GND/VSSPST	101
101	GND/VSSPST	119
119	GND/VSSPST	128
35	GND	100
52	GND	100
80	GND	100
100	GND	100

3	AVDD33/AVDDL	7
7	AVDD33/AVDDL	20
20	AVDD33/AVDDL	16
16	AVDD33/AVDDL	20
32	VDD25/VDD18	54
54	VDD25/VDD18	78
78	VDD25/VDD18	99
99	VDD25/VDD18	116
24	NC/VDD18	64
45	NC/VDD18	110
64	NC/VDD18	116
110	NC/VDD18	116

12	AVDD25/HSDAC	12
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1	AVDD25/HSDAC	12
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1	AVDD25/HSDAC	12
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1	AVDD25/HSDAC	12
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1	AVDD25/HSDAC	12
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1	AVDD25/HSDAC	12
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EEDO	108	EEDO
AUX/EEDI	109	EEDI
EESK	111	EESK
EECS	106	EECS
117	ACTIVITY#	
115	LINK 10 100#	
114		
113		
1	LAN TD+	
2	LAN TD-	
5	LAN RD+	
6	LAN RD-	

14	LAN X1	
122	LAN X2	

105		
23		
127		
72		
74		

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8	CTRL25	
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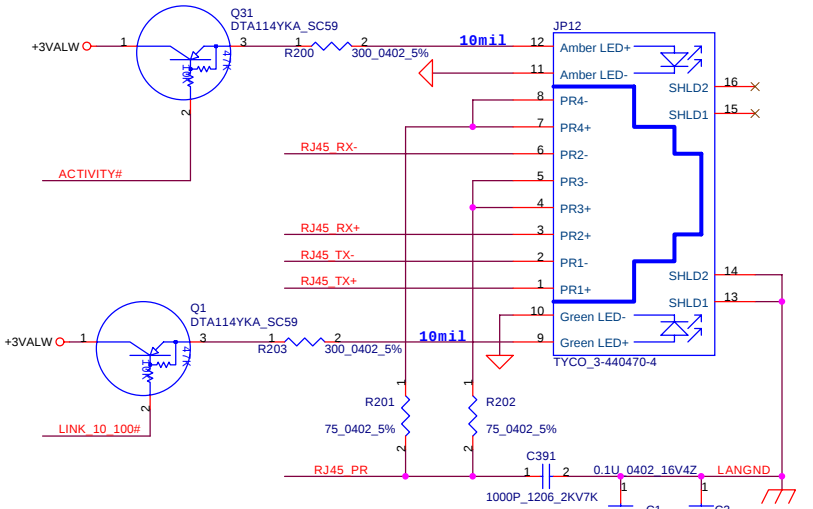
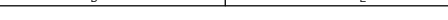
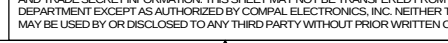
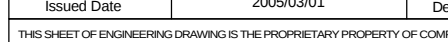
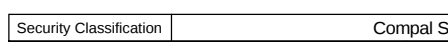
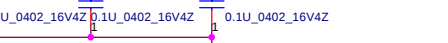
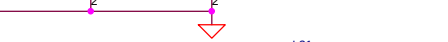
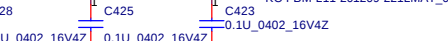
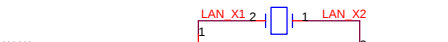
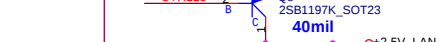
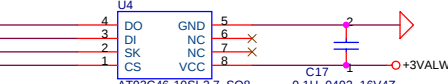
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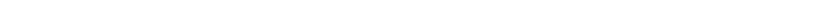
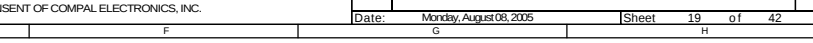
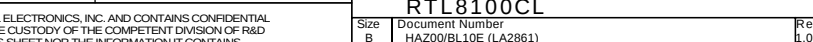
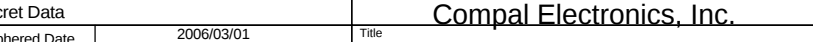
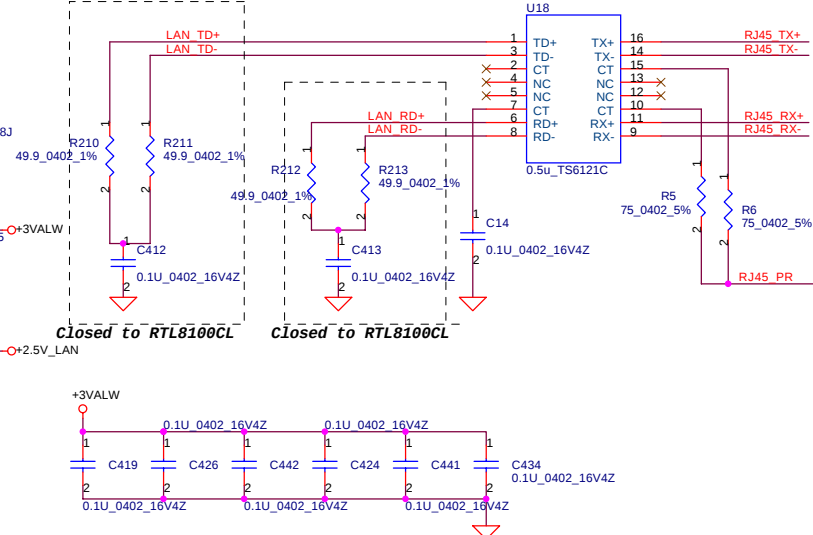
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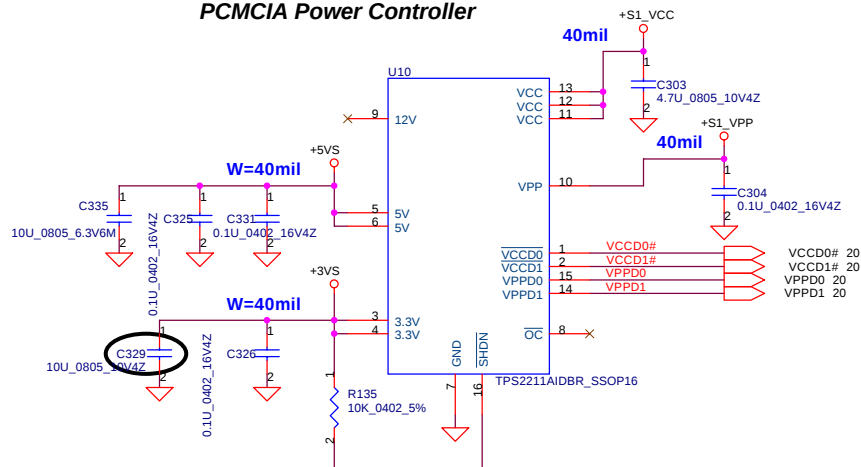
Termination plane should be coupled to chassis ground

Layout Note
TS6121 pls close to conn.

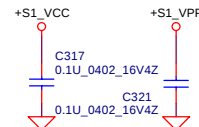
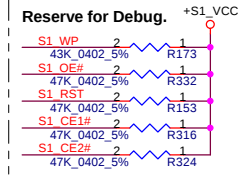
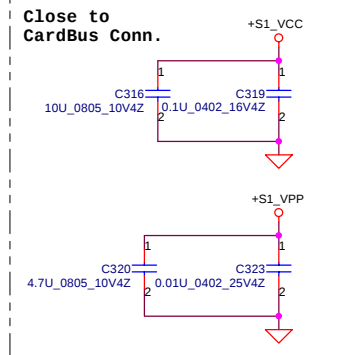
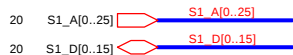


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				B	HA200/BL10E (LA2861)	1.0
				Date:	Monday, August 08, 2005	Sheet 19 of 42

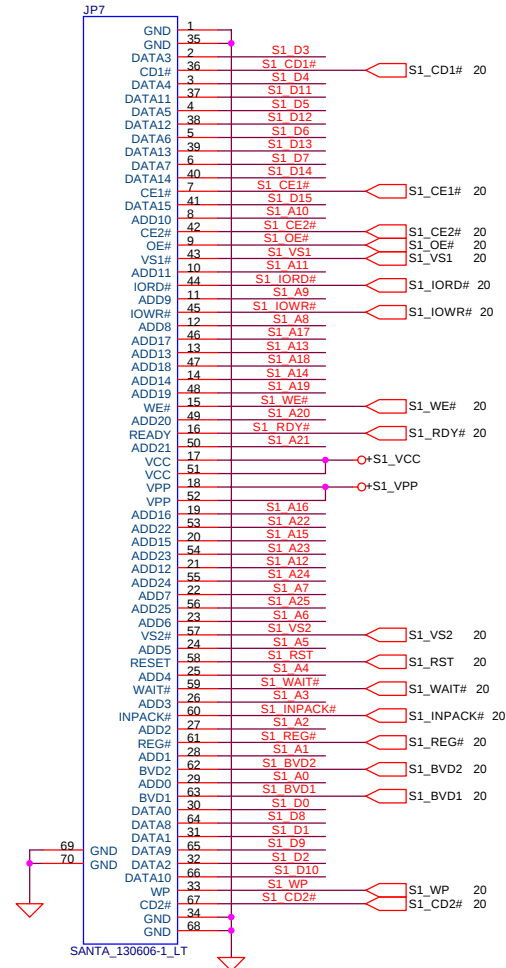
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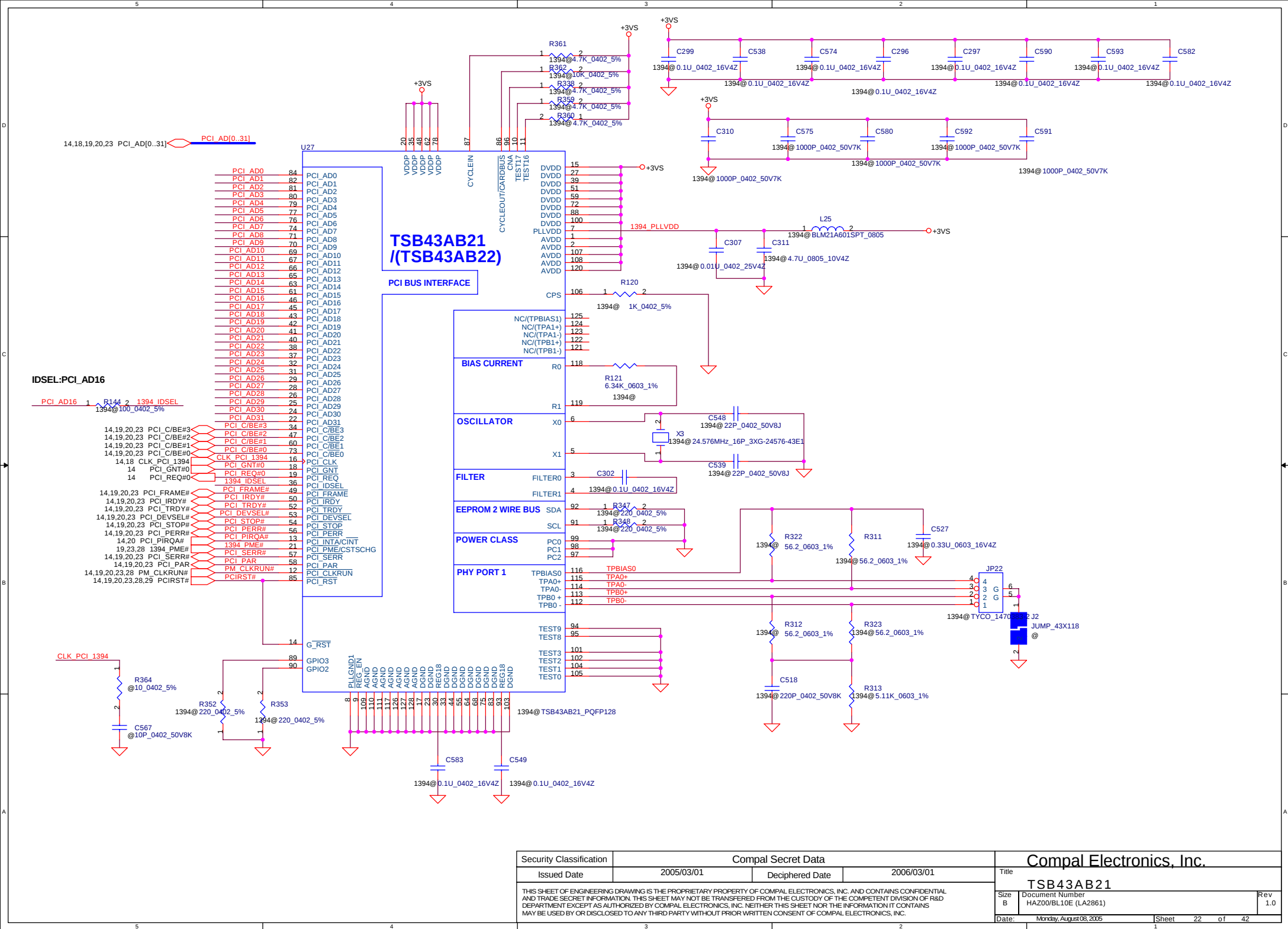
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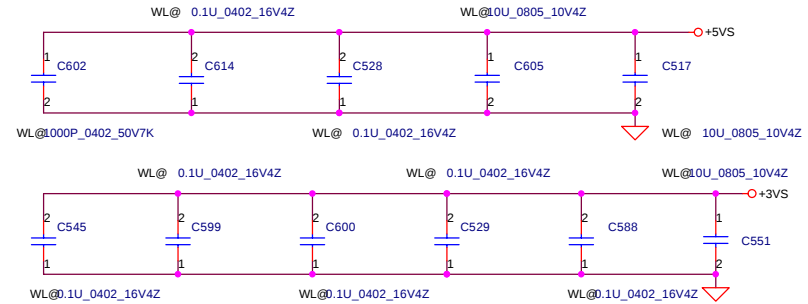
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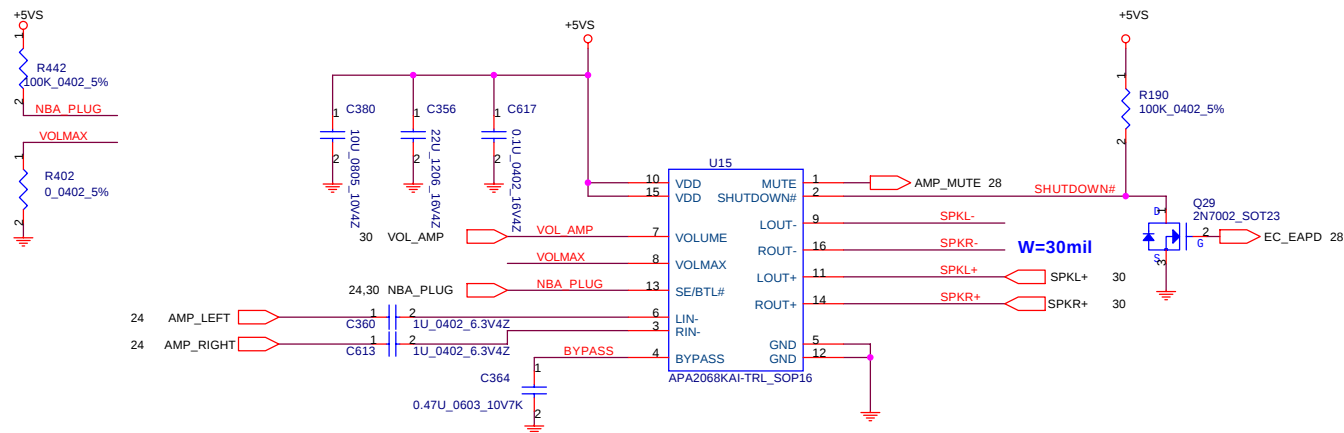
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Size	B	Document Number	HAZ00/BL10E (LA2861)	Rev	1.0
Date:	Thursday, August 04, 2005			Sheet	21 of 42



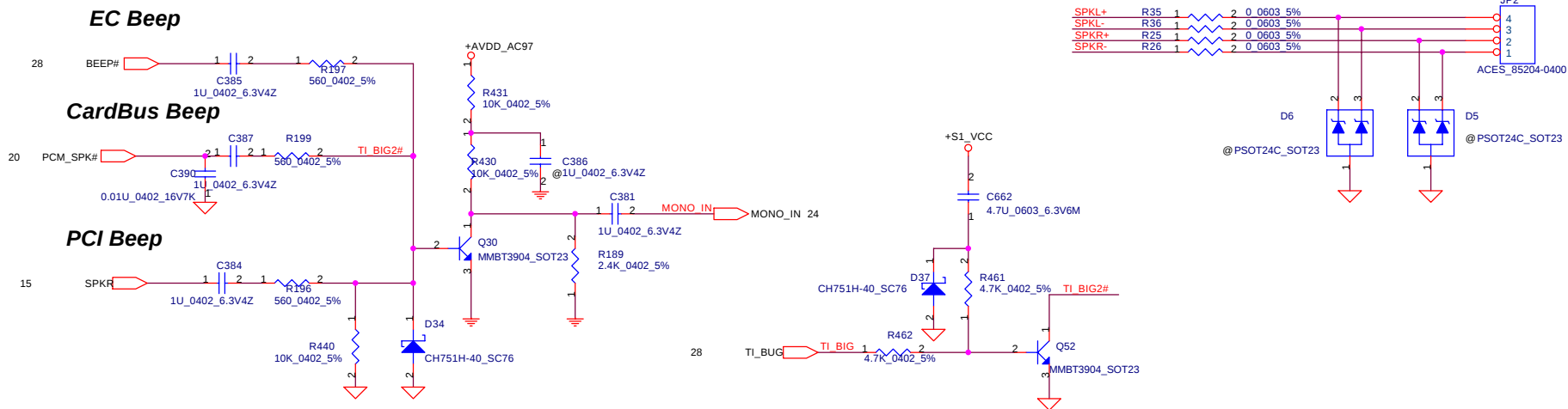
PCI_AD[0..31] PCI_AD[0..31] 14,18,19,20,22



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				Size B	Document Number HA200/BL10E (LA2861)	Rev 1.0
Date: Monday, August 08, 2005				Sheet 23 of 42		

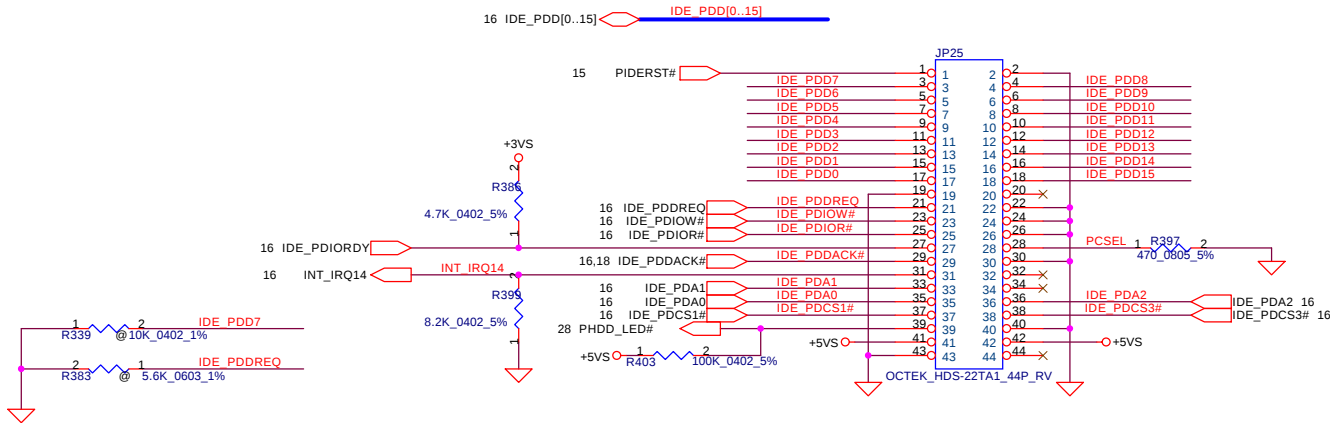


Speaker Conn.

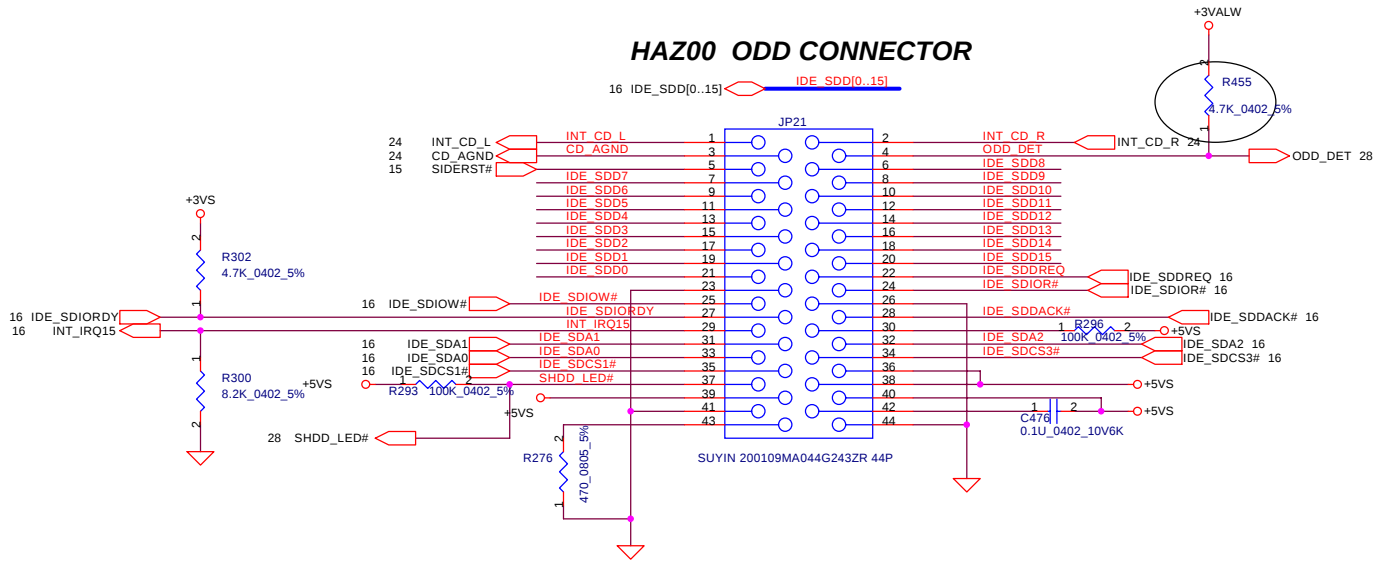


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Size	B	Document Number	HA200/BL10E (LA2861)	Rev	1.0
Date:	Monday, August 08, 2005			Sheet	25 of 42

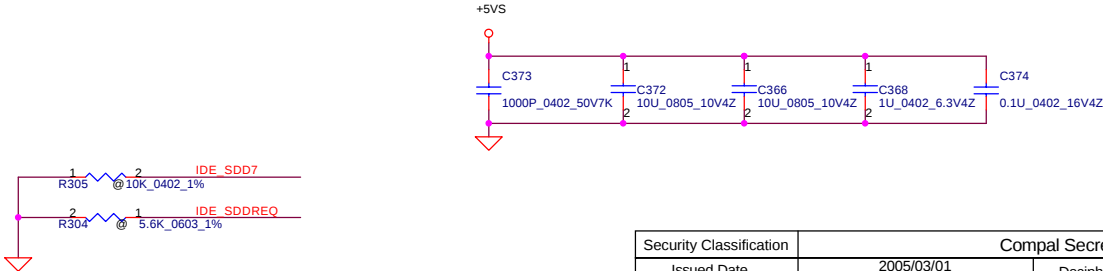
HDD CONNECTOR



HAZ00 ODD CONNECTOR

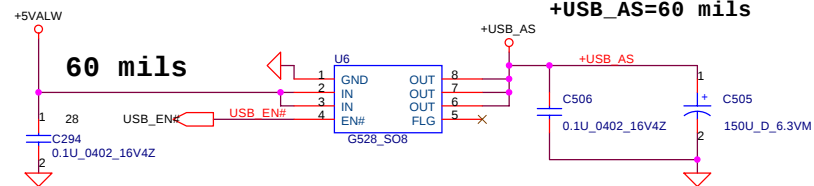


Place caps. near HDD
CONN.

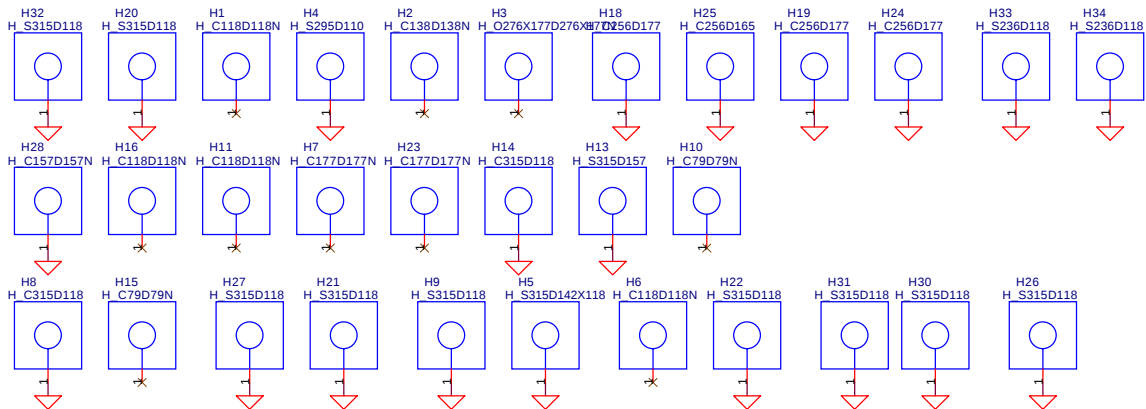
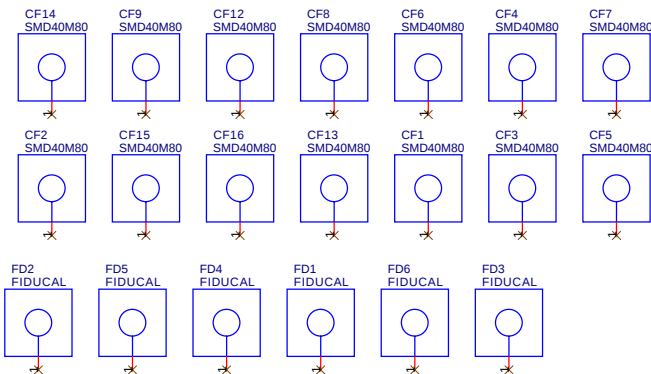
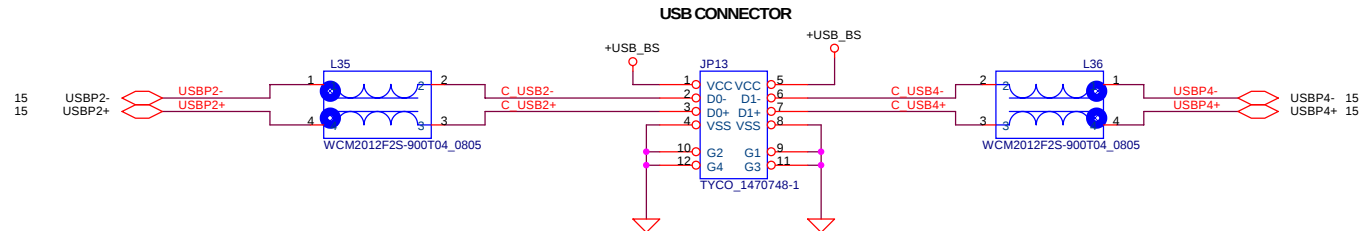
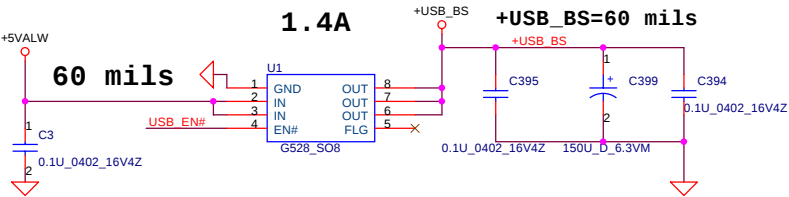
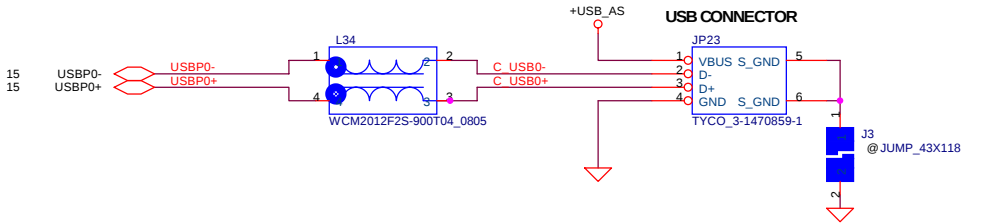


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Size B	Document Number HAZ00/BL10E (LA2861)	Rev 1.0	Date: Thursday, August 04, 2005	Sheet 26 of 42

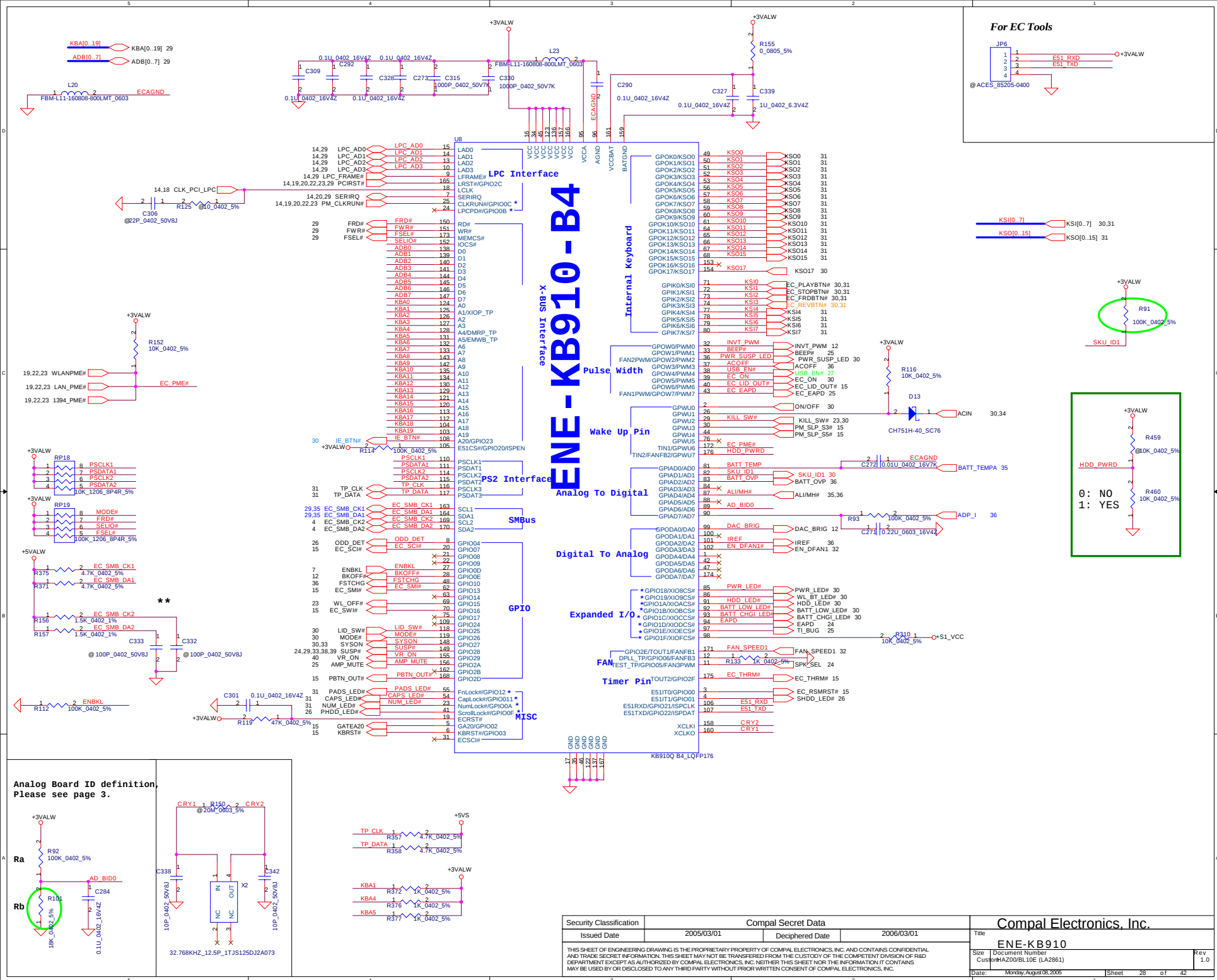
1.4A



Keep 20 mils minimum spacing between USB signals and others signals

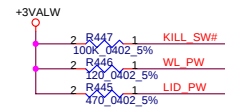
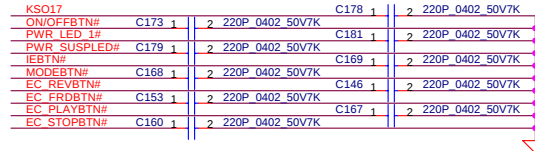
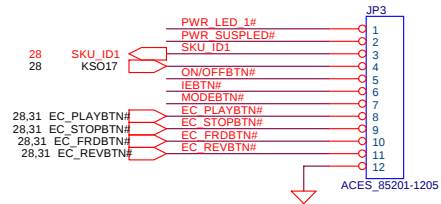


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Size	B	Document Number	HAZ00/BL10E (LA2861)	Rev 1.0
Date:	Thursday, August 04, 2005	Sheet	27 of 42	

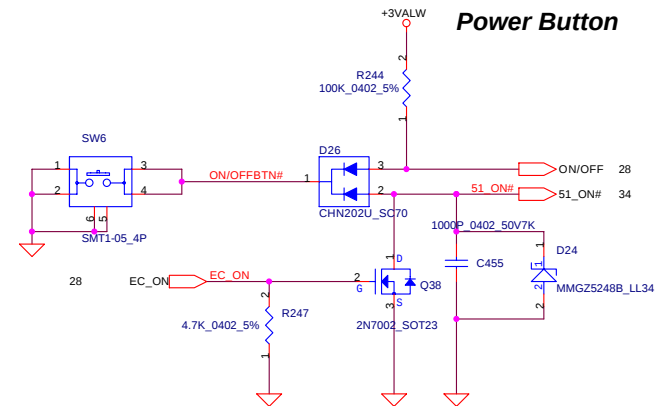
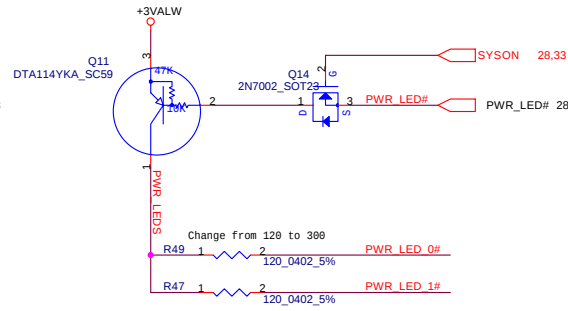
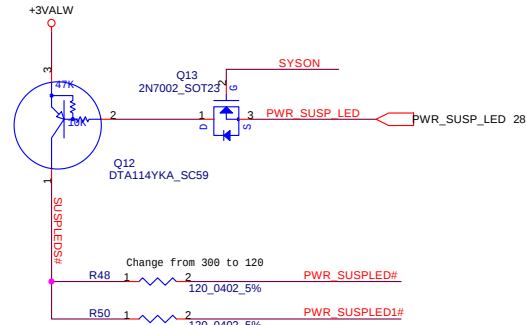
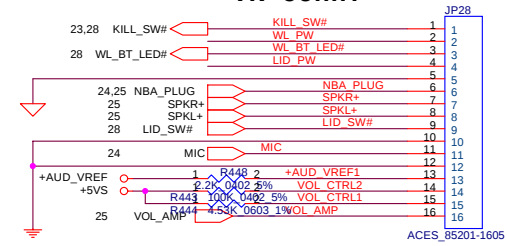


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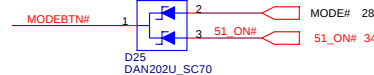
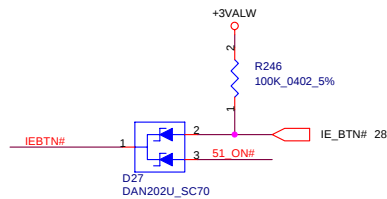
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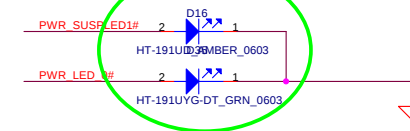
VR Conn.



Power Button



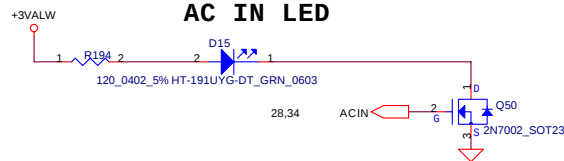
POWER/ON LED



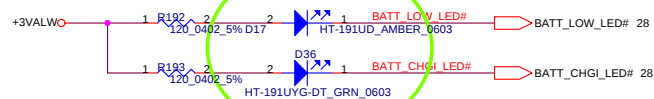
HDD LED



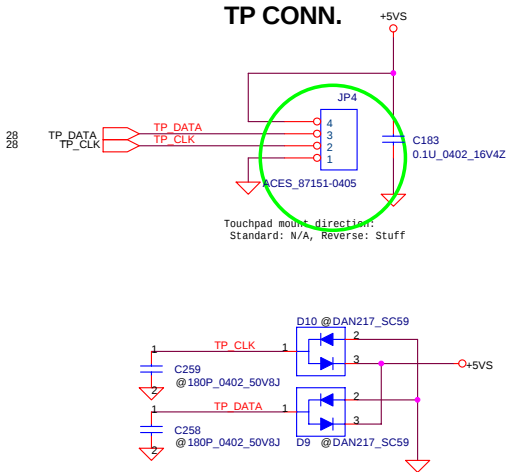
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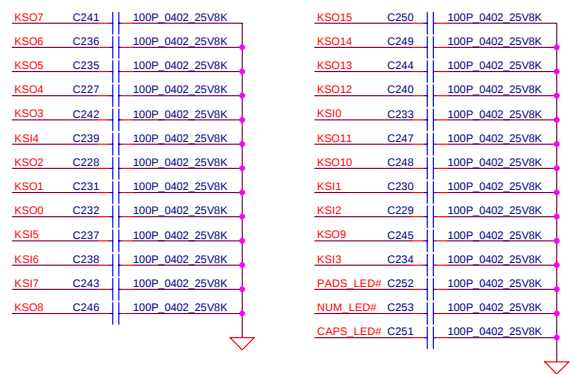
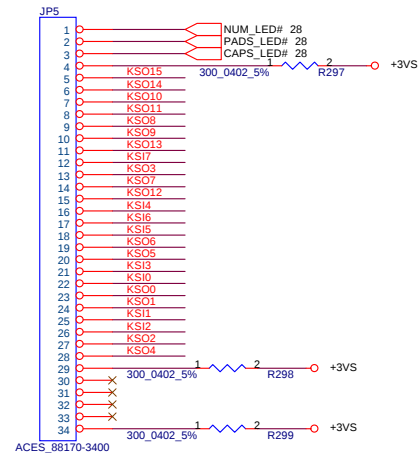
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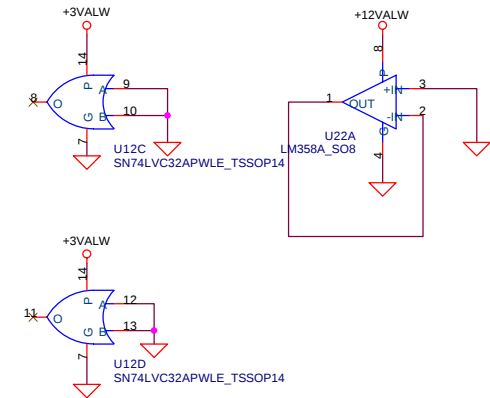
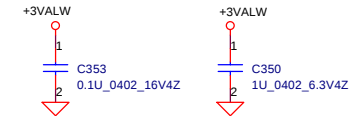


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				Customer	HA200/BL10E (LA2861)
				Rev	1.0
Date: Thursday, August 04, 2005				Sheet	30 of 42



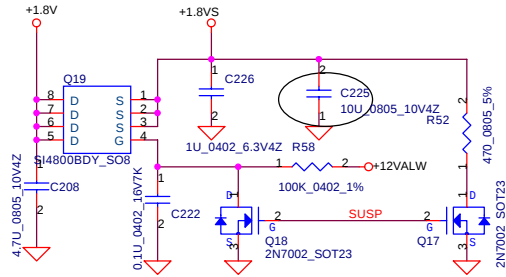
INT_KBD CONN.



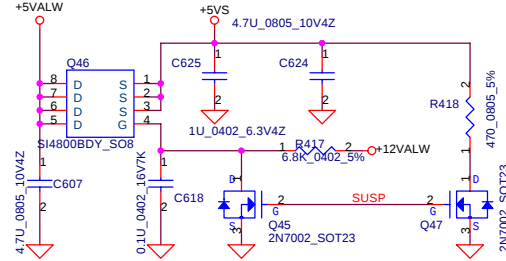
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				Date:	Thursday, August 04, 2005	Sheet 32 of 42

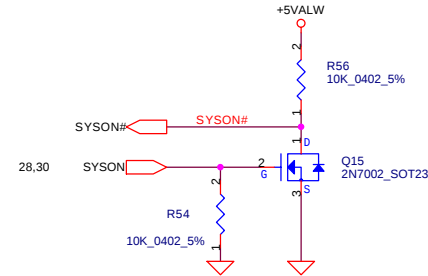
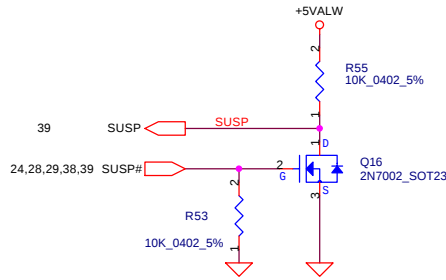
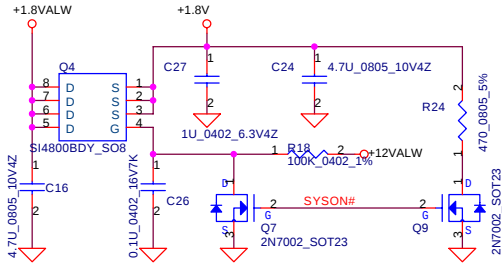
+1.8VALW TO +1.8VS



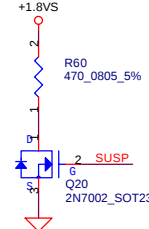
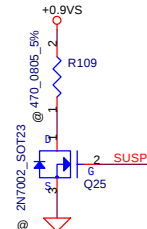
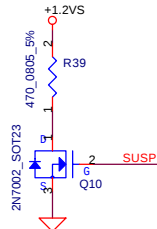
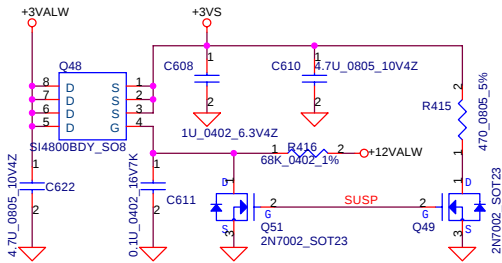
+5VALW TO +5VS



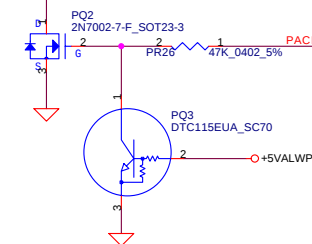
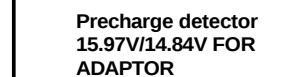
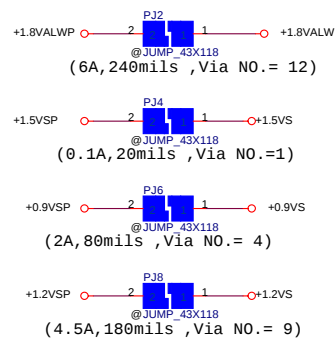
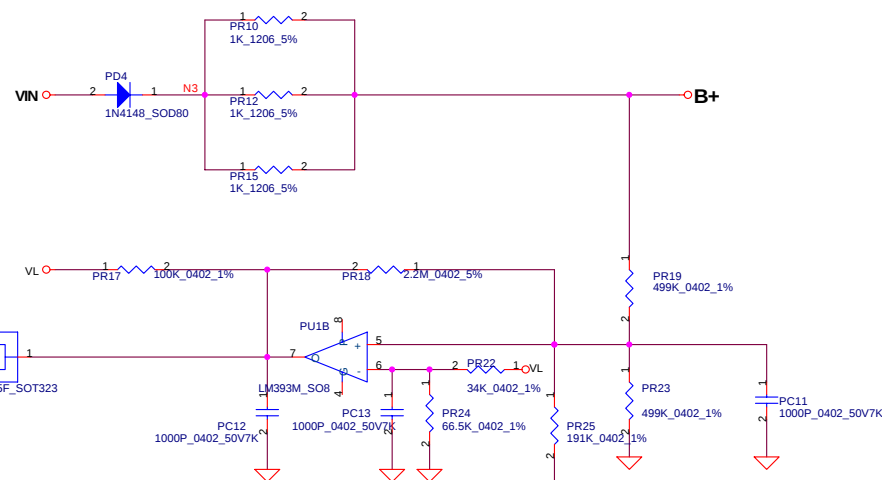
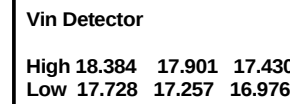
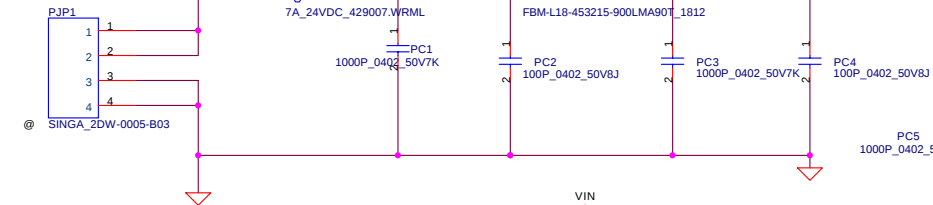
+1.8VALW TO +1.8V



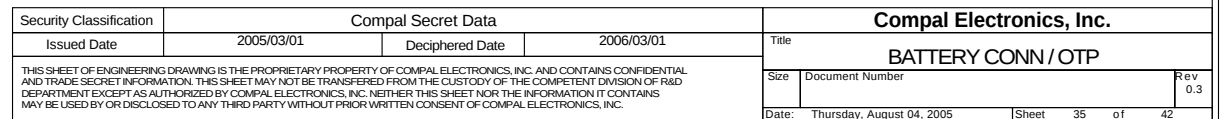
+3VALW TO +3VS

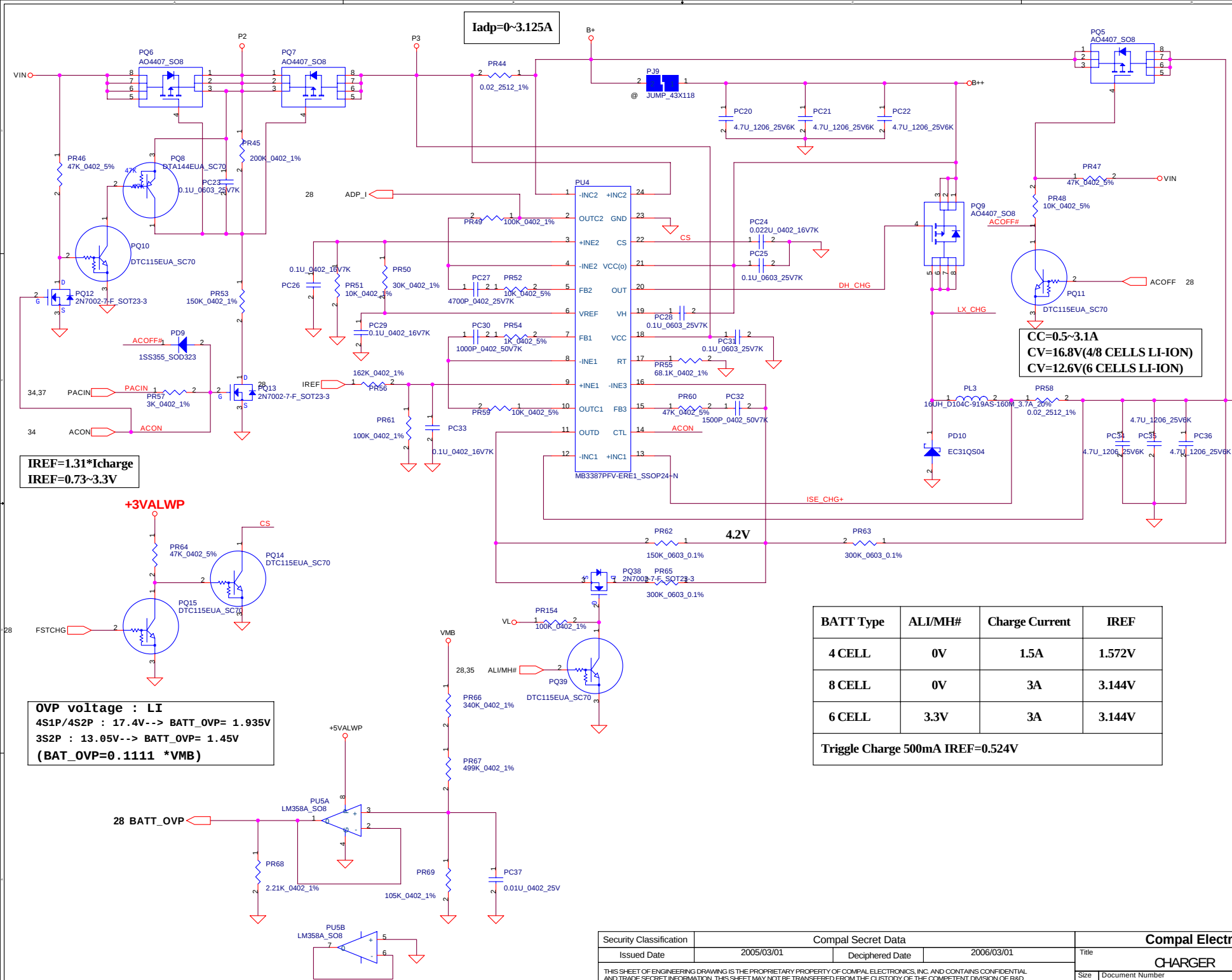


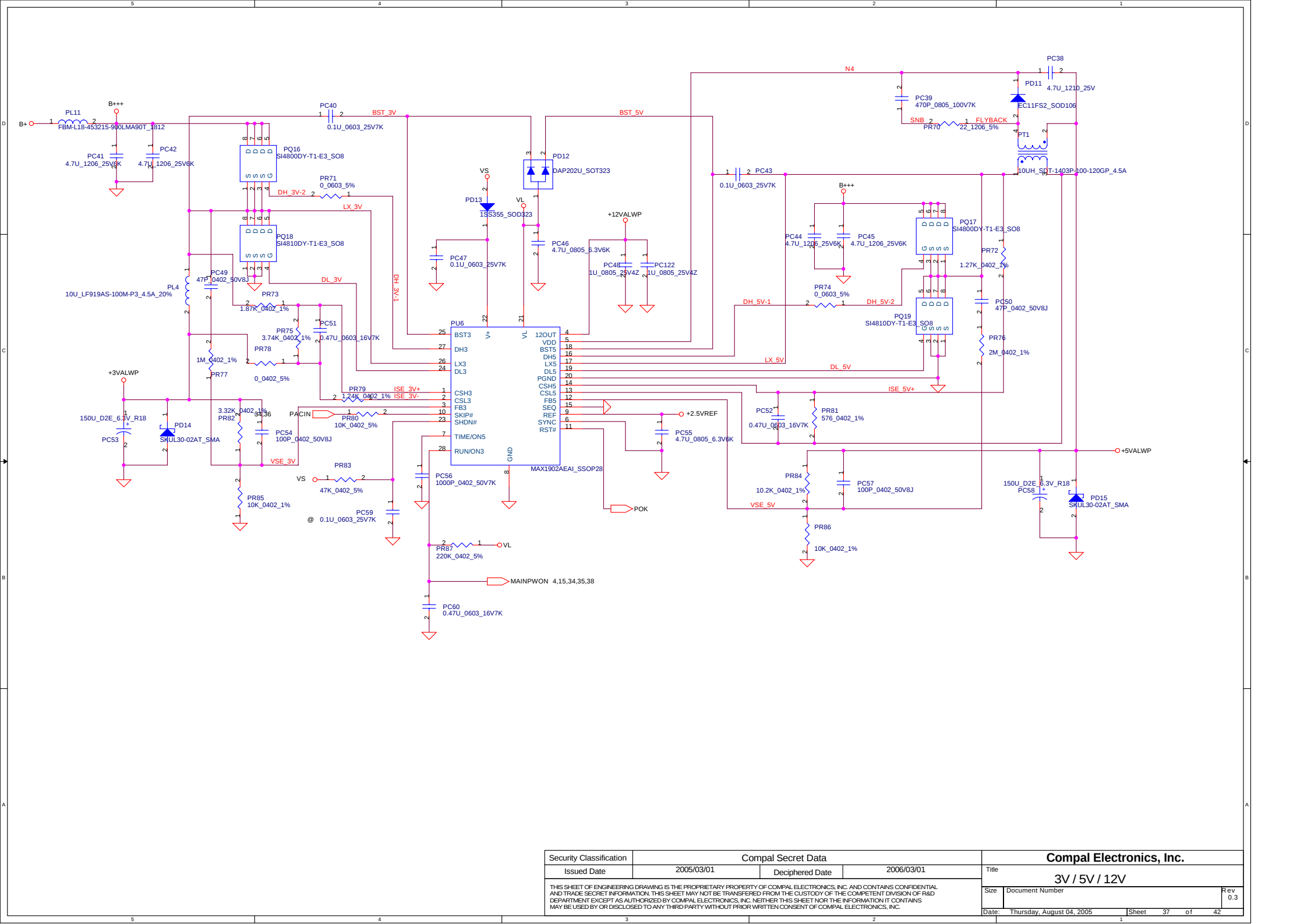
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Size	B	Document Number	HA200/BL10E (LA2861)	Rev	1.0
Date:	Monday, August 08, 2005			Sheet	33 of 42



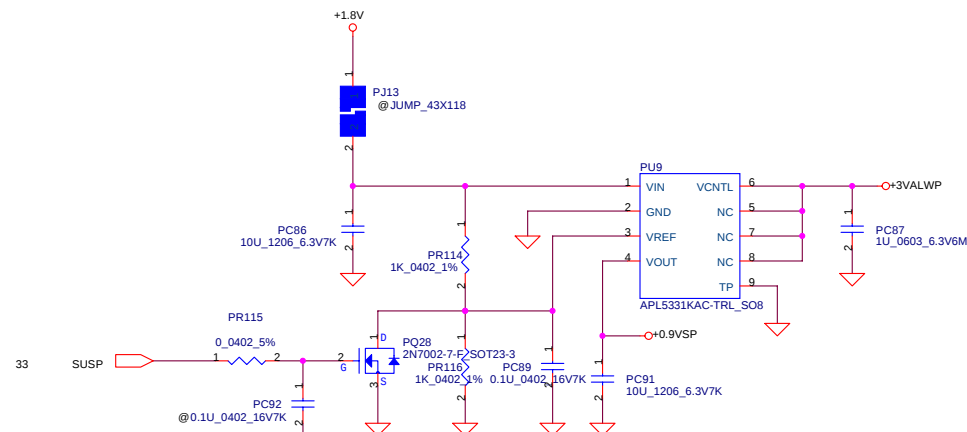
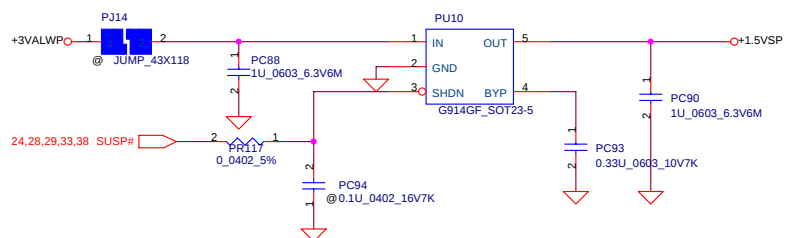
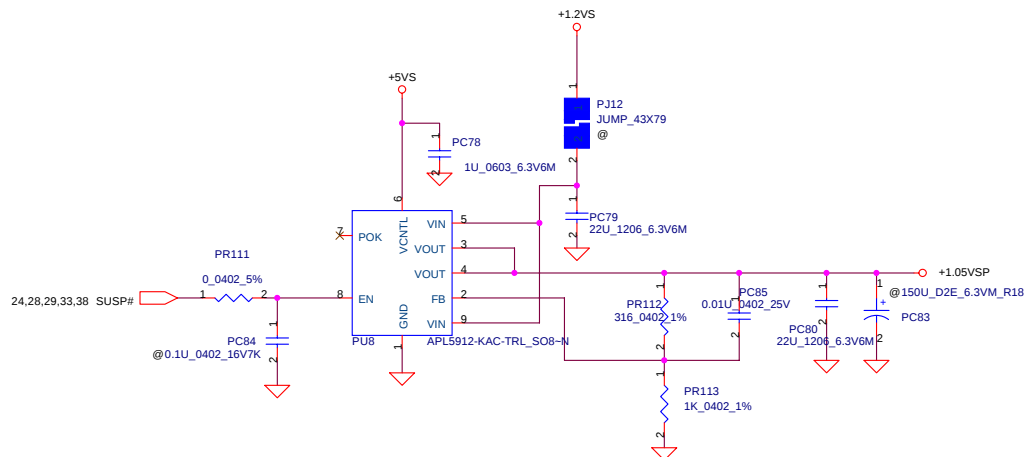
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				Date:	Thursday, August 04, 2005	Sheet 34 of 42

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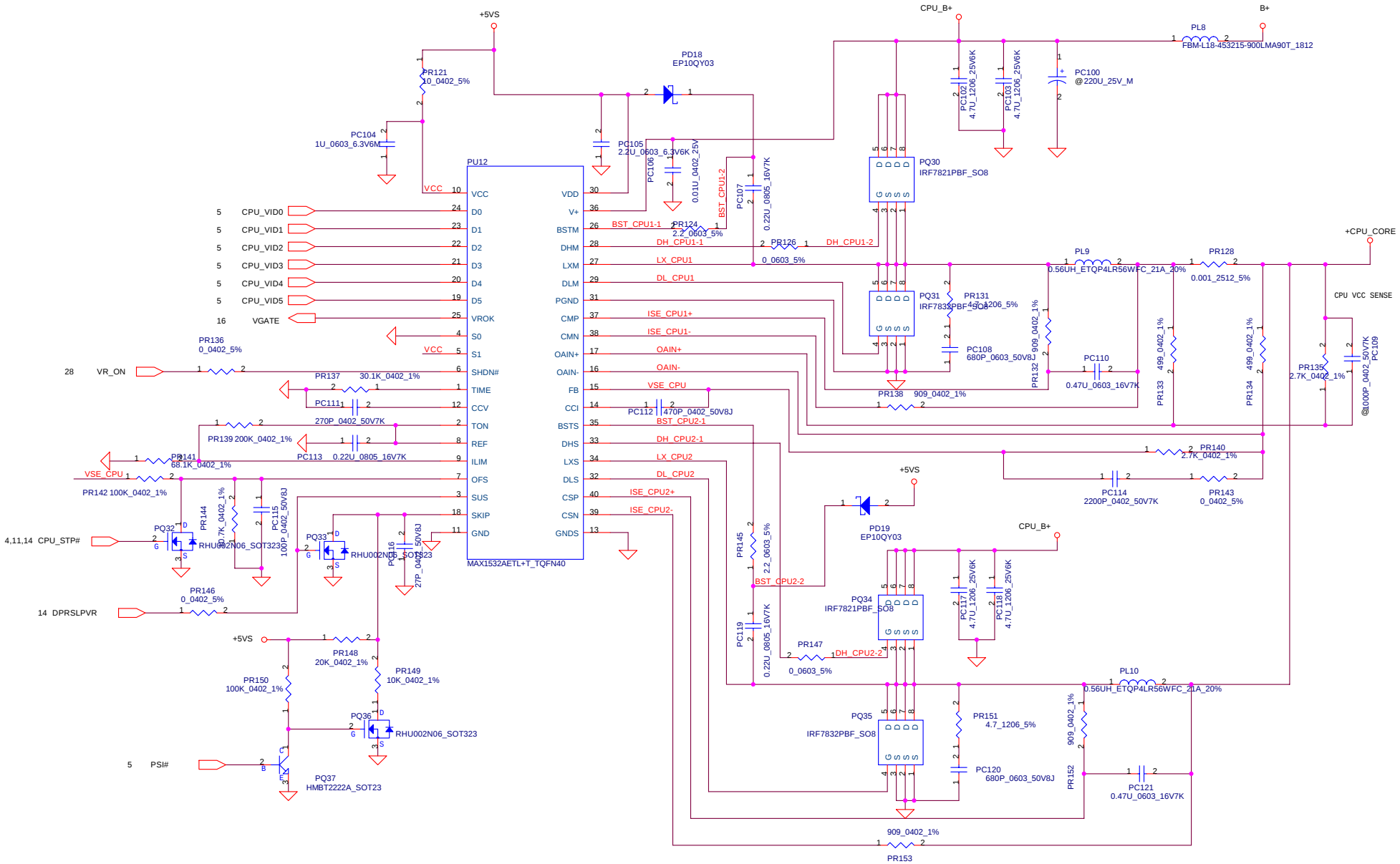




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						0.3
				Date:	Thursday, August 04, 2005	Sheet 39 of 42



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Size		Document Number		Rev	
Date:		Monday, August 08, 2005		Sheet 40 of 42	
				0.3	

0.1==>0.2		Written by Timo	
Date	Page	Action	Purpose
6/12	9	Add C642, C643 and C644	For Increase the DDR bypass capaciotrs
6/12	10	Add C645, C646 and C647	For Increase the DDR bypass capaciotrs
	12	Modify JP18 circuit	Making TV out function become correct
	15	Add @ on R317	Metting ATI reference circuit
	24	Del @ on R436	Solving MDC issue and sound slow issue
	26	Del R306 (move to sub board)	To differentiate between HAZ00 and HTW01 BIOS
	28	Add @ on Super I/O circuit	For DVT build
	29	Modify pin74 net-name of KB910	Solving reserve button no function
	31	Modify D16, D17	
		Add D35, D36	Change from double colors to signal color LED
6/22	27	Add H34, H33	For Me update new drawing

0.2==>0.3		Written by Timo	
7/8	8	Add C648, C649 and C650	Seperate the AVDD and DVDD for TVout and CRT
	17	Add C651~C657	
		Change C585, C587, C566, C533, C560, C573, C536 from 10 to 4.7U	For height limited of SB
	34	Change C225 from 4.7 to 10U	For height limited of SB
7/11	25	Del R456	
		Add Q52	For insert card bus device beep sound issue.
	27	Del R449~R454	For EMI request
7/13		Del Super I/O circuit	
	29	Add JP30, R457, C658	For LPC debug port
	23	ADD JP29, R456	For Port80 Debug card connector
	28	ADD R459, R460	For HDD password detect pin
	12	ADD J1, J4	
	22	ADD J2	
	27	ADD J3	For EMI request

0.3==>1.0		Written by Timo	
7/28	25	Add C662, R461, D37, R462, Q52	For Insert card bus device PoPo noise sound
	29	Change R101 from 8.2k to 18kohm	For Board ID change
	14	Change C587, C585, C651, C652, C566, C553, C560, C573, C653, C654, C655, C656, C536, C657	
	17	from 4.7U to 1U	For avoide the interfere area of HDD
		Change C288 from 150U fo 470UF	Making the capacitors of 1.8VS source blance of SB
		Add C660, C661	Making the capacitors of 1.8VALW and 3VS sources blance of SB
7/30	4	Add @ in C261	For throttle issue
	5	Add @ in C180	For cost down
	12	Add L38, L39, L40	For EMI issue

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				Date:	Monday, August 08, 2005
				Sheet	41 of 42
				Rev	1.0

EVT

page	Reason for change	Modify list
37	12V noise	Change PC38 from 4.7u_1206_25V to 4.7u_1210_25V
37	Lead free parts	Change PC53,PC58 to NEC lead free parts.
38	Modify 1.8V power sequence for HW requirement	Change PR100 from 0_0402_5% to 47K_0402_1% Add 0.1u_0402_16V at PC76
39	Modify 1.05V circuit	Delete PQ24,PQ26,PL7,PD17,PC82,PC81,PR109,PQ25,PQ27,PR110 Change PU8 to APL5912-KAC-TRL Change PC85 to 0.01u_0402_25V Change PR112 to 316_0402_1% Change PR13 to 1K_0402_1%
39	Delete reserved 1.5V circuit	Delete PU11,PC95,PR118,PR120,PQ29,PR119,PC99,PC97,PC98,PC96
39	Change 1.5V IC	Change PU10 from APL5151 to G914
40	Add snubber for CPU CORE	Add 4.7_1206_5% to PR131,PR151 Add 680P_0603_50V to PC108,PC120
37,38	Add bead at 3V/5V and 1.2V/1.8V input for EMI requirement	Add PL11,PL12 to replace PJ10,PJ11

DVT

34	Change VS resistor to 33 ohm	Change PR9 from 47_1206_5% to 33_1206_5%
34	Change 1N4148 to lead free P/N	Change PD2,PD3,PD4 P/N to SC11N414880
40	Change HMBT2222 to lead free P/N	Change PQ37 P/N to SB322220080
38	Raise 1.8V to 1.82V for HW requirement	Change PR94 from 10K_0402_1% to 10.2K_0402_1%

PVT

34	Change VS resistor to standard part	Change PR9 from 33_1206_5% to 68_1206_5% Add 68_1206_5% at PR155
38	Change 1.8VALWP power sequence for HW requirement	Change 47K_0402_1% from PR100 to PR156 Delete PC76 Change PC68 from 0.01u_0402_25V to 4700P_0402_25V

Pre-MP

38	Add BOOST 2.2 ohm and snubber at 1.8V / 1.2V for EMI	Add 4.7_1206_5% to PR157,PR158 Add 680P_0603_50V to PC123,PC124 Change PR90,PR91 from 0_0603_5% to 2.2_0603_5%
42	Change CPU CORE mosfet for EMI	Change PQ30,PQ34 from A04408 to IRF7821 Change PQ31,PQ35 from A04410 to IRF7832
42	Delete CPU VID 0 ohm debug resistor	Delete PR122,PR123,PR125,PR127,PR129,PR130

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