

Compal confidential

Schematics Document
Mobile Yonah uFCPGA with Intel
Calistoga_PM+ICH7-M core logic
2005-08-26
REV:0.2

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Model:HAQAA

File Name : LA-3011P

NAPA

Mobile Yonah

uFCPGA-479 CPU

page 4, 5, 6

Thermal Sensor
ADM1032AR

page 4

Clock Generator
ICS9LPRS325AKLFT

page 15

Accelerometer
LIS3L02AQ3TR

page 28

Intel Calistoga MCH
945PM
PCBGA 1466
page 7, 8, 9, 10, 11, 12

H_A#(3...31)

FSB

533/667MHz

H_D#(0...63)

DDR2 -400/533/667

Dual Channel

DDR2-SO-DIMM X2
BANK 0, 1, 2, 3
page 13, 14

Intel ICH7-M
mBGA-652
page 19, 20, 21, 22

DMI

USB2.0

Azalia

PCI BUS

CardBus Controller
TI PCI7412
page 22, 23

Slot 0
page 23

1394 port
page 22

5in1 Slot
page 22

LPC BUS

TPM1.2
SLB9635TT1.2
page 38

Super I/O
LPC47N217&207
page 33, 38

FIR
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ENE KB910QF
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CIR
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Touch Pad
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Int.KBD
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BIOS
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AMP & Audio Jack
TPA0232
page 30

Audio CKT
ALC861
page 29

SATA HDD Connector
page 19

PATA ODD Connector
page 19

USB conn x2
(Sub Board)
page 24

(port 2, 3)

BT Conn
page 24

(port 7)

USB conn x2
page 24

(port 4, 5)

USB2.0 HUB /
FP Conn
page 38

(port 0)

FingerPrinter UPEK TCS3C/TCD42A
USBx1
page 38

USB conn x1
(Docking)
page 34

(port 6)

PCI-E BUS

(port 1)

Mini Express Card
page 28

10/100/1000 LAN
82562GX/82573E/82573V
page 26, 27

RJ45/11 CONN
page 26

LCD CONN
page 17

nVIDIA G72/G73
ATI M52/M54
page 18

CRT / TV-OUT
page 16

LED
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RTC CKT.
page 19

Docking
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Power On/Off CKT.
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DC/DC Interface CKT.
page 39

Power Circuit DC/DC
Page, 40, 41, 42, 43, 44, 45, 46

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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (18.5V)	NA	NA	NA
B+	AC or battery power rail for power circuit	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V power rail for Processor I/O and MCH/I/CH core power	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+2.5VALW	3.3V always on power rail	ON	ON	ON*
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_VCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Internal PCI Devices

DEVICE	Bus	PCI Device ID	IDSEL #
LAN	1	D8	AD24
Azalia	0	D27	AD11
PCI-E	0	D28	AD12
USB1.1/2.0	0	D29	AD13
PCI to PCI (DMI to PCI)	0	D30	AD14
AC97 MODEM	0	D30	AD14
AC97 Audio	0	D30	AD14
PATA/SATA	0	D31	AD15
LPC I/F	0	D31	AD15
SMBUS	0	D31	AD15
CPU I/F	0	D31	AD15
DMA	0	D31	AD15
PMU	0	D31	AD15

External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
CARD BUS	D6	AD22	2	ABCD

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 1%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0.100 V
1	8.2K +/- 1%	0.216 V	0.250 V	0.289 V
2	18K +/- 1%	0.436 V	0.503 V	0.538 V
3	33K +/- 1%	0.712 V	0.819 V	0.875 V
4	56K +/- 1%	1.036 V	1.185 V	1.264 V
5	100K +/- 1%	1.453 V	1.650 V	1.759 V
6	200K +/- 1%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

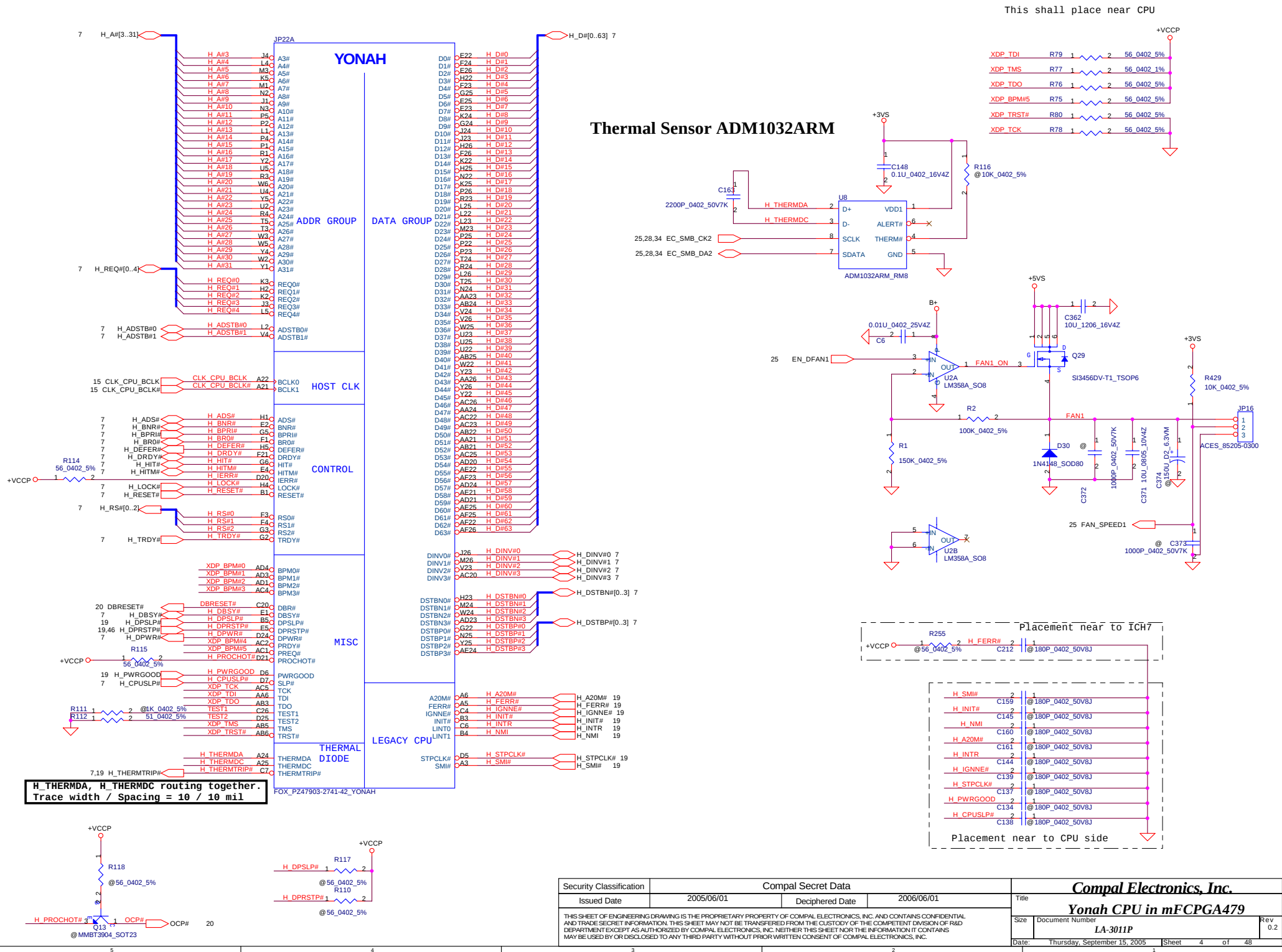
Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

SKU ID Table

SKU ID	SKU
0	
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
VGA	PM@ GM@
LAN	82573G@ 82573L@ 82573@ 82562@
INT MIC.	45MIC@
DOCKING	WD@ WOD@
CIR	CIR@
FIR	FIR@
SUPER I/O	217@ SI207@
Battery	45@



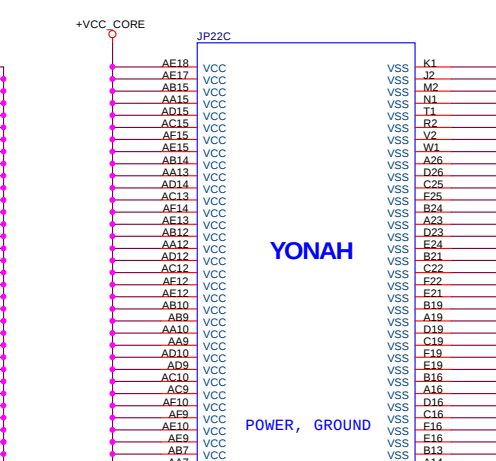
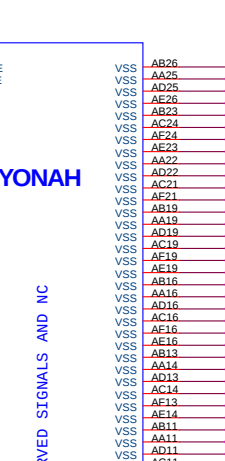
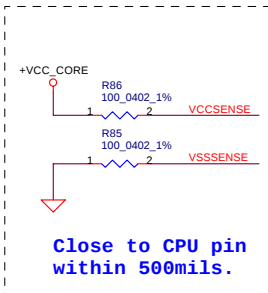
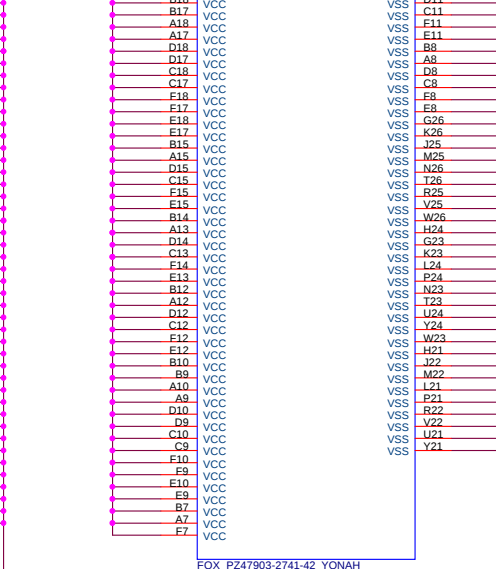
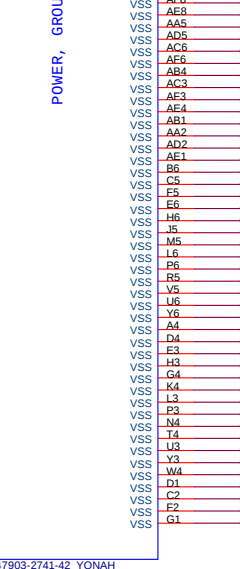
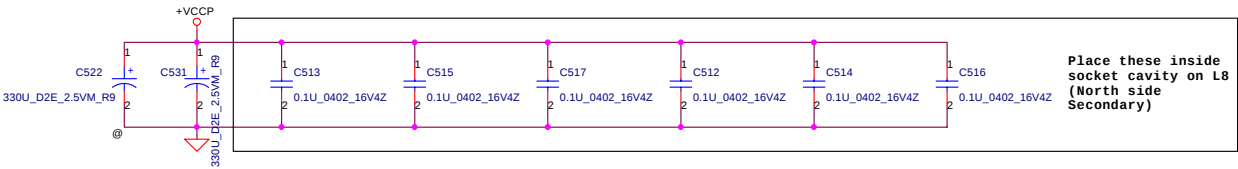
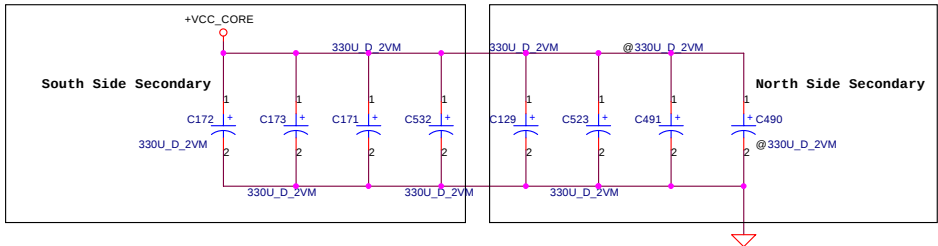
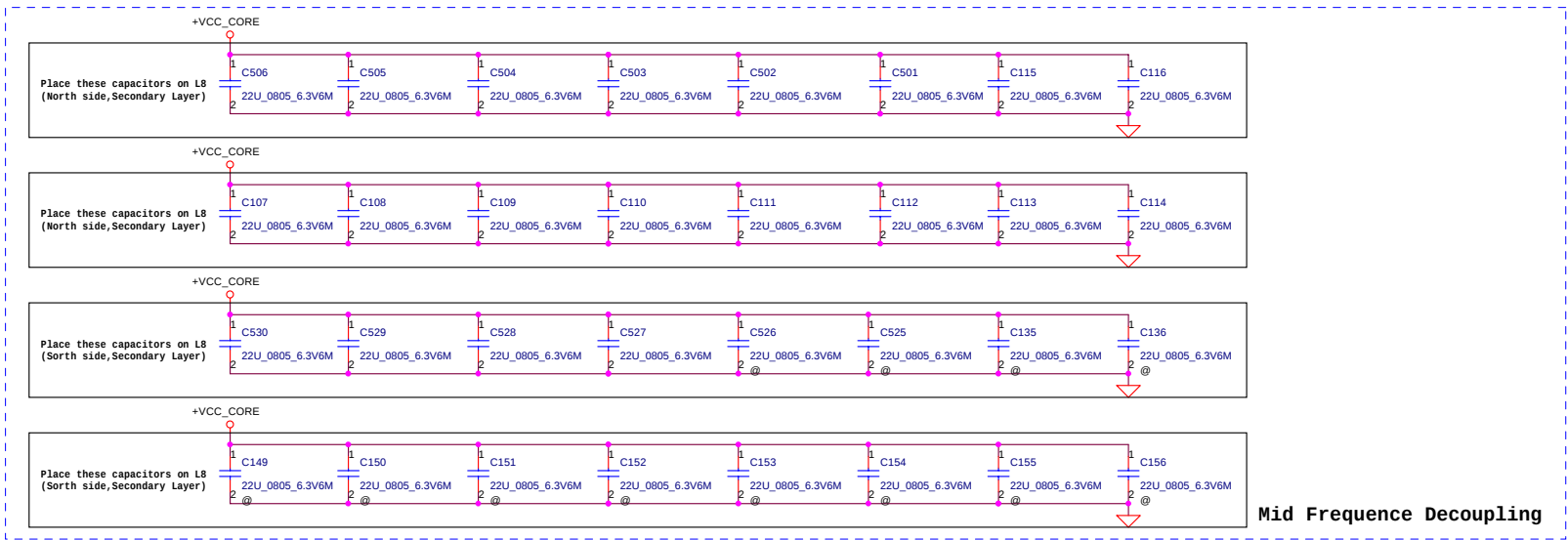
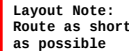
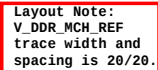
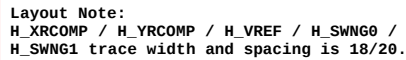


Figure 10 illustrates the pin connections for the CPU module. The diagram shows two rows of connections. The top row shows connections for pins 46, 46, 46, 46, 46, 46, and 46 on the left, connected to H_PSI#, CPU_VID0, CPU_VID1, CPU_VID2, CPU_VID3, CPU_VID4, and CPU_VID5 respectively. These are then connected to H_PSI#, AE6, AD6, AF5, AE5, AE4, and AE2 on the right. The bottom row shows connections for pins 15, 15, and 15 on the left, connected to V_CPU_GTLREF, CPU_BSEL0, CPU_BSEL1, and CPU_BSEL2 respectively. These are connected to AD26, B22, B23, and C21 on the right. The right side of the diagram also shows connections for PSI#, VID0, VID1, VID2, VID3, VID4, VID5, and VID6, and GTLREF, BSEL0, BSEL1, and BSEL2.

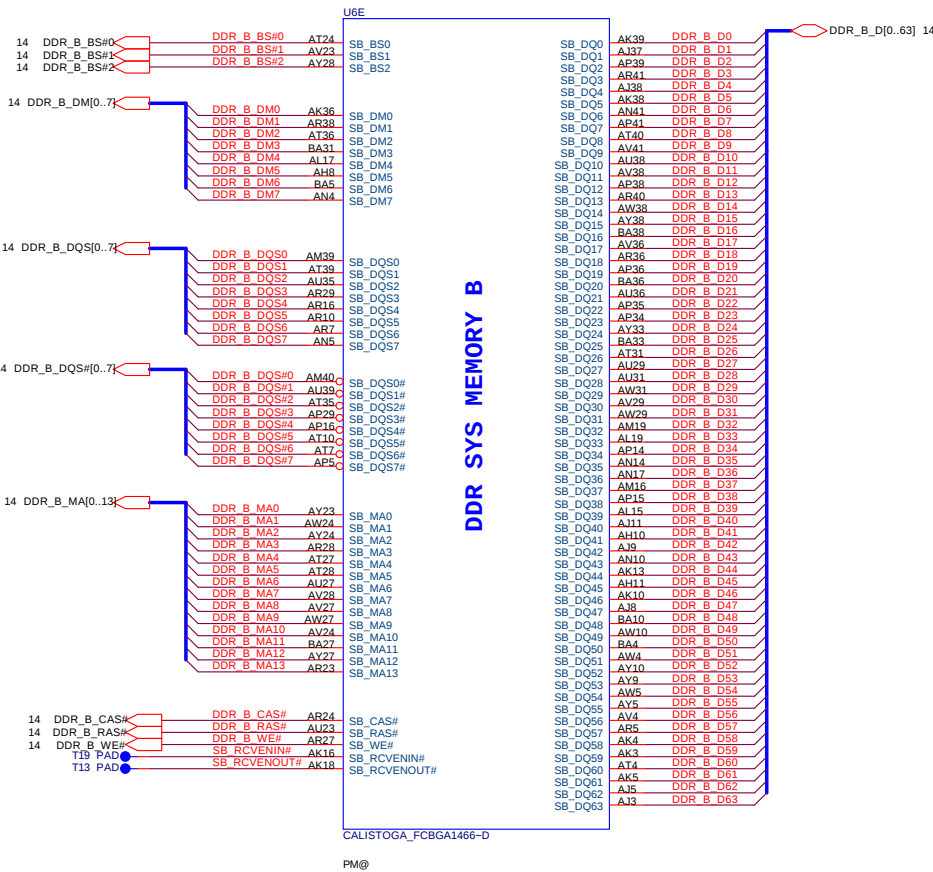
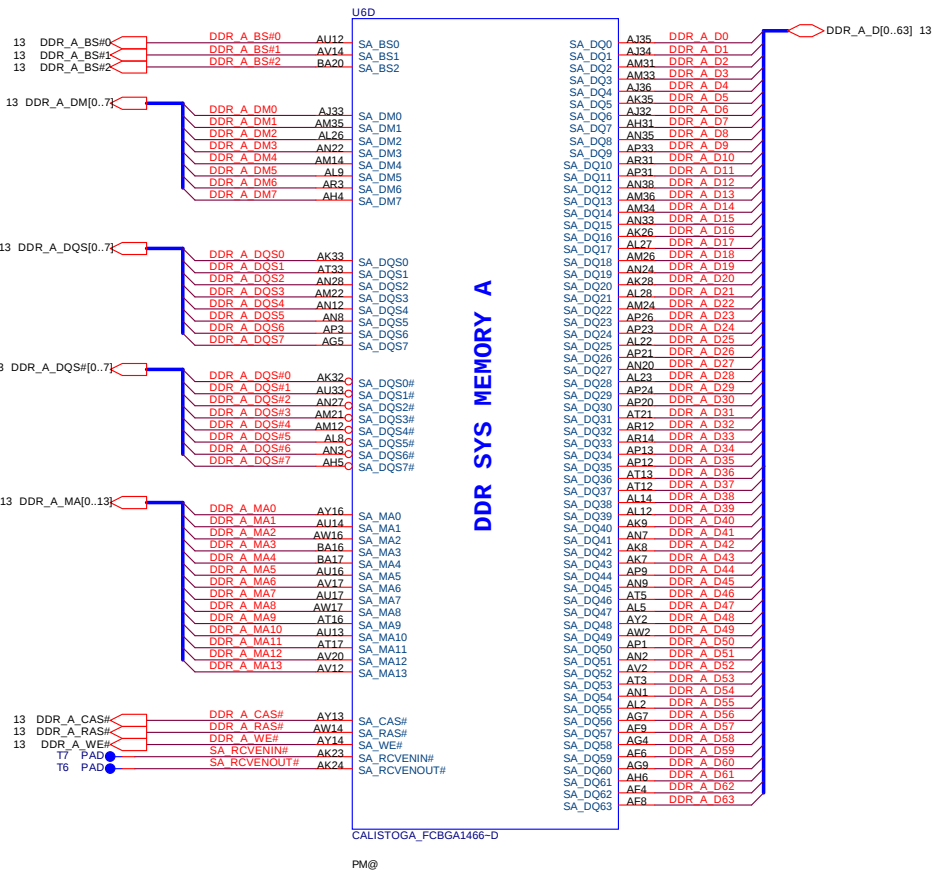




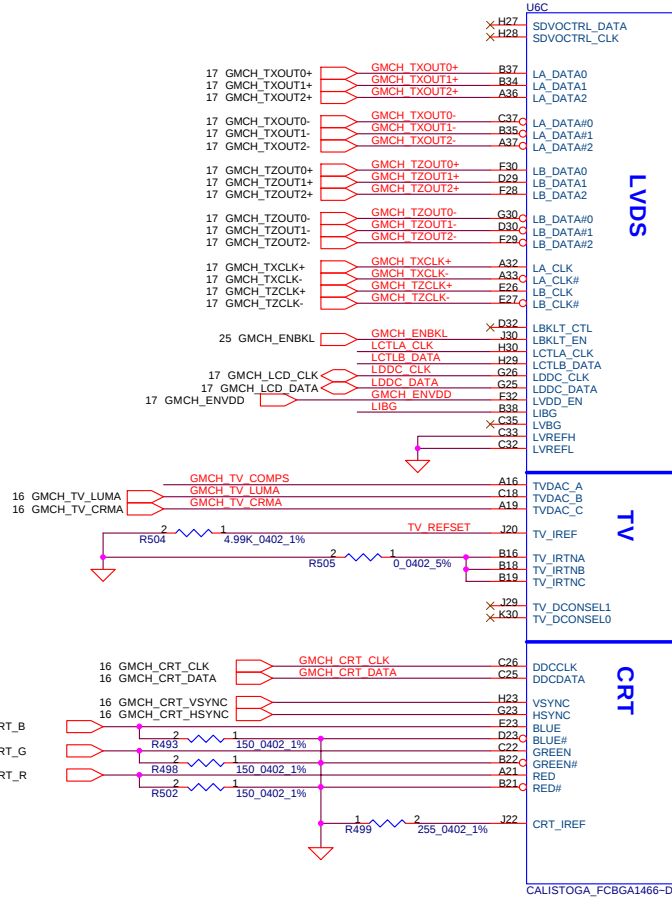
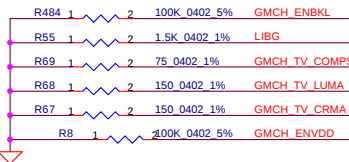
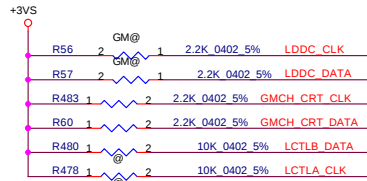
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PEGCOMP trace width and spacing is 18/25 mils.

EXP_COMP1	EXP_COMP0	F34	PCEI GTX C MRX N0
EXP_RXN0	G38	PCEI GTX C MRX N1	
EXP_RXN1	H34	PCEI GTX C MRX N2	
EXP_RXN2	J38	PCEI GTX C MRX N3	
EXP_RXN3	L34	PCEI GTX C MRX N4	
EXP_RXN4	M38	PCEI GTX C MRX N5	
EXP_RXN5	N34	PCEI GTX C MRX N6	
EXP_RXN6	P38	PCEI GTX C MRX N7	
EXP_RXN7	R34	PCEI GTX C MRX N8	
EXP_RXN8	T38	PCEI GTX C MRX N9	
EXP_RXN9	V34	PCEI GTX C MRX N10	
EXP_RXN10	W38	PCEI GTX C MRX N11	
EXP_RXN11	Y34	PCEI GTX C MRX N12	
EXP_RXN12	AA38	PCEI GTX C MRX N13	
EXP_RXN13	AB34	PCEI GTX C MRX N14	
EXP_RXN14	AC38	PCEI GTX C MRX N15	
EXP_RXN15			
EXP_RXP0	D34	PCEI GTX C MRX P0	
EXP_RXP1	E38	PCEI GTX C MRX P1	
EXP_RXP2	G34	PCEI GTX C MRX P2	
EXP_RXP3	H38	PCEI GTX C MRX P3	
EXP_RXP4	J34	PCEI GTX C MRX P4	
EXP_RXP5	L38	PCEI GTX C MRX P5	
EXP_RXP6	M34	PCEI GTX C MRX P6	
EXP_RXP7	N38	PCEI GTX C MRX P7	
EXP_RXP8	P34	PCEI GTX C MRX P8	
EXP_RXP9	R38	PCEI GTX C MRX P9	
EXP_RXP10	T34	PCEI GTX C MRX P10	
EXP_RXP11	V38	PCEI GTX C MRX P11	
EXP_RXP12	W34	PCEI GTX C MRX P12	
EXP_RXP13	Y38	PCEI GTX C MRX P13	
EXP_RXP14	AA34	PCEI GTX C MRX P14	
EXP_RXP15	AB38	PCEI GTX C MRX P15	

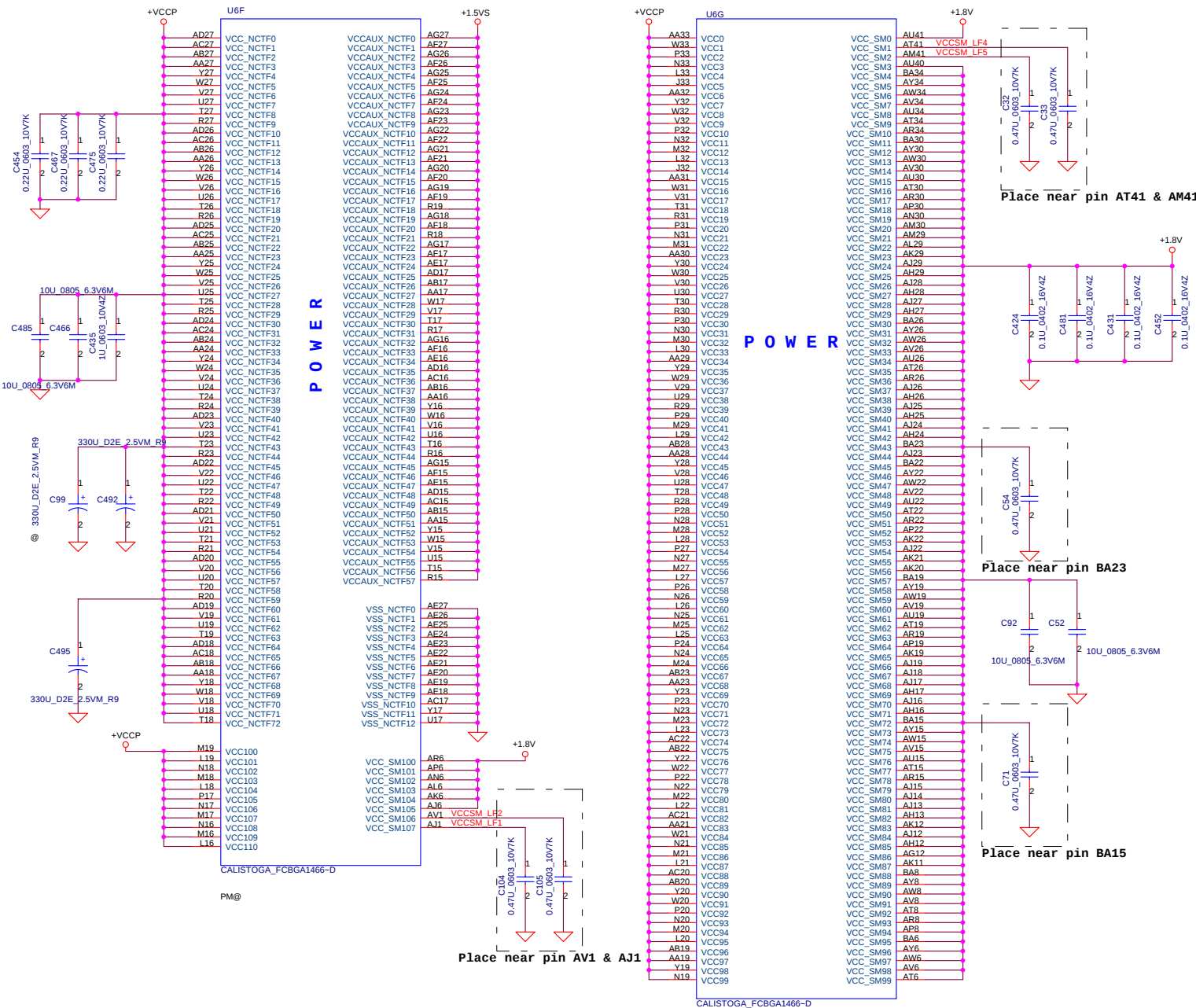
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EXP_TXN1	G40	C384	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N1
EXP_TXN2	H36	C384	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N2
EXP_TXN3	J40	C384	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N3
EXP_TXN4	L36	C398	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N4
EXP_TXN5	M40	C38	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N5
EXP_TXN6	N36	C382	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N6
EXP_TXN7	P40	C27	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N7
EXP_TXN8	R36	C386	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N8
EXP_TXN9	T40	C40	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N9
EXP_TXN10	V36	C380	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N10
EXP_TXN11	W40	C29	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N11
EXP_TXN12	Y36	C394	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N12
EXP_TXN13	AA40	C42	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N13
EXP_TXN14	AB36	C387	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N14
EXP_TXN15	AC40	C31	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N15
EXP_TXP0	D36	C401	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P0
EXP_TXP1	E40	C35	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P1
EXP_TXP2	G36	C385	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P2
EXP_TXP3	H40	C34	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P3
EXP_TXP4	J36	C389	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P4
EXP_TXP5	L40	C37	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P5
EXP_TXP6	M36	C383	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P6
EXP_TXP7	N40	C26	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P7
EXP_TXP8	P36	C397	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P8
EXP_TXP9	R40	C39	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P9
EXP_TXP10	T36	C381	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P10
EXP_TXP11	V40	C28	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P11
EXP_TXP12	W36	C395	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P12
EXP_TXP13	Y40	C41	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P13
EXP_TXP14	AA36	C388	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P14
EXP_TXP15	AB40	C30	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P15

Strap Pin Table

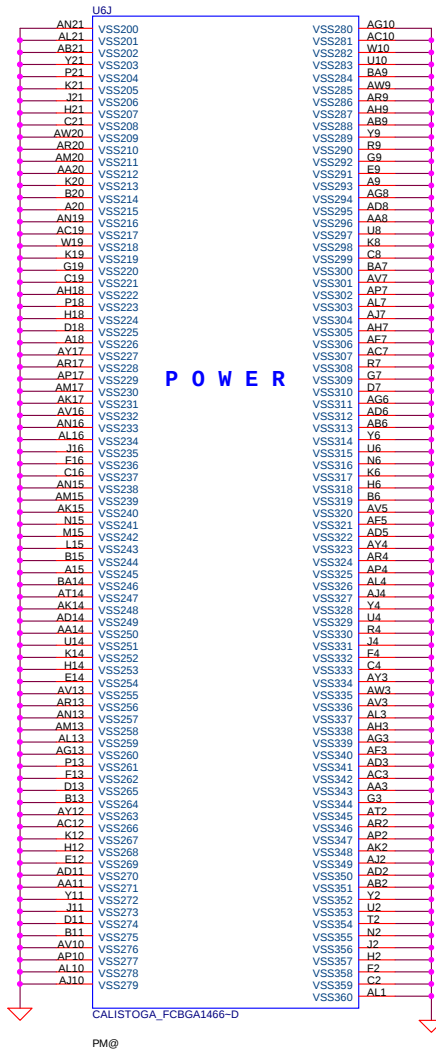
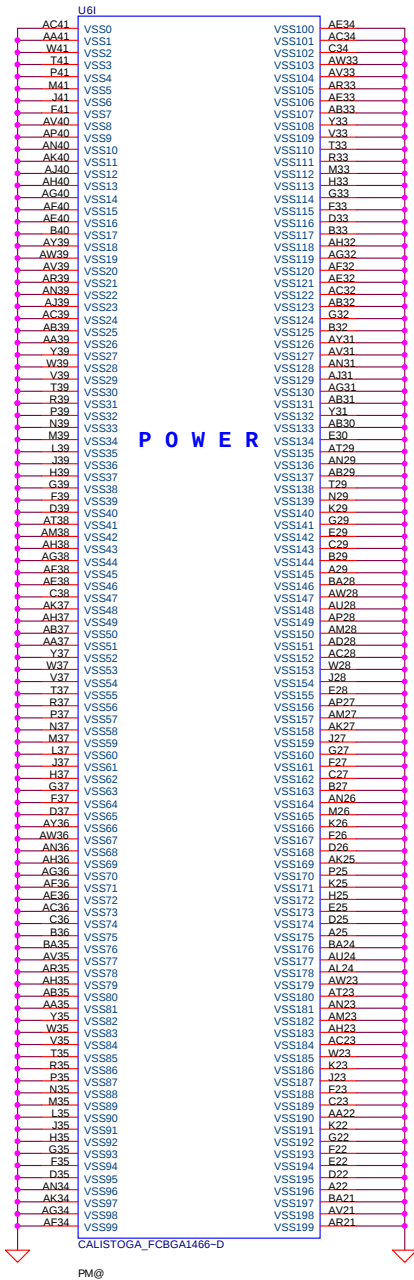
CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal operation (Default)*
CFG11	0 = Calistoga * (According to Intel Napa Schematic Checklist & CRB Rev1.301 document 2.2Kohm pull-downs resistor request) 1 = Reserved
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.

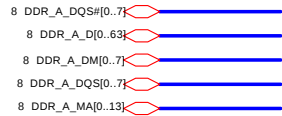
7	CFG5	R513	1	2	@ 2.2K 0402 5%
7	CFG7	R507	1	2	@ 2.2K 0402 5%
7	CFG9	R509	1	2	@ 2.2K 0402 5%
7	CFG11	R514	1	2	@ 2.2K 0402 5%
7	CFG12	R512	1	2	@ 2.2K 0402 5%
7	CFG13	R510	1	2	@ 2.2K 0402 5%
7	CFG16	R506	1	2	@ 2.2K 0402 5%
7	CFG18	R479	1	2	@ 1K 0402 5%
7	CFG19	R482	1	2	@ 1K 0402 5%
7	CFG20	R490	1	2	@ 1K 0402 5%



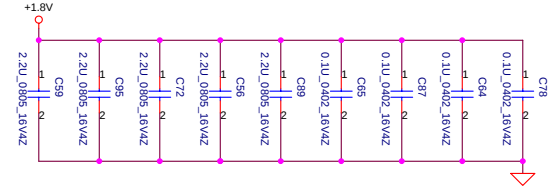
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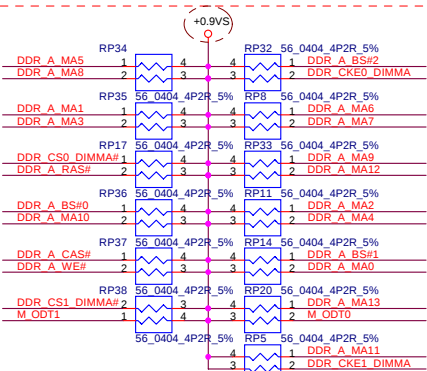
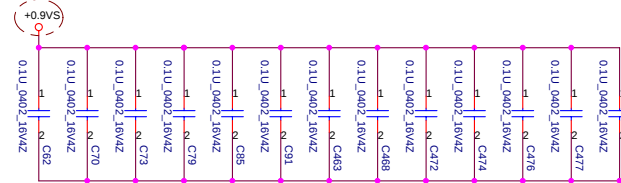
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					LA-3011P	0.2
Date: Thursday, September 15, 2005				Sheet	12	of 48



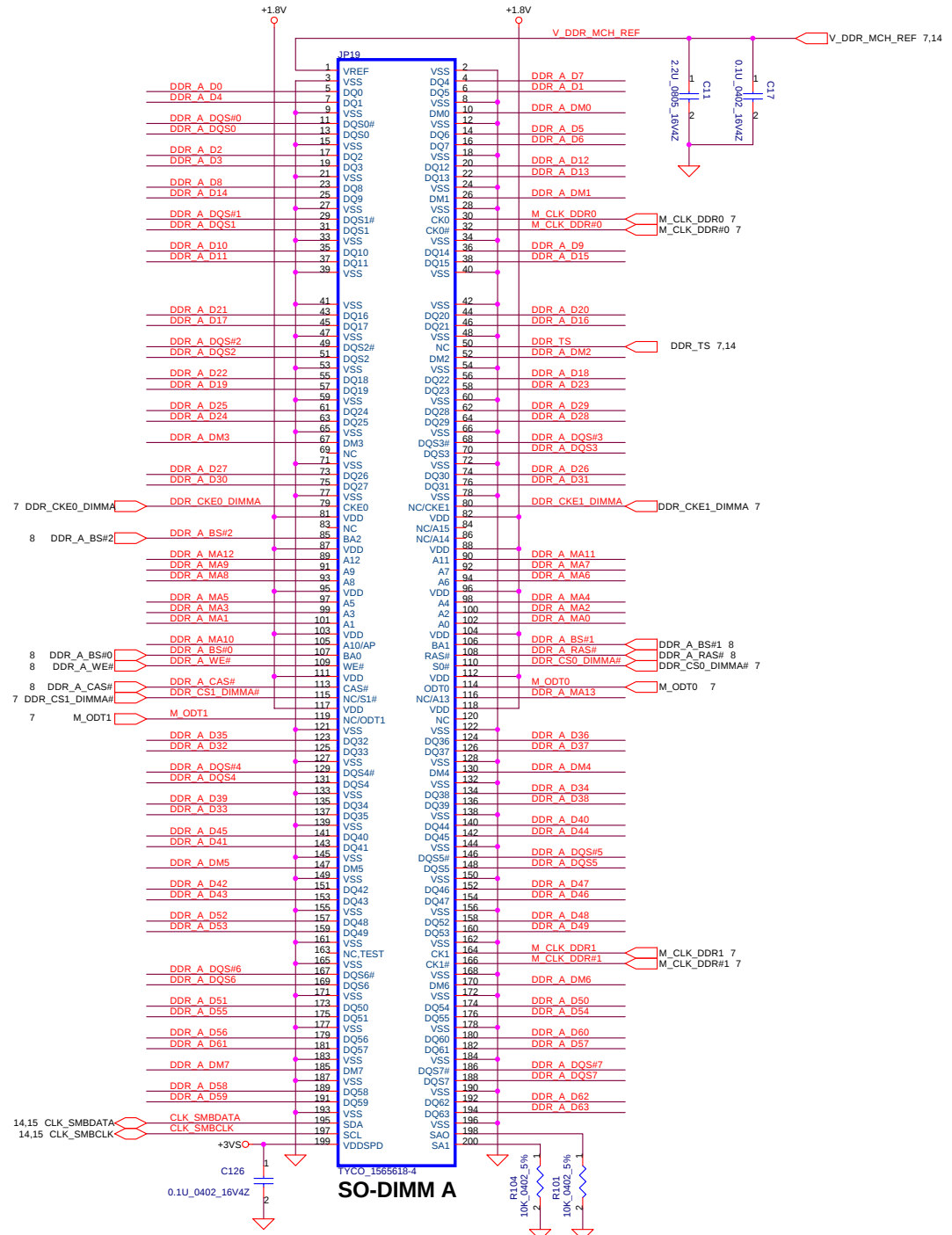
Layout Note:
Place near JP27



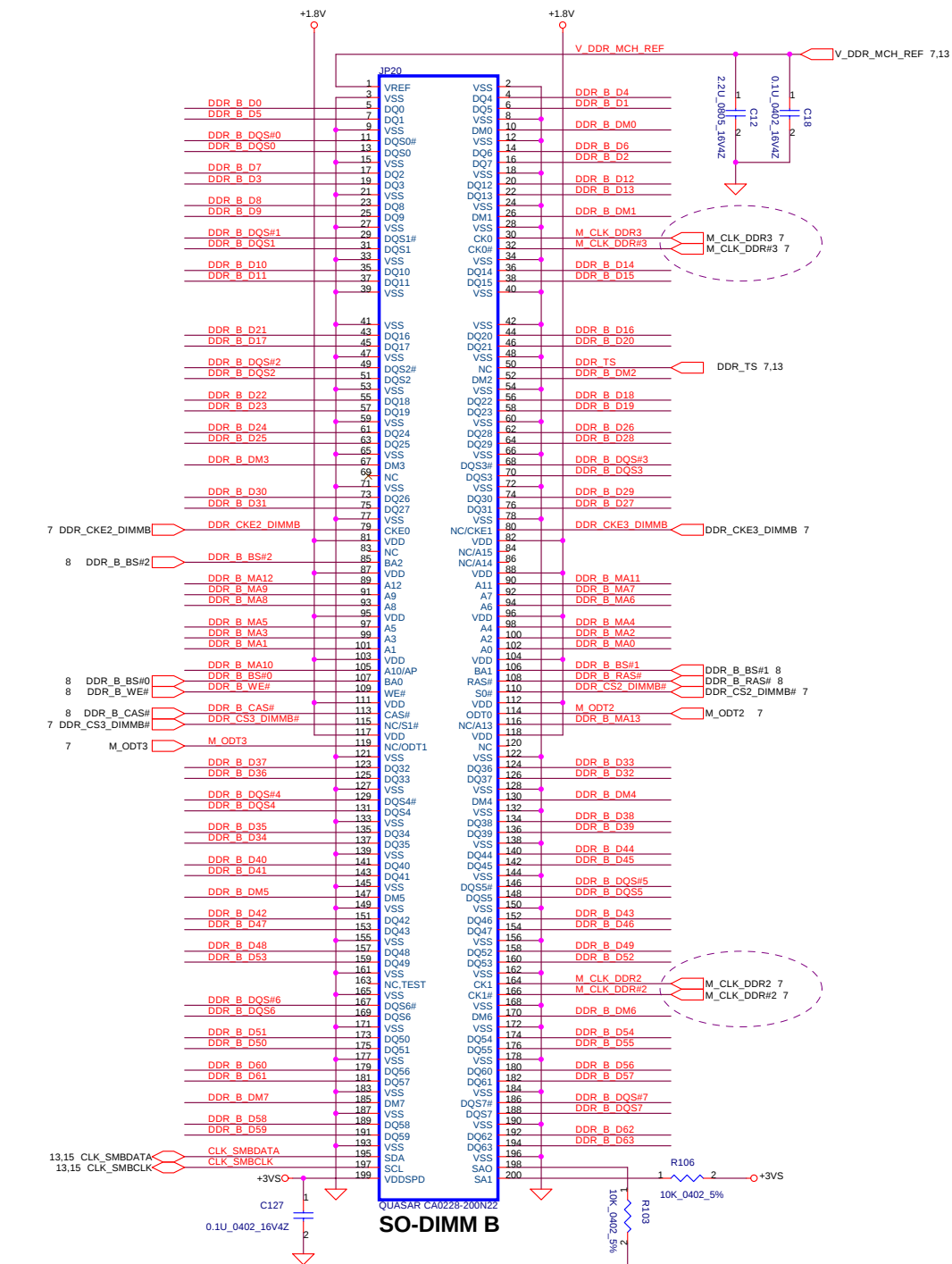
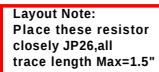
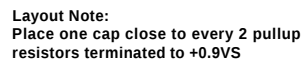
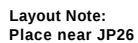
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS



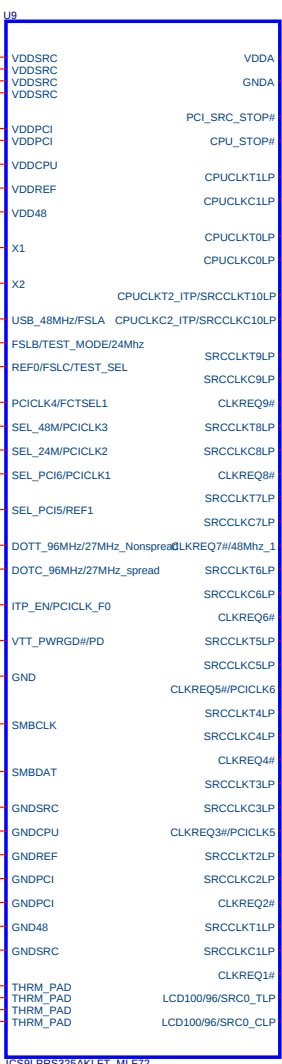
Layout Note:
Place these resistor
closely JP27, all
trace length Max=1.5"



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				2006/06/01				2006/06/01			
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								DDRII-SODIMM SLOT1			
								LA-3011P			
								Rev 0.2			
								Date: Thursday, September 15, 2005			
								Sheet 13 of 48			



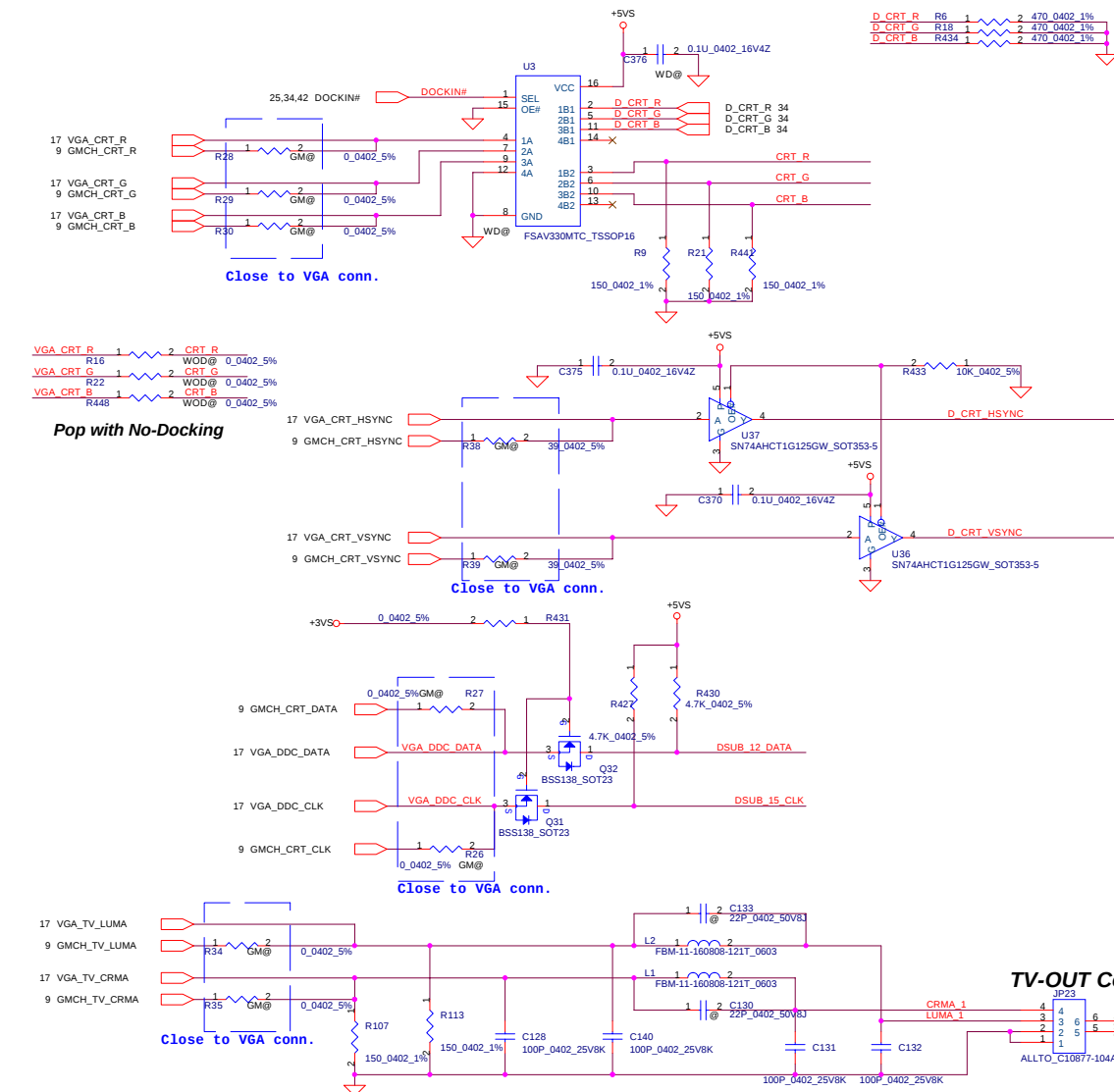
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Issued Date	2005/06/01	Deciphered Date	2006/06/01	Title DDRII-SODIMM SLOT2		
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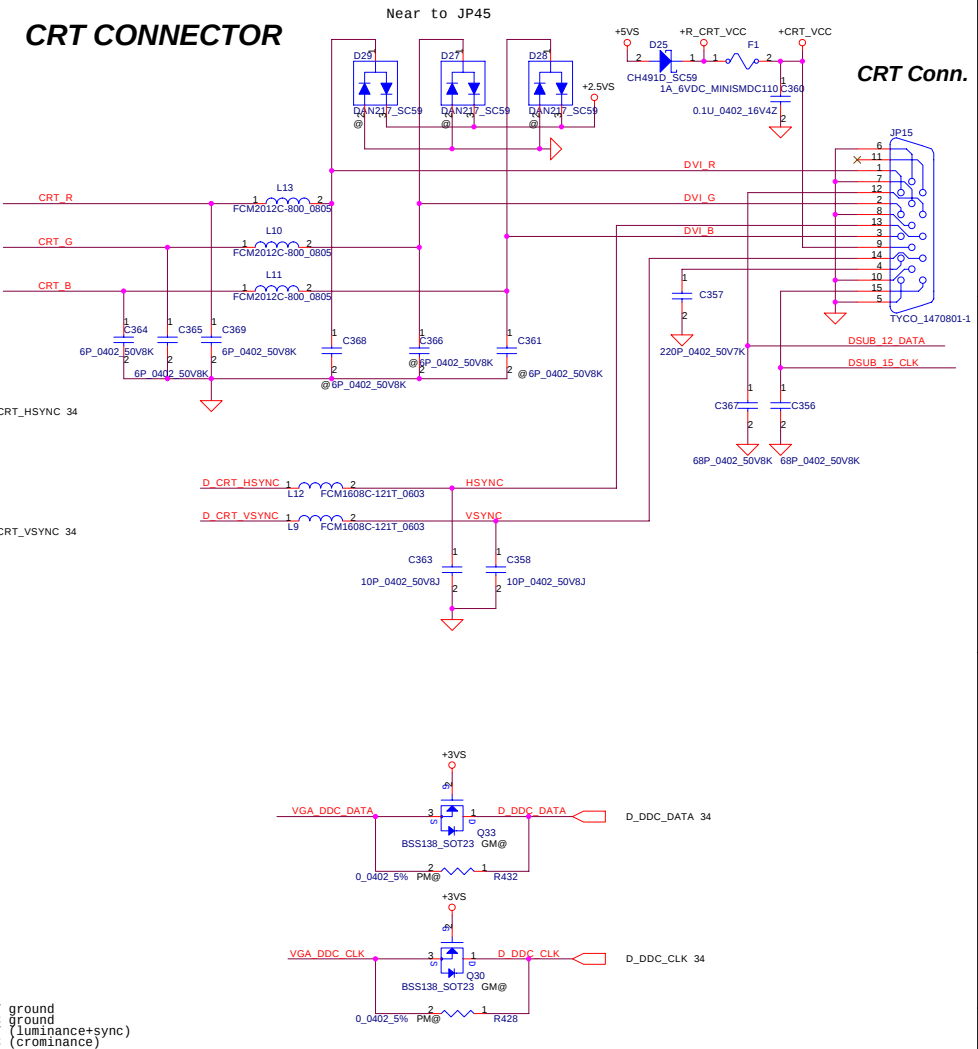
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Issued Date	2005/06/01	Deciphered Date	2006/06/01			
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				Clock generator		
				Size	Document Number	
				LA-3011P		
Date: Thursday, September 15, 2005				Sheet	15 of 48	

CRT Connector

Match with Docking resistor to 150ohm

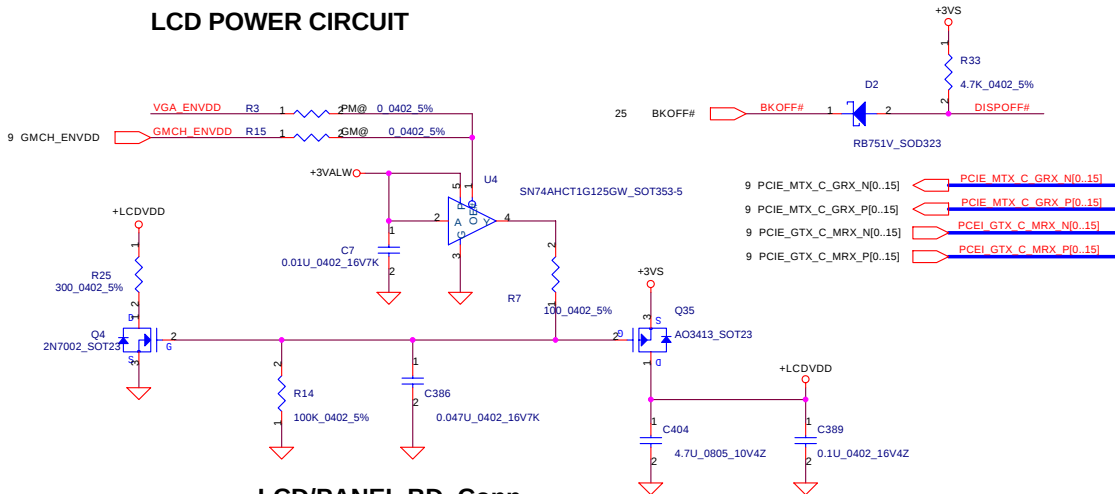


CRT CONNECTOR

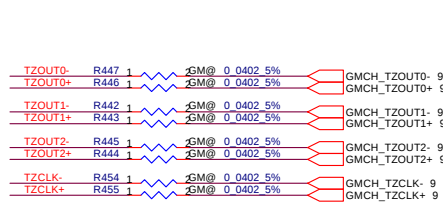
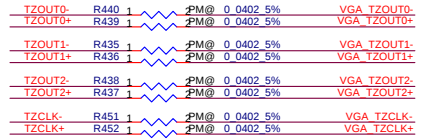
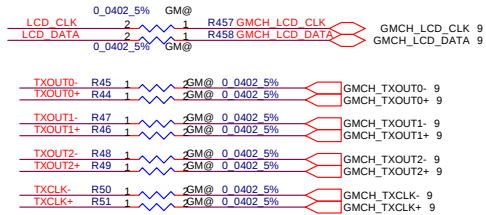
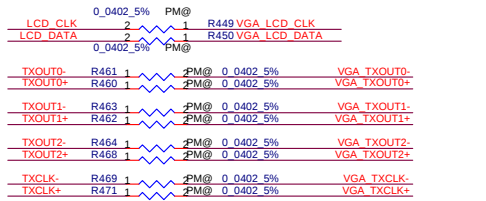
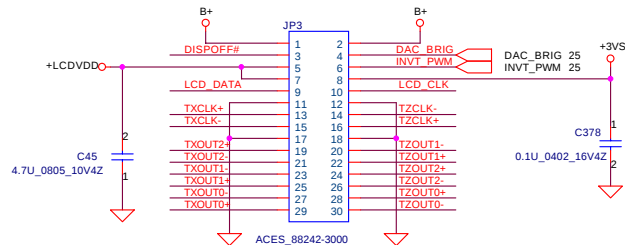


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					LA-3011P	0.2
				Date:	Thursday, September 15, 2005	Sheet 16 of 48

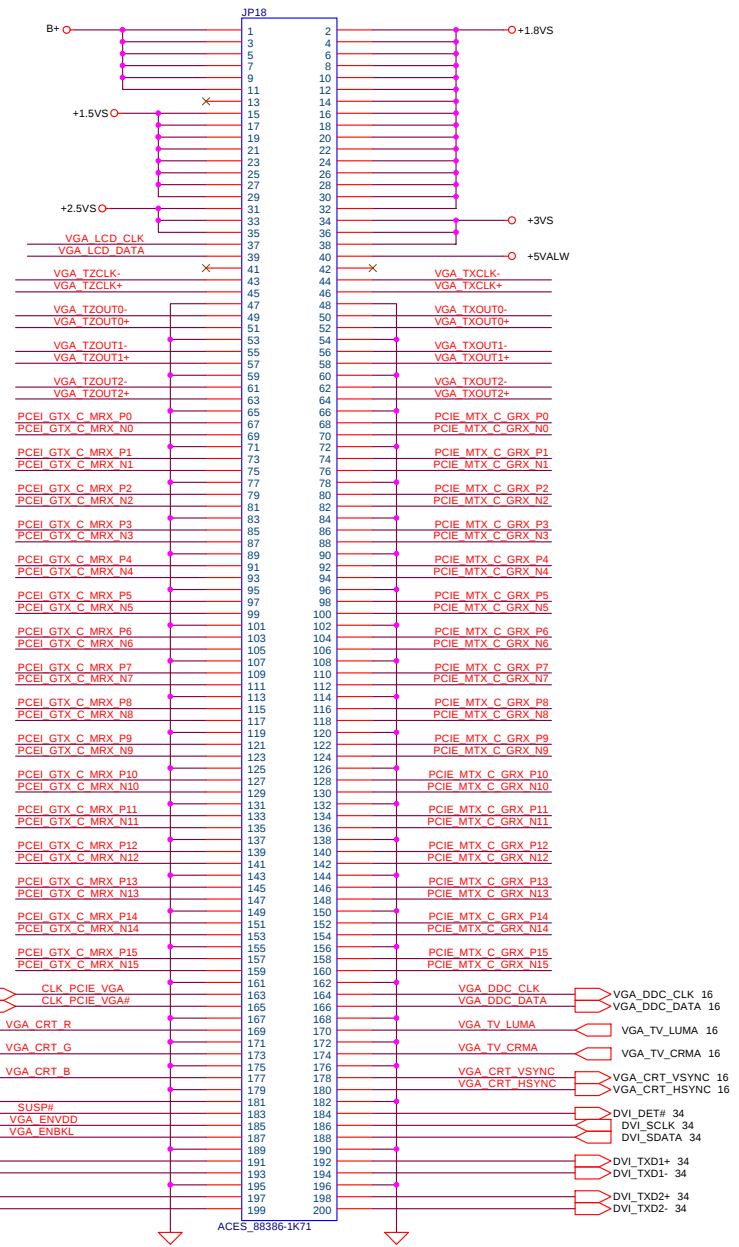
LCD POWER CIRCUIT



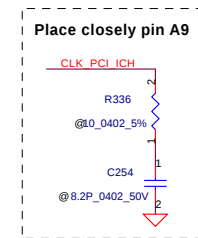
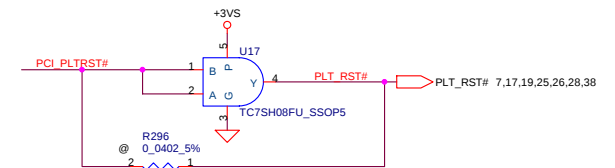
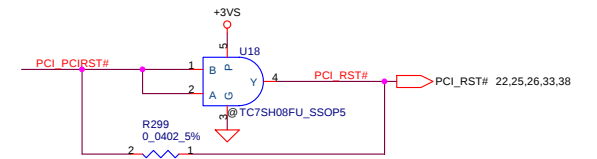
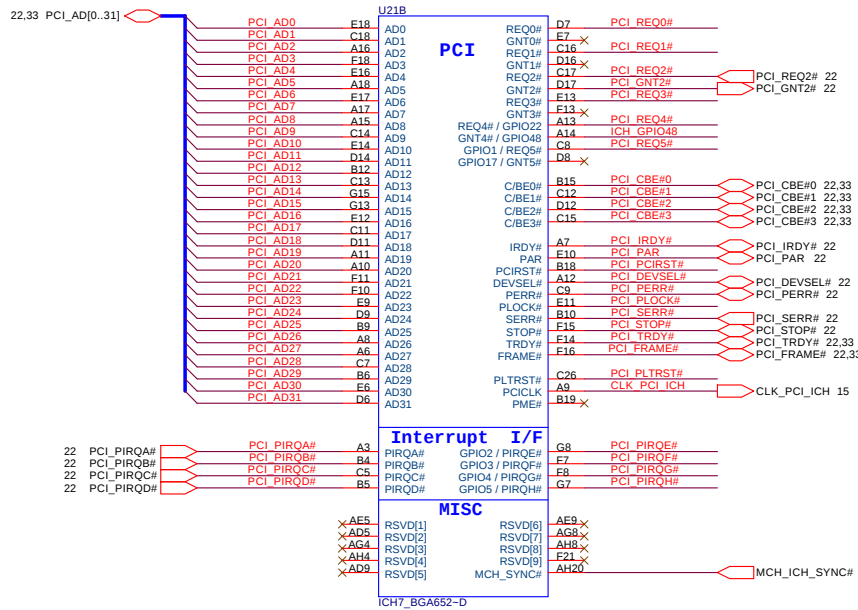
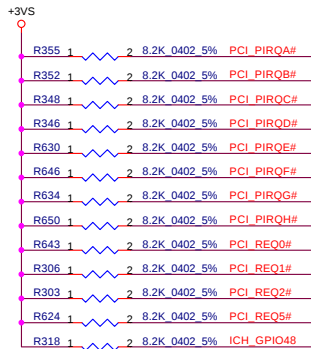
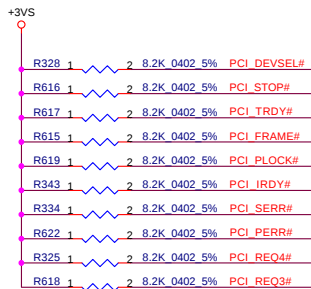
LCD/PANEL BD. Conn.



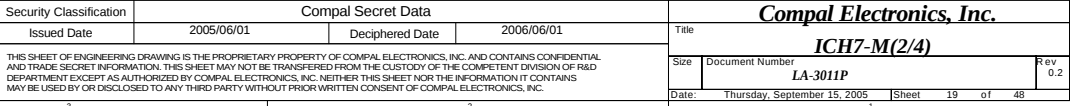
VGA BOARD Conn.

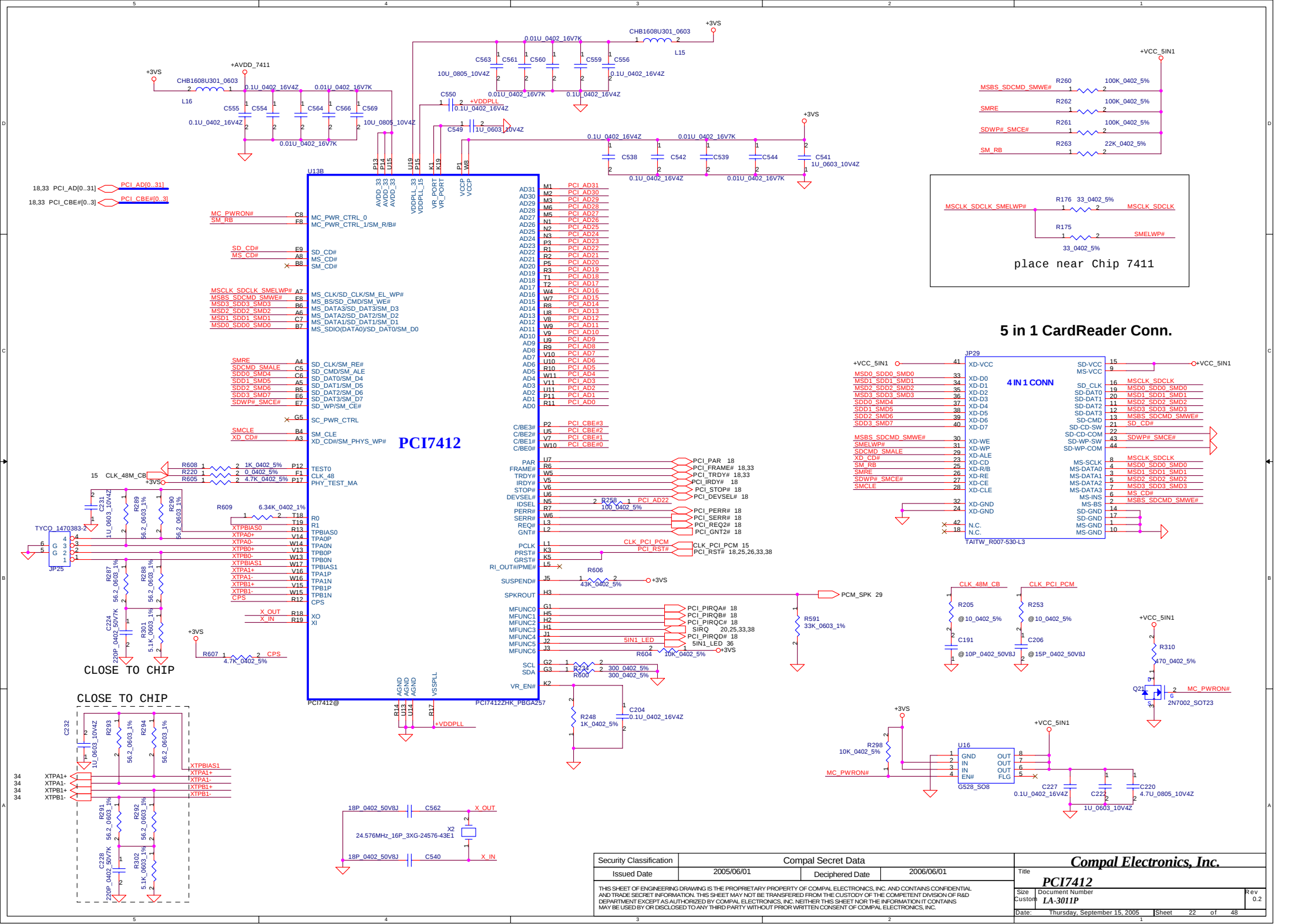


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								Size	Document Number			Rev			
									LA-3011P			0.2			
								Date:	Thursday, September 15, 2005			Sheet	17	of	48
								3				2			

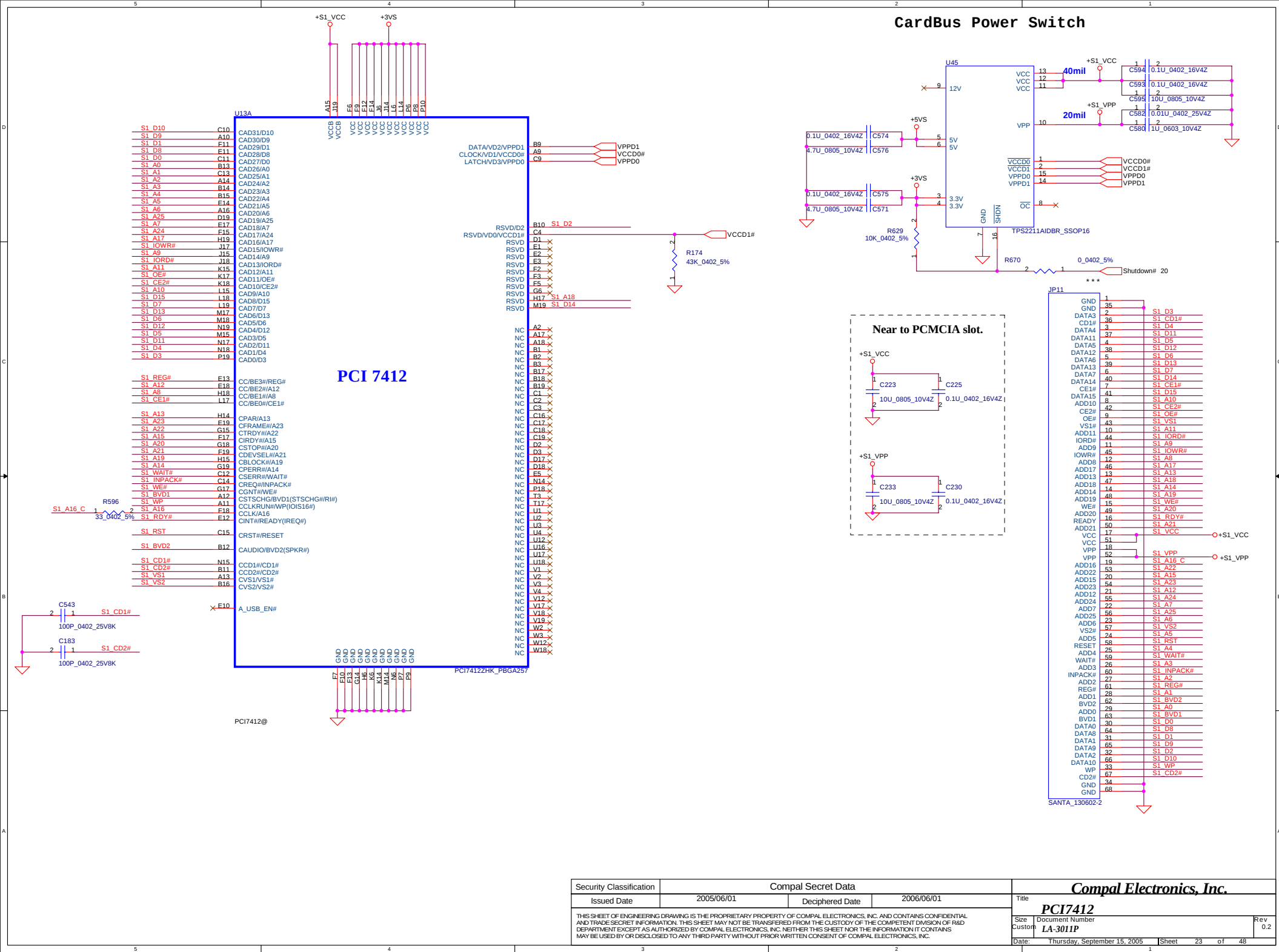


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				LA-3011P	Rev 0.2
Date: Thursday, September 15, 2005				Sheet 18	of 48

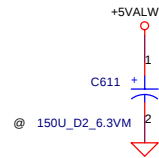




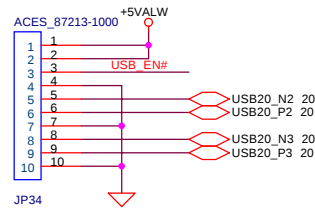
CardBus Power Switch



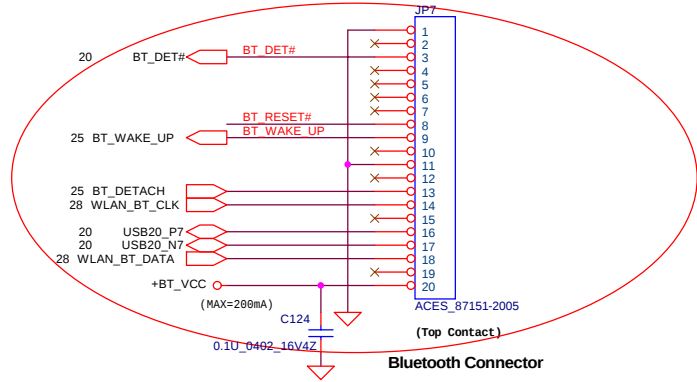
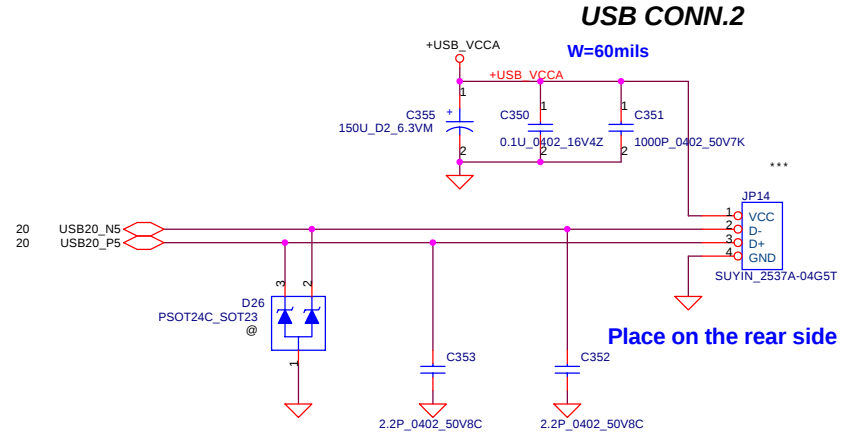
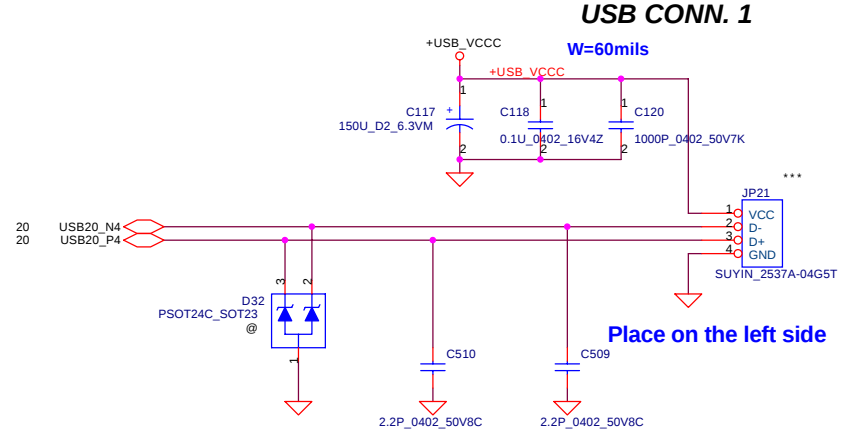
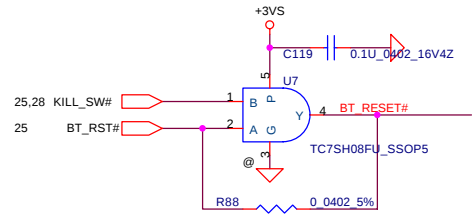
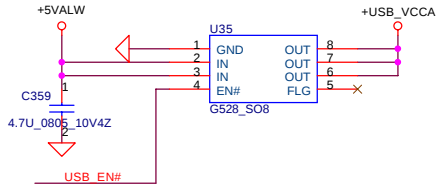
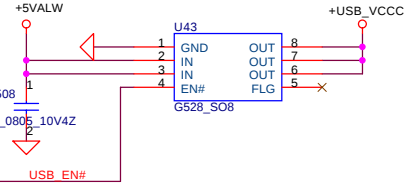
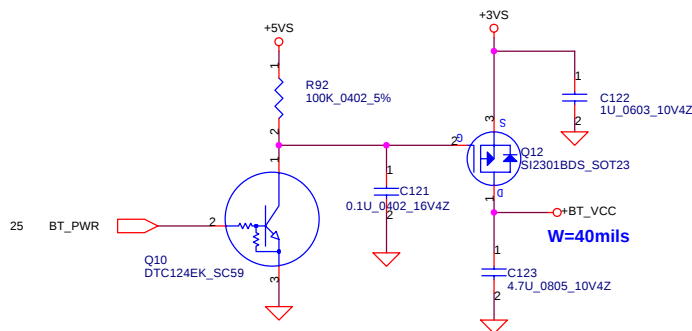
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Issued Date	2005/06/01	Deciphered Date	2006/06/01	PCI7412	
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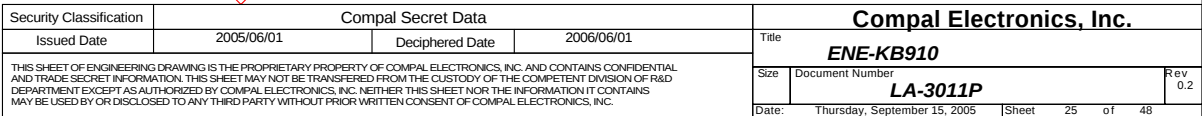
2 port in right side



Bluetooth Conn.

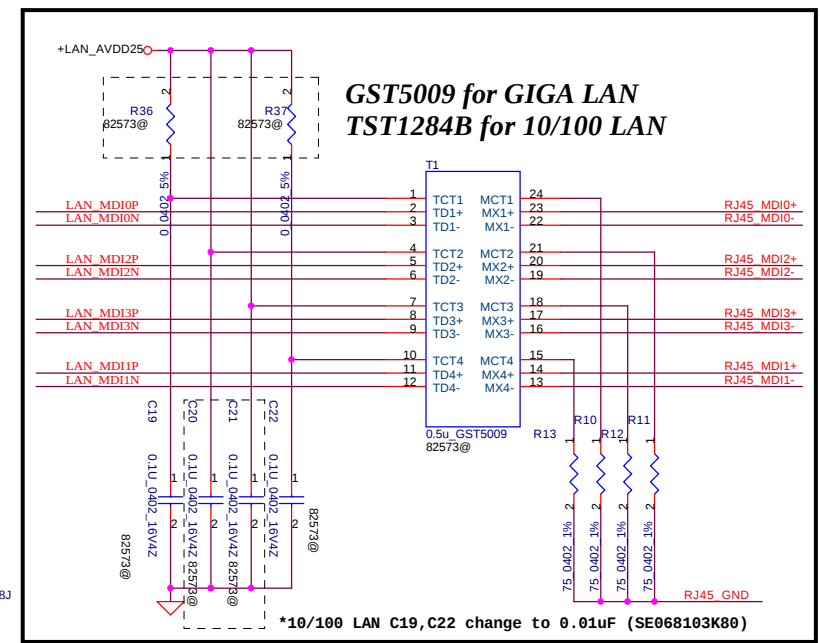
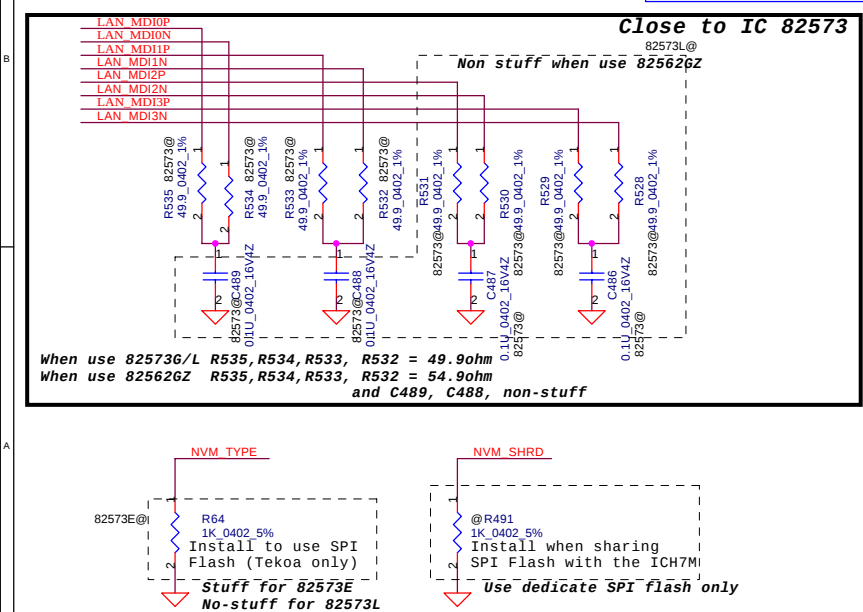
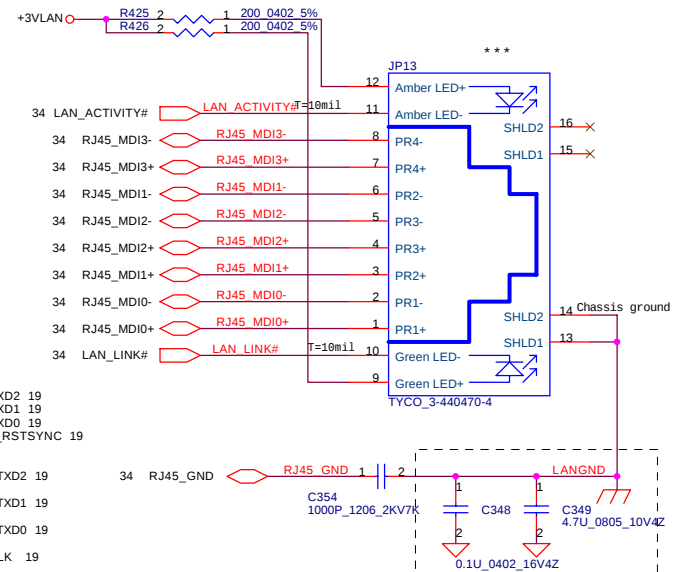
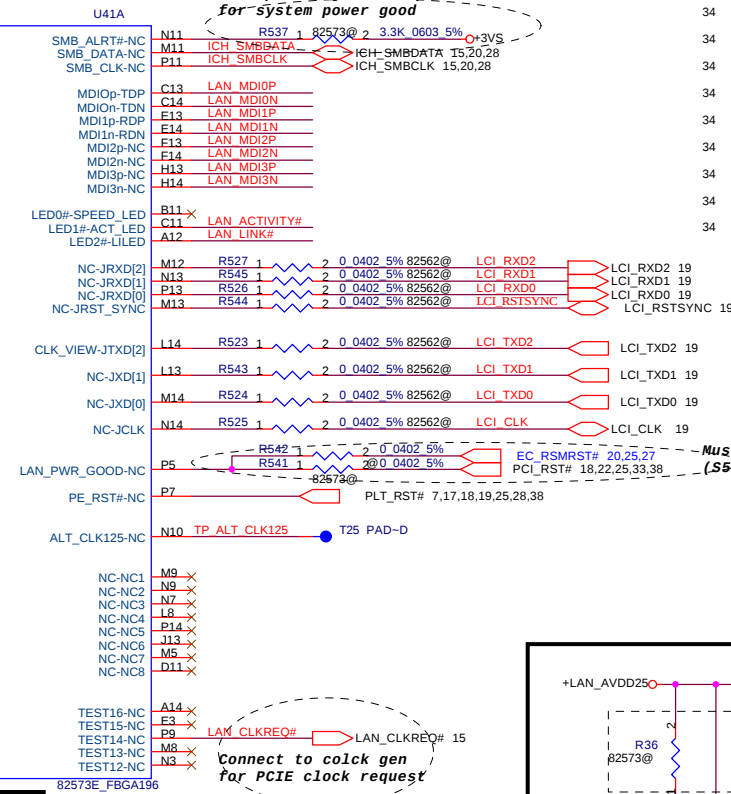
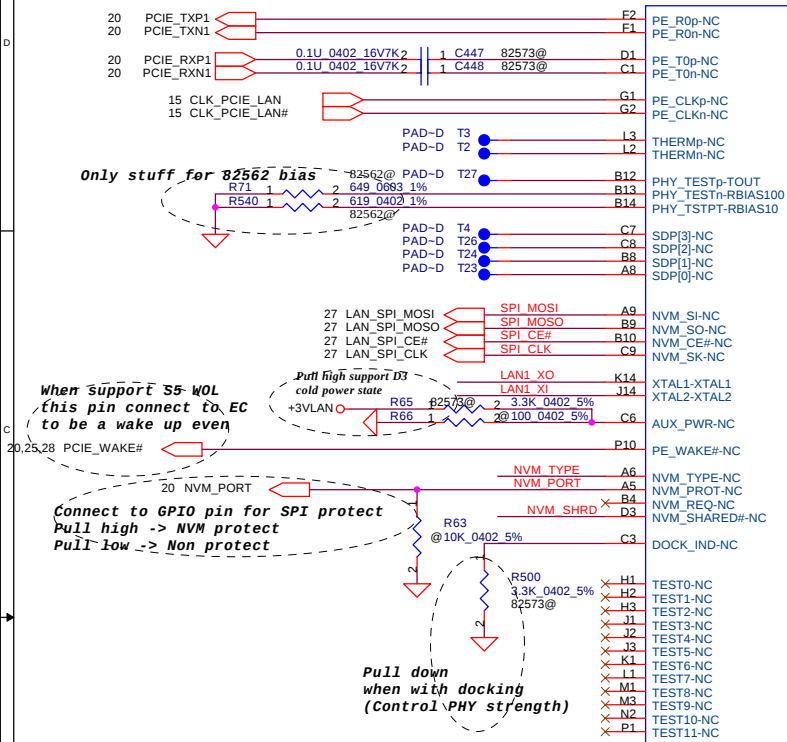


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Size	Document Number	Rev		0.2	
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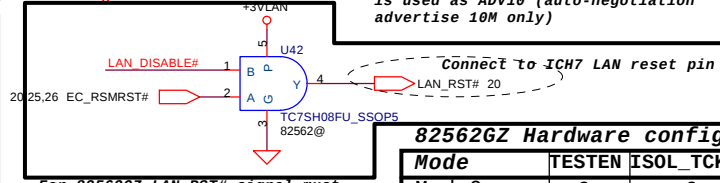
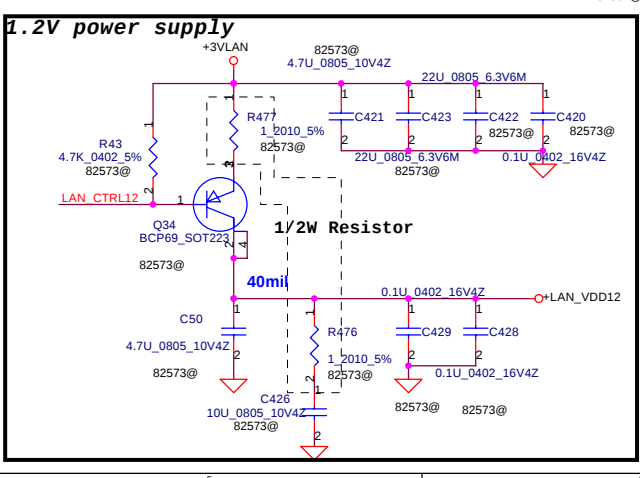
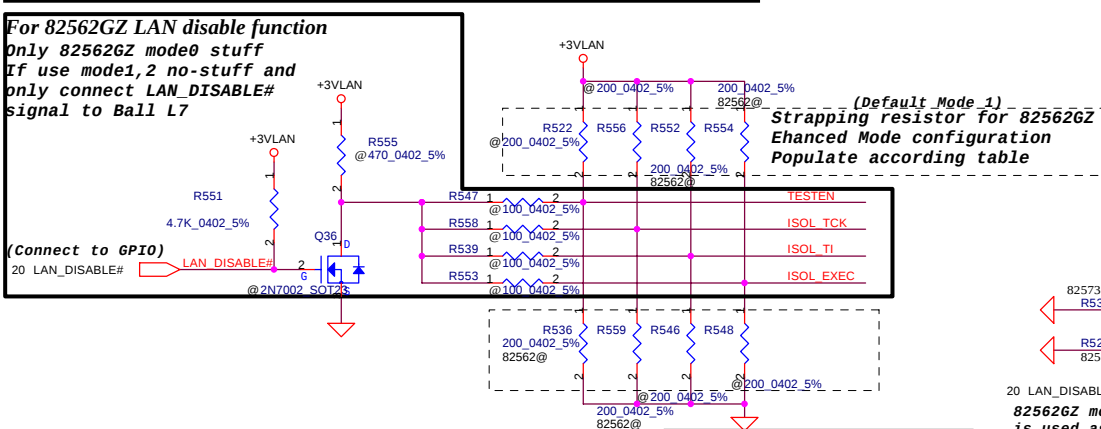
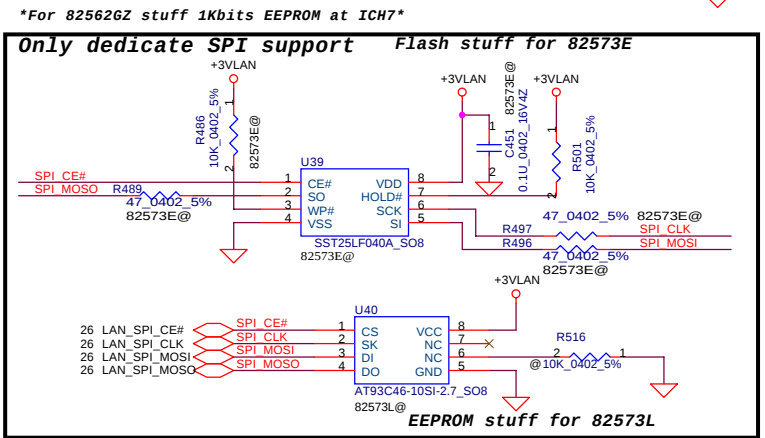
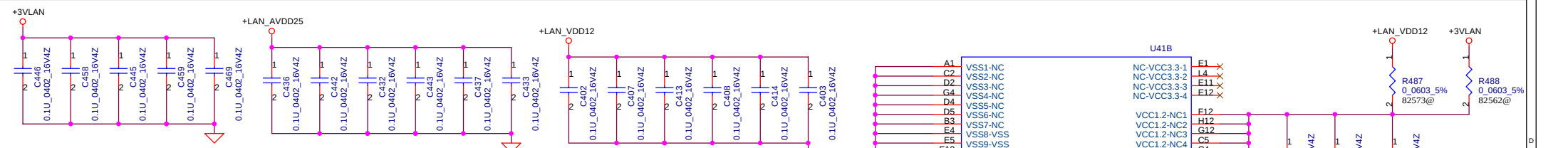


Tekoa 82573E -> IAMT support only (WoL Support)
Vidalia 82573L -> No management
82562GZ -> 10/100 support

ICH7 SMBALRT# signal reserve
a 0ohm resistor connect to S0 power
Must pull high to S0 power
for system power good

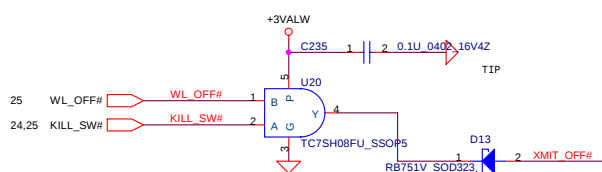
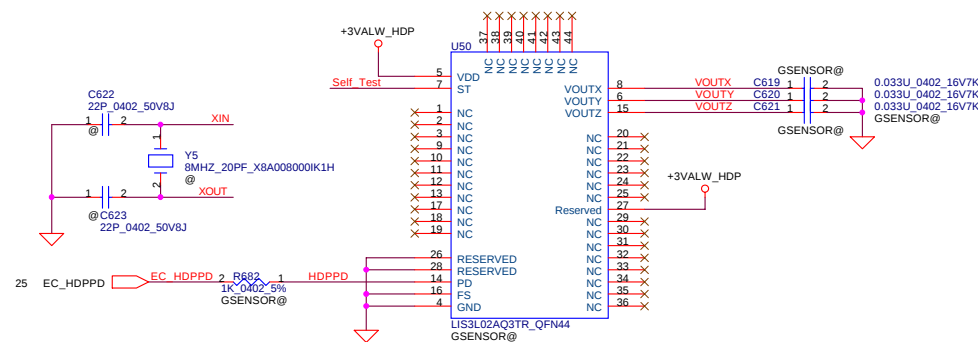


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								Intel 82573E/L and 82562GZ	
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Size		Document Number						Rev	
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Date:		Thursday, September 15, 2005				Sheet		26 of 48	

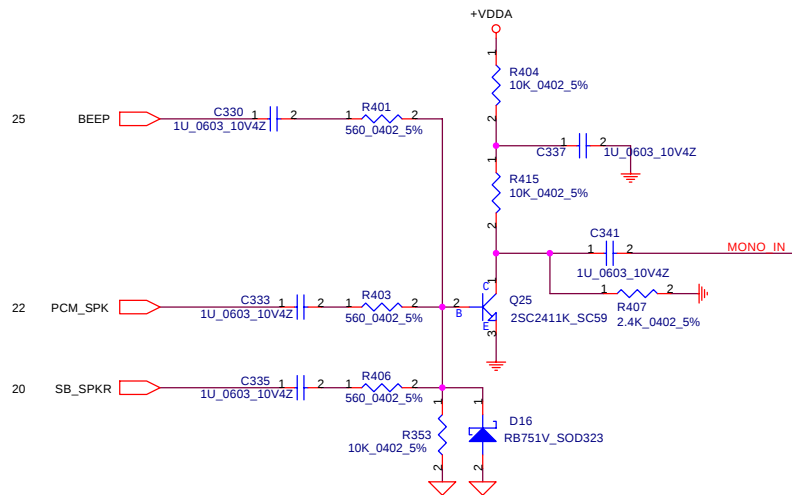


82562GZ Hardware configuration table (Default Mode 1)

Mode	TESTEN	ISOL_TCK	ISOL_TI	ISOL_EXEC	Mode	TESTEN	ISOL_TCK	ISOL_TI	ISOL_EXEC
Mode0	0	0	0	0	XOR tree	1	0	0	0
Mode1	0	0	1	1	Mode2	1	0	0	1
Test Mode	1	0	1	0	Mode3	1	0	1	1
Isolate	0	1	1	1	Mode4	1	1	0	0
Power down	1	1	1	1	Reserved	1	1	0	1
					Testing	1	1	1	0

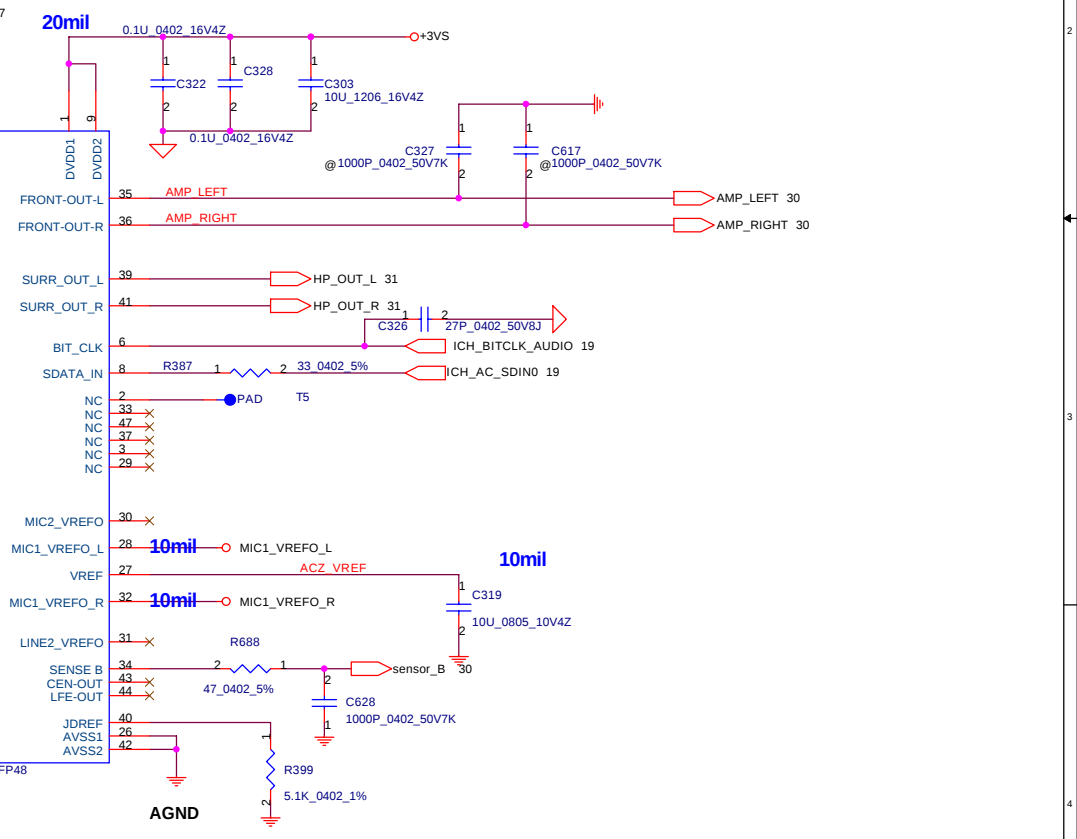
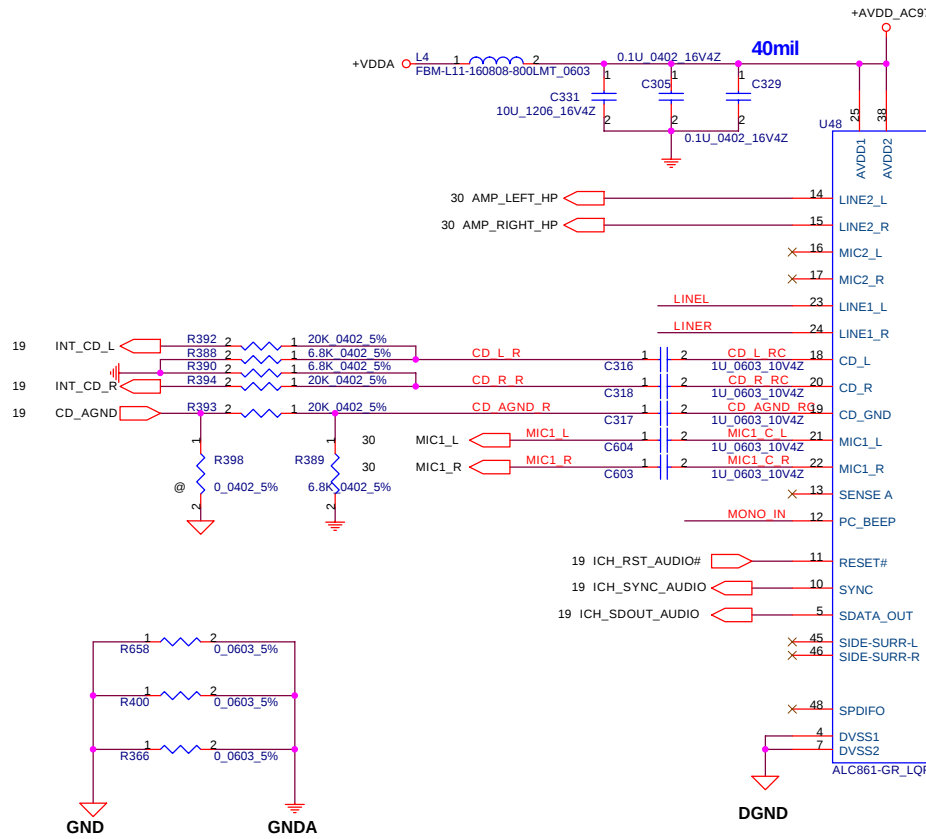
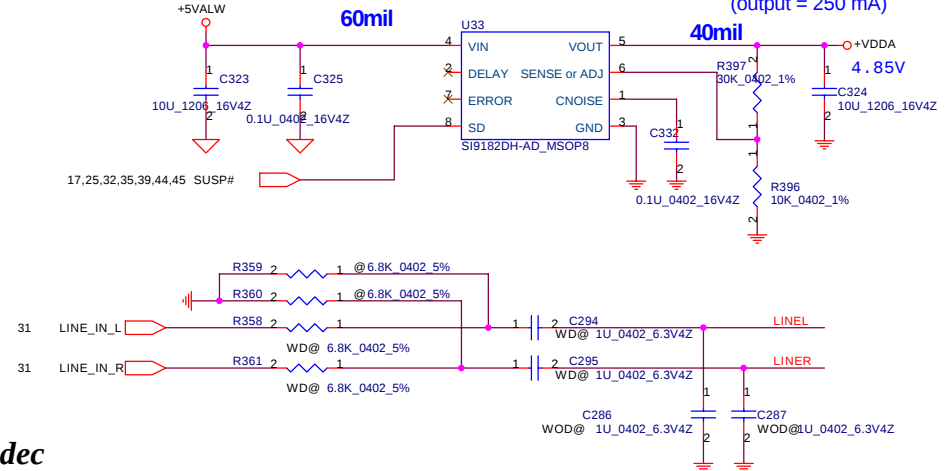


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					LA-3011P	0.
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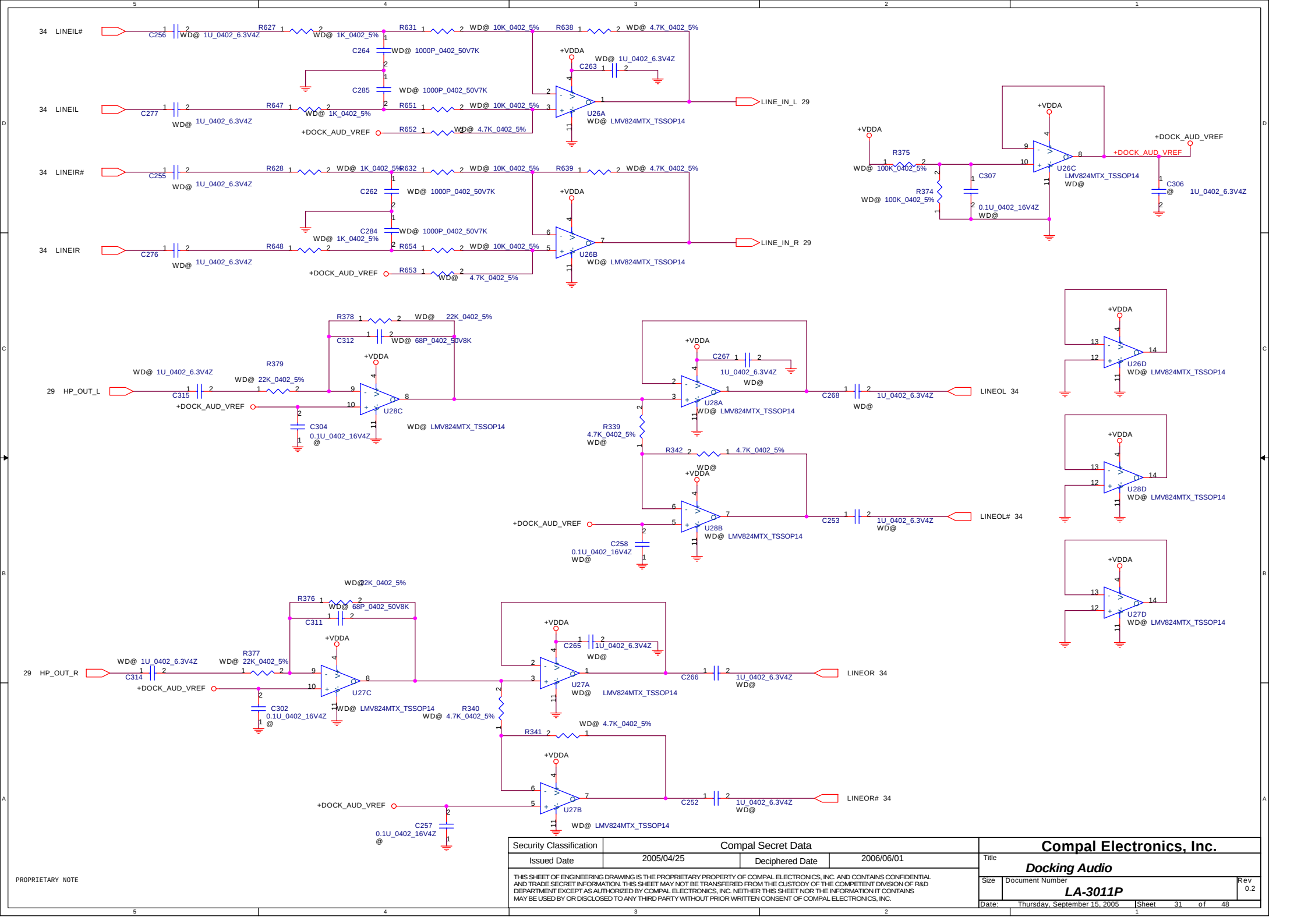


HD Audio Codec

28.7K for Module Design (VDDA = 4.702)
(output = 250 mA)
4.85V

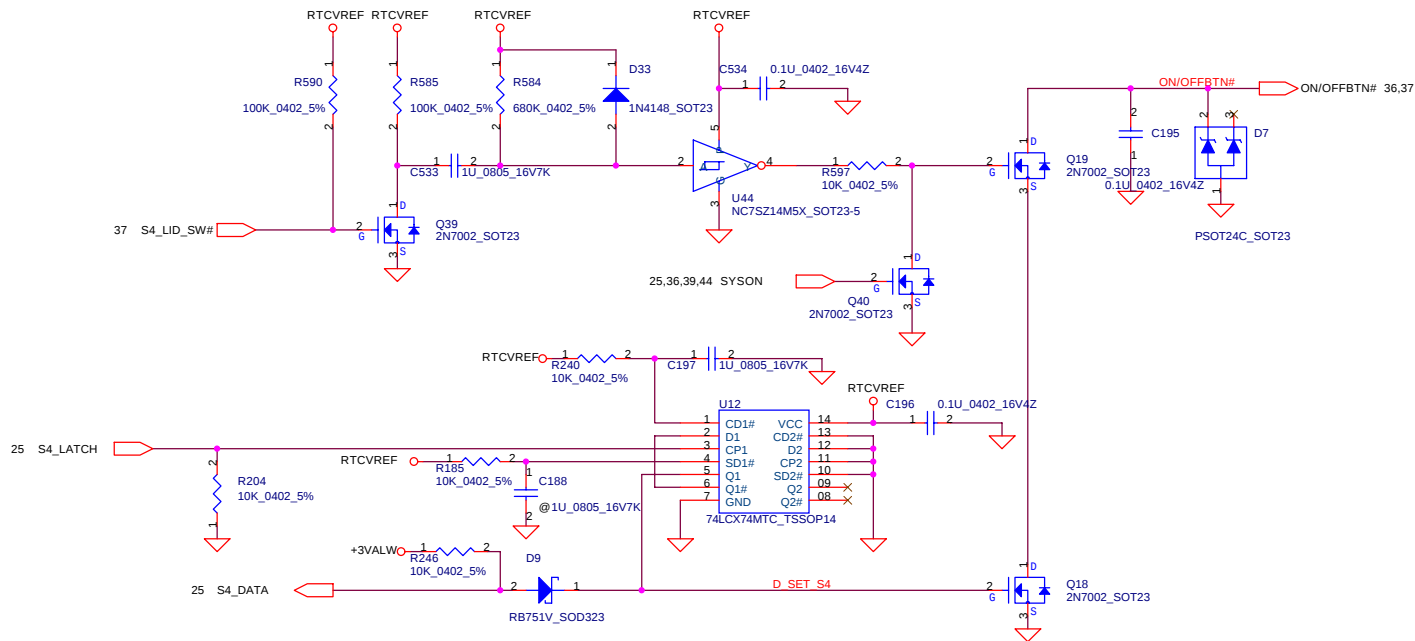


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Size	Document Number	Rev		0.2	
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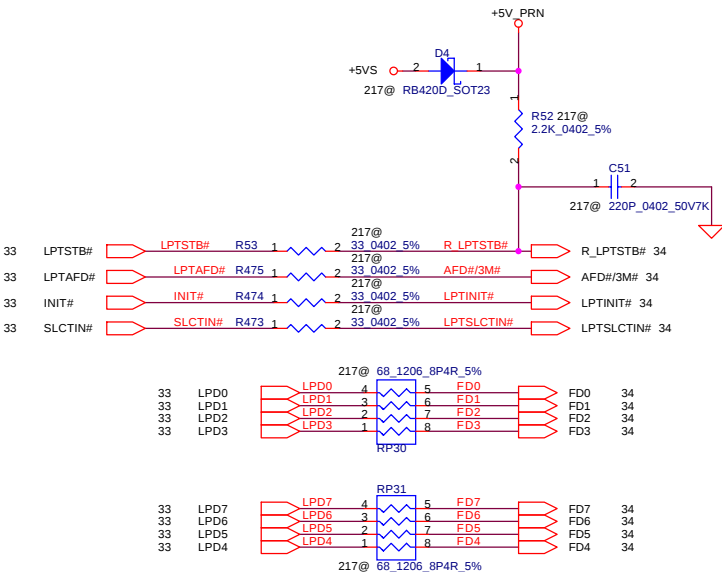


PROPRIETARY NOTE

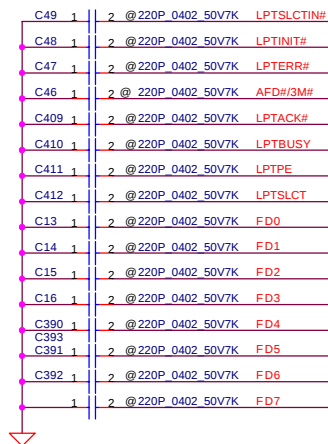
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					Rev 0.2



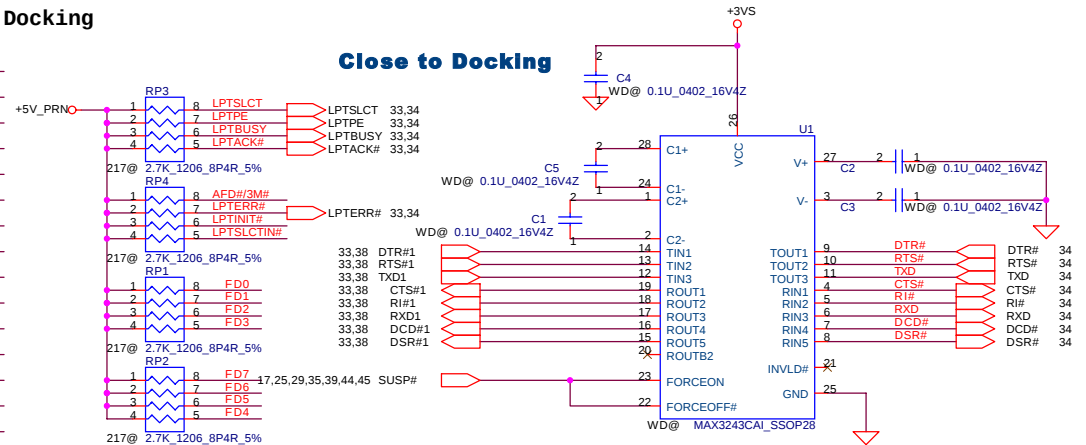
Docking Parallel Port



Close to Docking

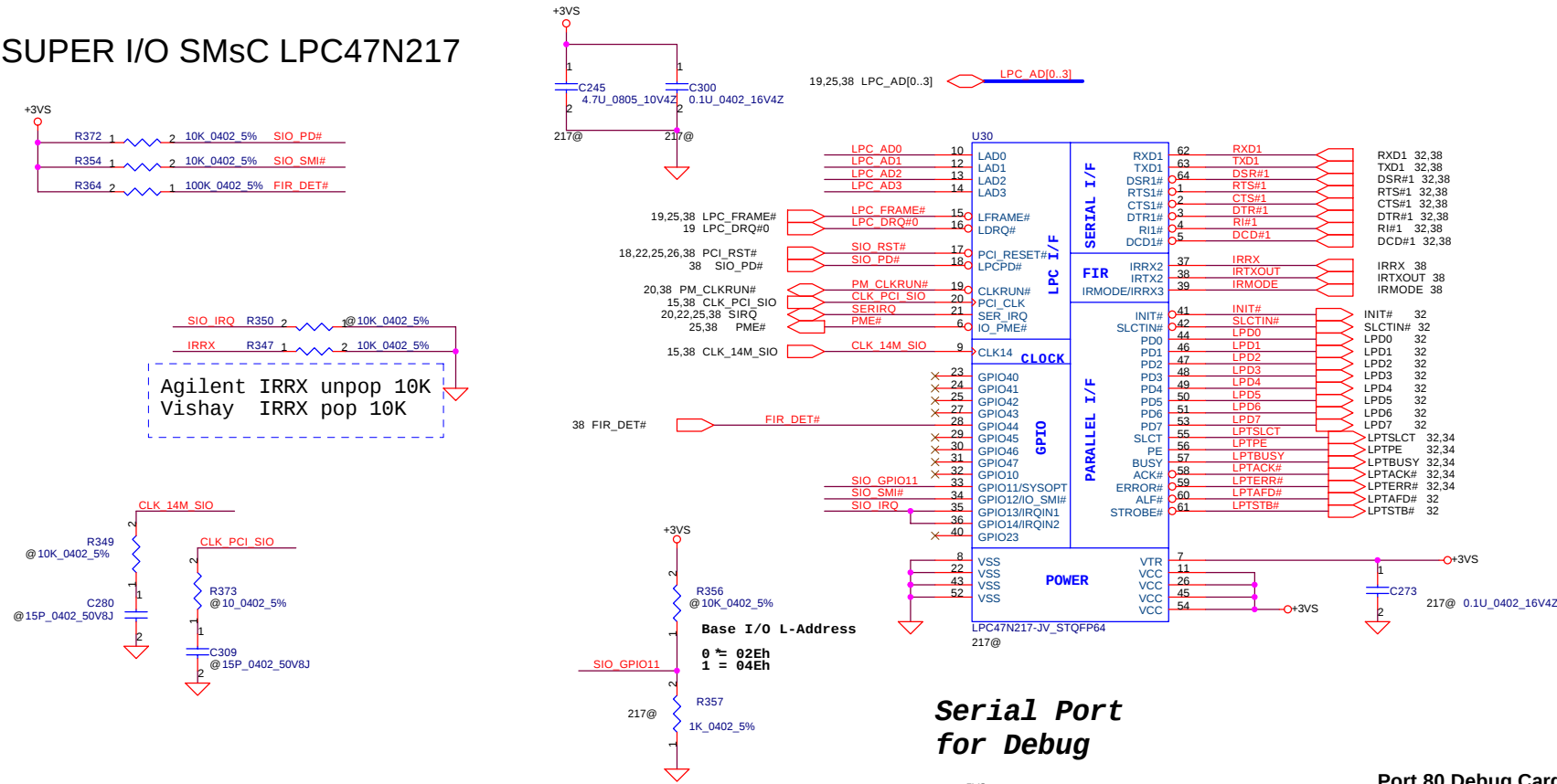


Close to Docking

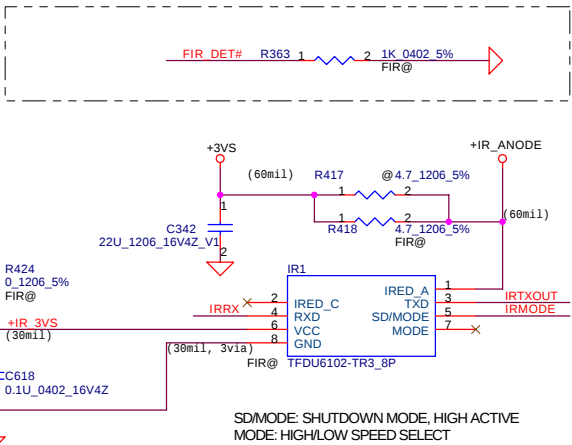


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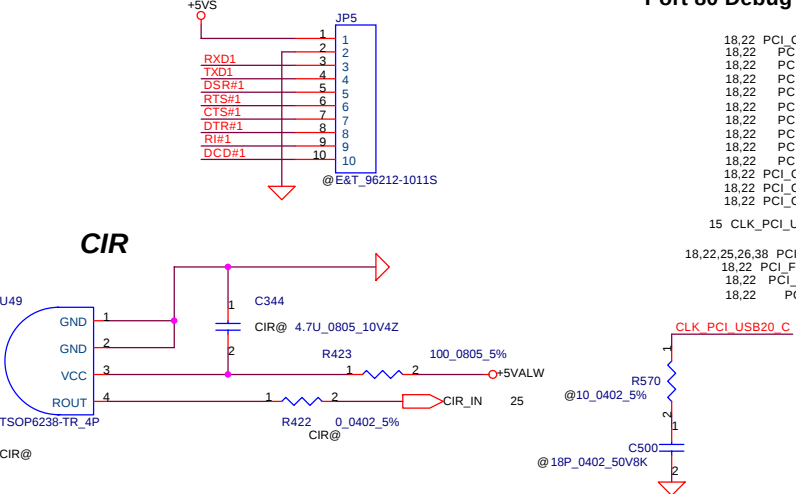
SUPER I/O SMC LPC47N217



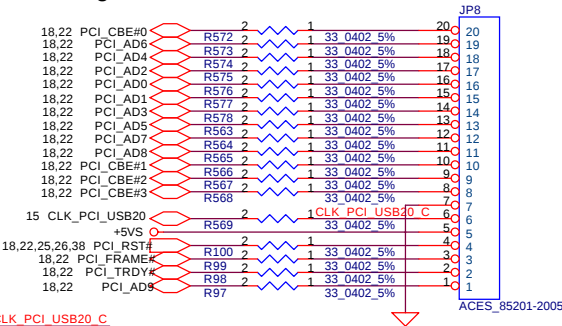
FIR Module L: R POP; FIR Enable H: R De-POP/FIR Disable



CIR

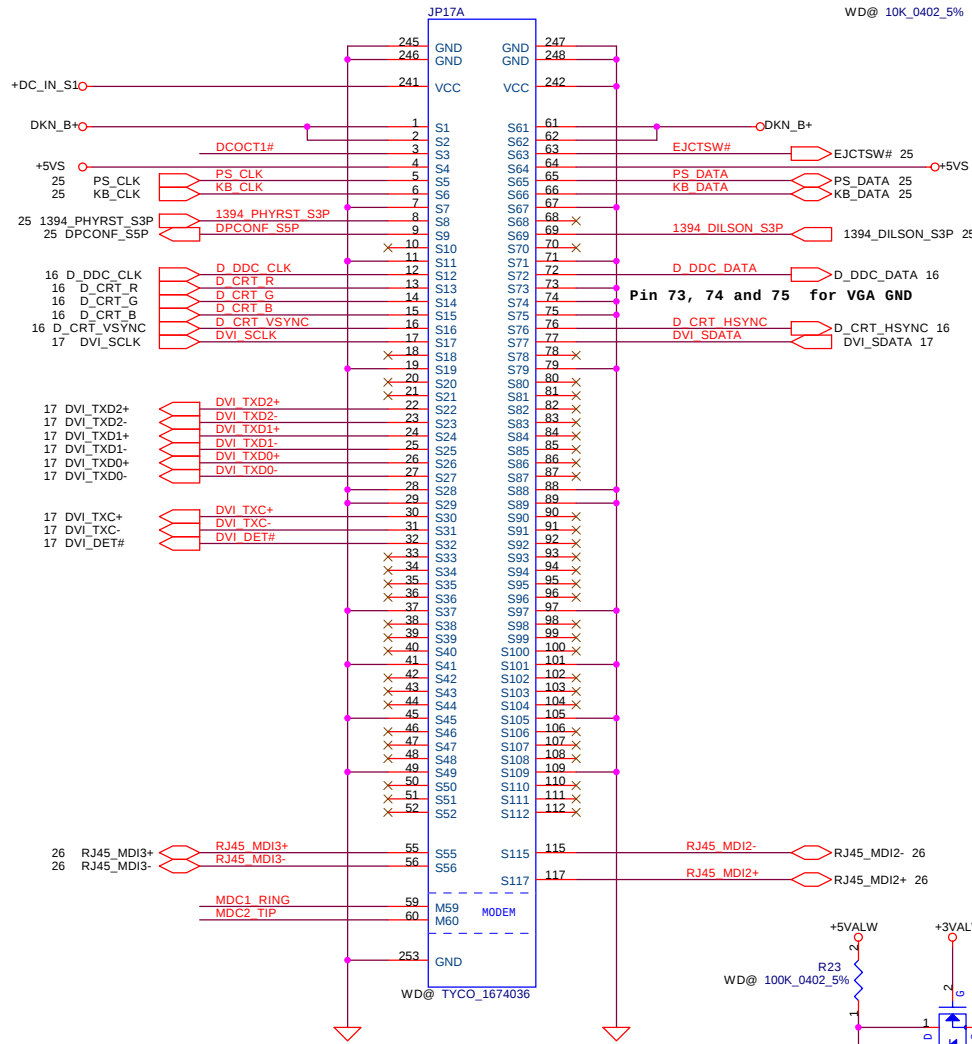


Port 80 Debug Card Connector

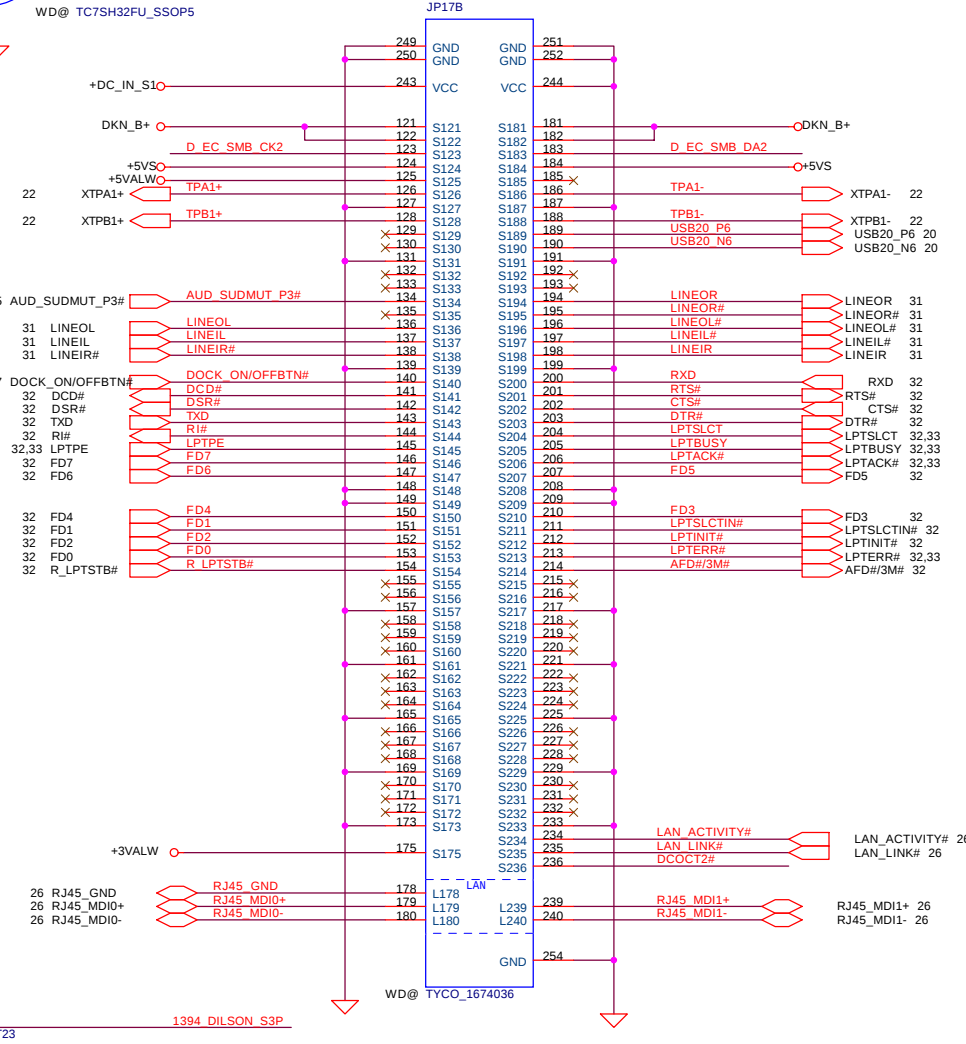
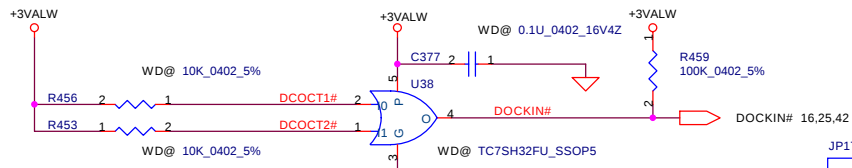
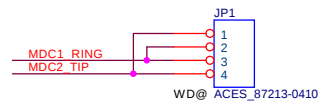


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Size		Document Number		Rev	
		LA-3011P		0.2	
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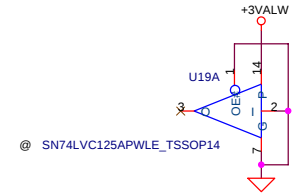
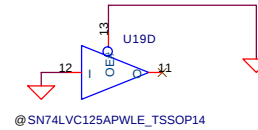
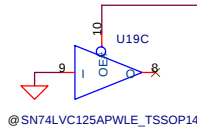
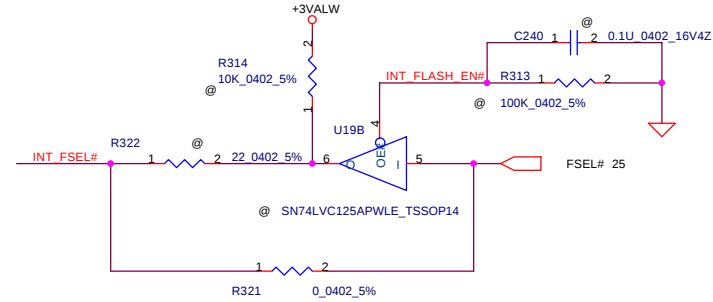
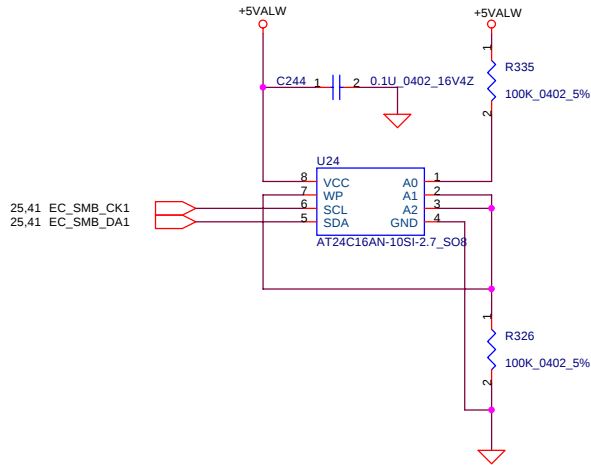
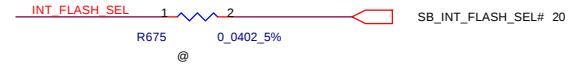
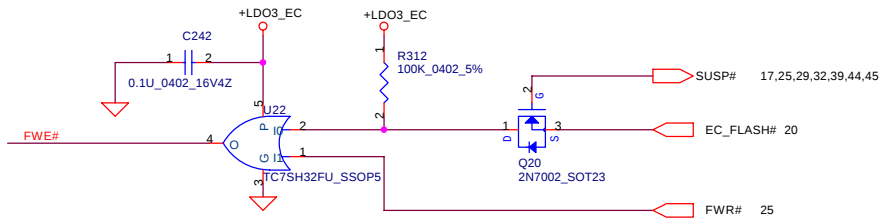
Docking Conn.



MDC to Docking Conn.



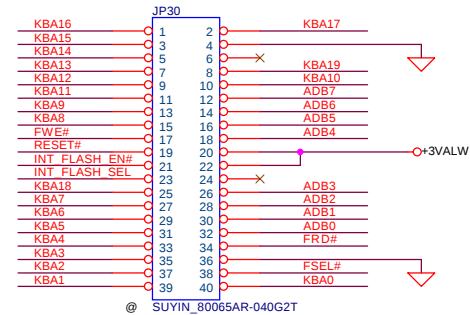
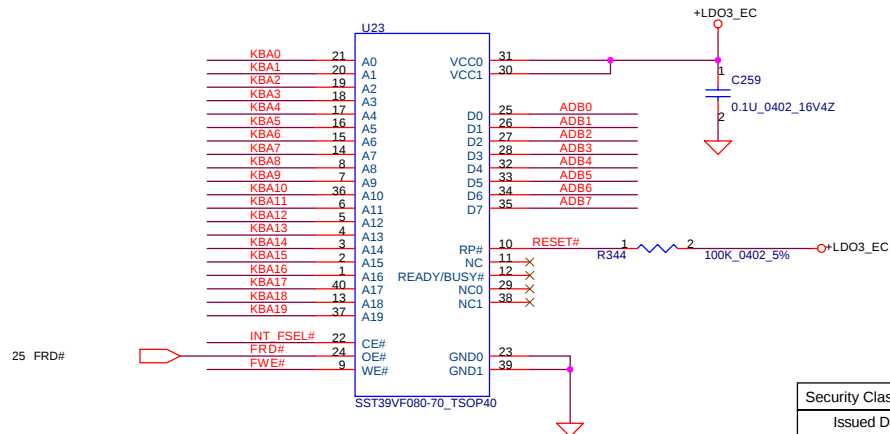
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								Size		Document Number		Rev	
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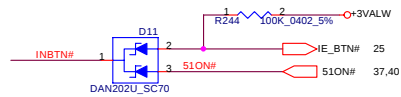
25 KBA[0..19] KBA[0..19]
25 ADB[0..7] ADB[0..7]

1MB ROM Socket

1MB Flash ROM

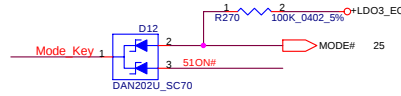


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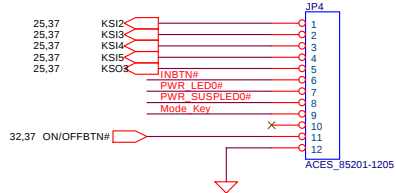


10C/106C: Green: SC591UYG000
10/10C: Blue: SC5191NB000

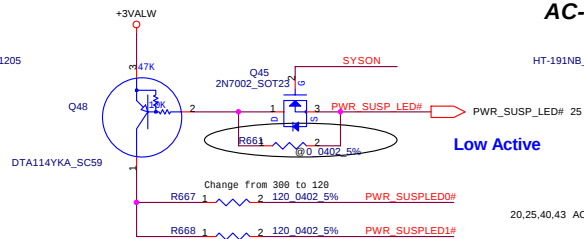
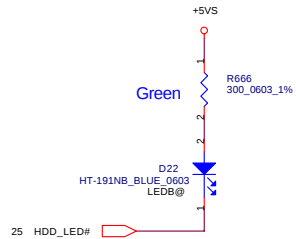
Vivace(SW-DJ) Button



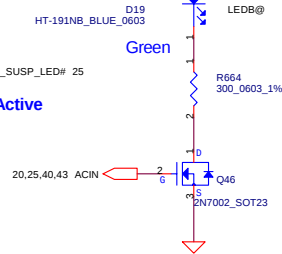
PWR BTN/B



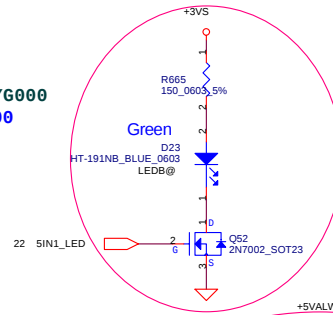
HDD LED



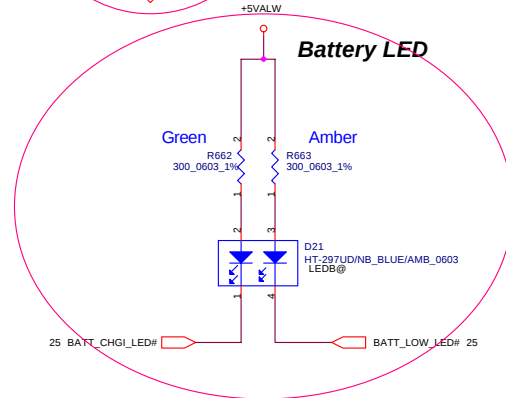
AC-IN LED



5 In 1 Card LED (Close to Socket)

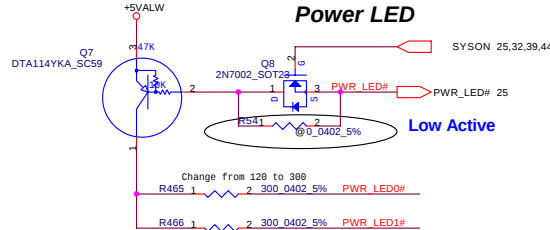


Battery LED

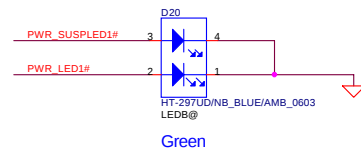


10/10C: Blue/Amber: SC597UDB000
10C/106C: Green/Amber: SC500001900

Power LED

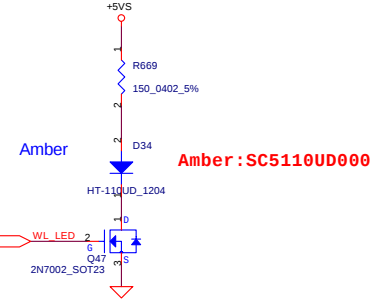


Amber



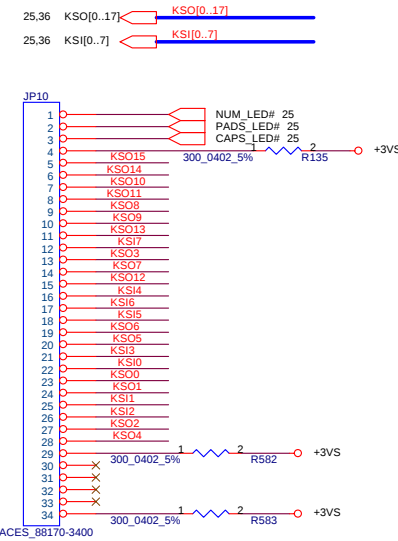
Green

Wireless Lan LED

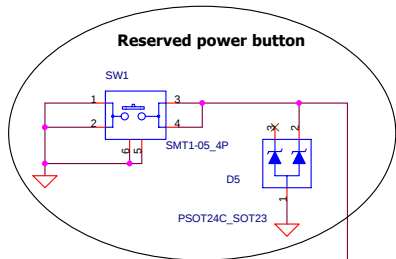
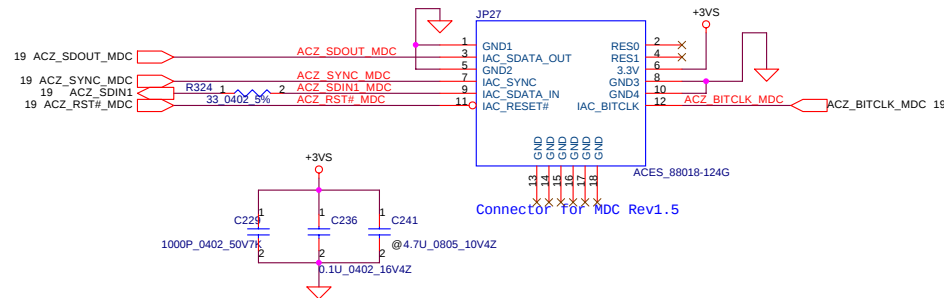


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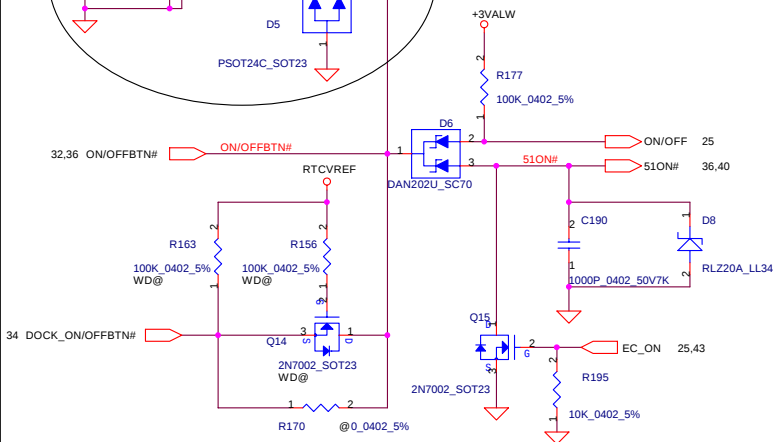
INT_KBD CONN.



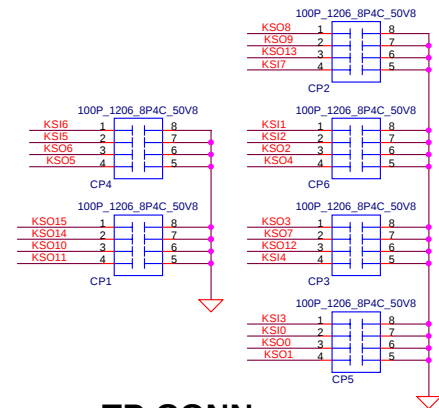
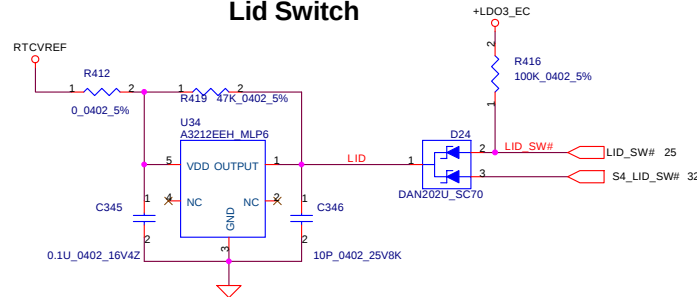
MDC 1.5 Conn.



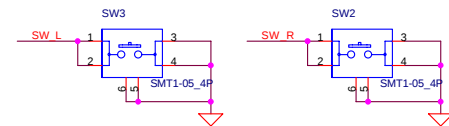
Power Button



Lid Switch



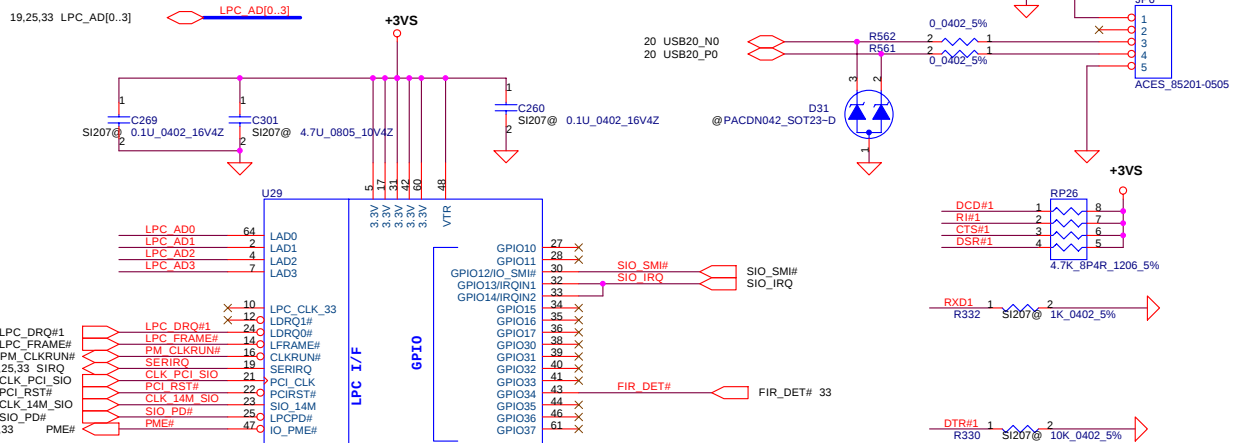
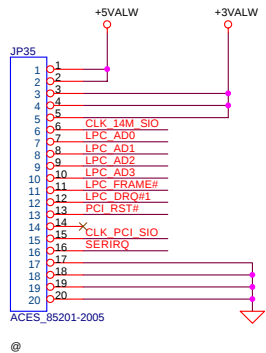
TP Button



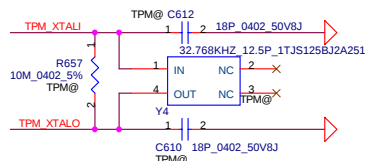
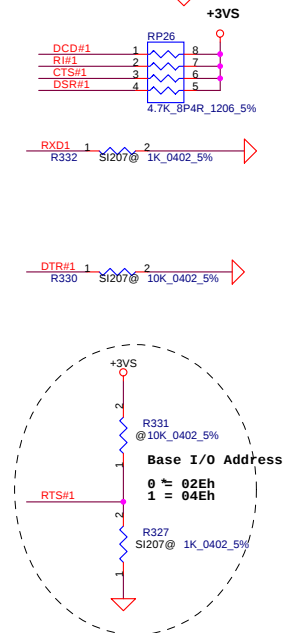
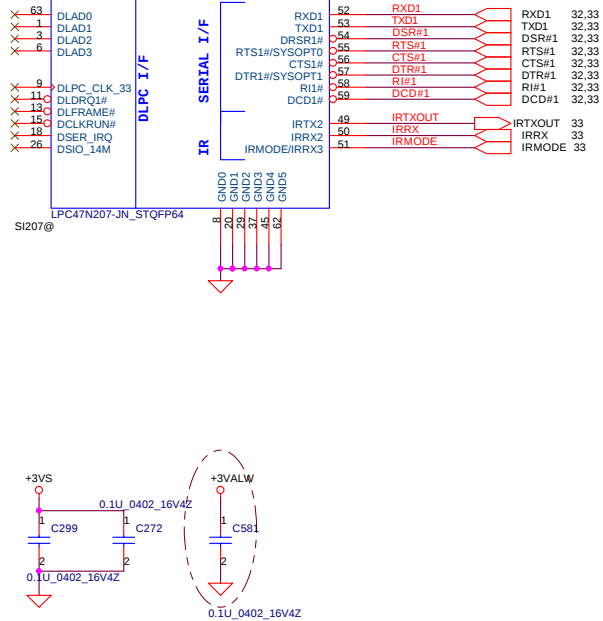
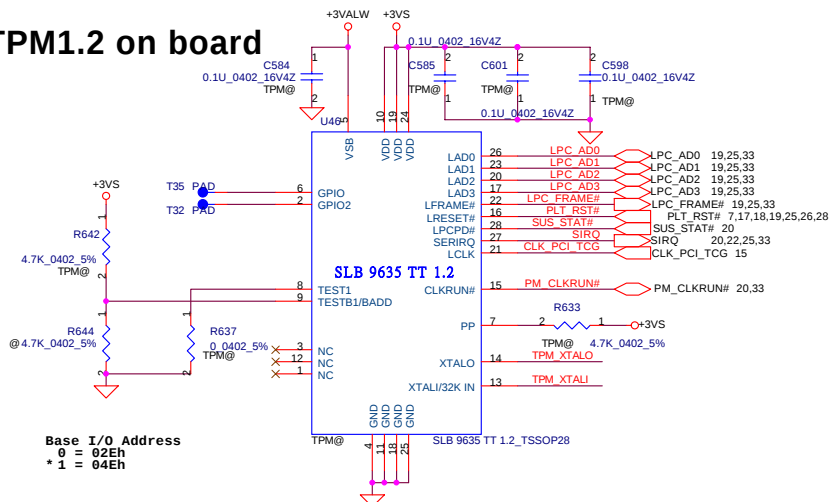
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Finger printer

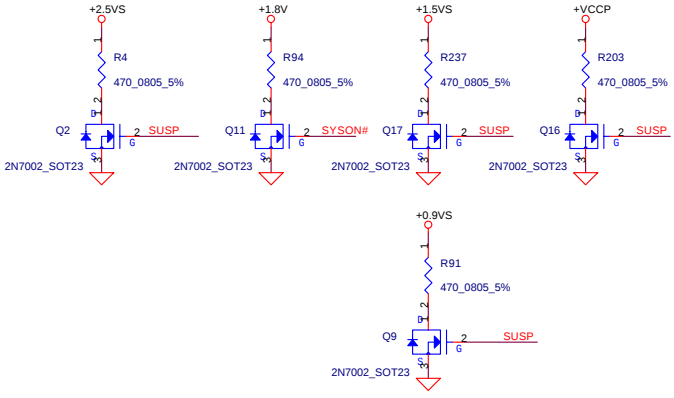
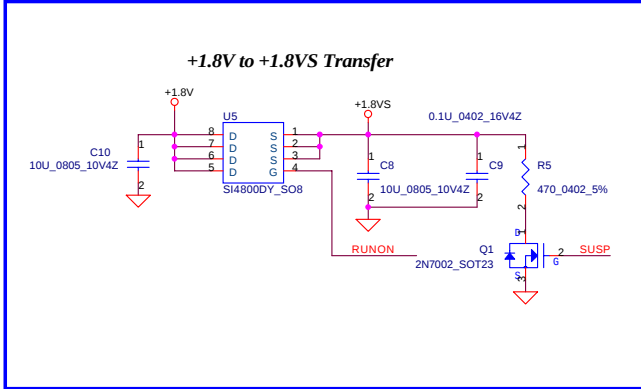
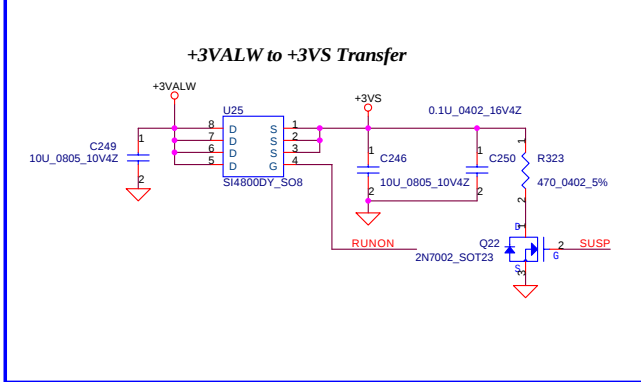
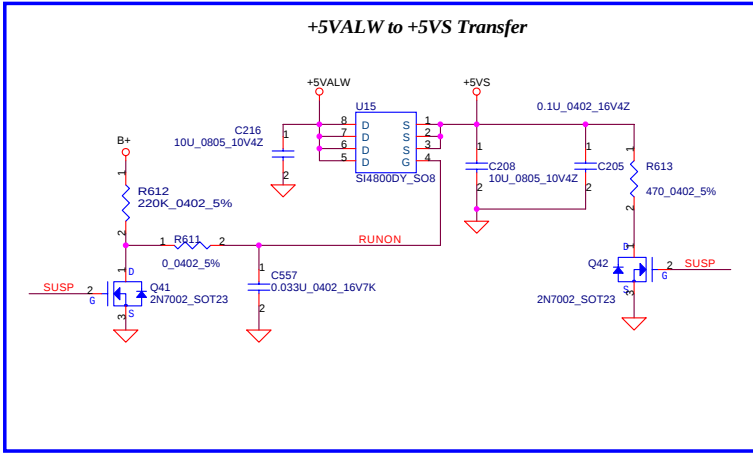
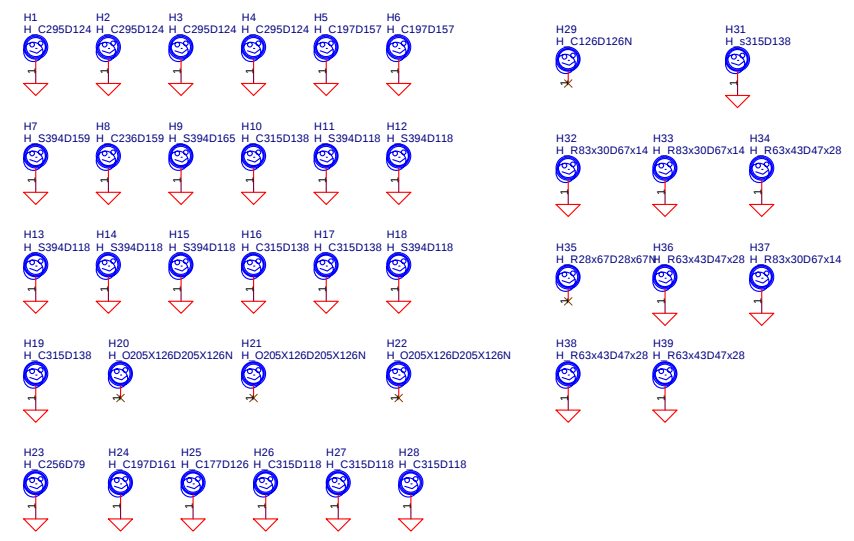
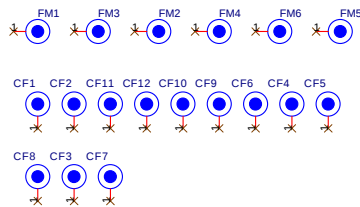
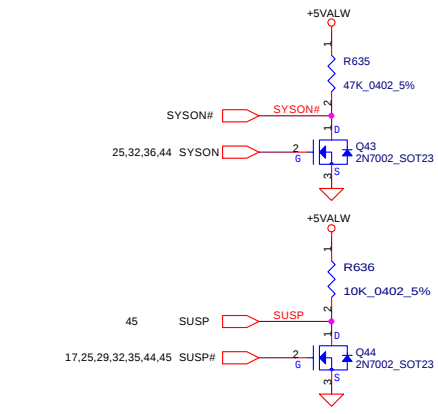
LPC Debug Port

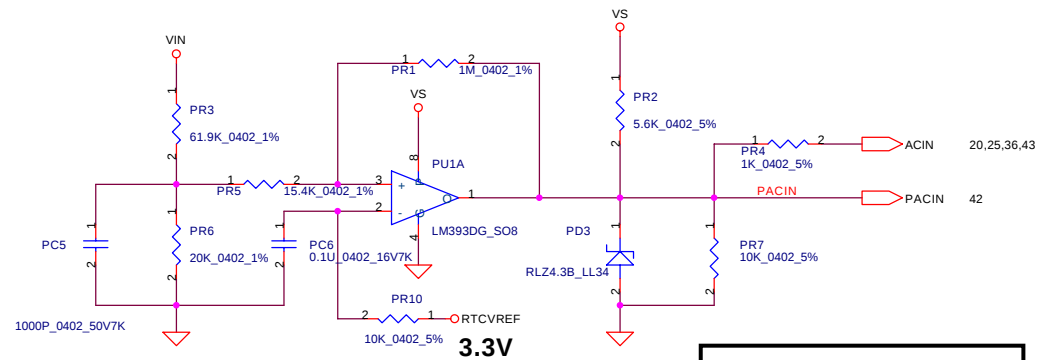
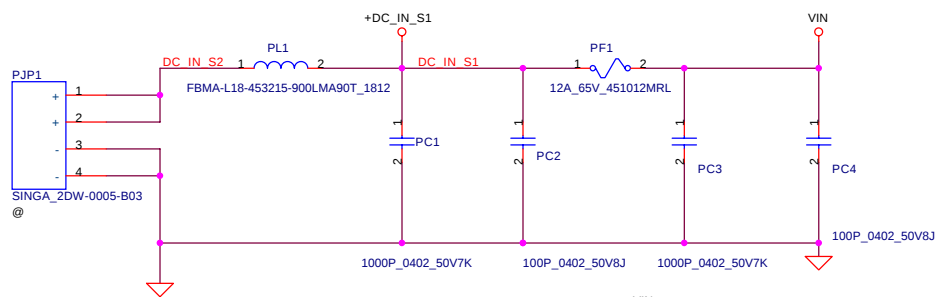


TPM1.2 on board



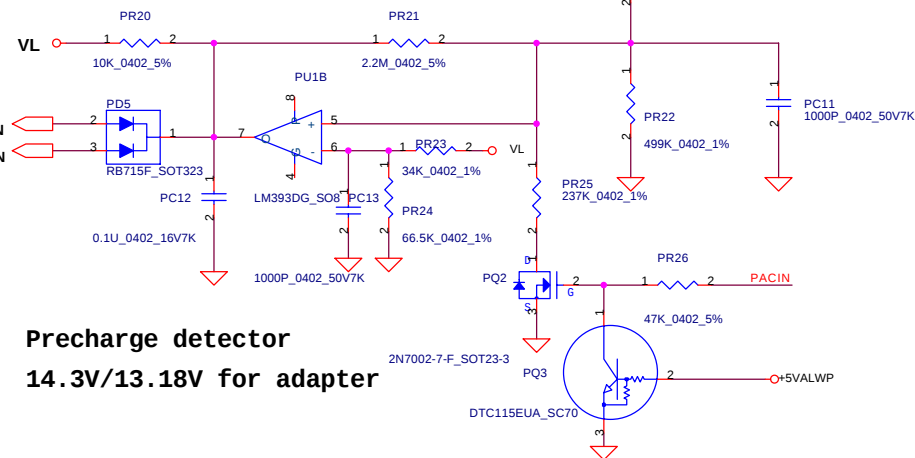
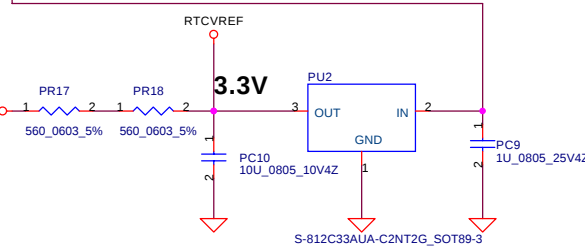
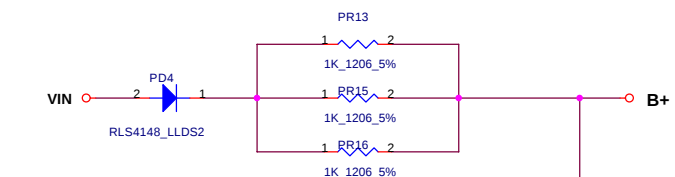
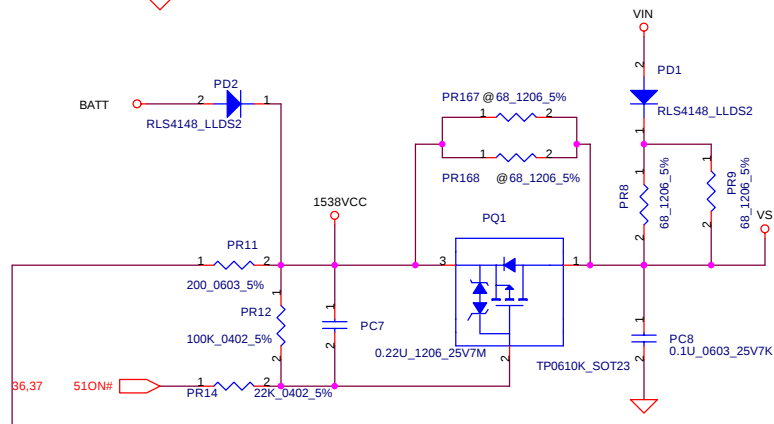
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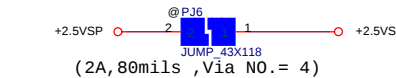
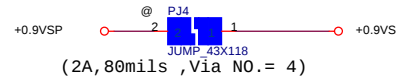
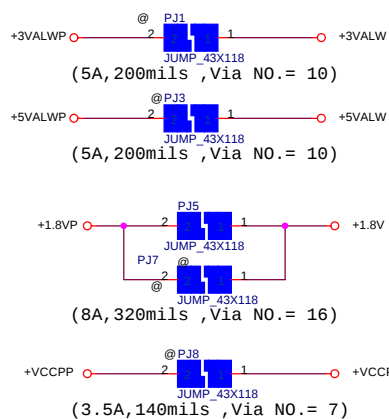


Vin Detector

High 14.57 14.01 13.46
Low 14.06 13.51 12.98

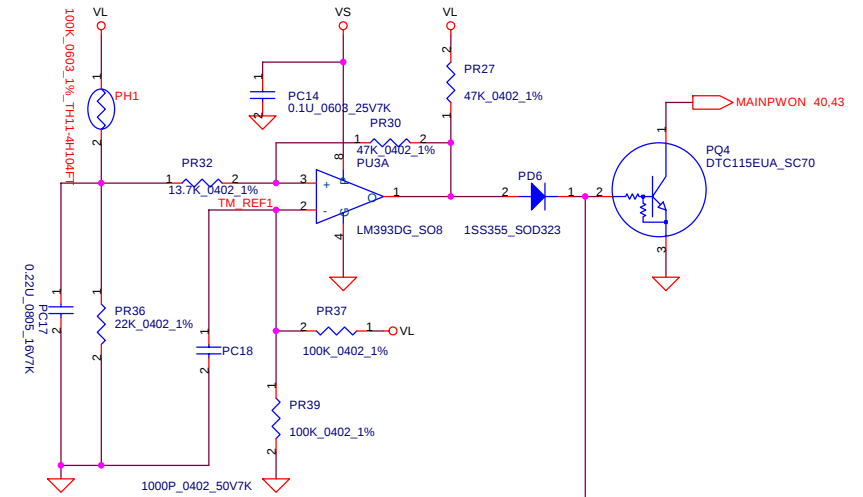
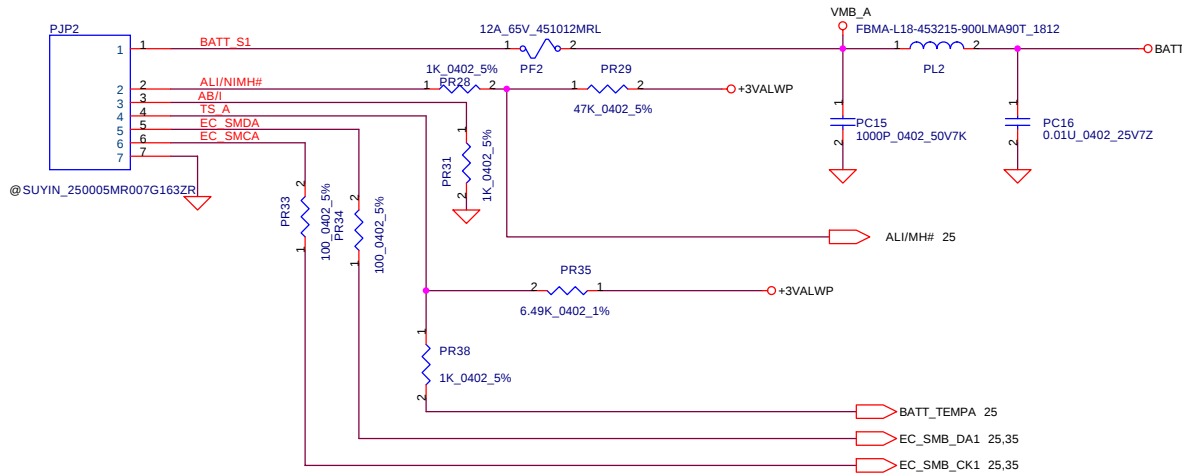


Precharge detector 14.3V/13.18V for adapter

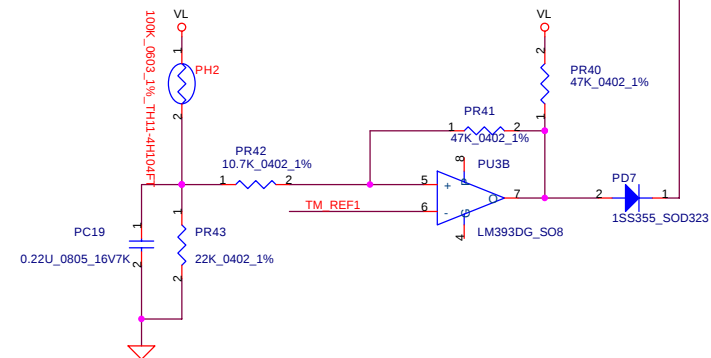


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Deciphered Date				2006/06/23				DCIN & DETECTOR			
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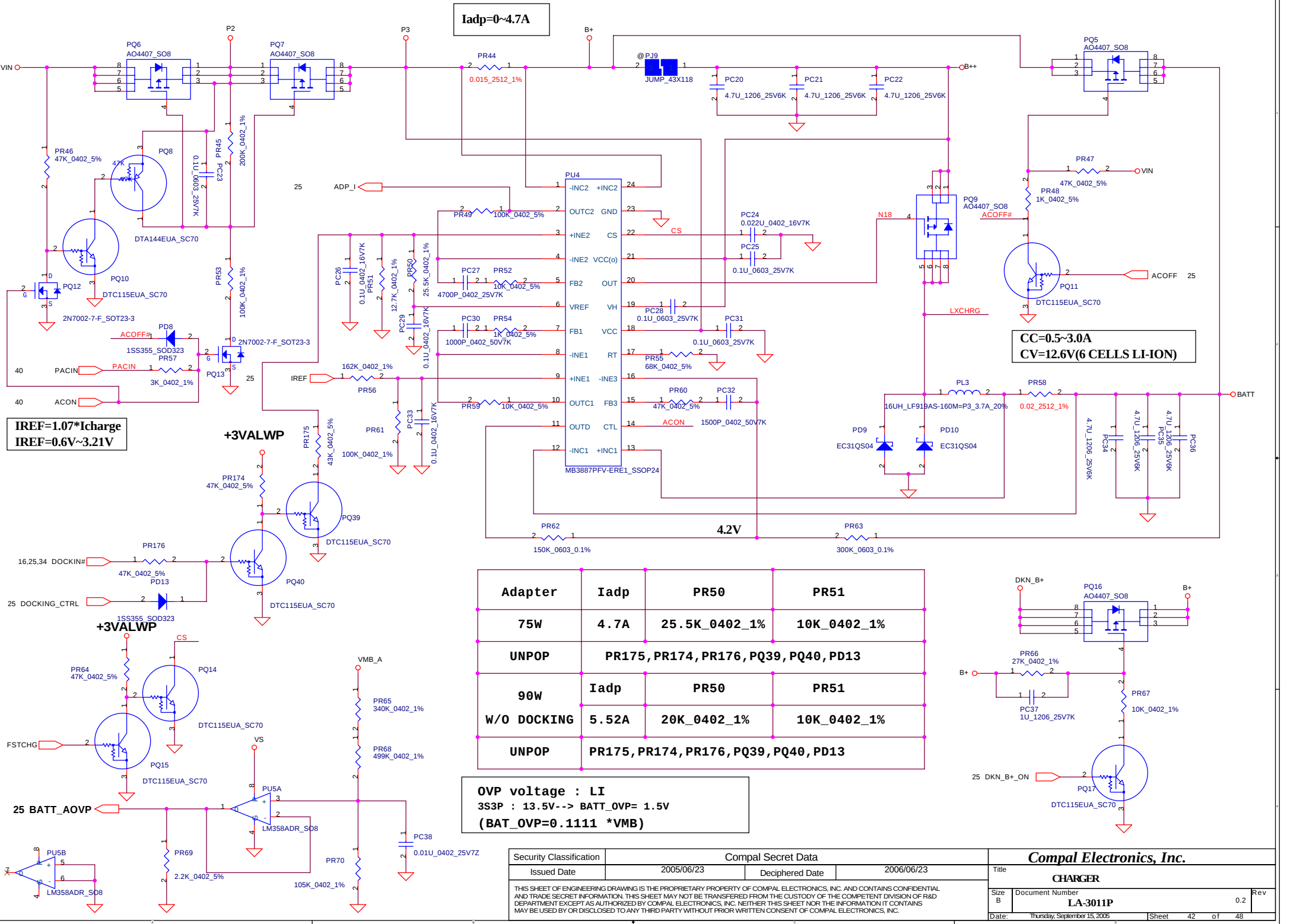
PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C



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Iadp=0~4.7A

IREF=1.07*Icharge
IREF=0.6V~3.21V

+3VALWP

CC=0.5~3.0A
CV=12.6V(6 CELLS LI-ION)

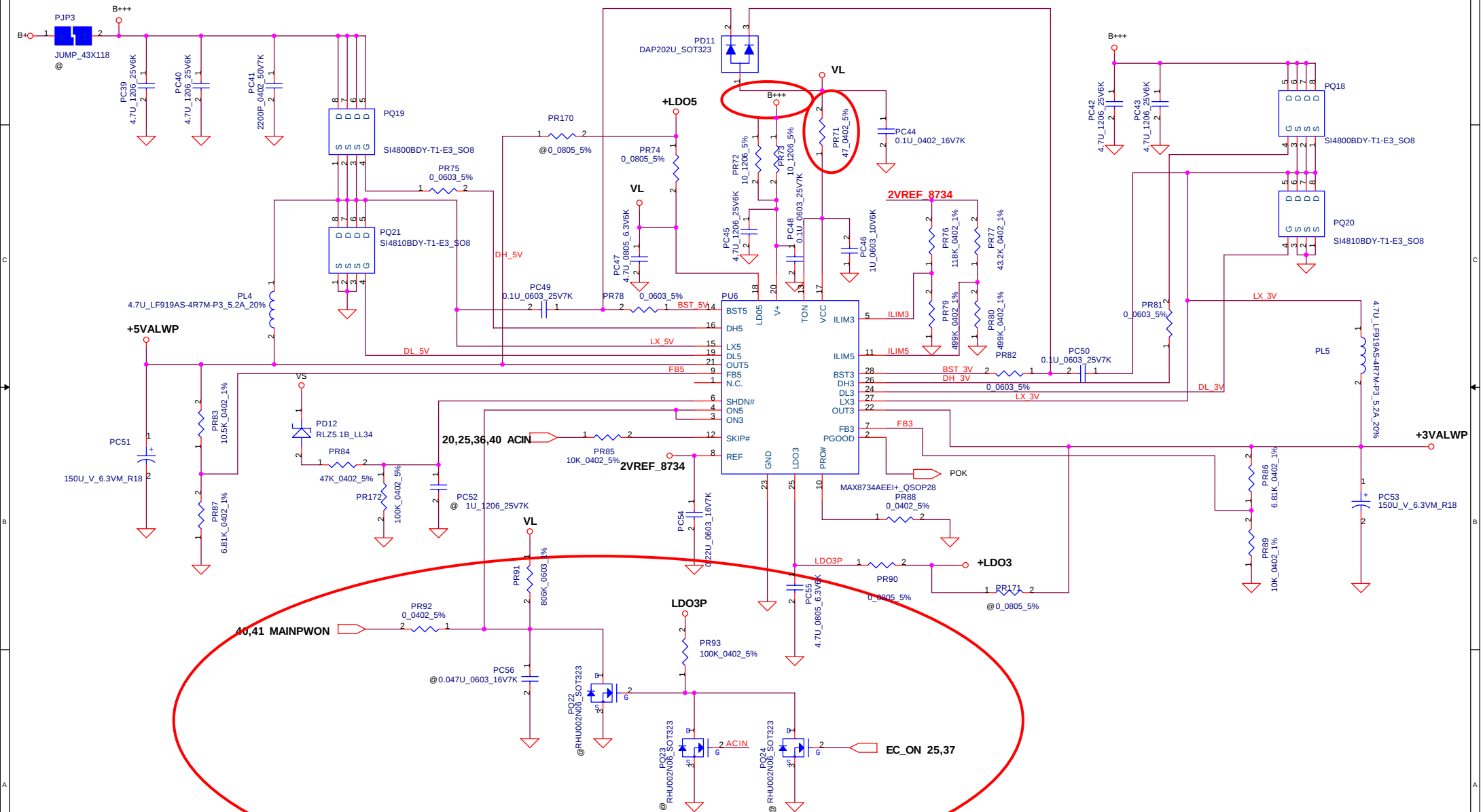
Adapter	Iadp	PR50	PR51
75W	4.7A	25.5K_0402_1%	10K_0402_1%
UNPOP		PR175, PR174, PR176, PQ39, PQ40, PD13	
90W	Iadp	PR50	PR51
W/O DOCKING	5.52A	20K_0402_1%	10K_0402_1%
UNPOP		PR175, PR174, PR176, PQ39, PQ40, PD13	

OVP voltage : LI
3S3P : 13.5V-> BATT_OVP= 1.5V
(BAT_OVP=0.1111 *VMB)

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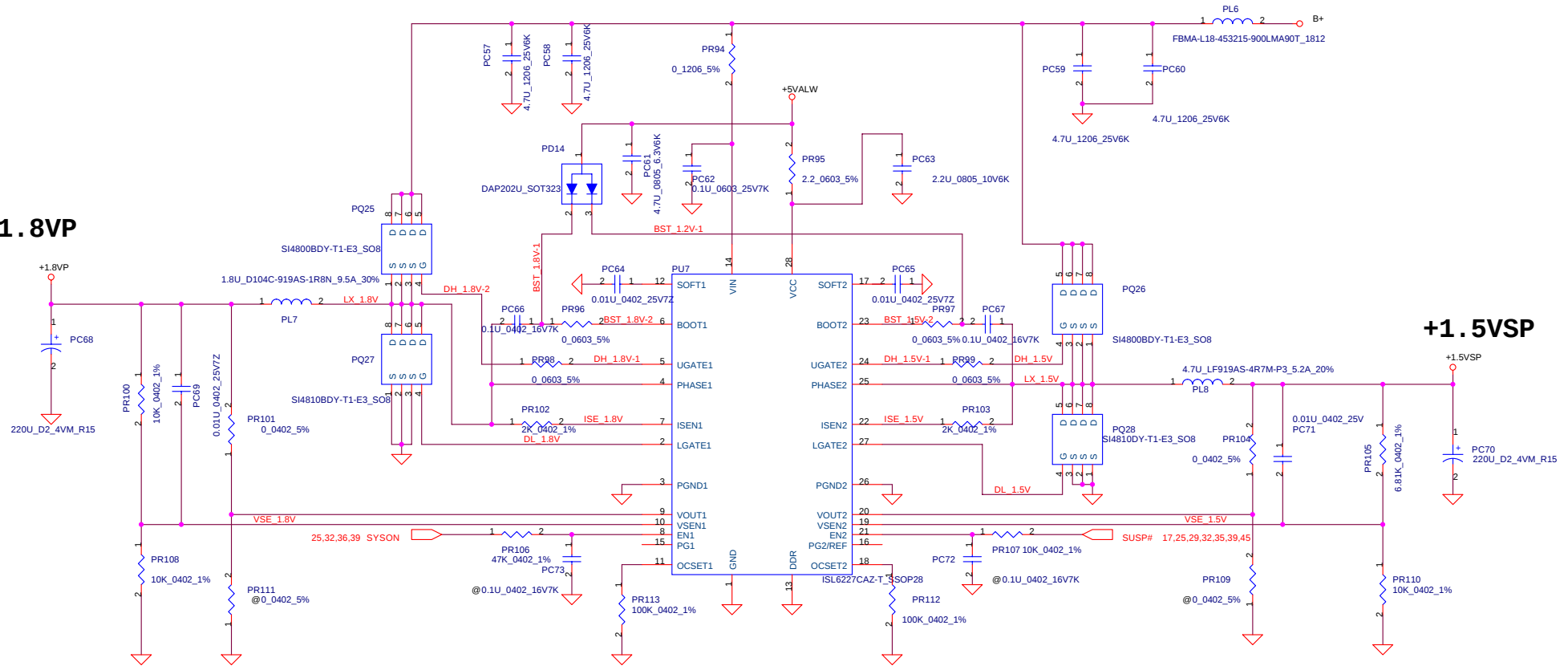
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CHARGER			
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	LA-3011P	0.2	
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+3.3VALWP/+5VALWP



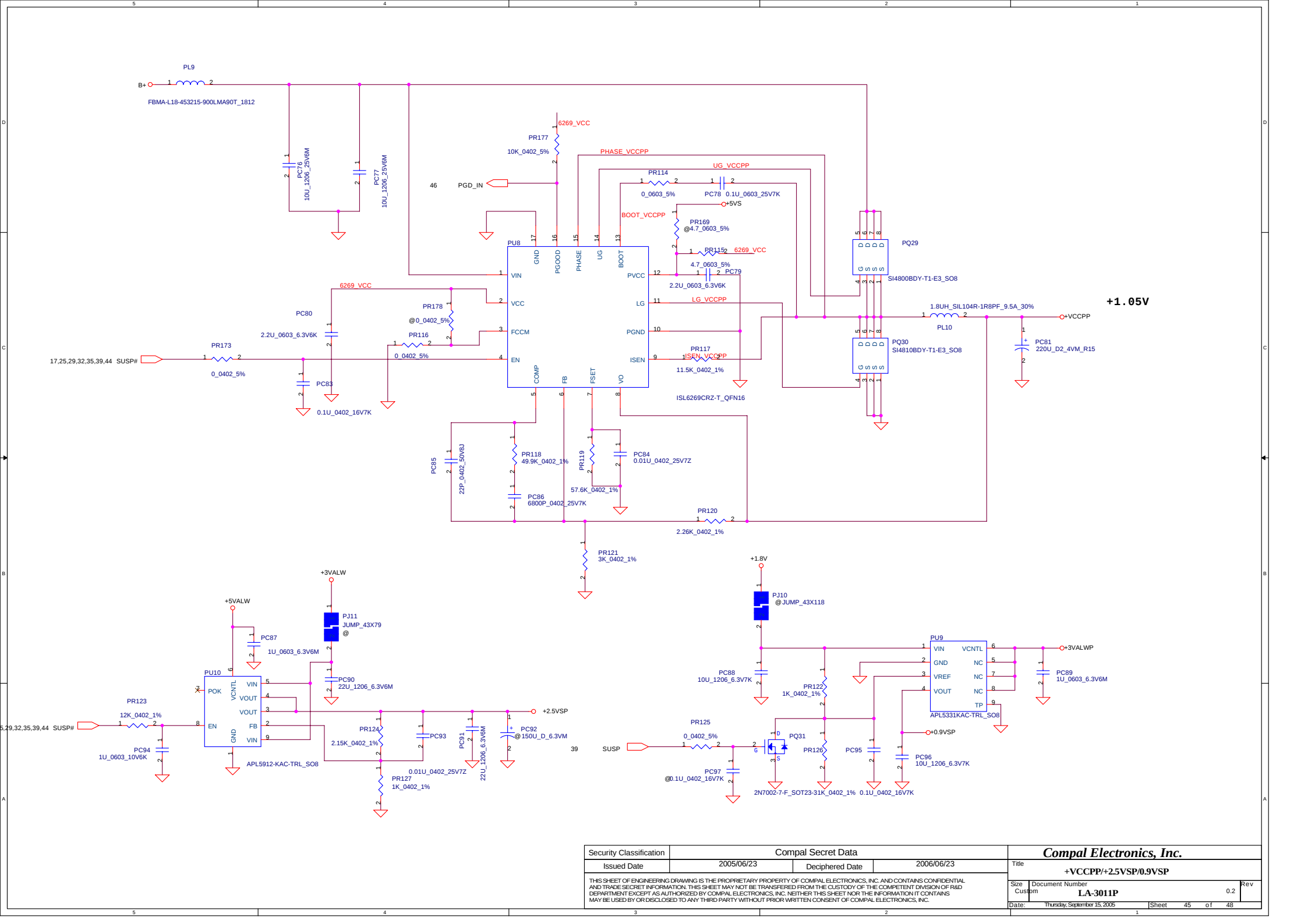
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+1.8VP



+1.5VSP

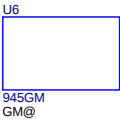
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								Size		Document Number		0.2		Rev	
								Custom		LA-3011P					
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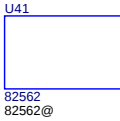
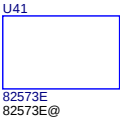
NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
8/8		P.15	Delete R589,R181,R190	No reserve those resistors
8/10		P.30	Add D35,R671	for G_beep function
8/10		P.25	Swap EC pin8 and Pin42	for G_beep function
8/11		P.30	Del R659,C613& Add D36	for G_beep function
8/16		P.7	unmount R503, R519	Intel Request
8/16		P.9	unmount R480, R478	Intel Request
8/16		P.11	unmount R514	Intel Request
8/16		P.20	Mount R249, Add R672,R673,R674	Intel Request
8/19		P.35	Add R675	For BIOS debug port
8/19		P.39	Modify R611, C557	For RUNON timing sequence
8/22		P.7	Add R676	Reserve for TS on SODIMM
8/22		P.28	Del U10,R128,R134,C162,C164,C169,C174,C175	Change G-sensor
8/23		P.28	Add C619,C620,C621,C622,C623,C624,C625,C626,C627	
8/23		P.28	Add R677,R678,R679,R680,R681,R682,R683,R684,R685,R686	
8/23		P.28	Del x_sensor, y_sensor, z_sensor connection to EC	G-sensor circuit modification
8/23		P.28	Add Q49,Q50,U50,U51,U52,Y5	For New G-sensor solution
8/24		P.17	Change JP18.40 to +5VALW	
8/24		P.29	Change U33.8 to SUSP#	
8/24		P.29	Change U33.8 to SUSP#	
8/25		P.16	Change D27,D28,D29 pin 3 to +2.5VS	for Intel's suggestion
8/25		P.37	Change JP9 connector to 6pin	To meet ME's definition
8/25		P.15	J10 change to Jump 43*79	for DFX request
8/25		P.19	CMOS_CLR1 change to Jump 43*79	for DFX request
8/30		P.39	Modify Screw holw location	
8/30		P.22	To correct MSBS_SDCMD_SMWE#/SDWPP#_SMCE# signals	
8/30		P.39	Change R612=220K,C557=0.033uF,R611=0ohm	for power on sequence
9/2		P.29	Add EC_HDPPD to U14.24 and R682	G-sensor circuit modification
9/5		P.09	Swap CRT_R & CRT_B	To fix CRT issue of GM
9/8		P.20	Change LAN_Disable from GPIO15 to GPIO28	
9/9		P.26	Swap RX /TX signals	
9/9		P.25	Swap EC pin8 & Pin42	for follow EVT pin definition
9/9		P.29/30	To separate Line out and HP signals	
9/12		P.30	D35/D36 change to Diode 4148	
9/12		P.30	Add R687 ,Q51	
9/12		P.29	Add R688,C628	
9/12		P.24	Change JP34 connector to ACES_87213-1000	
9/12		P.29	Delete R395	
9/12		P.16	Change F1 to SP04301P000	
9/13		P.38	Reserve SIO_SMI#/SIO_IRQ signals	
9/13		P.38	Reserve JP35 for BIOS debug	
9/14		P.22	Add Q52 for 5in1 LED	

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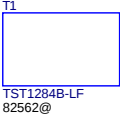
NB



LAN



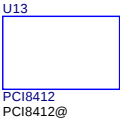
TRANSFORMER



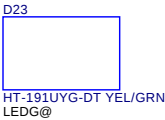
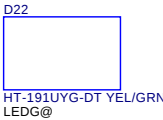
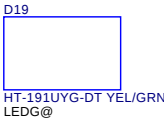
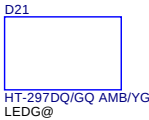
PCB



CARDBUS



Green LED



CAP for LAN

