# Compal confidential

## Schematics Document
## Mobile Yonah uFCPGA with Intel
## Calistoga_PM+ICH7-M core logic
## 2005-08-26
## REV:0.2

| | | | |
|---|---|---|---|
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| | | |
|---|---|---|
| *Compal Electronics, Inc.* | | |
| Title: *Cover Sheet* | | |
| Size: Custom | Document Number: *LA-3011P* | Rev: 0.2 |
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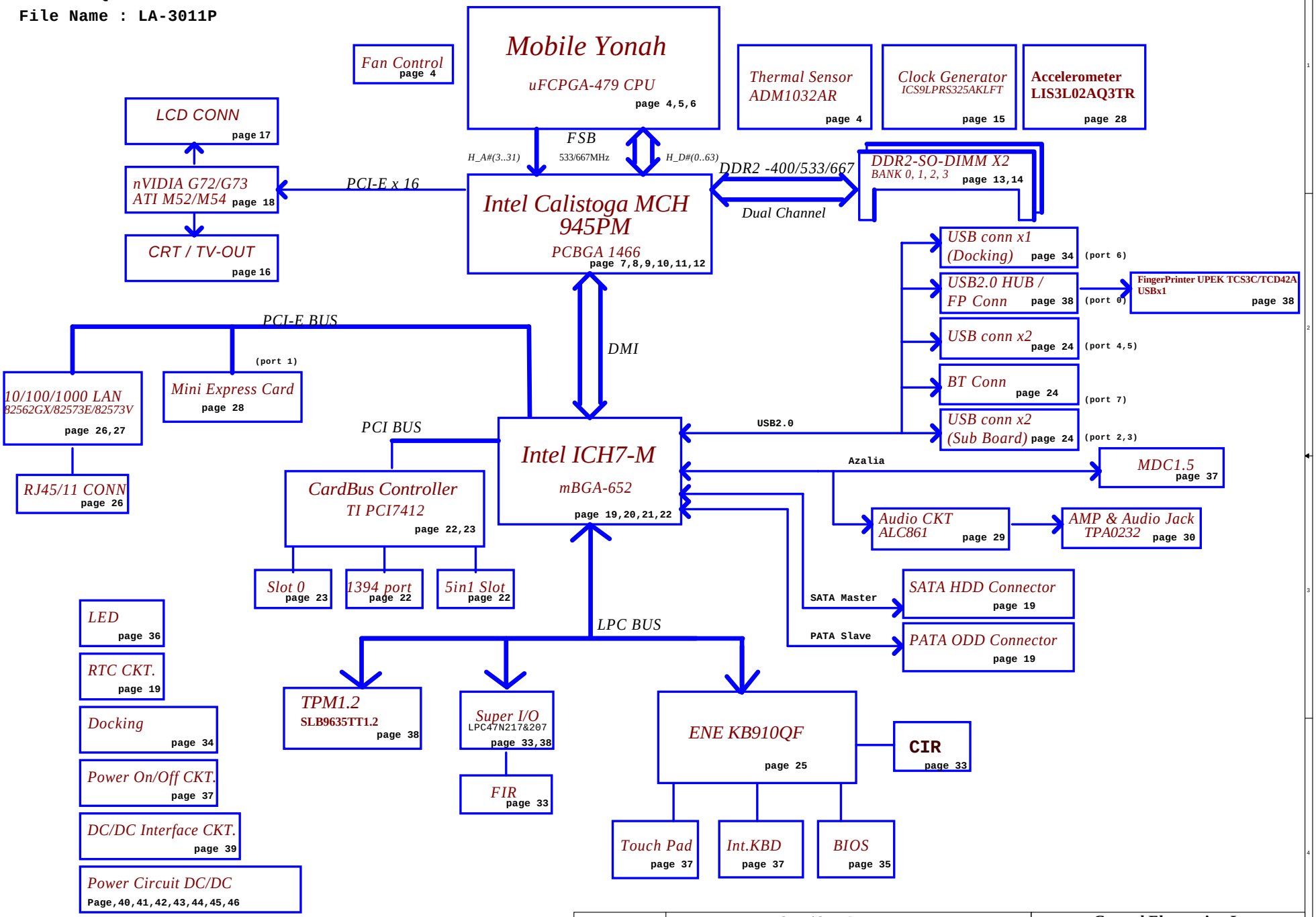
Model:HAQAA

File Name : LA-3011P

# NAPA

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Title: **Block Diagram**

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## Voltage Rails

| Power Plane | Description | S0-S1 | S3 | S5 |
|---|---|---|---|---|
| VIN | Adapter power supply (18.5V) | N/A | N/A | N/A |
| B+ | AC or battery power rail for power circuit | N/A | N/A | N/A |
| +CPU_CORE | Core voltage for CPU | ON | OFF | OFF |
| +VCCP | 1.05V power rail for Processor I/O and MCH/ICH core power | ON | OFF | OFF |
| +0.9VS | 0.9V switched power rail for DDRII Vtt | ON | OFF | OFF |
| +1.5VS | 1.5V switched power rail for PCI-E interface | ON | OFF | OFF |
| +1.8V | 1.8V power rail for DDRII | ON | ON | OFF |
| +1.8VS | 1.8V switched power rail | ON | OFF | OFF |
| +2.5VS | 2.5V switched power rail for MCH video PLL | ON | OFF | OFF |
| +2.5VALW | 3.3V always on power rail | ON | ON | ON* |
| +3VALW | 3.3V always on power rail | ON | ON | ON* |
| +3VS | 3.3V switched power rail | ON | OFF | OFF |
| +5VALW | 5V always on power rail | ON | ON | ON* |
| +5VS | 5V switched power rail | ON | OFF | OFF |
| +RTC_VCC | RTC power | ON | ON | ON |

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

## Internal PCI Devices

| DEVICE | Bus | PCI Device ID | IDSEL # |
|---|---|---|---|
| LAN | 1 | D8 | AD24 |
| Azalia | 0 | D27 | AD11 |
| PCI-E | 0 | D28 | AD12 |
| USB1.1/2.0 | 0 | D29 | AD13 |
| PCI to PCI (DMI to PCI) | 0 | D30 | AD14 |
| AC97 MODEM | 0 | D30 | AD14 |
| AC97 Audio | 0 | D30 | AD14 |
| PATA/SATA | 0 | D31 | AD15 |
| LPC I/F | 0 | D31 | AD15 |
| SMBUS | 0 | D31 | AD15 |
| CPU I/F | 0 | D31 | AD15 |
| DMA | 0 | D31 | AD15 |
| PMU | 0 | D31 | AD15 |

## External PCI Devices

| DEVICE | PCI Device ID | IDSEL # | REQ/GNT # | PIRQ |
|---|---|---|---|---|
| CARD BUS | D6 | AD22 | 2 | ABCD |

## I2C / SMBUS ADDRESSING

| DEVICE | HEX | ADDRESS |
|---|---|---|
| DDR SO-DIMM 0 | A0 | 10100000 |
| DDR SO-DIMM 1 | A4 | 10100100 |
| CLOCK GENERATOR (EXT.) | D2 | 11010010 |

## Board ID / SKU ID Table for AD channel

| | |
|---|---|
| Vcc | 3.3V +/- 5% |
| Ra/Rc/Re | 100K +/- 1% |

| Board ID | Rb / Rd / Rf | $V_{AD\_BID}$ min | $V_{AD\_BID}$ typ | $V_{AD\_BID}$ max |
|---|---|---|---|---|
| 0 | 0 | 0 V | 0 V | 0.100 V |
| 1 | 8.2K +/- 1% | 0.216 V | 0.250 V | 0.289 V |
| 2 | 18K +/- 1% | 0.436 V | 0.503 V | 0.538 V |
| 3 | 33K +/- 1% | 0.712 V | 0.819 V | 0.875 V |
| 4 | 56K +/- 1% | 1.036 V | 1.185 V | 1.264 V |
| 5 | 100K +/- 1% | 1.453 V | 1.650 V | 1.759 V |
| 6 | 200K +/- 1% | 1.935 V | 2.200 V | 2.341 V |
| 7 | NC | 2.500 V | 3.300 V | 3.300 V |

## BOARD ID Table

| Board ID | PCB Revision |
|---|---|
| 0 | 0.1 |
| 1 | 0.2 |
| 2 | |
| 3 | |
| 4 | |
| 5 | |
| 6 | |
| 7 | |

## SKU ID Table

| SKU ID | SKU |
|---|---|
| 0 | |
| 1 | |
| 2 | |
| 3 | |
| 4 | |
| 5 | |
| 6 | |
| 7 | |

## BTO Option Table

| BTO Item | BOM Structure |
|---|---|
| VGA | PM@<br>GM@ |
| LAN | 82573G@<br>82573L@<br>82573@<br>82562@ |
| INT MIC. | 45MIC@ |
| DOCKING | WD@<br>WOD@ |
| CIR | CIR@ |
| FIR | FIR@ |
| SUPER I/O | 217@<br>SI207@ |
| Battery | 45@ |

| | | | |
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Title: Notes List

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This shall place near CPU

# Thermal Sensor ADM1032ARM

JP22A — YONAH

ADDR GROUP | DATA GROUP | HOST CLK | CONTROL | MISC | LEGACY CPU | THERMAL DIODE

FOX_PZ47903-2741-42_YONAH

**H_THERMDA, H_THERMDC routing together.**
**Trace width / Spacing = 10 / 10 mil**

ADM1032ARM_RM8

Placement near to ICH7

Placement near to CPU side

| | | | |
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Title: **Yonah CPU in mFCPGA479**

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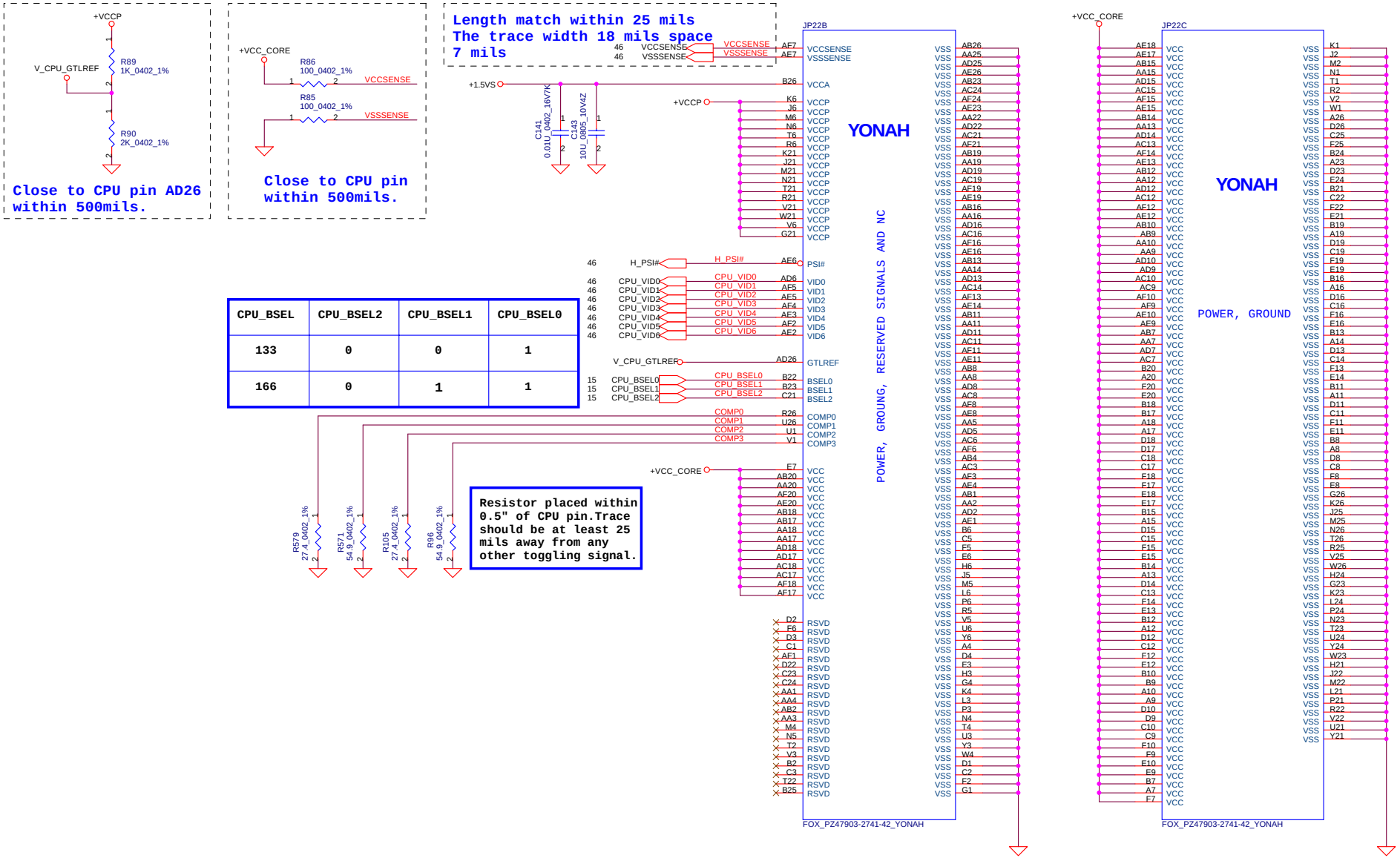


| CPU_BSEL | CPU_BSEL2 | CPU_BSEL1 | CPU_BSEL0 |
|---|---|---|---|
| 133 | 0 | 0 | 1 |
| 166 | 0 | 1 | 1 |

| | | | |
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Title: Yonah CPU in mFCPGA479

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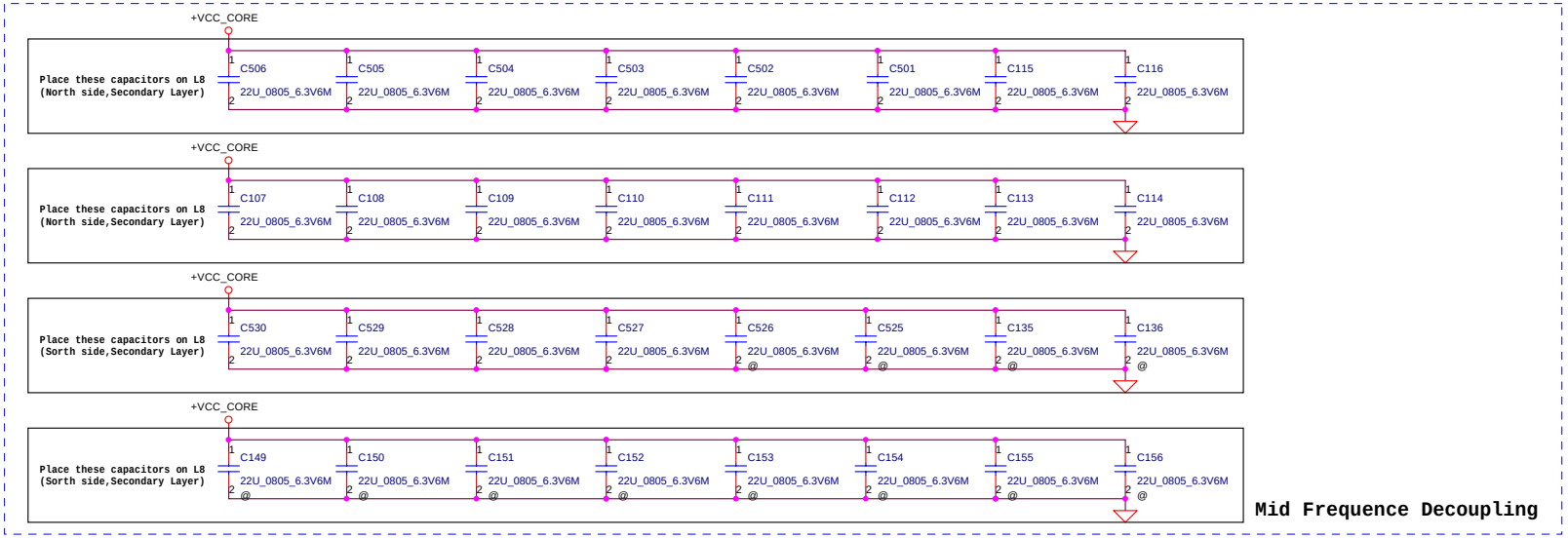
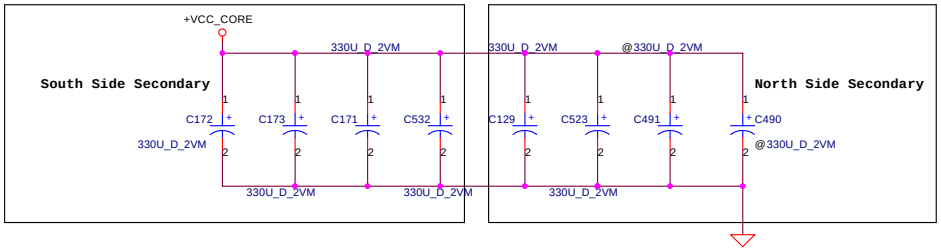
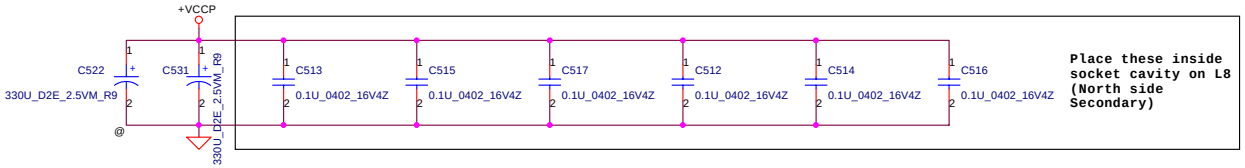



**ESR <= 1.5m ohm**
**Capacitor > 1980uF**

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Title: **CPU Bypass capacitors**

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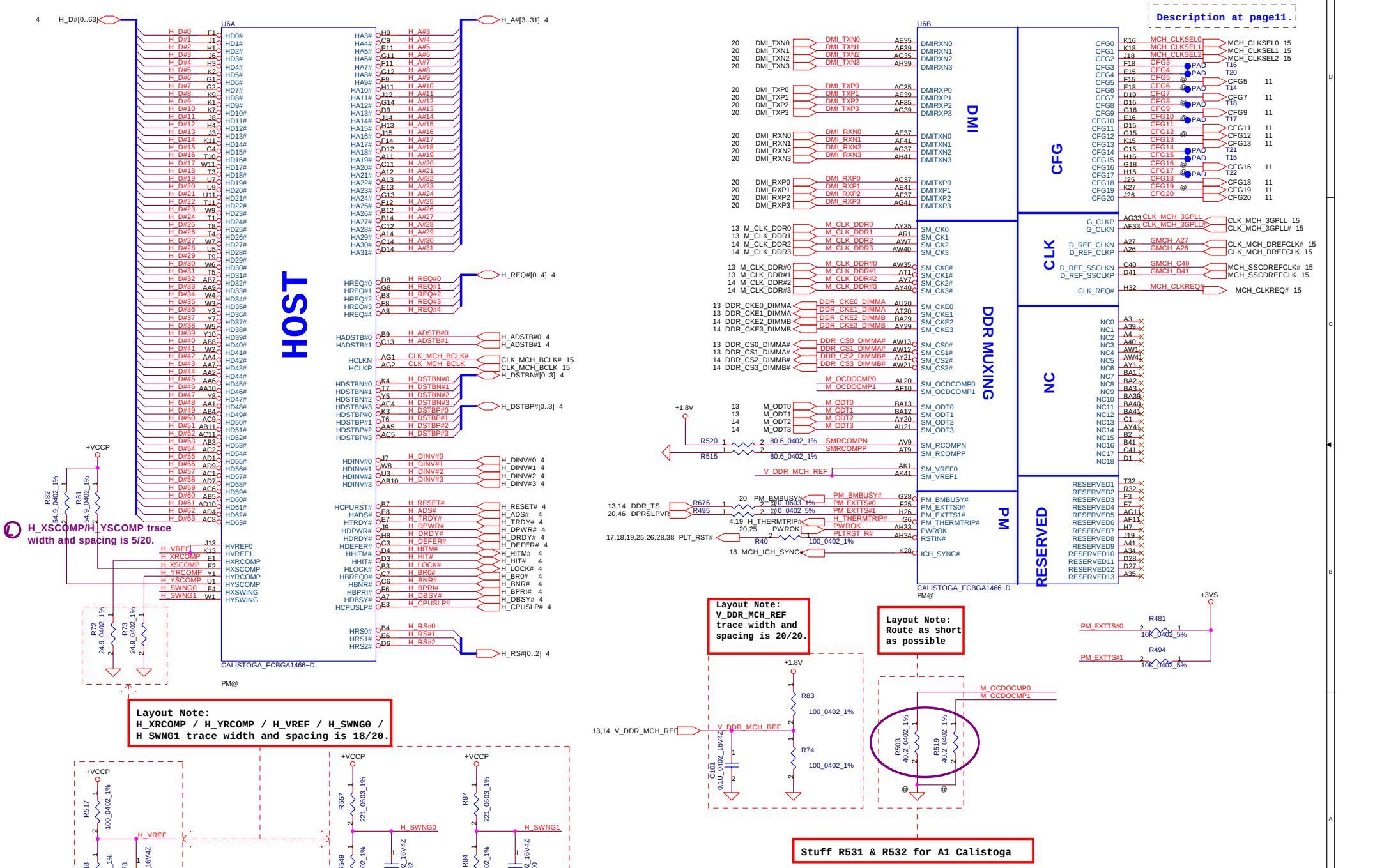


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Title: **Calistoga (1/6)**

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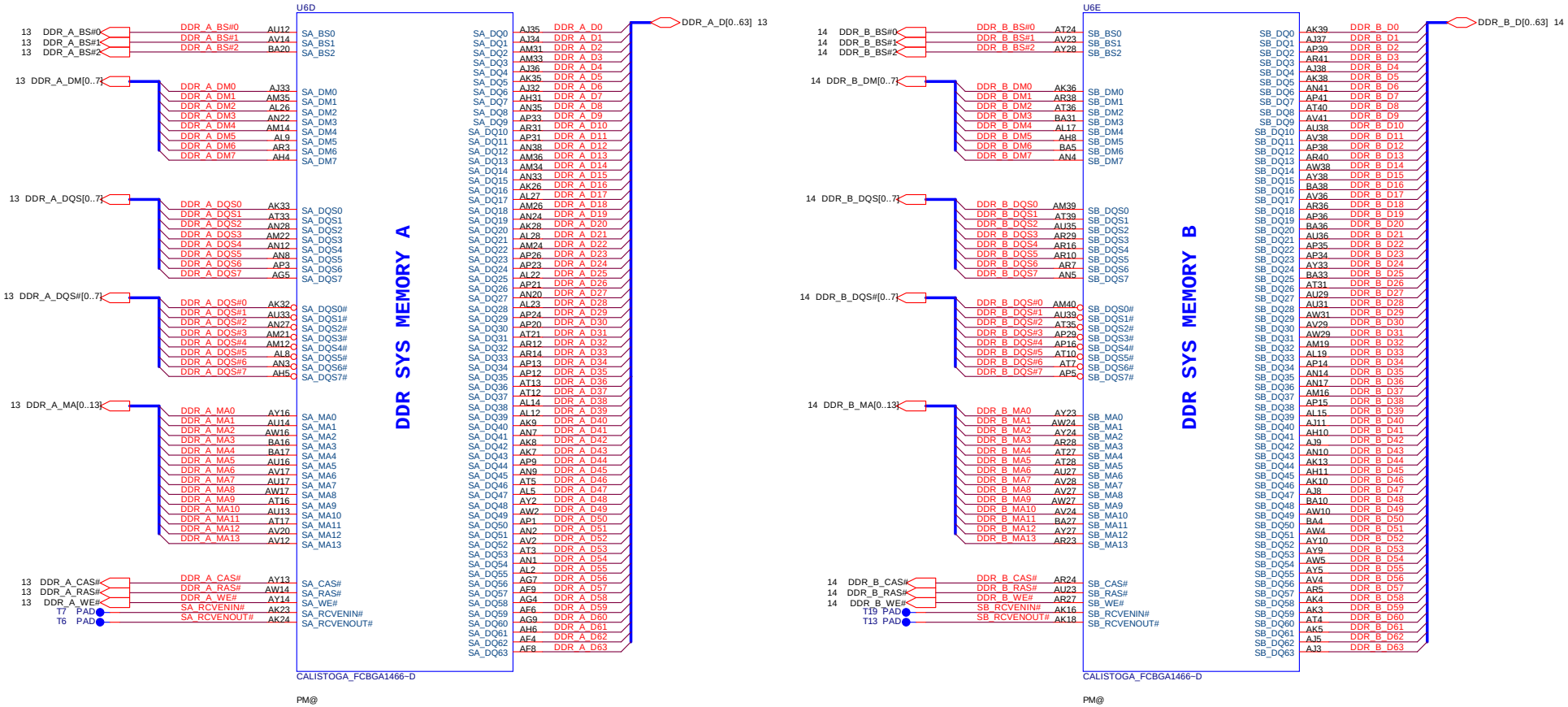


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Title: **Calistoga (2/6)**

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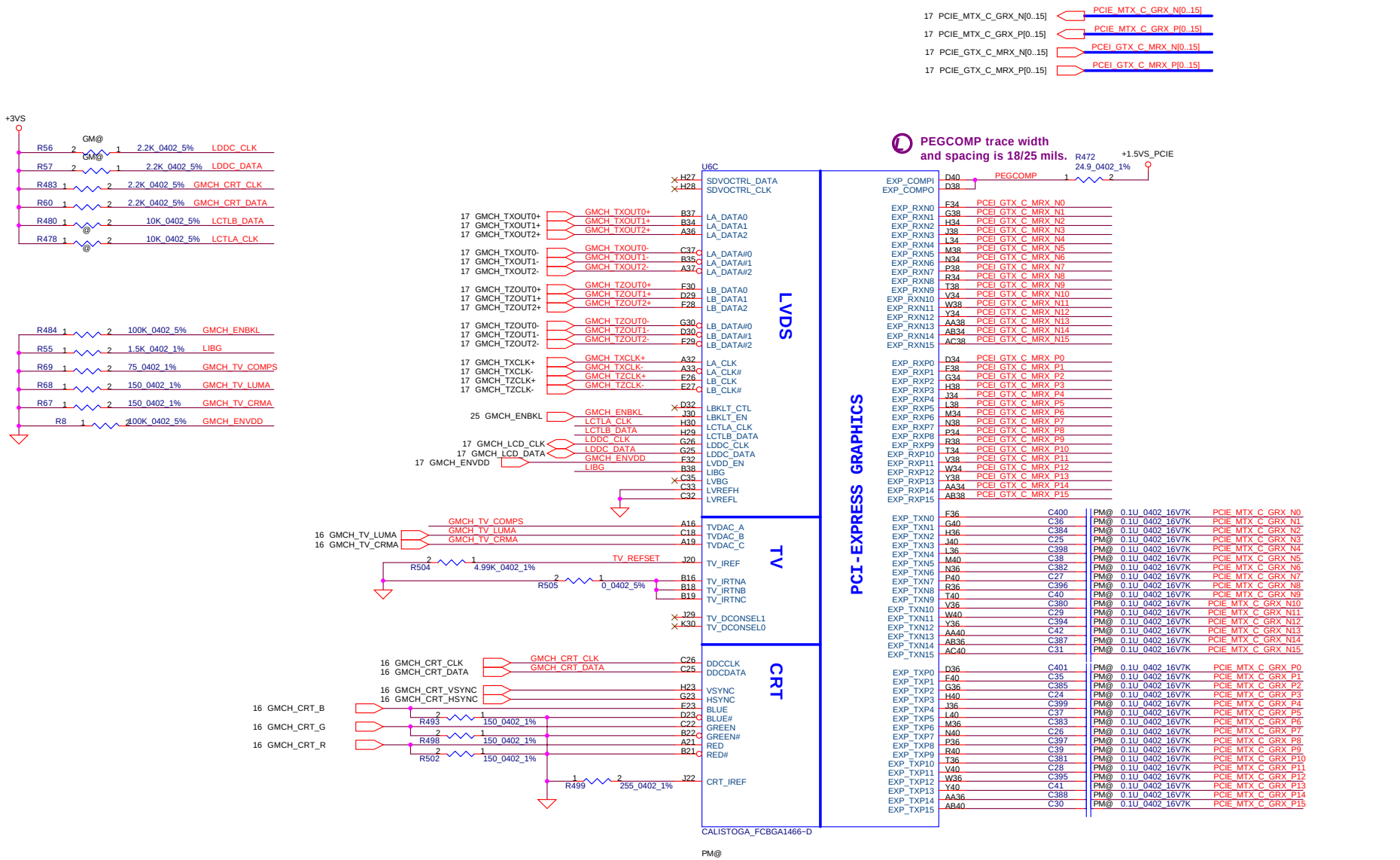


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Title: **Calistoga (3/6)**

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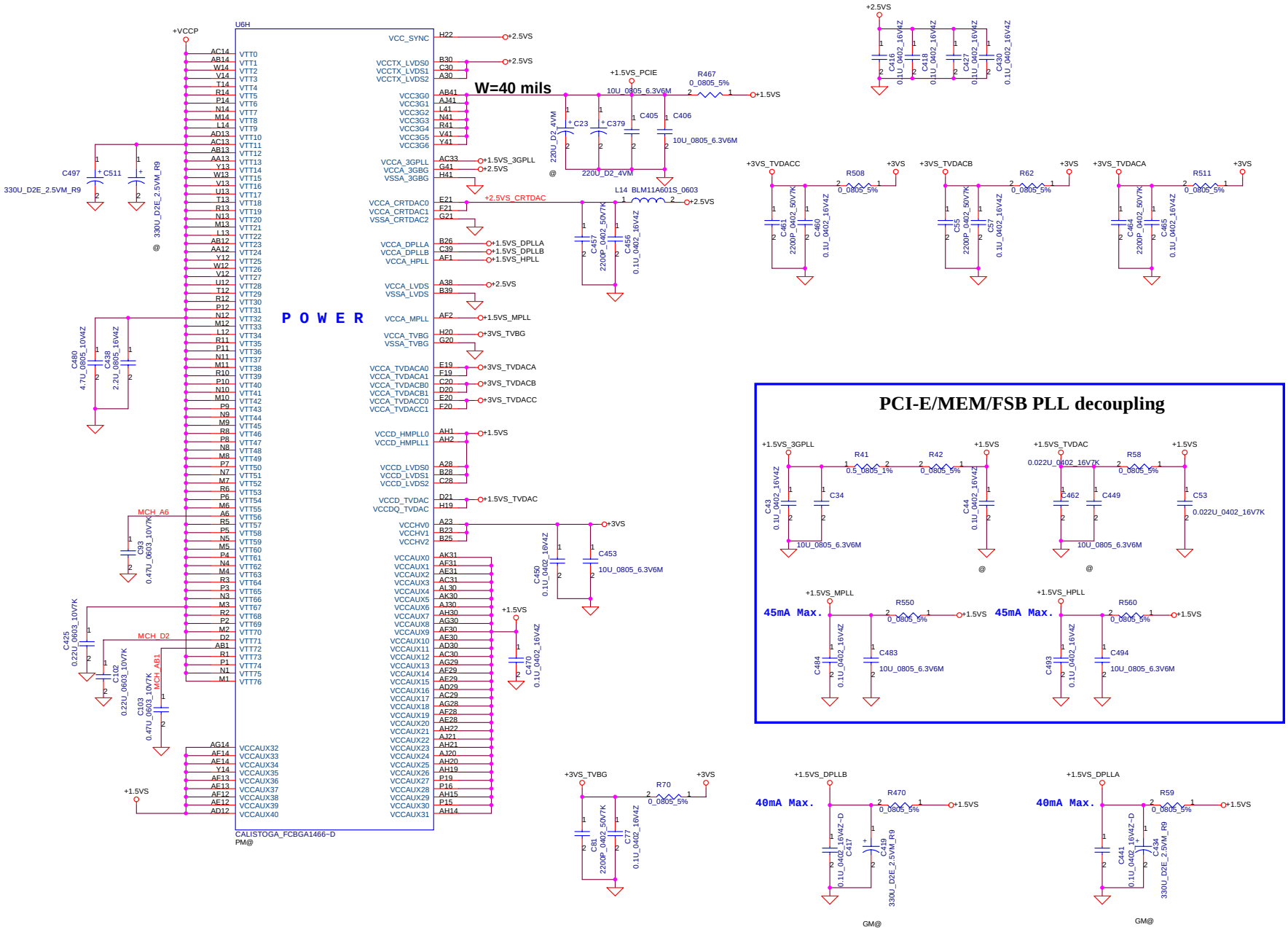


| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
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**Compal Electronics, Inc.**

Title: *Calistoga (4/6)*

| Size | Document Number | Rev |
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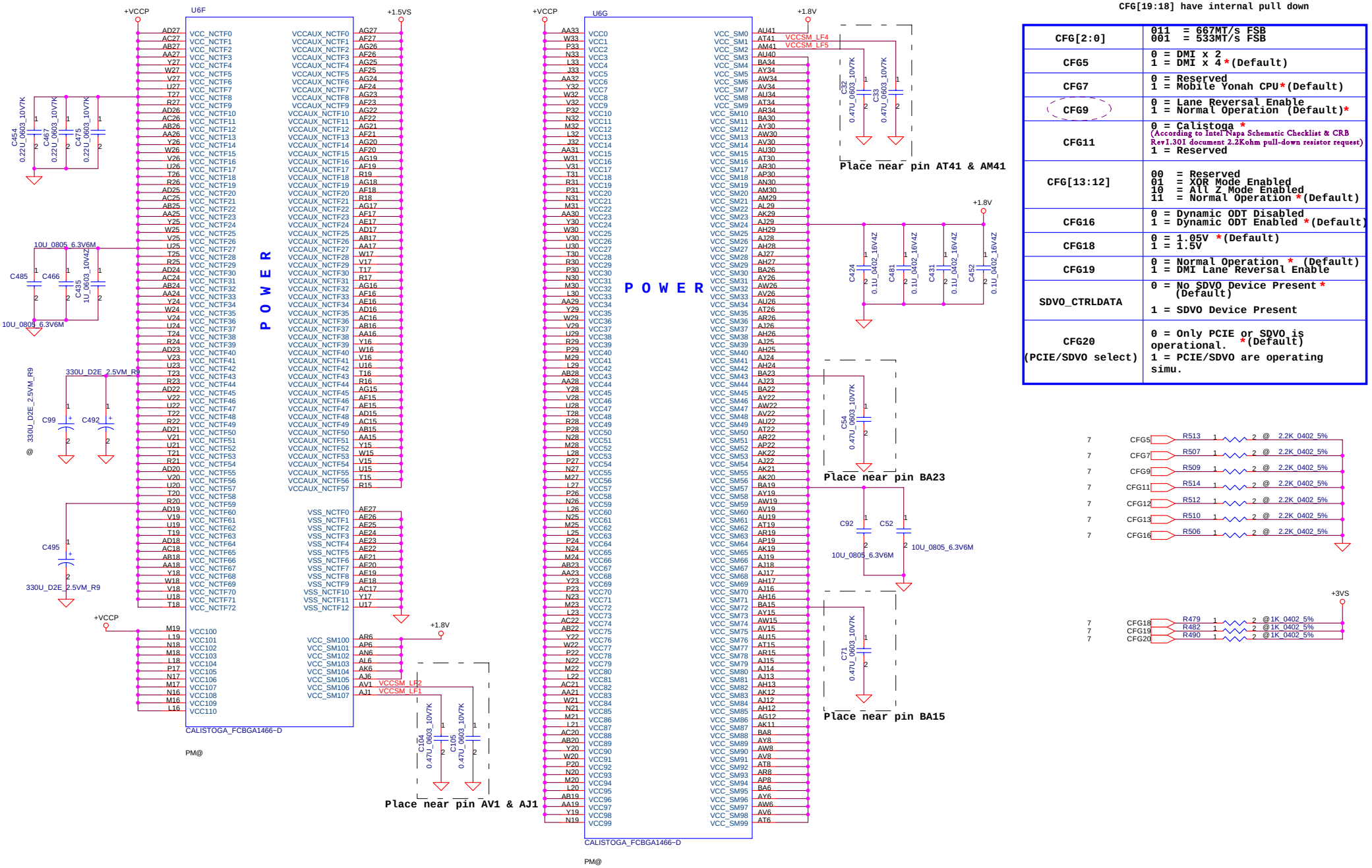
# Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

| | |
|---|---|
| CFG[2:0] | 011 = 667MT/s FSB<br>001 = 533MT/s FSB |
| CFG5 | 0 = DMI x 2<br>1 = DMI x 4 *(Default) |
| CFG7 | 0 = Reserved<br>1 = Mobile Yonah CPU*(Default) |
| CFG9 | 0 = Lane Reversal Enable<br>1 = Normal Operation (Default)* |
| CFG11 | 0 = Calistoga *<br>(According to Intel Napa Schematic Checklist & CRB Rev1.301 document 2.2Kohm pull-down resistor request)<br>1 = Reserved |
| CFG[13:12] | 00 = Reserved<br>01 = XOR Mode Enabled<br>10 = All Z Mode Enabled<br>11 = Normal Operation *(Default) |
| CFG16 | 0 = Dynamic ODT Disabled<br>1 = Dynamic ODT Enabled *(Default) |
| CFG18 | 0 = 1.05V *(Default)<br>1 = 1.5V |
| CFG19 | 0 = Normal Operation * (Default)<br>1 = DMI Lane Reversal Enable |
| SDVO_CTRLDATA | 0 = No SDVO Device Present * (Default)<br>1 = SDVO Device Present |
| CFG20 (PCIE/SDVO select) | 0 = Only PCIE or SDVO is operational. *(Default)<br>1 = PCIE/SDVO are operating simu. |

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Title: **Calistoga (5/6)**

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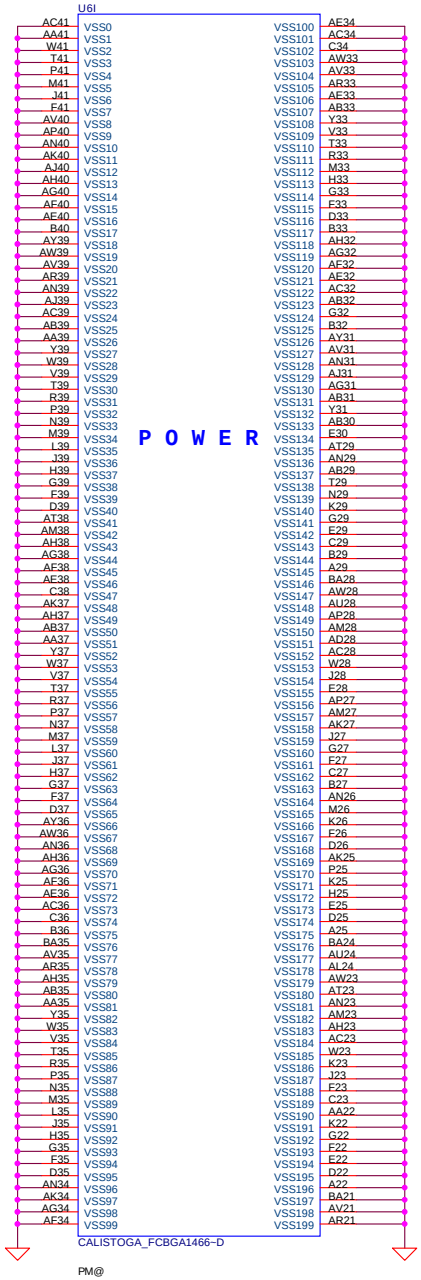


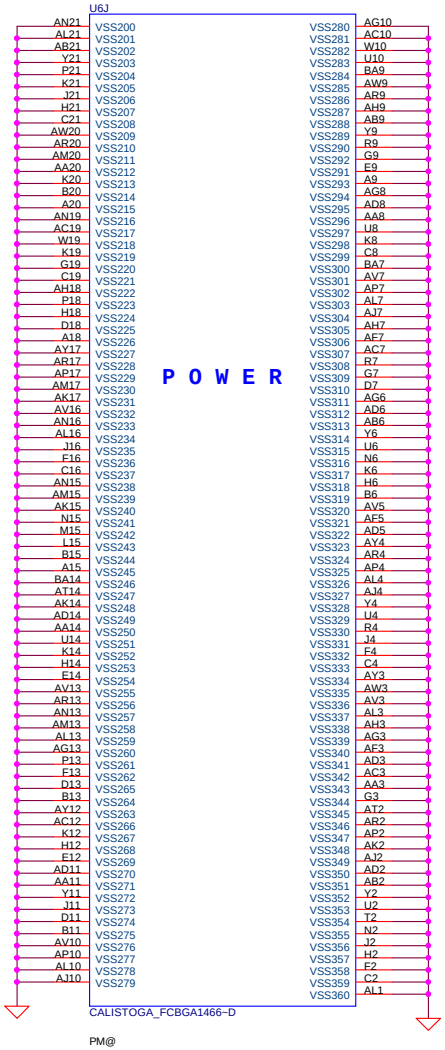


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Title: **Calistoga (6/6)**

| Size | Document Number | Rev |
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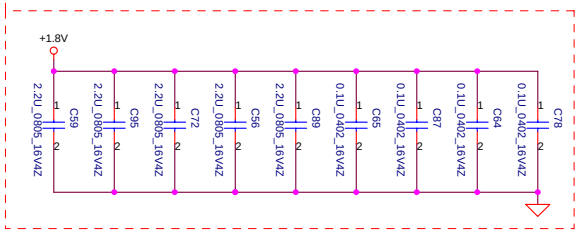
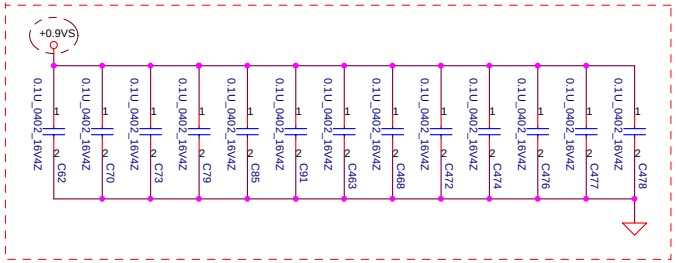
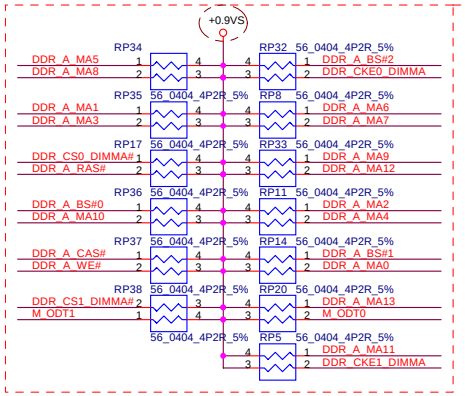
8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
8 DDR_A_MA[0..13]

**Layout Note:**
**Place near JP27**




**Layout Note:**
**Place one cap close to every 2 pullup resistors terminated to +0.9VS**




**Layout Note:**
**Place these resistor closely JP27,all trace length Max=1.5"**


| | | | |
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Title: **DDRII-SODIMM SLOT1**

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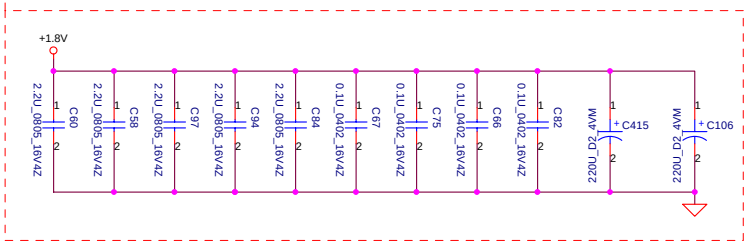
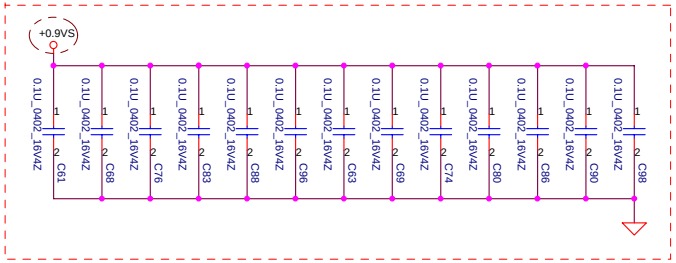
8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..13]

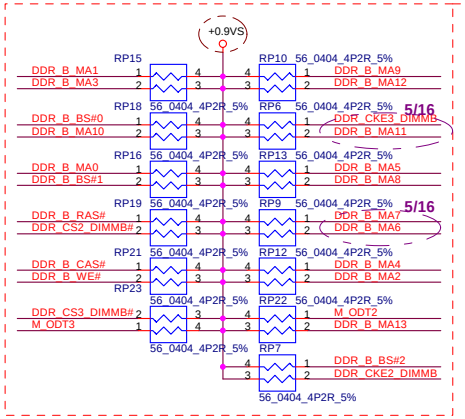
**Layout Note:**
**Place near JP26**

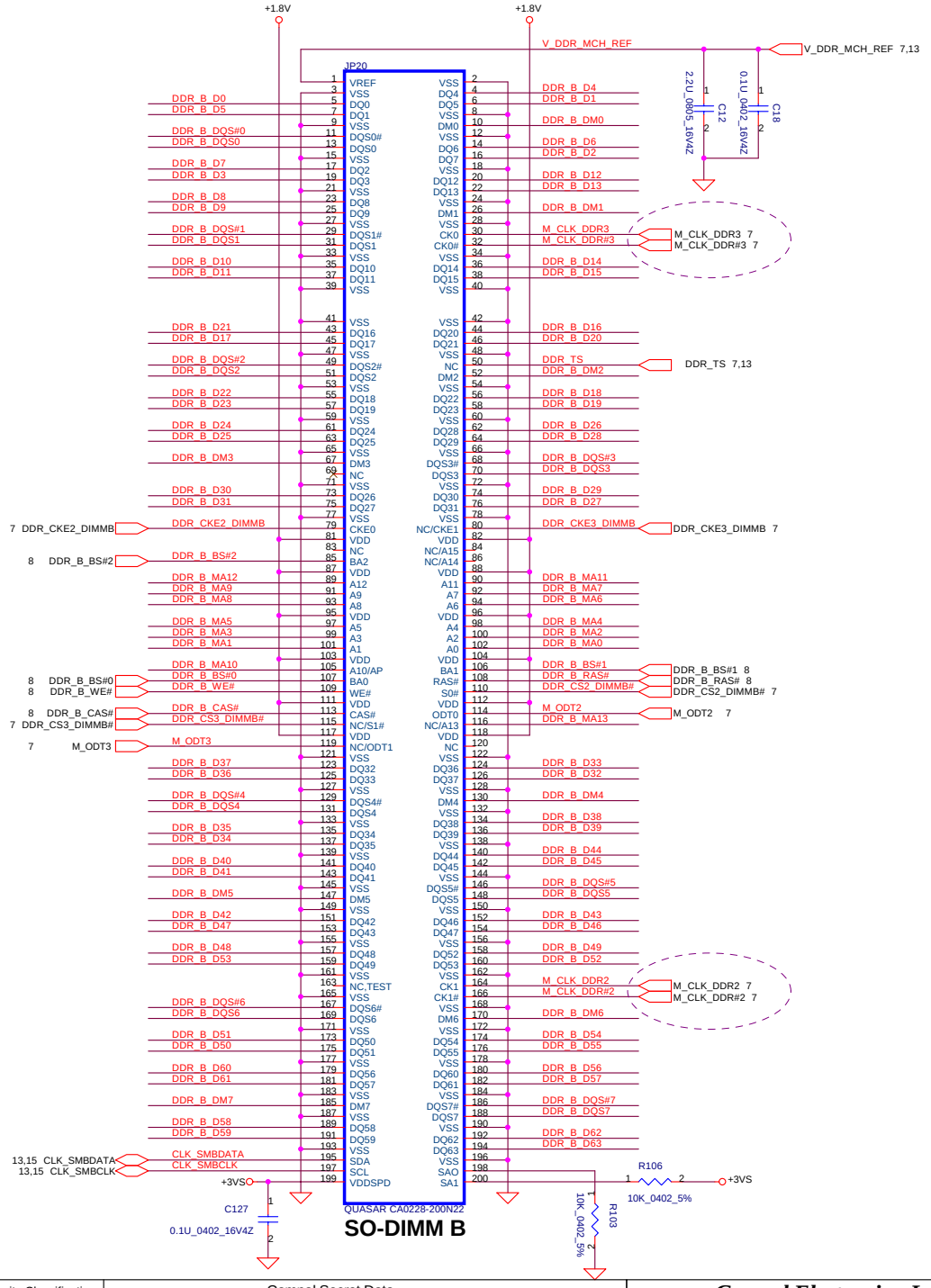



**Layout Note:**
**Place one cap close to every 2 pullup resistors terminated to +0.9VS**




**Layout Note:**
**Place these resistor closely JP26,all trace length Max=1.5"**

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Title: **DDRII-SODIMM SLOT2**

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| FSLC CLKSEL2 | FSLB CLKSEL1 | FSLA CLKSEL0 | CPU MHz | SRC MHz | PCI MHz |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 133 | 100 | 33.3 |
| 0 | 1 | 1 | 166 | 100 | 33.3 |

5/20

Place these components near each pin within 40 mils.

Reserve for ICS954305

Reserve for ICS954305 & R need change to 475ohm

*0:CLKREQ5# for Pin 29

*1:PCICLK3 for Pin28

1:24M *0:test Mode for Pin 45

1:48M *0:CLKREQ7# for Pin 38

1:CPU ITP *0:SRC 10

1:27M/SRC0 *0:DOT 96M/LCD100

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Title: **Clock generator**

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# CRT Connector

Match with Docking resistor to 150ohm

## CRT CONNECTOR

Near to JP45

**Close to VGA conn.**

**Pop with No-Docking**

**Close to VGA conn.**

**Close to VGA conn.**

**Close to VGA conn.**

## TV-OUT Conn.

1. Y ground
2. C ground
3. Y (luminance+sync)
4. C (crominance)

## CRT Conn.

| | | | |
|---|---|---|---|
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| Issued Date | 2005/06/01 | Deciphered Date | 2006/06/01 |



**Compal Electronics, Inc.**

Title: *CRT & TVout Connector*

Size | Document Number: *LA-3011P* | Rev: 0.2

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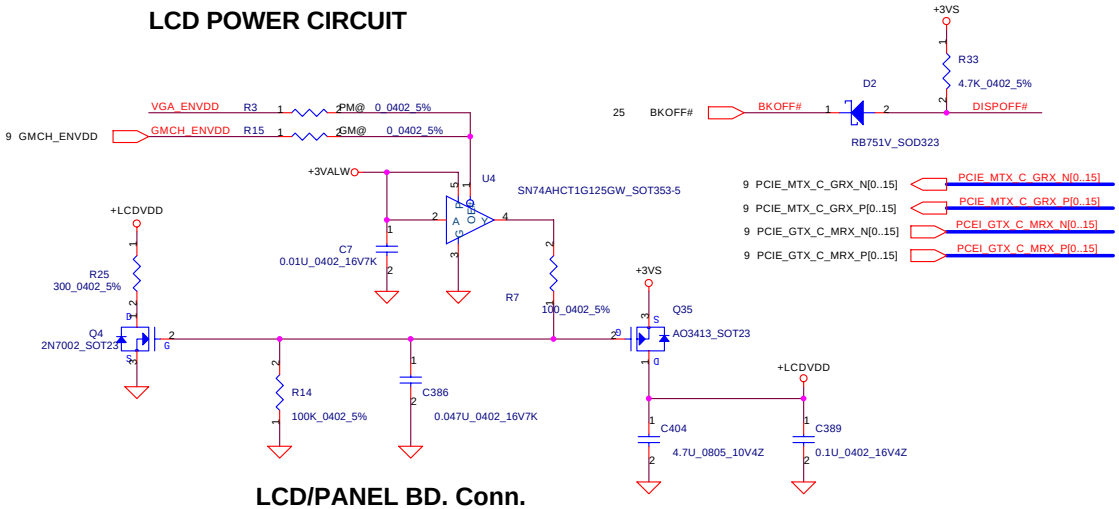
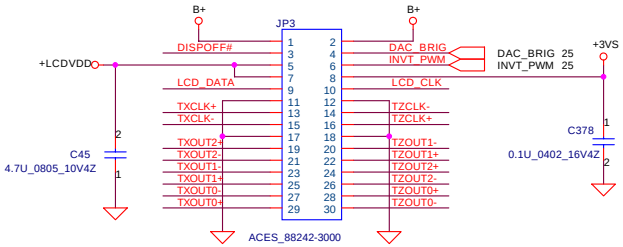
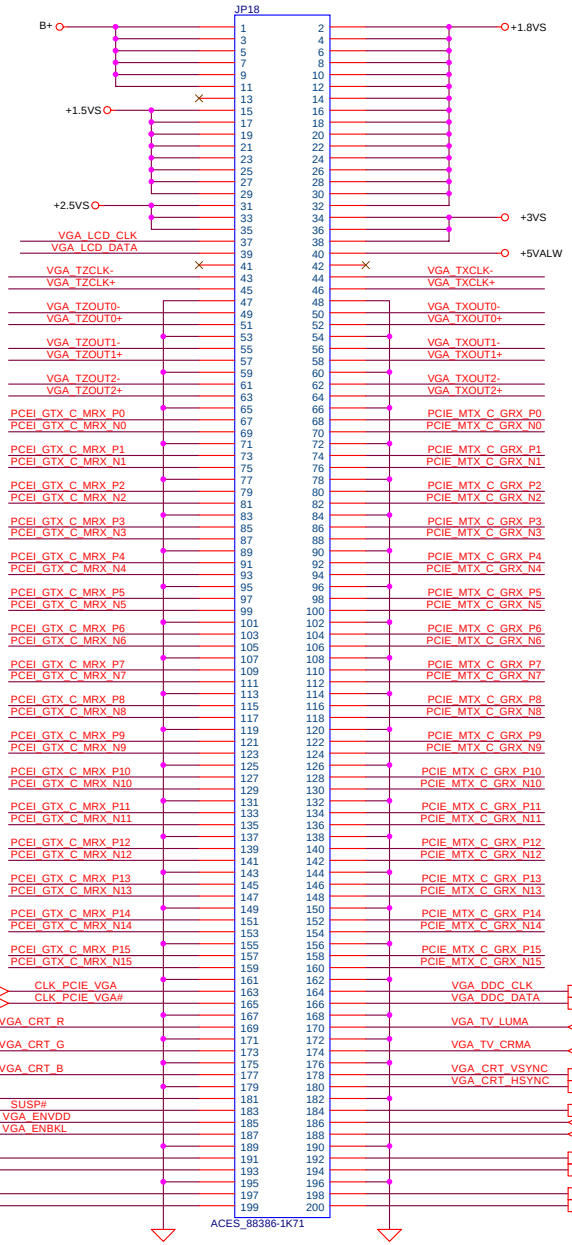
# LCD POWER CIRCUIT

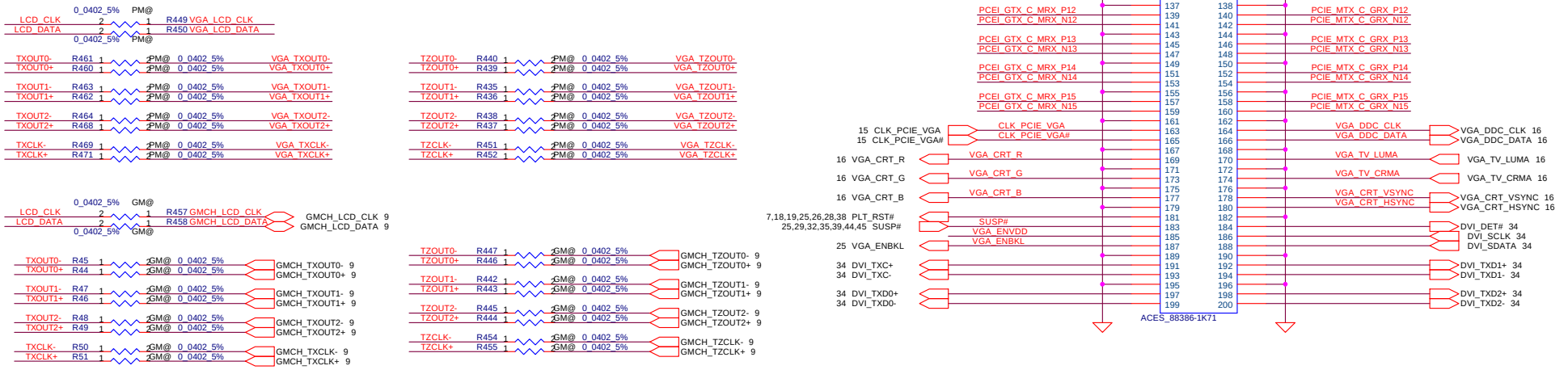



# LCD/PANEL BD. Conn.




# VGA BOARD Conn.

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|---|---|---|---|
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Title: *VGA / LCD CONN.*

Size | Document Number: *LA-3011P* | Rev: 0.2

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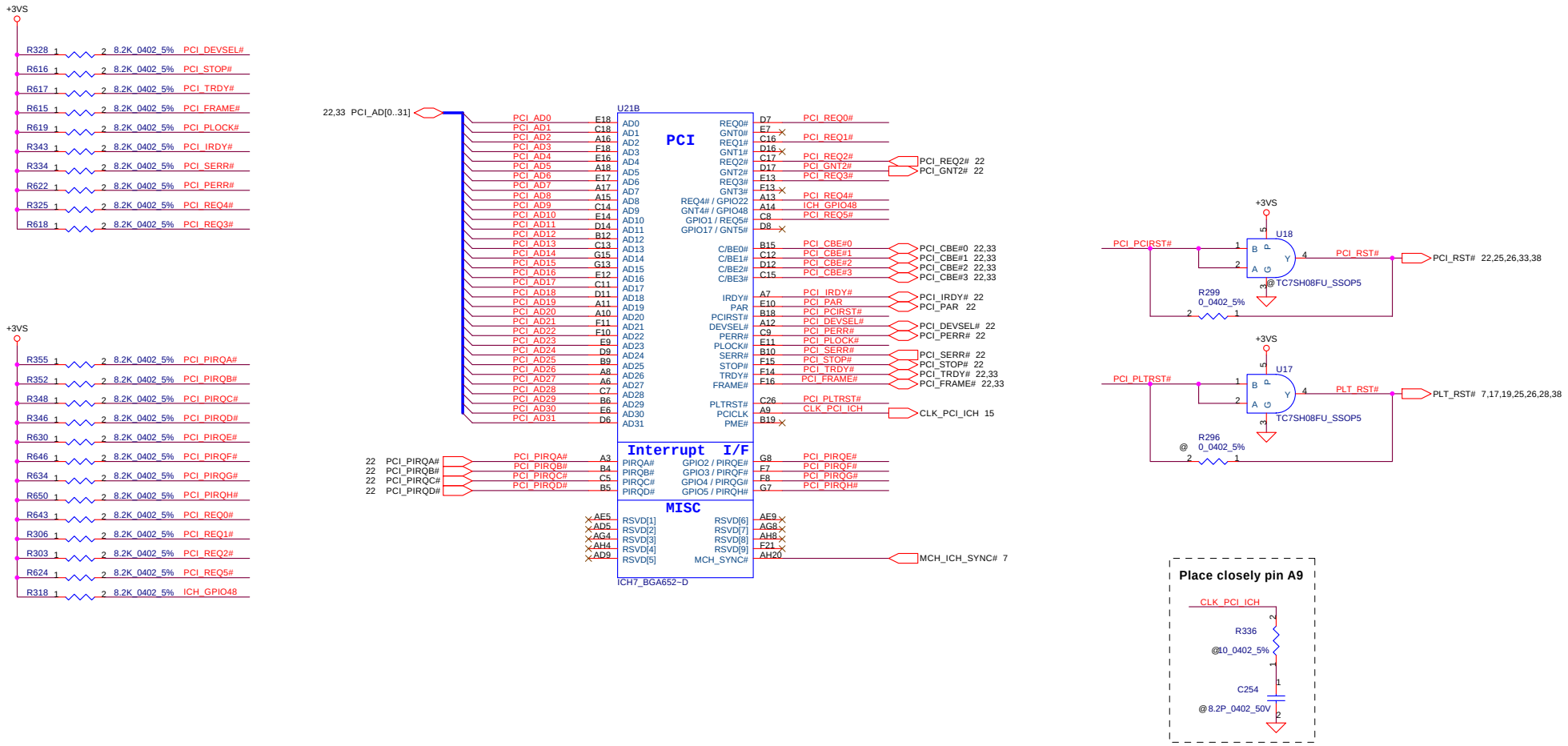


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Title: **ICH7-M(1/4)**

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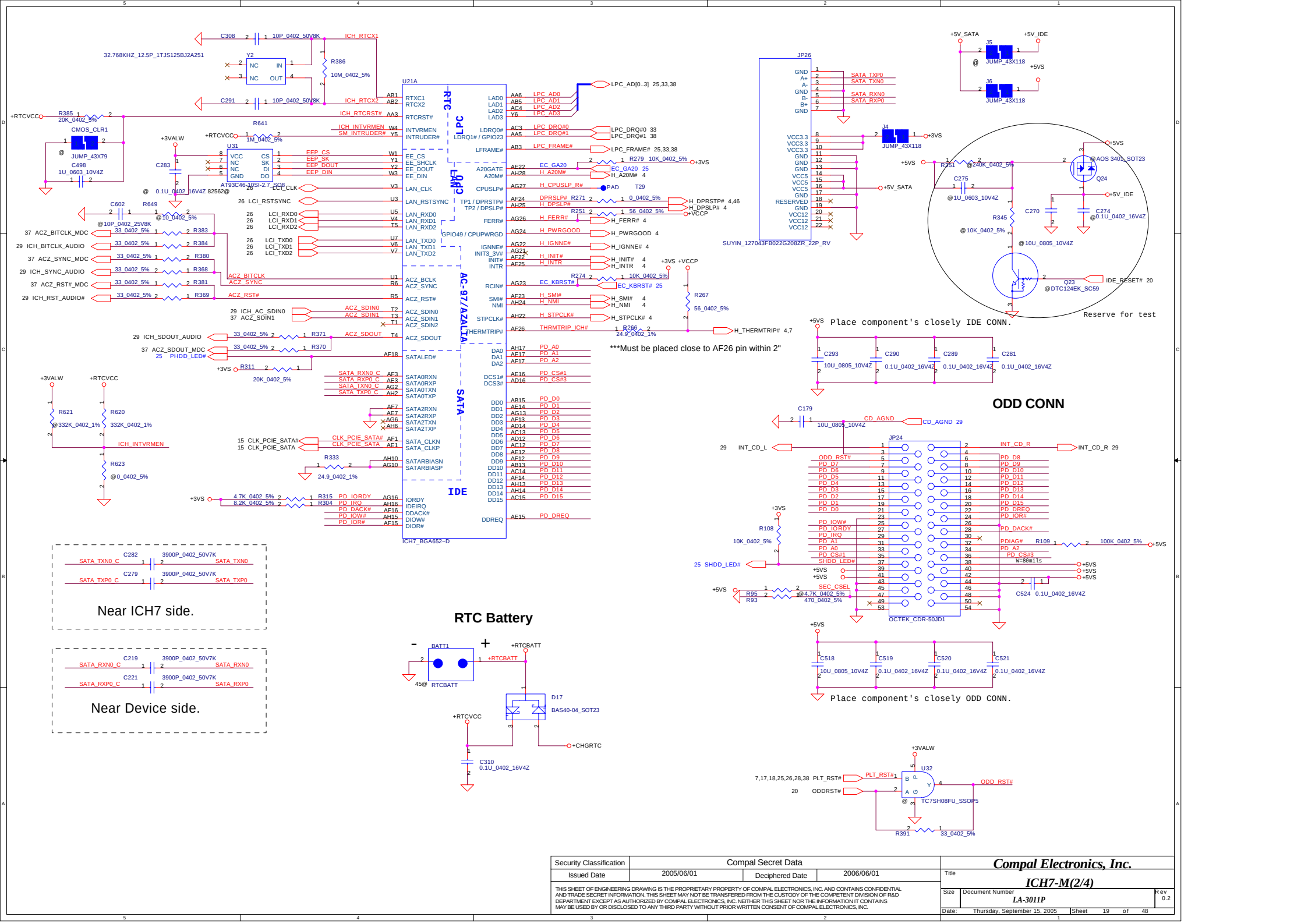
|---|---|---|
| | LA-3011P | 0.2 |

Date: Thursday, September 15, 2005 | Sheet 18 of 48


ICH7_BGA652-D
Near ICH7 side.
Near Device side.
RTC Battery
Place component's closely IDE CONN.
Place component's closely ODD CONN.
ODD CONN
***Must be placed close to AF26 pin within 2"
Reserve for test
SUYIN_127043FB022G2082ZR_22P_RV
OCTEK_CDR-50JD1
Security Classification
Compal Secret Data
Issued Date
2005/06/01
Deciphered Date
2006/06/01
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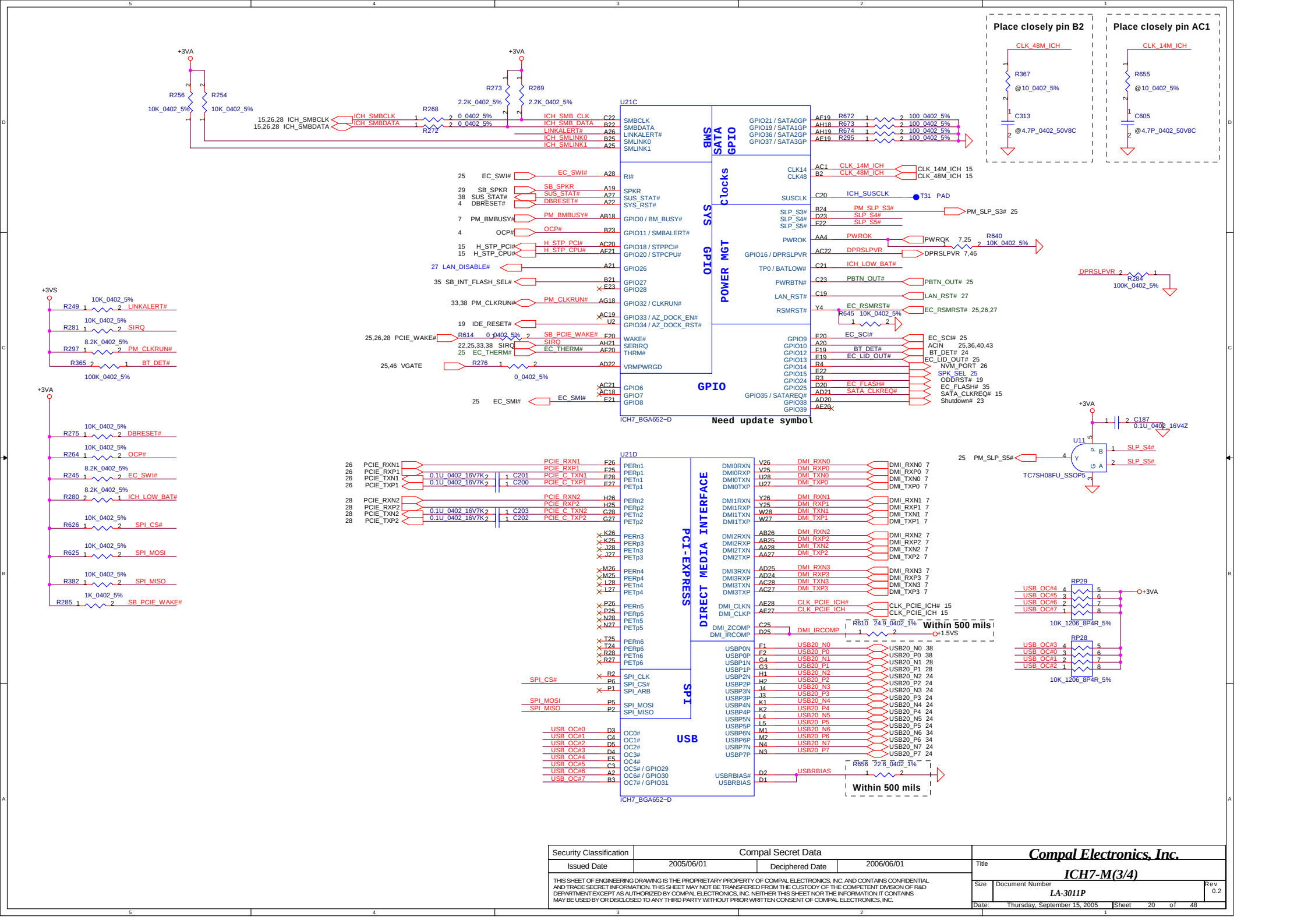
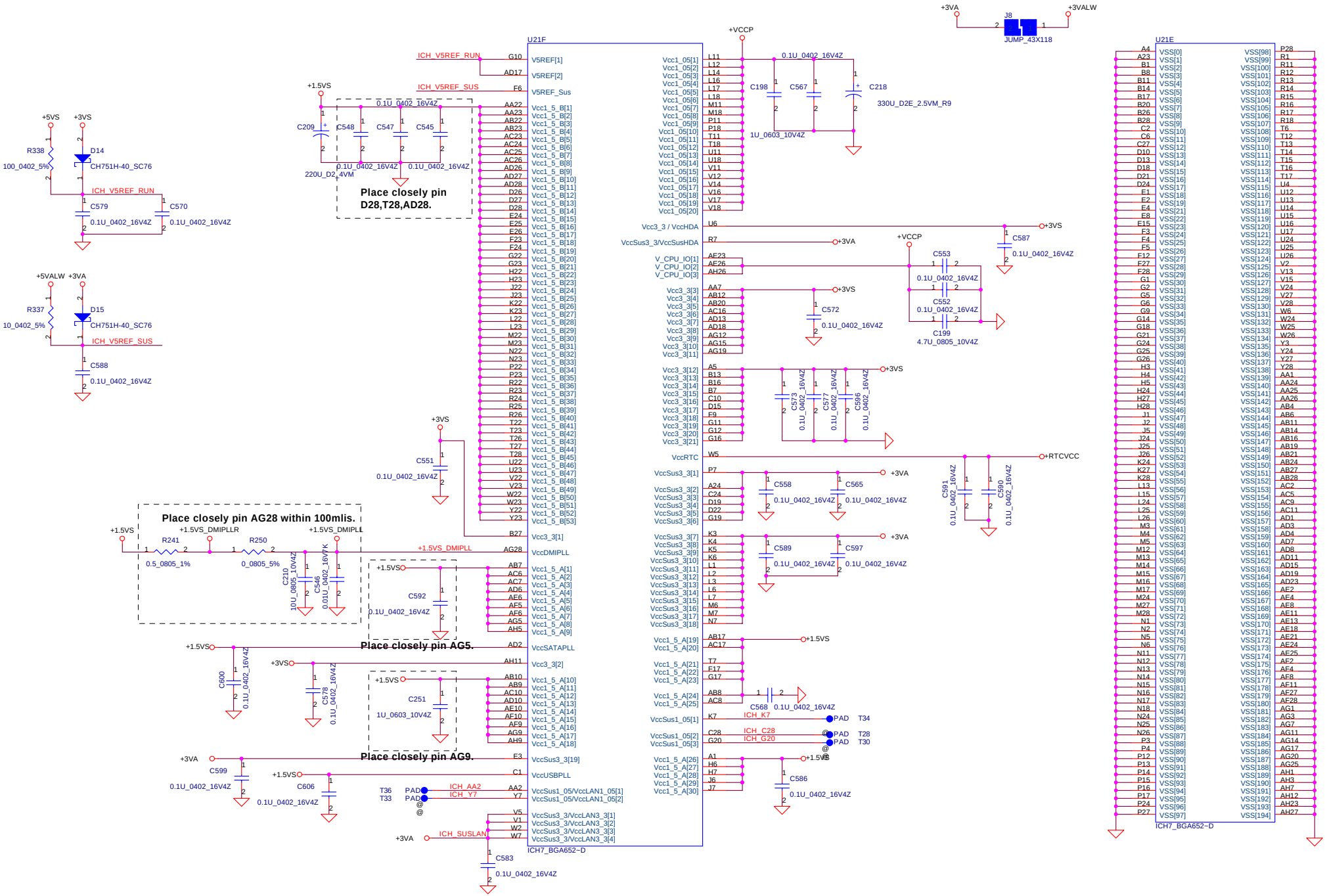
Compal Electronics, Inc.
Title
ICH7-M(2/4)
Size
Document Number
LA-3011P
Rev
0.2
Date: Thursday, September 15, 2005
Sheet 19 of 48




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/01 | Deciphered Date | 2006/06/01 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: ICH7-M(3/4) | | | |
| Size | Document Number: LA-3011P | | Rev: 0.2 |
| Date: Thursday, September 15, 2005 | Sheet 20 of 48 | | |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/01 | Deciphered Date | 2006/06/01 |



**Compal Electronics, Inc.**

Title: **ICH7-M(4/4)**

| Size | Document Number | Rev |
|---|---|---|
| | LA-3011P | 0.2 |

Date: Thursday, September 15, 2005 | Sheet 21 of 48

# PCI7412

## 5 in 1 CardReader Conn.

CLOSE TO CHIP

CLOSE TO CHIP

place near Chip 7411

| | | | |
|---|---|---|---|
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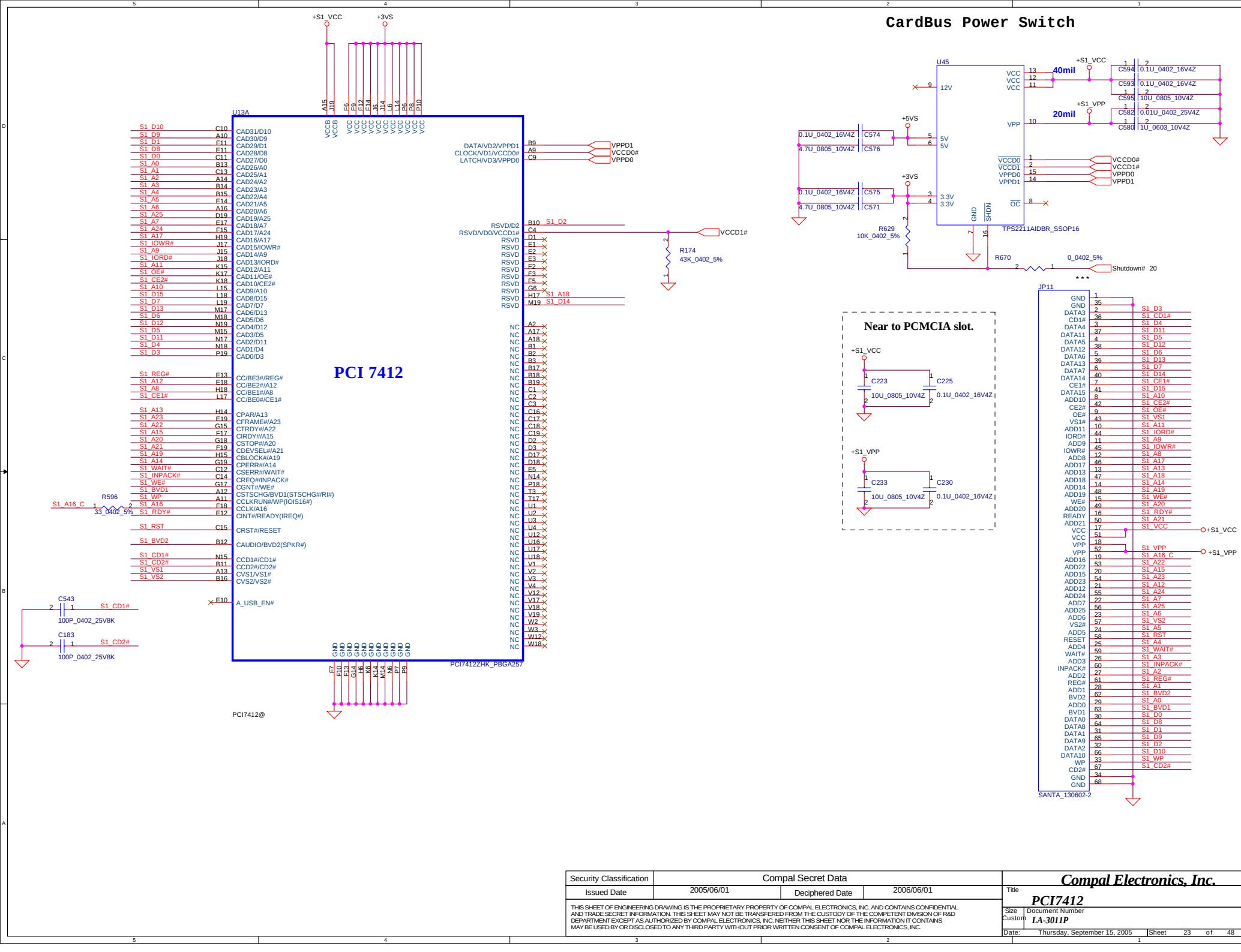
**Compal Electronics, Inc.**

Title: **PCI7412**

Size: Custom | Document Number: **LA-3011P** | Rev: 0.2

Date: Thursday, September 15, 2005 | Sheet 22 of 48

# CardBus Power Switch




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/01 | Deciphered Date | 2006/06/01 |



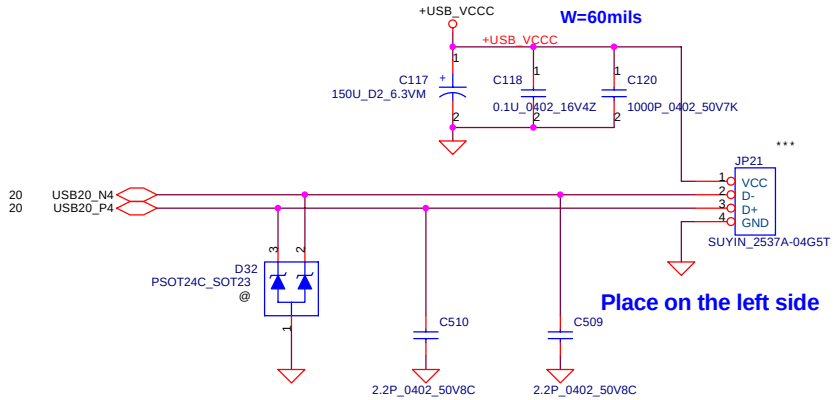
**Compal Electronics, Inc.**

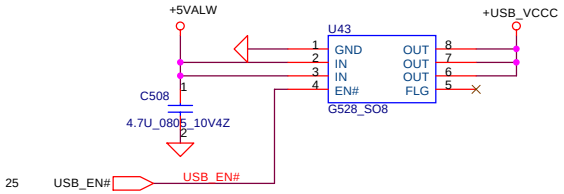
Title: **PCI7412**

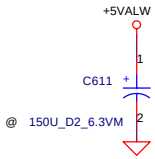
| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-3011P | 0.2 |

Date: Thursday, September 15, 2005 | Sheet 23 of 48

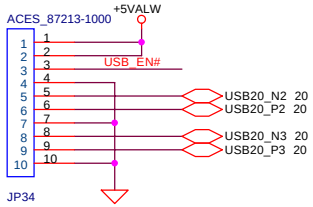
## USB CONN. 1



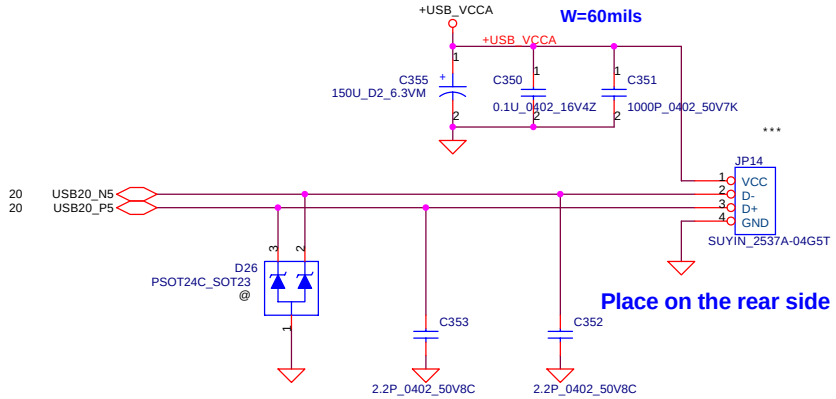



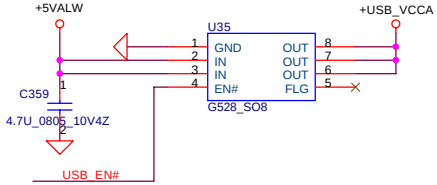




## 2 port in right side

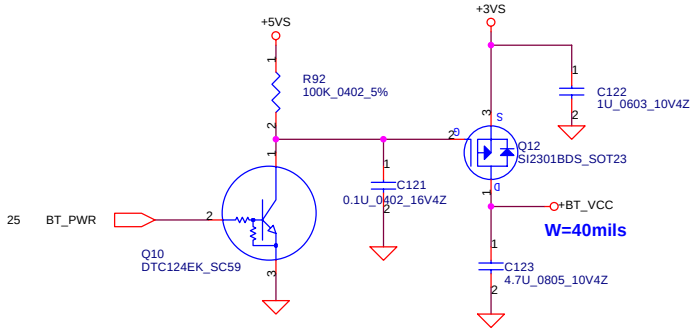


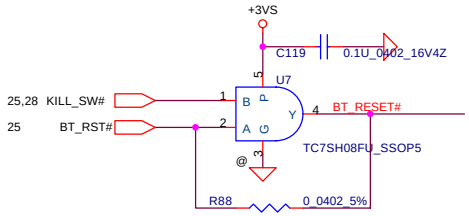

## USB CONN.2

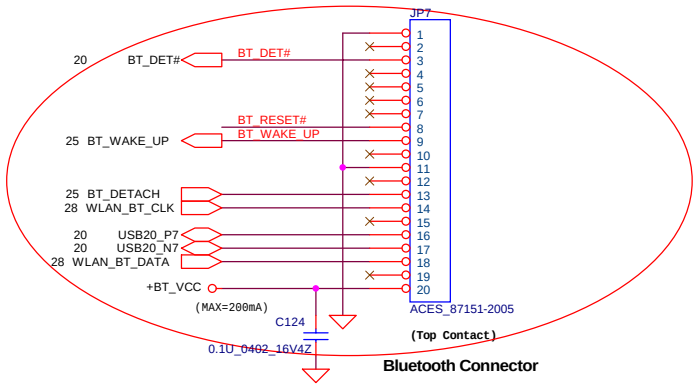



## Bluetooth Conn.

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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/01 | Deciphered Date | 2006/06/01 |



**Compal Electronics, Inc.**

Title: ***USB & BT Connector***

| Size | Document Number | Rev |
|---|---|---|
| | ***LA-3011P*** | 0.2 |

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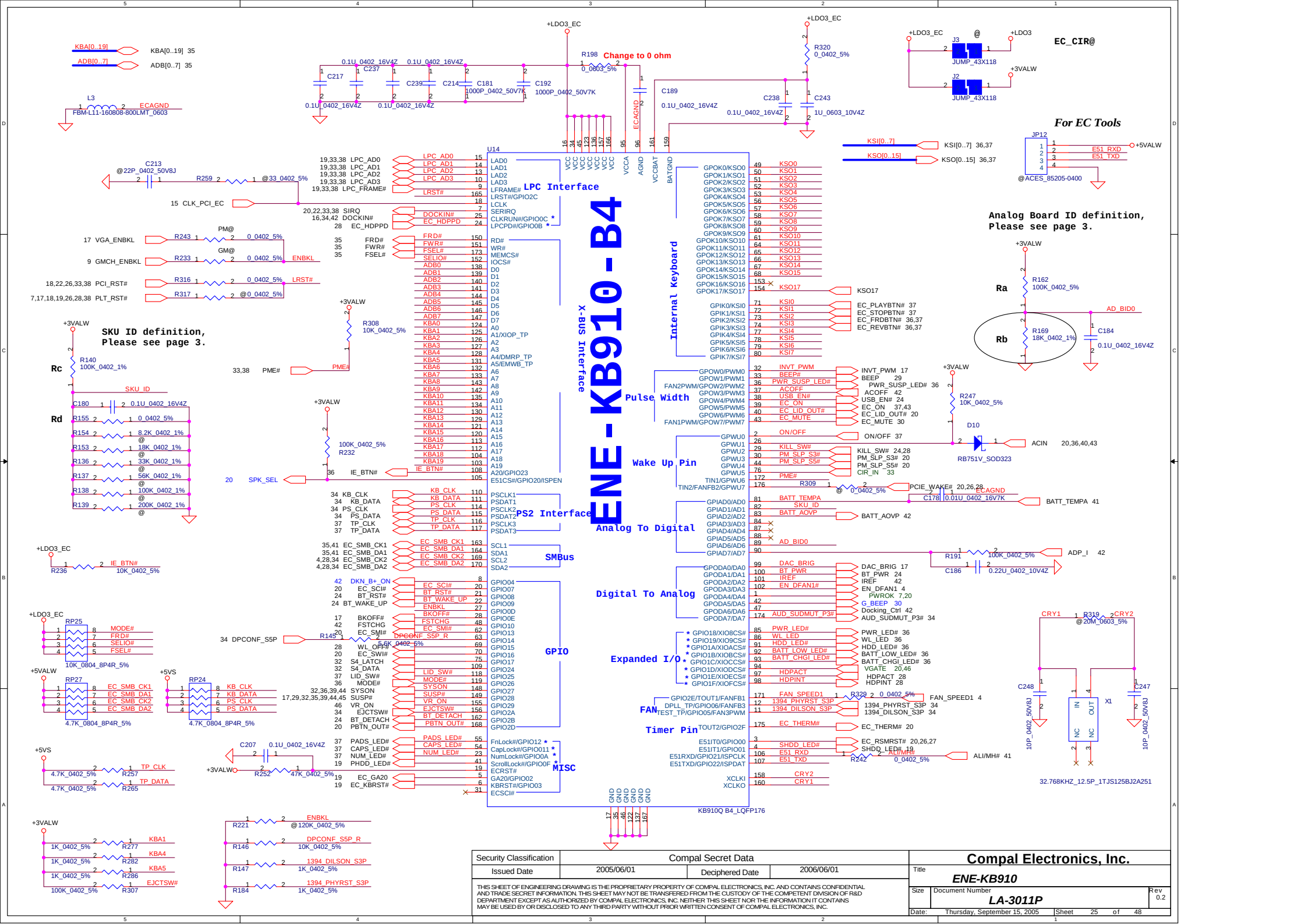



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/01 | Deciphered Date | 2006/06/01 |



**Compal Electronics, Inc.**

Title: ***ENE-KB910***

| Size | Document Number | Rev |
|---|---|---|
| | ***LA-3011P*** | 0.2 |

Date: Thursday, September 15, 2005 | Sheet 25 of 48

**Tekoa 82573E -> IAMT support only (WoL Support)**
**Vidalia 82573L -> No management**
**82562GZ -> 10/100 support**

*Only stuff for 82562 bias*

*When support S5 WOL this pin connect to EC to be a wake up even*

*Pull high support D3 cold power state*

*Connect to GPIO pin for SPI protect*
*Pull high -> NVM protect*
*Pull low -> Non protect*

*Pull down when with docking (Control PHY strength)*

**ICH7 SMBALRT# signal reserve**
**a 0ohm resistor connect to S0 power**
*Must pull high to S0 power for system power good*

*Must connect to RSMRST# (S5 power)*

*Connect to colck gen for PCIE clock request*

*Close to IC 82573*
*Non stuff when use 82562GZ*

*When use 82573G/L R535,R534,R533, R532 = 49.9ohm*
*When use 82562GZ R535,R534,R533, R532 = 54.9ohm and C489, C488, non-stuff*

*Stuff for 82573E*
*No-stuff for 82573L*

*Use dedicate SPI flash only*

*GST5009 for GIGA LAN*
*TST1284B for 10/100 LAN*

**10/100 LAN C19,C22 change to 0.01uF (SE068103K80)*

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/10 | Deciphered Date | 2006/06/01 |

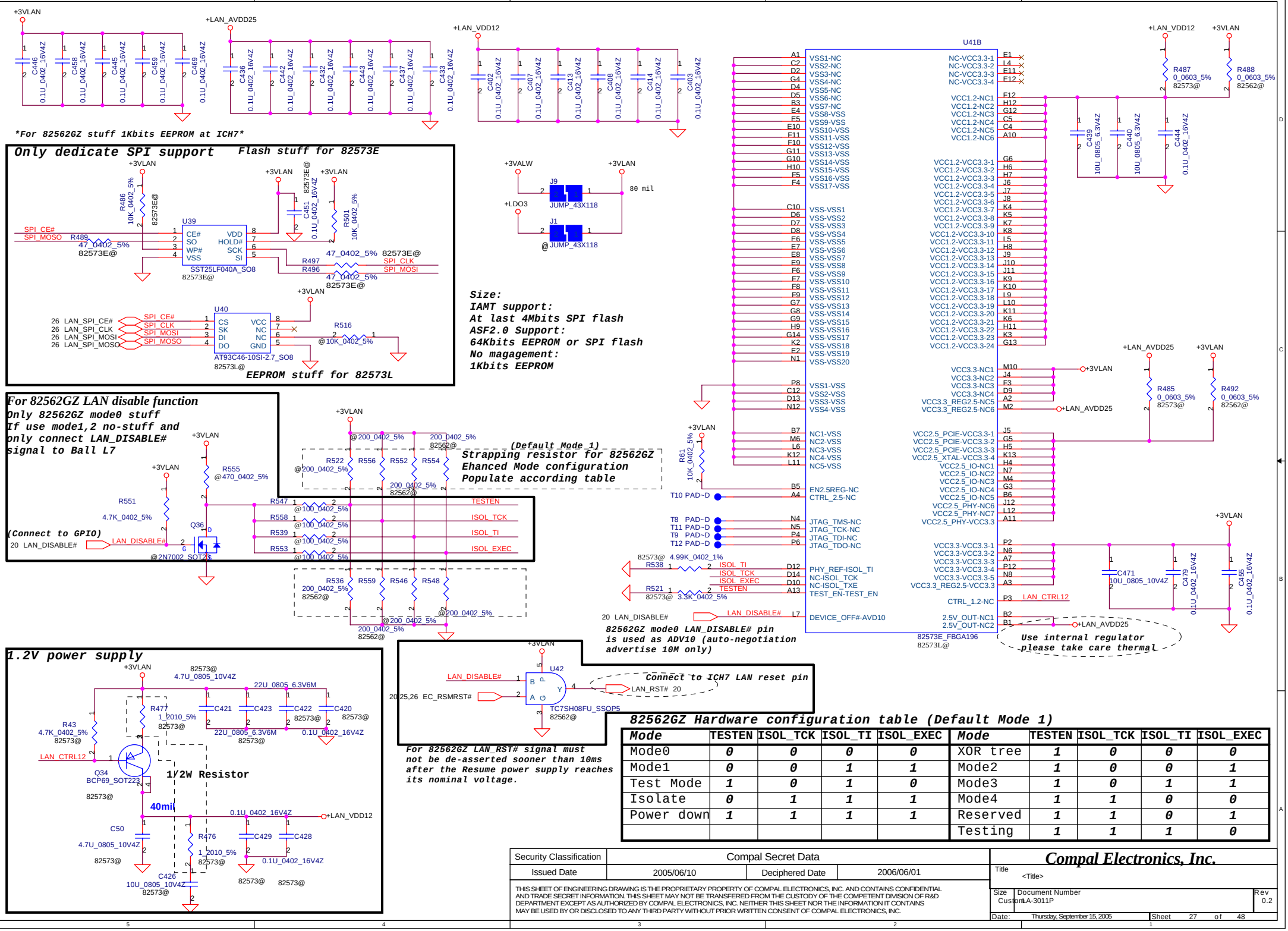


**Compal Electronics, Inc.**

Title: **Intel 82573E/L and 82562GZ**

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-3011P | 0.2 |

Date: Thursday, September 15, 2005 Sheet 26 of 48



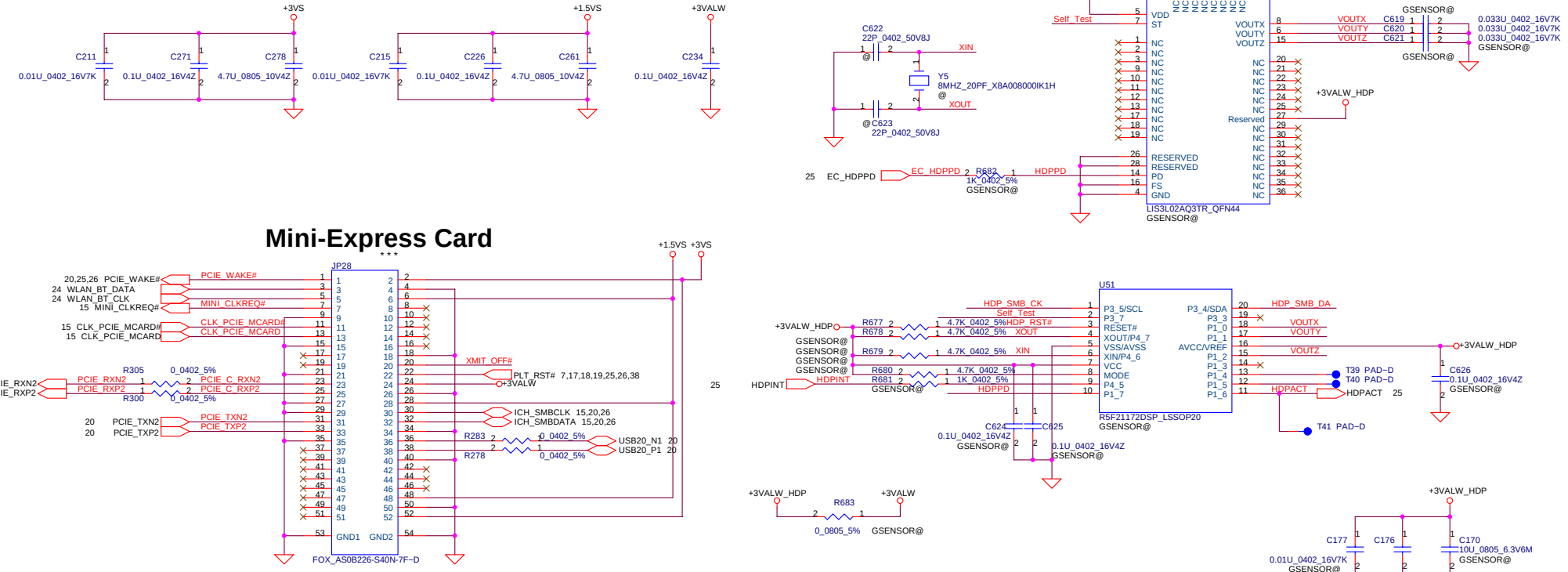

## 82562GZ Hardware configuration table (Default Mode 1)

| Mode | TESTEN | ISOL_TCK | ISOL_TI | ISOL_EXEC | Mode | TESTEN | ISOL_TCK | ISOL_TI | ISOL_EXEC |
|---|---|---|---|---|---|---|---|---|---|
| Mode0 | 0 | 0 | 0 | 0 | XOR tree | 1 | 0 | 0 | 0 |
| Mode1 | 0 | 0 | 1 | 1 | Mode2 | 1 | 0 | 0 | 1 |
| Test Mode | 1 | 0 | 1 | 0 | Mode3 | 1 | 0 | 1 | 1 |
| Isolate | 0 | 1 | 1 | 1 | Mode4 | 1 | 1 | 0 | 0 |
| Power down | 1 | 1 | 1 | 1 | Reserved | 1 | 1 | 0 | 1 |
| | | | | | Testing | 1 | 1 | 1 | 0 |



**Compal Electronics, Inc.**

| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size: Custom | Document Number: LA-3011P | | Rev: 0.2 |
| Date: Thursday, September 15, 2005 | | Sheet 27 of 48 | |

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| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/01 | Deciphered Date | 2006/06/01 |

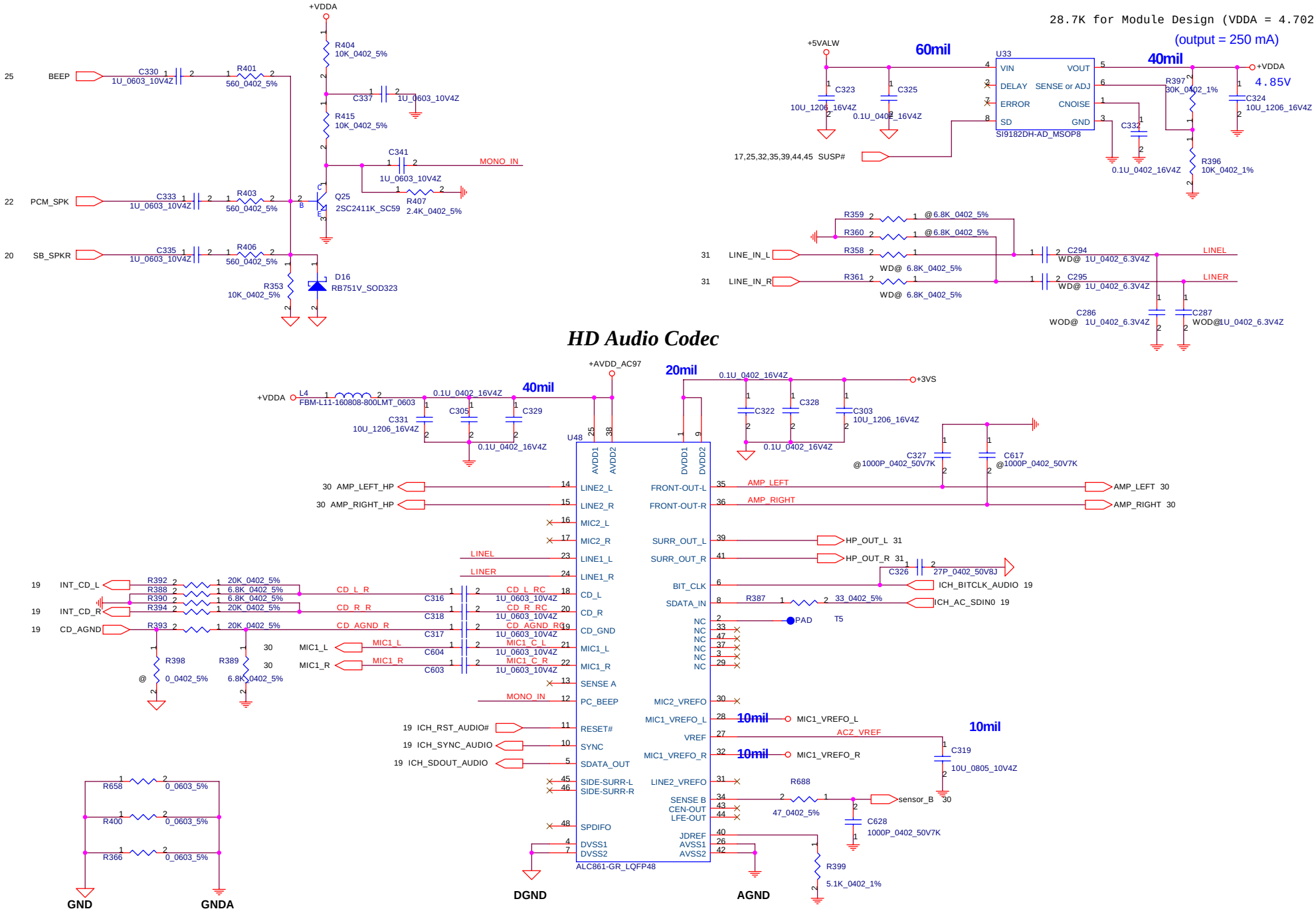


**Compal Electronics, Inc.**

Title: **Mini-Card/Mini-PCI/Accelerometer**

| Size | Document Number | Rev |
|---|---|---|
| | LA-3011P | 0.2 |

Date: Thursday, September 15, 2005 | Sheet 28 of 48




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/05/12 | Deciphered Date | 2006/06/01 |

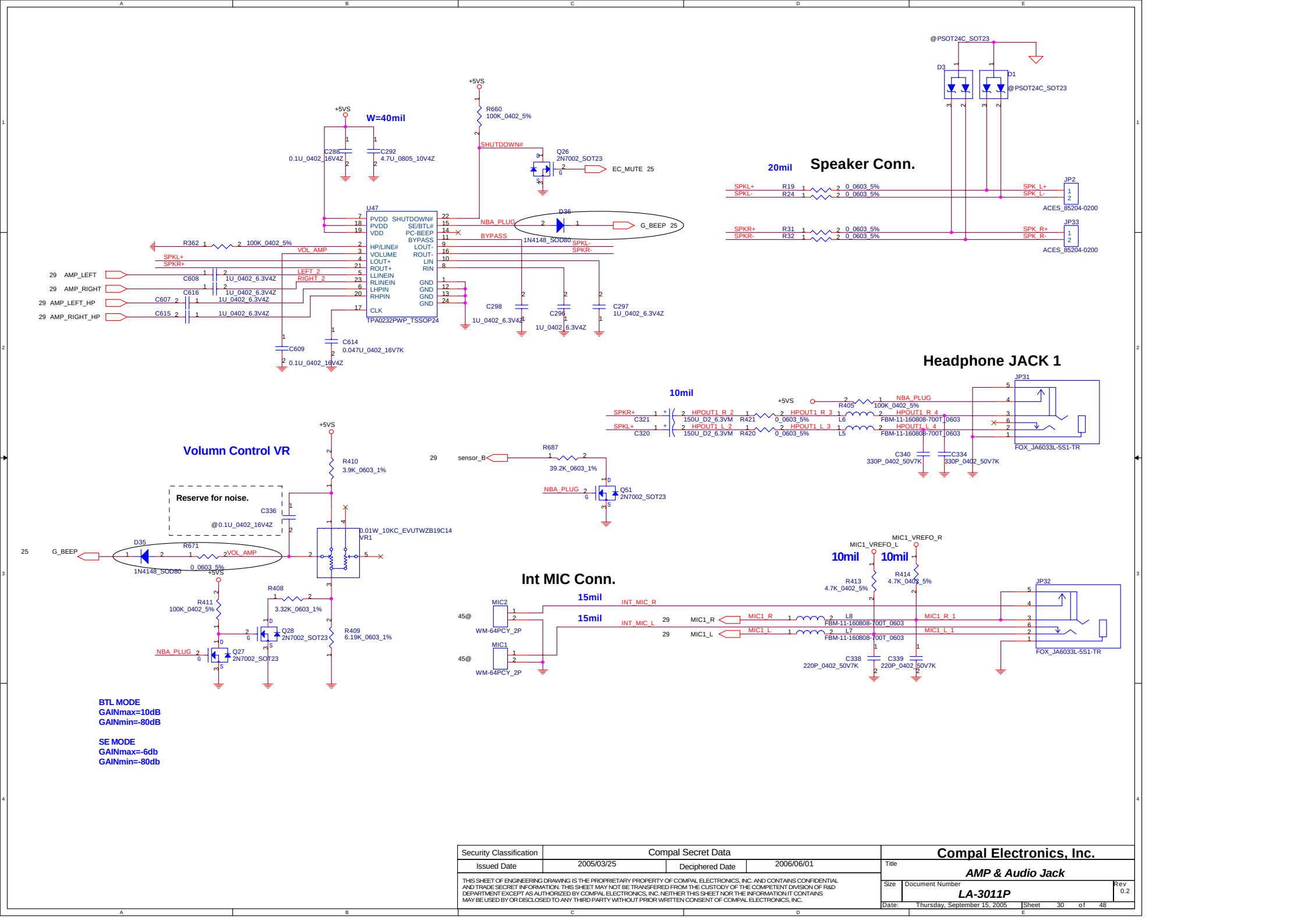


**Compal Electronics, Inc.**

Title: HD Audio Codec ALC260D

| Size | Document Number | Rev |
|---|---|---|
| B | LA-3011P | 0.2 |

Date: Thursday, September 15, 2005 Sheet 29 of 48




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/03/25 | Deciphered Date | 2006/06/01 |

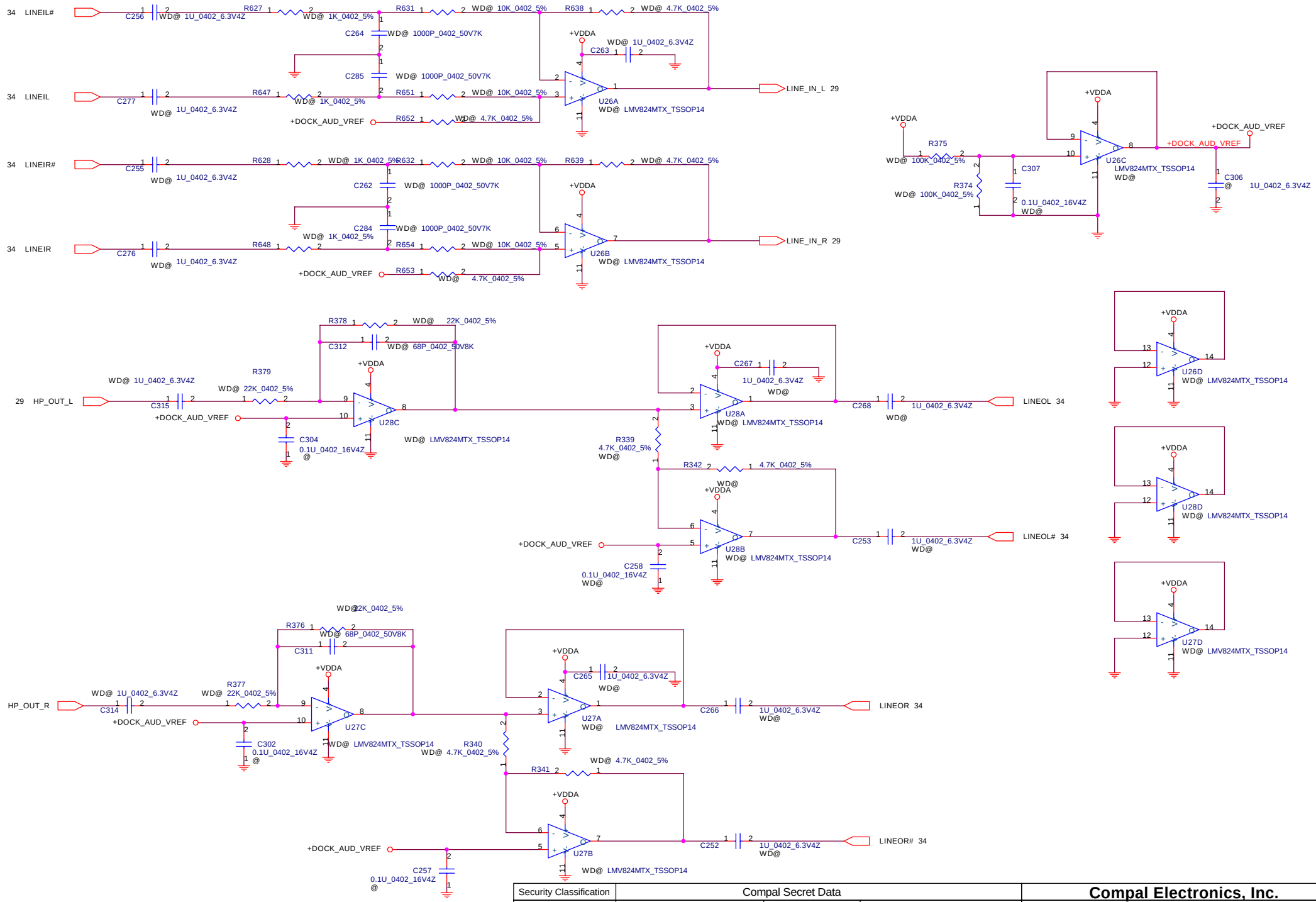


**Compal Electronics, Inc.**

Title: ***AMP & Audio Jack***

| Size | Document Number | Rev |
|---|---|---|
| | ***LA-3011P*** | 0.2 |

Date: Thursday, September 15, 2005 Sheet 30 of 48




PROPRIETARY NOTE

| | | | |
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| Issued Date | 2005/04/25 | Deciphered Date | 2006/06/01 |

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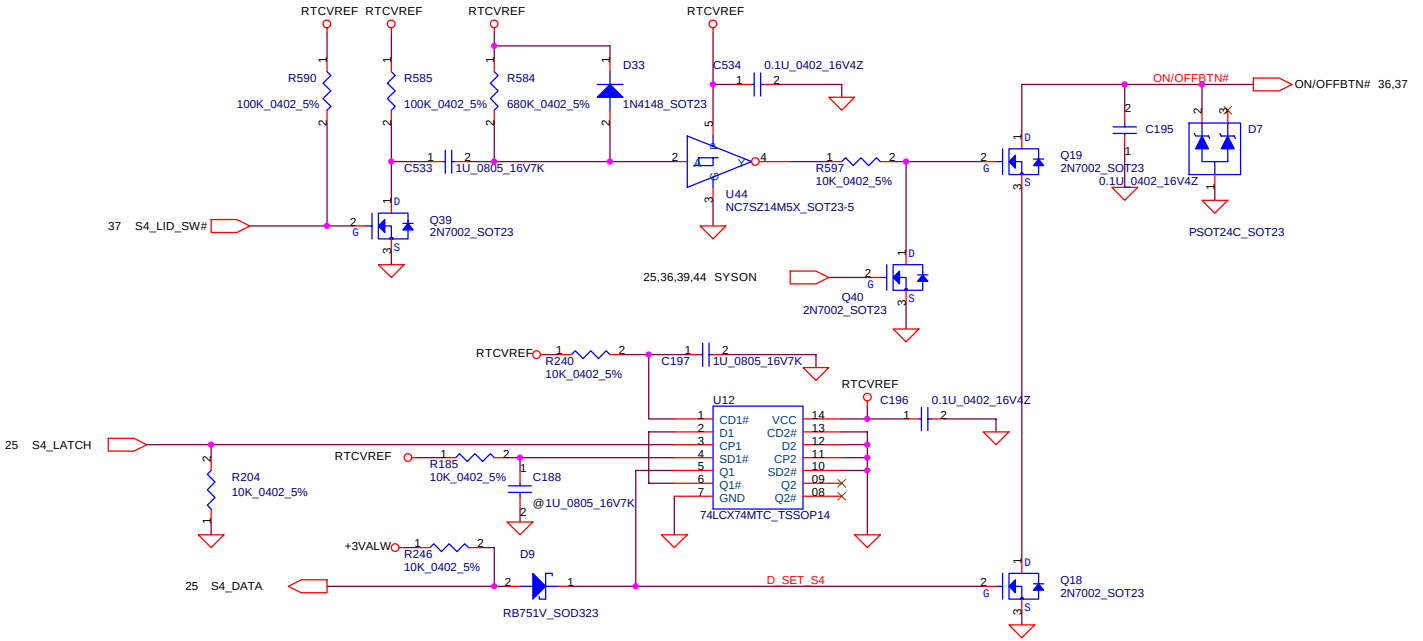
**Compal Electronics, Inc.**

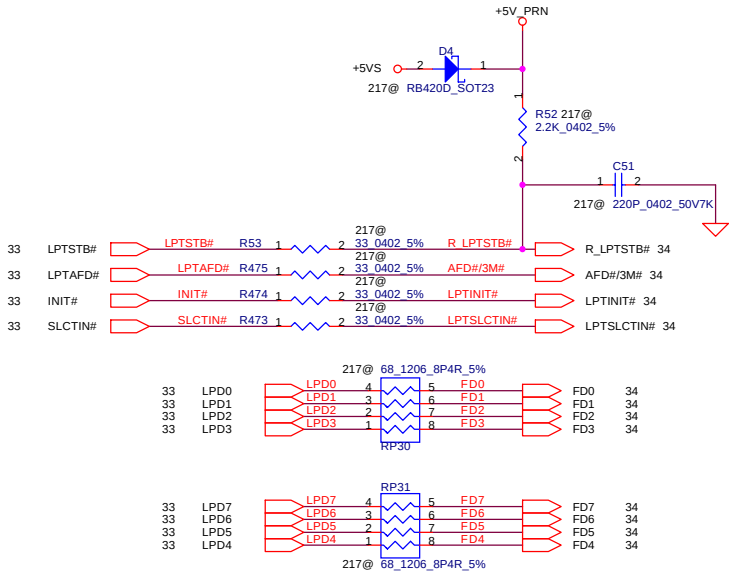
Title: ***Docking Audio***

Size | Document Number: ***LA-3011P*** | Rev: 0.2

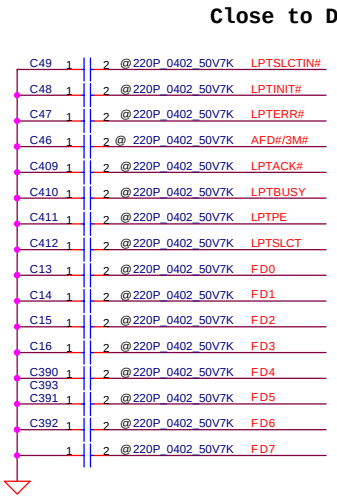
Date: Thursday, September 15, 2005 | Sheet 31 of 48



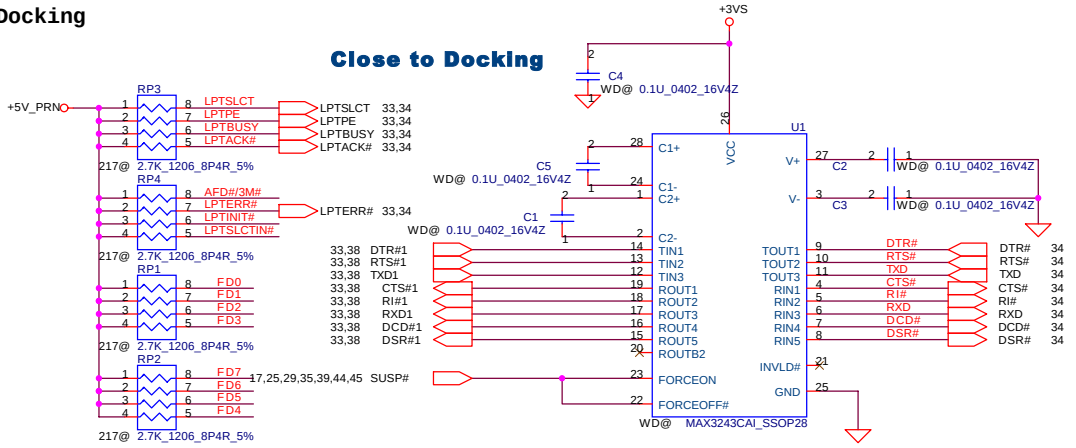

## Docking Parallel Port




## Close to Docking




## Close to Docking

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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/04/25 | Deciphered Date | 2006/06/01 |



**Compal Electronics, Inc.**

Title: ***COM/PARALLEL***

| Size | Document Number | Rev |
|---|---|---|
| | ***LA-3011P*** | 0.2 |

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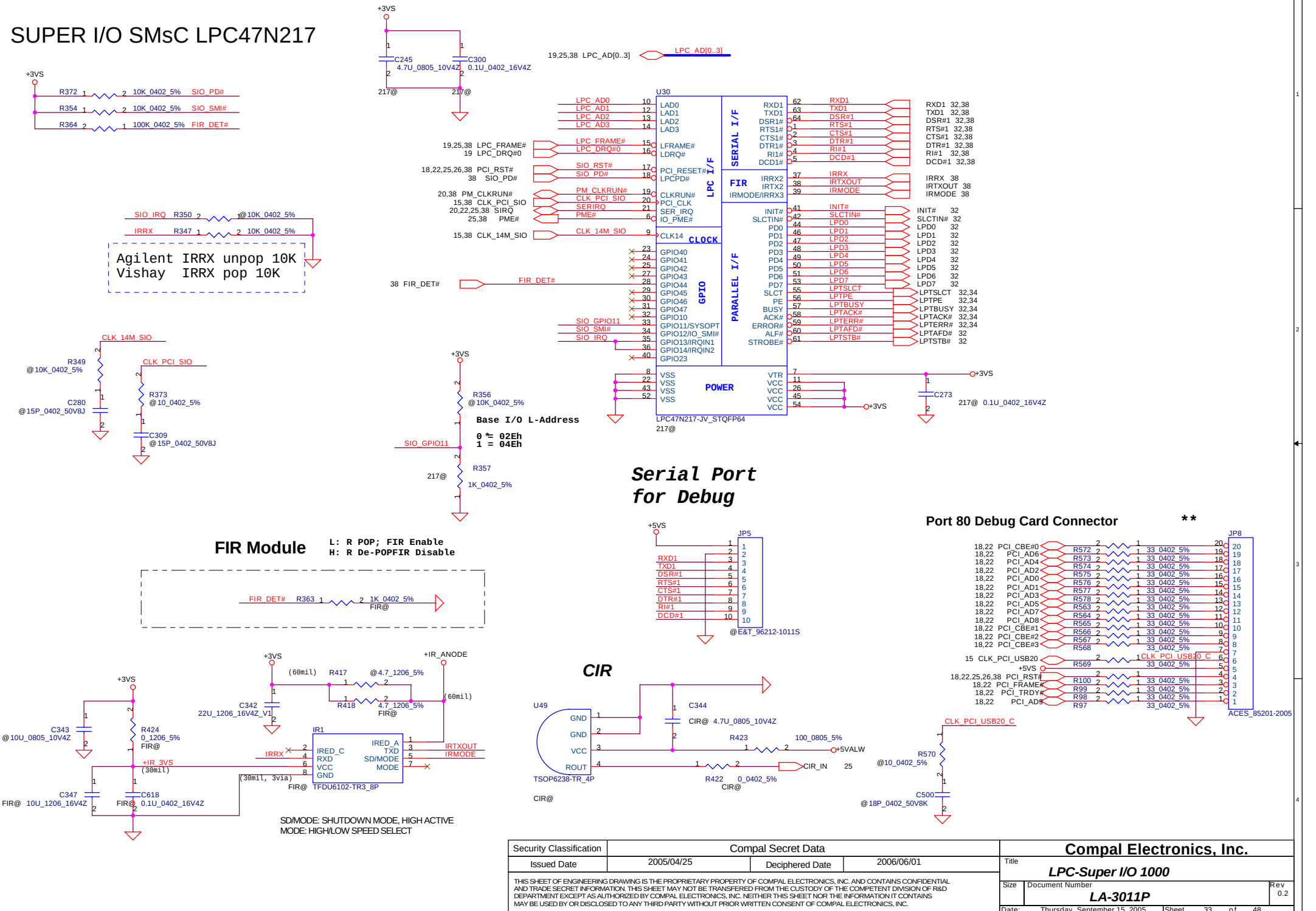
# SUPER I/O SMsC LPC47N217




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/04/25 | Deciphered Date | 2006/06/01 |



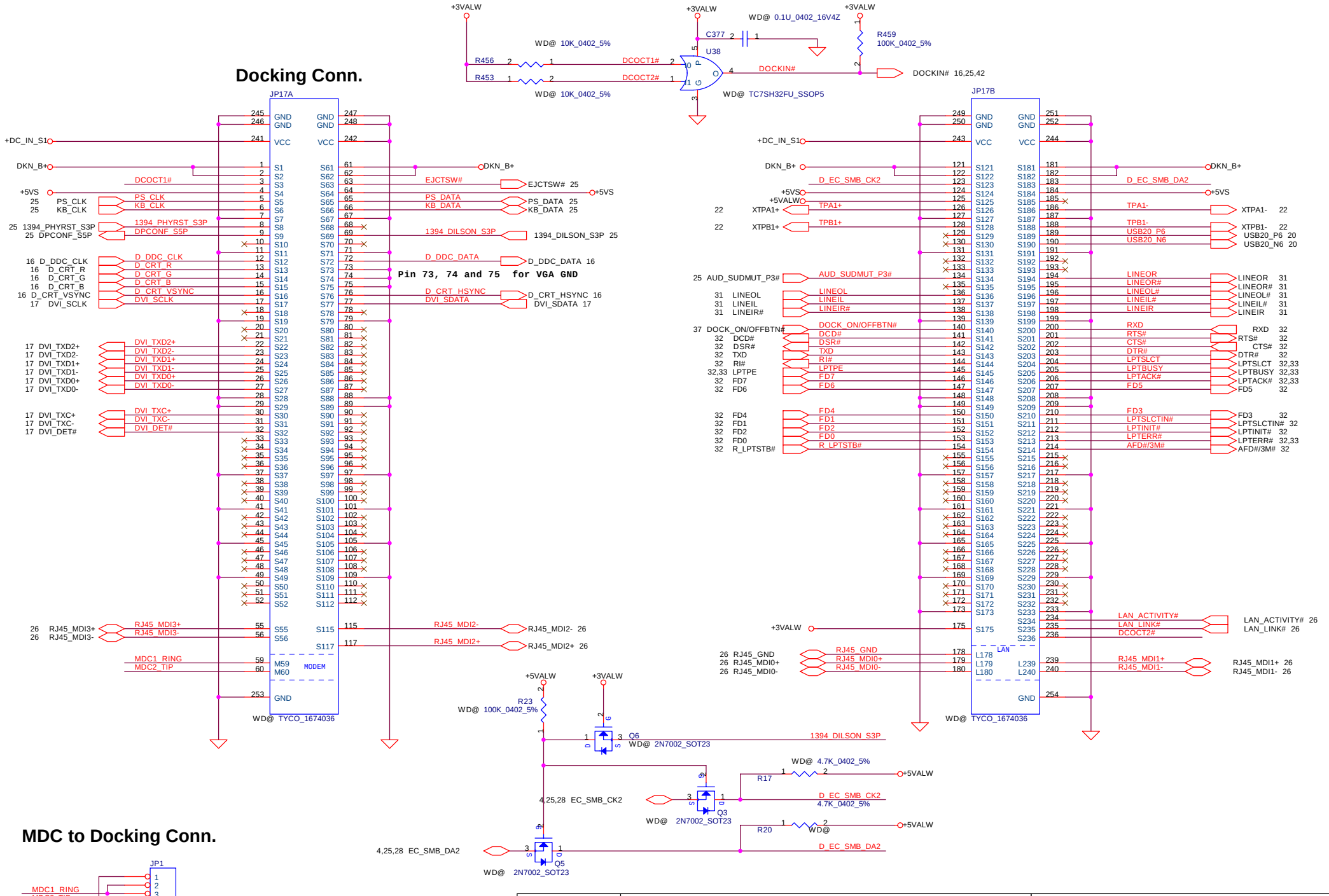
**Compal Electronics, Inc.**

Title: *LPC-Super I/O 1000*

| Size | Document Number | Rev |
|---|---|---|
| | *LA-3011P* | 0.2 |

Date: Thursday, September 15, 2005 Sheet 33 of 48

# Docking Conn.




# MDC to Docking Conn.




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2005/06/01 | Deciphered Date | 2006/06/01 |

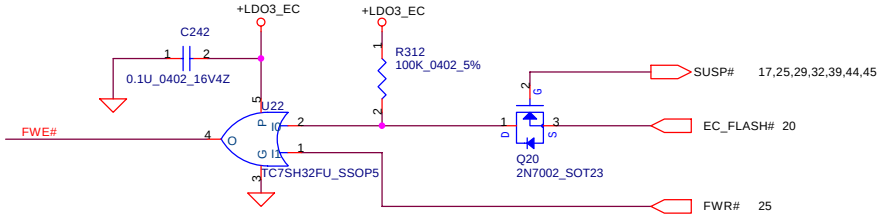


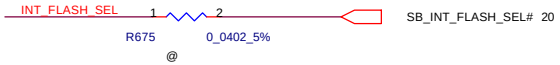
**Compal Electronics, Inc.**

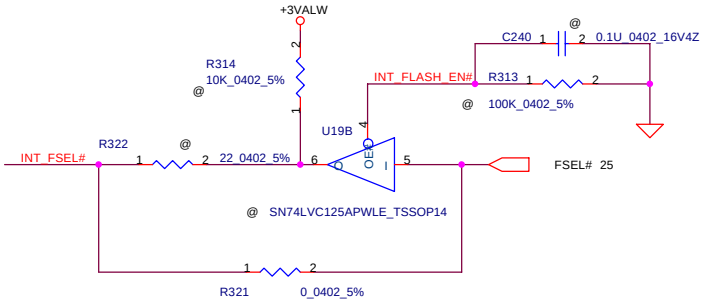
Title: ***Docking***

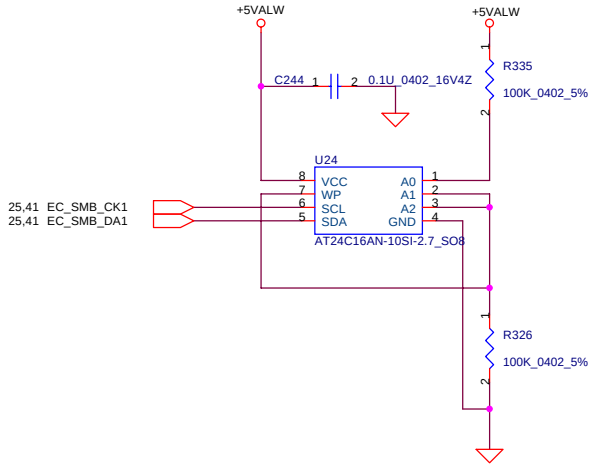
Size | Document Number: ***LA-3011P*** | Rev: 0.2

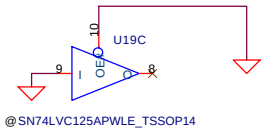
Date: Thursday, September 15, 2005 | Sheet 34 of 48

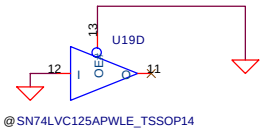


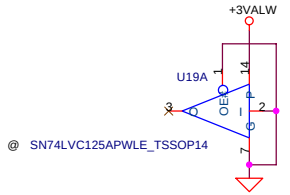



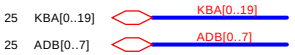



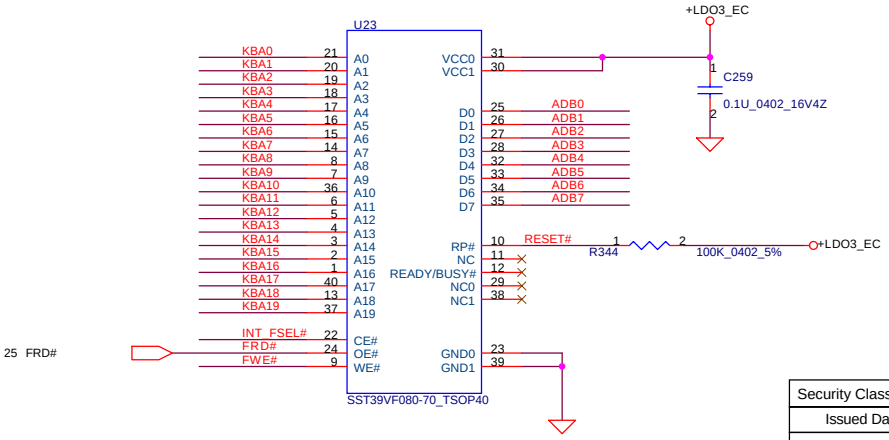



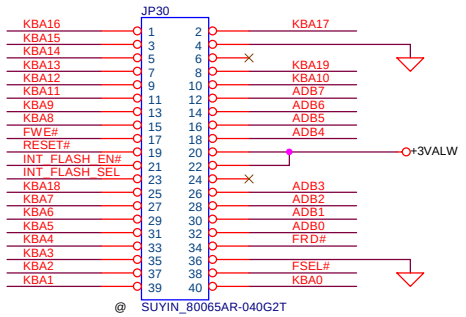




## 1MB Flash ROM




## 1MB ROM Socket




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/01 | Deciphered Date | 2006/06/01 |

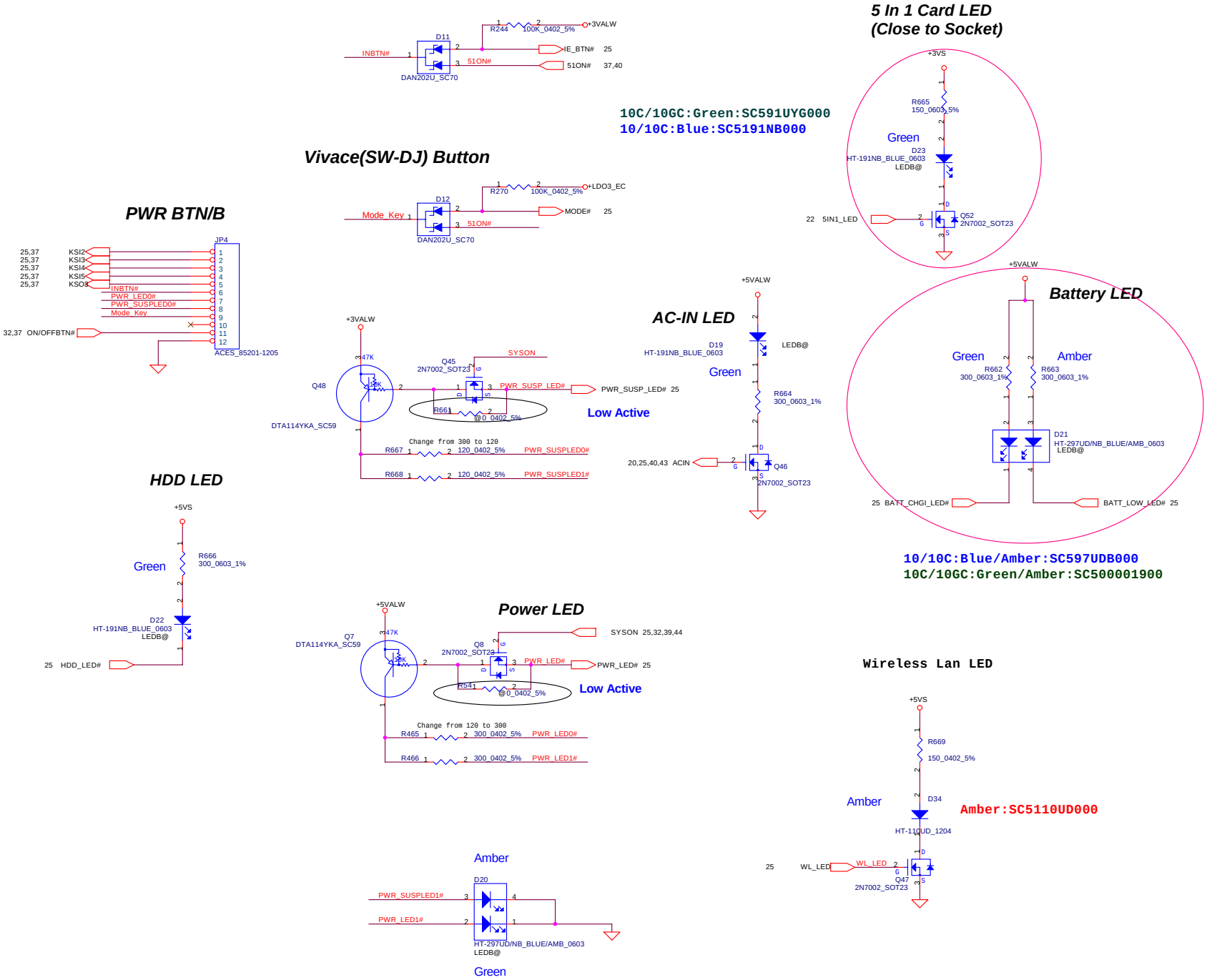


**Compal Electronics, Inc.**

Title: ***BIOS & EXT. I/O PORT***

| Size | Document Number | Rev |
|---|---|---|
| | ***LA-3011P*** | 0.2 |

Date: Thursday, September 15, 2005 | Sheet 35 of 48




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/01 | Deciphered Date | 2006/06/01 |



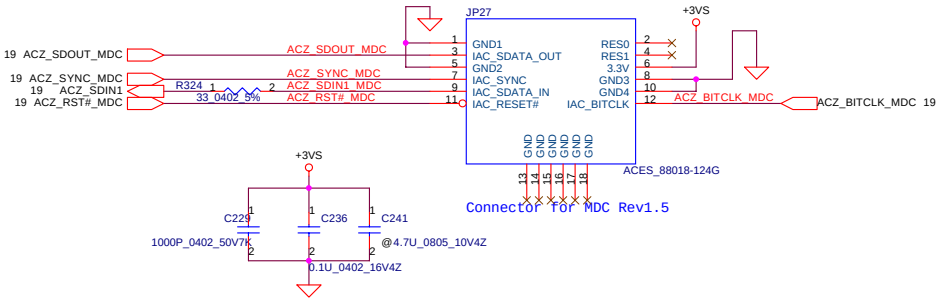
**Compal Electronics, Inc.**

Title: *MDC/BT/KBD/ON_OFF/LID*

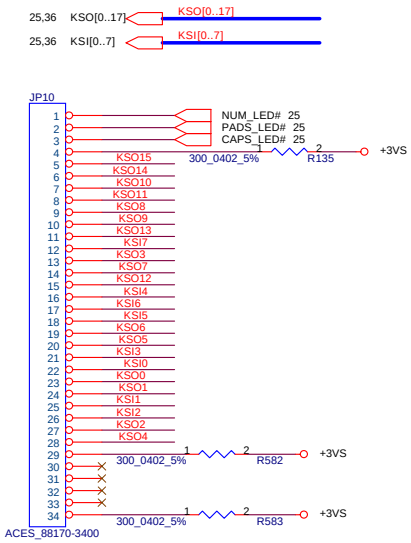
| Size | Document Number | Rev |
|---|---|---|
| | *LA-3011P* | 0.2 |

Date: Thursday, September 15, 2005 | Sheet 36 of 48

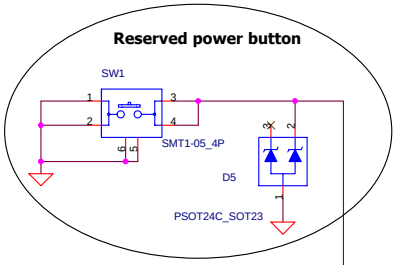
# MDC 1.5 Conn.



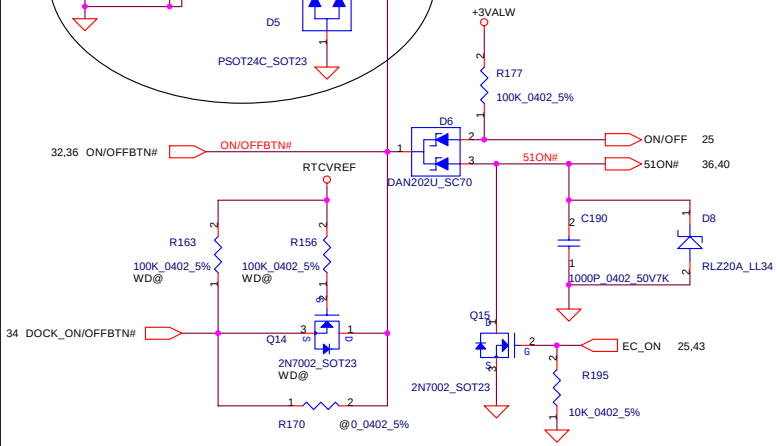

# INT_KBD CONN.



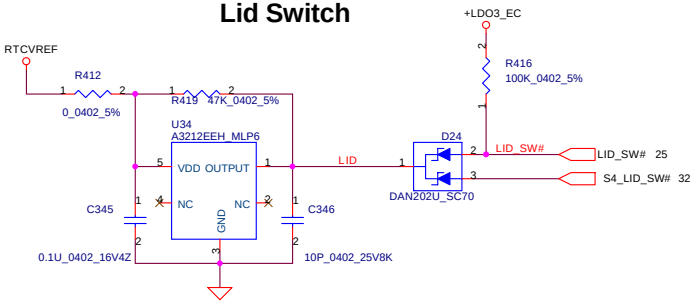

## Reserved power button

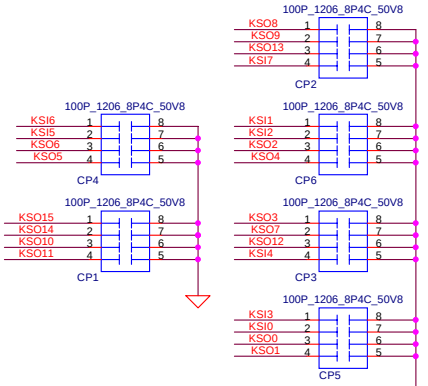



## Power Button

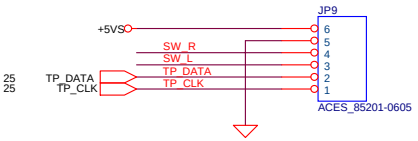



## Lid Switch

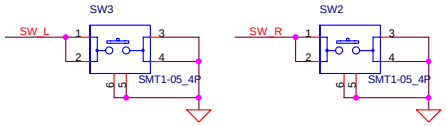



## TP CONN.




## TP Button



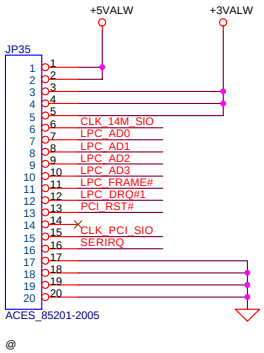

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/01 | Deciphered Date | 2006/06/01 |



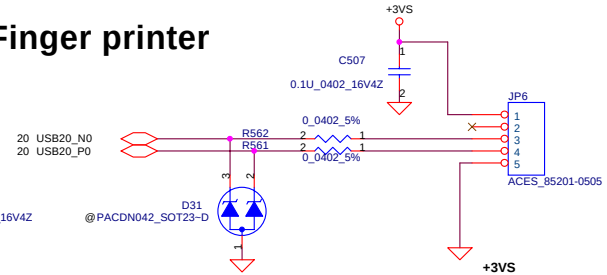
| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | MDC/KBD/ON_OFF/LID |
| Size | Document Number: LA-3011P |
| Rev | 0.2 |
| Date: Friday, September 16, 2005 | Sheet 37 of 48 |

# SUPER I/O SMsC LPC47N207

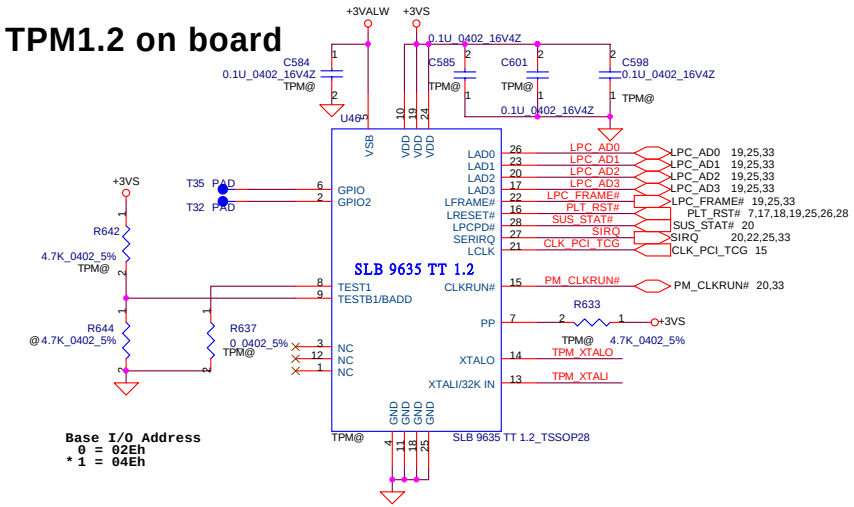
## LPC Debug Port

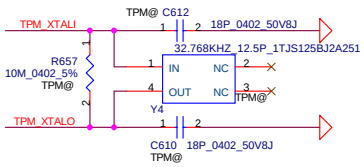


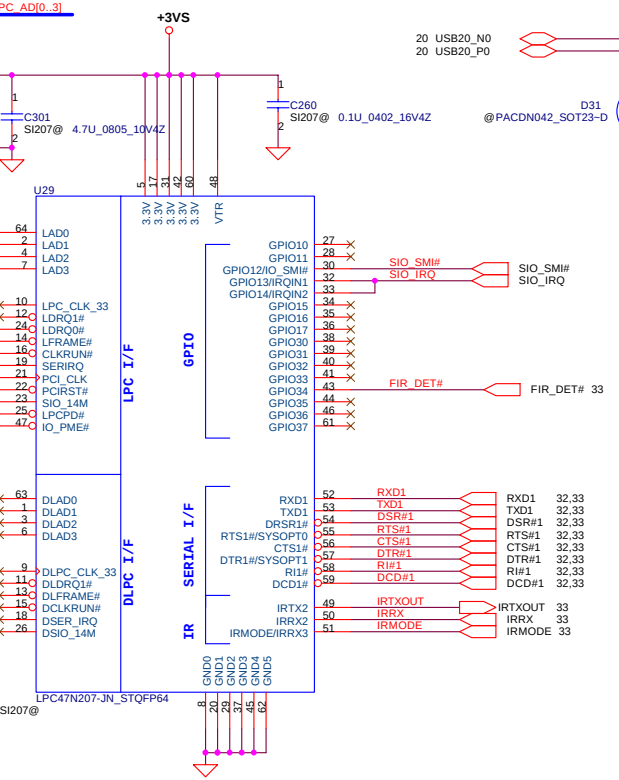

## Finger printer

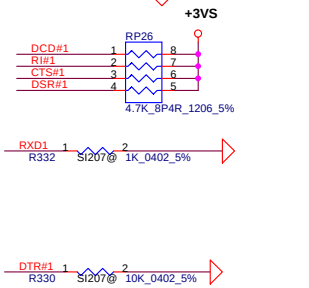


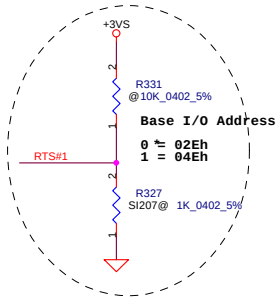

## TPM1.2 on board

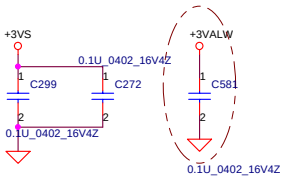


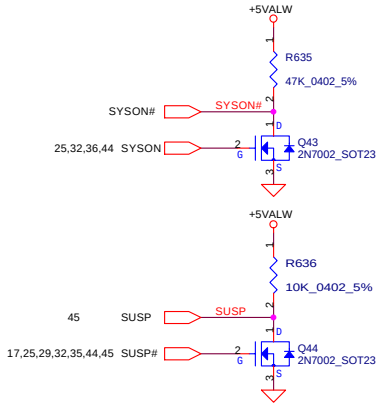



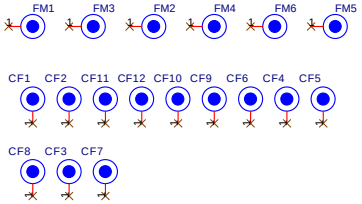



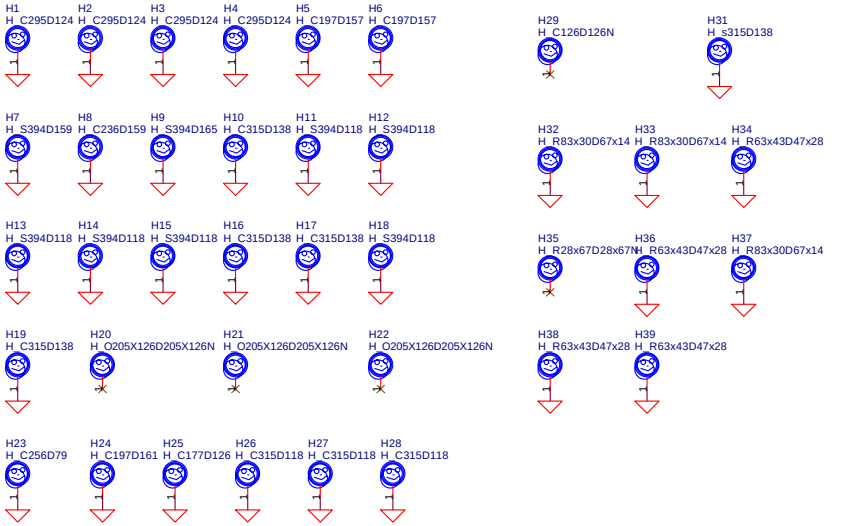

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/01 | Deciphered Date | 2006/06/01 |



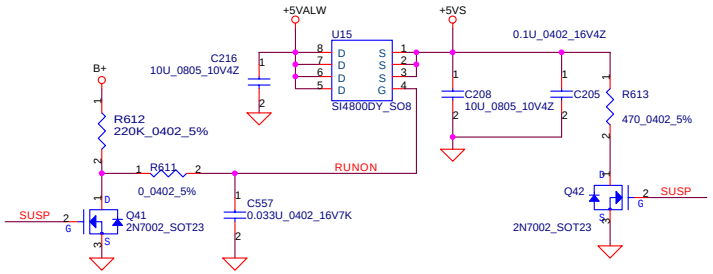
| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | TCG/BIOS ROM/PS2/LED/SW |
| Size | Document Number: LA-3011P |
| Rev | 0.2 |
| Date: Thursday, September 15, 2005 | Sheet 38 of 48 |



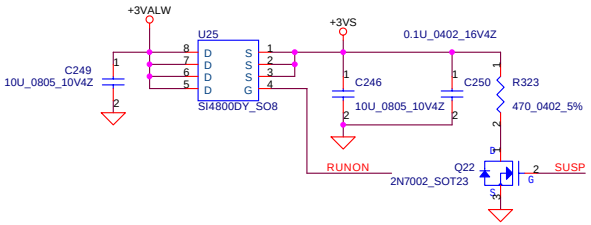



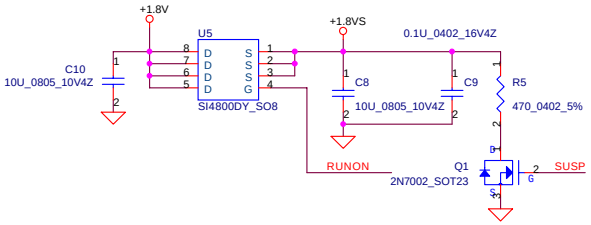

### +5VALW to +5VS Transfer

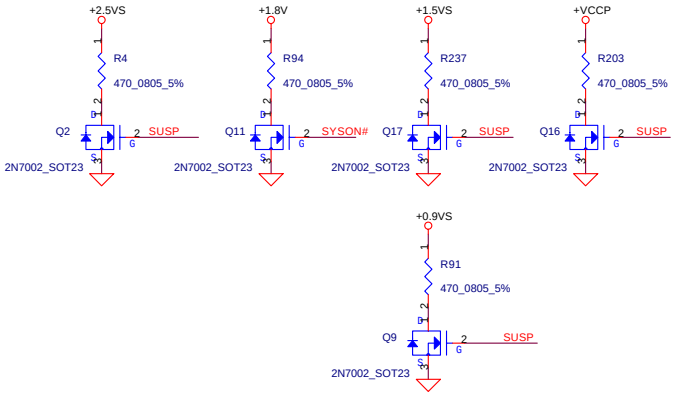



### +3VALW to +3VS Transfer




### +1.8V to +1.8VS Transfer

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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/01 | Deciphered Date | 2006/06/01 |

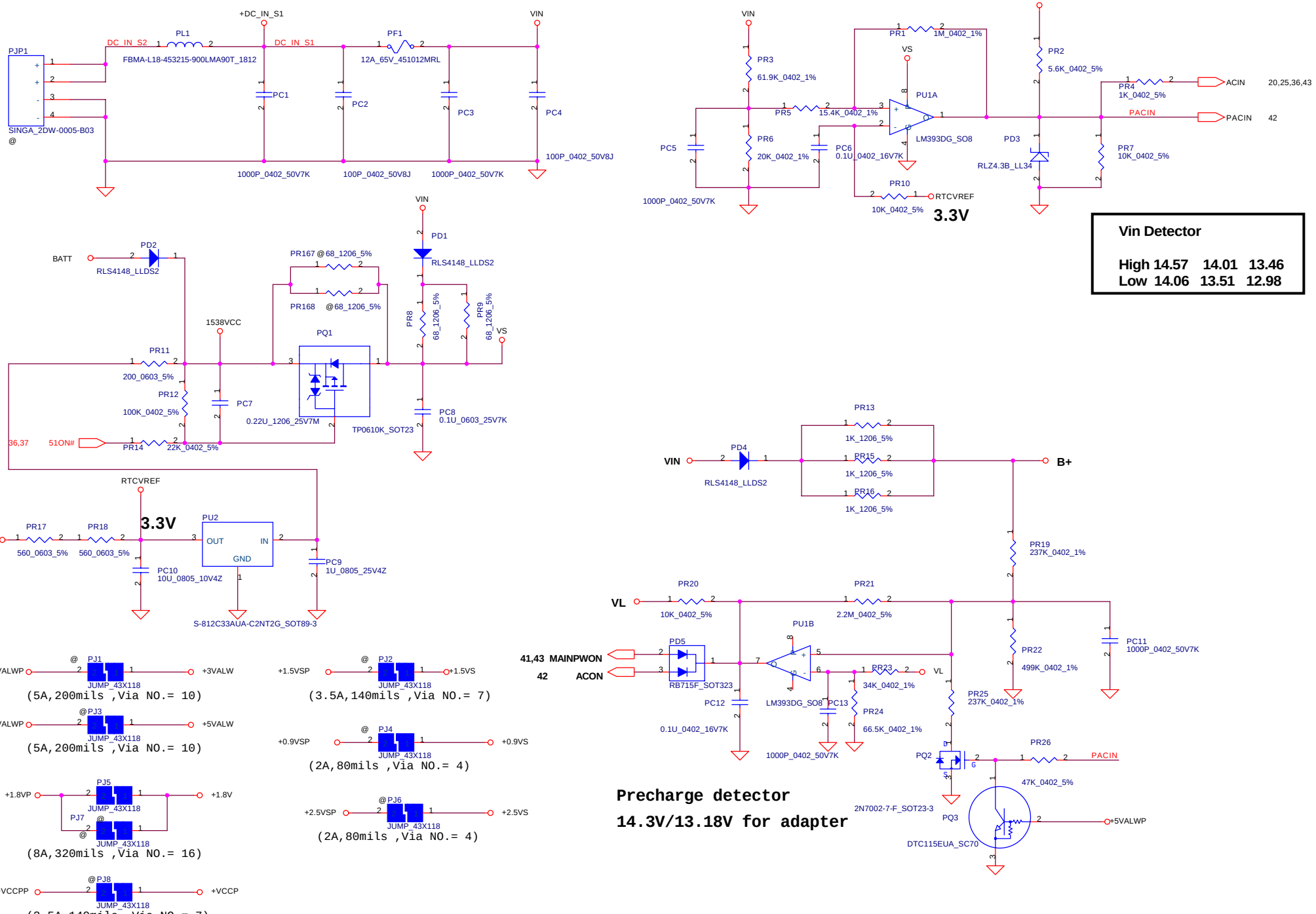


**Compal Electronics, Inc.**

Title: **DC/DC Circuits**

| Size | Document Number | Rev |
|---|---|---|
| | LA-3011P | 0.2 |

Date: Thursday, September 15, 2005 | Sheet 39 of 48




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/23 | Deciphered Date | 2006/06/23 |



**Compal Electronics, Inc.**

Title: DCIN & DETECTOR

| Size | Document Number | Rev |
|---|---|---|
| B | LA-3011P | 0.2 |

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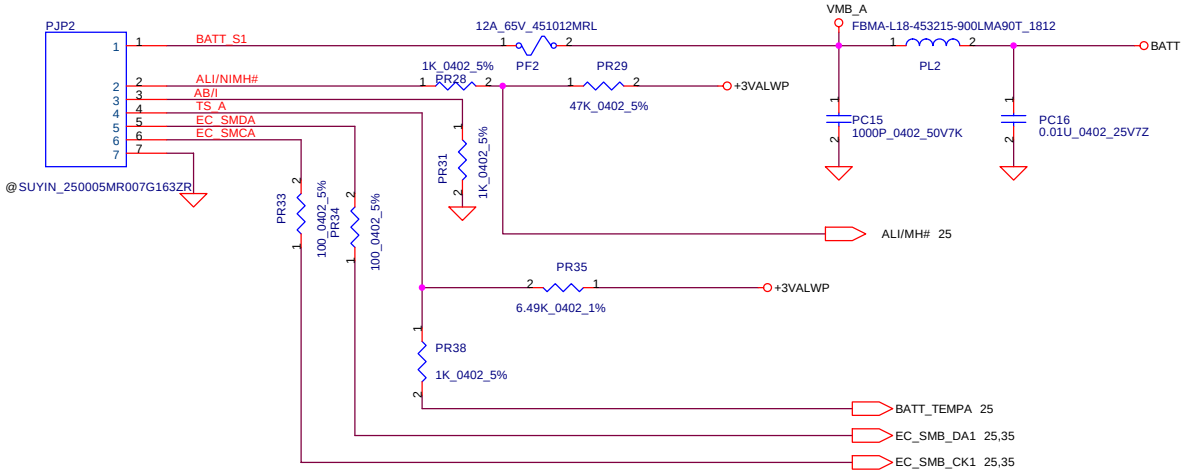
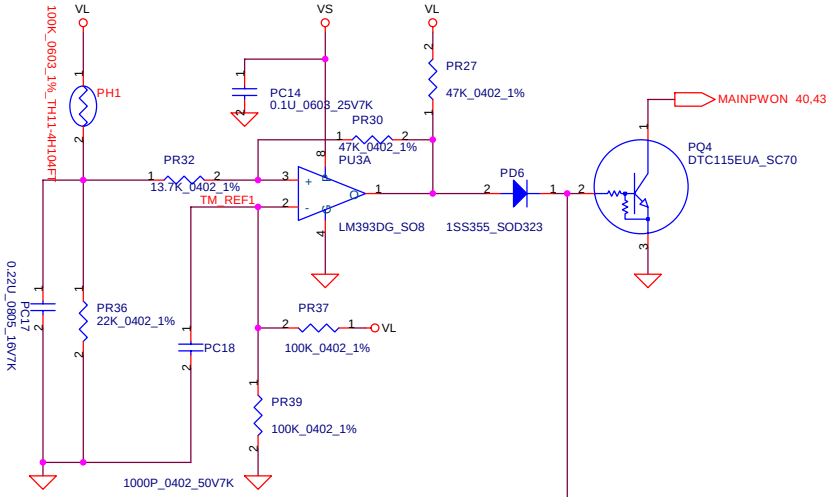
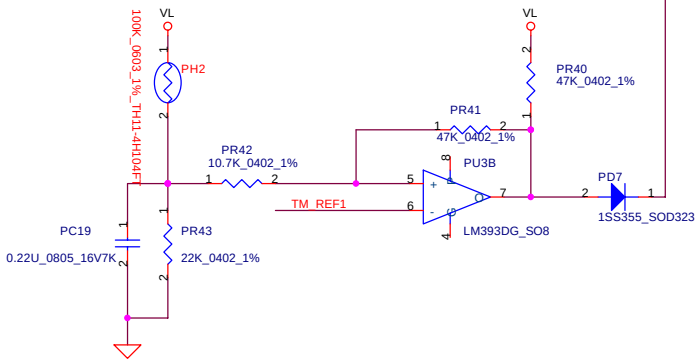
**PH1 under CPU botten side :**
CPU thermal protection at 84 degree C
Recovery at 45 degree C




**PH2 near main Battery CONN :**
BAT. thermal protection at 79 degree C
Recovery at 45 degree C

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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/23 | Deciphered Date | 2006/06/23 |

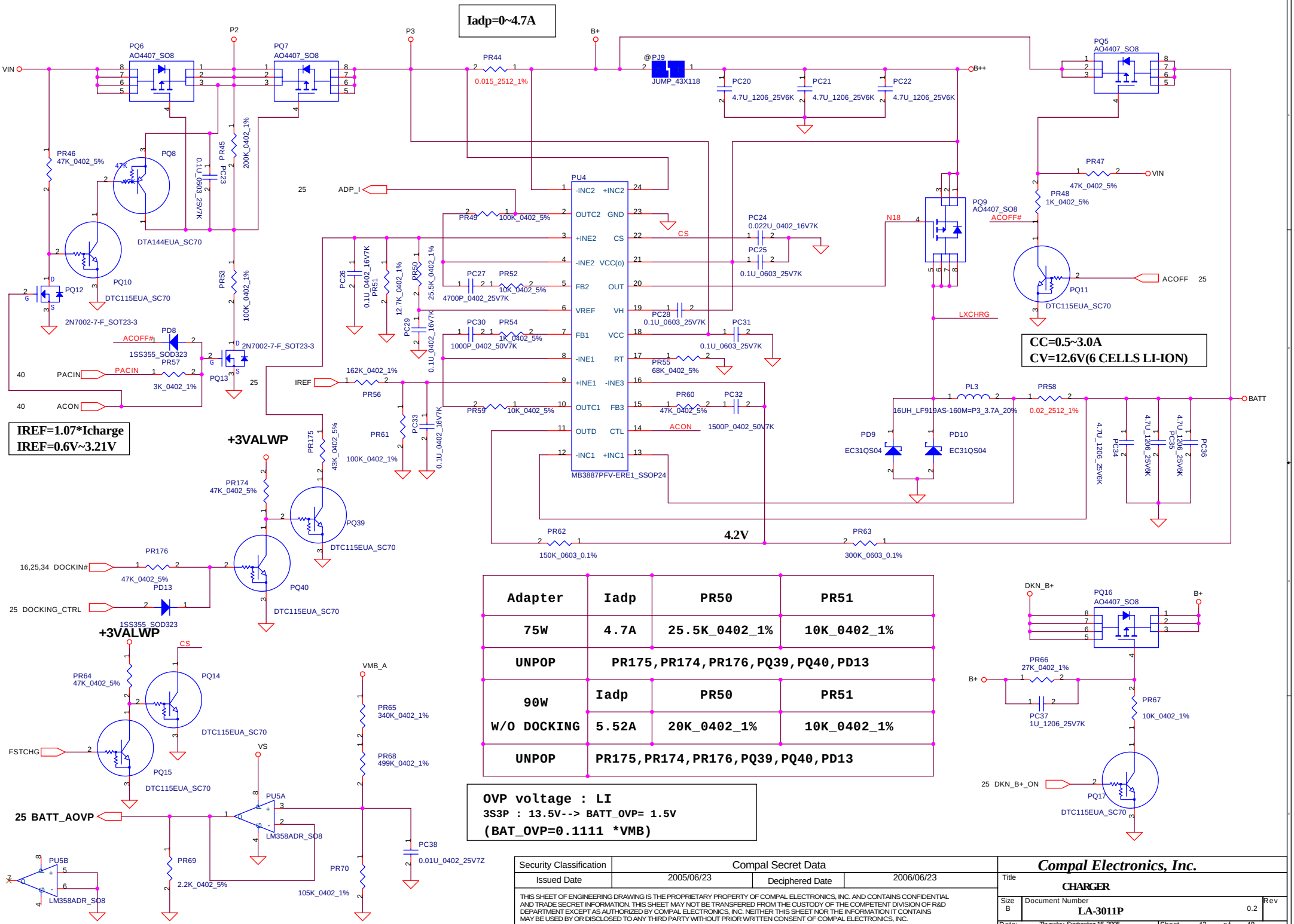


**Compal Electronics, Inc.**

Title: **BATTERY CONN /OTP**

| Size | Document Number | Rev |
|---|---|---|
| B | **LA-3011P** | 0.2 |

Date: Thursday, September 15, 2005 Sheet 41 of 48




| Adapter | Iadp | PR50 | PR51 |
|---|---|---|---|
| 75W | 4.7A | 25.5K_0402_1% | 10K_0402_1% |
| UNPOP | PR175,PR174,PR176,PQ39,PQ40,PD13 | | |
| 90W W/O DOCKING | Iadp | PR50 | PR51 |
| | 5.52A | 20K_0402_1% | 10K_0402_1% |
| UNPOP | PR175,PR174,PR176,PQ39,PQ40,PD13 | | |

OVP voltage : LI
3S3P : 13.5V--> BATT_OVP= 1.5V
(BAT_OVP=0.1111 *VMB)

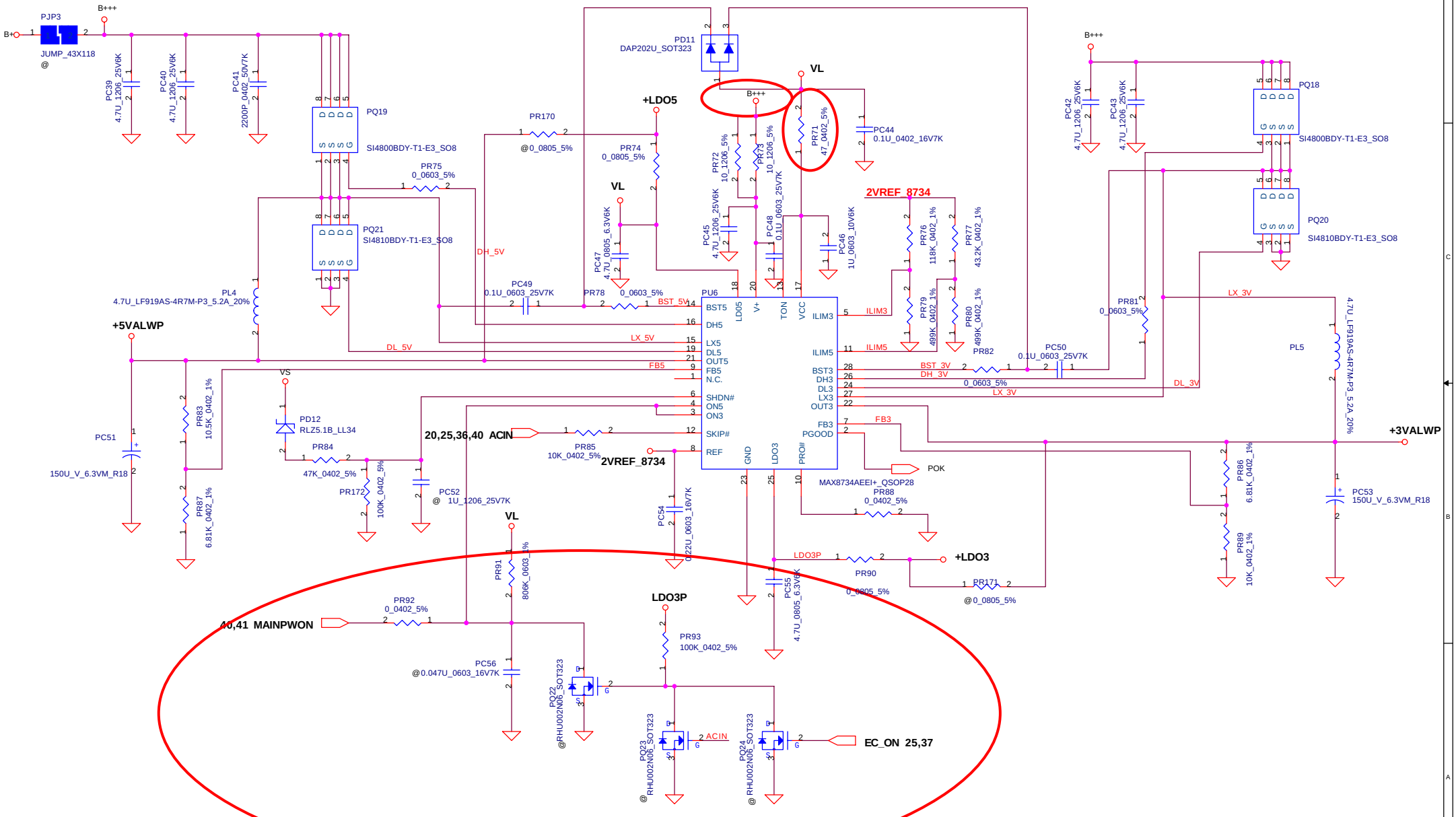
| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/23 | Deciphered Date | 2006/06/23 |



**Compal Electronics, Inc.**

| | | |
|---|---|---|
| Title | CHARGER | |
| Size B | Document Number LA-3011P | Rev 0.2 |
| Date: Thursday, September 15, 2005 | Sheet 42 of 48 | |

# +3.3VALWP/+5VALWP

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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/23 | Deciphered Date | 2006/06/23 |

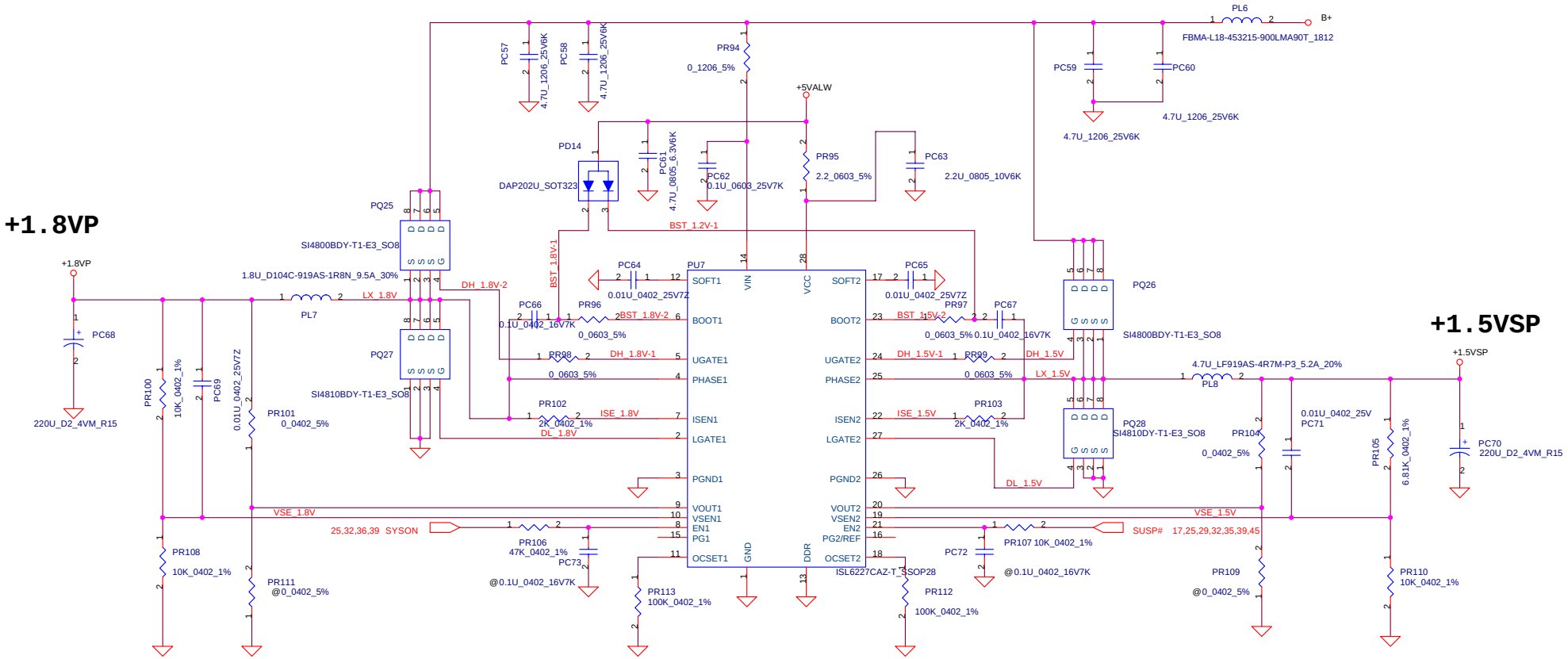


**Compal Electronics, Inc.**

Title: +5V/+3V

Size: Custom | Document Number: LA-3011P | Rev: 0.2

Date: Thursday, September 15, 2005 | Sheet 43 of 48




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/23 | Deciphered Date | 2006/06/23 |

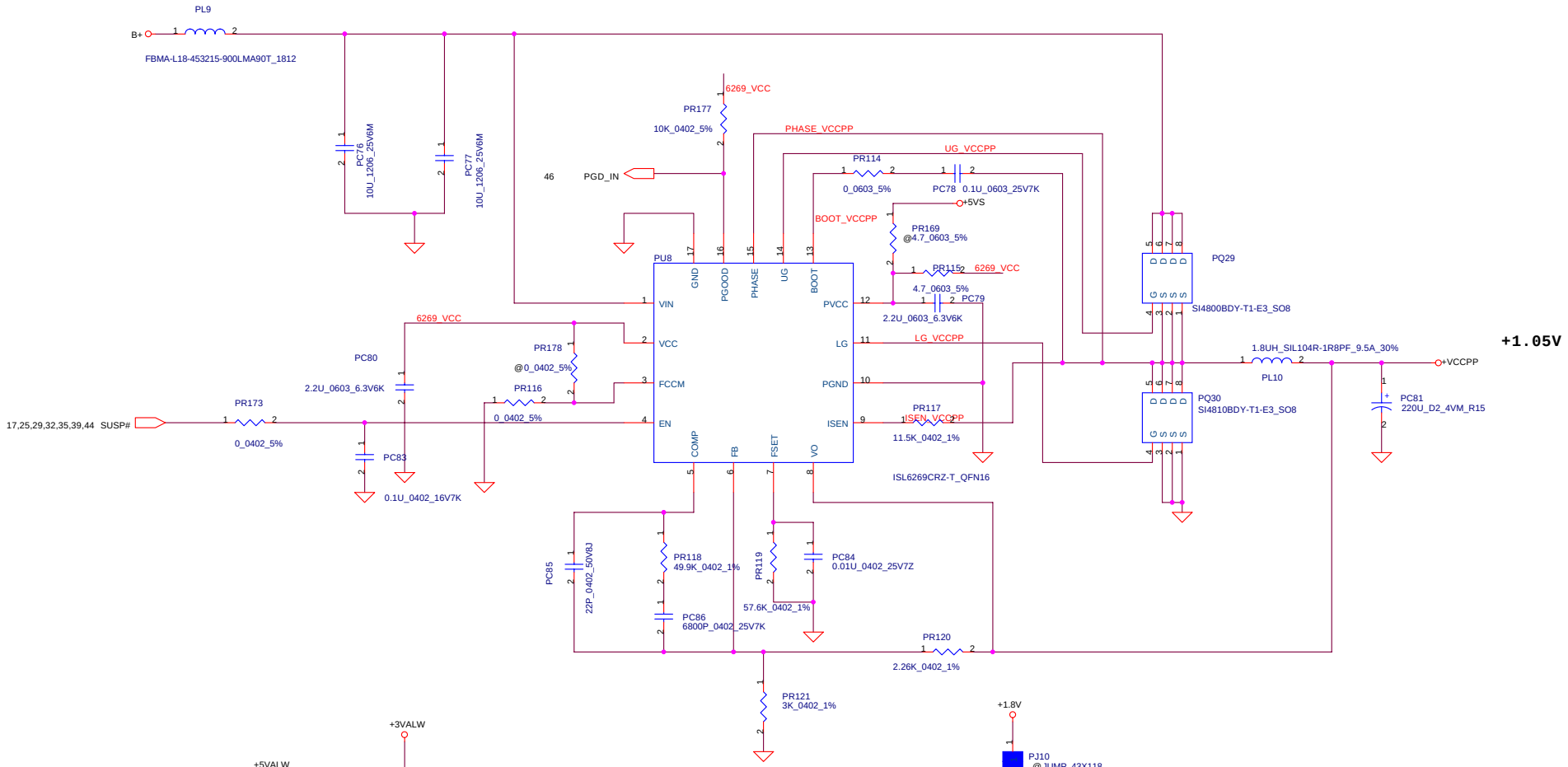


**Compal Electronics, Inc.**

Title: **+1.8V/+1.5V**

Size: Custom | Document Number: **LA-3011P** | Rev: 0.2

Date: Thursday, September 15, 2005 | Sheet 44 of 48




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/23 | Deciphered Date | 2006/06/23 |

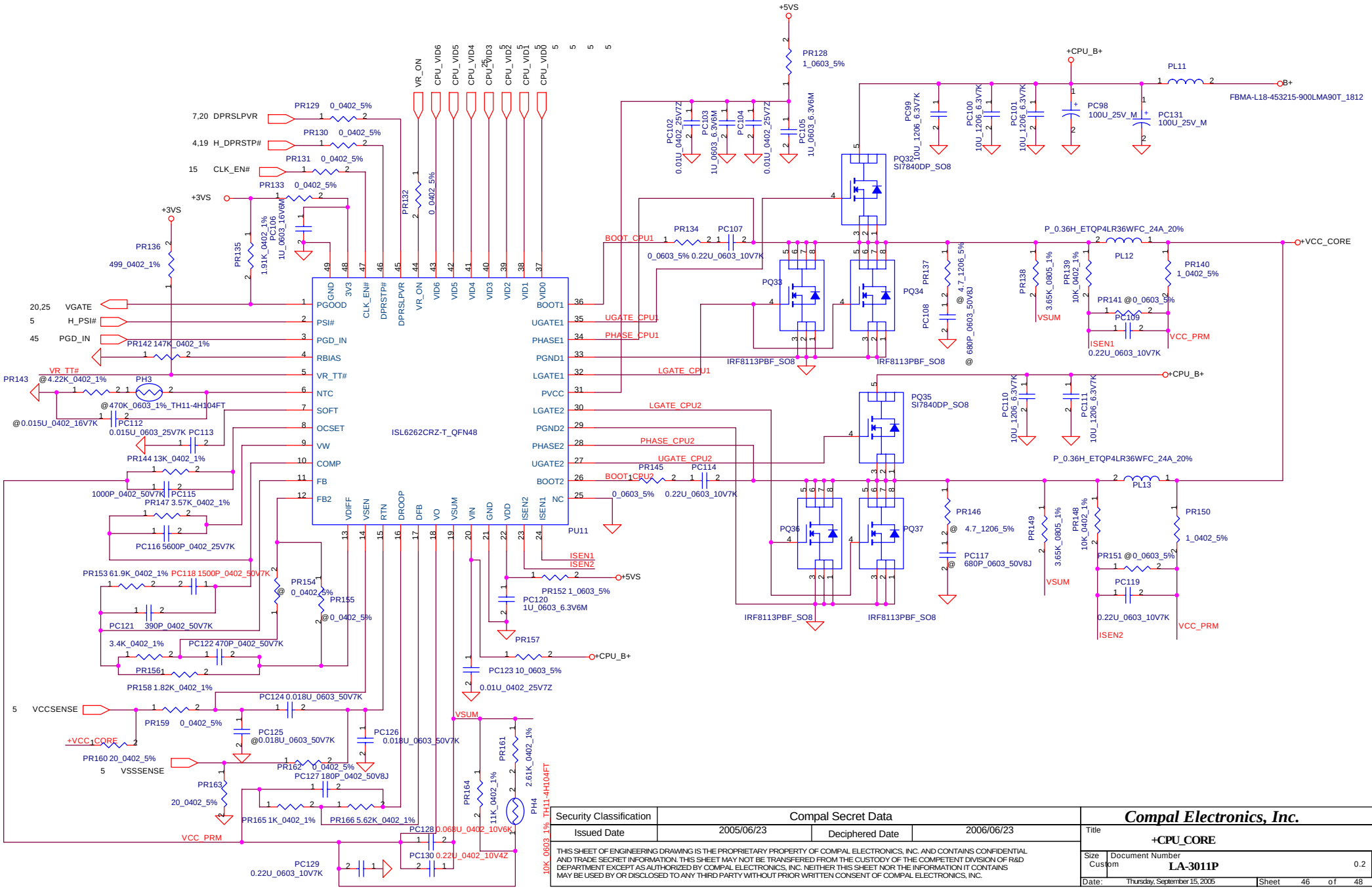


**Compal Electronics, Inc.**

Title: **+VCCPP/+2.5VSP/0.9VSP**

Size: Custom | Document Number: **LA-3011P** | Rev: 0.2

Date: Thursday, September 15, 2005 | Sheet 45 of 48




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/06/23 | Deciphered Date | 2006/06/23 |



**Compal Electronics, Inc.**

Title: +CPU_CORE

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-3011P | 0.2 |

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| NO | DATE | PAGE | MODIFICATION LIST | PURPOSE |
|---|---|---|---|---|
| 8/8 | | P.15 | Delete R589,R181,R190 | No reserve those resistors |
| 8/10 | | P.30 | Add D35,R671 | for G_beep function |
| 8/10 | | P.25 | Swap EC pin8 and Pin42 | for G_beep function |
| 8/11 | | P.30 | Del R659,C613& Add D36 | for G_beep function |
| 8/16 | | P.7 | unmount R503, R519 | Intel Request |
| 8/16 | | P.9 | unmount R480, R478 | Intel Request |
| 8/16 | | P.11 | unmount R514 | Intel Request |
| 8/16 | | P.20 | Mount R249, Add R672,R673,R674 | Intel Request |
| 8/19 | | P.35 | Add R675 | For BIOS debug port |
| 8/19 | | P.39 | Modify R611, C557 | For RUNON timing sequence |
| 8/22 | | P.7 | Add R676 | Reserve for TS on SODIMM |
| 8/22 | | P.28 | Del U10,R128,R134,C162,C164,C169,C174,C175 | Change G-sensor |
| 8/23 | | P.28 | Add C619,C620,C621,C622,C623,C624,C625,C626,C627 | |
| 8/23 | | P.28 | Add R677,R678,R679,R680,R681,R682,R683,R684,R685,R686 | |
| 8/23 | | P.28 | Del x_sensor, y_sensor, z_sensor connection to EC | G-sensor circuit modification |
| 8/23 | | P.28 | Add Q49,Q50,U50,U51,U52,Y5 | For New G-sensor solution |
| 8/24 | | P.17 | Change JP18.40 to +5VALW | |
| 8/24 | | P.29 | Change U33.8 to SUSP# | |
| 8/24 | | P.29 | Change U33.8 to SUSP# | |
| 8/25 | | P.16 | Change D27,D28,D29 pin 3 to +2.5VS | for Intel's suggestion |
| 8/25 | | P.37 | Change JP9 connector to 6pin | To meet ME's definition |
| 8/25 | | P.15 | J10 change to Jump 43*79 | for DFX request |
| 8/25 | | P.19 | CMOS_CLR1 change to Jump 43*79 | for DFX request |
| 8/30 | | P.39 | Modify Screw holw location | |
| 8/30 | | P.22 | To correct MSBS_SDCMD_SMWE#/SDWP#_SMCE# signals | |
| 8/30 | | P.39 | Change R612=220K,C557=0.033uF,R611=0ohm | for power on sequence |
| 9/2 | | P.29 | Add EC_HDPPD to U14.24 and R682 | G-sensor circuit modification |
| 9/5 | | P.09 | Swap CRT_R & CRT_B | To fix CRT issue of GM |
| 9/8 | | P.20 | Change LAN_Disable from GPIO15 to GPIO28 | |
| 9/9 | | P.26 | Swap RX /TX signals | |
| 9/9 | | P.25 | Swap EC pin8 & Pin42 | for follow EVT pin definition |
| 9/9 | | P.29/30 | To separate Line out and HP signals | |
| 9/12 | | P.30 | D35/D36 change to Diode 4148 | |
| 9/12 | | P.30 | Add R687 ,Q51 | |
| 9/12 | | P.29 | Add R688,C628 | |
| 9/12 | | P.24 | Change JP34 connector to ACES_87213-1000 | |
| 9/12 | | P.29 | Delete R395 | |
| 9/12 | | P.16 | Change F1 to SP04301P000 | |
| 9/13 | | P.38 | Reserve SIO_SMI#/SIO_IRQ signals | |
| 9/13 | | P.38 | Reserve JP35 for BIOS debug | |
| 9/14 | | P.22 | Add Q52 for 5in1 LED | |

**NB**

U6
945GM
GM@

**LAN**

U41
82573E
82573E@

U41
82562
82562@

**TRANSFORMER**

T1
TST1284B-LF
82562@

**PCB**

ZZZ
PCB ZKU LA-3011P REV0

**CARDBUS**

U13
PCI8412
PCI8412@

**Green LED**

D20
HT-297DQ/GQ AMB/YG
LEDG@

D21
HT-297DQ/GQ AMB/YG
LEDG@

D19
HT-191UYG-DT YEL/GRN
LEDG@

D22
HT-191UYG-DT YEL/GRN
LEDG@

D23
HT-191UYG-DT YEL/GRN
LEDG@

**CAP for LAN**

C19
0.01U
82562@

C22
0.01U
82562@

| | | |
|---|---|---|
| Title: ISPD | | |
| Size: B | Document Number: LA-2621 | Rev: 0.3 |
| Date: Thursday, September 15, 2005 | Sheet 48 of 48 | |