NBWAA

Low Cost Los Angeles 10L

LA-5821P REV 1.0 Schematics

Intel Penryn/ Cantiga/ ICH9M

2008-08-10 Rev. 1.0

Security Classification	Compal Secret Data		
Issued Date	2009/07/28	Deciphered Date	2010/07/28

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Model Name : NBWAA
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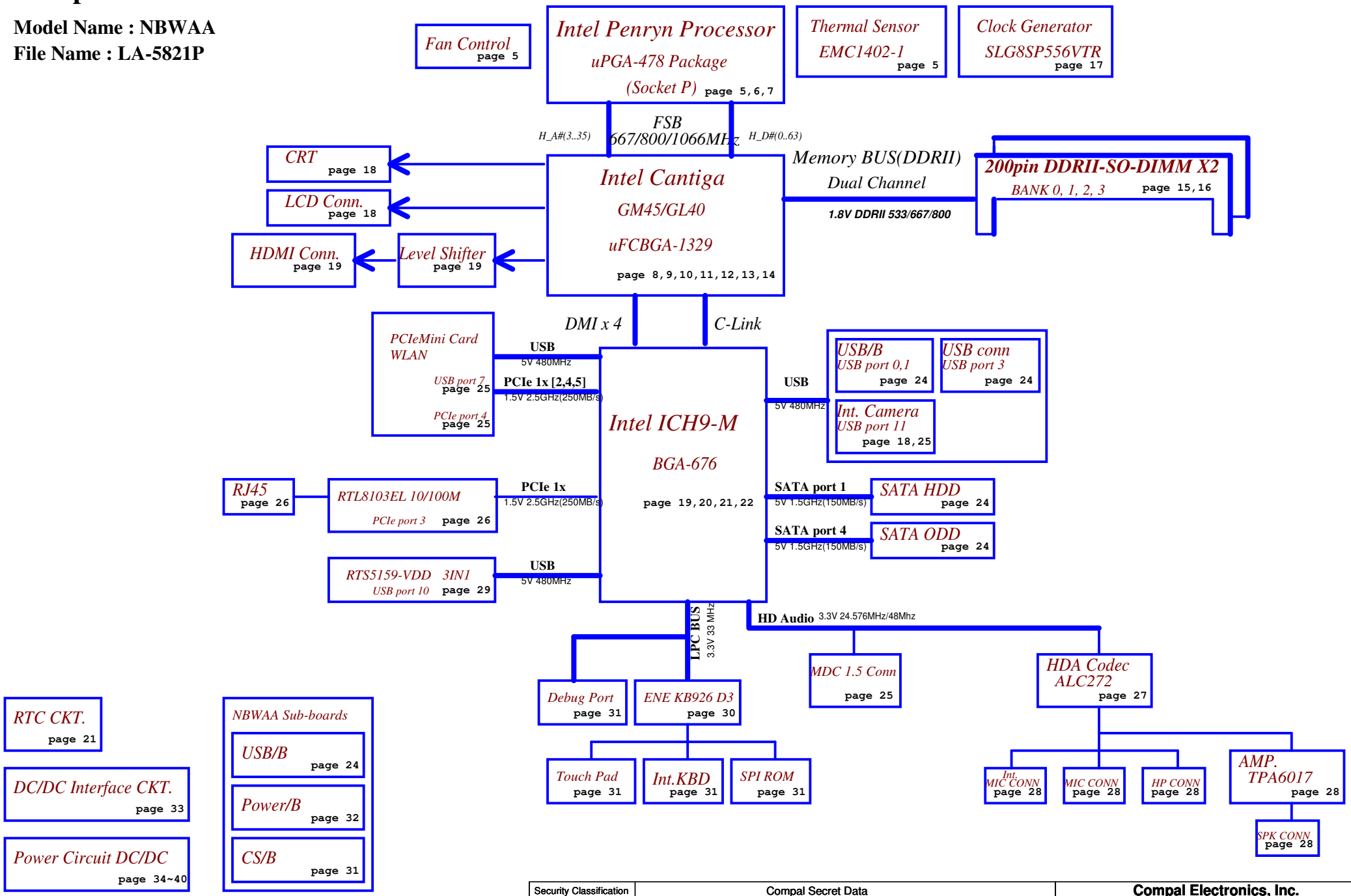

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Title: Block Diagrams

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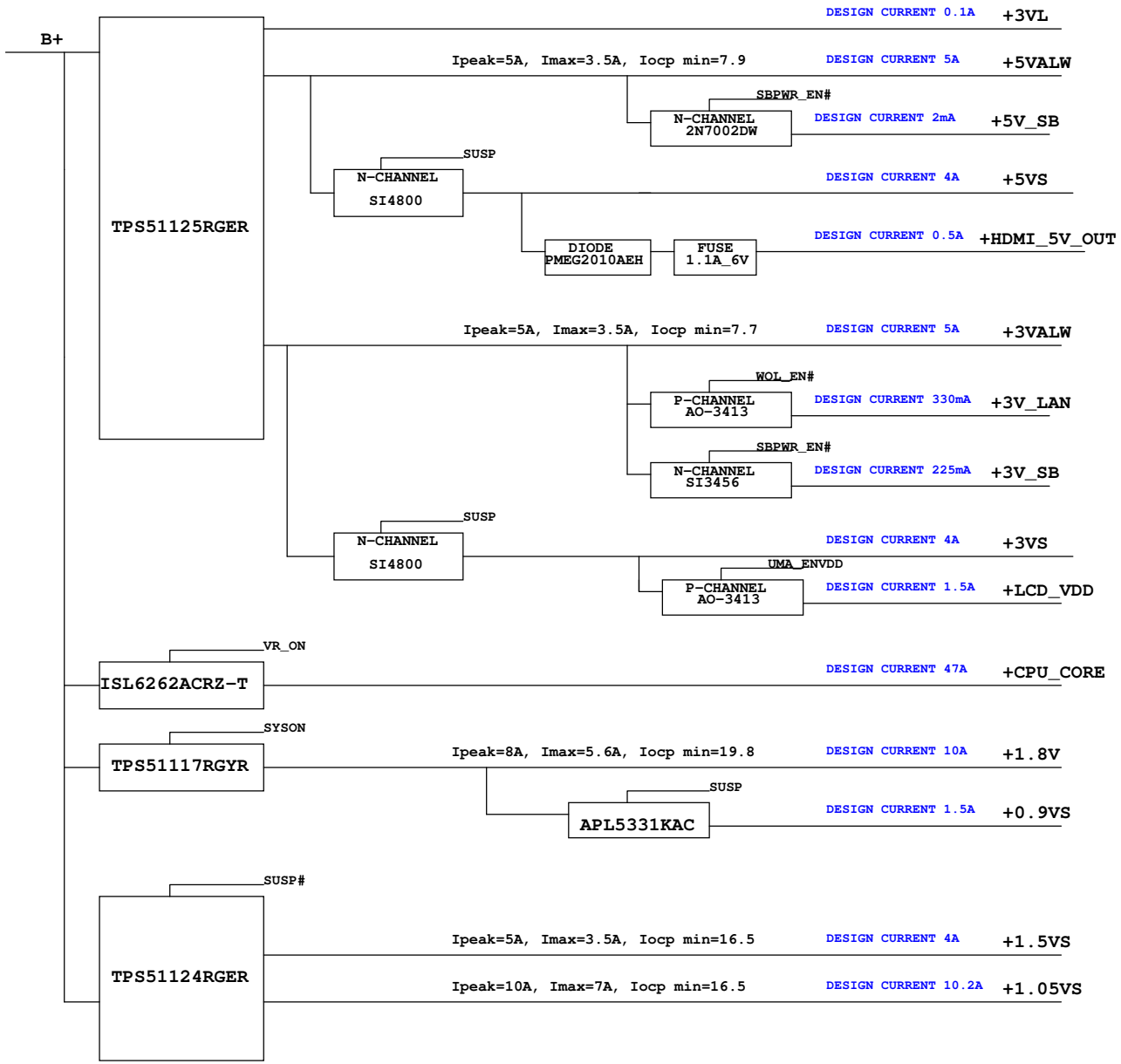

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Title: **Power Tree**

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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VL	5V always on power rail	ON	ON	ON	ON
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON
+CPU_CORE	Core voltage for VGA chip	ON	ON	OFF	OFF
+VGA_PCIE_1.1VS	1.1V switched power rail for VGA PCIE	ON	ON	OFF	OFF
+1.8VS	1.8V power rail for VRAM	ON	ON	OFF	OFF

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		

BTO Option Table

Function	North Bridge		RJ11	CAMERA	MIC	HDMI	
description	GM	GL				Y	
explain	GM45	GL40	MODEM	CAMERA	MIC	HDMI	Non-HDMI
BTO	GM45R3@ GM45R1@	GL40R3@ GL40R1@	MDC@	CAM@	MIC@	IHDMI@	NIHDMI@

External PCI Devices

EC SM Bus1 address

Power	Device	Address
+3VL	EC KB926 D3	
+3VL	Smart Battery	0001 011X b
+3VL	FUN/B (CAP Sensor)	

EC SM Bus2 address

Power	Device	Address
+3VS	EC KB926 D3	
+3VS	CPU THM Sen SMSC SMC1402	0100 110x b

ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
+3VS	Clock Generator (SLG8SP556V)	1101 001Xb
+3VS	DDR DIMM0	1001 000Xb
+3VS	DDR DIMM1	1001 010Xb
+3VS		

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Title: Notes List

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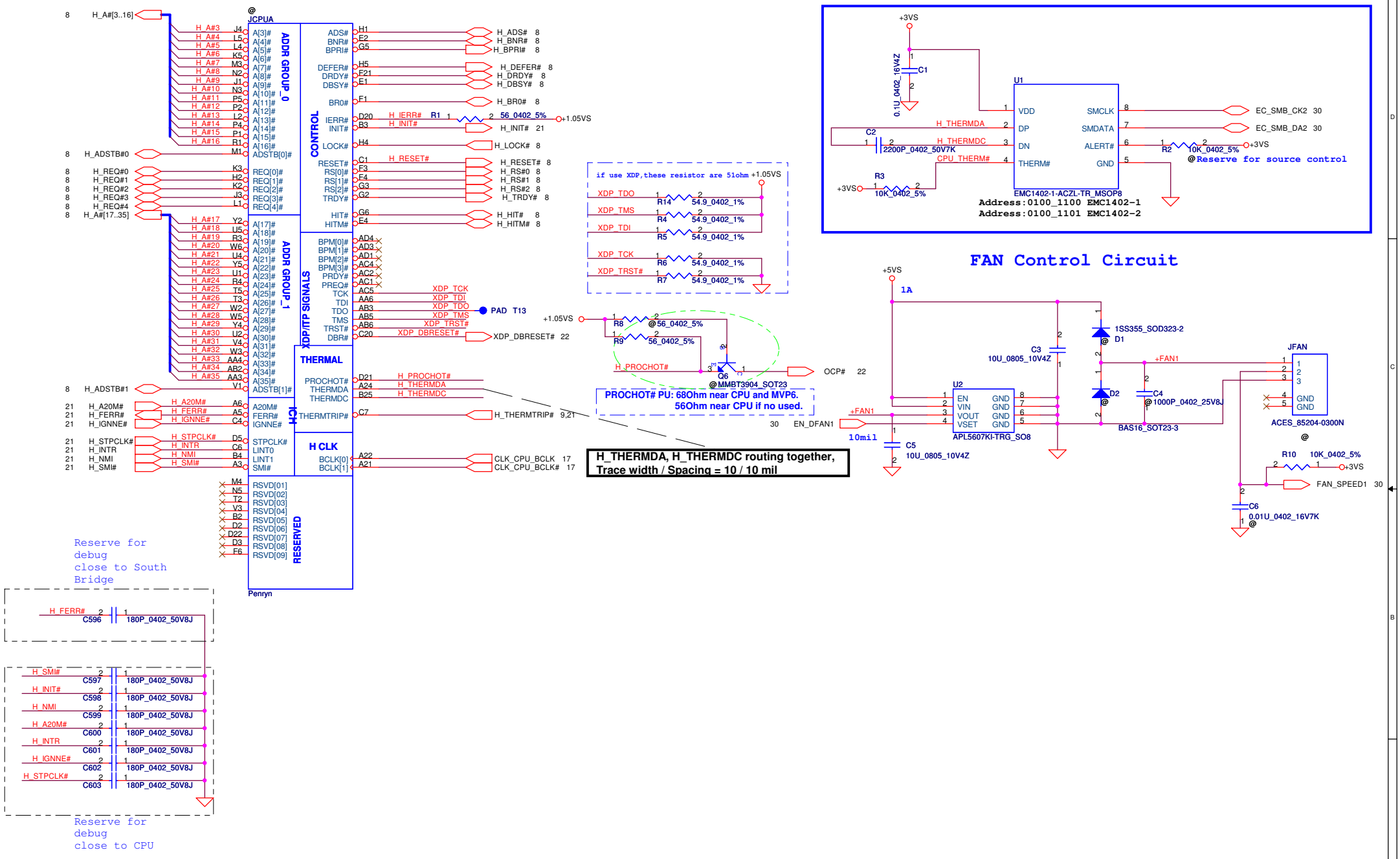

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Title: Penryn(1/3)-AGTL+/THM/FAN

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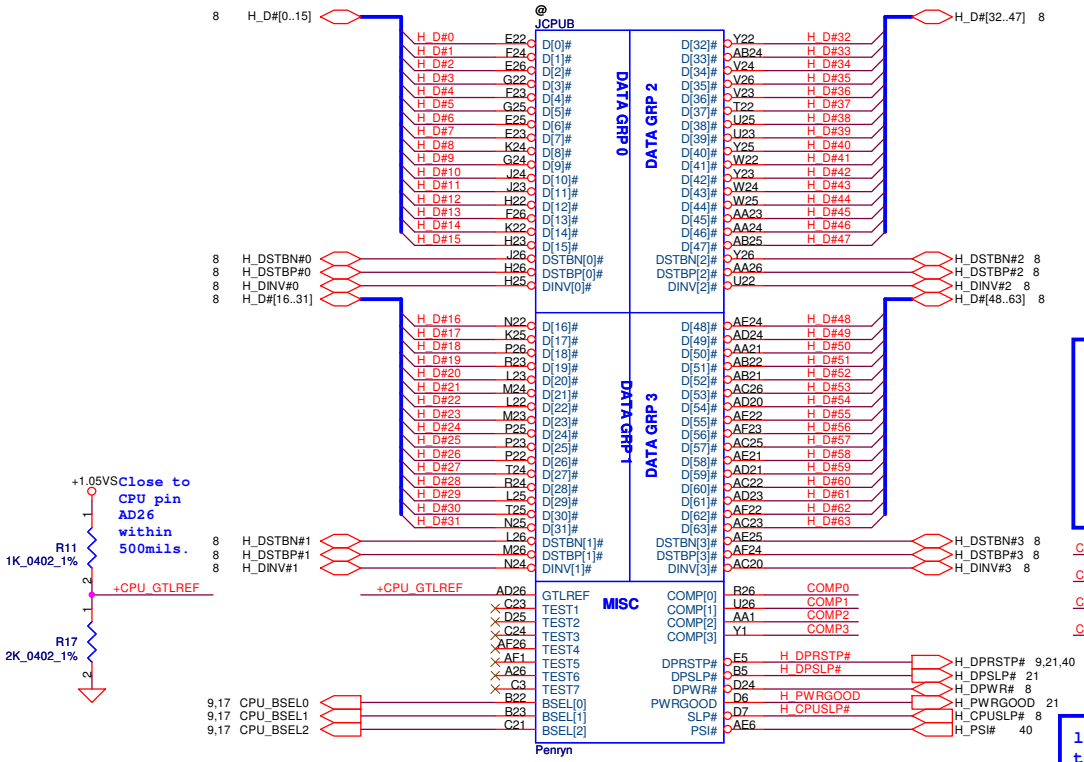
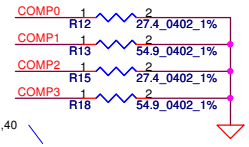


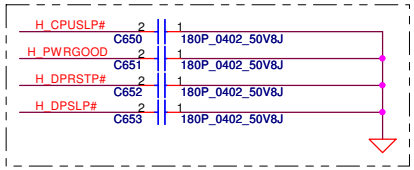
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



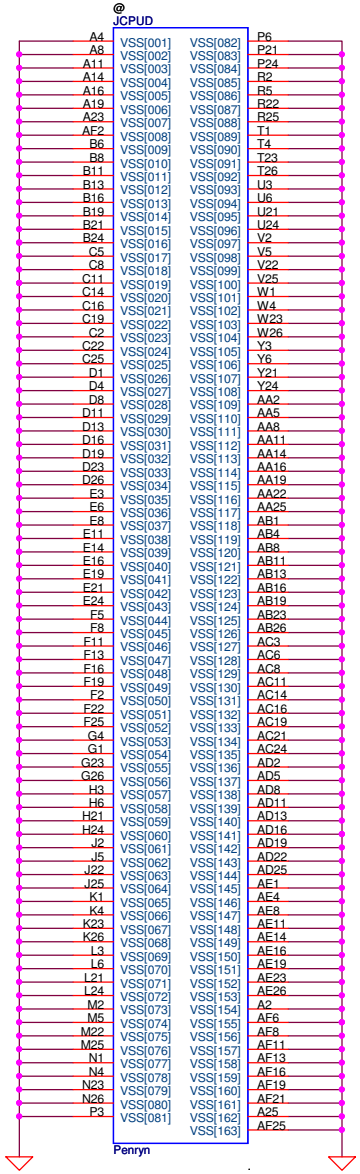
layout note: Please use "Daisy Chain" to layout and the signal (H_DPRSTP#) is routed from ICH9 to power IC, then to NB and CPU

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



Reserve for debug close to CPU



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Compal Electronics, Inc.

Title: Penryn(2/3)-AGTL+/GND

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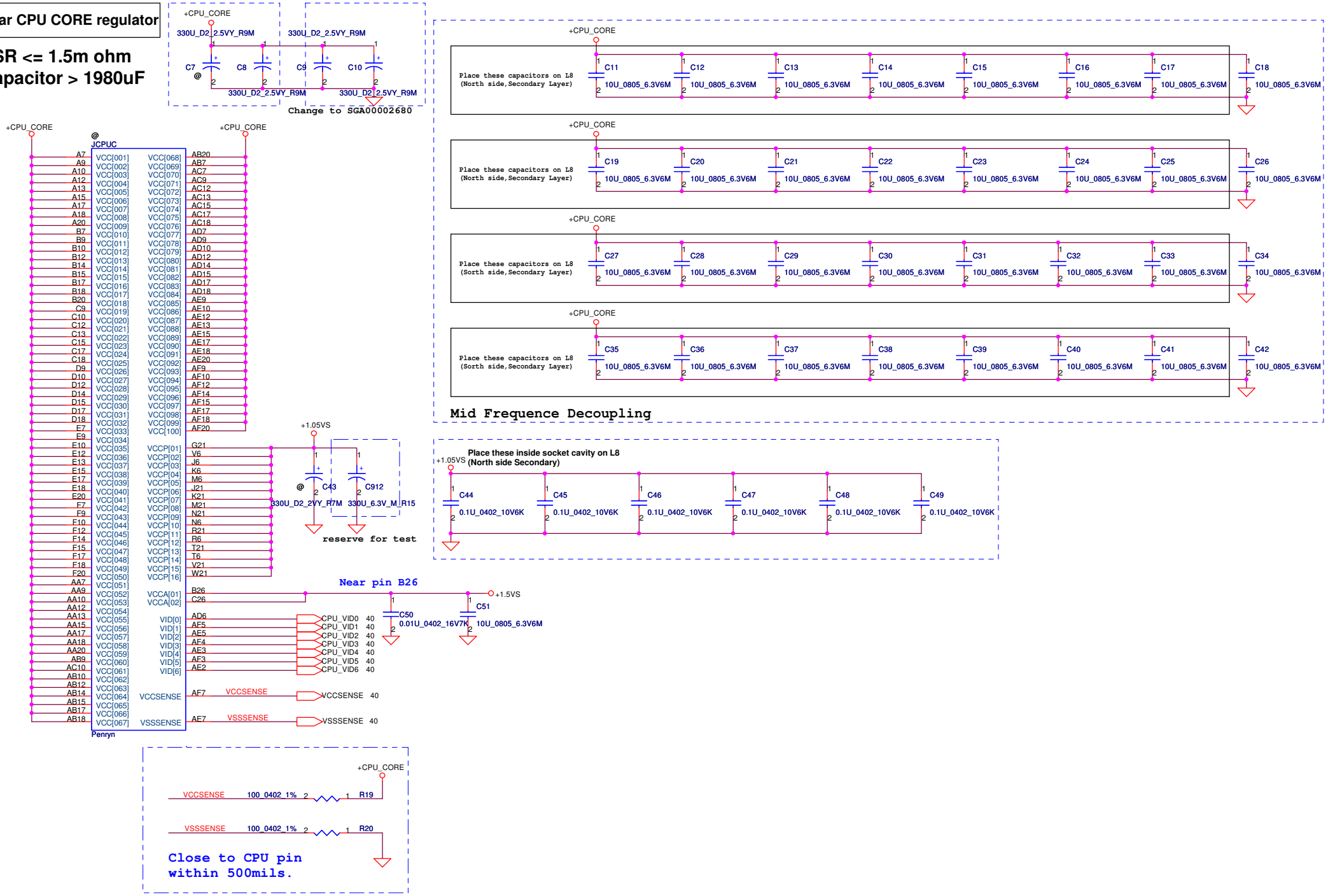
Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF



Length match within 25 mils. The trace width/space/other is 14/7/25.

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Compal Electronics, Inc.

Title: Penryn(3/3)-PWR/Bypass

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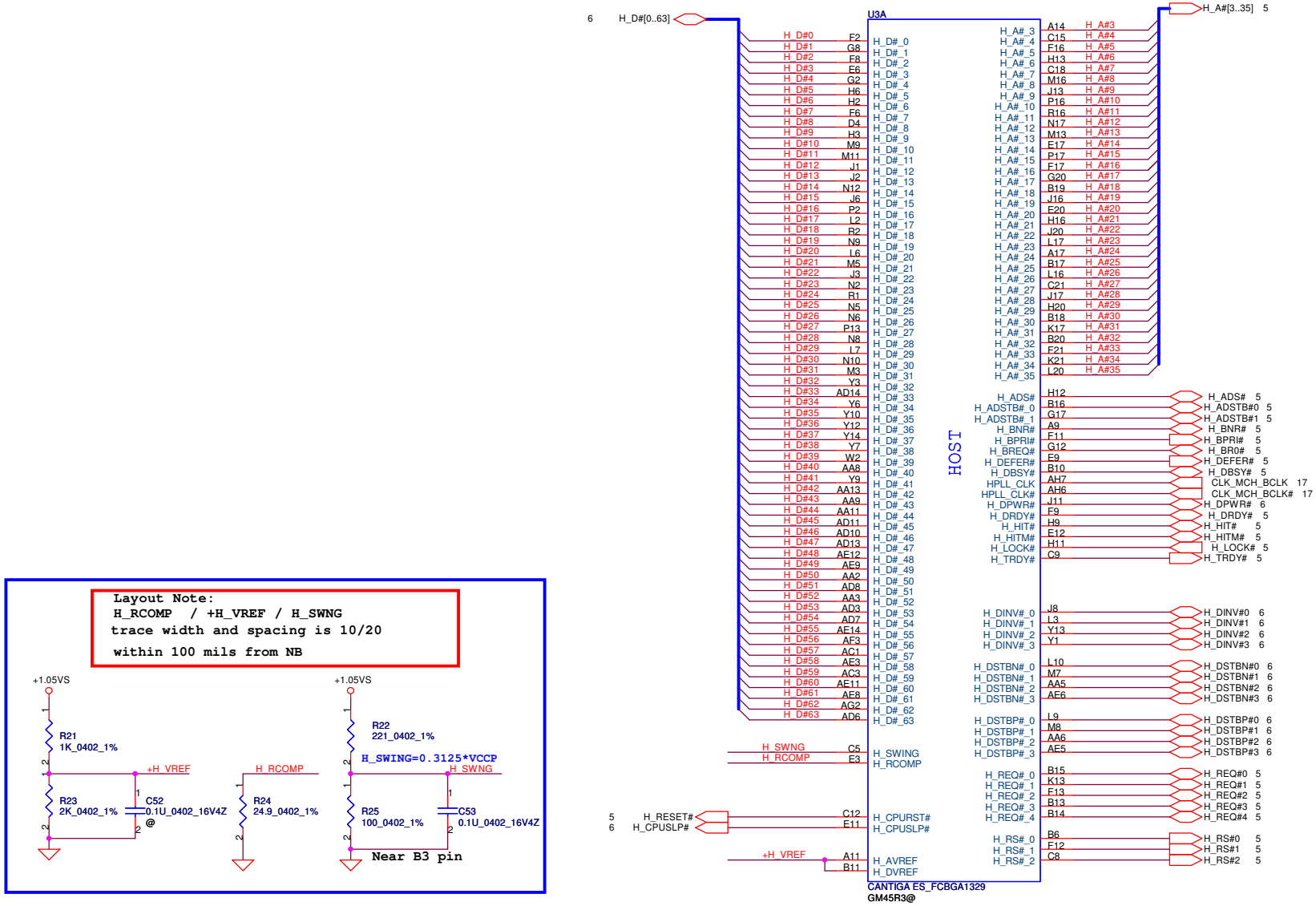

Layout Note:
H_RCOMP / +H_VREF / H_SWNG
trace width and spacing is 10/20
within 100 mils from NB

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Title: Cantiga GMCH(1/7)-GTL

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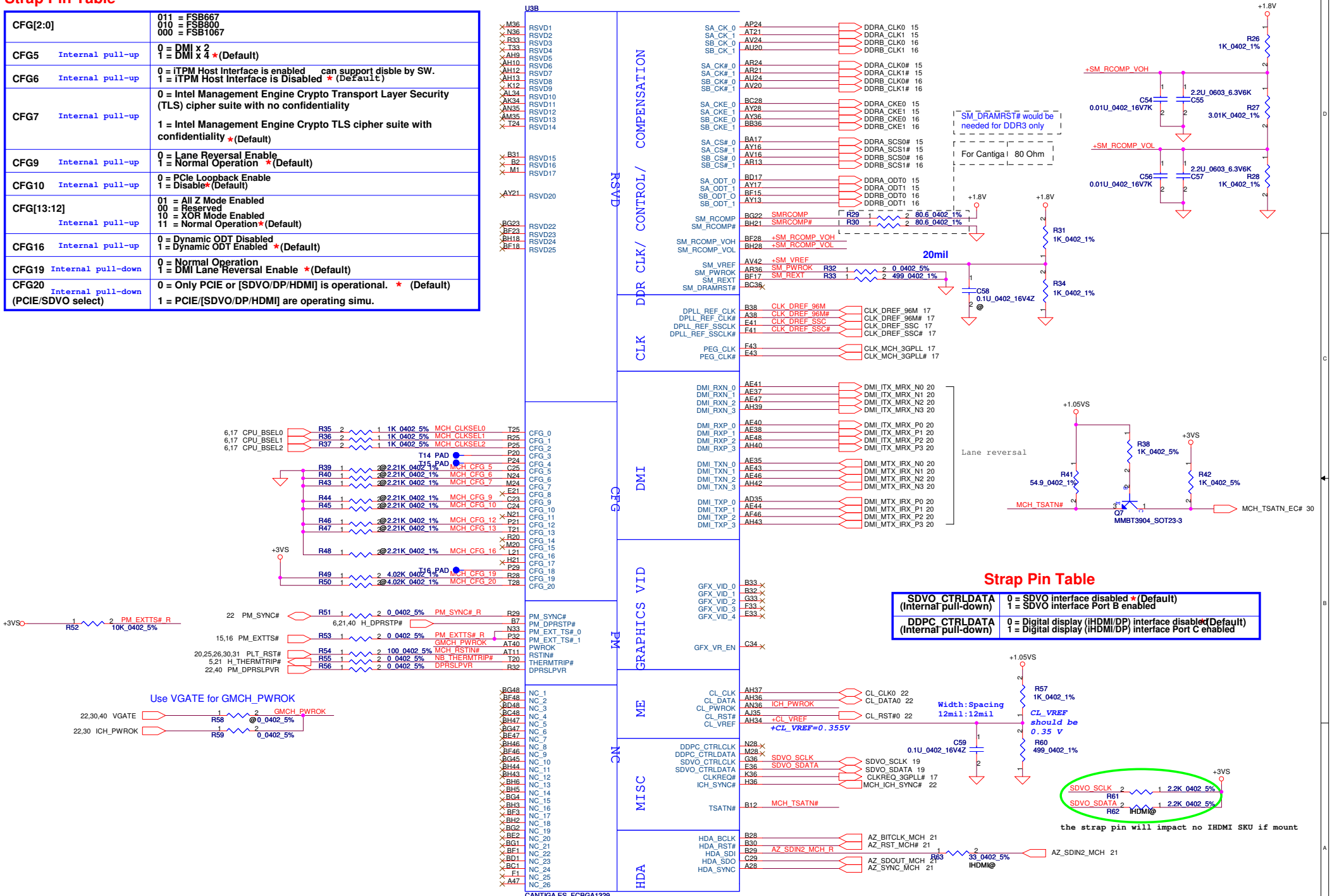
Strap Pin Table

CFG[2:0]		011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6	Internal pull-up	0 = iTPM Host Interface is enabled can support disble by SW. 1 = iTPM Host Interface is Disabled * (Default)
CFG7	Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9	Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10	Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12]	Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation*(Default)
CFG16	Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19	Internal pull-down	0 = Normal Operation 1 = DMI Lane Reversal Enable *(Default)
CFG20 (PCIE/SDVO select)	Internal pull-down	0 = Only PCIE or [SDVO/DP/HDMI] is operational. * (Default) 1 = PCIE/[SDVO/DP/HDMI] are operating simu.



Strap Pin Table

SDVO_CTRLDATA (Internal pull-down)	0 = SDVO interface disabled *(Default) 1 = SDVO interface Port B enabled
DDPC_CTRLDATA (Internal pull-down)	0 = Digital display (iHDMI/DP) interface disabled*(Default) 1 = Digital display (iHDMI/DP) interface Port C enabled

the strap pin will impact no IHDMI SKU if mount

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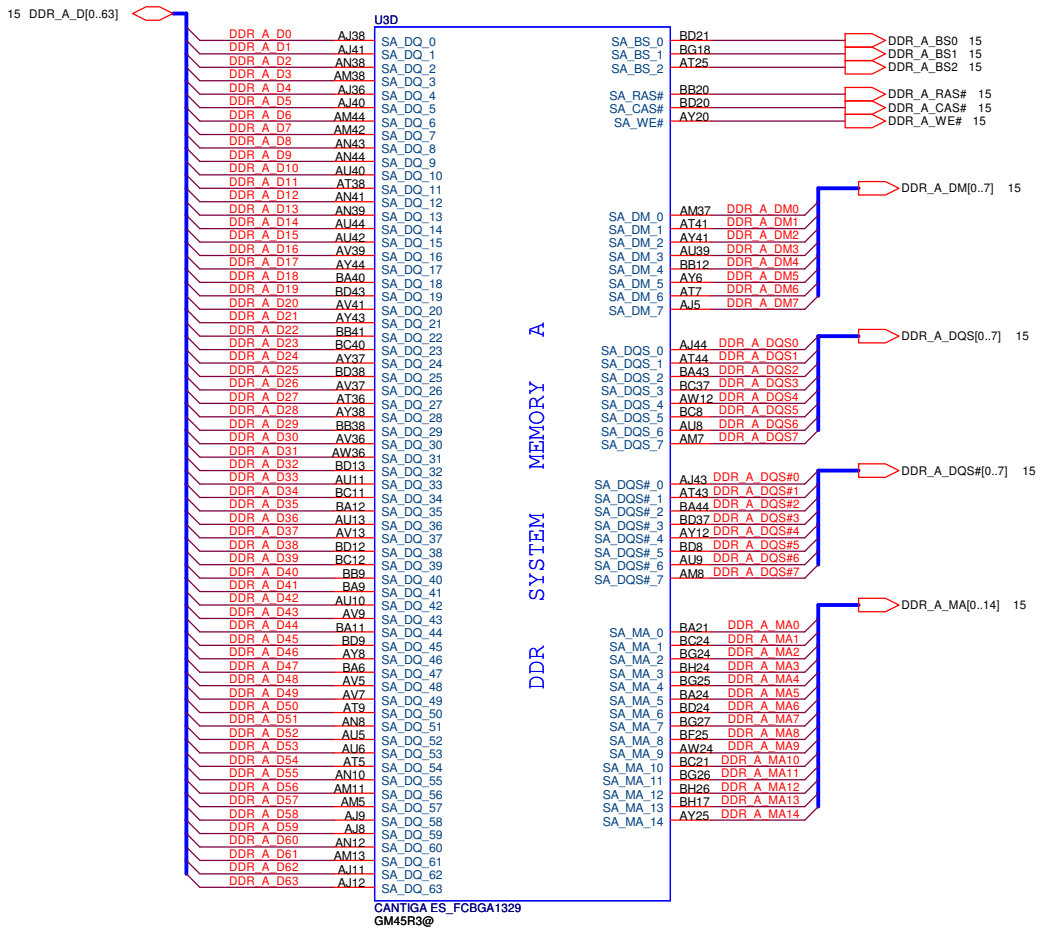

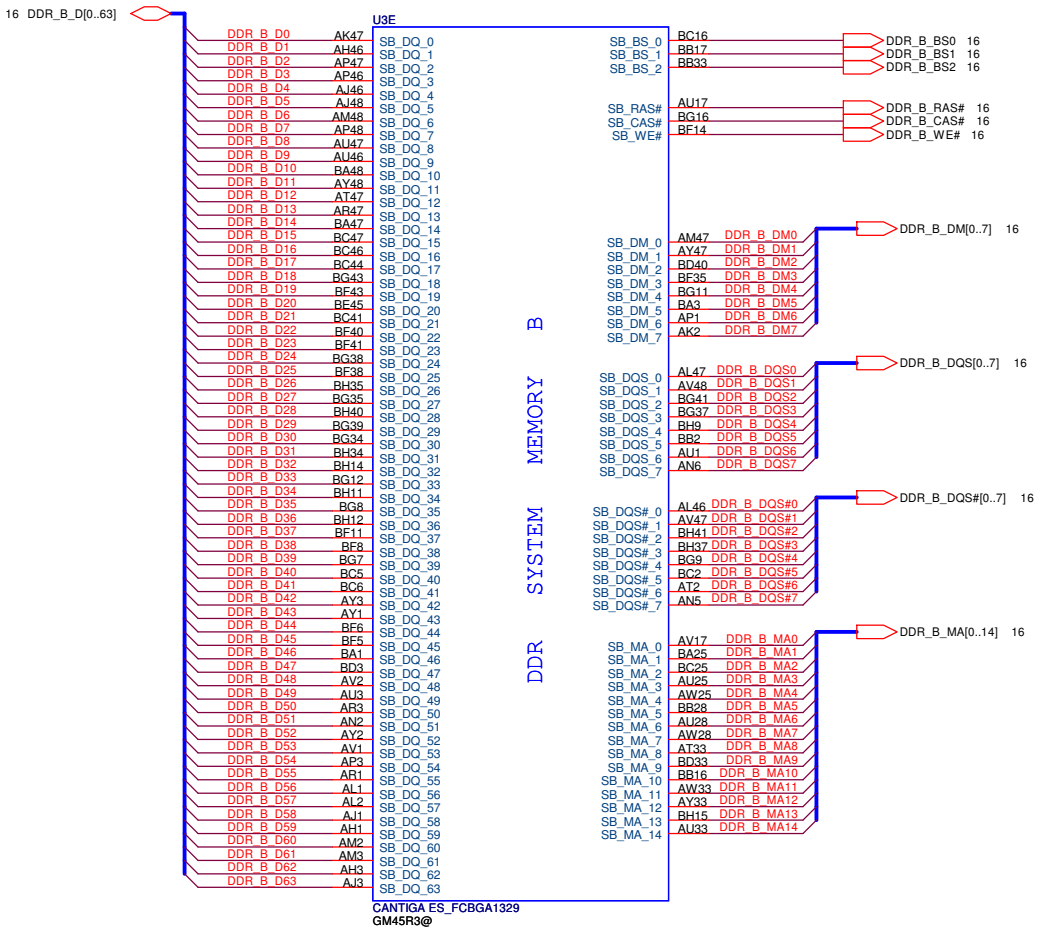

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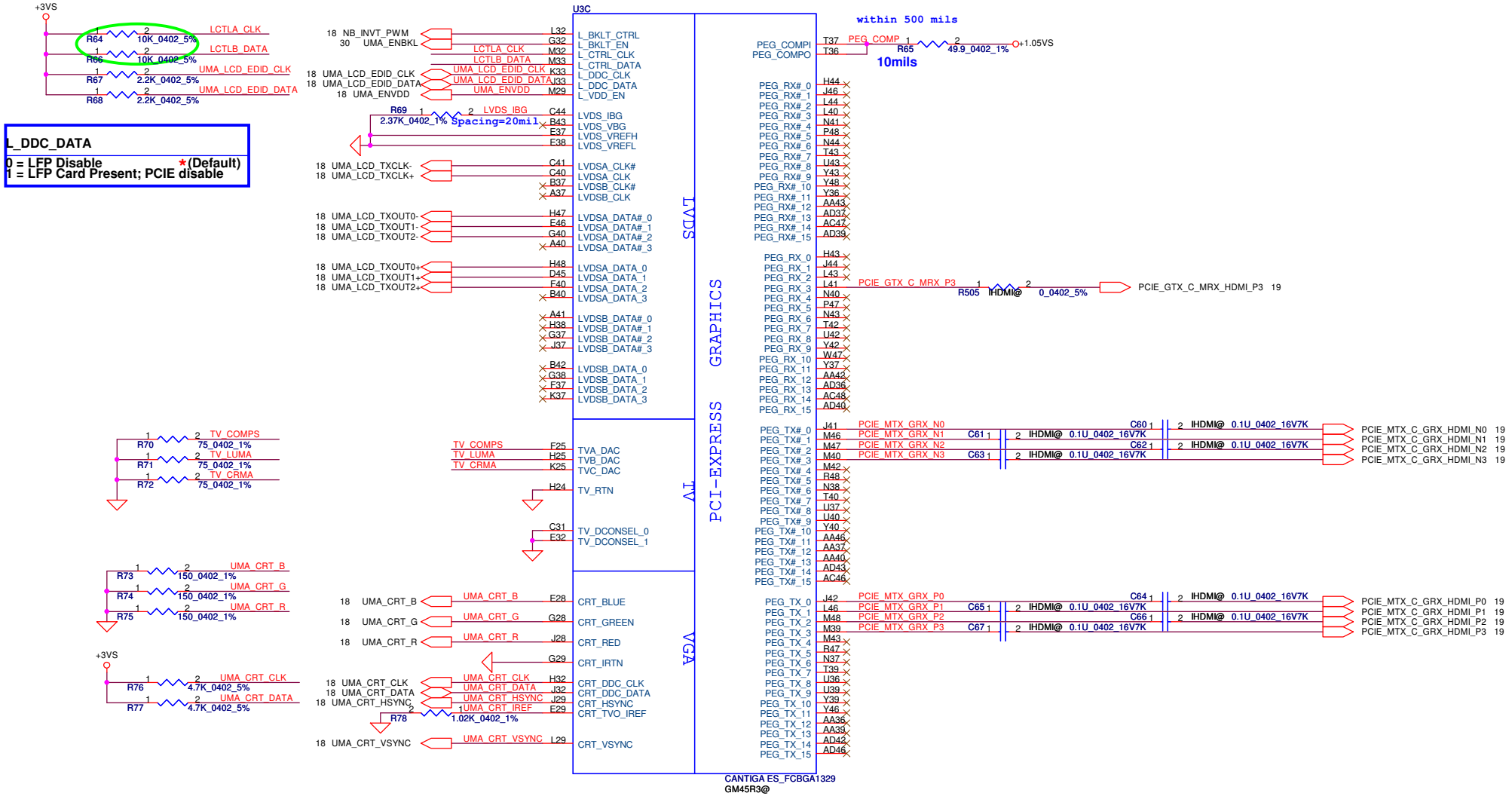

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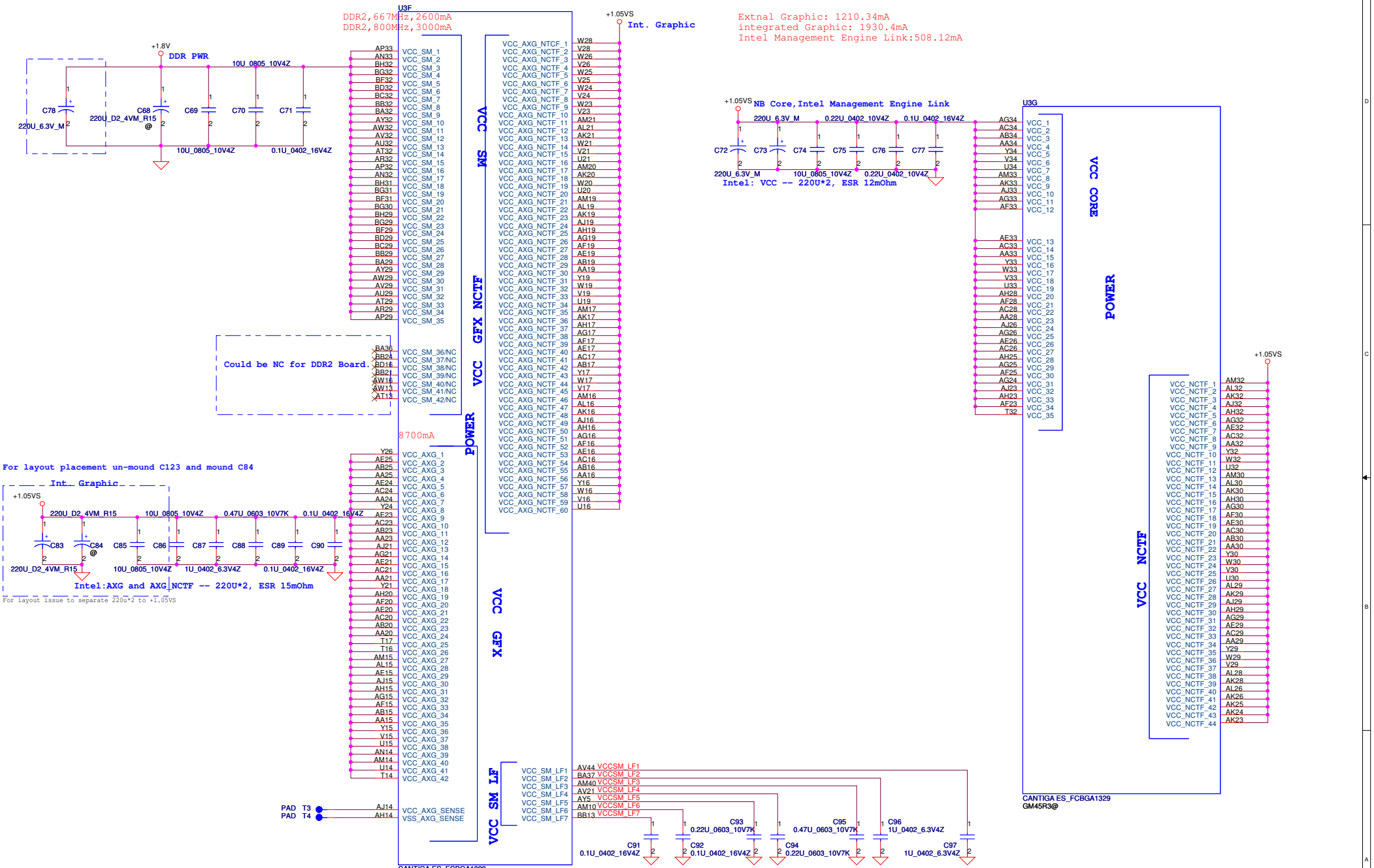

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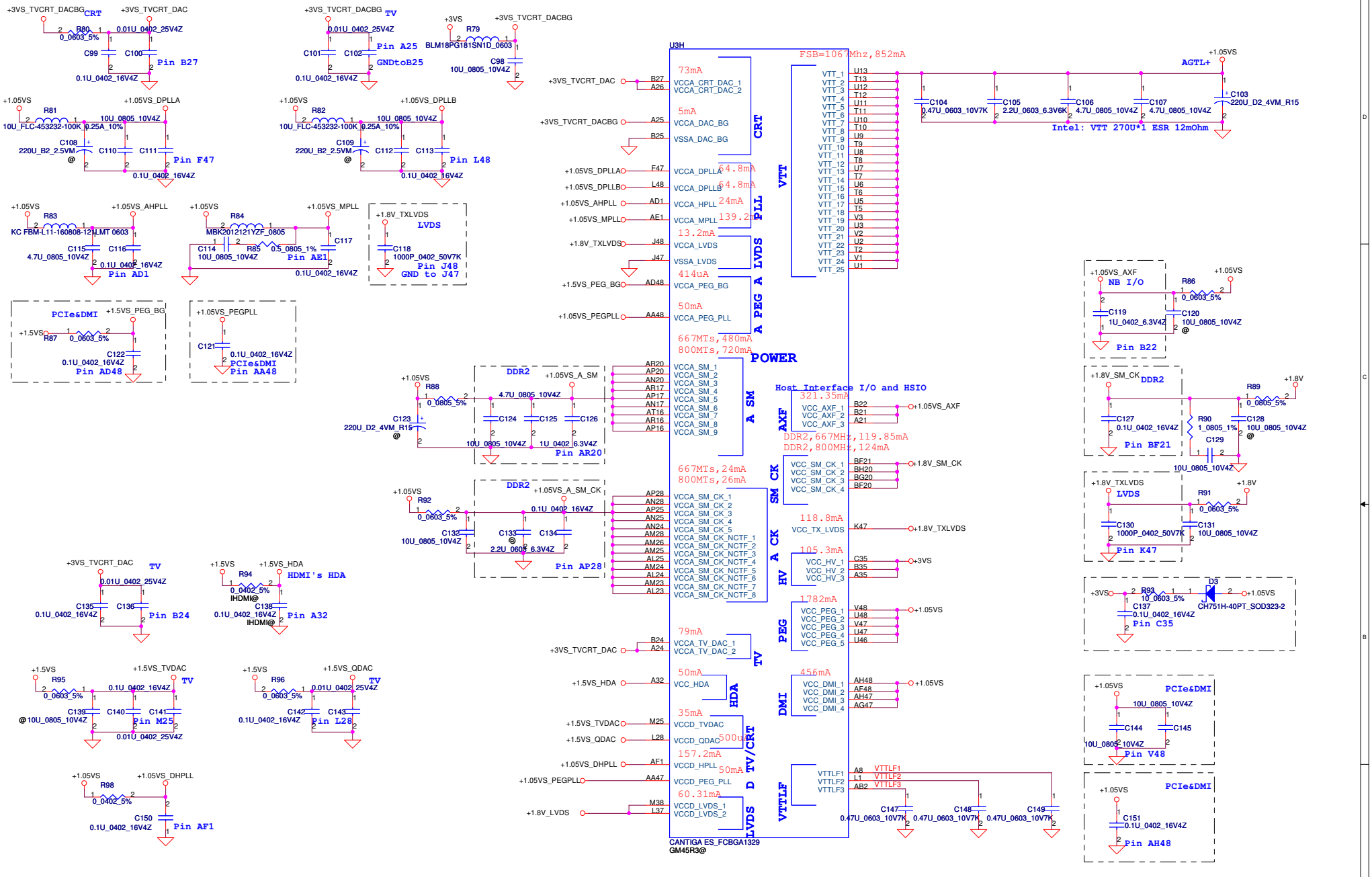
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CANTIGA ES_FCBGA1329
GM45R3@
POWER
CRT
VTT
PLL
LVDS
PEG
SM
AXF
SM CK
A CK
HV
PEG
DMI
HDA
TV/CRT
D
VTTLF
FSB=1067Mhz,852mA
Host Interface I/O and HSIO
DDR2,667MHz,119.85mA
DDR2,800MHz,124mA
Intel: VTT 270U*1 ESR 12mOhm
Pin A25
GNDtoB25
Pin B27
Pin F47
Pin L48
Pin AD1
Pin AE1
Pin J48
GND to J47
Pin AD48
Pin AA48
Pin AR20
Pin AP28
Pin B24
Pin A32
Pin M25
Pin L28
Pin AF1
Pin AA47
Pin M38
Pin B22
Pin BF21
Pin K47
Pin C35
Pin V48
Pin AH48
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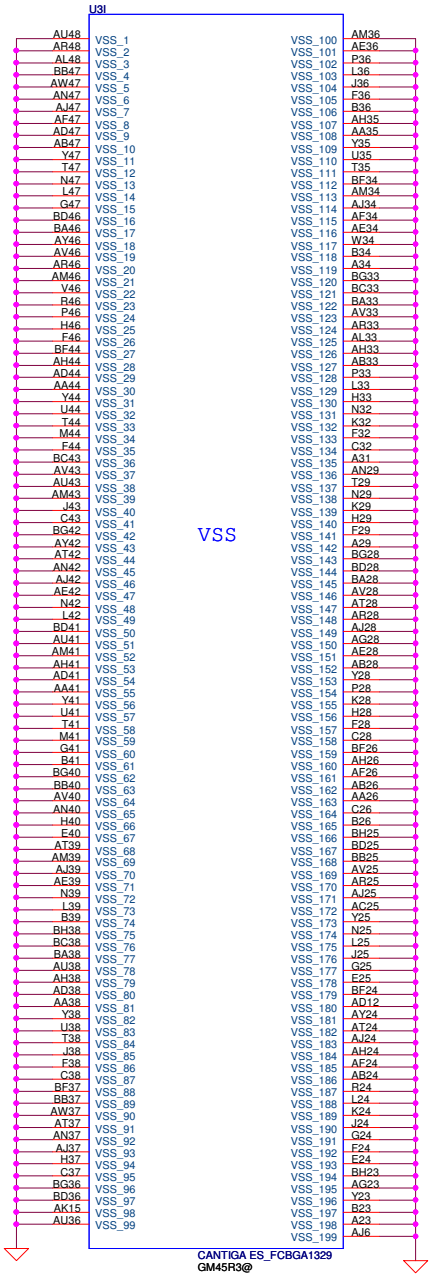

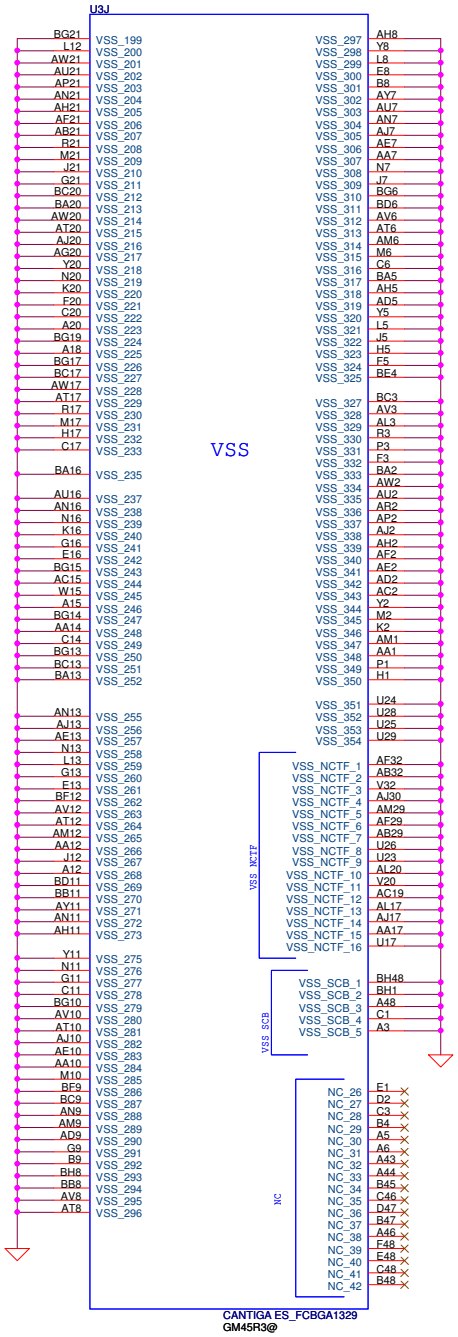

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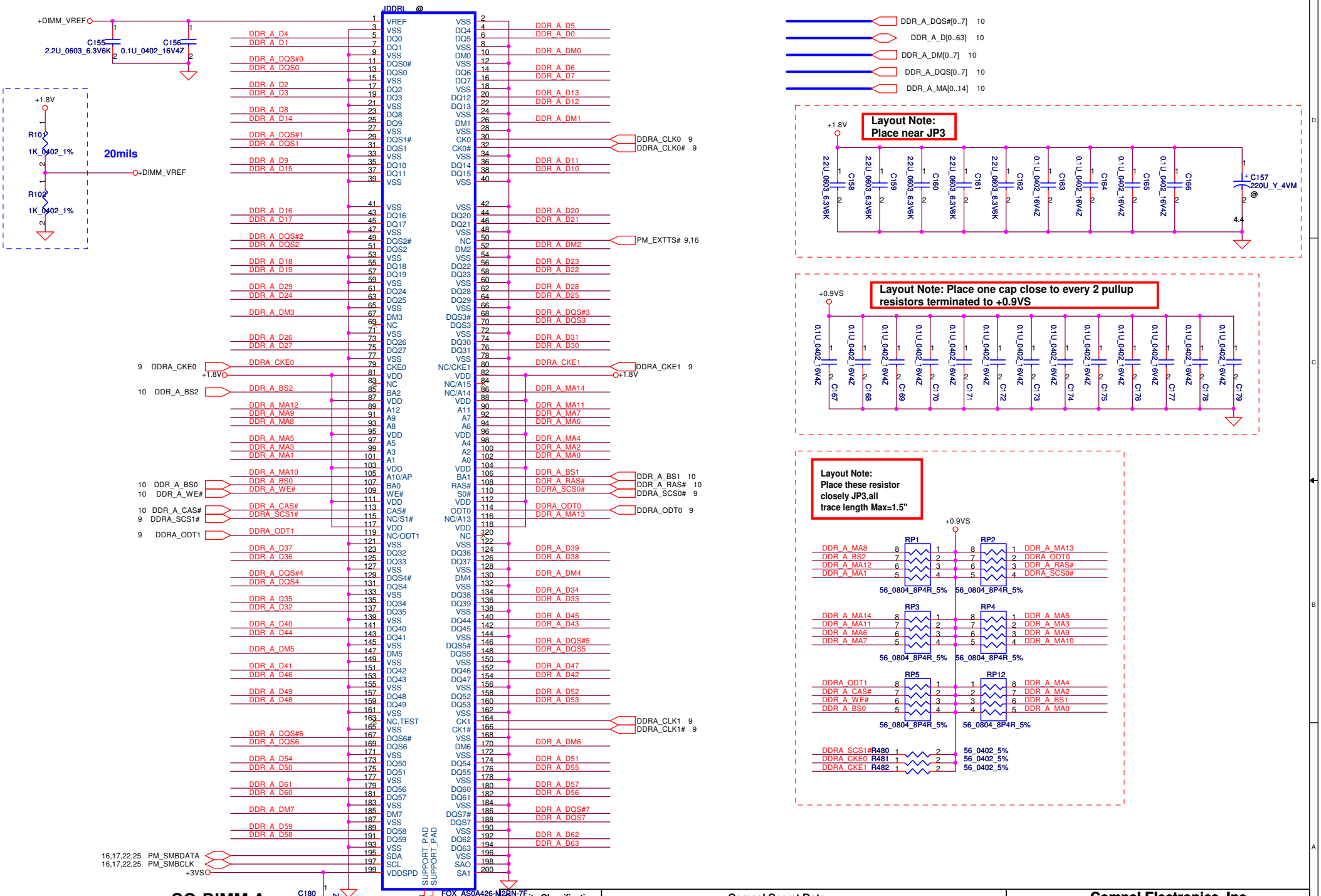

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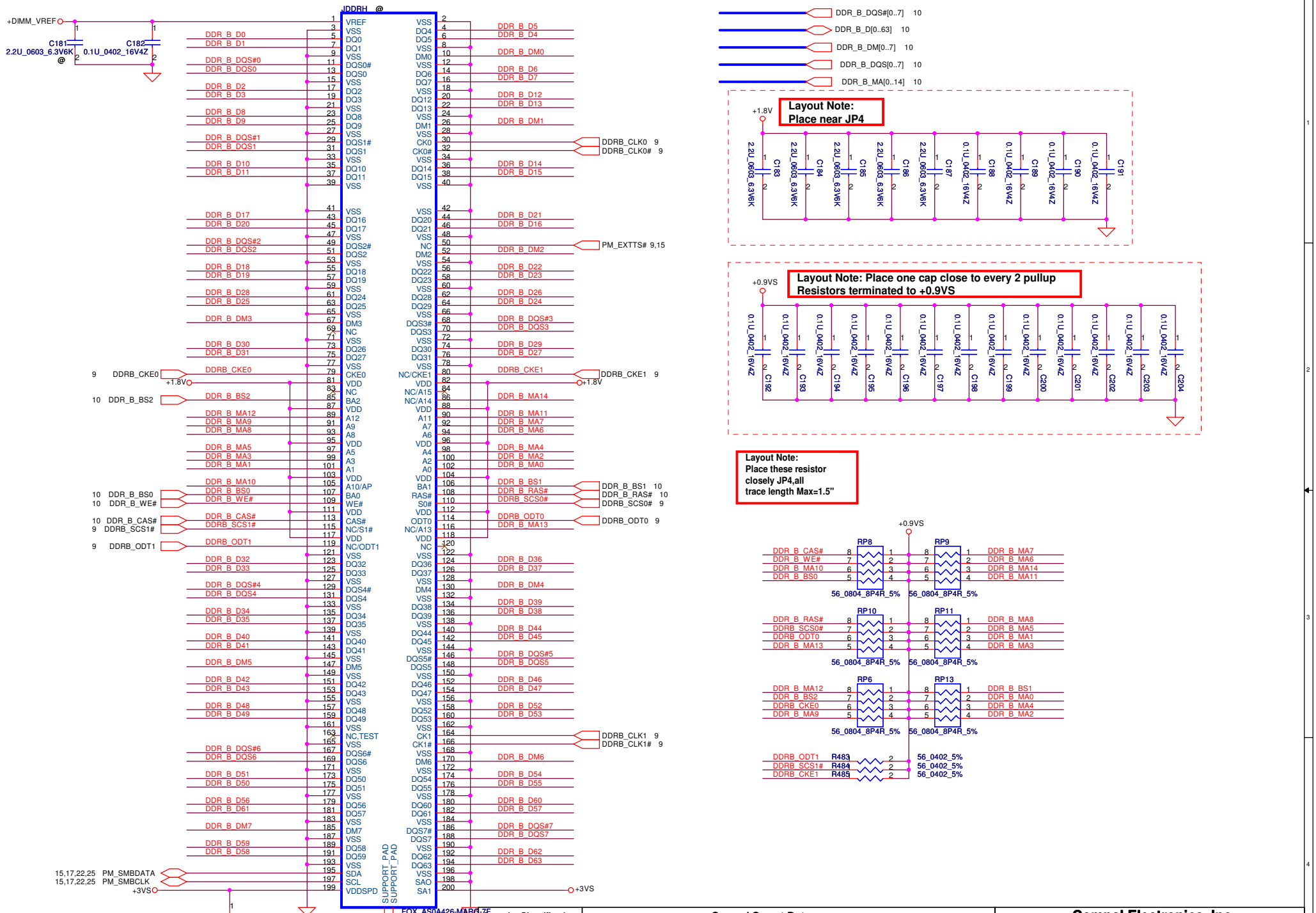

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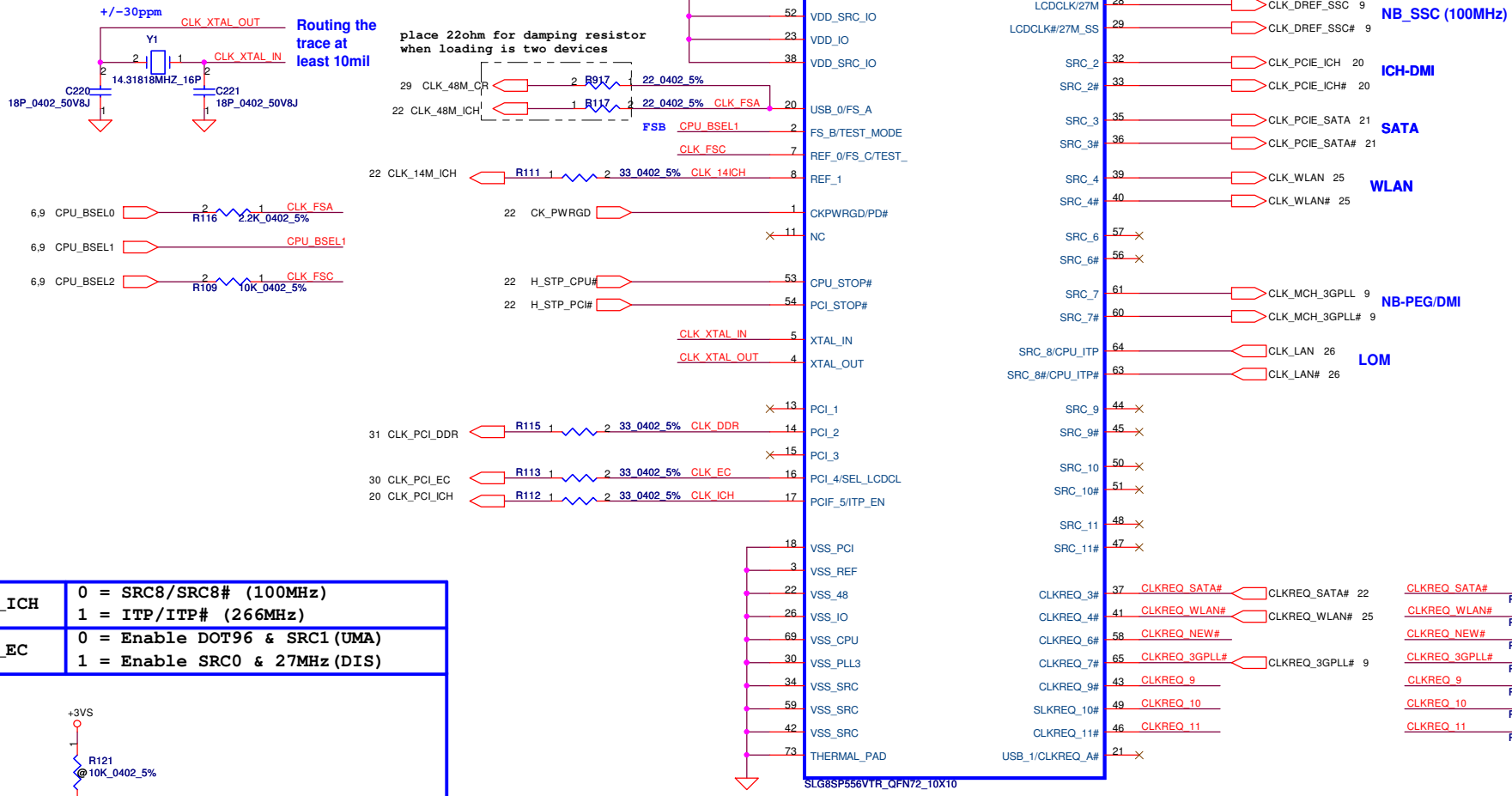
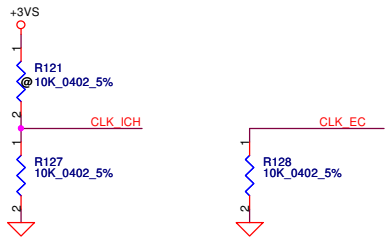
Compal Electronics, Inc.

Title	DDRII-SODIMM1	
Size	Document Number: NBWAA LA5821P M/B	Rev 1.0
Date: Monday, August 10, 2009	Sheet 16 of 41	

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



CLK_ICH	0 = SRC8/SRC8# (100MHz) 1 = ITP/ITP# (266MHz)
CLK_EC	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

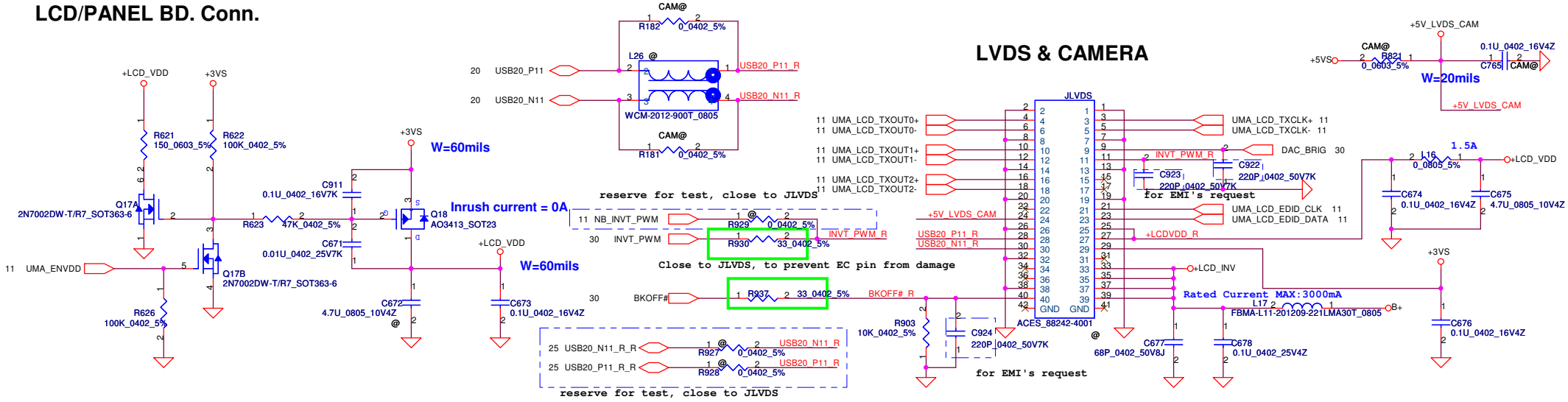
Title: Clock Generator

Size | Document Number: NBWAA LA5821P M/B | Rev 1.0

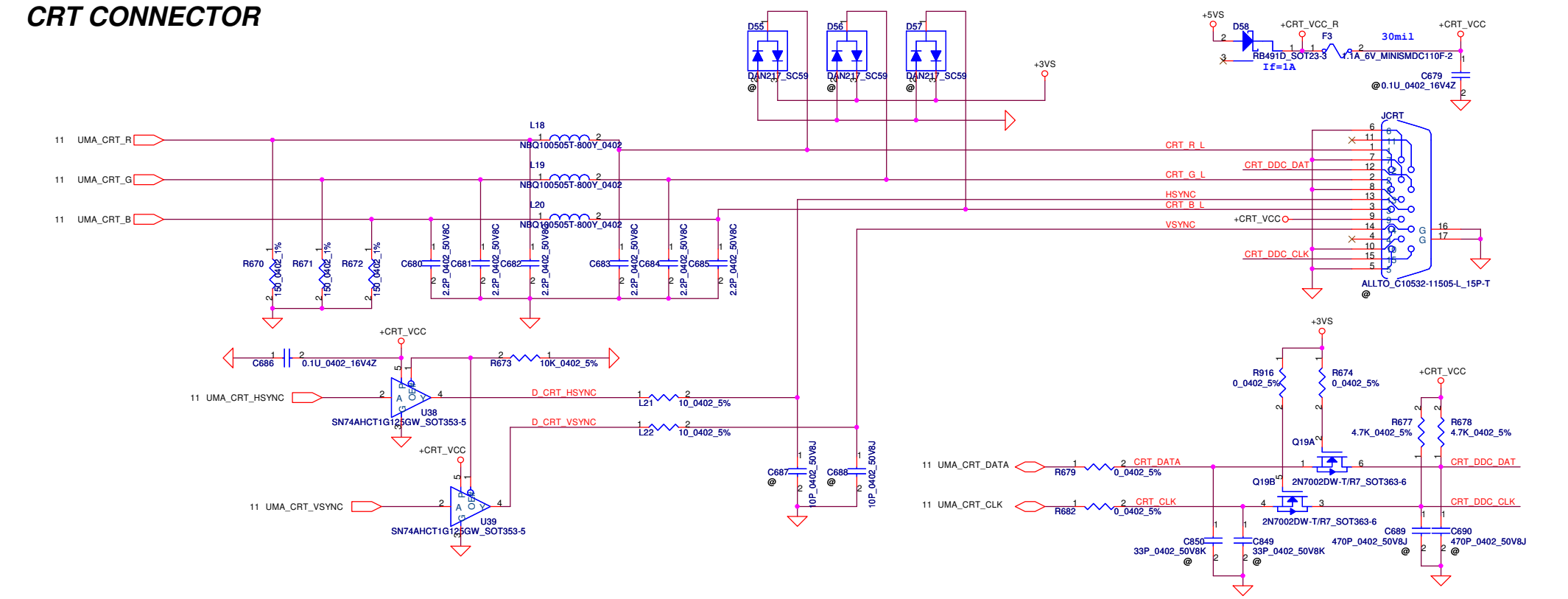
Date: Monday, August 10, 2009 | Sheet 17 of 41

LCD/PANEL BD. Conn.

LVDS & CAMERA



CRT CONNECTOR



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Issued Date	2009/07/28	Deciphered Date	2010/07/28

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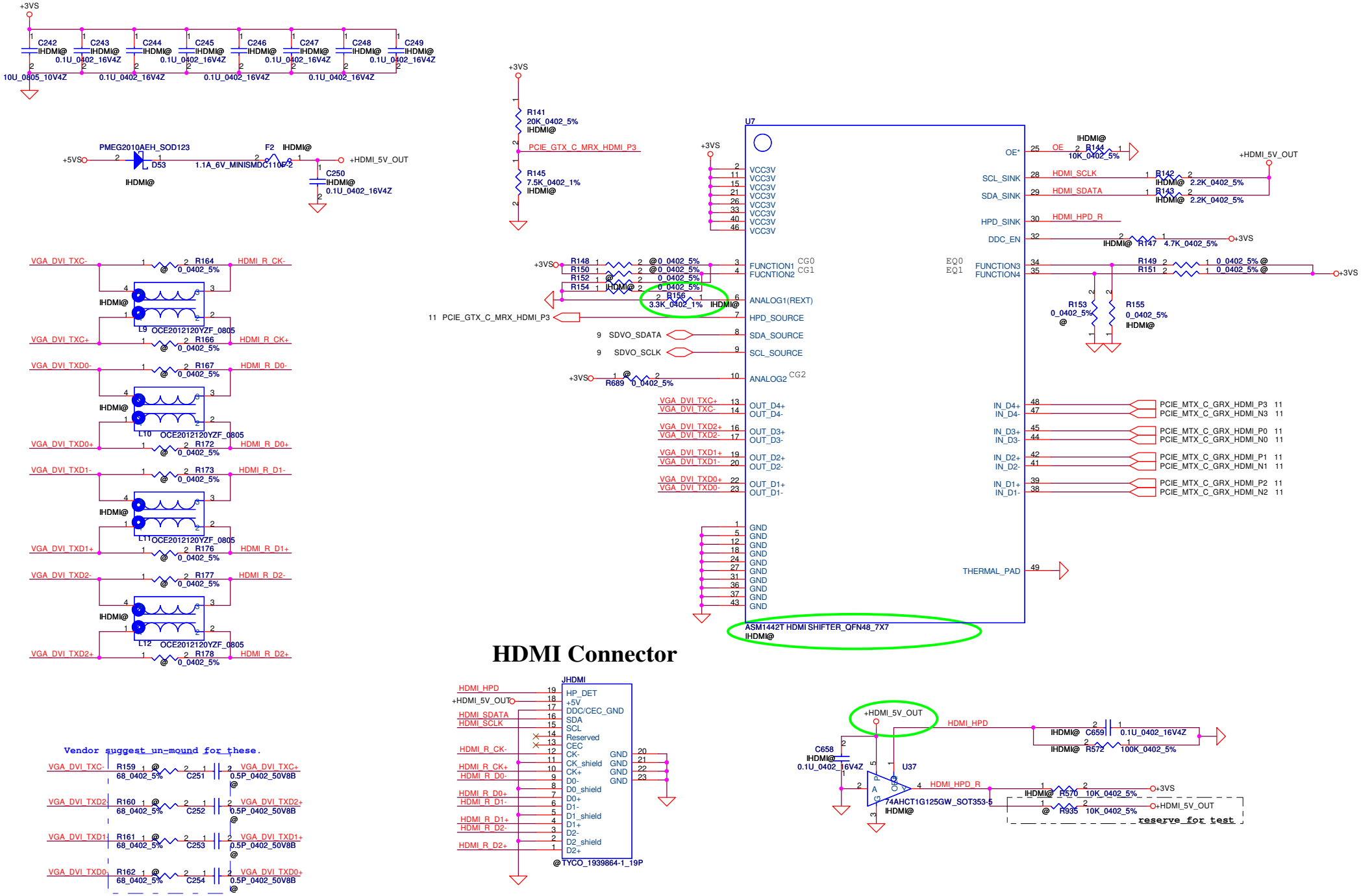
Compal Electronics, Inc.

Title: **LVDS/CAM & CRT**

Size | Document Number: **NBWAA LA5821P M/B** | Rev: 1.0

Date: Thursday, August 06, 2009 | Sheet 18 of 41



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Issued Date	2009/07/28	Deciphered Date	2010/07/28

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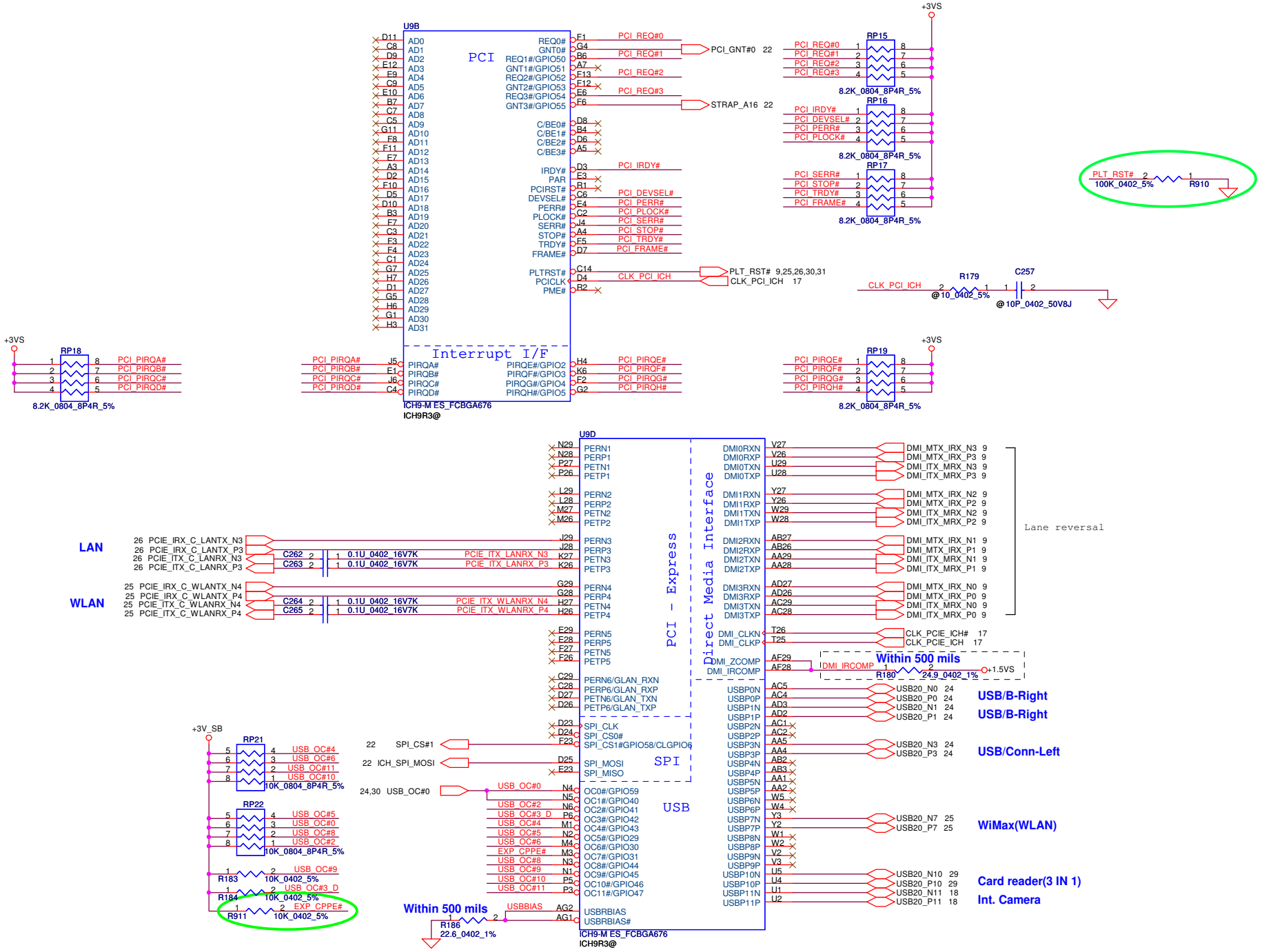
Compal Electronics, Inc.

Title: HDMI Connector

Size | Document Number: NBWAA LA5821P M/B | Rev: 1.0

Date: Monday, August 10, 2009 | Sheet 19 of 41



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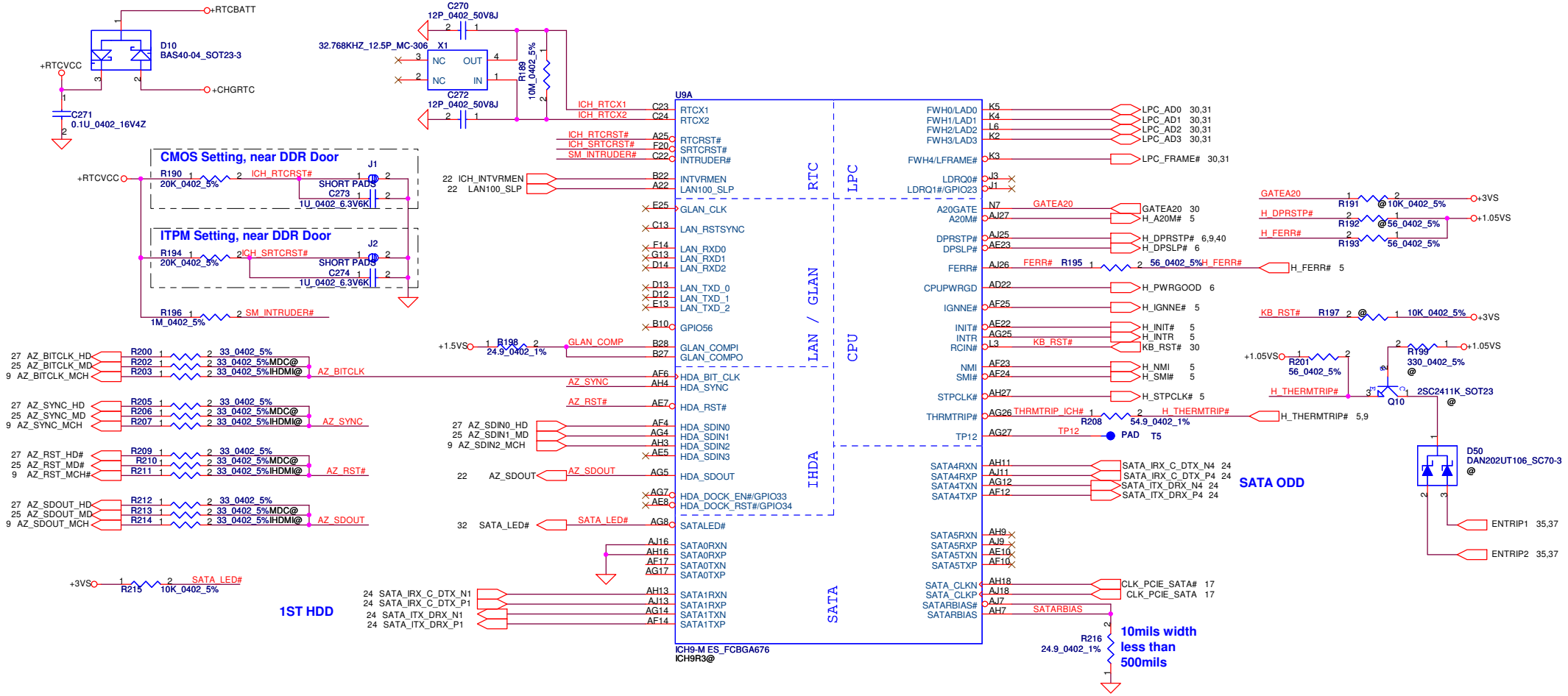
Compal Electronics, Inc.

Title: ICH9M(1/4)-PCI

Size | Document Number: NBWAA LA5821P M/B | Rev: 1.0

Date: Monday, August 10, 2009 | Sheet 20 of 41



Security Classification	Compal Secret Data		
Issued Date	2009/07/28	Deciphered Date	2010/07/28

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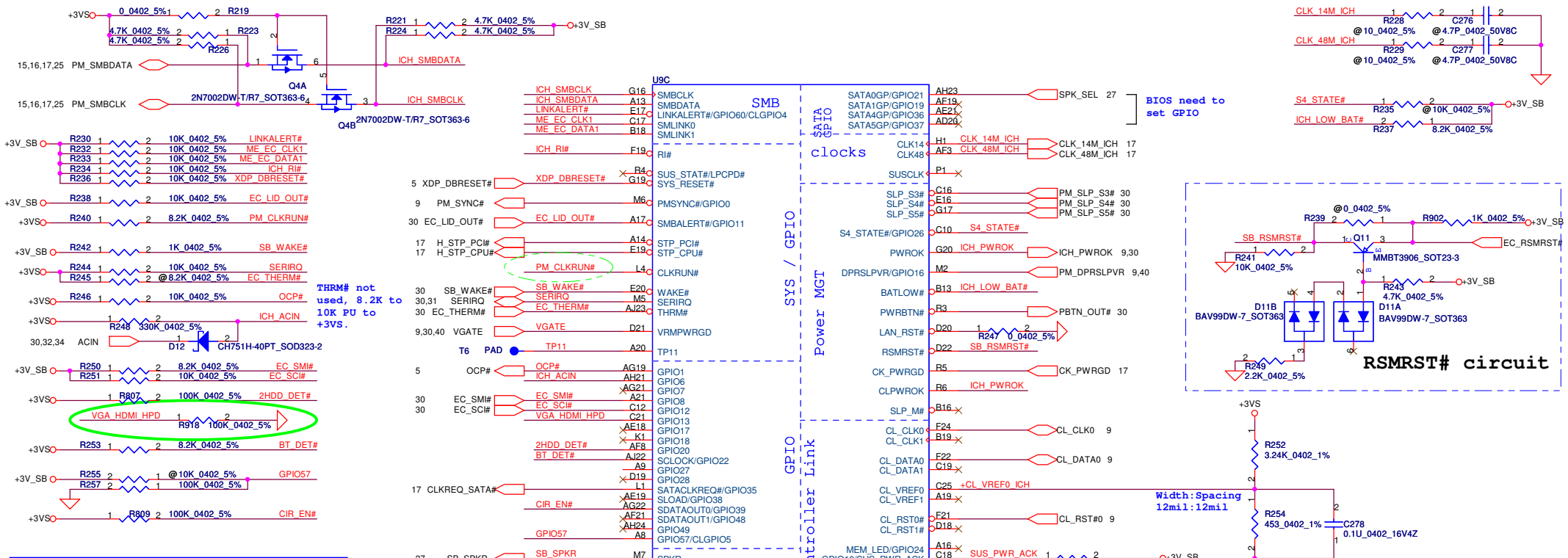
Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size | Document Number: NBWAA LA5821P M/B | Rev: 1.0

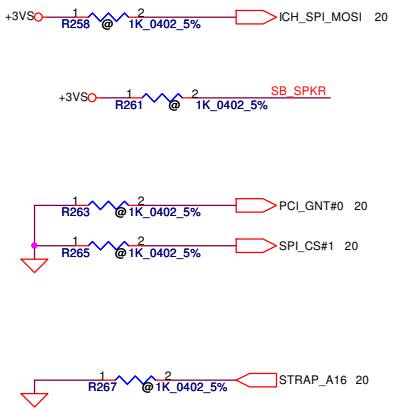
Date: Monday, August 10, 2009 | Sheet 21 of 41



iTPM Physical Presence	
CLGPIO5 Mobil Platform	Assert = iTPM Physical Presence Enable De-assert = iTPM disable **Only used in iAMT w/ME Firmware
GPIO57	Desktop Platform used only

SUS_PWR_ACK	Mobile Platform used only
GPIO10	Desktop Platform used only

ICH9M Strap Pin

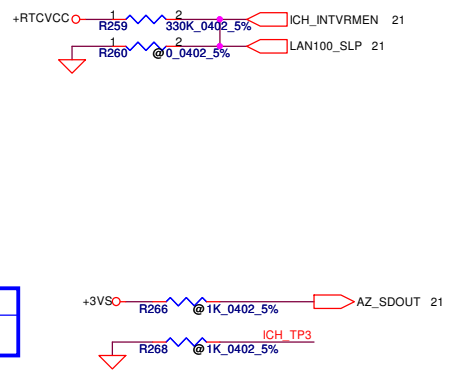


Internal TPM Strap(Internal pull-down)	
SPI_MOSI	Low= Disable High= iTPM enable by MCH strap*

No Reboot Strap (Internal pull-up)	
SB_SPKR	Low= *Default High= "No Reboot"

Boot BIOS Strap (Internal pull-up)		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	0	RESERVED
0	1	SPI
1	0	PCI
1	1	LPC* (Default)

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default* (Internal pull-up)



Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

Flash Descriptor Security Override Strap	
GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

DMI Termination Voltage	
GPIO49	Low= Desktop used High= Mobile* (Internal pull-up)

XOR Chain Entrance Strap		
ICH_TP3 (Internal pull-up)	HDA_SDOUT (Internal pull-down)	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

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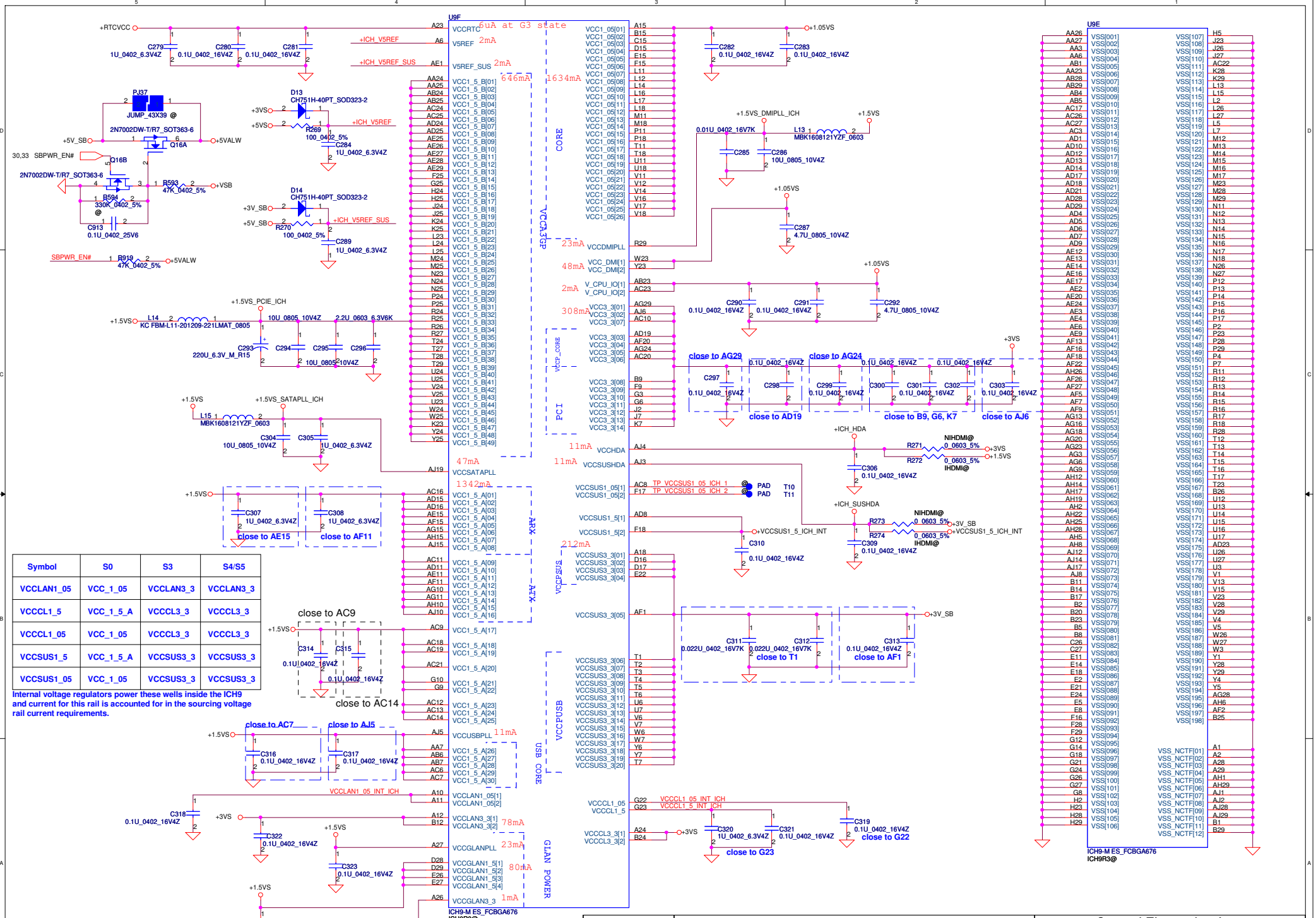
Compal Electronics, Inc.

Title: ICH9M(3/4)-USB,GPIO,PCIE

Size | Document Number: NBWAA LA5821P M/B | Rev 1.0

Date: Monday, August 10, 2009 | Sheet 22 of 41



Symbol	S0	S3	S4/S5
VCCLAN1_05	VCC_1_05	VCCLAN3_3	VCCLAN3_3
VCCCL1_5	VCC_1_5_A	VCCCL3_3	VCCCL3_3
VCCCL1_05	VCC_1_05	VCCCL3_3	VCCCL3_3
VCCSUS1_5	VCC_1_5_A	VCCSUS3_3	VCCSUS3_3
VCCSUS1_05	VCC_1_05	VCCSUS3_3	VCCSUS3_3

Internal voltage regulators power these wells inside the ICH9 and current for this rail is accounted for in the sourcing voltage rail current requirements.

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Compal Electronics, Inc.

Title: ICH9M(4/4)-POWER&GND

Size | Document Number: NBWAA LA5821P M/B | Rev: 1.0

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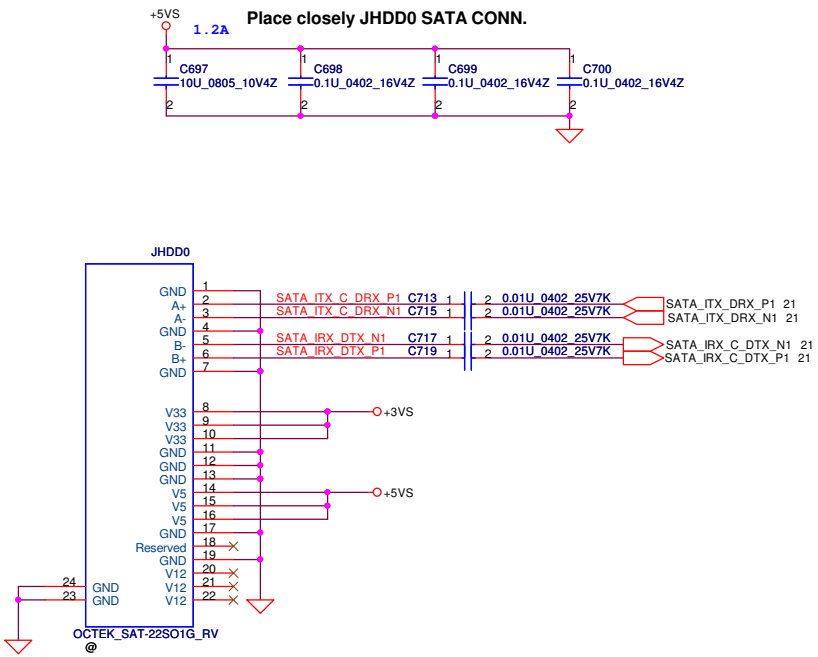
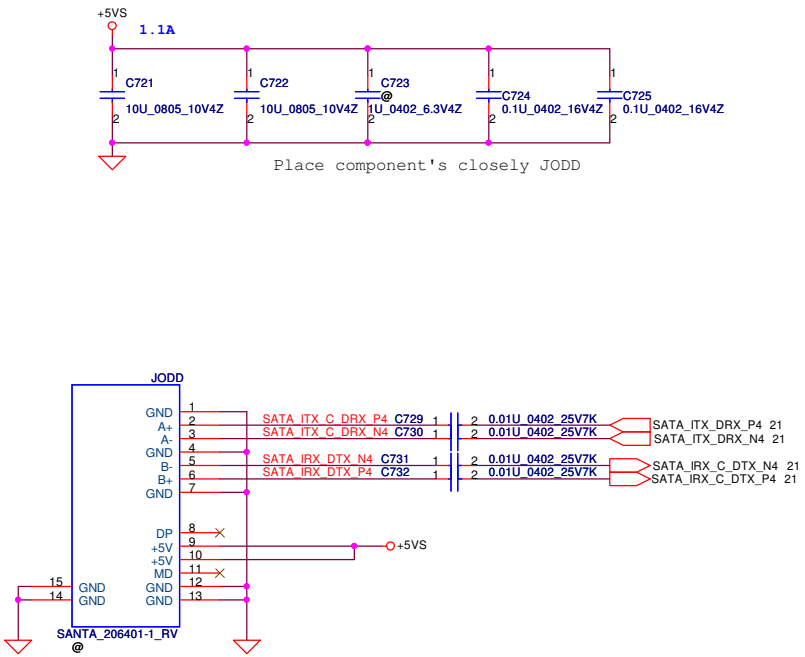
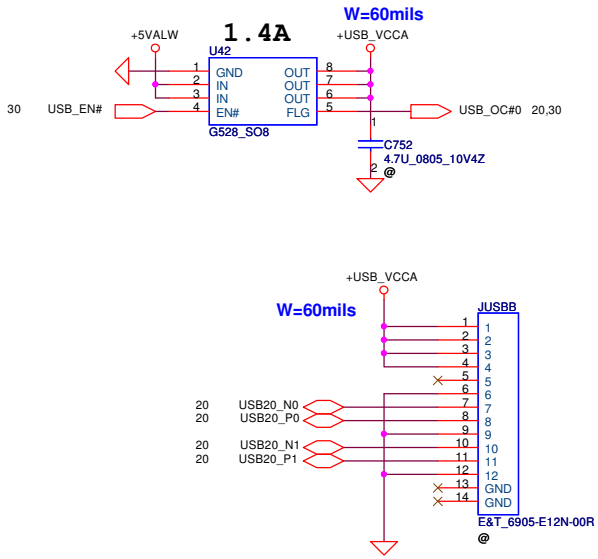
SATA HDD Conn.



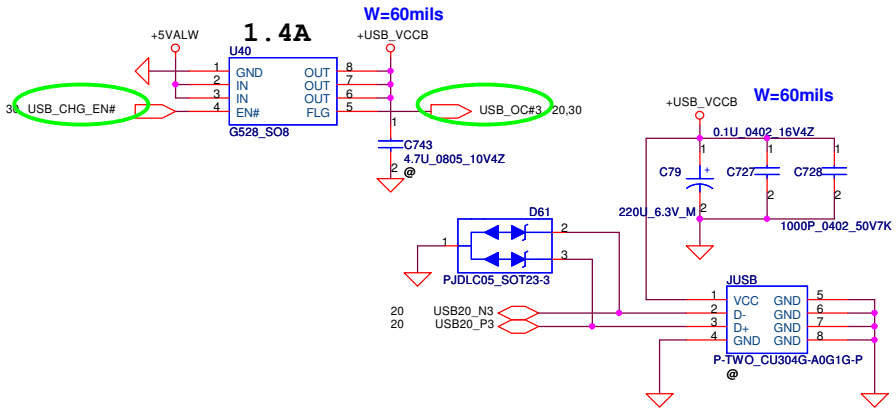
SATA ODD Conn



USB Board Conn



USB Left Conn



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Title	SATA-HDD/ODD& USB	
Size	Document Number: NBWAA LA5821P M/B	Rev 1.0
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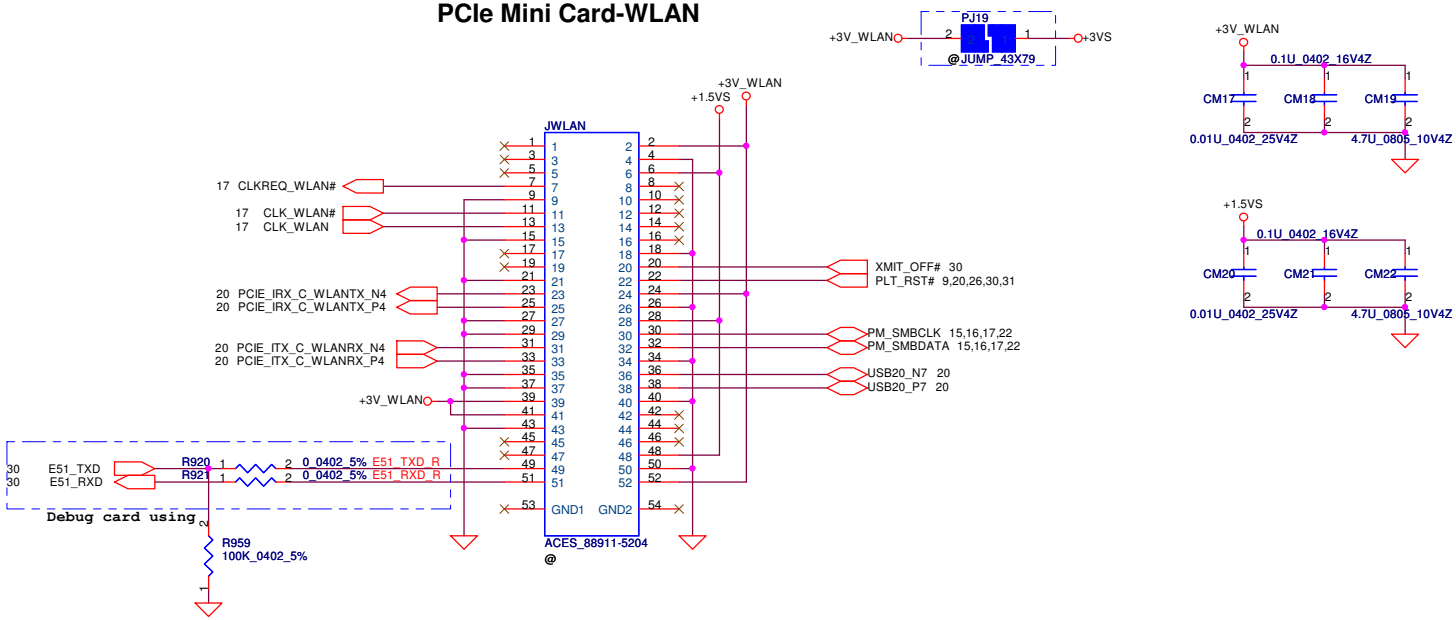
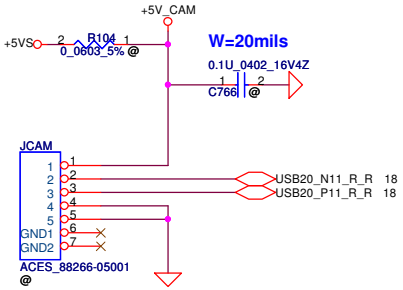
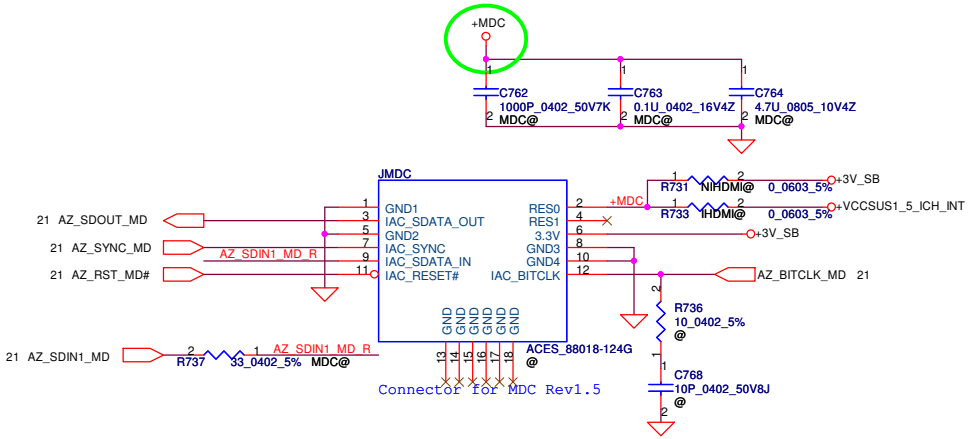
PCIe Mini Card-WLAN



Int. Camera



MDC 1.5 Conn.



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Compal Electronics, Inc.

Title: **WLAN/MDC/CAMERA**

Size | Document Number: **NBWAA LA5821P M/B** | Rev: 1.0

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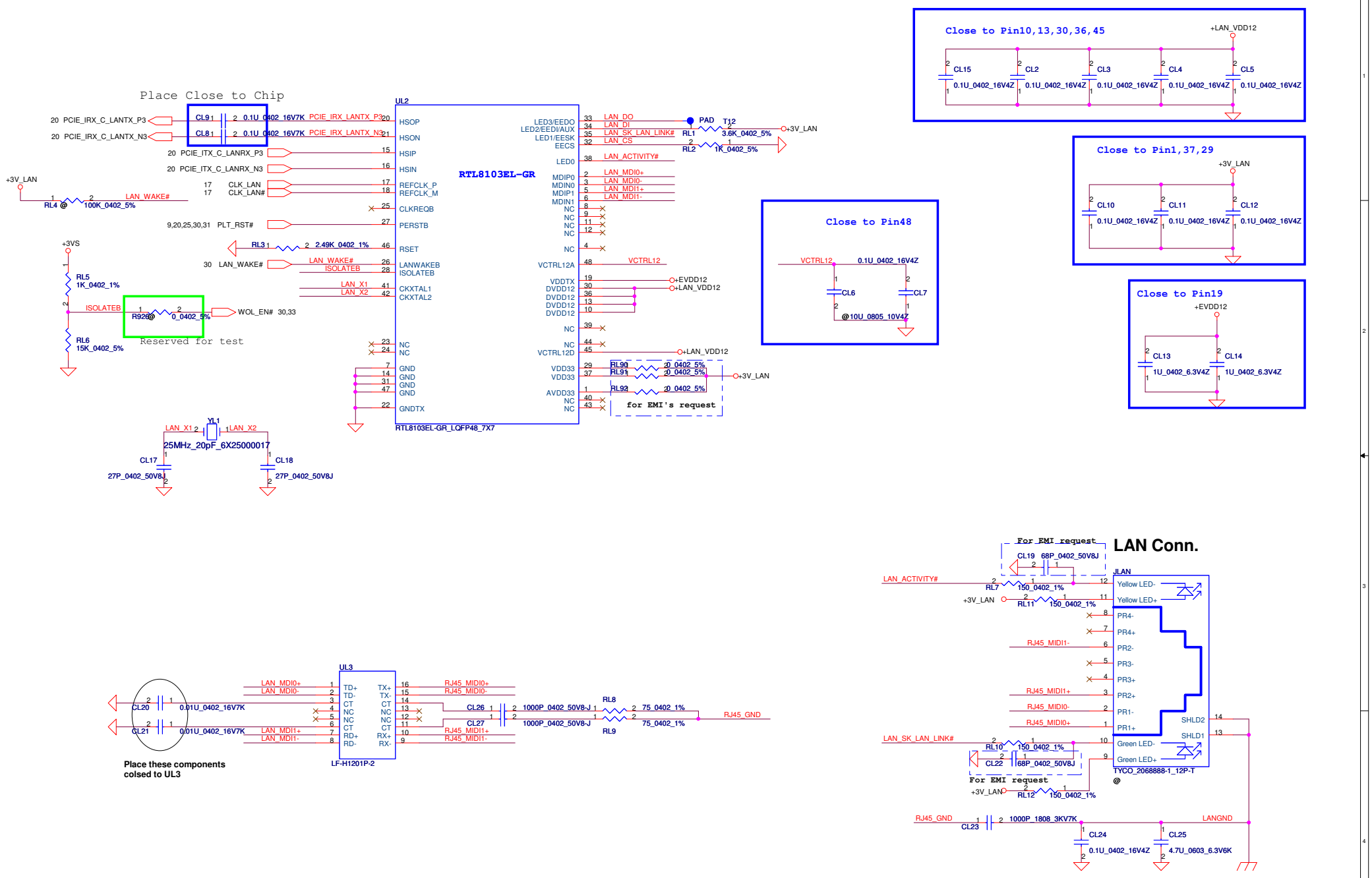

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Compal Electronics, Inc.

Title: **RTL8103EL 10/100 LAN**

Size	Document Number	Rev
Custom	NBWAA LA5821P M/B	1.0

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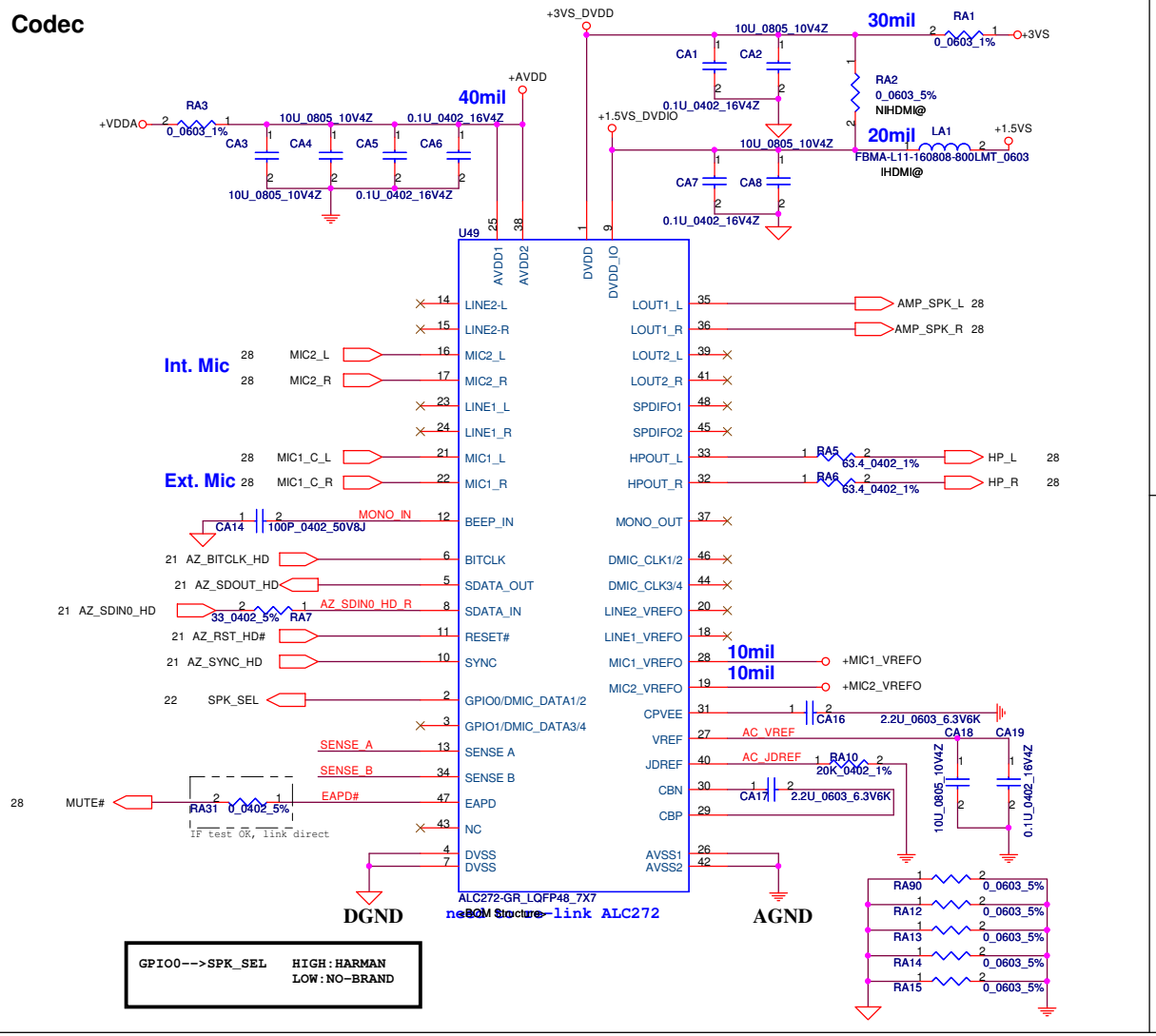
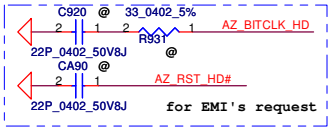
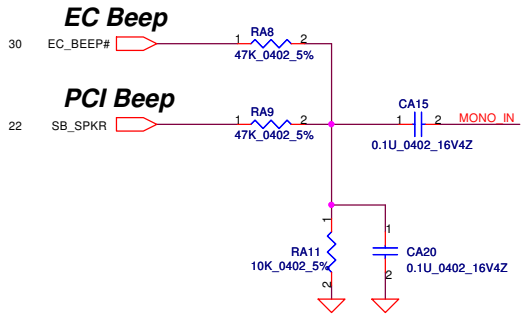
Codec



GPIO0-->SPK_SEL HIGH:HARMAN
LOW:NO-BRAND

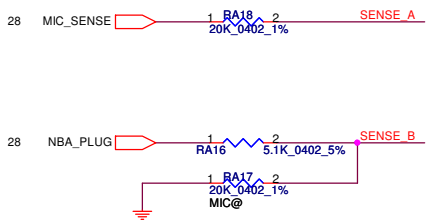


Beep sound



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	FM tuner
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out

place close to chip



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Compal Electronics, Inc.

Title: HD CODEC ALC272

Size | Document Number: NBWAA LA5821P M/B | Rev 1.0

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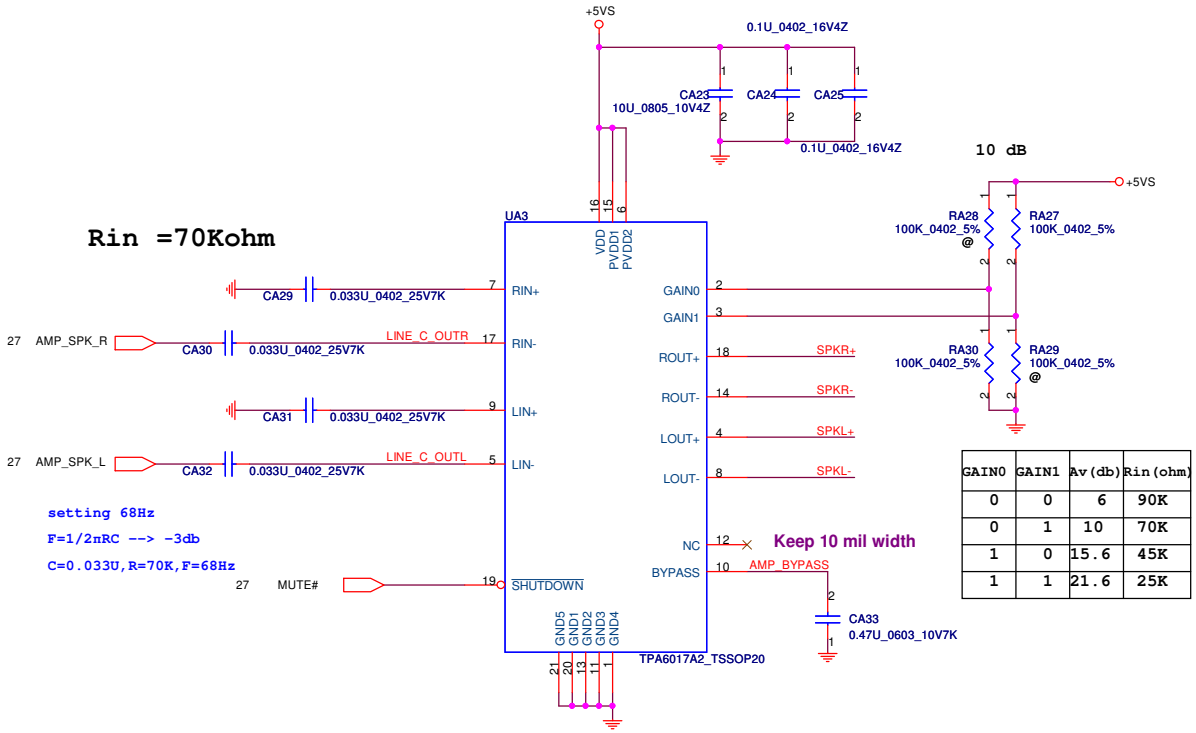
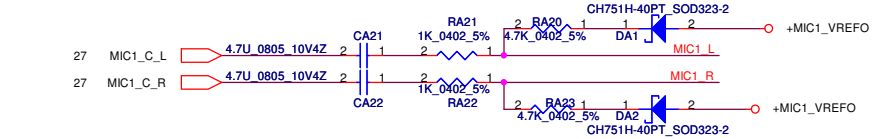
TPA6017 Medium Range Amplifier

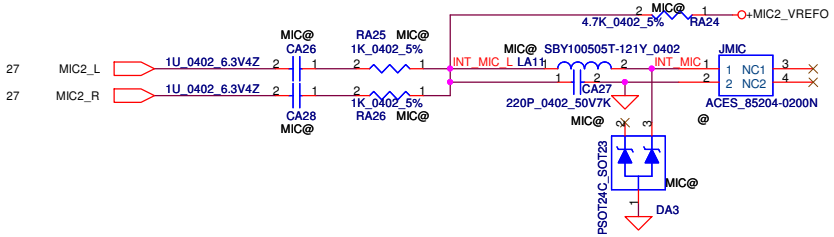


GAIN0	GAIN1	Av(db)	Rin(ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K

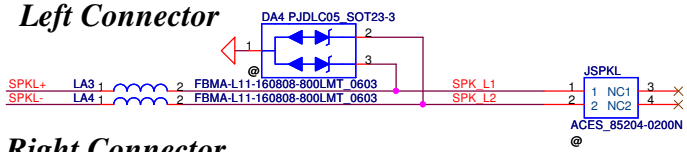
Ext. Mic



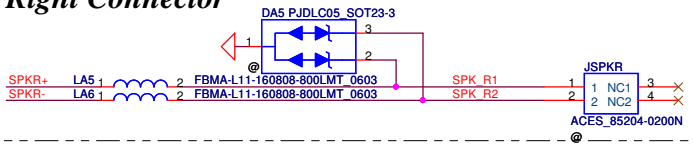
Int. Mic



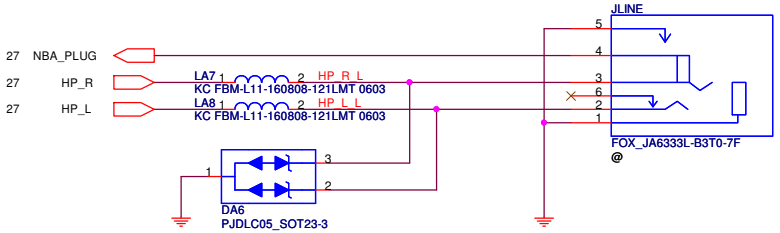
Left Connector



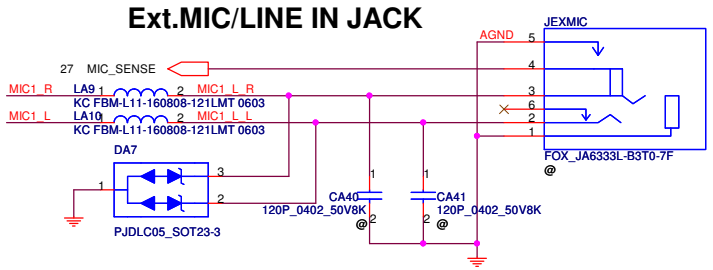
Right Connector



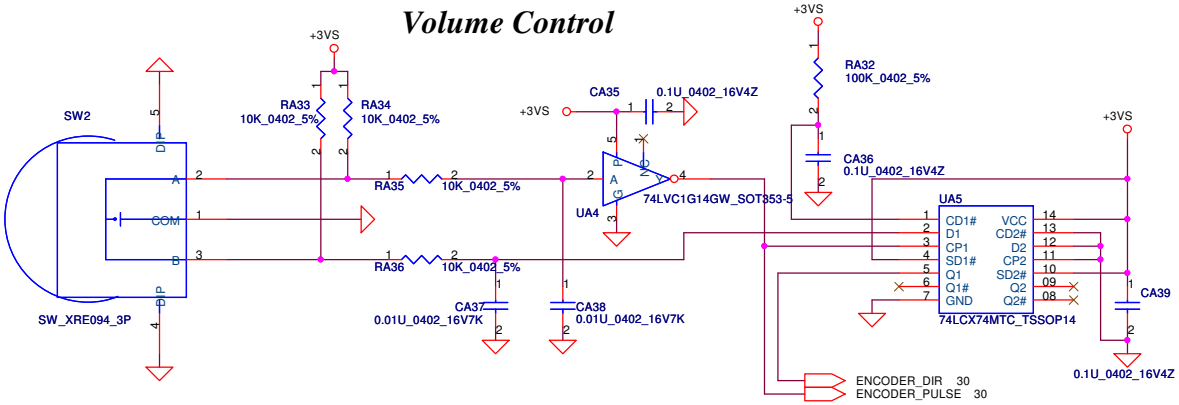
HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK



Volume Control



Security Classification	Compal Secret Data		
Issued Date	2009/07/28	Deciphered Date	2010/07/28

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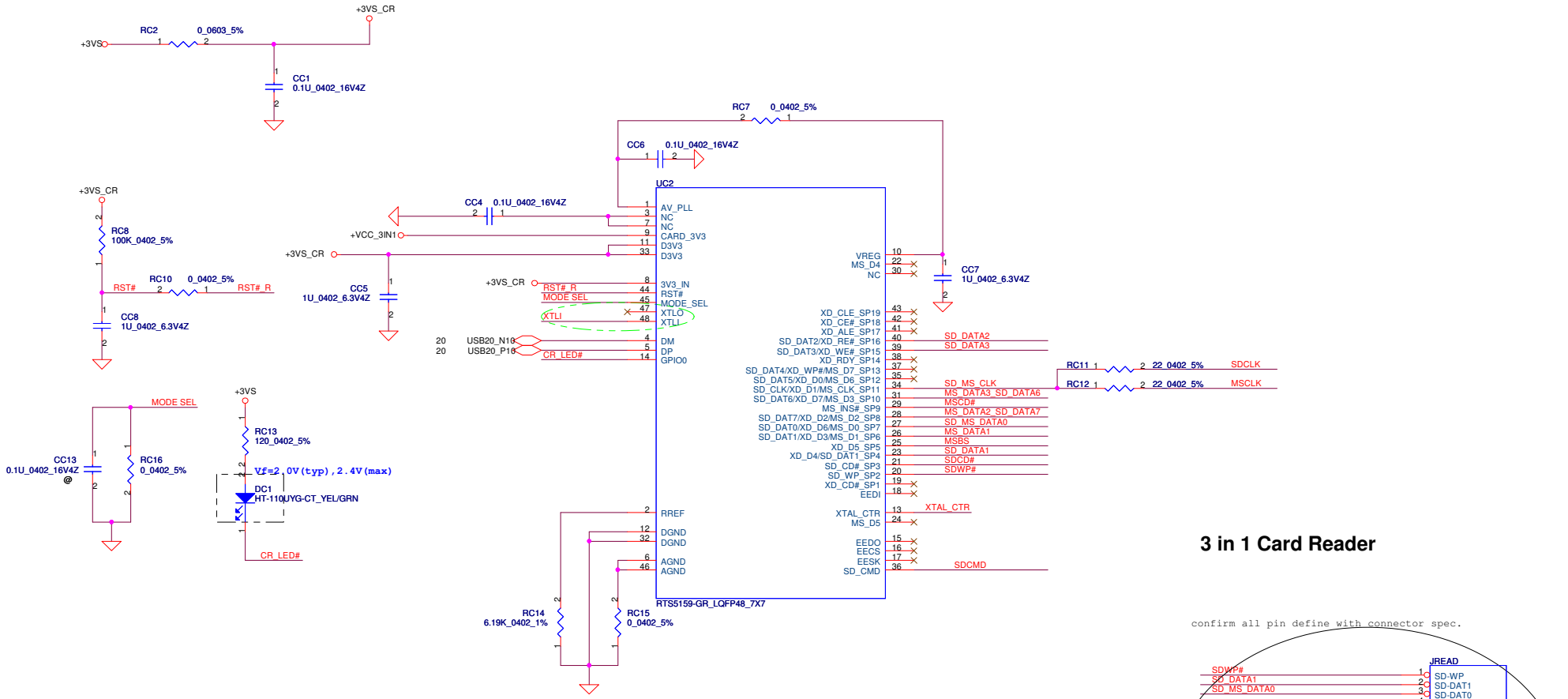
Title: AUDIO AMP/MIC/SPK/VR

Size | Document Number: NBWAA LA5821P M/B | Rev: 1.0

Date: Thursday, August 06, 2009 | Sheet 28 of 41



R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	

Security Classification	Compal Secret Data		
Issued Date	2009/07/28	Deciphered Date	2010/07/28

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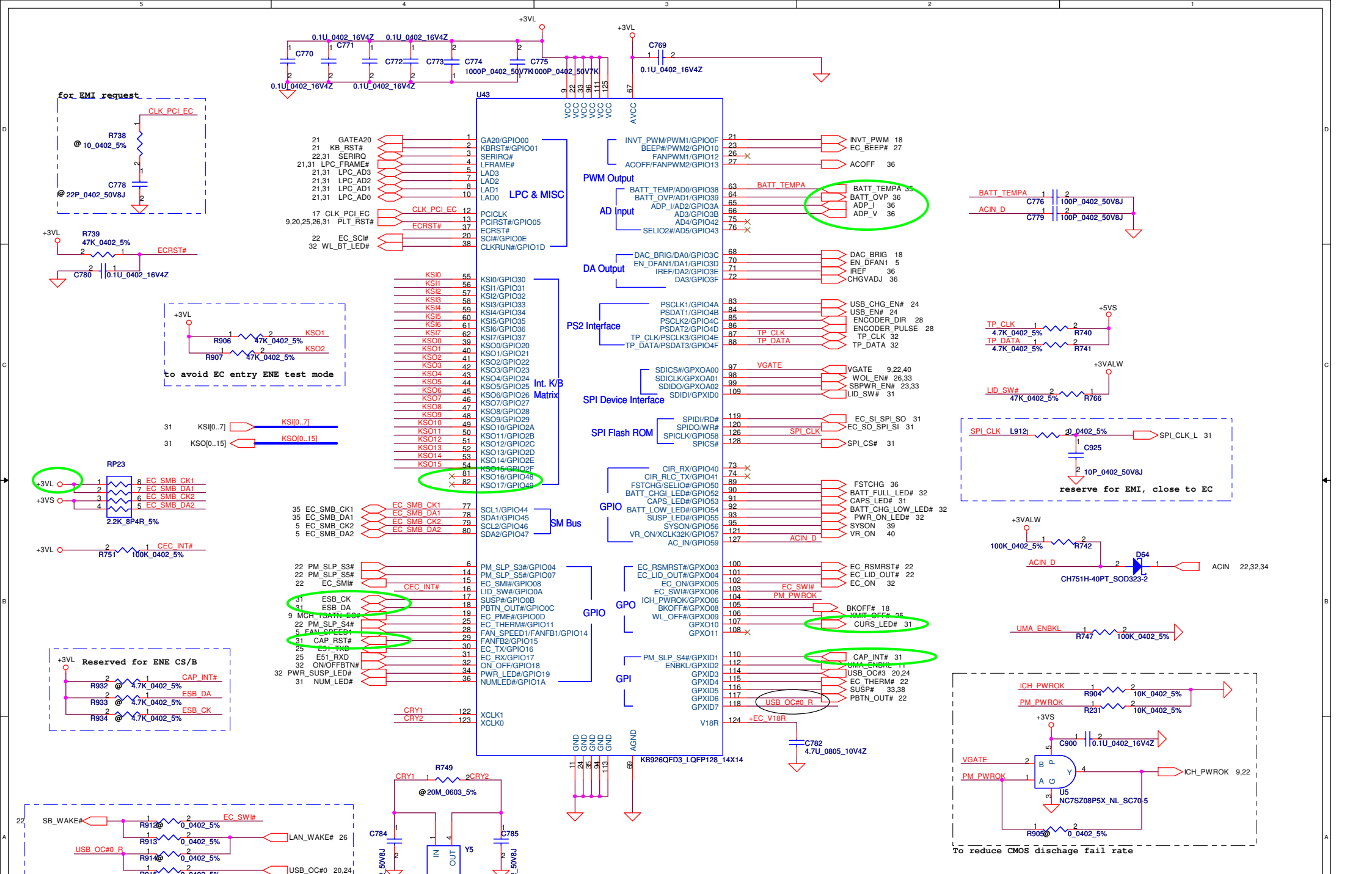
Compal Electronics, Inc.

Title: **RTS5159 Card Reader**

Size: Custom | Document Number: NBWAA LA5821P M/B | Rev: 1.0

Date: Monday, August 10, 2009 | Sheet 29 of 41



Security Classification	Compal Secret Data		
Issued Date	2009/07/28	Deciphered Date	2010/07/28

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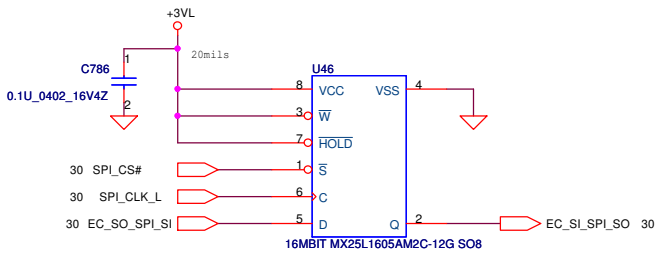
Compal Electronics, Inc.

Title: ENE-KB926 RevD3

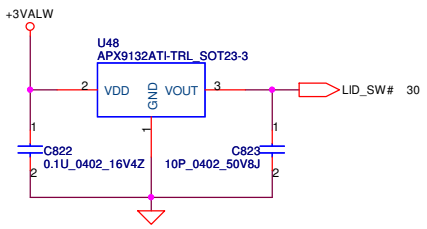
Size | Document Number: NBWAA LA5821P M/B | Rev: 1.0

Date: Monday, August 10, 2009 | Sheet 30 of 41

SPI Flash (16Mb*1)

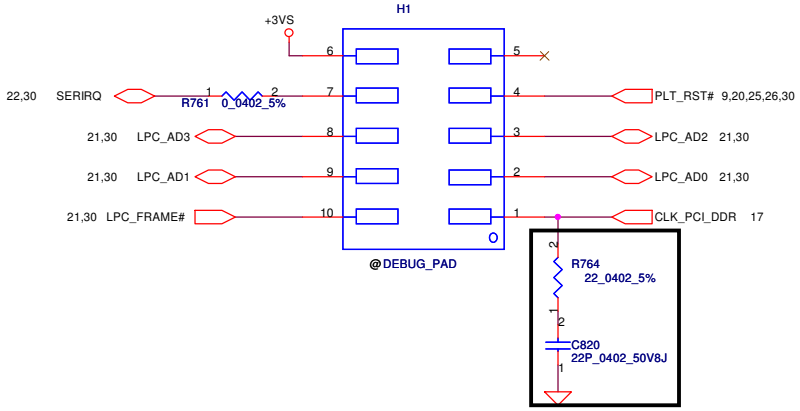


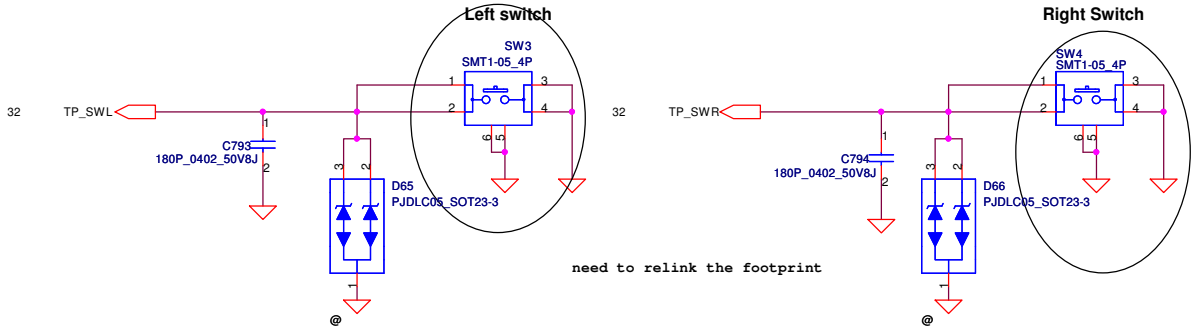
Lid SW



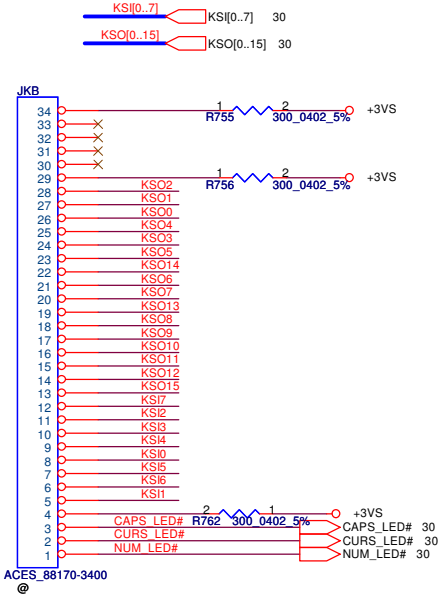
LPC Debug Port

Please place the PAD under DDR DIMM.

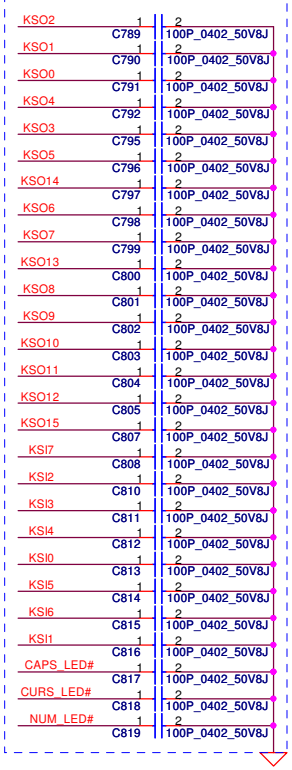




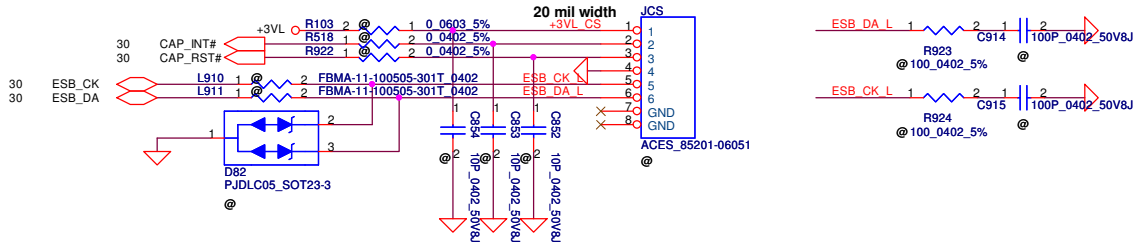
KEYBOARD CONN.



please close to JKB



CS/B Connector



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Issued Date	2009/07/28	Deciphered Date	2010/07/28

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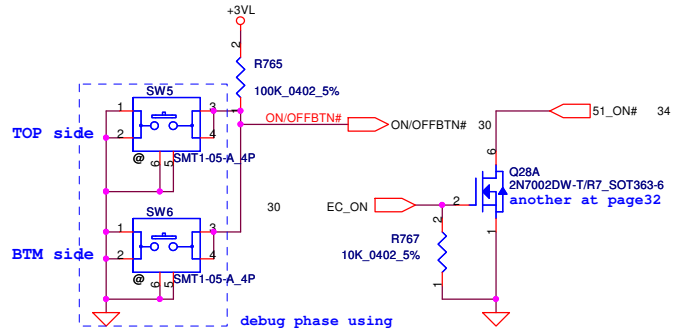
Compal Electronics, Inc.

Title: SPI ROM/TP/KB/Debug/CS Board

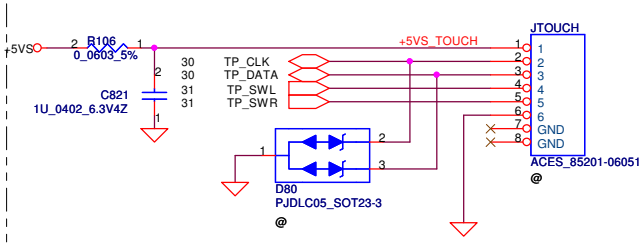
Size | Document Number: NBWAA LA5821P M/B | Rev 1.0

Date: Monday, August 10, 2009 | Sheet 31 of 41

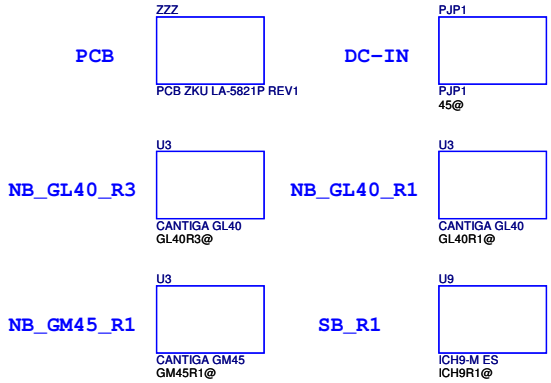
Power Button



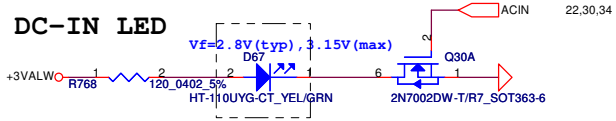
Touch Pad Connector



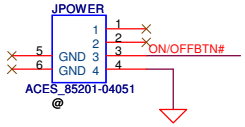
ISPD



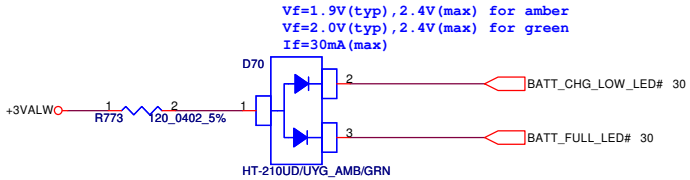
DC-IN LED



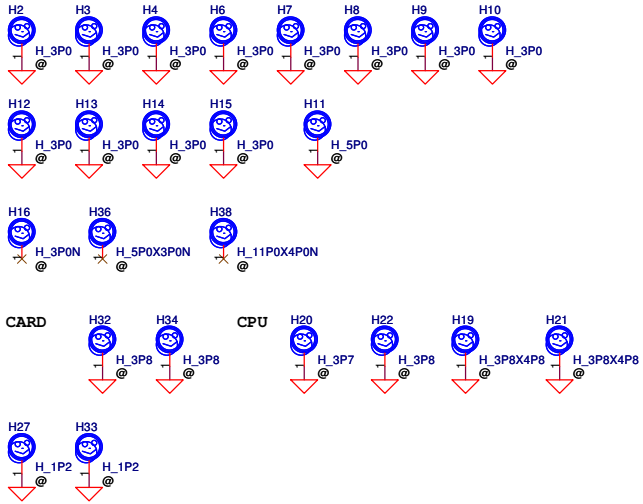
PWR/B



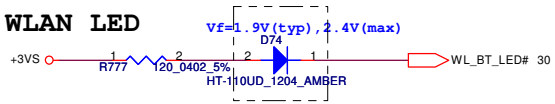
BATT CHARGE/FULL LED



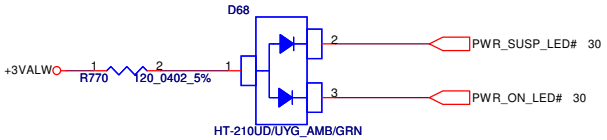
Screw Hole



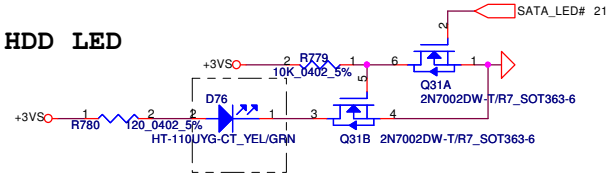
WLAN LED



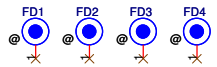
POWER/SUSPEND LED



HDD LED



PCB Fedical Mark PAD



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Compal Electronics, Inc.

Title: Comm. SW/ Sub Conn./LEDS/ISPD

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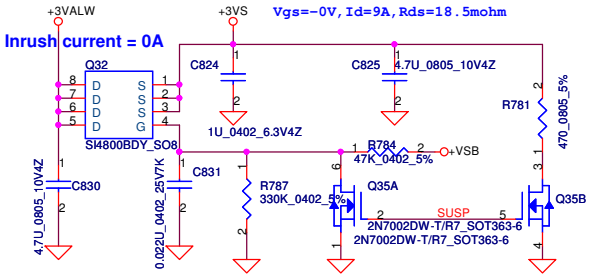
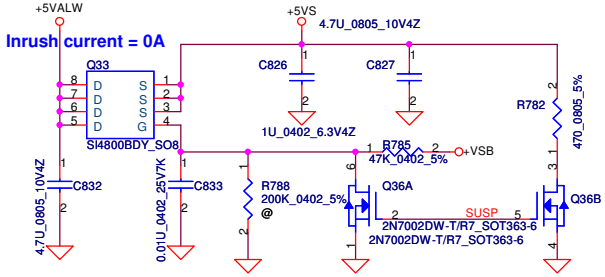
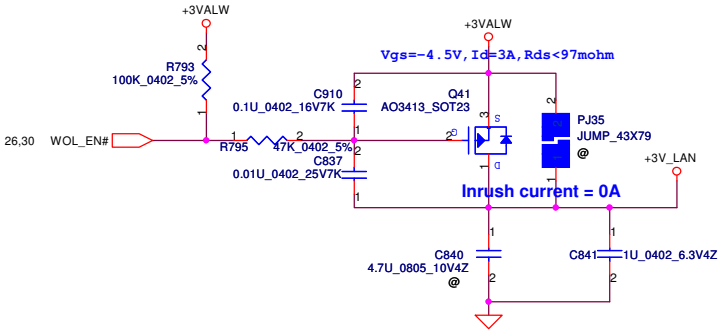
+3VALW TO +3VS



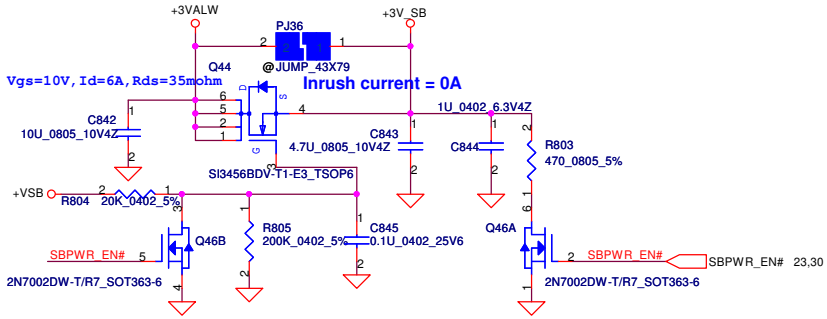
+5VALW TO +5VS

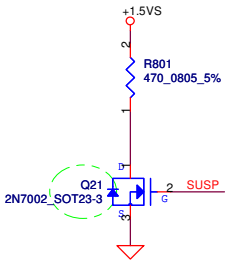


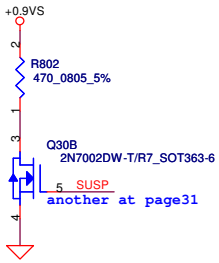
+3VALW TO +3V_LAN

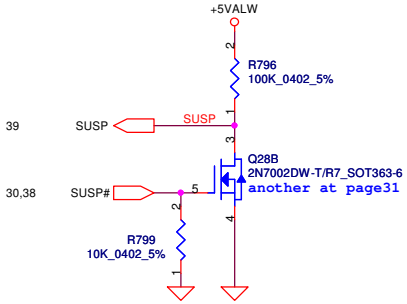


+3VALW TO +3V_SB









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Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size | Document Number: NBWAA LA5821P M/B | Rev: 1.0

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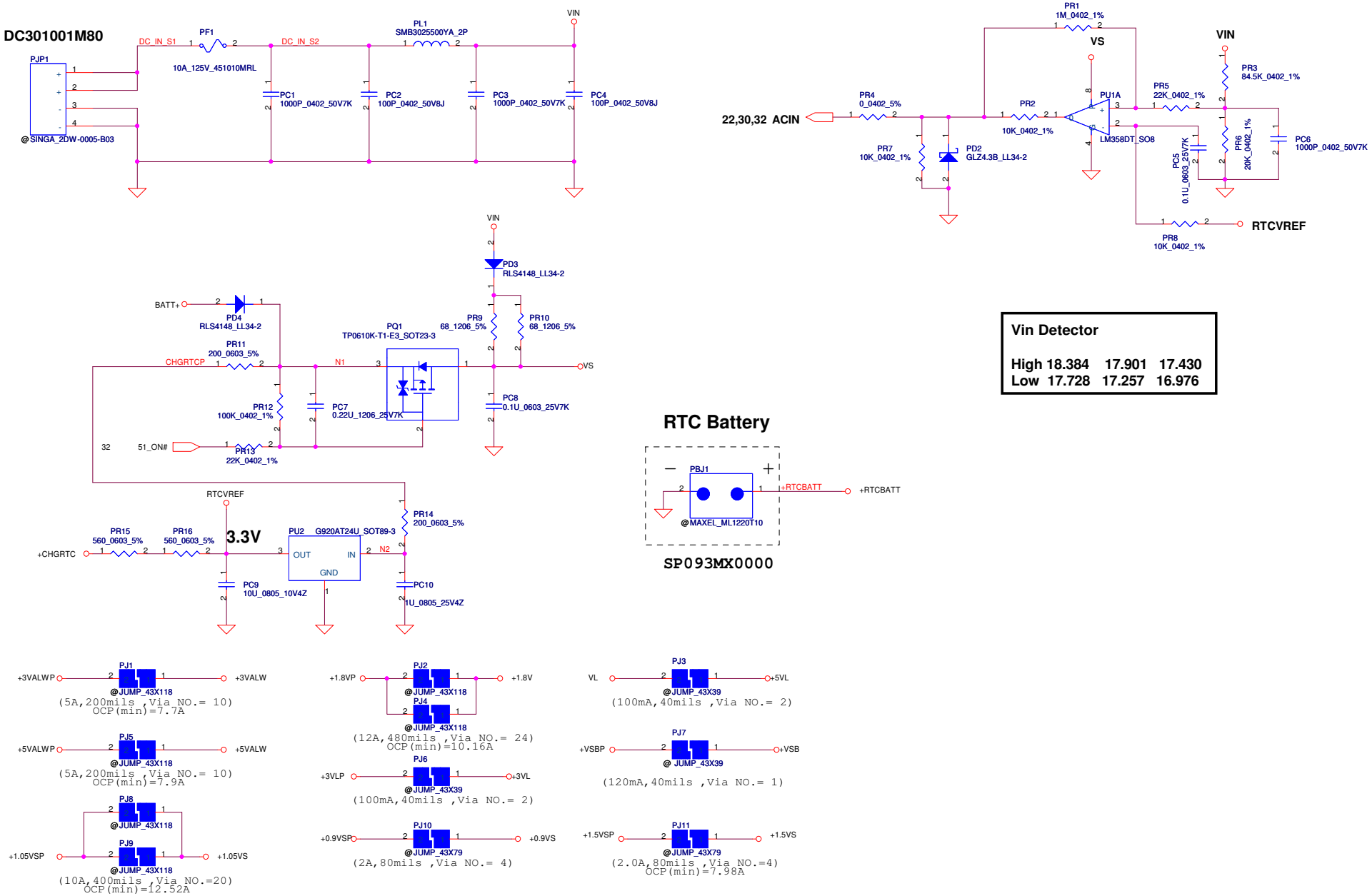

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Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size | Document Number: KTKAA | Rev: 1.0

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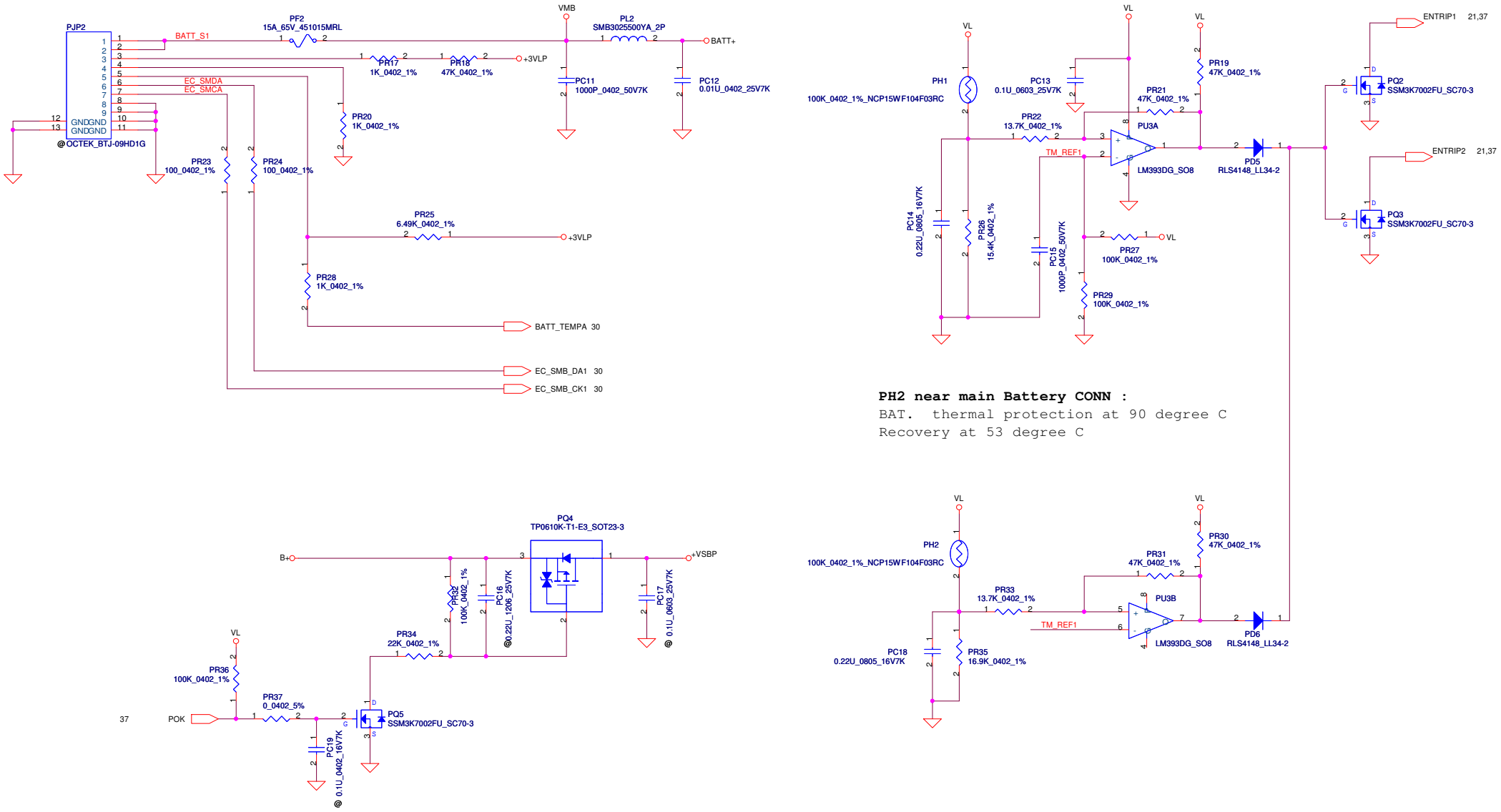

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Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size: | Document Number: KTKAA | Rev: 1.0

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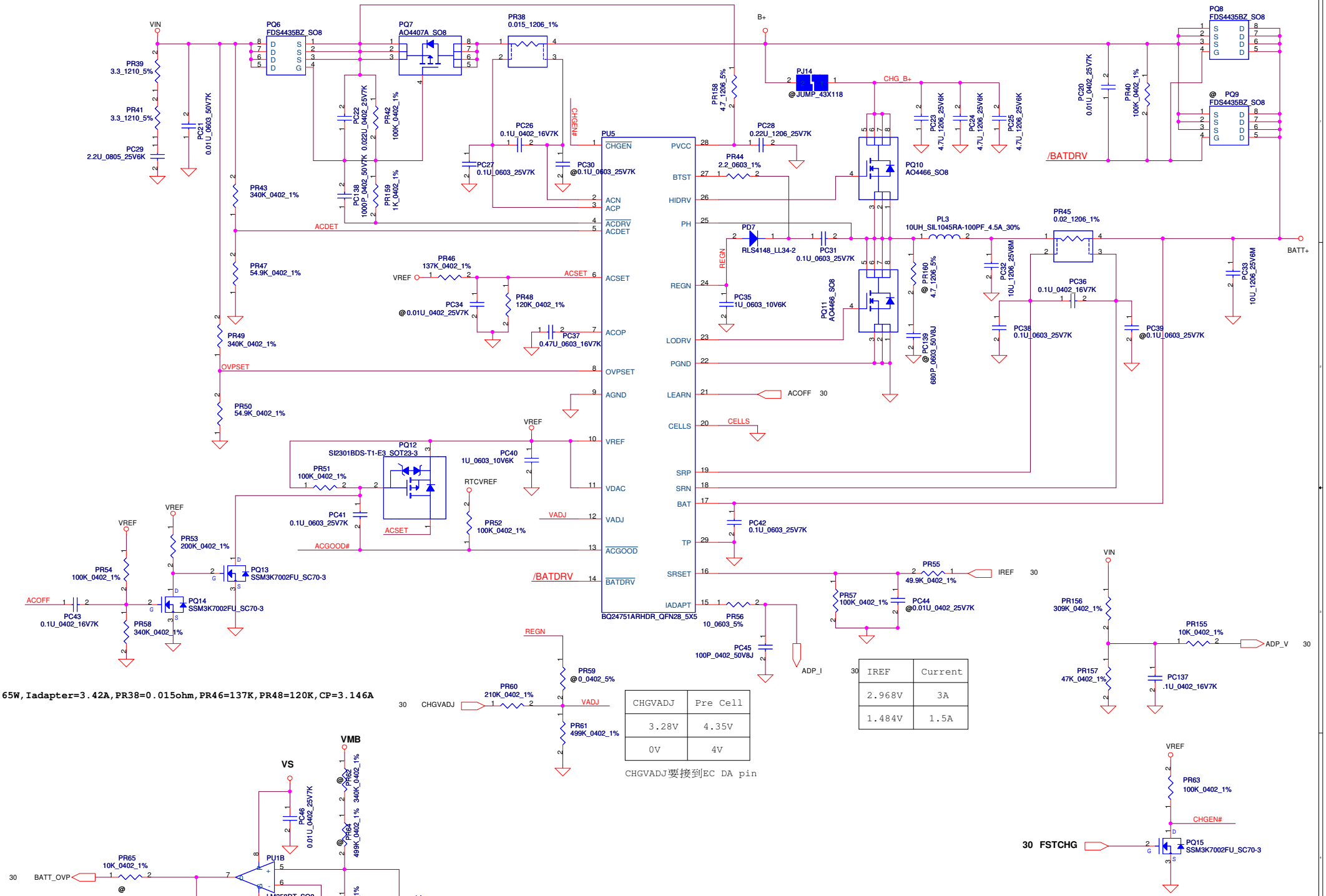

65W,Iadapter=3.42A,PR38=0.015ohm,PR46=137K,PR48=120K,CP=3.146A

CHGVADJ	Pre Cell
3.28V	4.35V
0V	4V

CHGVADJ要接到EC DA pin

IREF	Current
2.968V	3A
1.484V	1.5A

Security Classification	Compal Secret Data		
Issued Date	2009/07/28	Deciphered Date	2010/07/28

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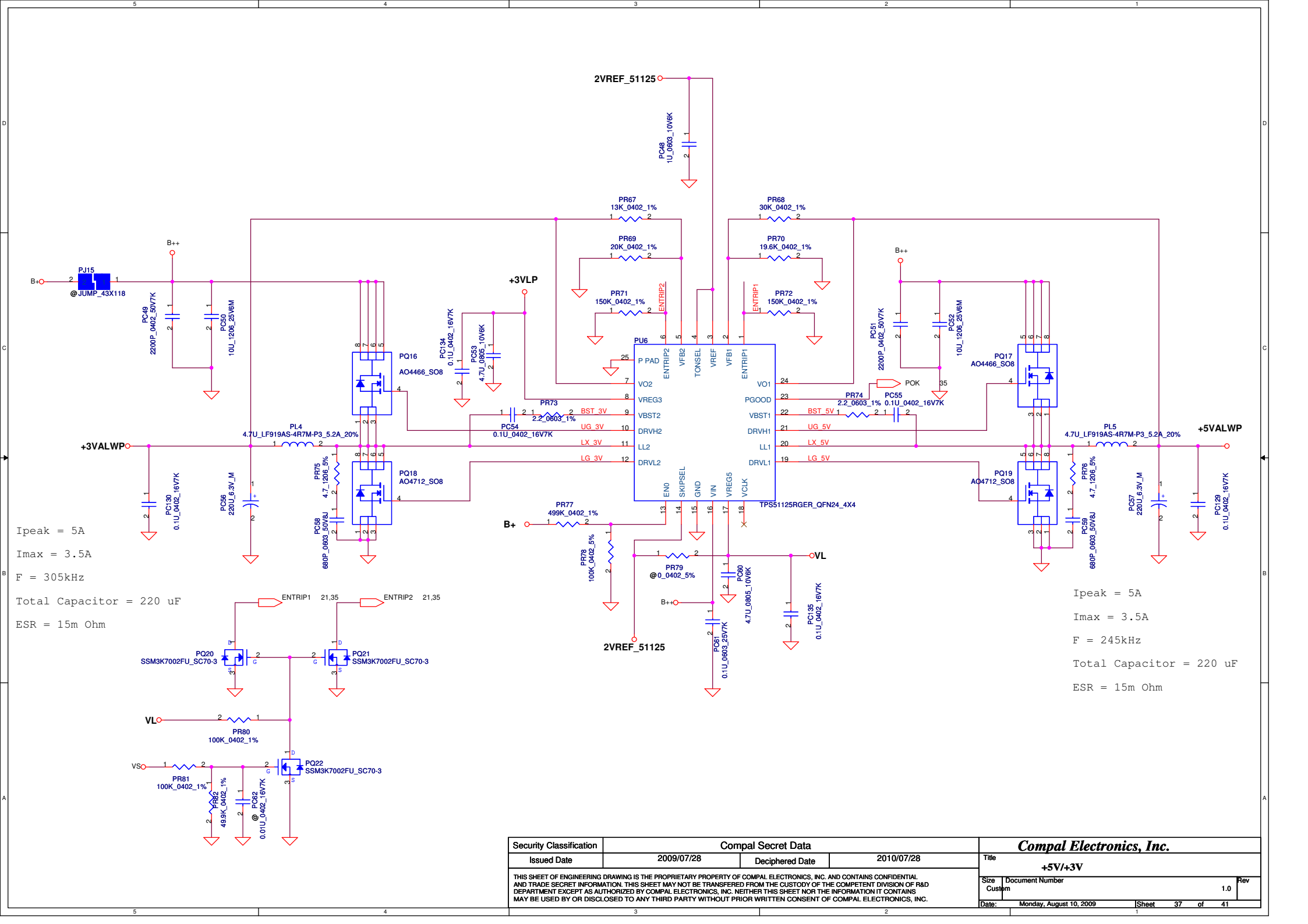
Compal Electronics, Inc.

Title: CHARGER

Size: | Document Number: KTKAA | Rev: 1.0

Date: Monday, August 10, 2009 | Sheet 36 of 41



Security Classification	Compal Secret Data		
Issued Date	2009/07/28	Deciphered Date	2010/07/28

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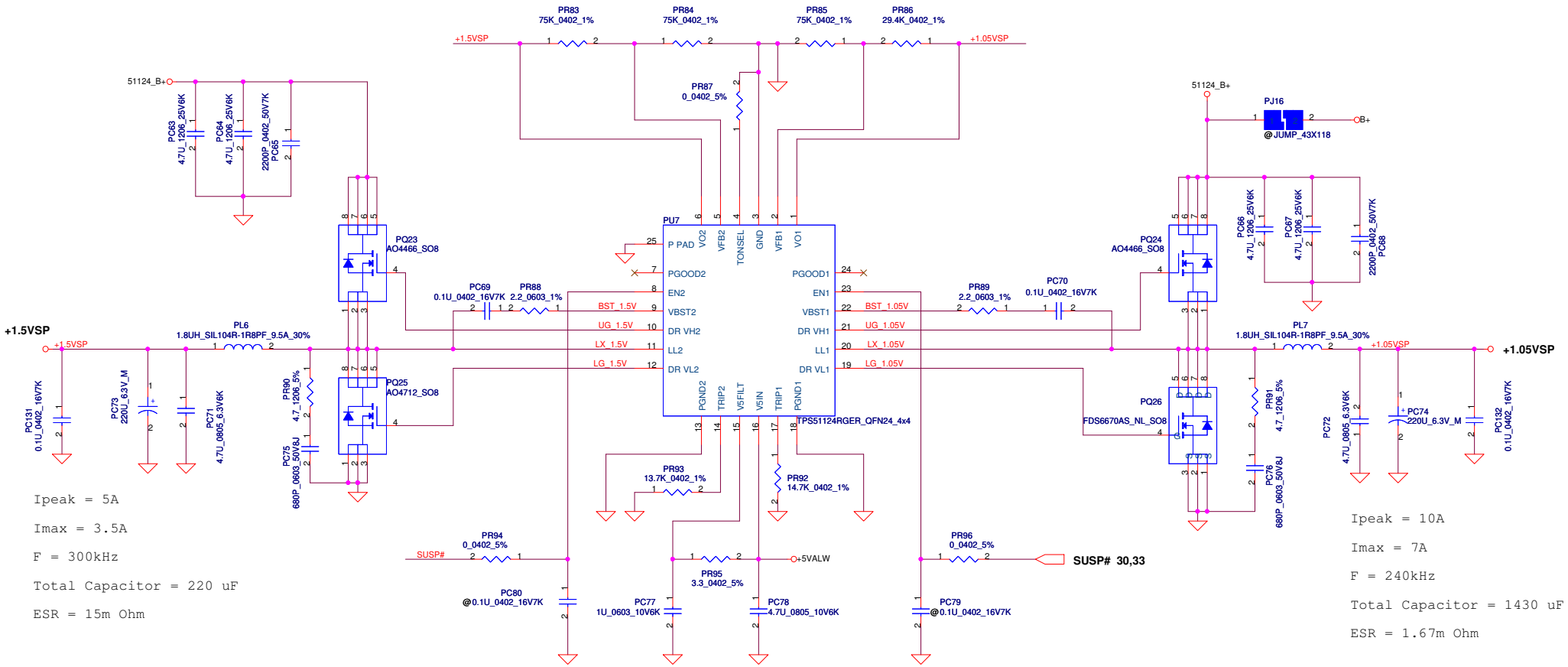
Compal Electronics, Inc.

Title: +5V/+3V

Size: Custom | Document Number | Rev: 1.0

Date: Monday, August 10, 2009 | Sheet 37 of 41



Security Classification	Compal Secret Data		
Issued Date	2009/07/28	Deciphered Date	2010/07/28

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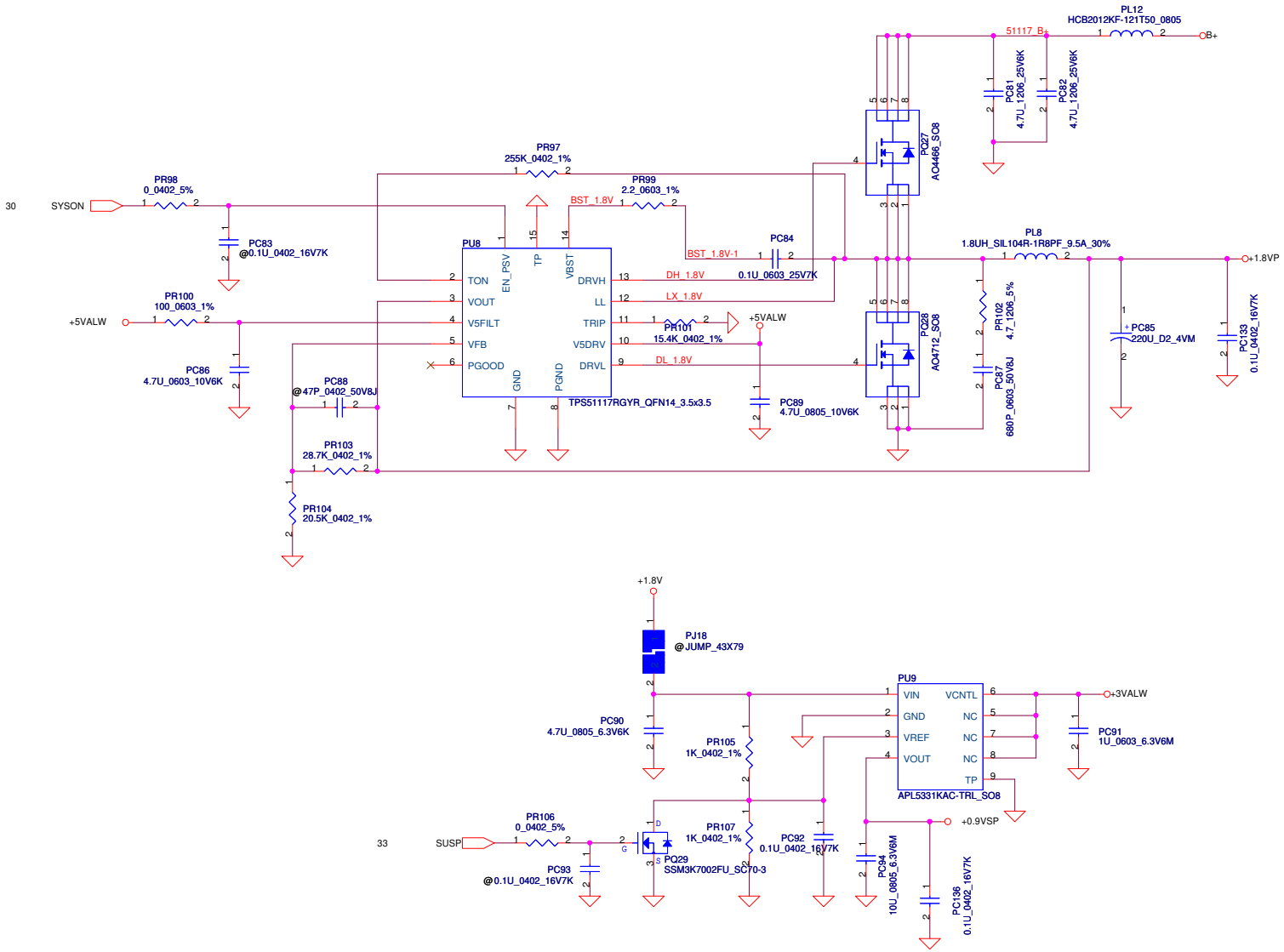
Compal Electronics, Inc.

Title: 1.05V / 1.5V

Size | Document Number | Rev 1.0

Date: Monday, August 10, 2009 | Sheet 38 of 41



Ipeak = 8A

Imax = 5.6A

F = 312kHz

Total Capacitor = 440 uF

ESR = 7.5m Ohm

Security Classification	Compal Secret Data		
Issued Date	2009/07/28	Deciphered Date	2010/07/28

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Title: 1.8V / 0.9V

Size | Document Number | Rev 1.0

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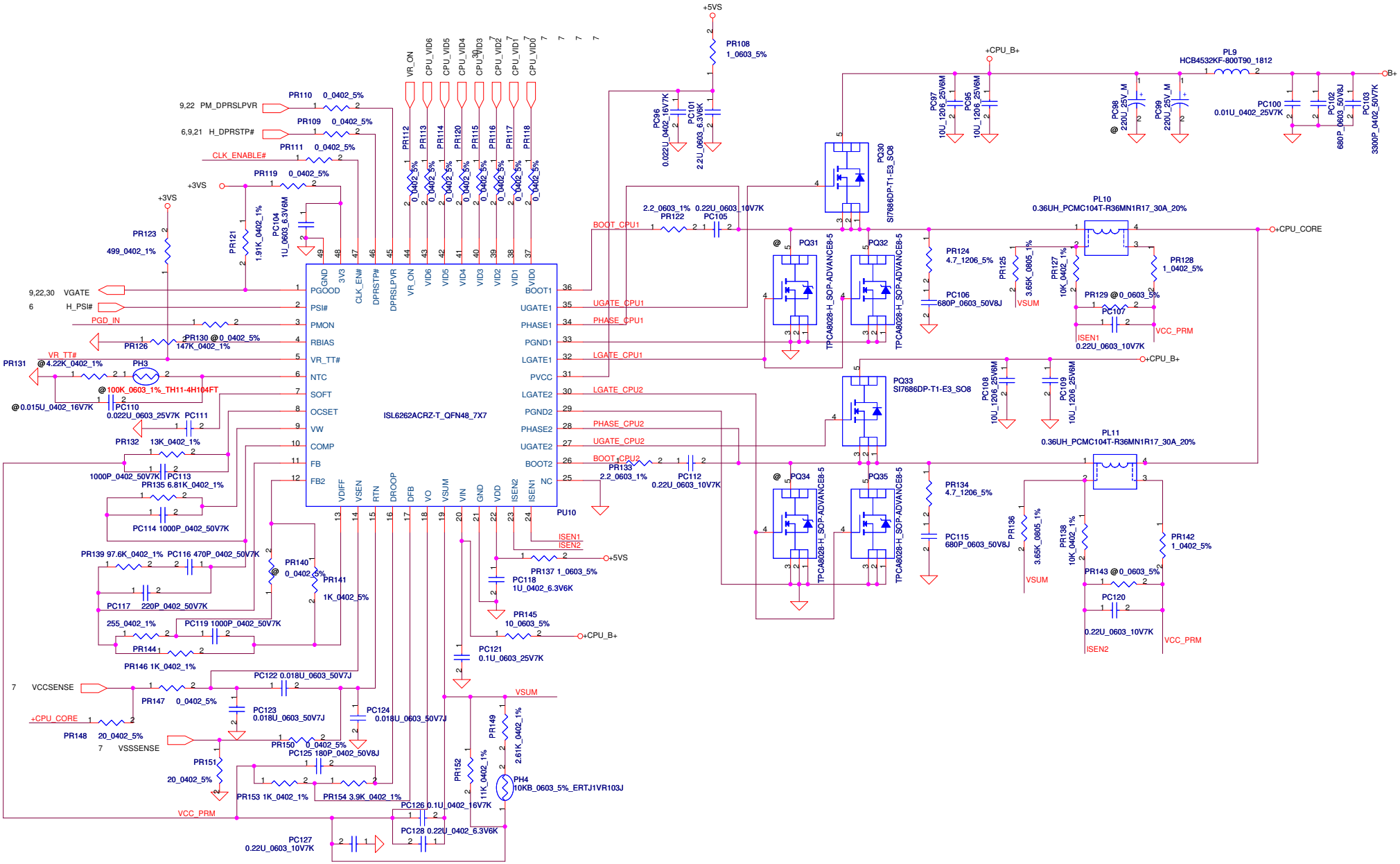

Security Classification	Compal Secret Data		
Issued Date	2009/07/28	Deciphered Date	2010/07/28

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Compal Electronics, Inc.

Title: +CPU_CORE

Size: Custom | Document Number | Rev: 1.0

Date: Monday, August 10, 2009 | Sheet 40 of 41

PIR (Product Improve Record)

NBWAA LA-5821P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	08/06	18	Add R936 on BKOFF#; R937 on INVT_PWM	To prevent EC pin damage
2.	08/06	26	Add RL90, RL91, RL91 on +3V_LAN	For EMI's request
3.	08/06	18	Add C922, C923, C924 220pF on DAC_BRIG, INVT_PWM_R, BKOFF#_R	For EMI's request
4.	08/06	31	Delete R752, C787 on SPI_CLK; Add L912, C925 on SPI_CLK_L	For EMI's request
5.	08/06	28	Add LA11 on INT_MIC_L	For EMI's request
6.	08/06	28	Mount D61, DA3, DA6, DA7	For ESD's request
7.	08/06	32	Un-mount SW5, SW6	Power button, no need after pre-MP

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