LA-1641 REV0.2 Schematic Document

Intel Mobile P4 uFCBGA/uFCPGA Northwood Celeron
with Montara GML / ICH4-M / Integrated VGA

2002-10-22

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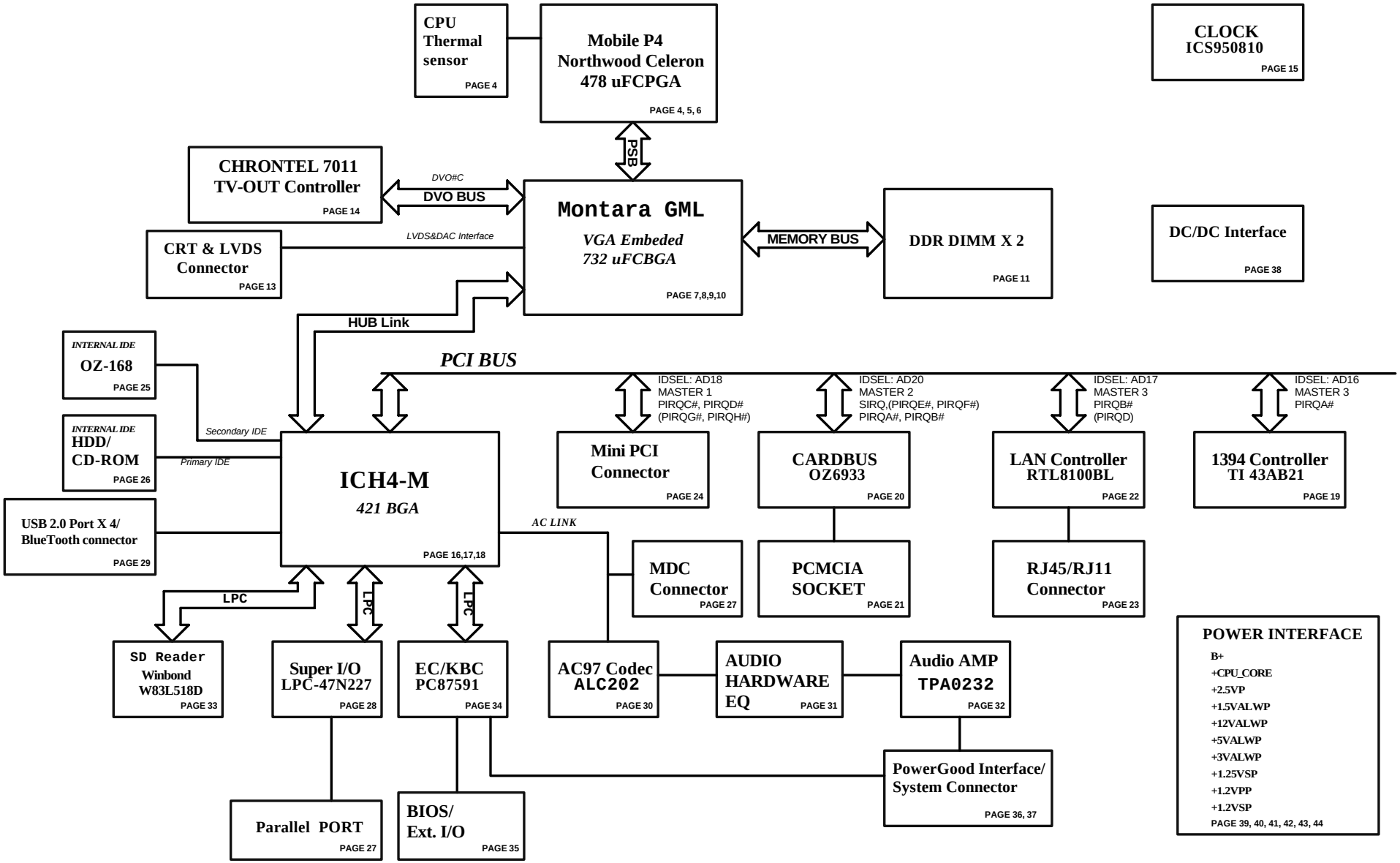
COMPAL CONFIDENTIAL

REV:0.1



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_VCC	Core voltage for CPU	ON	OFF	OFF
+1.2VP	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.2VS	1.2V switched power rail for Montara core	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB(PIRQE/PIRQF)
LAN	AD17	3	PIRQB(PIRQD)
Mini-PCI	AD18	1/1	PIRQC/PIRQD(PIRQG/PIRQH)
1394	AD16	0	PIRQA

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
(24C04)	1011 000Xb

EC SM Bus2 address

Device	Address
ADM1032	1001 110X b
OZ168	0011 0100 b
Smart Battery	0001 011X b
Docking	0011 011X b
DOT Board	XXXX XXXXb

ICH4 SM Bus address

Device	Address
Clock Generator (ICS-950810)	1101 001X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	0.6
6	0.7
7	0.8

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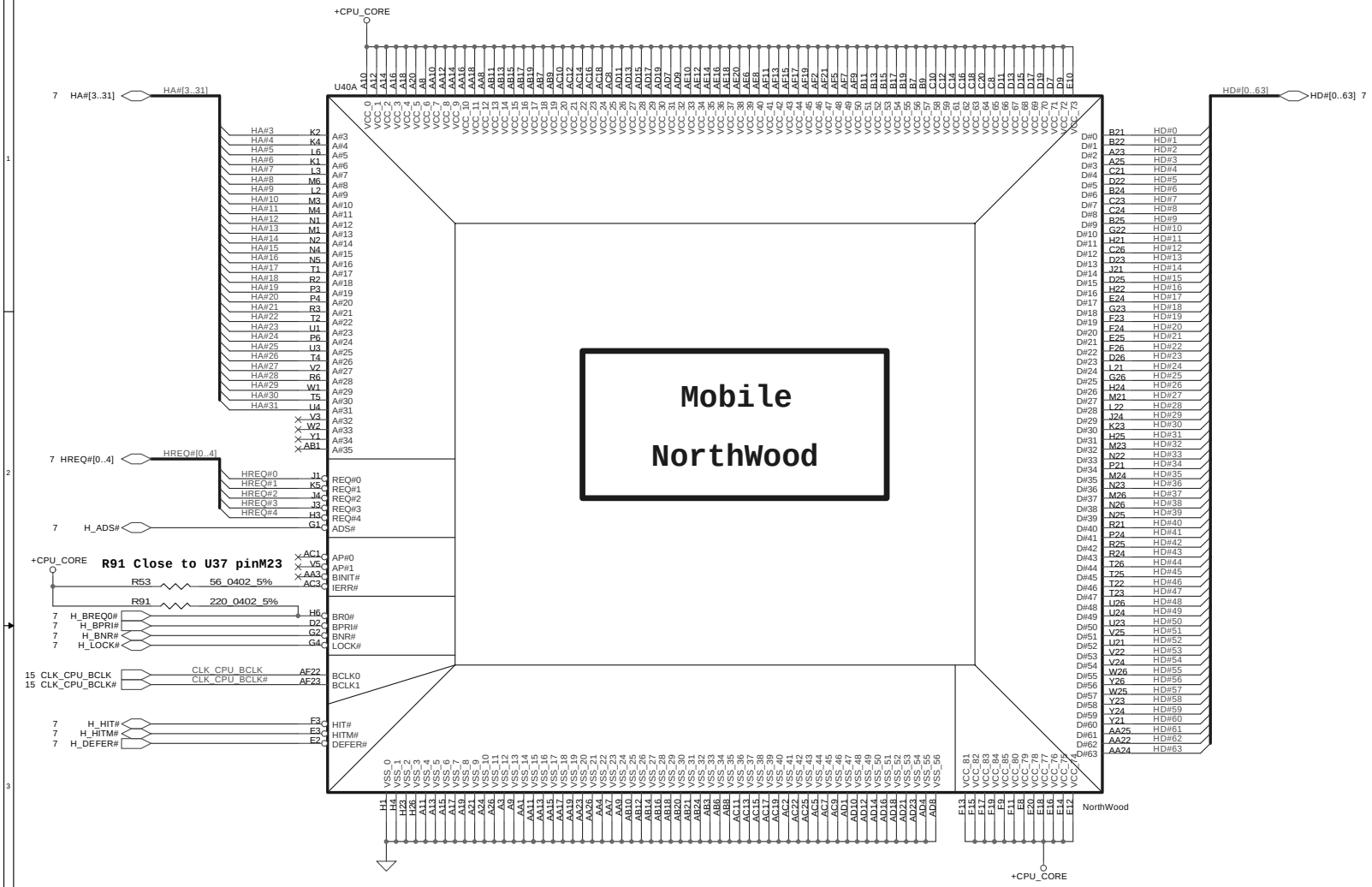
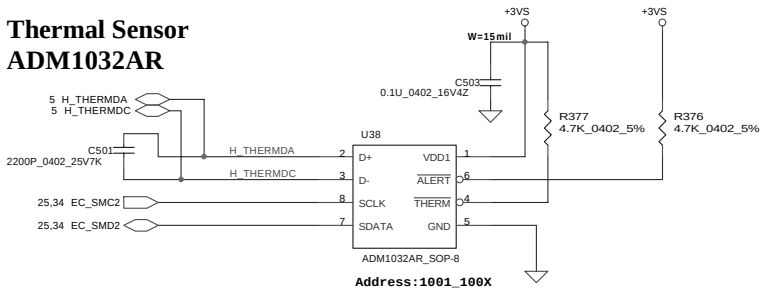


Thermal Sensor
ADM1032AR



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Title	Mobile P4-Celeron (1/2)	
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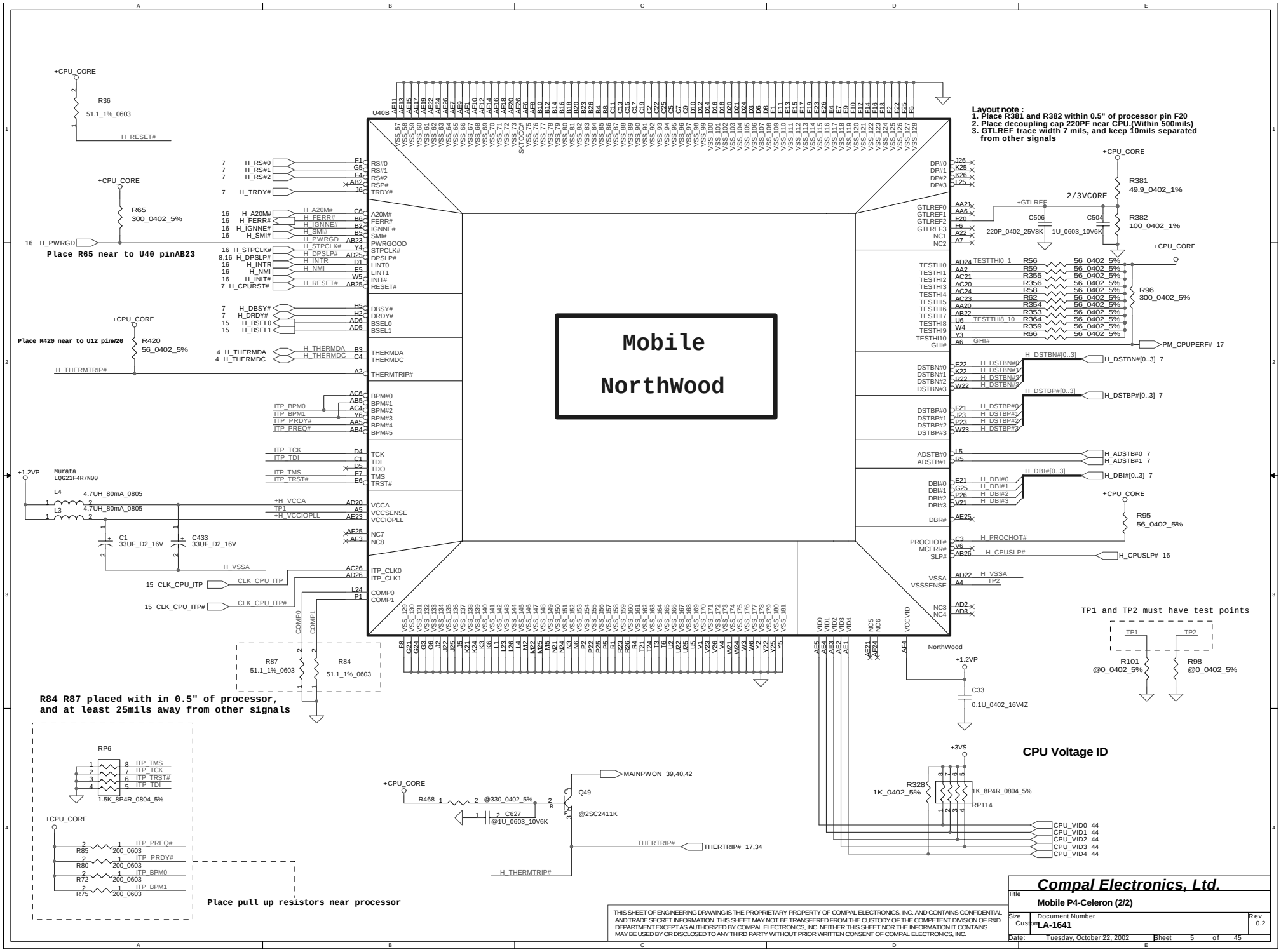
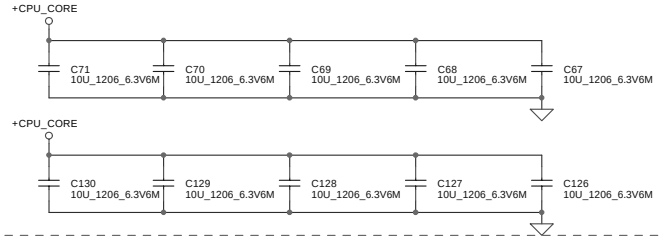

Mobile
NorthWood
U40B
Layout note :
1. Place R381 and R382 within 0.5" of processor pin F20
2. Place decoupling cap 220PF near CPU.(Within 500mils)
3. GTLREF trace width 7 mils, and keep 10mils separated from other signals
Place R65 near to U40 pinAB23
Place R420 near to U12 pinW20
R84 R87 placed with in 0.5" of processor, and at least 25mils away from other signals
Place pull up resistors near processor
TP1 and TP2 must have test points
CPU Voltage ID
NorthWood
Compal Electronics, Ltd.
Mobile P4-Celeron (2/2)
LA-1641
Tuesday, October 22, 2002

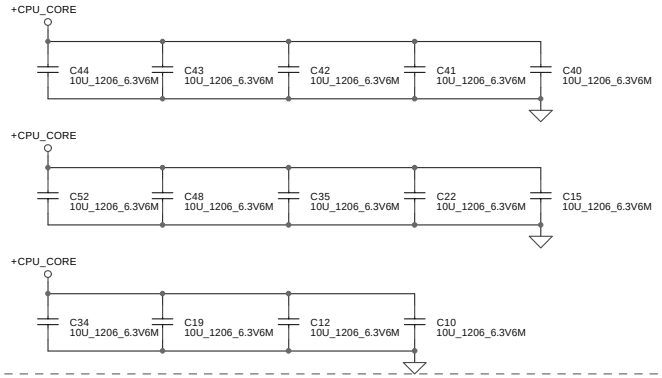
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

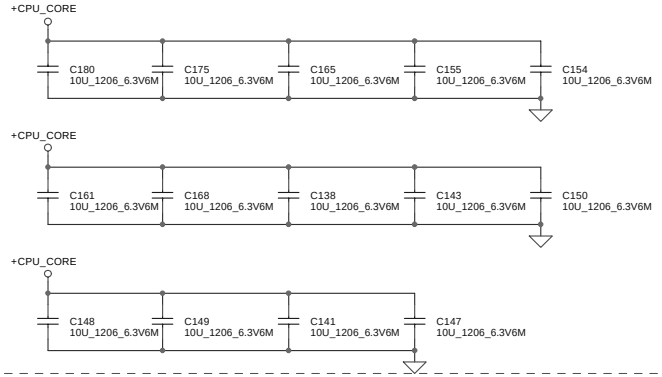
Please place these cap in the socket cavity area



Please place these cap on the socket north side



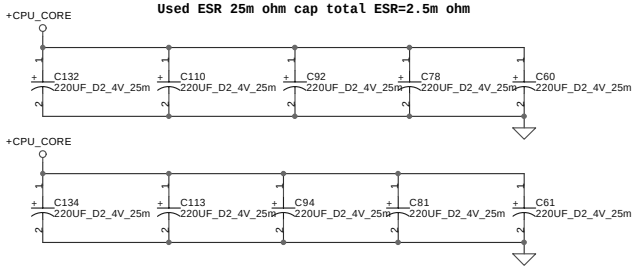
Please place these cap on the socket south side

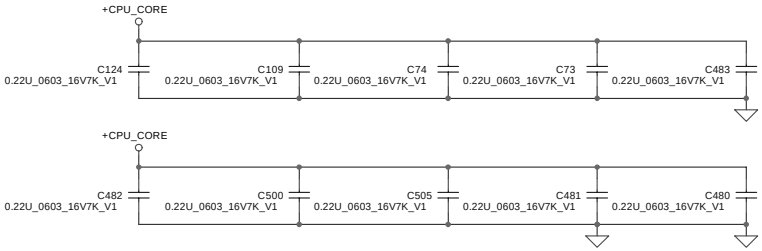


Layout note :

Place close to CPU power and ground pin as possible (<1inch)

Used ESR 25m ohm cap total ESR=2.5m ohm





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Title: **CPU Decoupling**		
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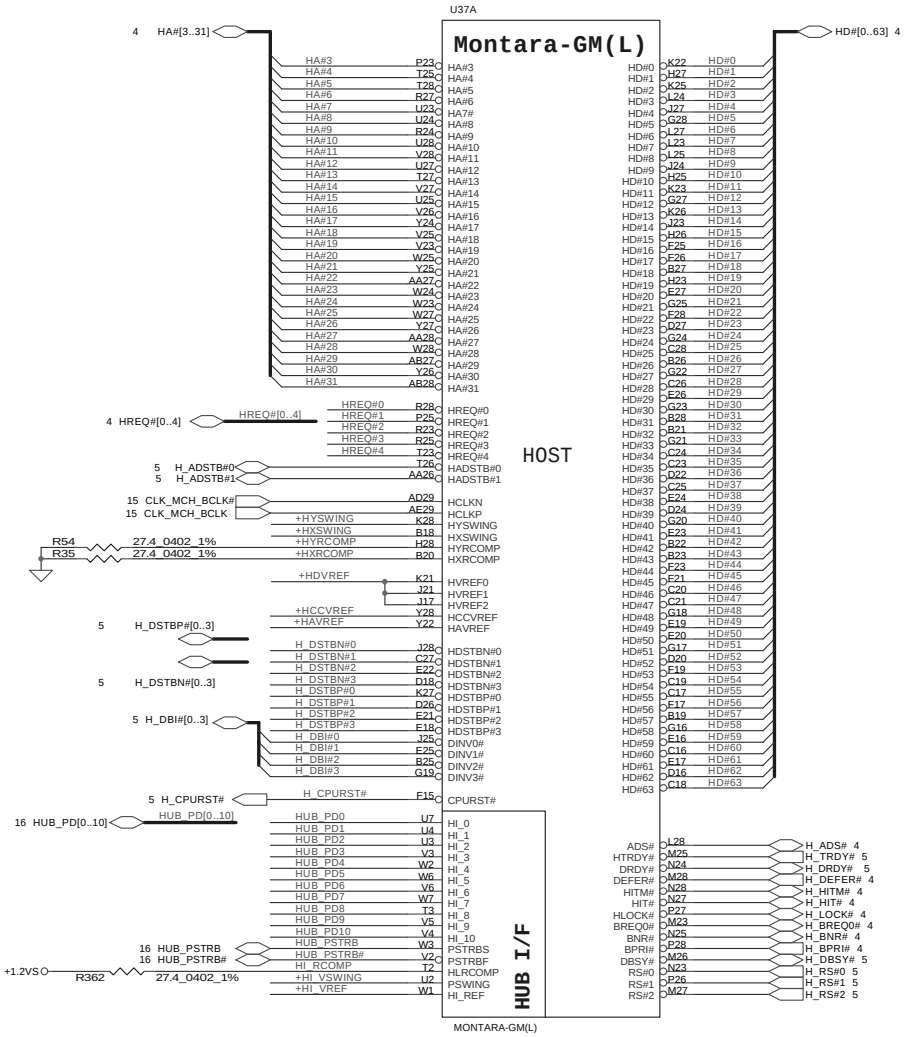
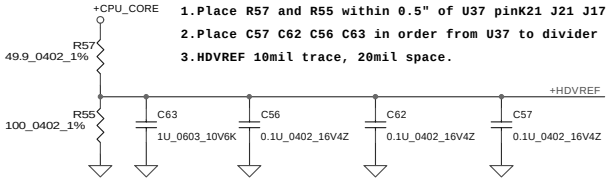
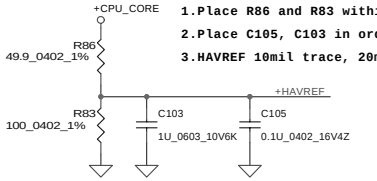


Host data Ref. Voltage



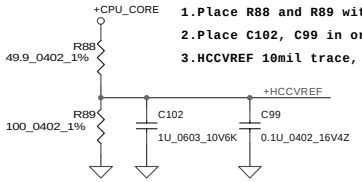
1.Place R57 and R55 within 0.5" of U37 pinK21 J21 J17
2.Place C57 C62 C56 C63 in order from U37 to divider
3.HDVREF 10mil trace, 20mil space.

Host address Ref. Voltage



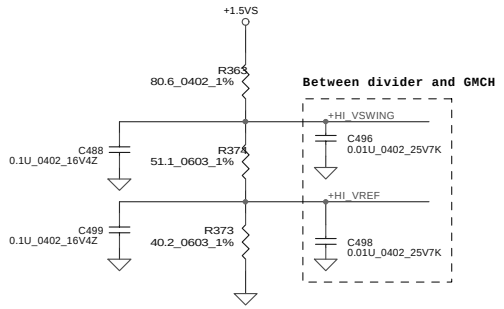
1.Place R86 and R83 within 0.5" of U37 pinY22
2.Place C105, C103 in order from U37 to divider
3.HAVREF 10mil trace, 20mil space.

Host common clock Ref. Voltage



1.Place R88 and R89 within 0.5" of U37 pinY28
2.Place C102, C99 in order from U37 to divider
3.HCCVREF 10mil trace, 20mil space.

HUB I/F REF VOLTAGE



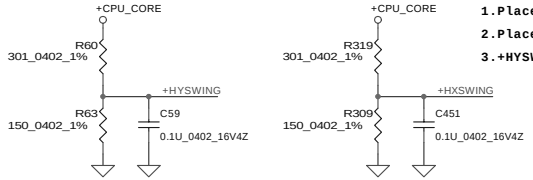
Place this schematic close to GMCH

Layout Note:

1.Place R35 and R54 within 0.5" of U37 pinH28 B20

2.Both HYRCOMP and HXRCOMP trace width are 18mil and 25mils away from other signals

HXSWING and HYSWING Ref. Voltage



1.Place R60 and R63 within 0.5" of U37 pinK28
2.Place R319 and R309 within 0.5" of U37 pinB18
3.+HYSWING, +HXSWING 10mil trace, 20mil space.

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Title	Montara-GML (HOST)	
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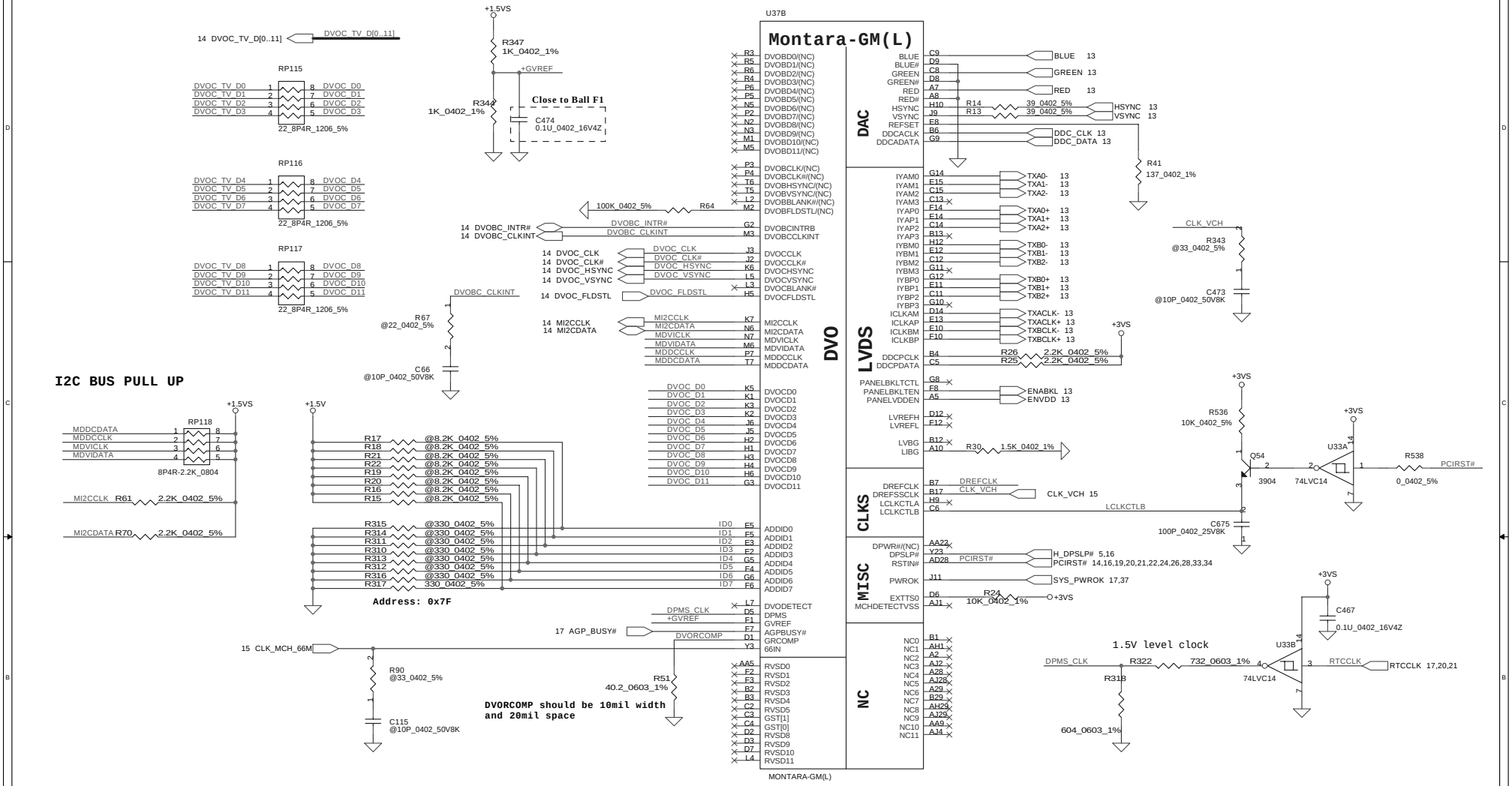
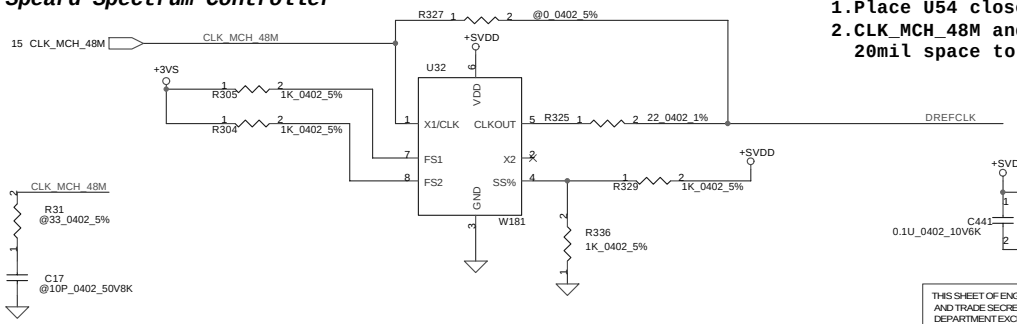
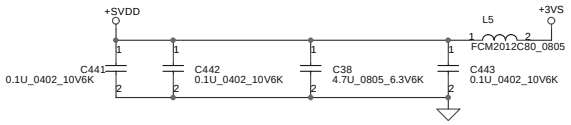


Speard Spectrum Controller



Layout Note:

1. Place U54 close to U3
2. CLK_MCH_48M and DREFCLK 5mil Trace and keep 20mil space to other signal.



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Title	Montara-GML (LVDS)	
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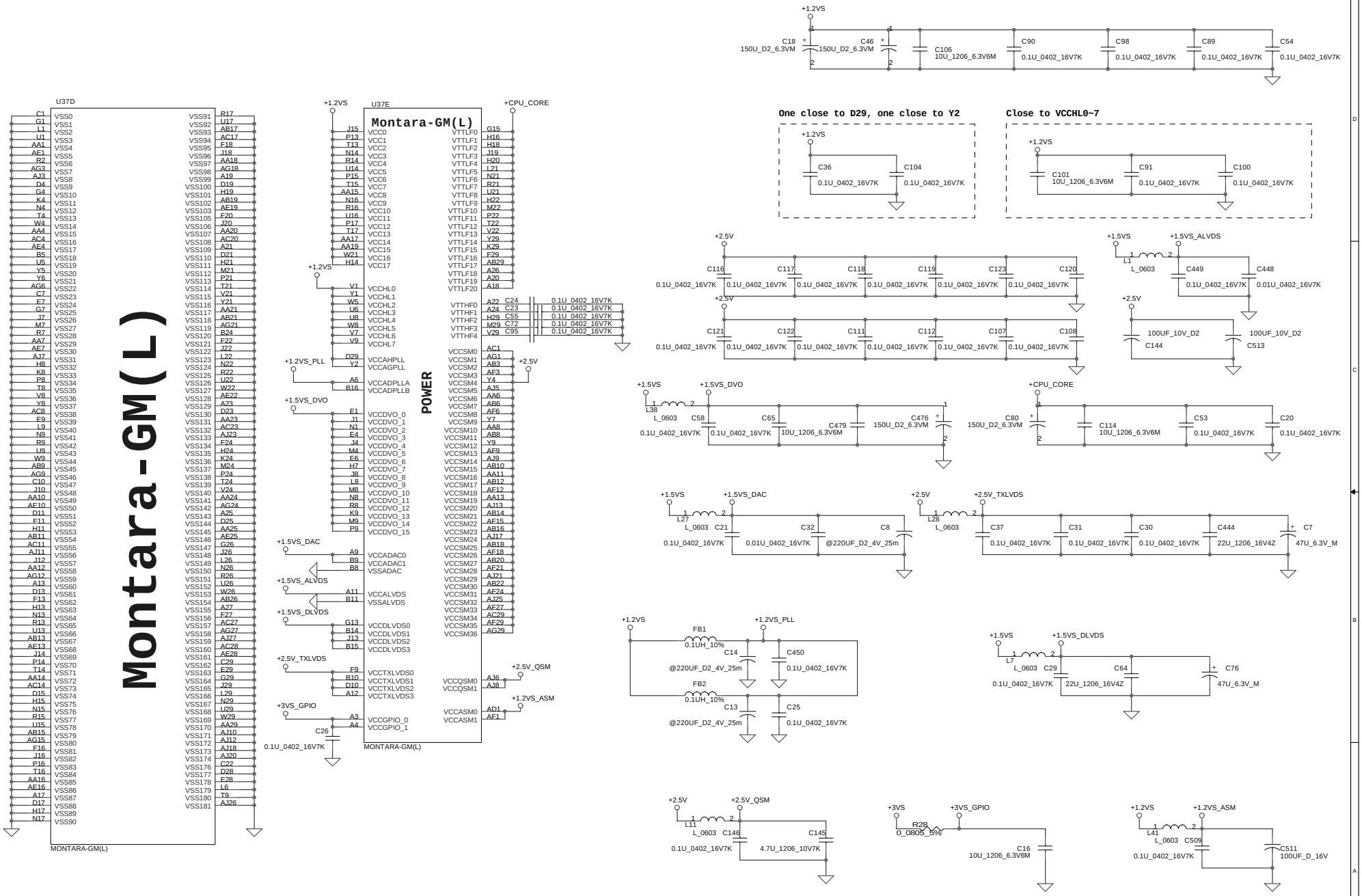

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Title	Montara-GML (POWER)
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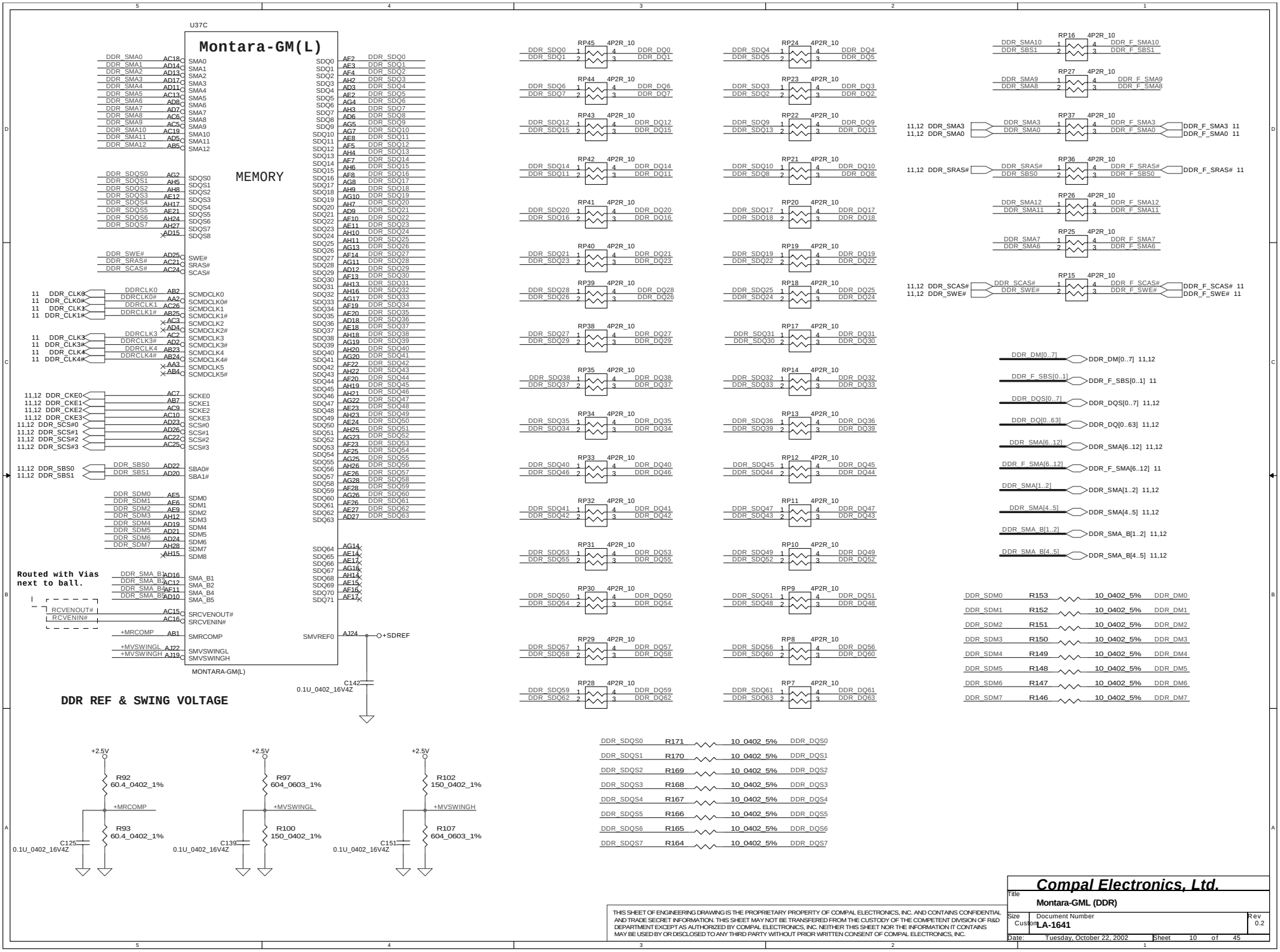

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Title	Montara-GML (DDR)		
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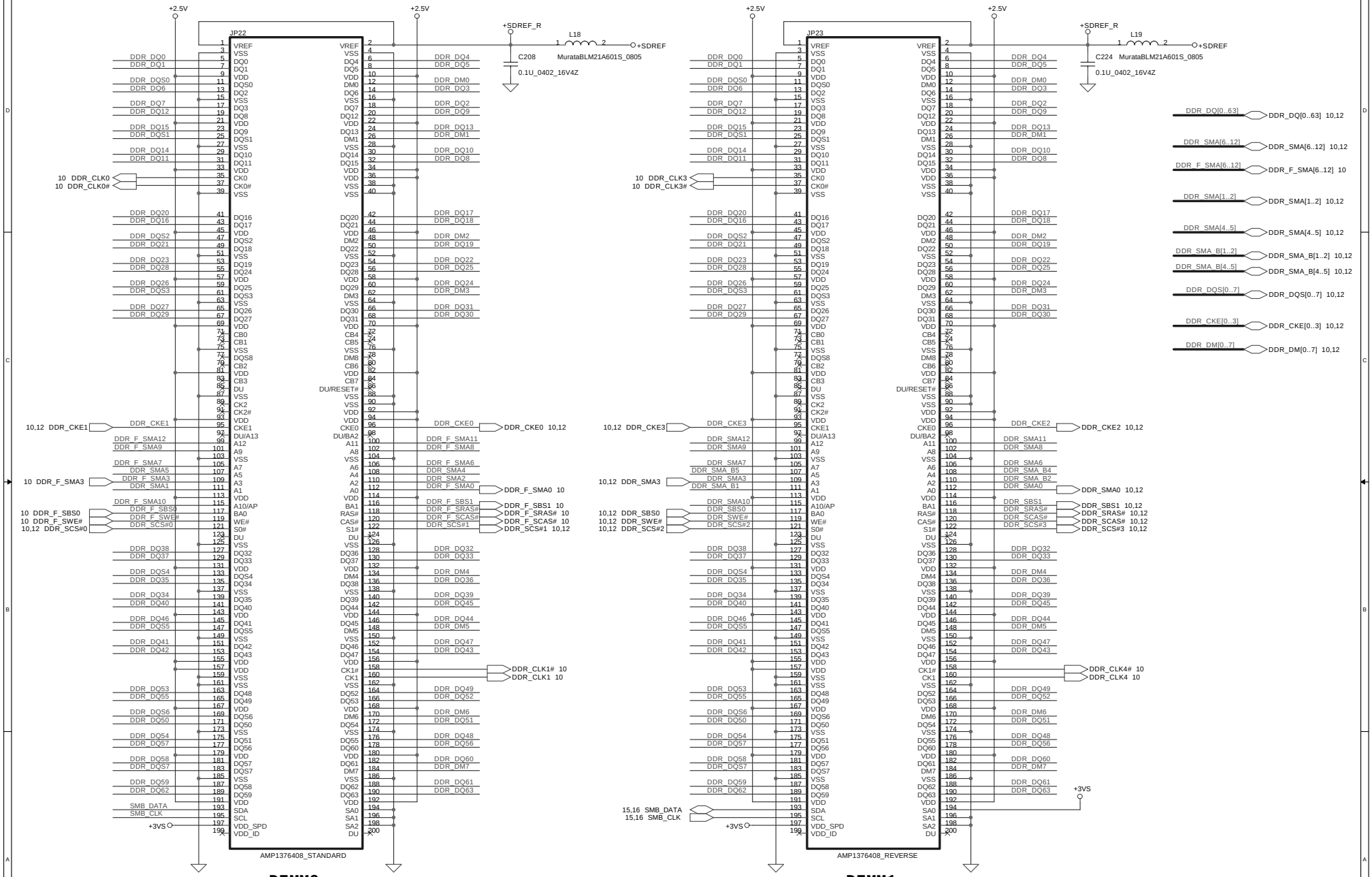

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Title	DDR-DIMM0&1	
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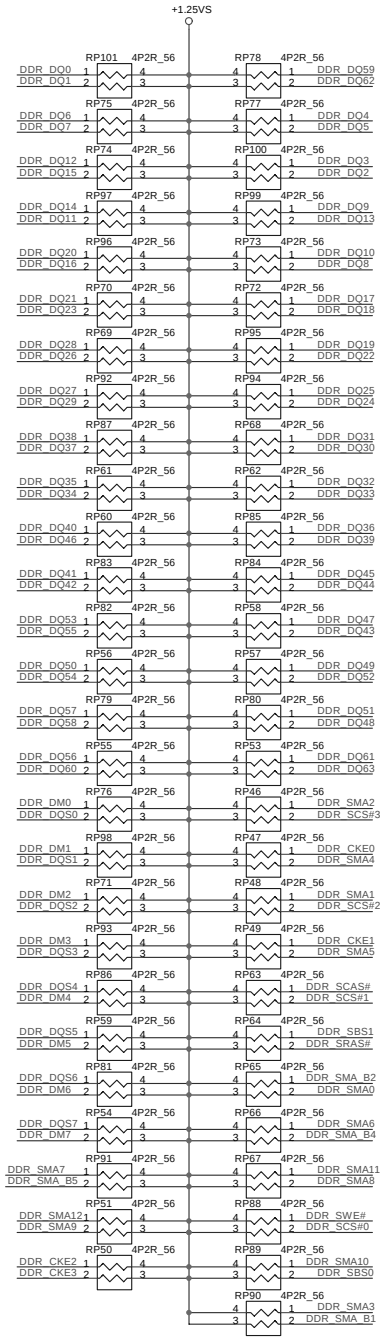
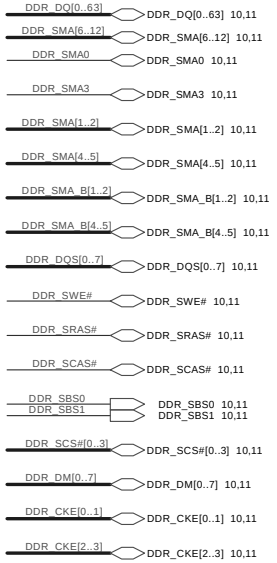
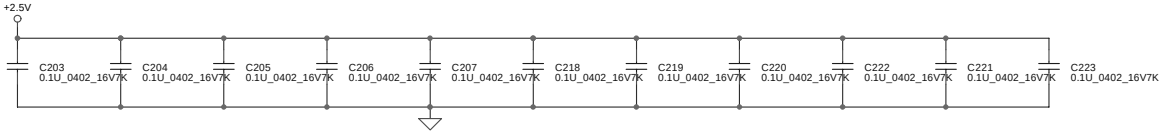
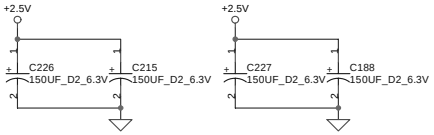




Layout note :

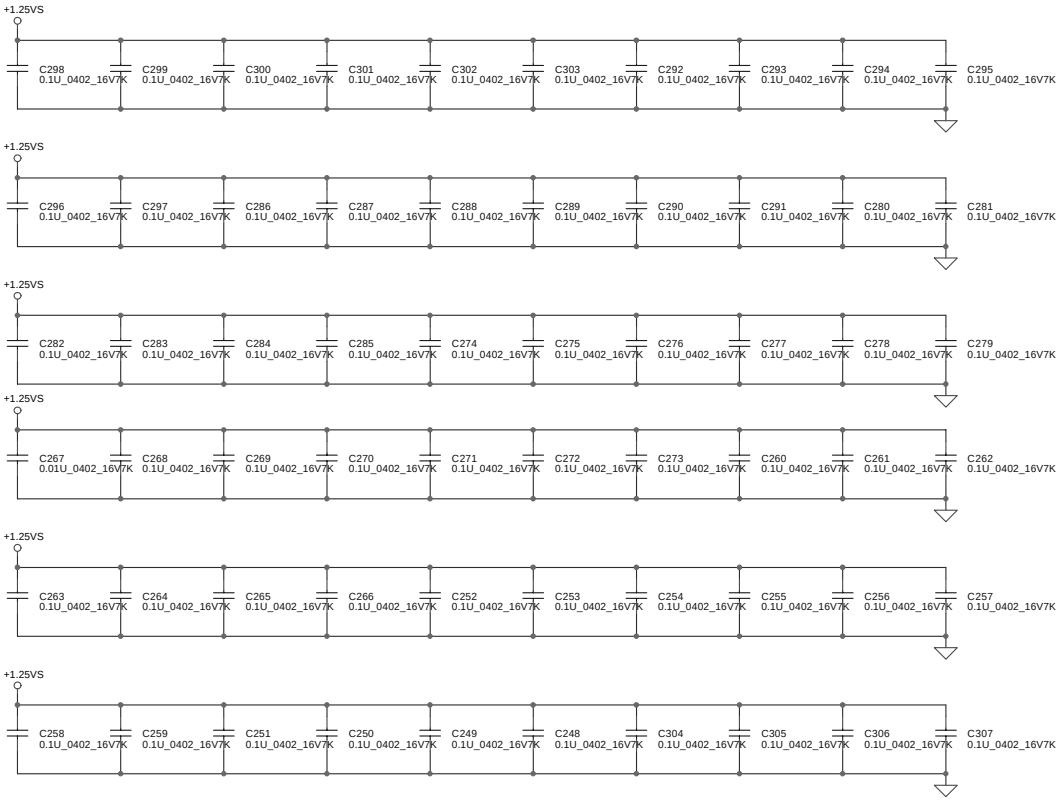
Distribute as close as possible to DDR-SODIMM.





Layout note :

Place one cap close to every 2 pull up resistors termination to +1.25V



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Title	DDR Pull-up and Decoupling	
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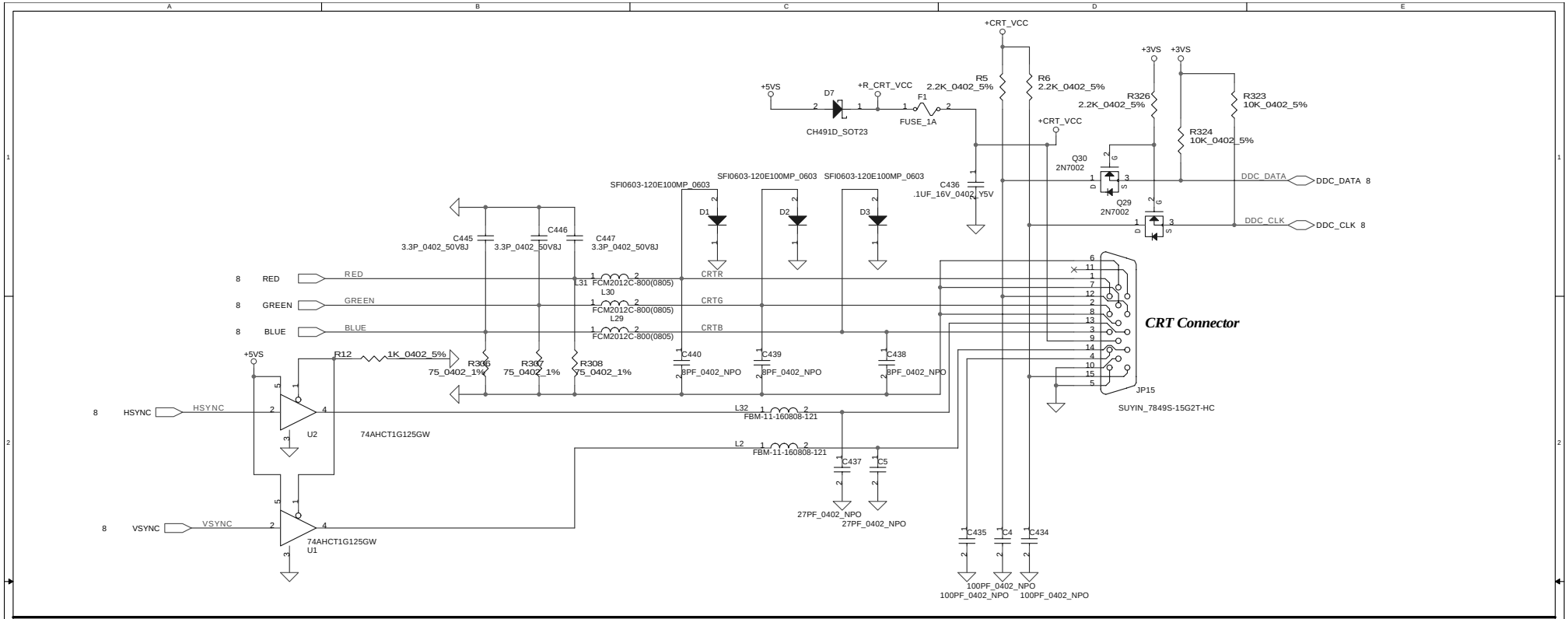

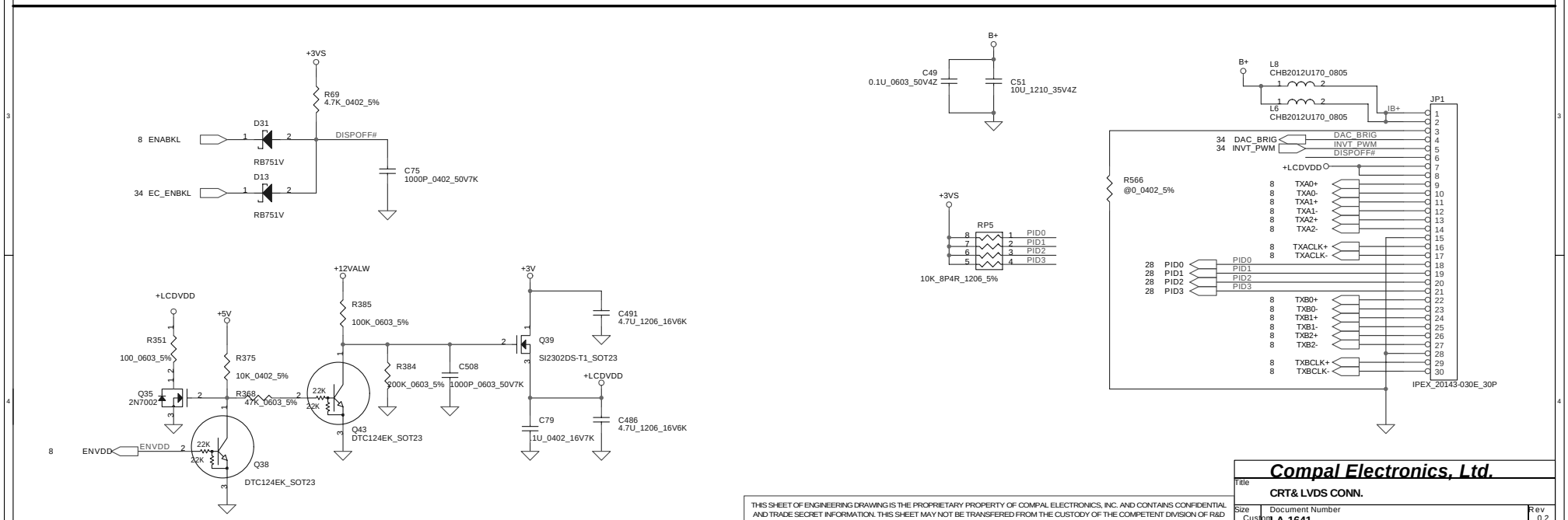

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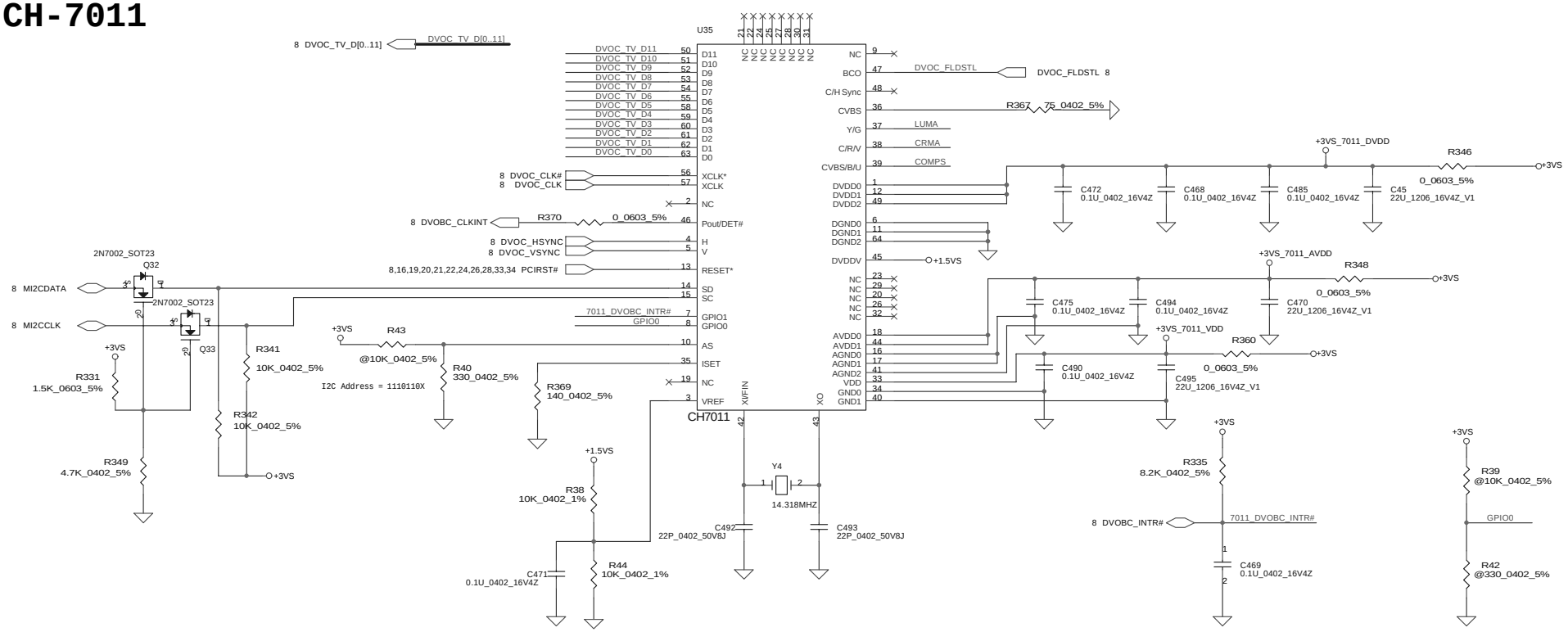
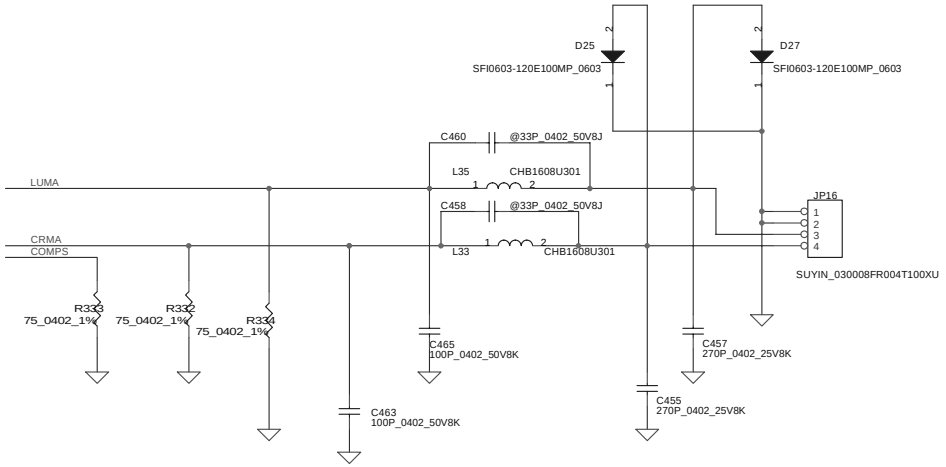
Compal Electronics, Ltd.

Title	CRT& LVDS CONN.	
Size: Custom	Document Number: LA-1641	Rev: 0.2
Date: Tuesday, October 22, 2002	Sheet 13 of 45	

CH-7011



TV-OUT CONN.



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Compal Electronics, Ltd.

Title	CH-7011& TV-CONN.	
Size: Custom	Document Number: LA-1641	Rev: 0.2
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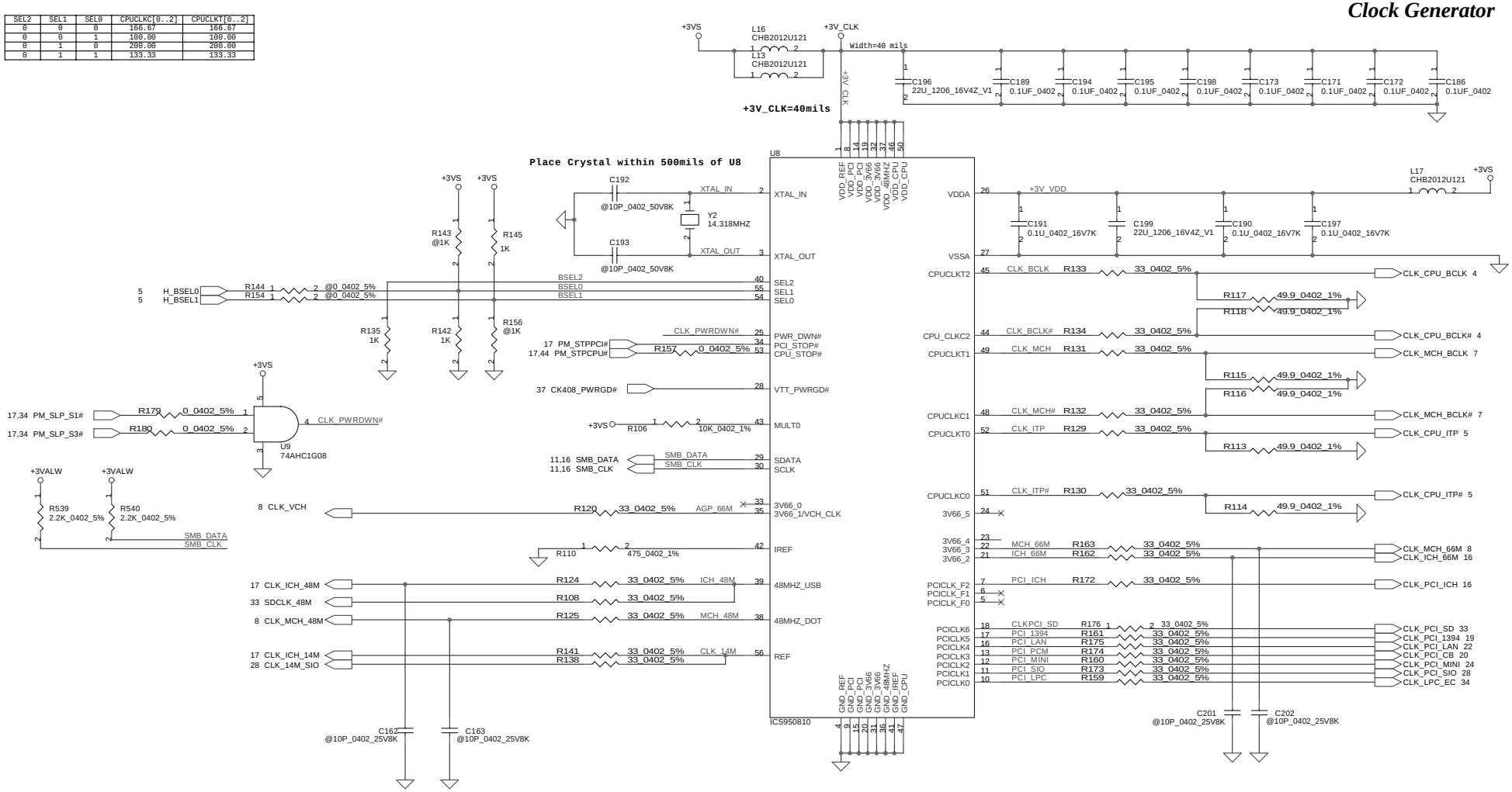
Clock Generator

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33



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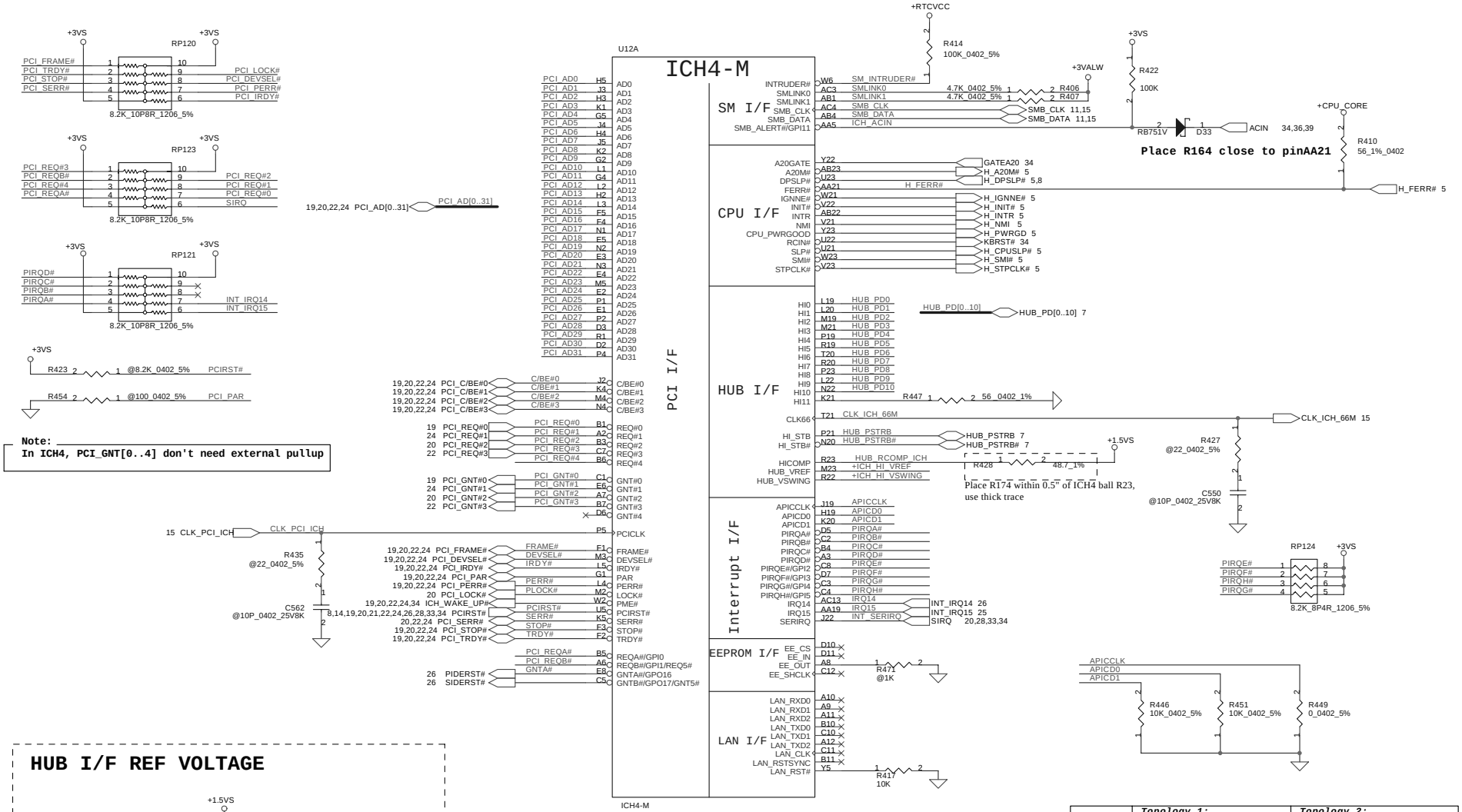
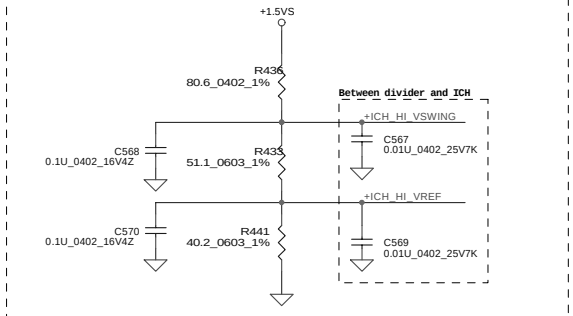
Compal Electronics, Ltd.

Title: Clock Generator		
Size: Custom	Document Number: LA-1641	Rev: 0.2
Date: Tuesday, October 22, 2002	Sheet 15 of 45	



HUB I/F REF VOLTAGE



Place this schematic close to ICH

	Topology 1: *Mount R458 RP122 R533* *Unmount R474 RP125*	*Topology 2:* *Mount R458 R474 RP125* *Unmount RP122 R533*
1394	**Trace: PIRQA#_1394** **Use IRQA**	**Trace: PIRQA#_1394** **Use IRQA**
CardBus	**Trace:PIRQA#/E#** **PIRQB#/F#/D#** **Use IRQA IRQB**	**Trace:PIRQA#/E#** **PIRQB#/F#/D#** **Use IRQE IRQF**
LAN	**Trace:PIRQ_LAN/B#/D#** **Use IRQB**	**Trace:PIRQB#/F#/D#** **Use IRQD**
MINIPCI	**Trace:PIRQC#/G#** **PIRQD#/H#** **Use IRQC IRQD**	**Trace:PIRQC#/G#** **PIRQD#/H#** **Use IRQG IRQH**

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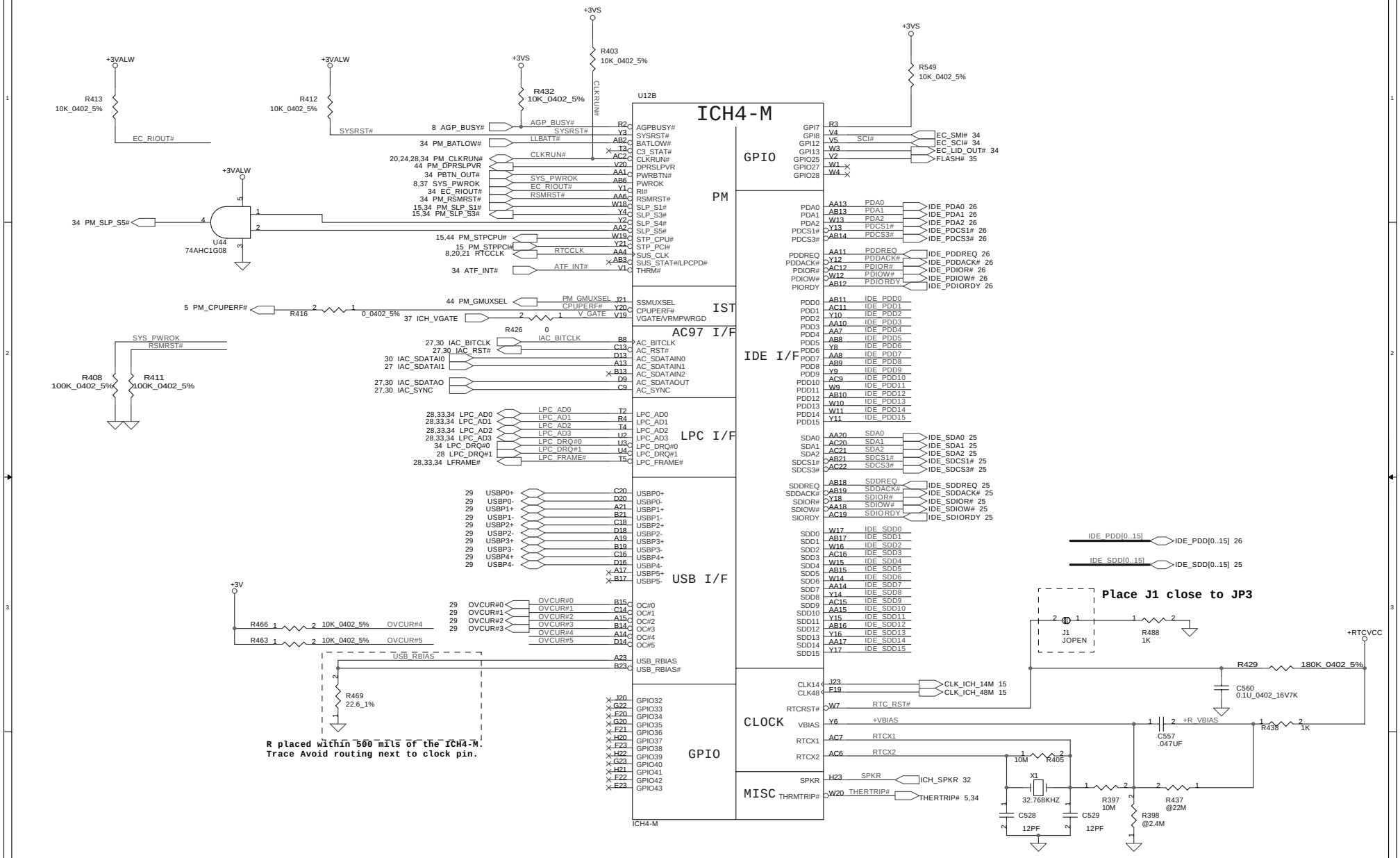
Compal Electronics, Ltd.

Title: ICH4-M(1/2)

Size: Custom | Document Number: LA-1641 | Rev: 0.2

Date: Tuesday, October 22, 2002 | Sheet 16 of 45



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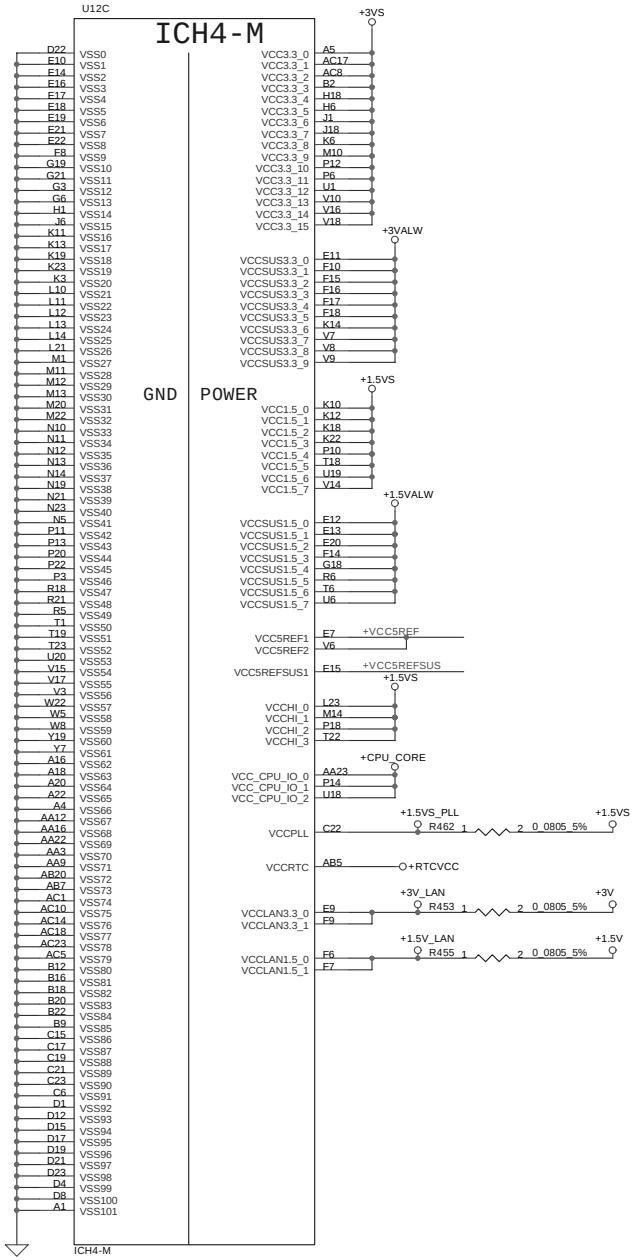
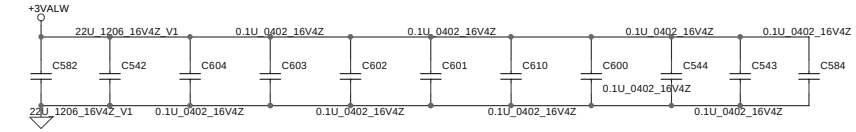
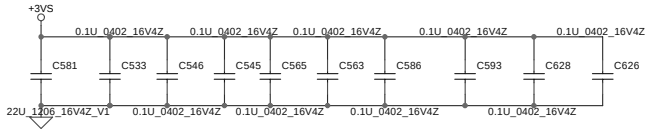
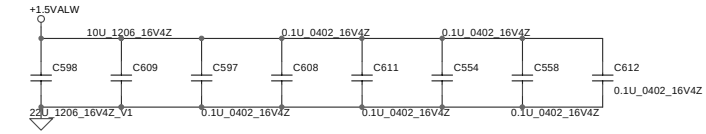
Compal Electronics, Ltd.

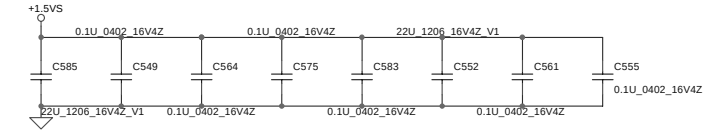
Title	ICH4-M(2/2)	
Size: Custom	Document Number: LA-1641	Rev: 0.2
Date: Tuesday, October 22, 2002	Sheet 17 of 45	

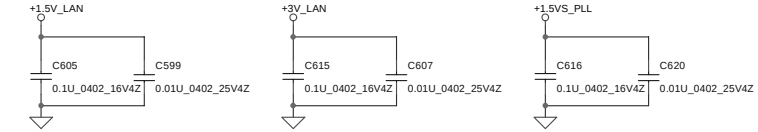


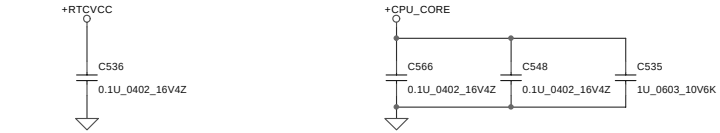


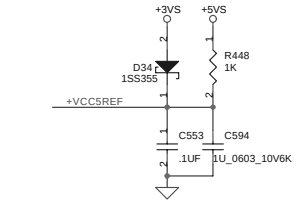


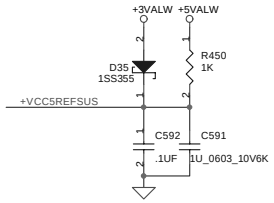












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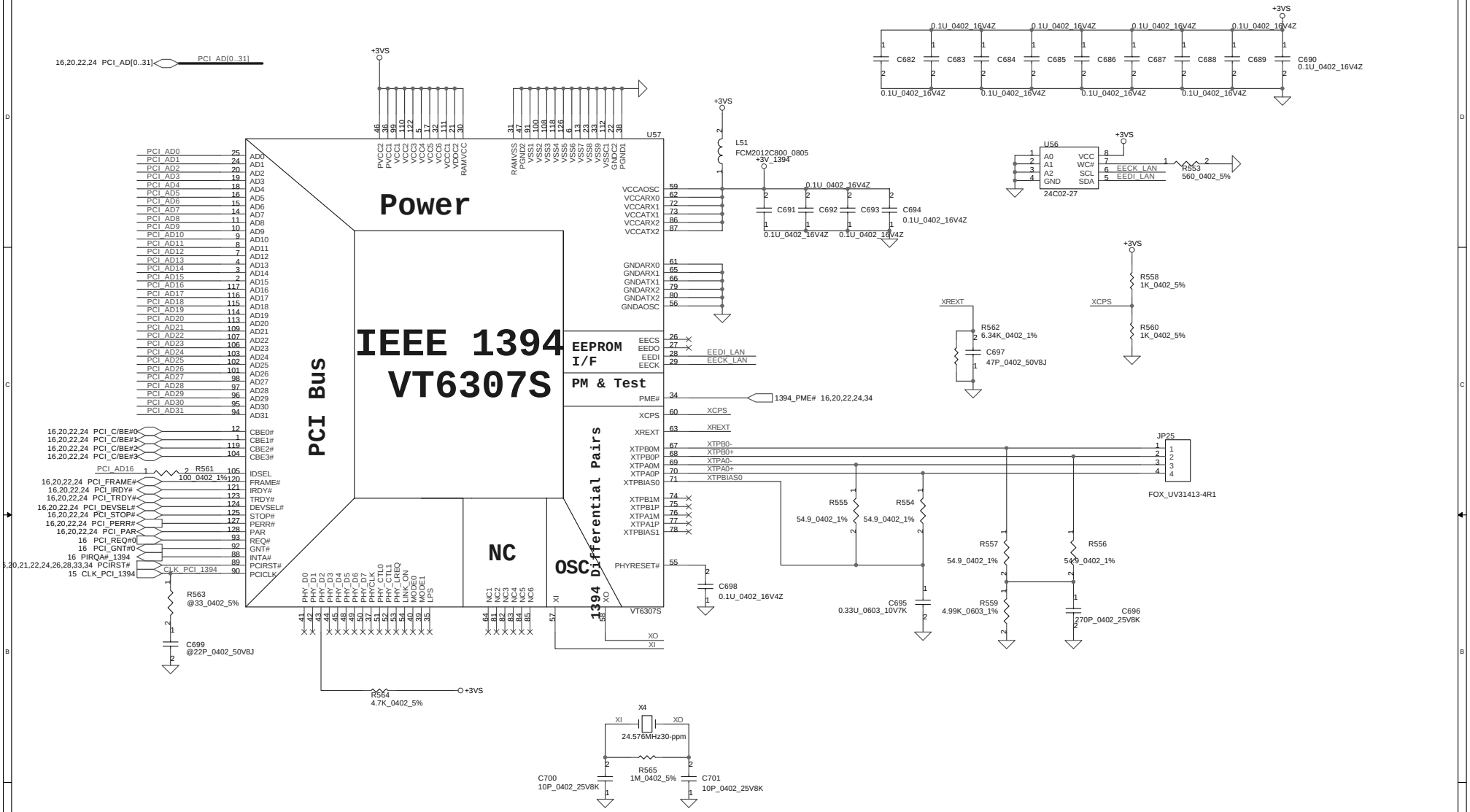
Compal Electronics, Ltd.

Title: **ICH4-M Pullups & Decoupling**

Size	Document Number	Rev
Custom	LA-1641	0.2

Date: Tuesday, October 22, 2002 | Sheet 18 of 45



Note:These components need to close to chip pins.

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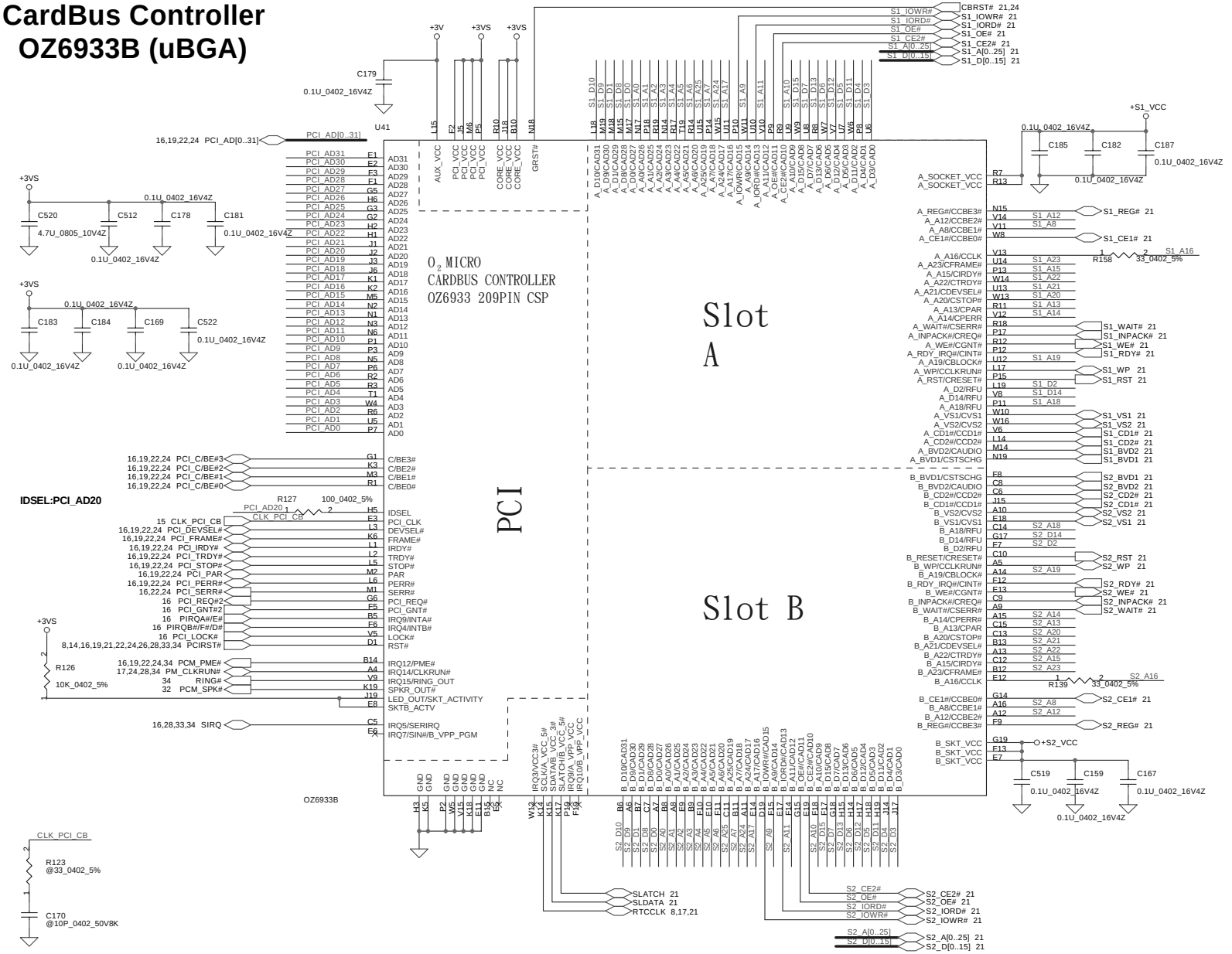
Compal Electronics, Inc.

Title: **IEEE-1394 VT6306**

Size: Custom | Document Number: **BCL50 LA1671** | Rev: 0.1

Date: Tuesday, October 22, 2002 | Sheet 19 of 45

CardBus Controller
OZ6933B (uBGA)



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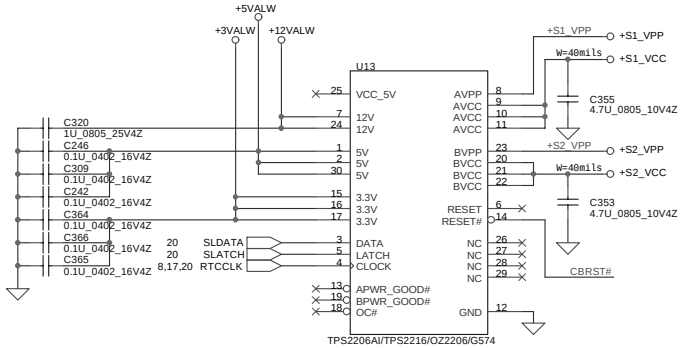
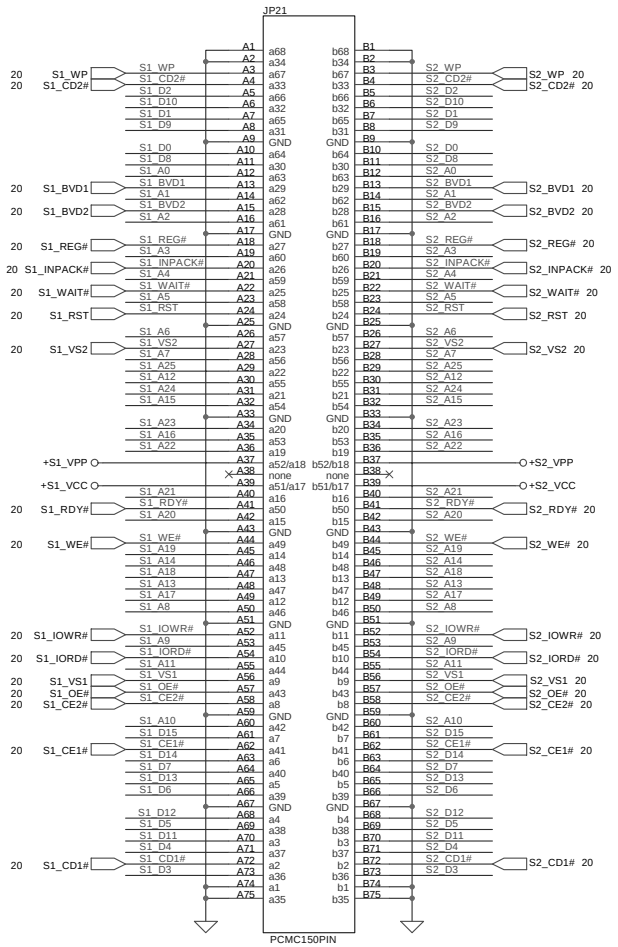
Compal Electronics, Ltd.

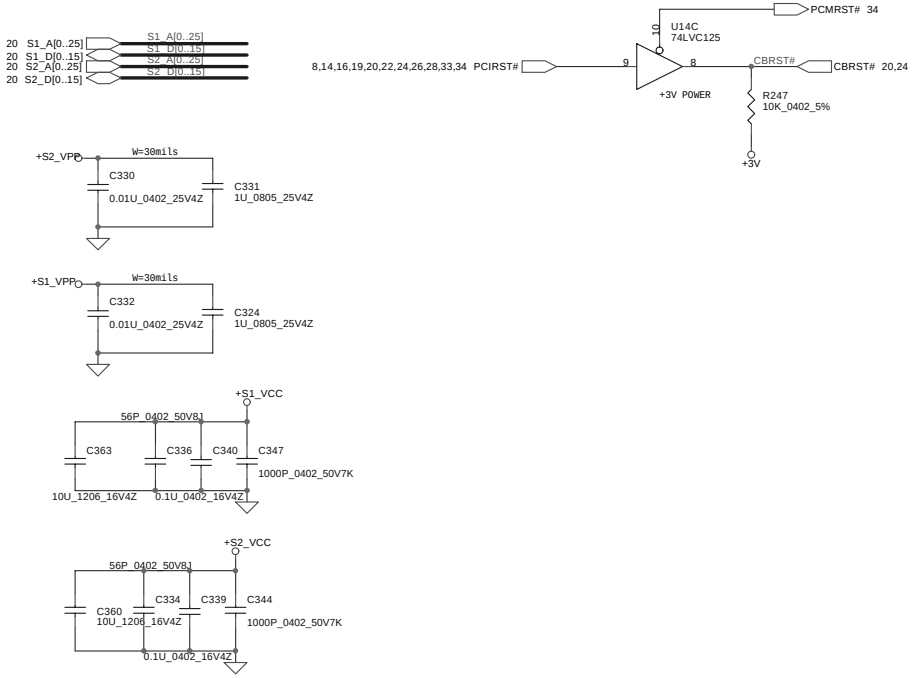
Title	CardBus Controller<OZ6933>	
Size: Custom	Document Number: LA-1641	Rev: 0.2
Date: Tuesday, October 22, 2002	Sheet 20 of 45	

PCMCIA POWER CTRL.

CARDBUS SOCKET







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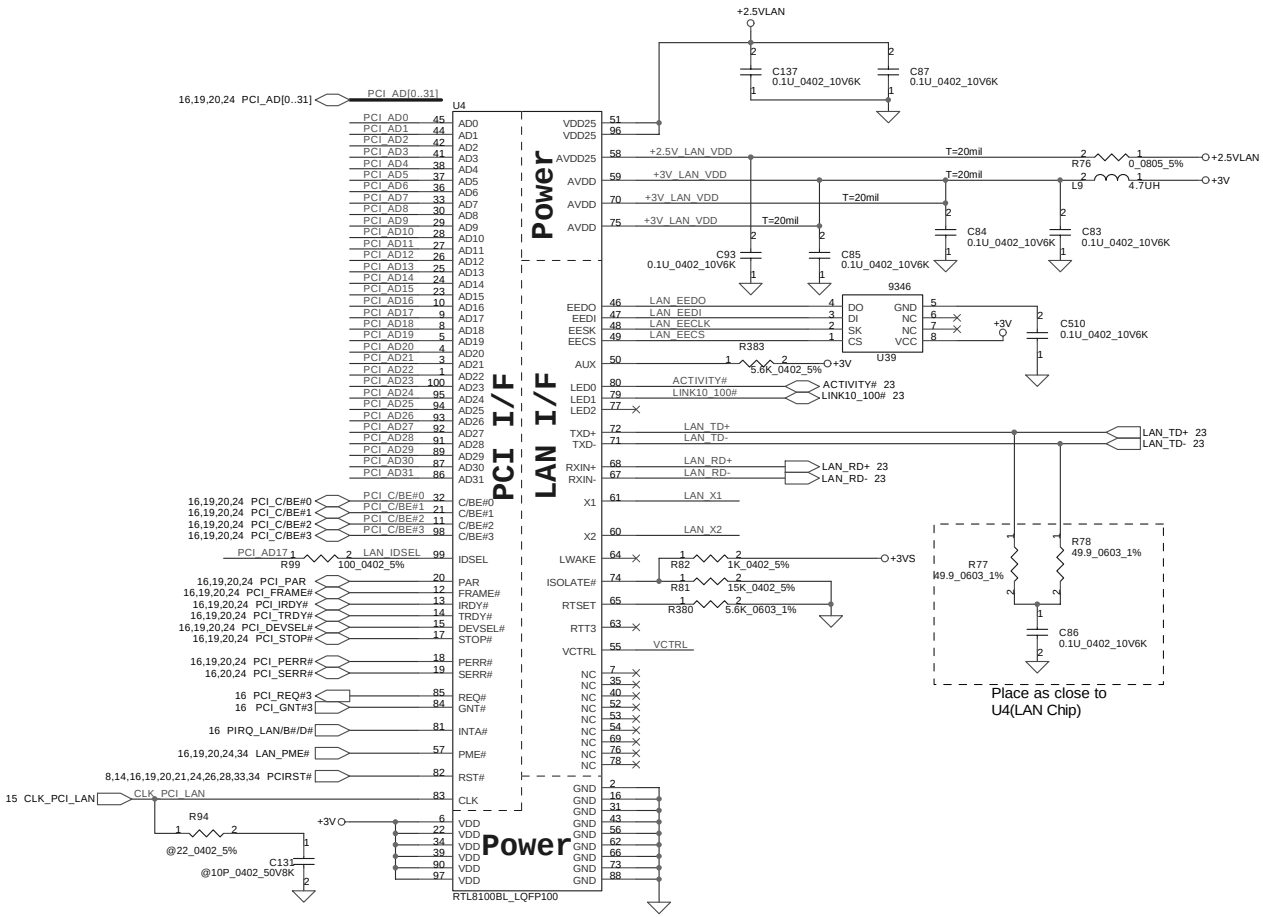
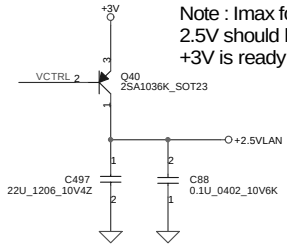
Compal Electronics, Ltd.

Title	FOXCONN PCMCIA SOCKET	
Size: Custom	Document Number: LA-1641	Rev: 0.2
Date: Tuesday, October 22, 2002	Sheet 21 of 45	

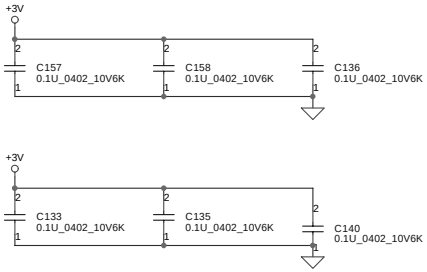


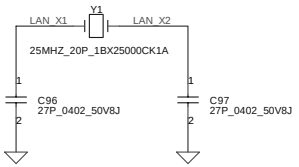
1.Q40 pin2 close to U4 pin55
2.C497 and C88 close to Q40 pin1



Note : Imax for VDD25 = 40mA
2.5V should be ready before
+3V is ready

2.5VLAN power generated by VCTRL.





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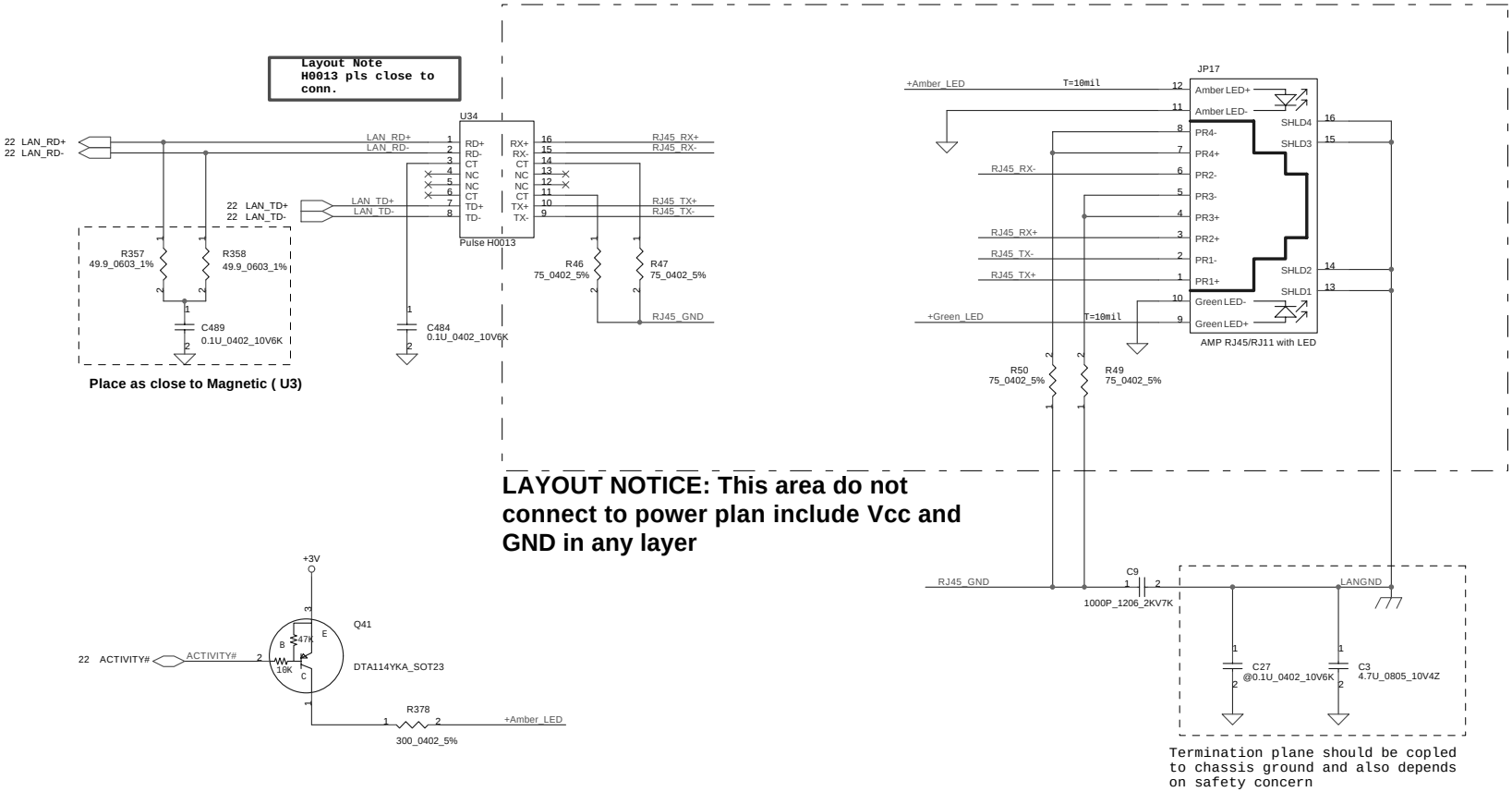
Compal Electronics, Ltd.

Title	LAN-Realtek RTL8100BL	
Size: Custom	Document Number: LA-1641	Rev: 0.2
Date: Tuesday, October 22, 2002	Sheet 22 of 45	

Keep Out 40mil



LAYOUT NOTICE: This area do not connect to power plan include Vcc and GND in any layer

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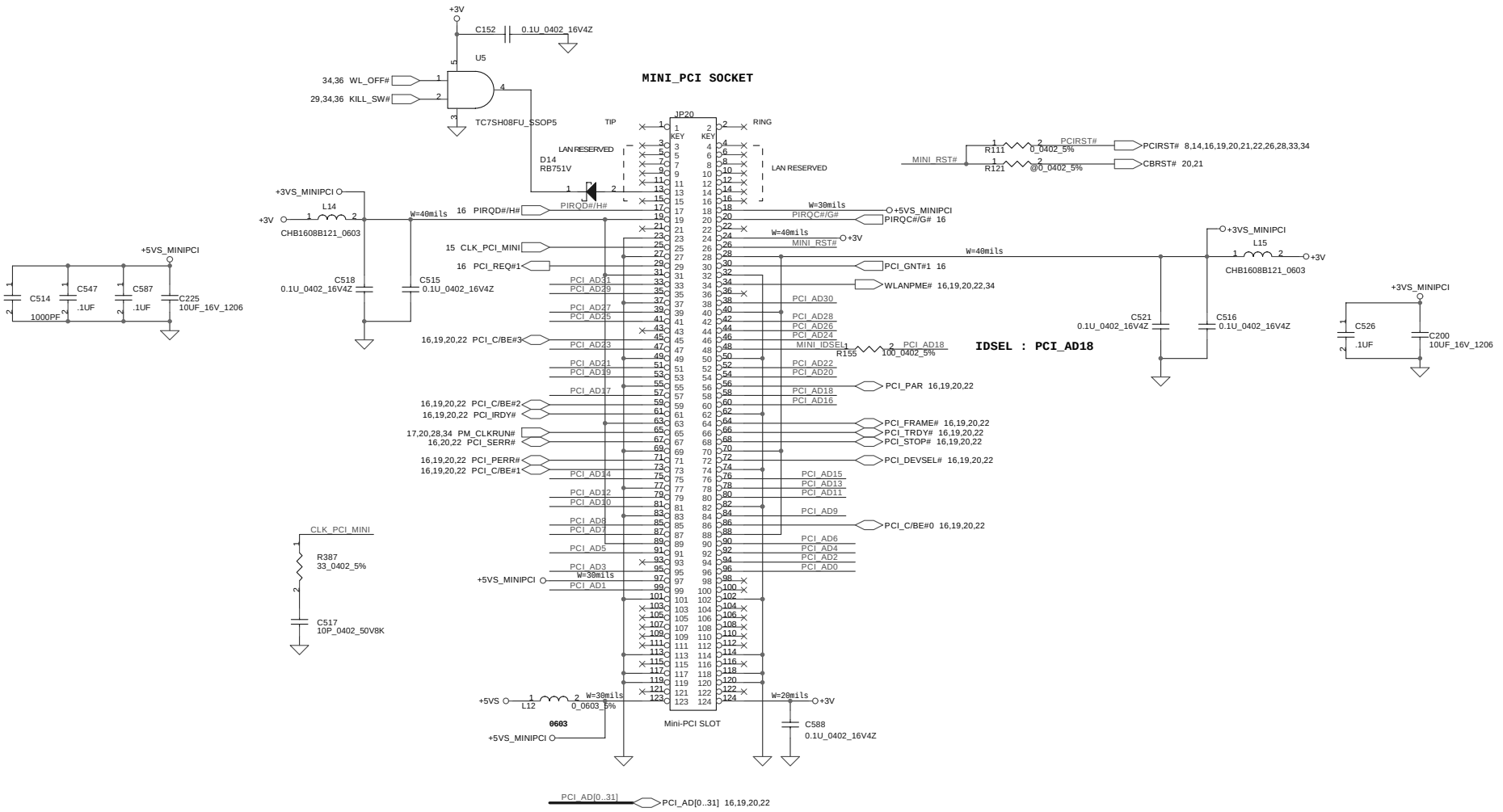
Compal Electronics, Ltd.

Title	RJ11/RJ45 Connector	
Size Custom	Document Number LA-1641	Rev 0.2
Date: Tuesday, October 22, 2002	Sheet 23 of 45	



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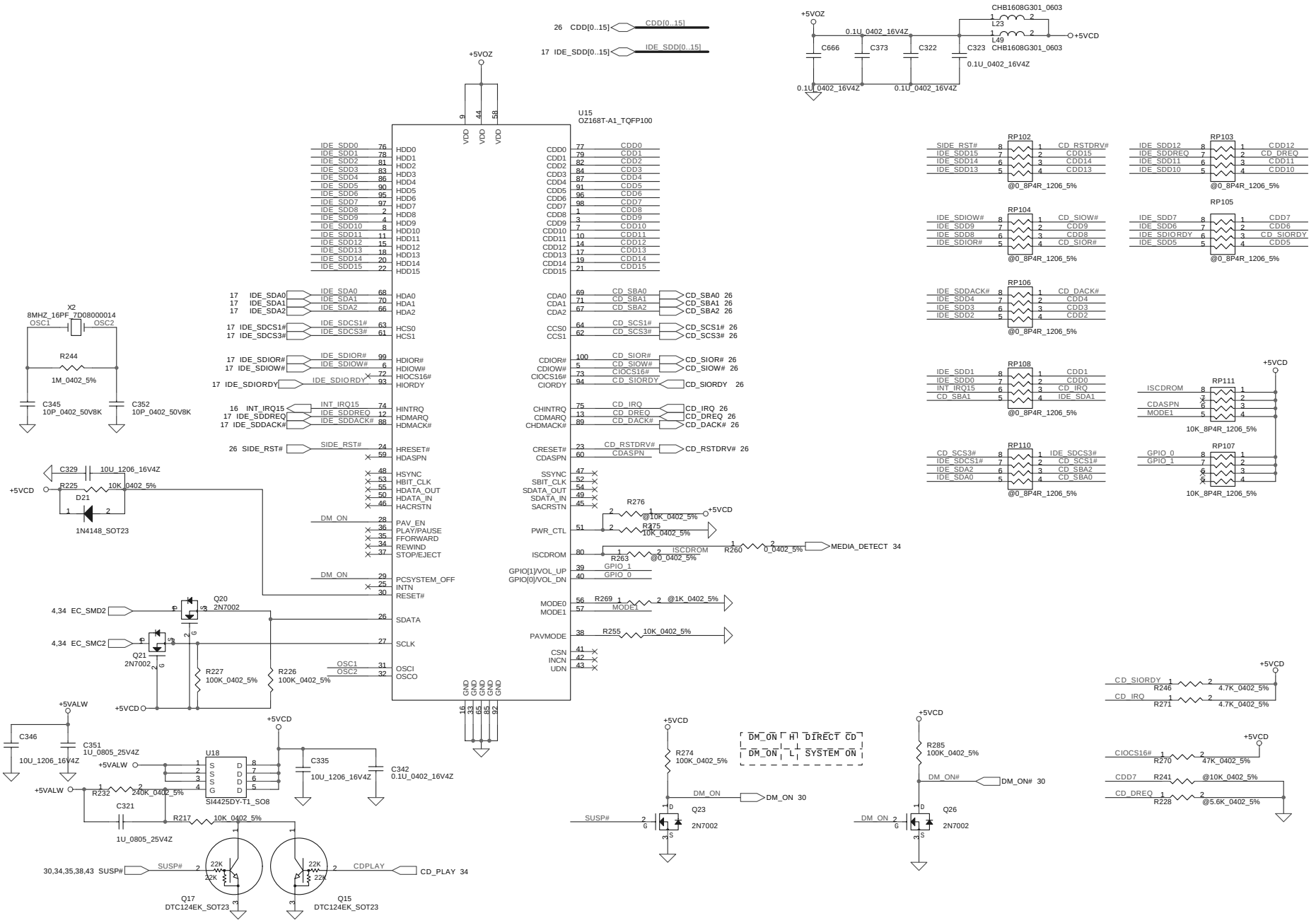
Compal Electronics, Ltd.

Title	Mini PCI Slot	
Size: Custom	Document Number: LA-1641	Rev: 0.2
Date: Tuesday, October 22, 2002	Sheet 24 of 45	



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Compal Electronics, Inc

Title: **OZ-168 CD_PLAY**

Size: Custom | Document Number: **LA1541** | Rev: 0.2

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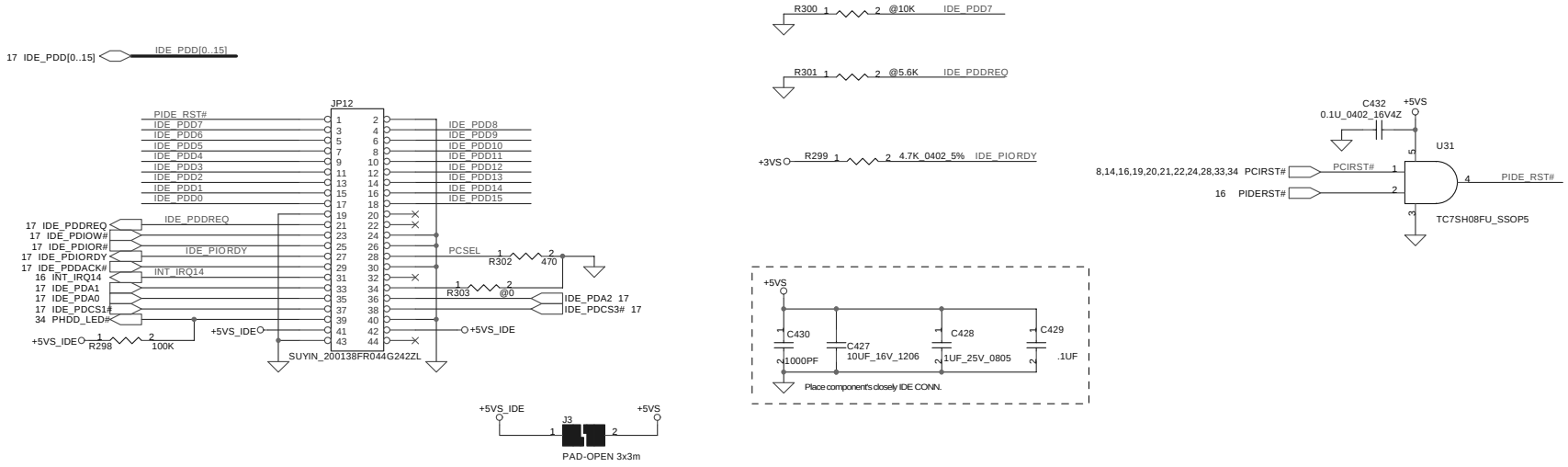
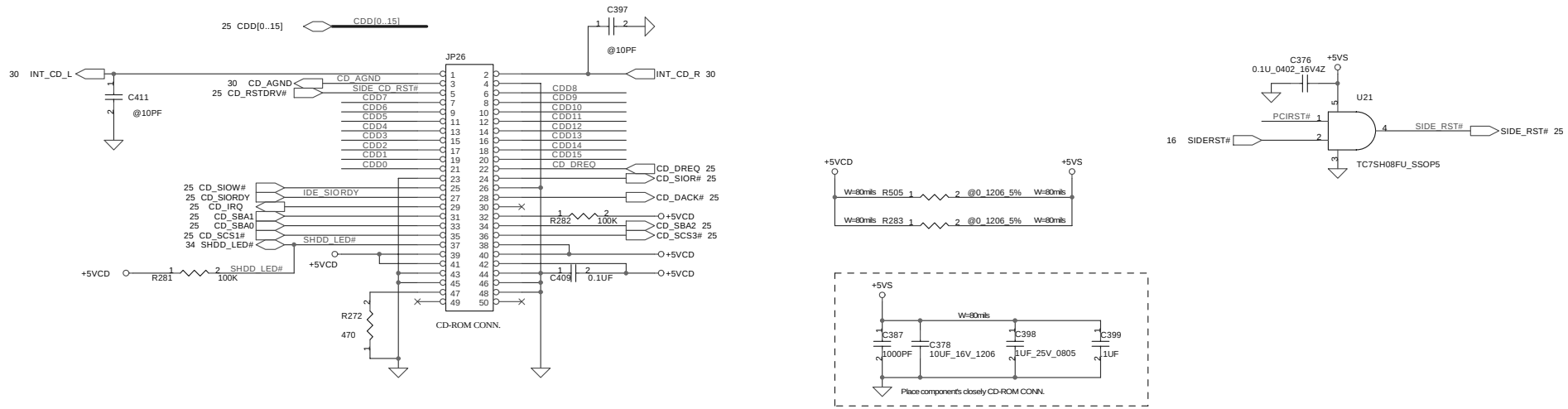
IDE Module CONN.



CD-ROM Module CONN.



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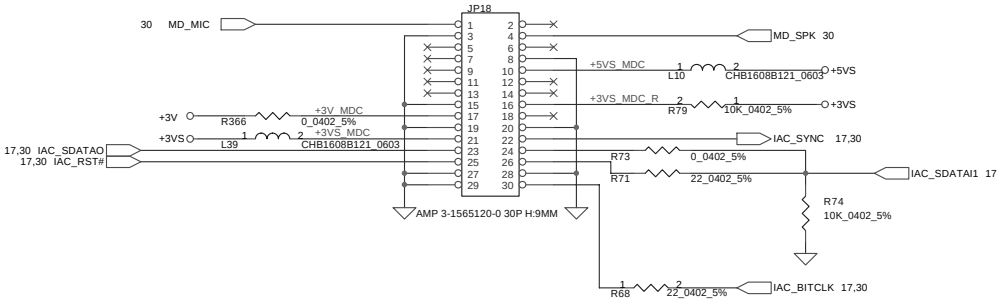
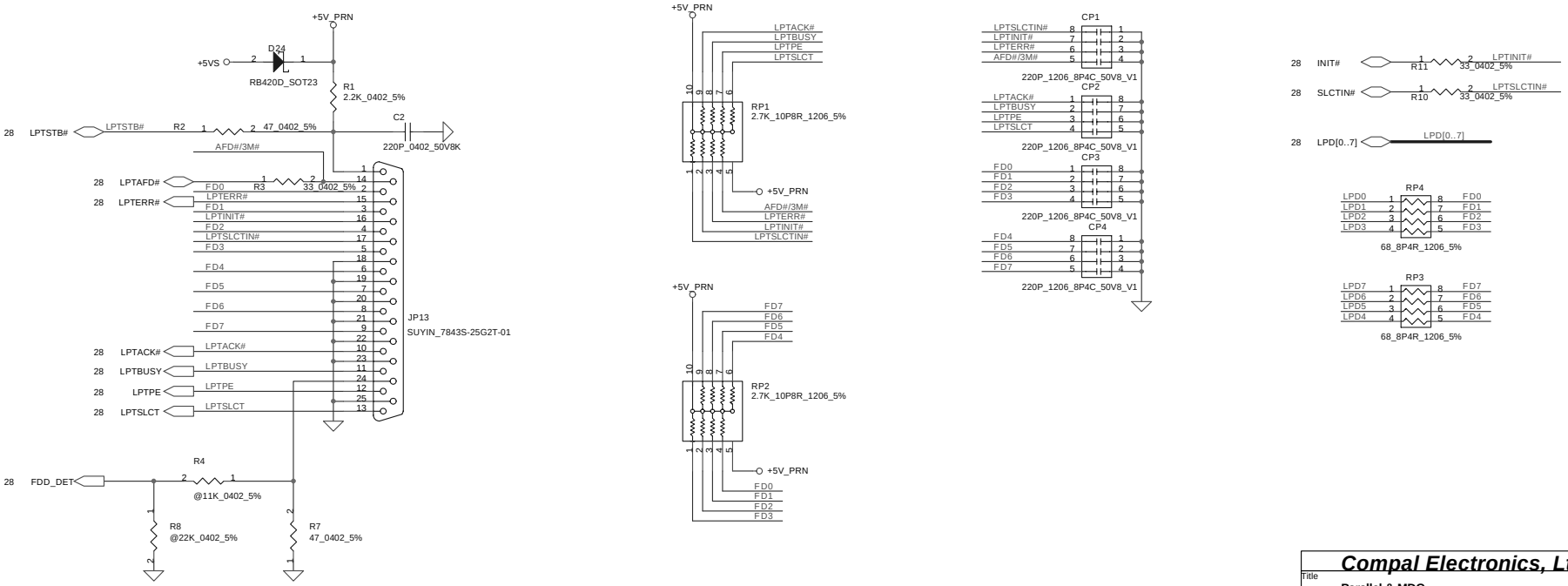
Compal Electronics, Ltd.		
Title: IDE & CD-ROM Connector		
Size: Custom	Document Number: LA-1641	Rev: 0.2
Date: Tuesday, October 22, 2002	Sheet 26 of 45	

MDC Connector



Parallel Port



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Title	Parallel & MDC	
Size: Custom	Document Number: LA-1641	Rev: 0.2
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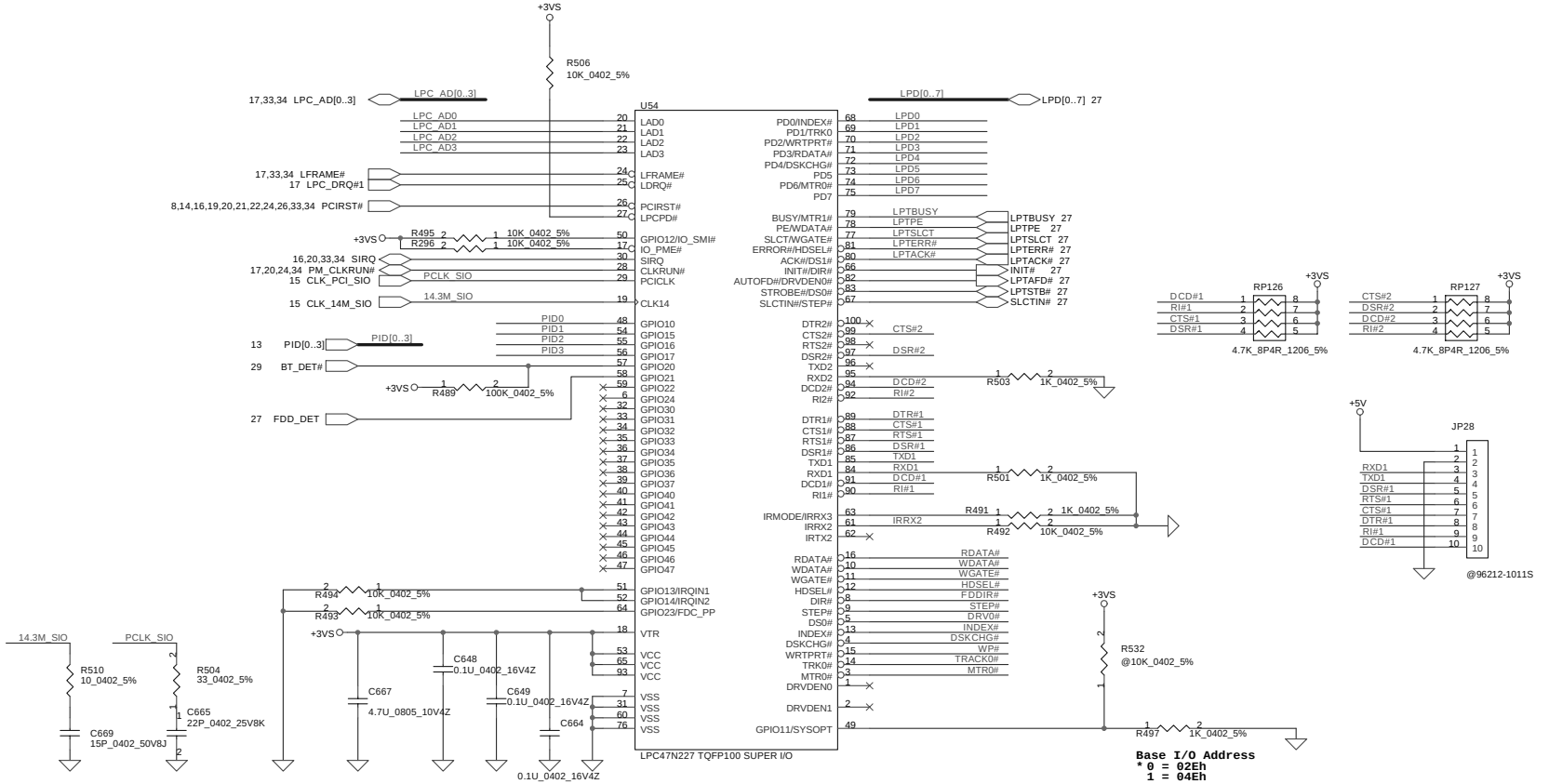
SUPER I/O SMsC FDC47N227



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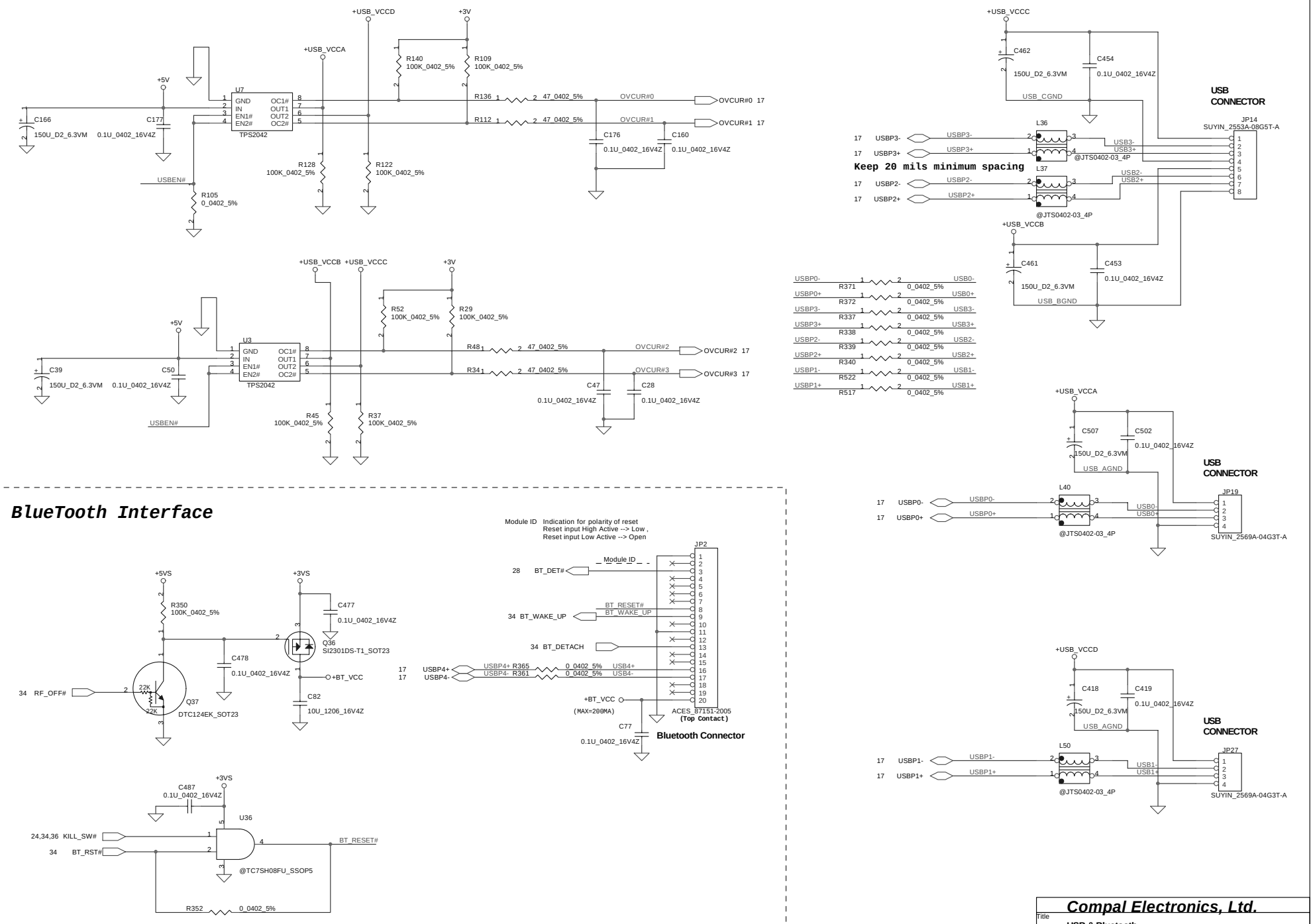
Compal Electronics, Ltd.

Title	LPC-Super I/O	
Size: Custom	Document Number: LA-1641	Rev: 0.2
Date: Tuesday, October 22, 2002	Sheet 28 of 45	



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Compal Electronics, Ltd.

Title	USB & Bluetooth	
Size: Custom	Document Number: LA-1641	Rev: 0.2
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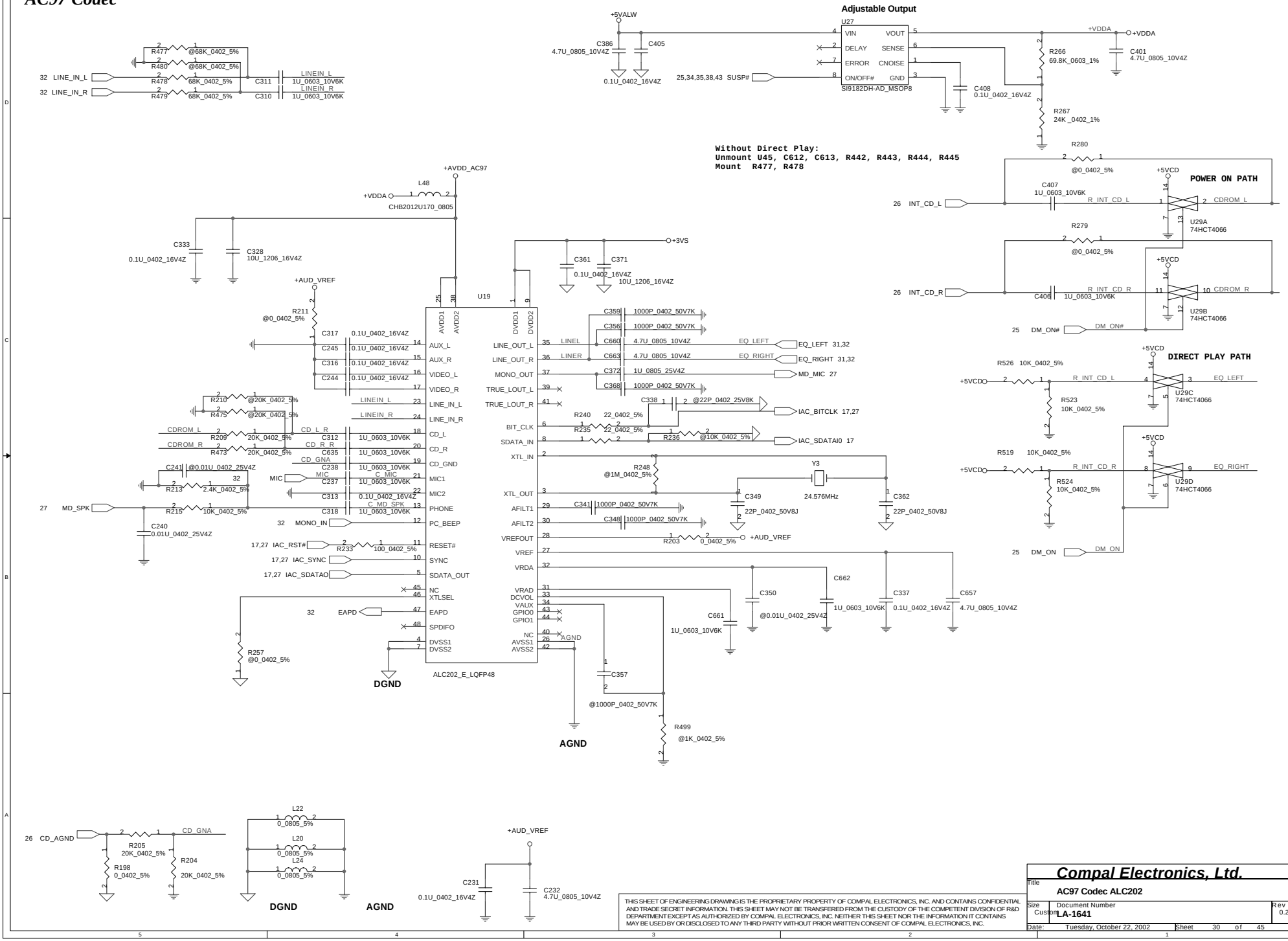
AC97 Codec



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Compal Electronics, Ltd.

Title	AC97 Codec ALC202	
Size: Custom	Document Number: LA-1641	Rev: 0.2
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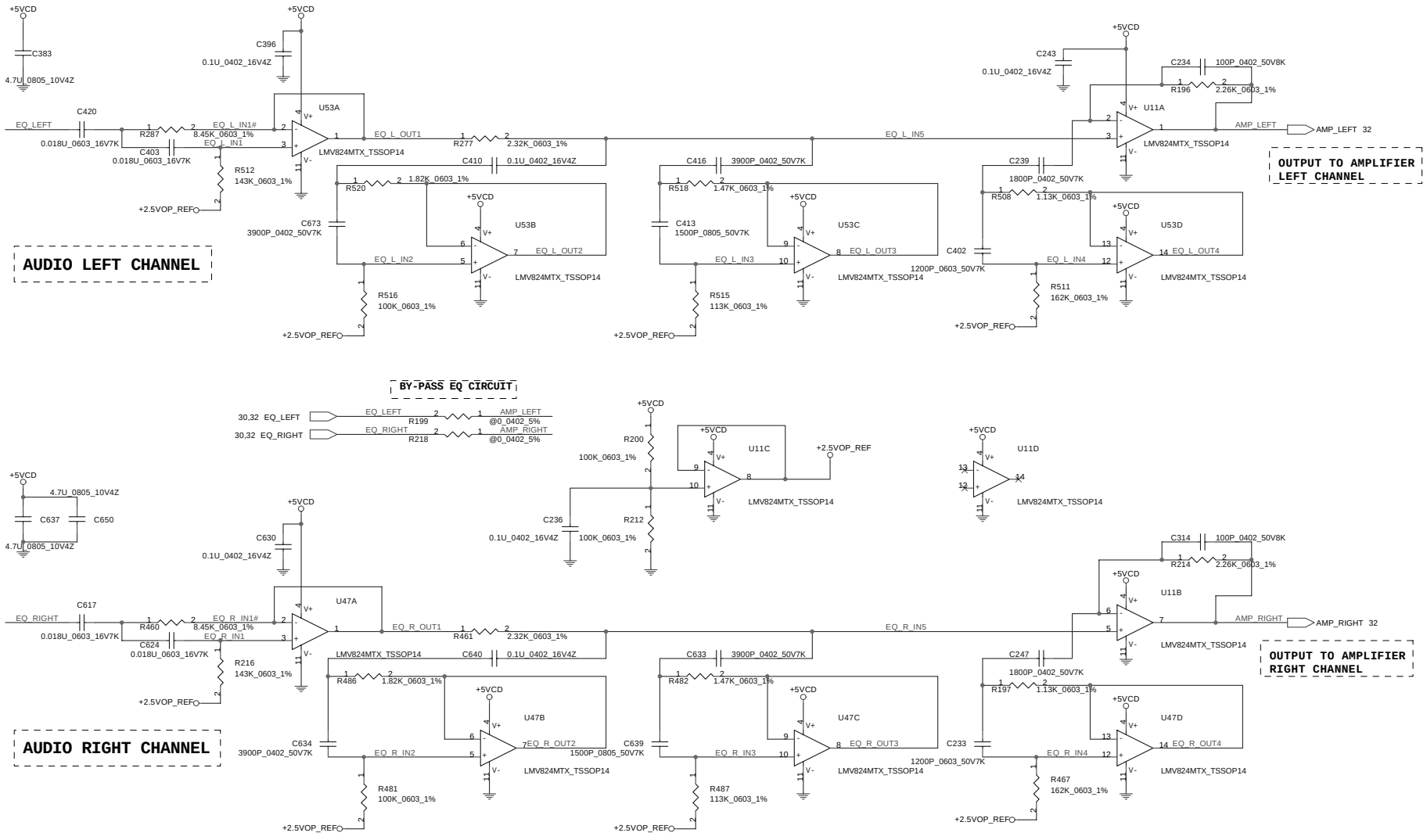

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Compal Electronics, Ltd.

Title	H/W EQ	
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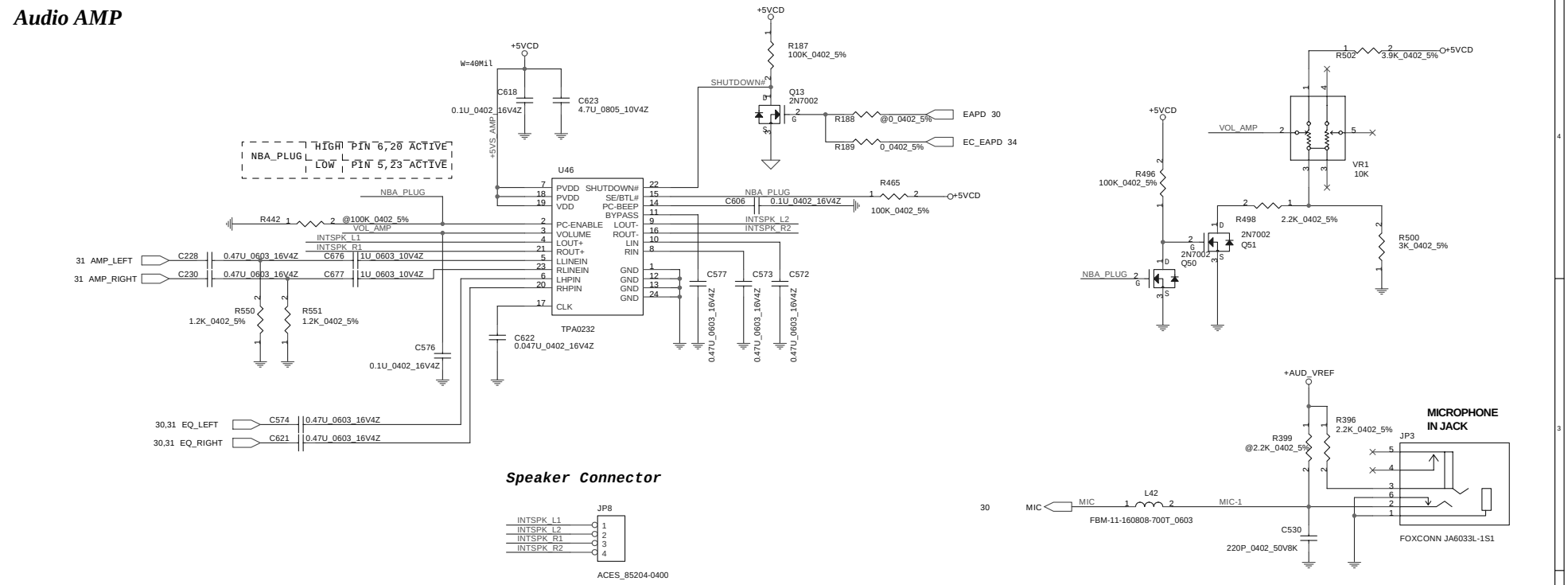
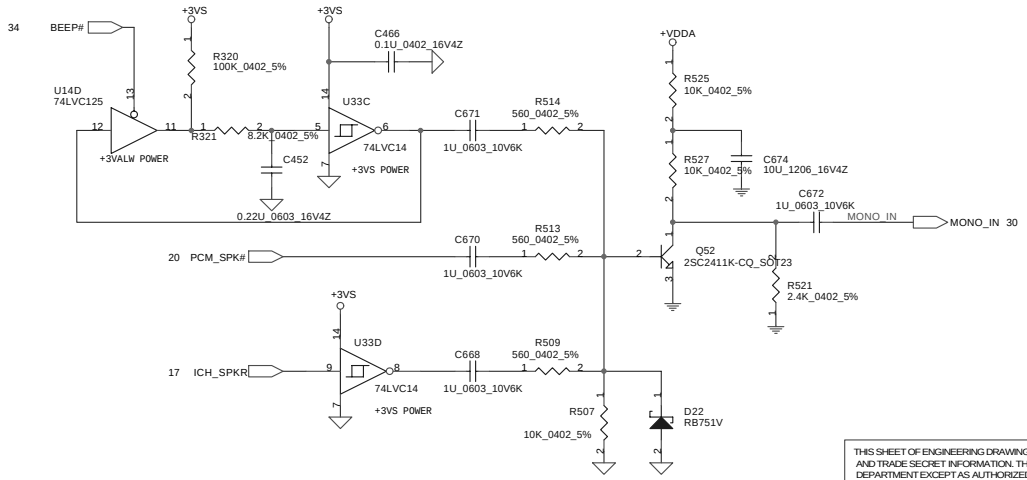
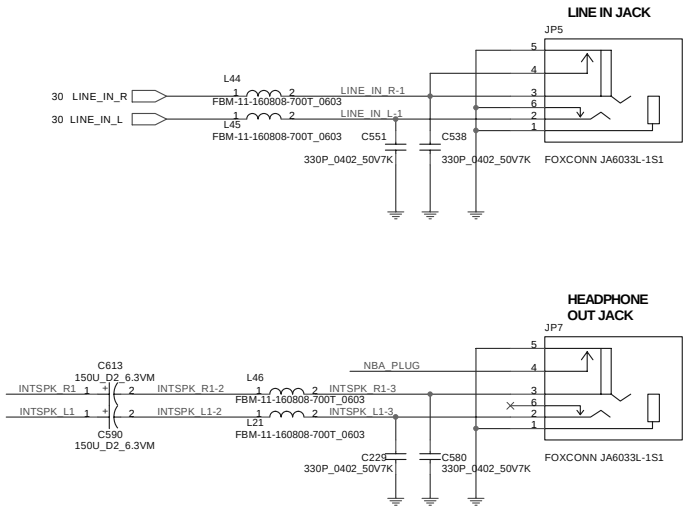
Audio AMP



Speaker Connector

System Sound





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Compal Electronics, Ltd.

Title	Audio AMP & JACK	
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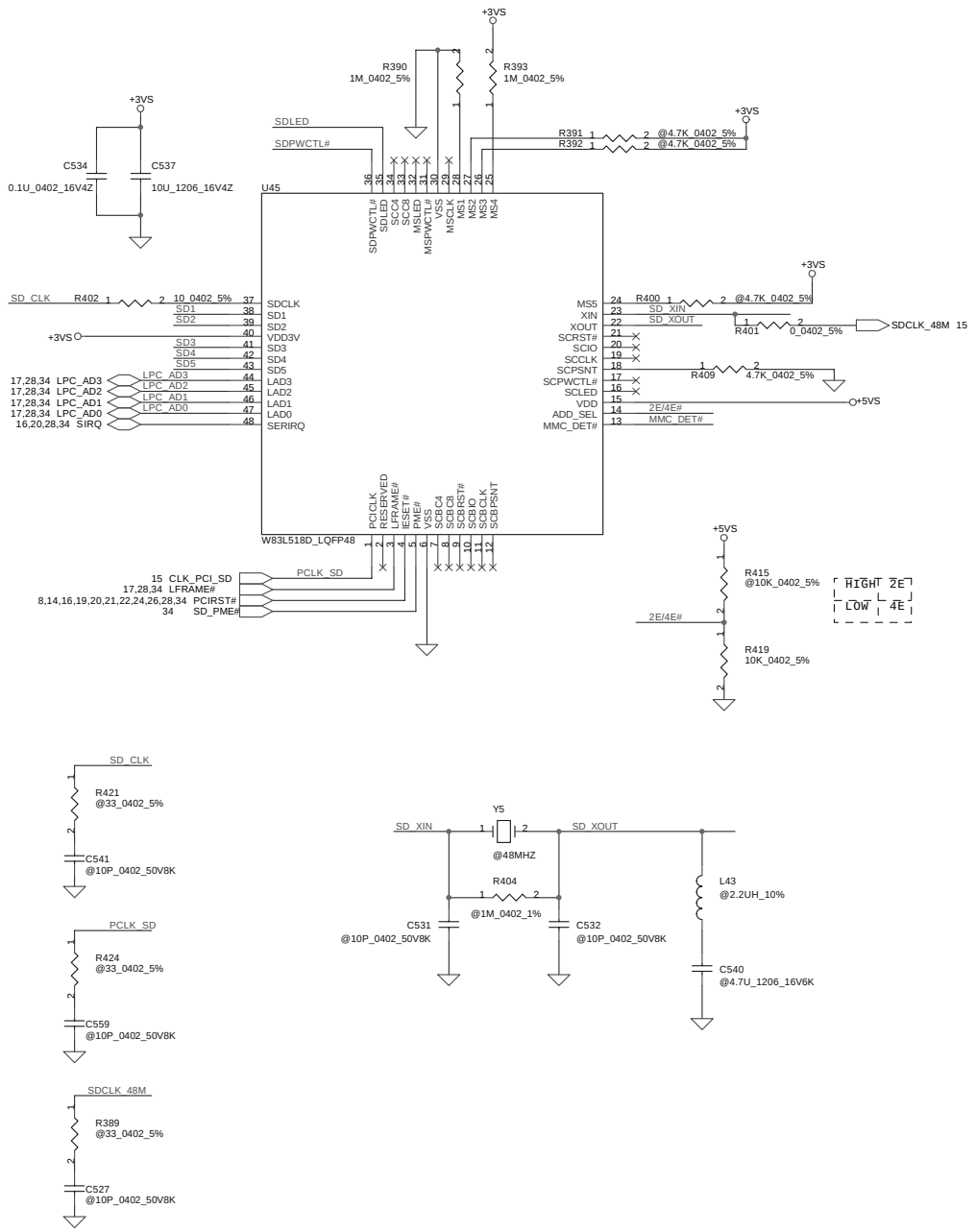
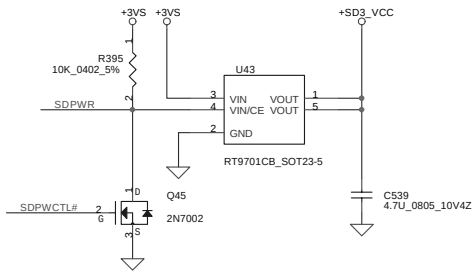
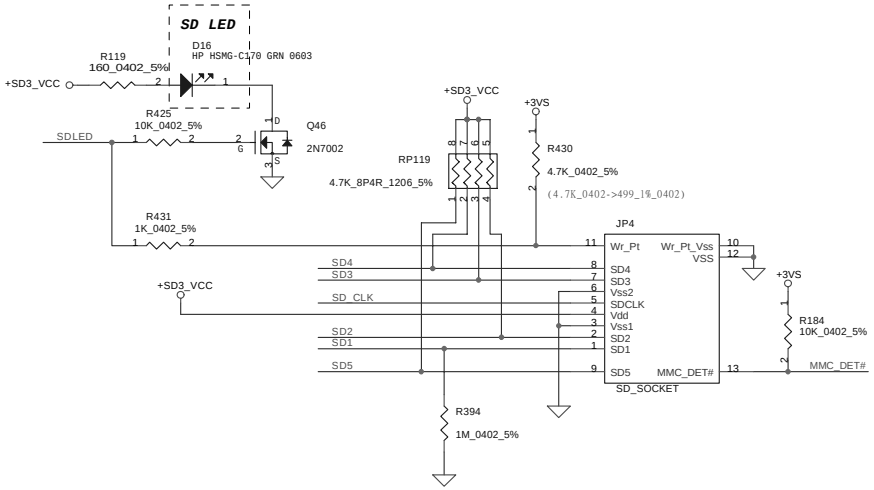
SD Card Reader



SD Power Switch



SD SOCKET



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Compal Electronics, Ltd.

Title	SD Controller W83L518D	
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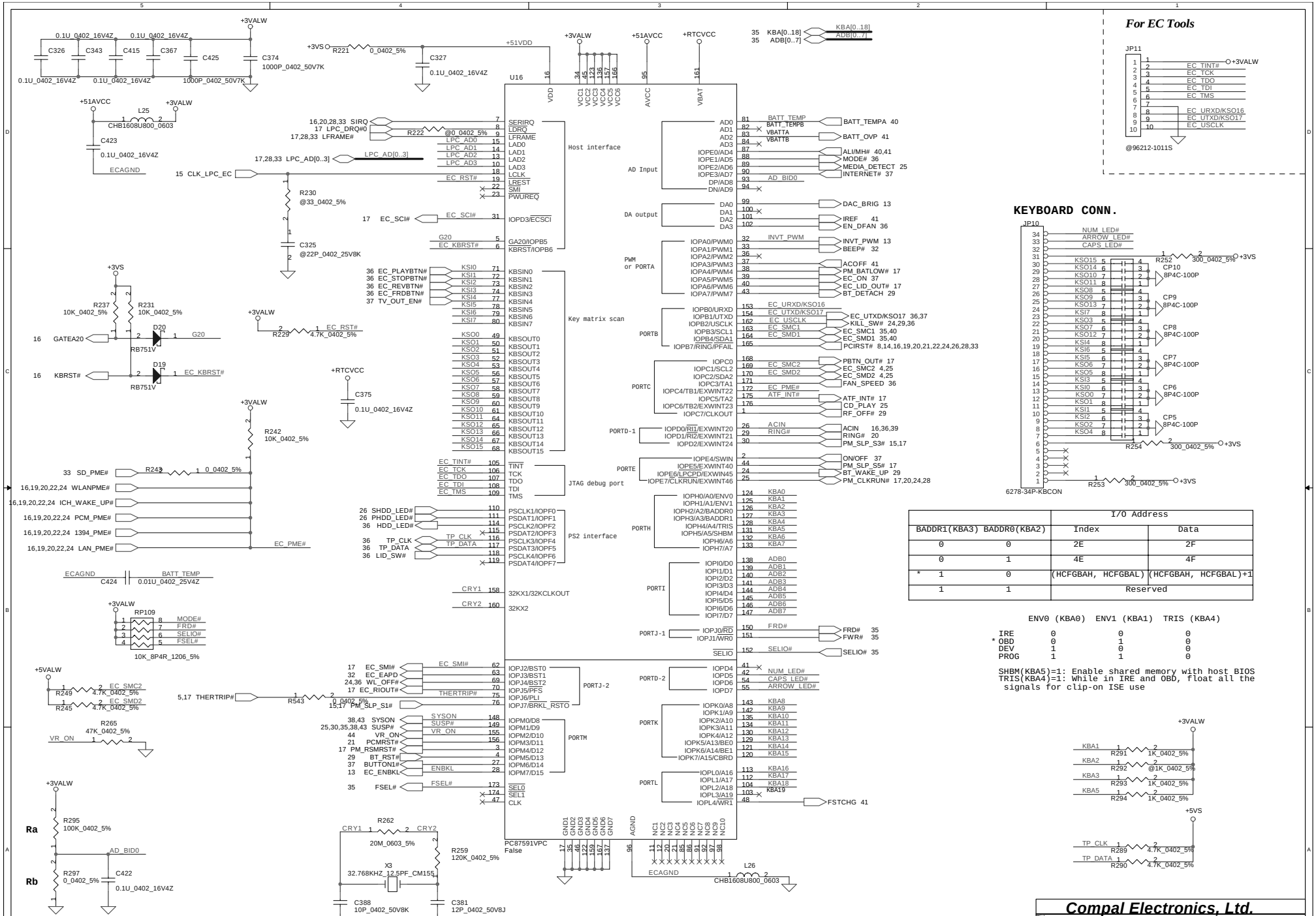
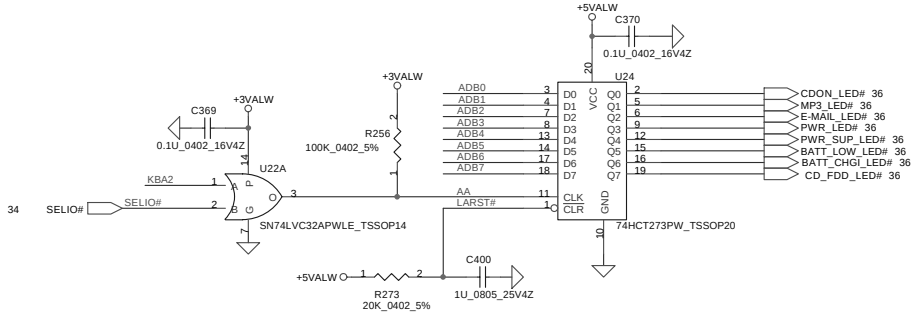


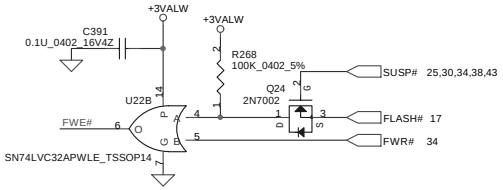
	I/O Address	
BADDR1(KBA3) BADDR0(KBA2)	Index	Data
0 0	2E	2F
0 1	4E	4F
* 1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

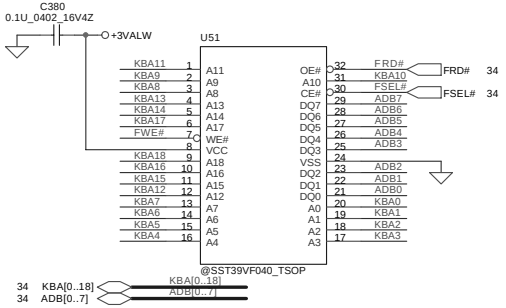
	ENV0 (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM(KBA5)=1: Enable shared memory with host BIOS
TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use

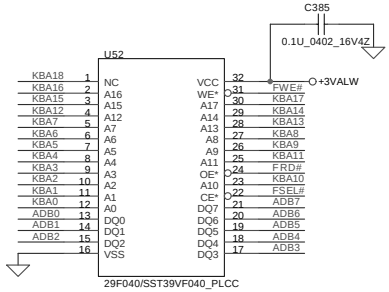


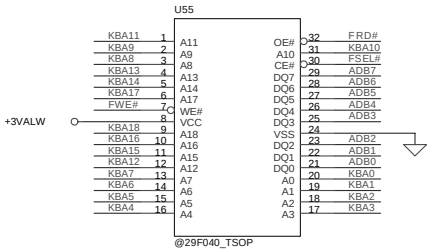
System BIOS

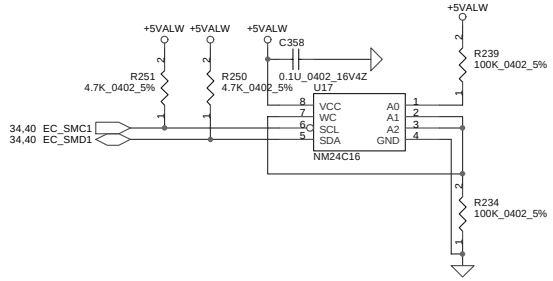




SMBus EEPROM







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Title	BIOS & Ext.I/O	
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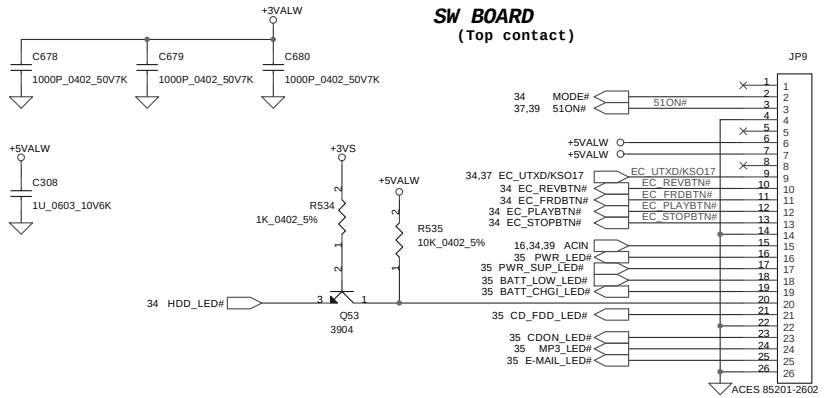
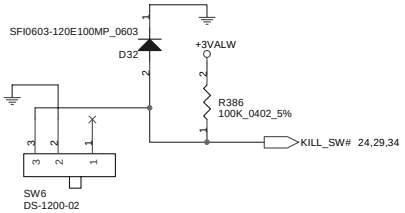
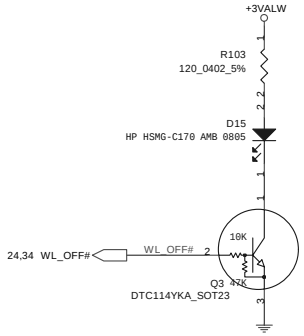
SW BOARD
(Top contact)



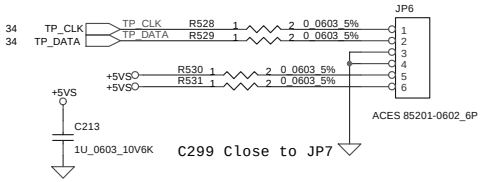
Kill SWITCH



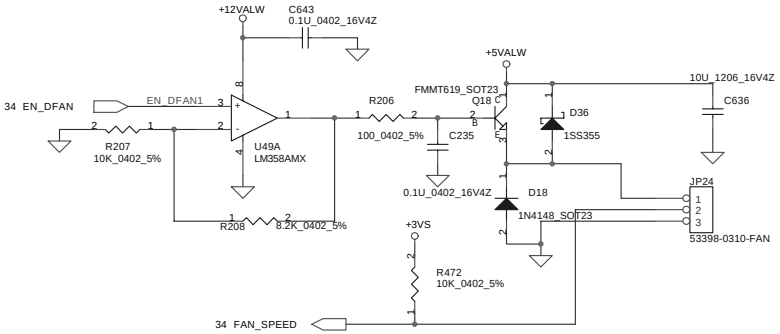
WIRELESS ACTIVE AMB LED



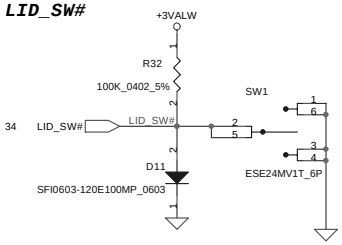
Touch Pad Connector



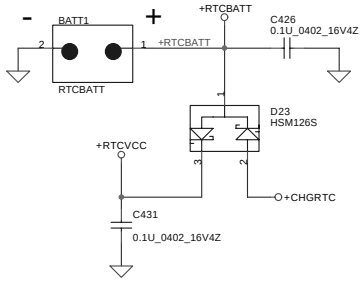
FAN CONN



LID_SW#



RTC BATT



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Title	System Connectors	
Size: Custom	Document Number: LA-1641	Rev: 0.2
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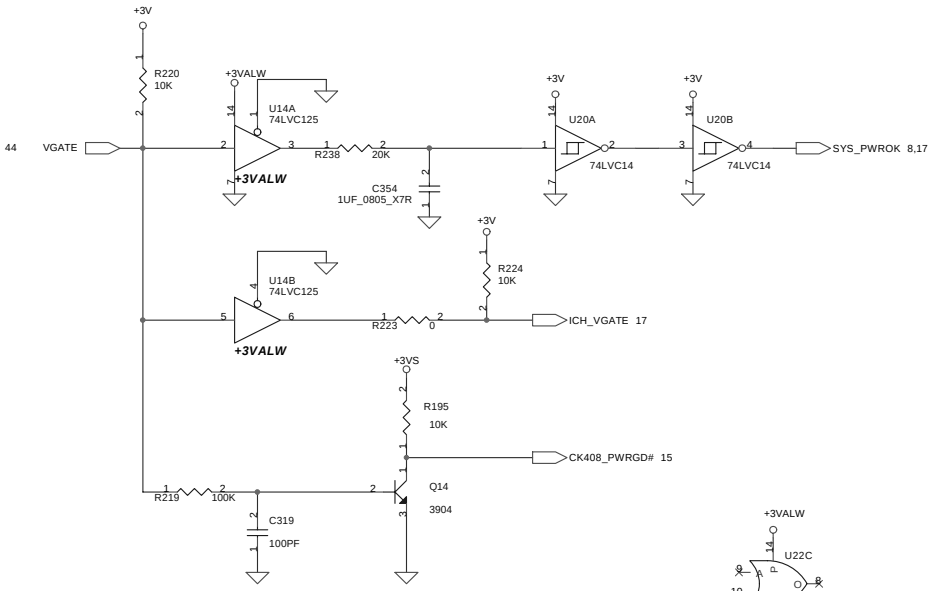
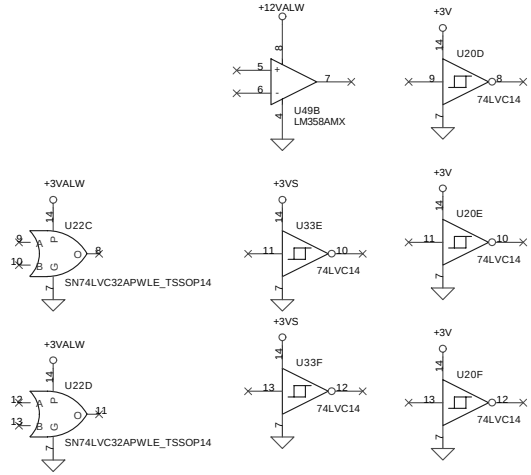
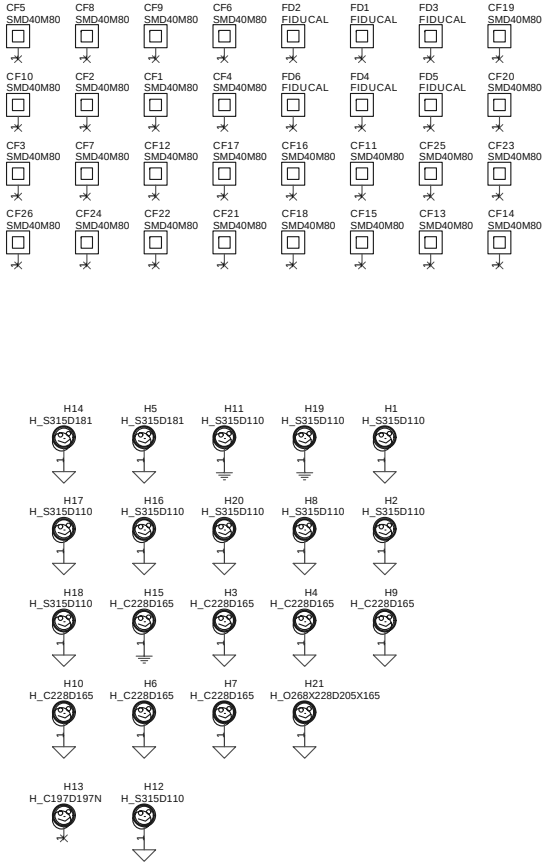
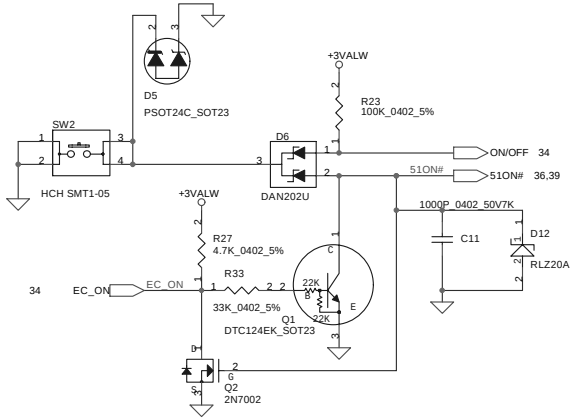
Power Good Circuit



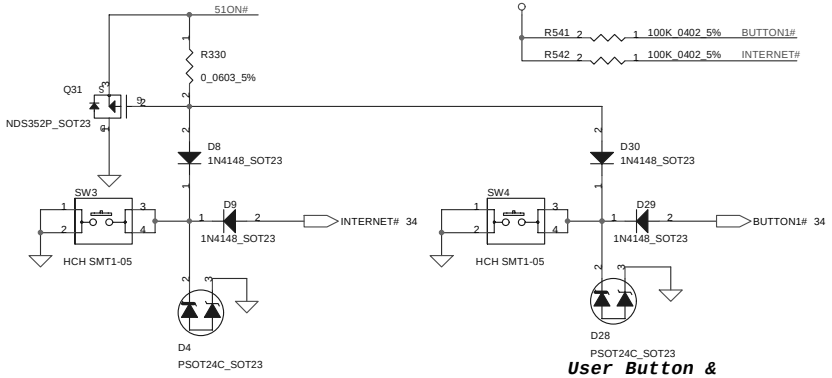




Power Button

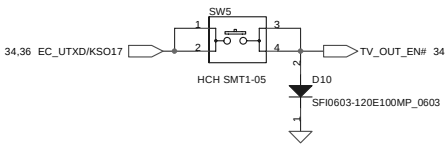


Internet Button



User Button & E-MAIL SW

TV-OUT BUTTON



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Compal Electronics, Ltd.

Title: PowerGood		
Size: Custom	Document Number: LA-1641	Rev: 0.2
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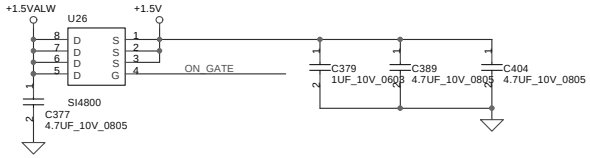
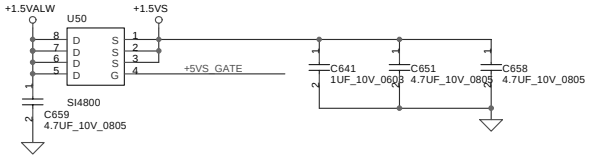
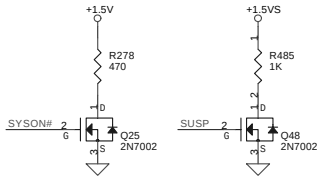
+1.5VALW To +1.5V Transfer



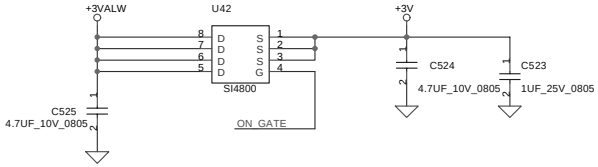
+1.5VALW To +1.5VS Transfer



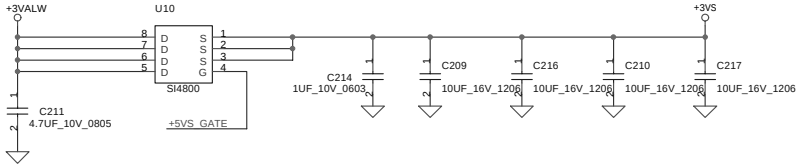
+1.5V & +1.5VS Discharge



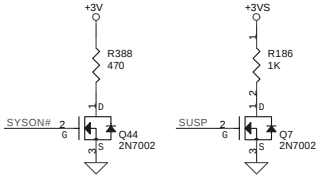
+3VALW To +3V Transfer



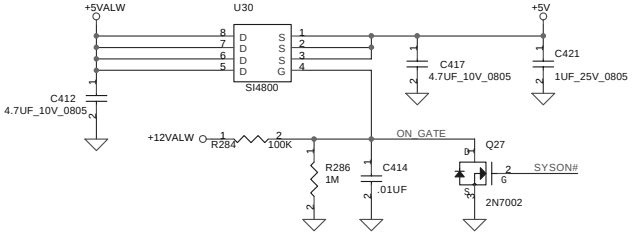
+3VALW To +3VS Transfer



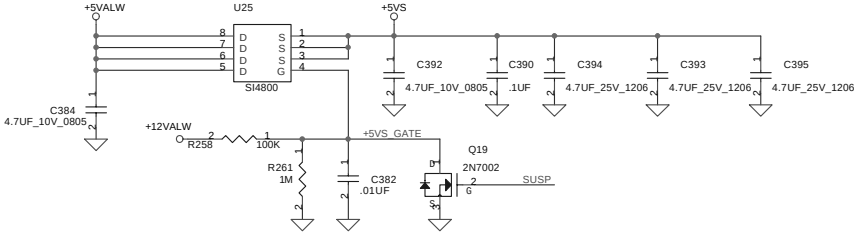
+3V & +3VS Discharge



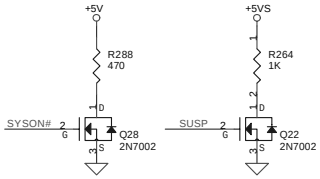
+5VALW To +5V Transfer



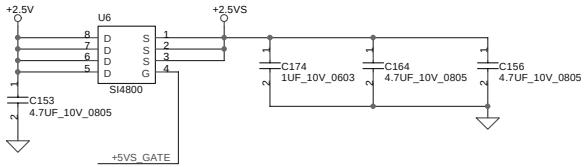
+5VALW To +5VS Transfer

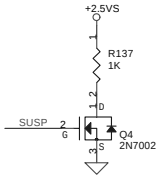


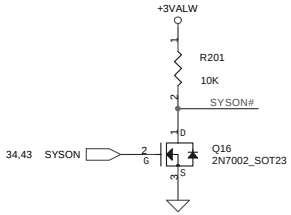
+5V & +5VS Discharge

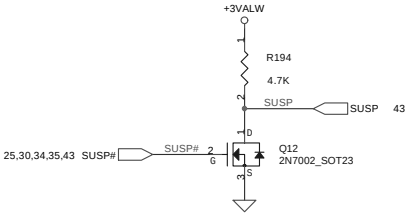


+2.5V To +2.5VS Transfer









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Compal Electronics, Ltd.

Title	DC/DC Interface	
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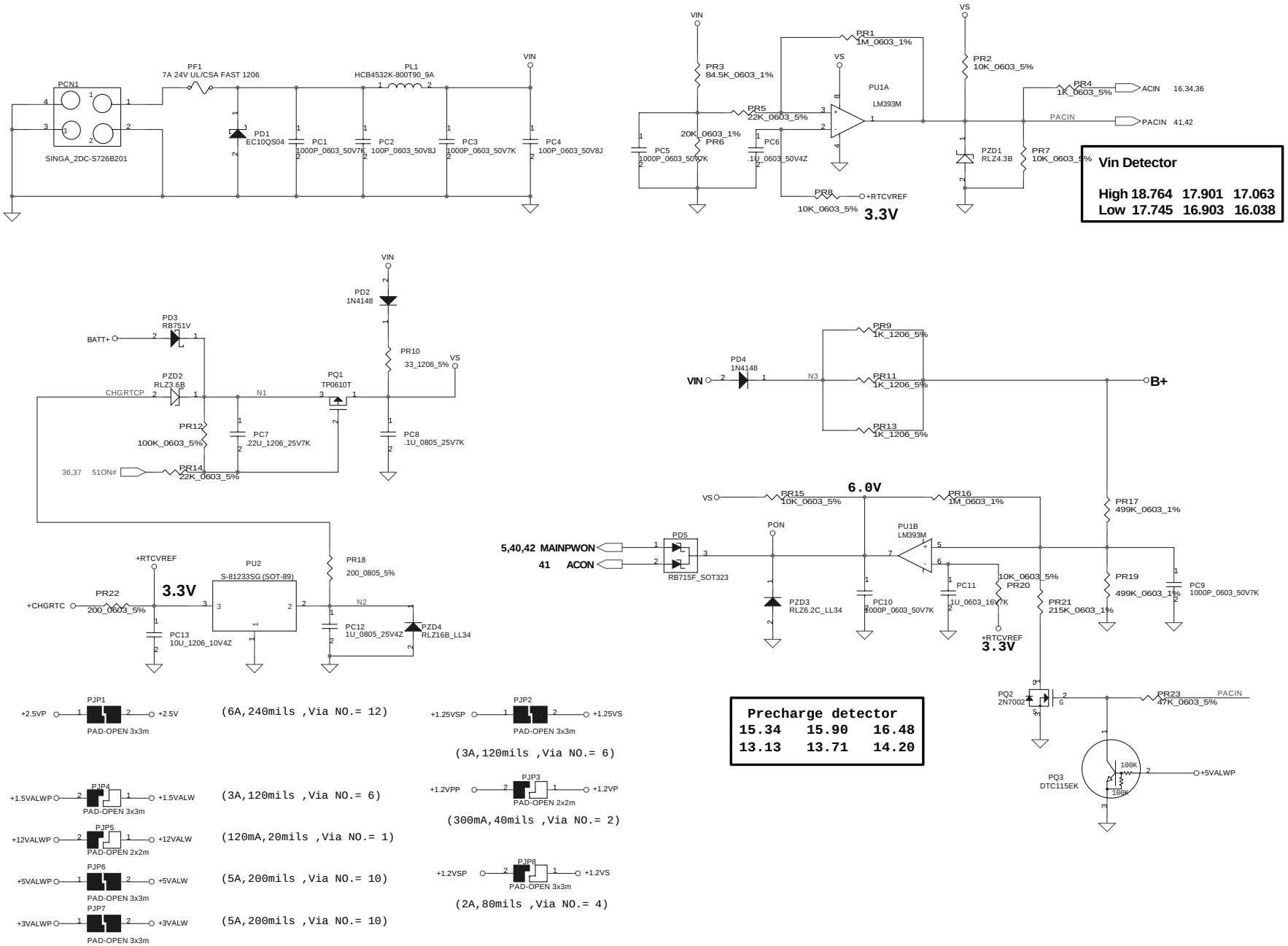

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Compal Electronics, Inc.

Title: **DCIN & DETECTOR**

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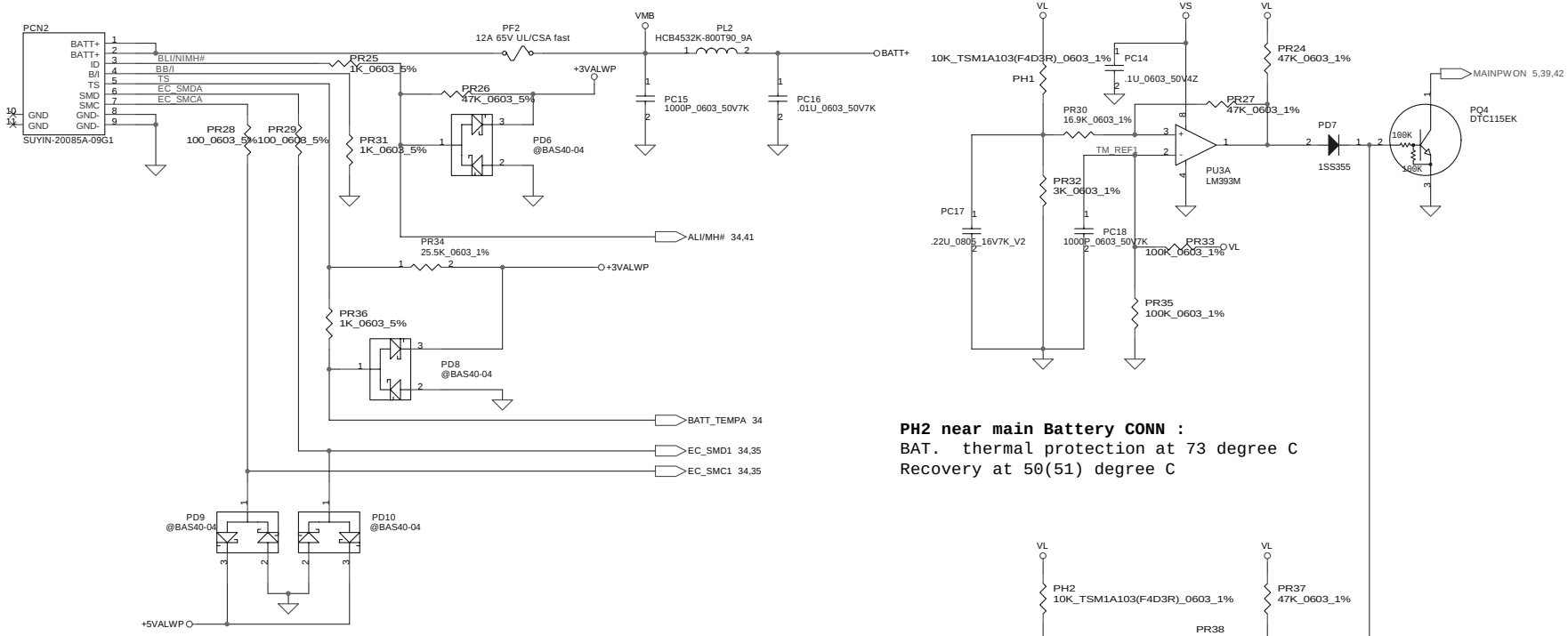
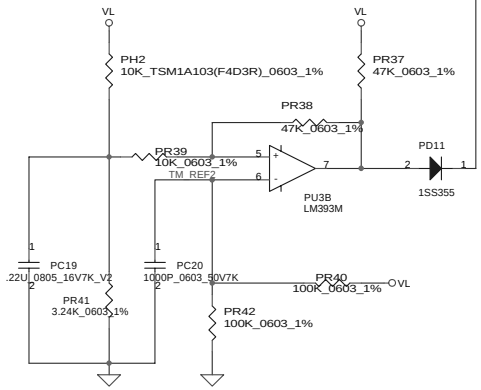
PH1 under CPU botten side :
CPU thermal protection at 87 degree C
Recovery at 48 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 73 degree C
Recovery at 50(51) degree C



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Compal Electronics, Inc.

Title: **BATTERY CONN / OTP**

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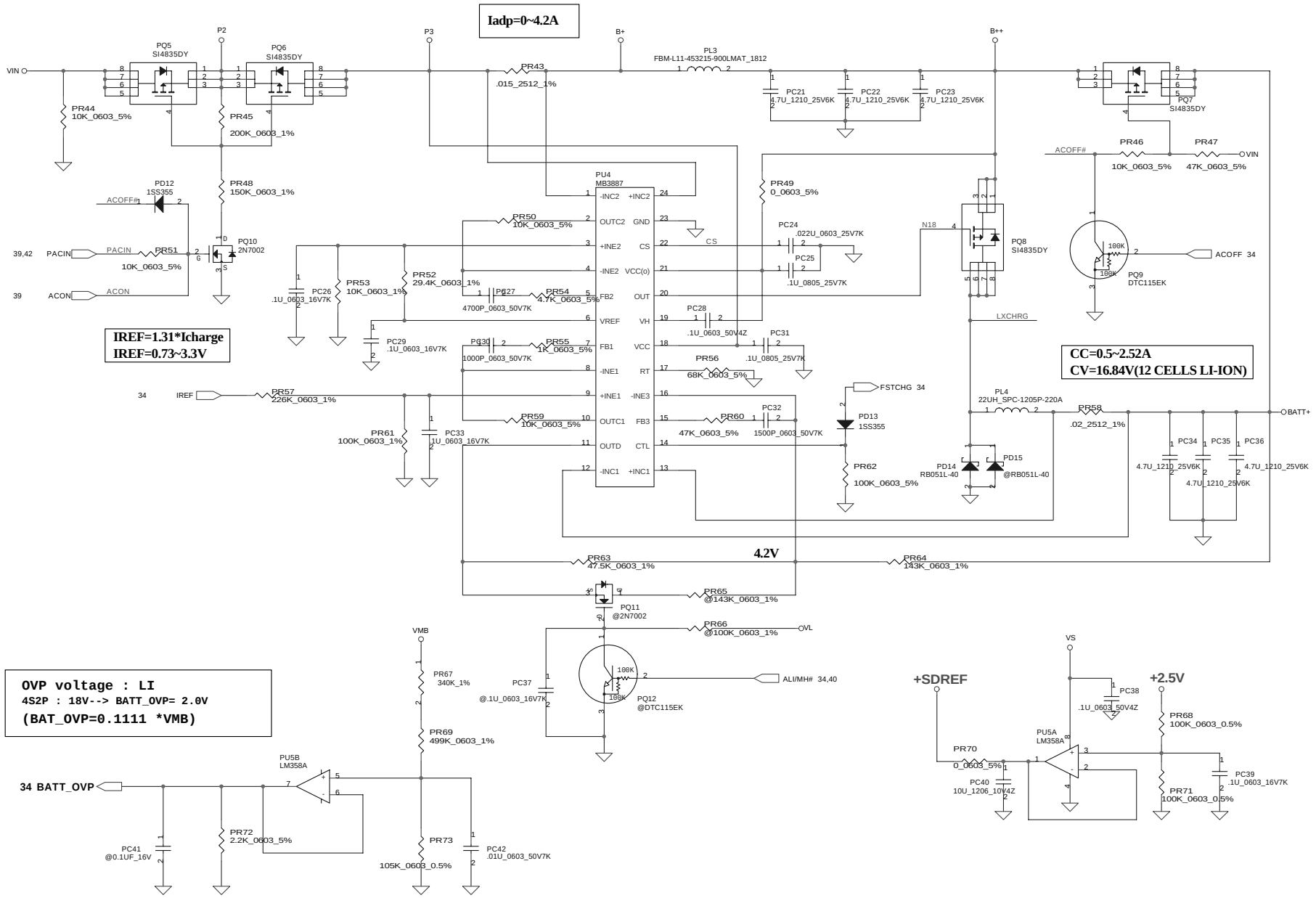

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Compal Electronics, Inc.

Title: **CHARGER**

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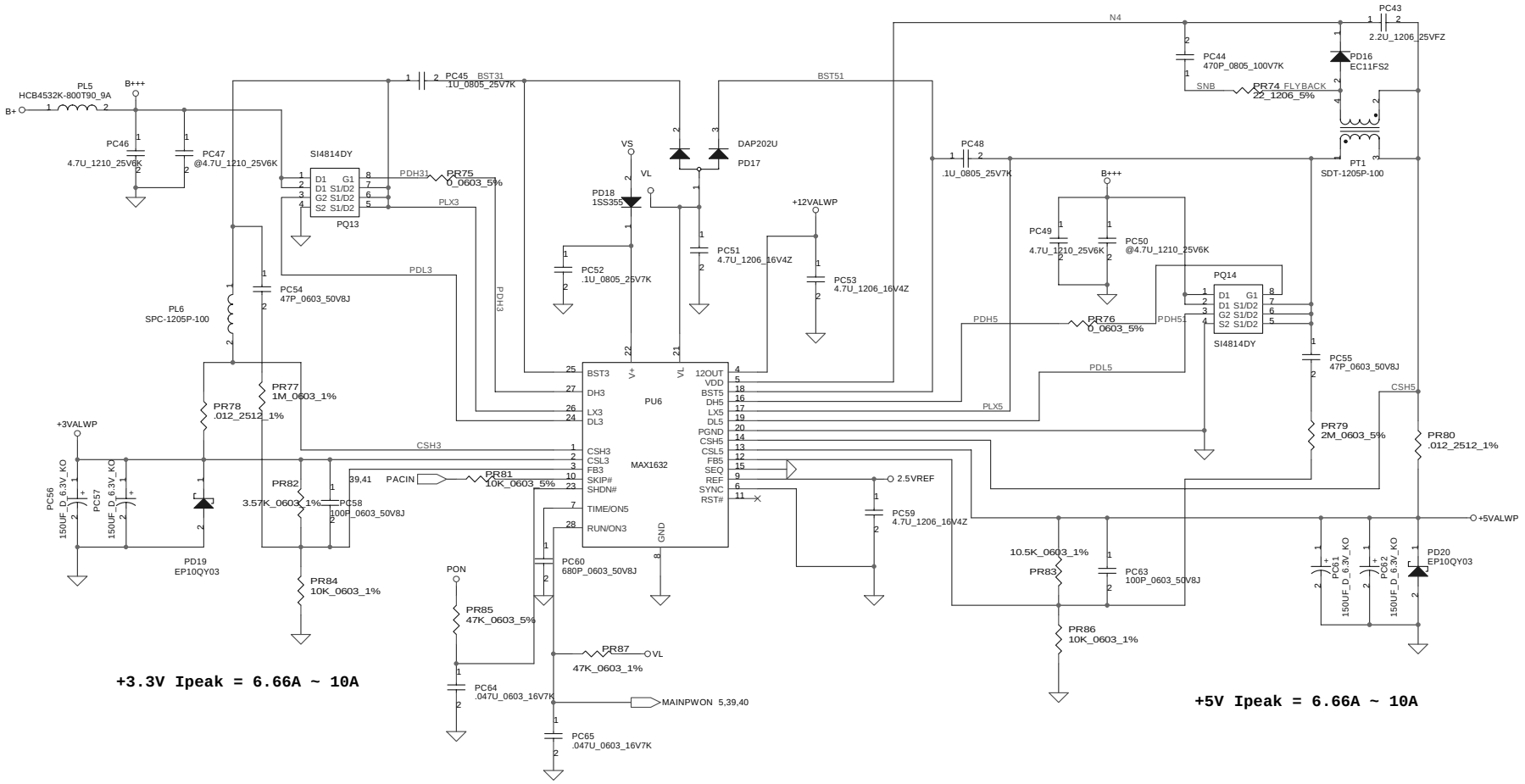

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Compal Electronics, Inc.

Title: **5V/3.3V/12V**

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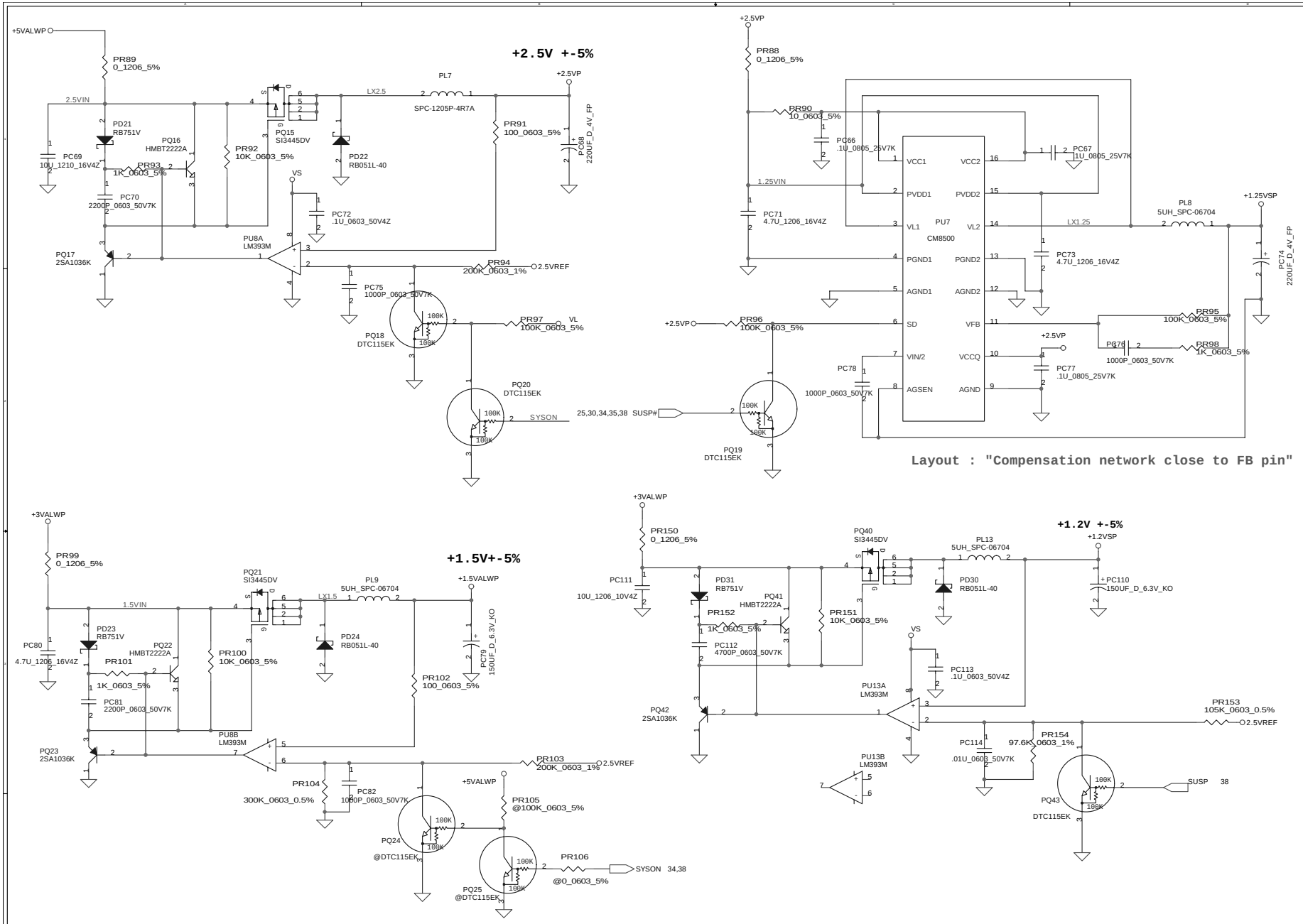

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Compal Electronics, Inc.

Title: **DDR / 2.5V / 1.25V/1.5V**

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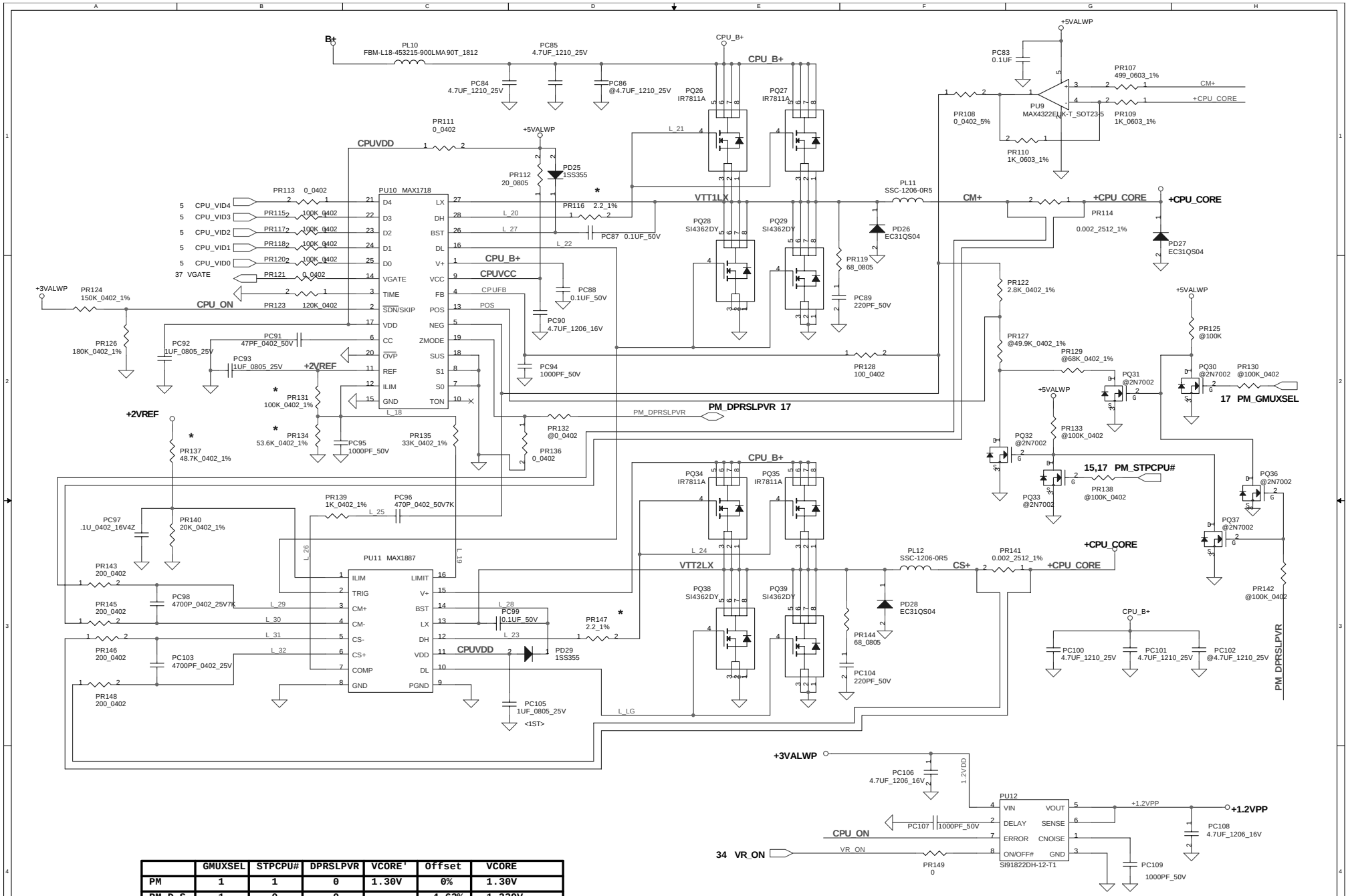

	GMUXSEL	STPCPU#	DPRSLPVR	VCORE'	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0		4.62%	1.239V
BM	0	1	0	1.20V	2.0%	1.176V
BM D-S	0	0	0		4.62%	1.144V
Deeper	X	0	1	1.0V	0%	1.0V

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Compal Electronics, Inc.

Title: **+CPU_CORE**

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REV 0.2

Date	Page	Description
09/27		Update Rev0.1 to Rev.0.2
10/16	8	Change U32(SSC) source from CLK_VCH to CLK_MCH_48M
	8	Change Q55 R537 R538 to U33A
	13	Add zero Ohm resistor between pin3 of JP1 and GND.
	15	Add R539 R540 2.2K pull high to +3VALW on net SMB_DATA and SMB_CLK
10/17	17	Add R549 on ICH4 GPI7 pull high to +3VS
	26	Add J3 between +5VS and +5VS_IDE
	17	Delete net USB_EN# and PAL/NTSC# on U12 pinW4 & pinW1
	29	Modify BlueTooth schematic
	32	Add Pass-High Filter (R550, R551, C676, C677) on net AMP_LEFT, AMP_RIGHT
	32	Change R465 power plan from +5VS to +5VCD
	34	Add Net Thertrip#, PM_SLP_S1#, BT_RST# on EC
	35	Change U23 to U22B
10/18	36	Change FAN Schematic from PWM to RPM
	37	Add R541 and R542 100K pull high to +3VALW on net Button1#, Internet#
10/22		Formal release Schematic Rev0.2

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