

COMPAL CONFIDENTIAL

MODEL NAME : *Sapporo XA*

COMPAL P/N : **DFL10**

PCB NO : **LA-2051**

Revision : *0.1A*

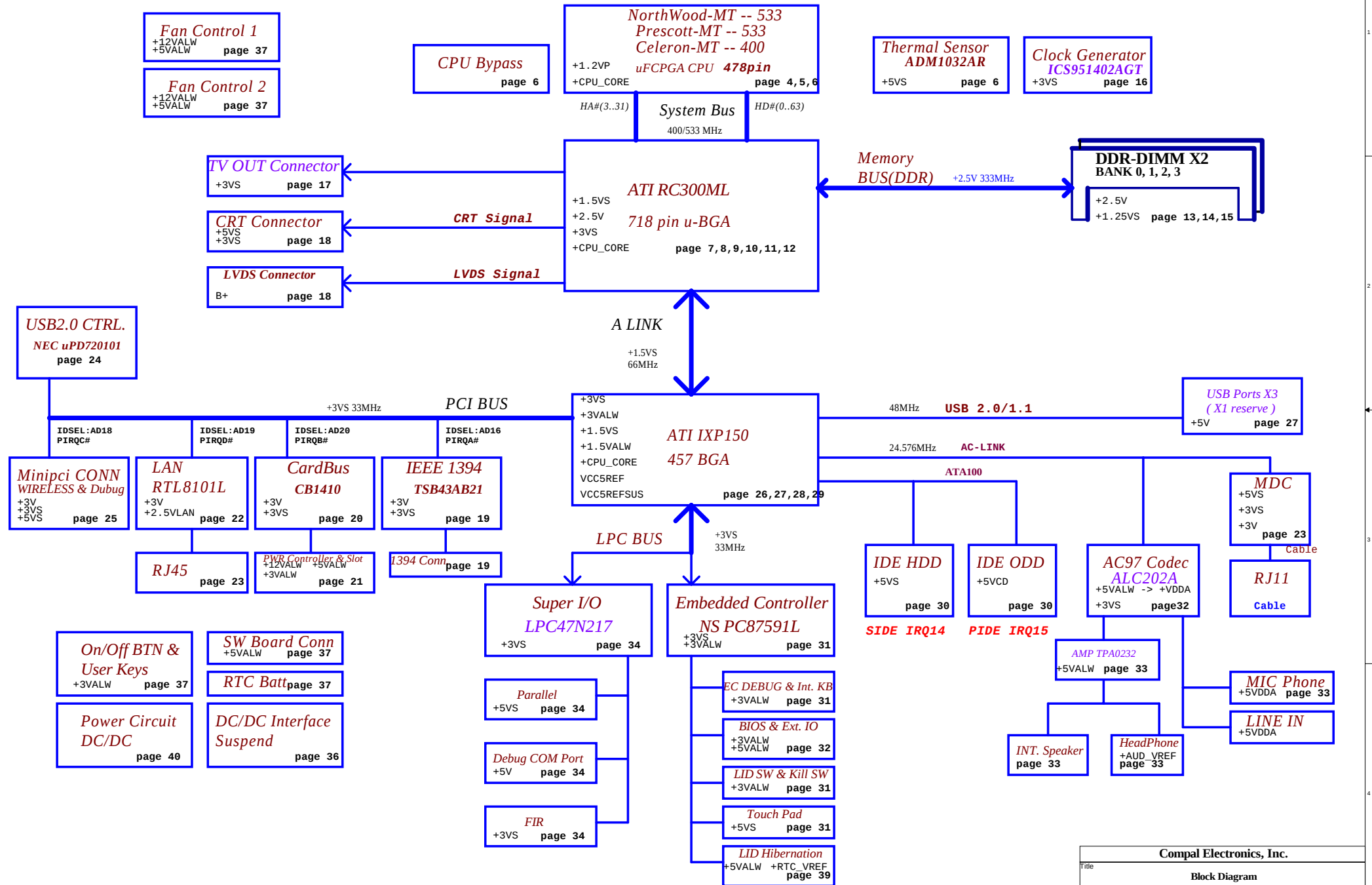
Sapporo XA Schematics Document

uFCBGA/uFCPGA NorthWood MT

2003 8 27 v0.1A

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Title			
Cover Sheet			
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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.2V	The voltage for Processor VID select	ON	OFF	OFF
+1.25VS	1.25V switched power rail for DDR Vtt	ON	OFF	OFF
+1.5VS	1.5V I/O power rail for ATI-RS300M/RC300M NB AGP.	ON	OFF	OFF
+1.8VS	1.8V switched power rail for ATI-RS300M/RC300M NB.	ON	OFF	OFF
+2.5VALW	2.5V always on power rail	ON	ON	ON*
+2.5V	2.5V system power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V system power rail for SB,LAN,CardReader and HUB.	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V system power rail .	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
NB Internal VGA	N/A	N/A	A
AGP BUS	AGP_DEVSEL	N/A	A
SOUTHBRIDGE	AD31 (INT.)	N/A	N/A
USB	AD30 (INT.)	N/A	D
AC97	AD31 (INT.)	N/A	B
ATA 100	AD31 (INT.)	N/A	A
ETHERNET	AD24(INT.)	N/A	C
1394	AD16	0	A
LAN	AD19	1	D
CARD BUS	AD20	2	A
Wireless LAN(MINI PCI) AD18		3	C

EXT USB AD23(EXT.) 4 A,C,D

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16)	1010 000X b		

EC SM Bus2 address

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 X
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 X

Power Managment table

Signal	+3VALW +5VALW +12VALW	+5V +3V +2.5V	+2.5VS +1.8VS +5VS +3VS +1.5VS +CPU_CORE +1.25VS
State			
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

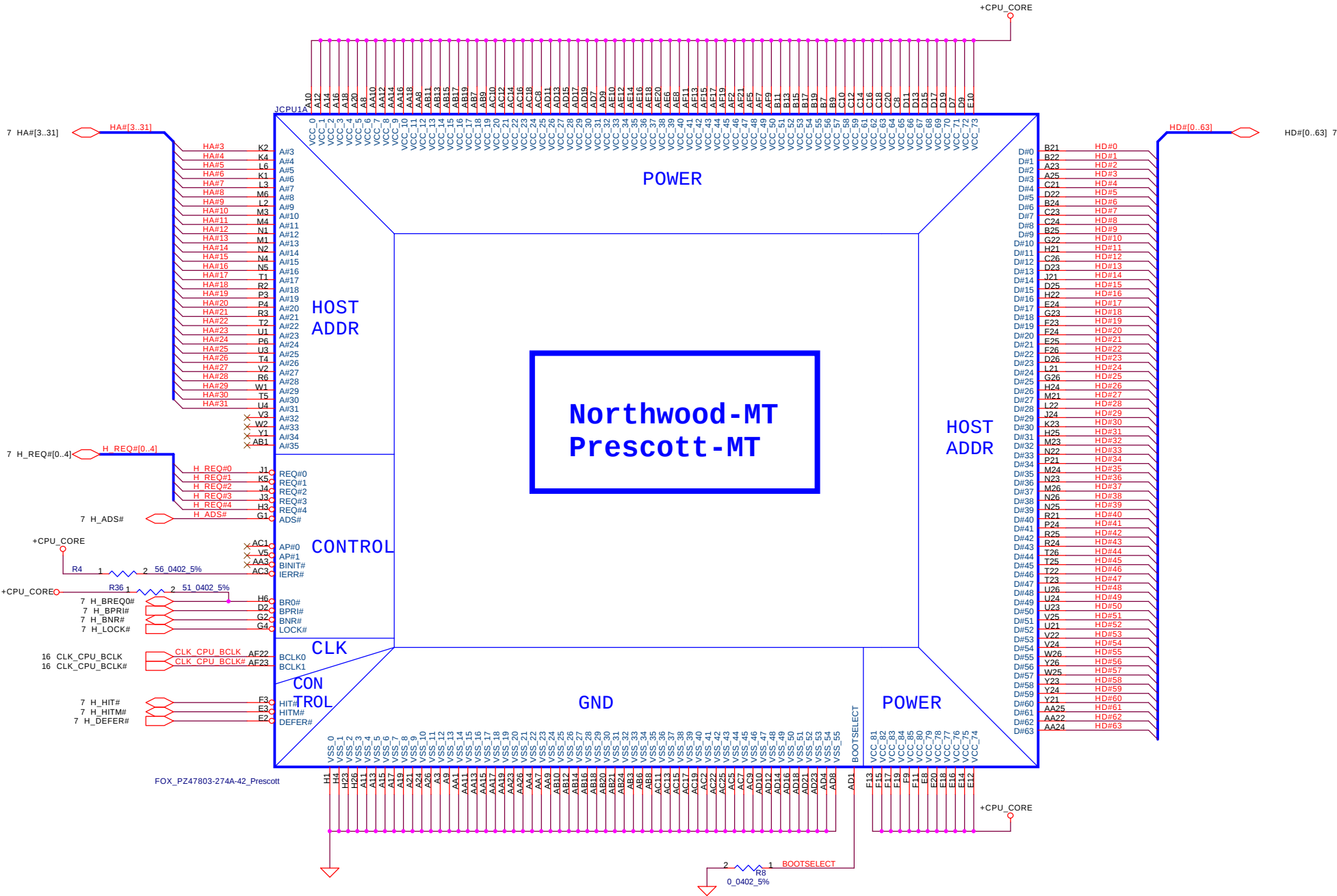
Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

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Title			
Note & Revision			
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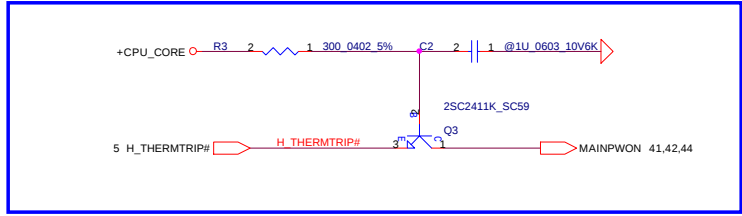
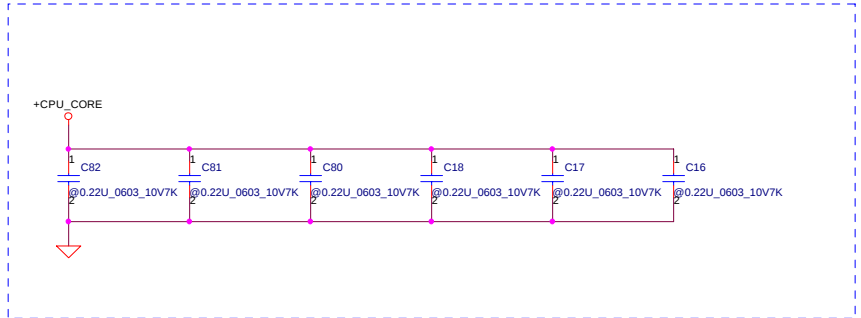
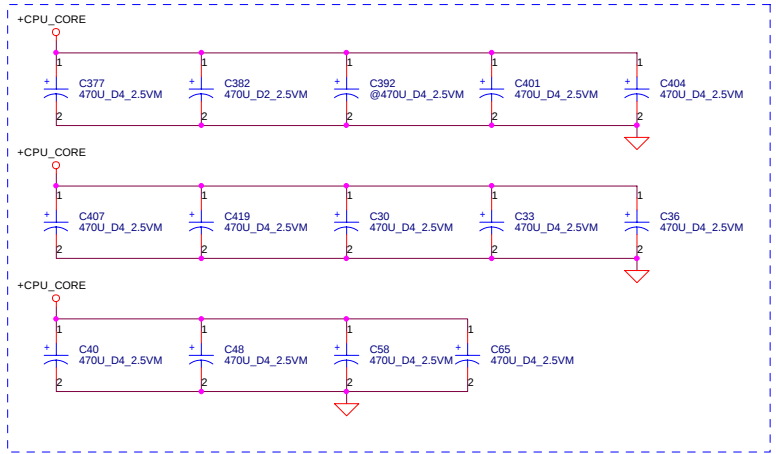
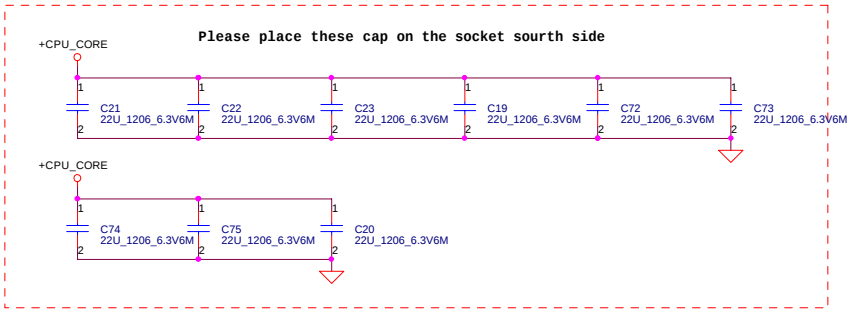
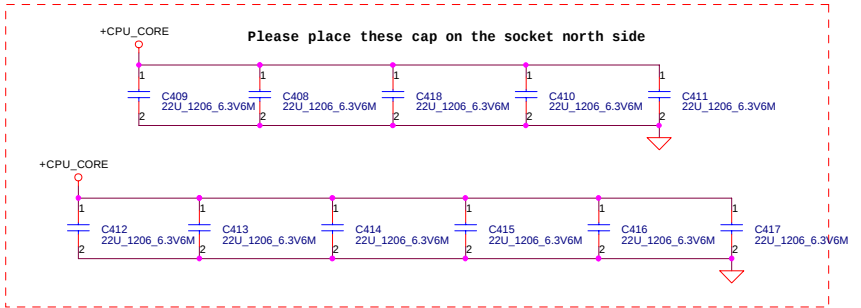
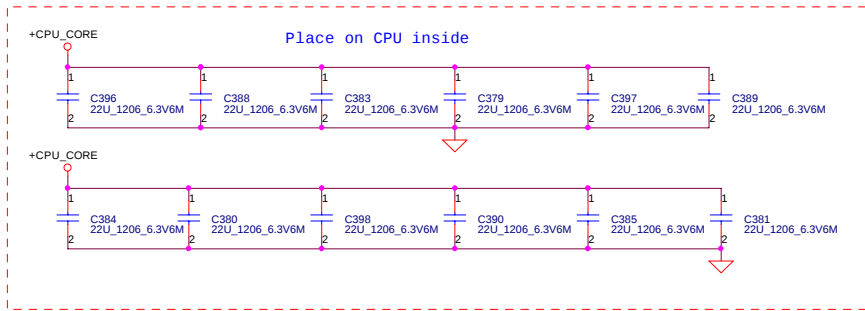
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Compal Electronics, Inc.		
Prescott / P4 uFCPGA (1/2)		
Title	Document Number	Rev
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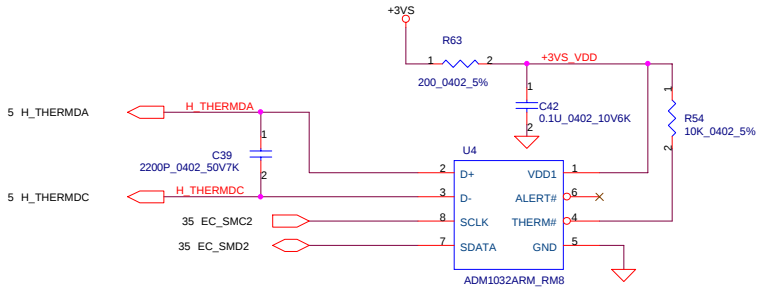
Layout note :
Place close to CPU, Use 2-3 vias per PAD.
Place 22uF caps x31 pcs, populated 14pcs.

Layout note :
Place close to CPU power and ground pin as possible (<1inch)

For Desktop's CPU:
470uFx15/12mOhm H=1.8 each
Total 0.923m ohm

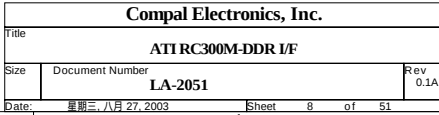


CPU Temperature Sensor



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Title CPU Decoupling CAP.			
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12.26 A_AD[0..31] A AD[0..31]
12.26 A_CBE#[0..3] A CBE#[0..3]

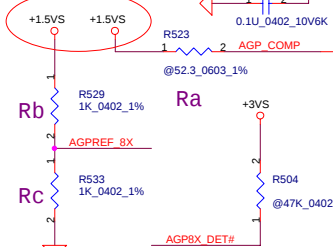
A AD0 AK5 ALINK_AD0
A AD1 AJ5 ALINK_AD1
A AD2 AJ6 ALINK_AD2
A AD3 AH4 ALINK_AD3
A AD4 AJ3 ALINK_AD4
A AD5 AJ2 ALINK_AD5
A AD6 AH2 ALINK_AD6
A AD7 AH1 ALINK_AD7
A AD8 AG2 ALINK_AD8
A AD9 AG1 ALINK_AD9
A AD10 AG3 ALINK_AD10
A AD11 AE3 ALINK_AD11
A AD12 AF1 ALINK_AD12
A AD13 AF2 ALINK_AD13
A AD14 AE4 ALINK_AD14
A AD15 AE3 ALINK_AD15
A AD16 AE4 ALINK_AD16
A AD17 AE5 ALINK_AD17
A AD18 AE6 ALINK_AD18
A AD19 AC2 ALINK_AD19
A AD20 AC4 ALINK_AD20
A AD21 AB3 ALINK_AD21
A AD22 AB5 ALINK_AD22
A AD23 AB5 ALINK_AD23
A AD24 AB6 ALINK_AD24
A AD25 AA2 ALINK_AD25
A AD26 AA4 ALINK_AD26
A AD27 AA5 ALINK_AD27
A AD28 AA6 ALINK_AD28
A AD29 Y3 ALINK_AD29
A AD30 Y5 ALINK_AD30
A AD31 Y6 ALINK_AD31

A CBE#0 AG4 ALINK_CBE#0
A CBE#1 AE2 ALINK_CBE#1
A CBE#2 AC3 ALINK_CBE#2
A CBE#3 AC3 ALINK_CBE#3

12.26 A_PAR A STROBE# A ACAT# A END#
26 A_PIRQA# R517 1 2 0.0402_5%
19.20,24,26 PCI_PIRQA#
26 A_DEVSEL# A DEVSSEL# A OFF#
26 A_SBRREQ# A SBREQ#
26 A_SBGNT# A SBGNT#

+3VS 8.2K_0402_5% R500

AGP8X_DET# M5
AGPREF_8X C615 1 2 0.1U_0402_10V6K
AGP_COMP R523 1 2 @52.3_0603_1%



CHS-216GP9050A21_BGA718

	8X(M9+M10@)	4X(NAGP@)
Ra	169_0402_1%	52_1_0402_1%
Rb	324_0402_1%	1K_0402_1%
Rc	100_0402_1%	1K_0402_1%

PCI Bus 0 / A-Link / IF
PCI BUS 1 / AGP Bus (GPIO , TMD5 , ZVPort)

AGP_AD0/TMD2_HSYNC Y2
AGP_AD1/TMD2_VSYNC W3
AGP_AD2/TMD2_D1 W2
AGP_AD3/TMD2_D0 V3
AGP_AD4/TMD2_D3 V2
AGP_AD5/TMD2_D2 V1
AGP_AD6/TMD2_D5 U3
AGP_AD7/TMD2_D4 U2
AGP_AD8/TMD2_D6 T2
AGP_AD9/TMD2_D9 R2
AGP_AD10/TMD2_D8 R1
AGP_AD11/TMD2_D11 N3
AGP_AD12/TMD2_D10 N2
AGP_AD13 AGP_AD13
AGP_AD14 AGP_AD14
AGP_AD15 AGP_AD15
AGP_AD16/TMD1_VSYNC L2
AGP_AD17/TMD1_HSYNC L1
AGP_AD18/TMD1_DE K2
AGP_AD19/TMD1_D0 J3
AGP_AD20/TMD1_D1 J2
AGP_AD21/TMD1_D3 J1
AGP_AD22/TMD1_D4 F3
AGP_AD24/TMD1_D1 F2
AGP_AD25/TMD1_D6 F2
AGP_AD26/TMD1_D9 F2
AGP_AD27/TMD1_D8 E2
AGP_AD28/TMD1_D11 E1
AGP_AD29/TMD1_D10 D2
AGP_AD30/TMD5_HPD D1
AGP_AD31 ALINK_AD31

AGP2_SBSTB/AGP3_SBSTB/NC/LVDS_BLOK
AGP2_SBSTB/AGP3_SBSTB/NC/ENA_BL
AGP2_ADSTB0/AGP3_ADSTB0/TMD2_CLK#
AGP2_ADSTB0/AGP3_ADSTB0/TMD2_CLK
AGP2_ADSTB1/AGP3_ADSTB1/TMD1_CLK#
AGP2_ADSTB1/AGP3_ADSTB1/TMD1_CLK

AGP2_CBE#0/AGP3_CBE0/TMD2_D7
AGP2_CBE#1/AGP3_CBE1/TMD2_DE
AGP2_CBE#2/AGP3_CBE2
AGP2_CBE#3/AGP3_CBE3/TMD1_D5

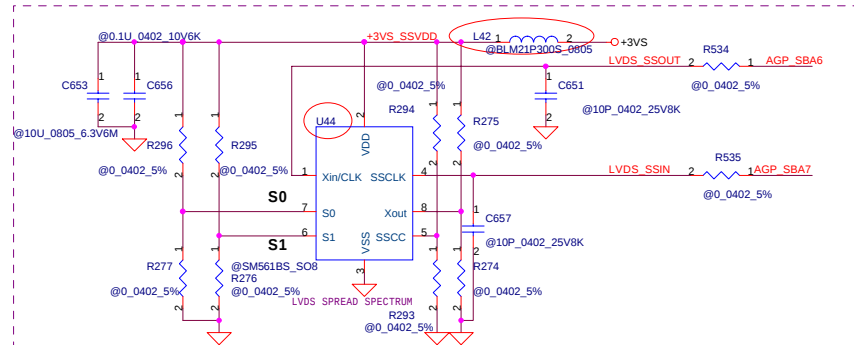
AGP2_IRDY#/AGP3_IRDY#/GPIO8/I2C_CLK
AGP2_TRDY#/AGP3_TRDY#/TMD5_DVI_CLK
AGP2_STOP#/AGP3_STOP#/GPIO10/DDC_DATA

AGP2_FRAME#/AGP3_FRAME#/TMD5_DVI_DATA
AGP2_DEVSEL#/AGP3_DEVSEL#/GPIO9/I2C_DATA
AGP2_PIPE#/AGP3_DBI_HI
AGP2_NCI/AGP3_DBI_LO
AGP2_RBF#/AGP3_RBF
AGP2_WBF#/AGP3_WBF

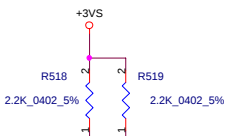
AGP2_SBA0/AGP3_SBA#0/GPIO0/VDDC_CNTL0
AGP2_SBA1/AGP3_SBA#1/GPIO1/VDDC_CNTL1
AGP2_SBA2/AGP3_SBA#2/GPIO2/LVDS_BLOK#
AGP2_SBA3/AGP3_SBA#3/GPIO3/DIGON
AGP2_SBA4/AGP3_SBA#4/GPIO4/STP_AGP#
AGP2_SBA5/AGP3_SBA#5/GPIO5/AGP_BUSY#
AGP2_SBA6/AGP3_SBA#6/GPIO6/LVDS_SSOUT
AGP2_SBA7/AGP3_SBA#7/GPIO7/LVDS_SSIN

AGP_ST0
AGP_ST1
AGP_ST2

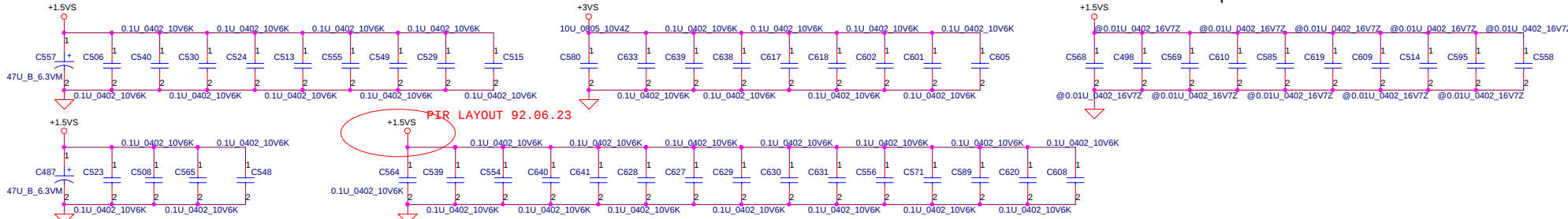
DDC_CLK C3
DDC_DAT C2
AGP_SBA2 E4
AGP_SBA3 E4
AGP_SBA4 E6
AGP_SBA5 E5
AGP_SBA6 G6
AGP_SBA7 G5



Note: PLACE CLOSE TO U2 (NB RC300M)



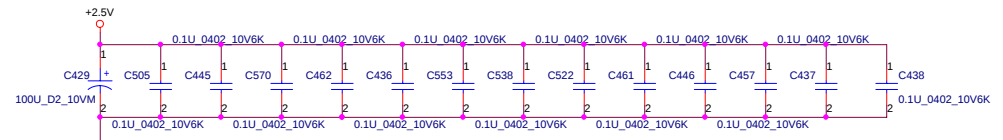
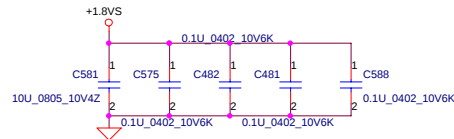
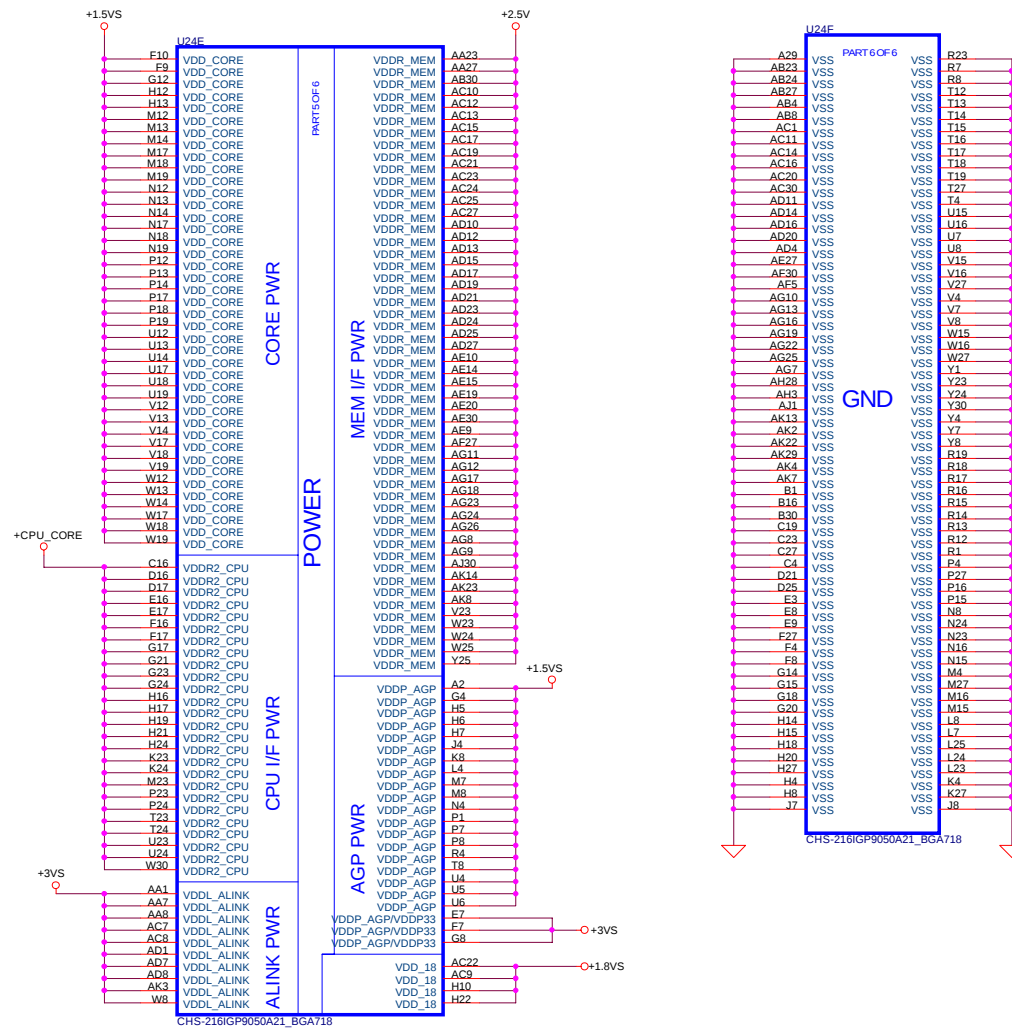
ATI request



Note: PLACE CLOSE TO U27 (NB RC300M)

Compal Electronics, Inc.			
Title			
ATI RC300M-AGP, ALINK BUS			
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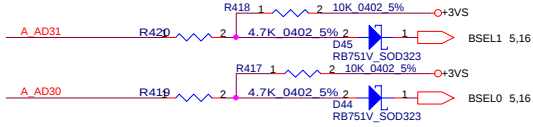
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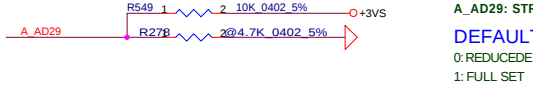
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Title			
ATI RC300M-POWER			
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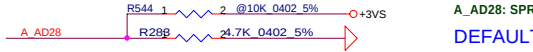
9,26 A_AD[0..31] A_AD[0..31]
9,26 A_CBE#[0..3] A_CBE#[0..3]



A_AD[31..30] : FSB CLK SPEED
DEFAULT: 01
00: 100 MHZ
01: 133 MHZ
10: 200MHZ
11:166 MHZ



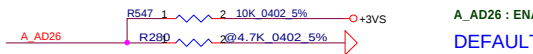
A_AD29: STRAP CONFIGURATION
DEFAULT:1
0: REDUCEDE SET
1: FULL SET



A_AD28: SPREAD SPECTRUM ENABLE
DEFAULT:0
0: DISABLE
1: ENABLE



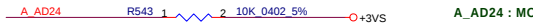
A_AD27: FrcShortReset#
DEFAULT: 1
0: TEST MODE
1: NORMAL MODE



A_AD26 : ENABLE IOQ
DEFAULT: 1
0: IOQ=1
1: IOQ=12



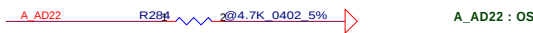
A_AD25/A_AD17 : CPU VOLTAGE[1..0]
DEFAULT: 10
AD25=1 DESTOP CPU
AD25=0 MOBILE CPU
AD17 - -DON'T CARE
00: 1.05V
01: 1.35V
11: 1.75V
10: 1.45V



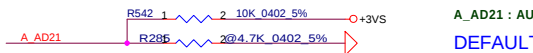
A_AD24 : MOBILE CPU SELECT
DEFAULT: 1
0: BANIAS CPU
1: OTHER CPU



A_AD23 : CLOCK BYPASS DISABLE
DEFAULT: 1
0: TEST MODE
1: NORMAL



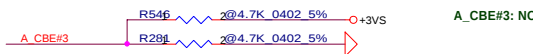
A_AD22 : OSC PAD OUTPUT PCICLK
DEFAULT : 1
0:PCICLK OUT
1: OSC CLK OUT



A_AD21 : AUTO_CAL ENABLE
DEFAULT : 1
0: DISABLE
1: ENABLE



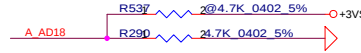
A_AD20 : INTERNAL CLK GEN ENABLE
DEFAULT : 0
0: DISABLE
1: ENABLE



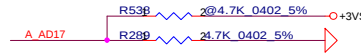
A_CBE#3: NOT USED



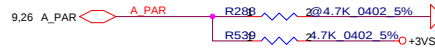
A_CBE#0 :NO USED



A_AD18 : ENABLE PHASE CALIBRATION
DEFAULT: 0
0: DISABLE
1:ENABLE



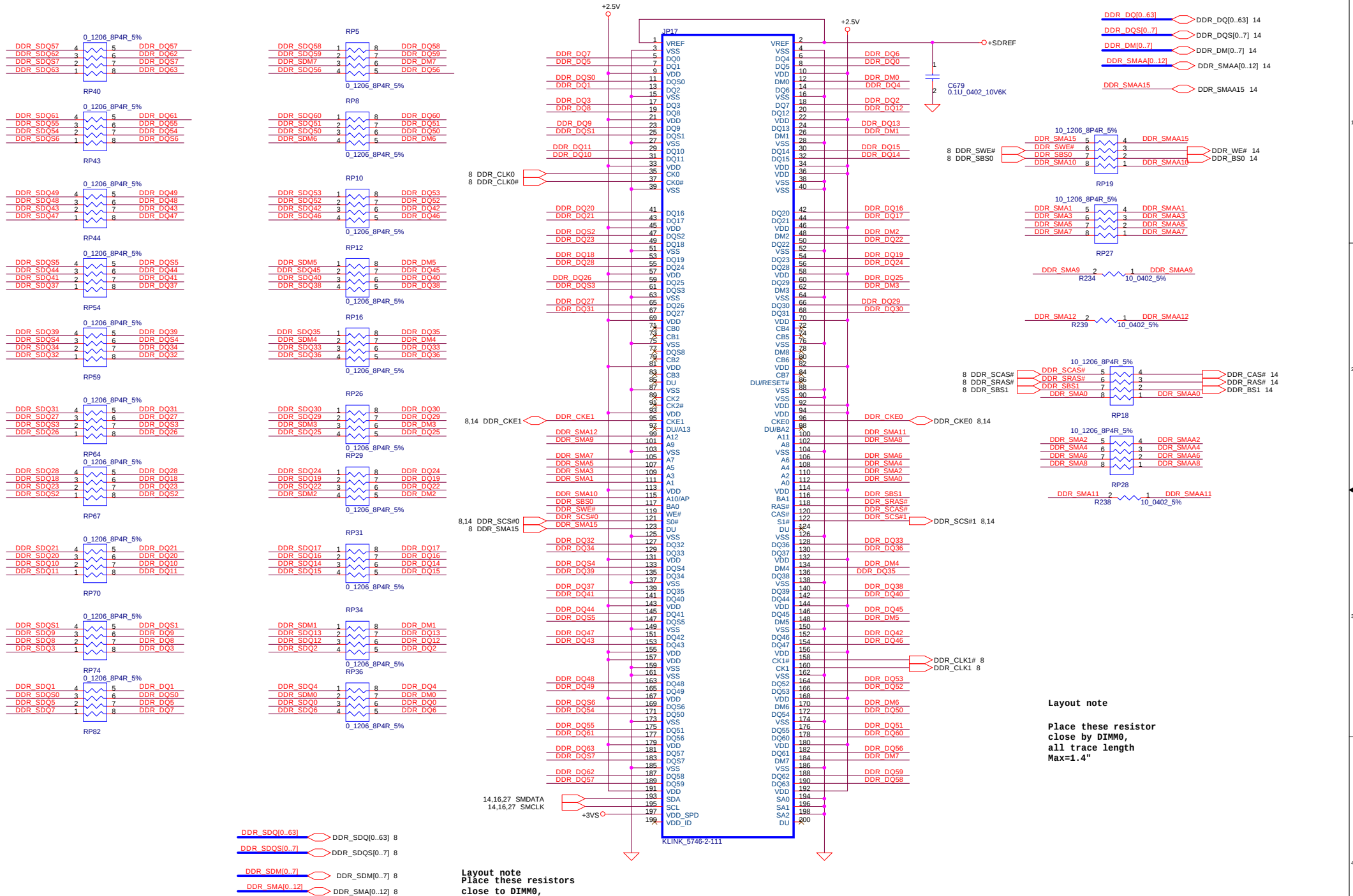
A_AD25/A_AD17 : CPU VOLTAGE[1..0]
DEFAULT: 0
00: 1.05V
01: 1.35V
11: 1.75V
10: 1.45V



PAR: EXTENDED DEBUG MODE
DEFAULT : 1
0: DEBUG MODE
1: NORMAL

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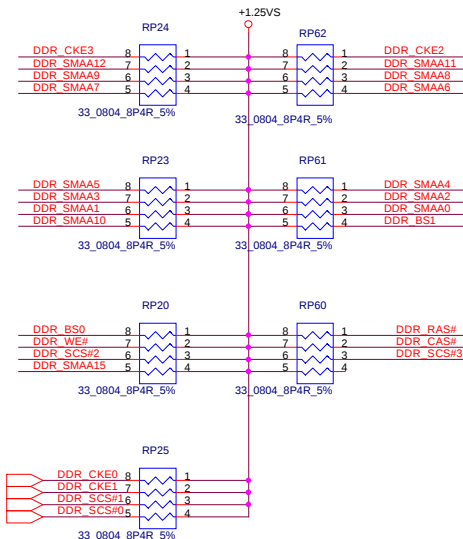
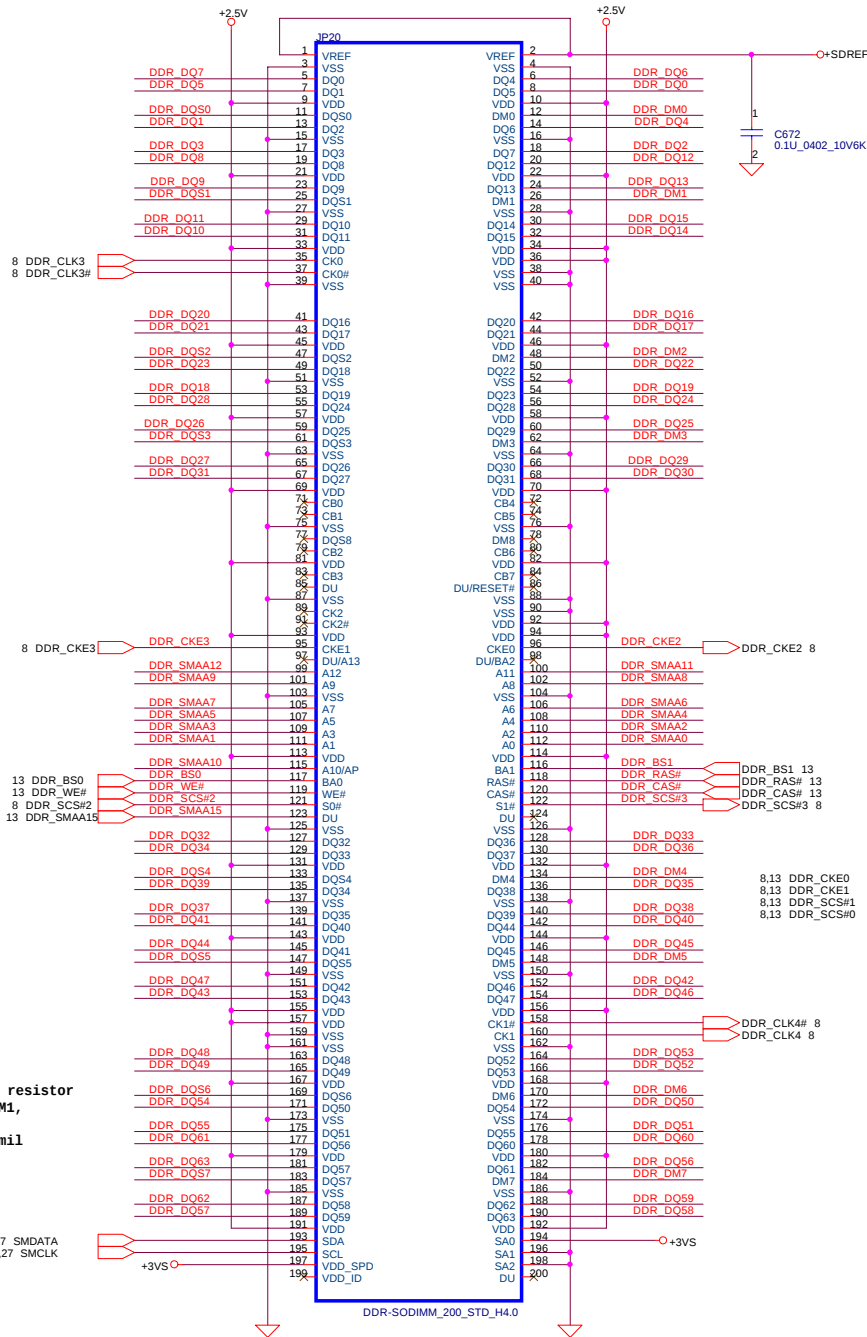
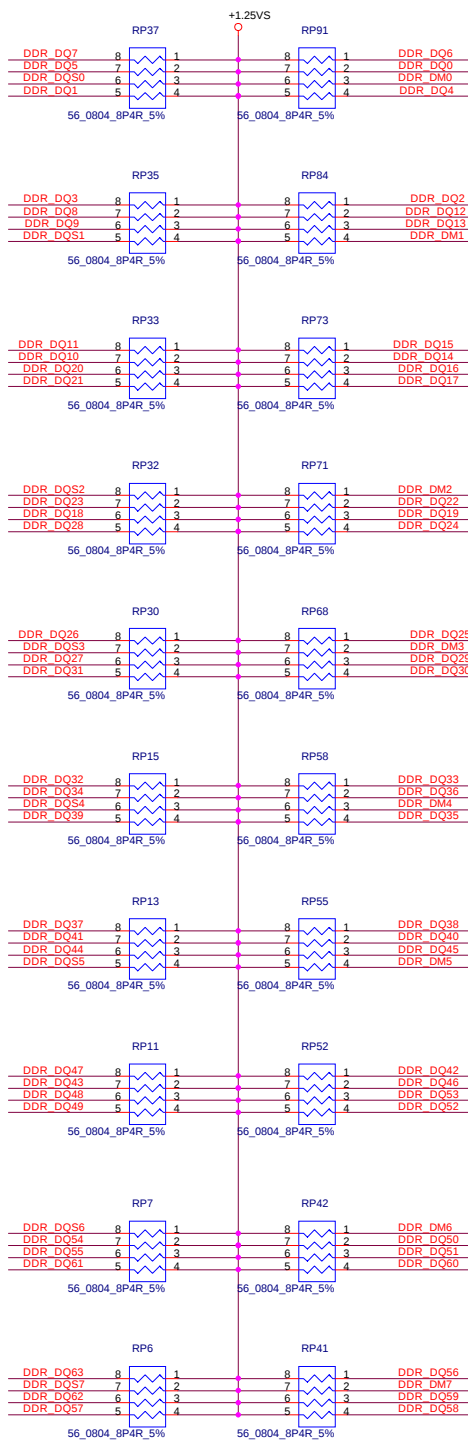
Compal Electronics, Inc.			
Title			
AT1RC300M-SYSTEM STRAP			
Size	Document Number	Rev	
	L/A-2051	0.1A	
Date:	星期三, 八月 27, 2003	Sheet	12 of 51



DDR TOPOLOGY 1 FOR SMAA[0, 3, 6:12], SBA[1, 0], SRAS#, SCAS#, SWE#

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Compal Electronics, Inc.			
Title			
DDR-SODIMM SLOT0			
Size	Document Number	Rev	
	LA-2051	0.1A	
Date	星期三, 八月 27, 2003	Sheet	13 of 51



Layout note
Place these resistor
closely DIMM1,
all trace
length<=800mil

13,16,27 SMATA
13,16,27 SMCLK

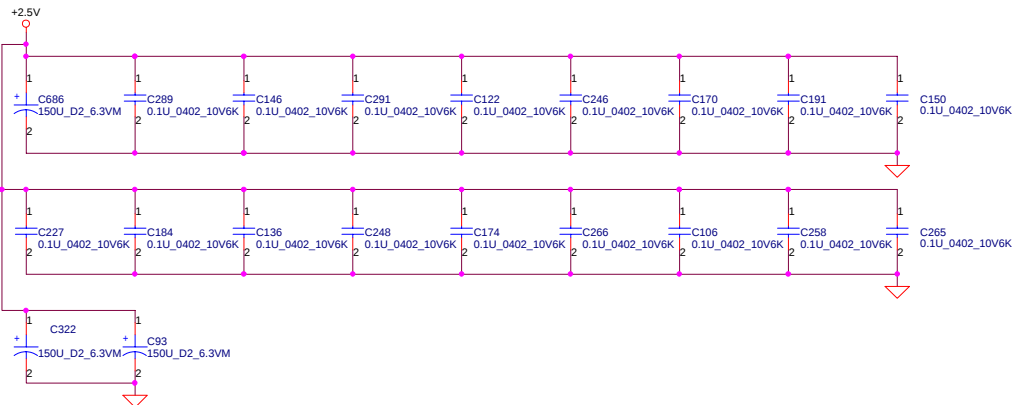
DDR TOPOLOGY 1 FOR SMAA[0, 3, 6:12], SBA[1, 0], SRAS#, SCAS#, SWE#

Layout note
Place these resistor
close by DIMM1,
all trace length
Max=0.8"

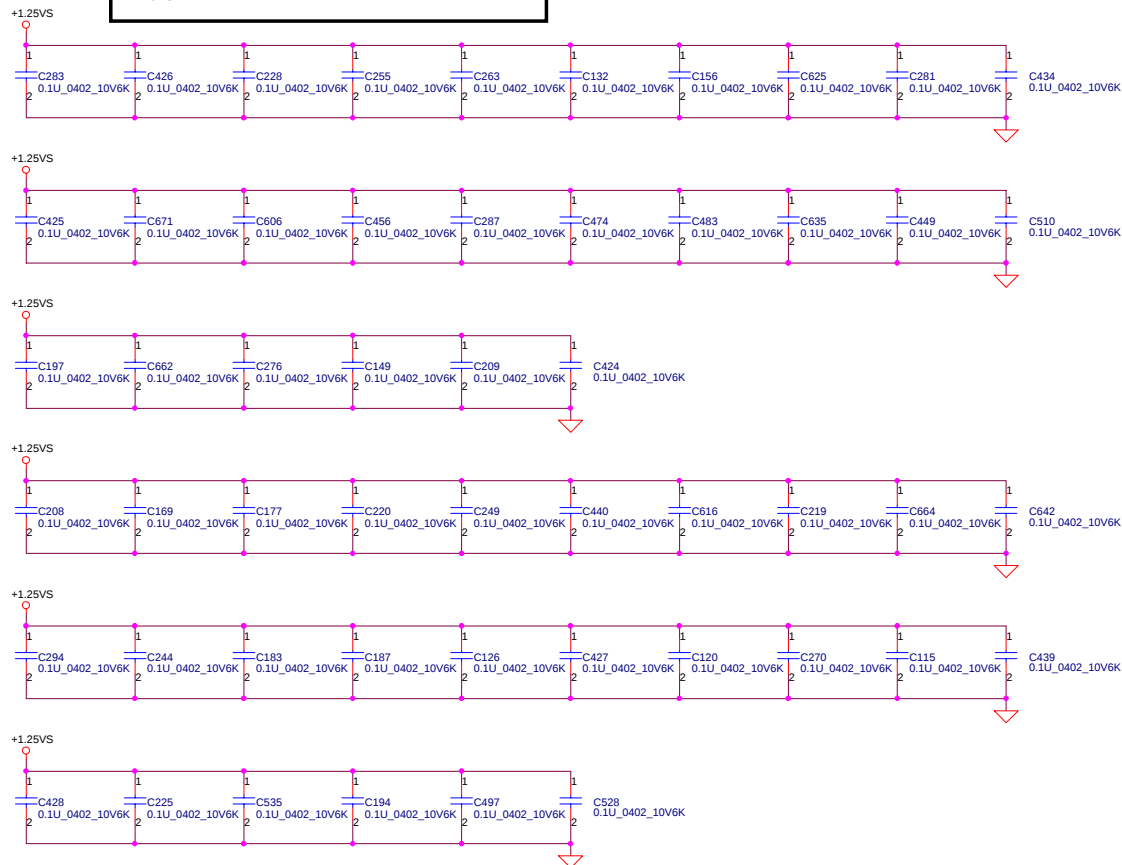
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Compalelectronics, Inc.			
Title			
DDR-SODIMM SLOT1			
Size	Document Number	Rev	
	LA-2051	0.1A	
Date:	星期三, 八月 27, 2003	Sheet	14 of 51

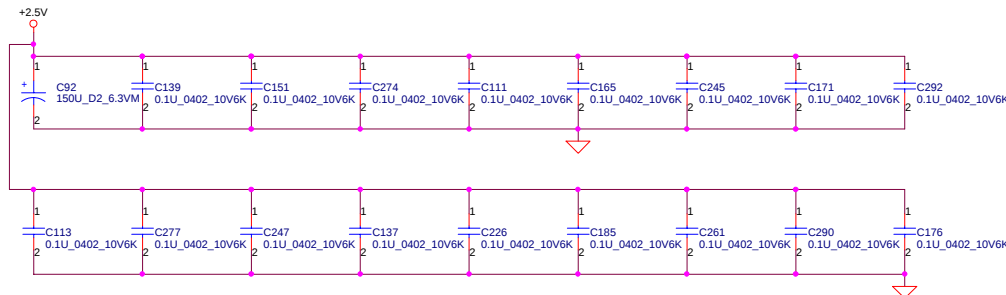
Layout note :
Distribute as close as possible
to DDR-SODIMM0.



Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25VS

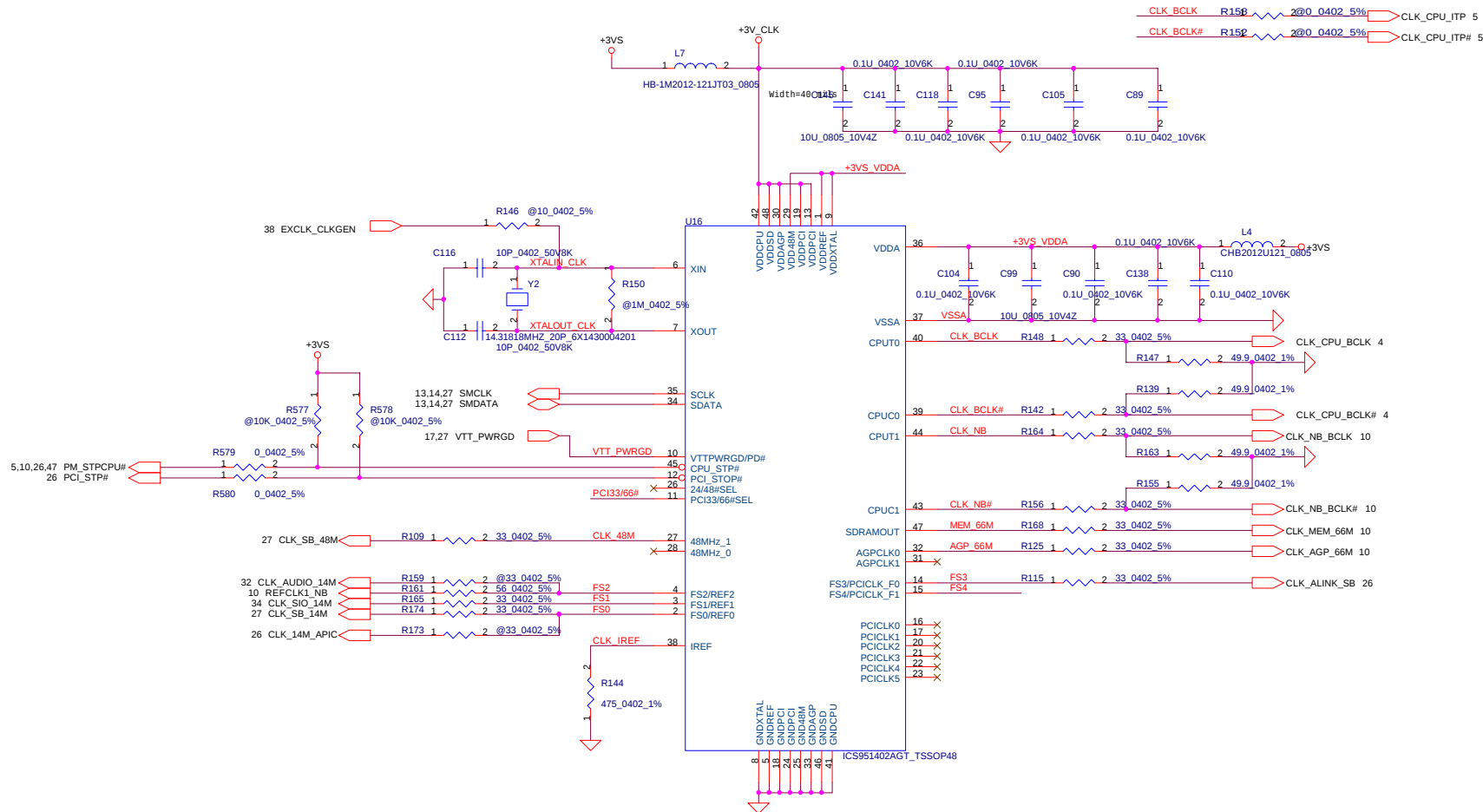


Layout note :
Distribute as close as possible
to DDR-SODIMM1.



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Compal Electronics, Inc.			
Title			
DDR SODIMM Decoupling			
Size	Document Number	Rev	
	L/A-2051	0.1A	
Date:	星期三, 八月 27, 2003	Sheet	15 of 51



CLOCK FREQUENCY SELECT TABLE

FS4	FS3	FS2	FS1	FS0	CPU	MEM	With Spread Enabled...
0	0	0	1	0	200	200	Spread OFF OR Center spread +/-0.3%
0	0	0	0	1	133	133	
0	0	0	0	0	100	100	

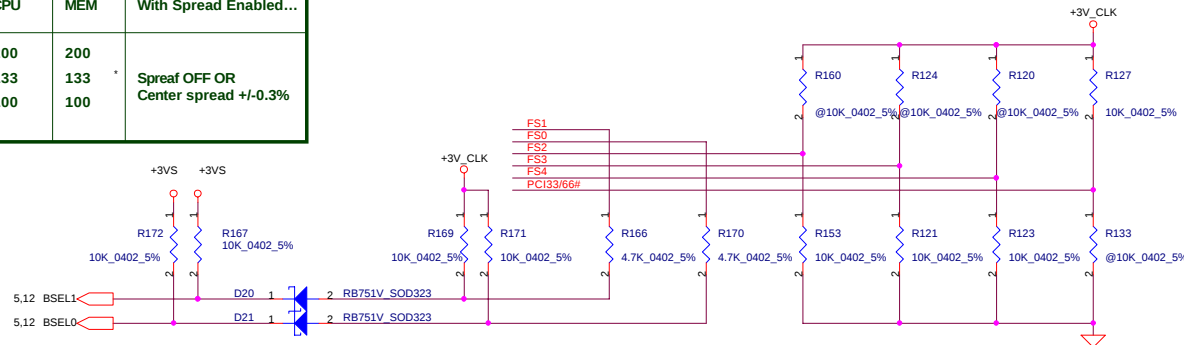
**

Note: 0 = PULL LOW
1 = PULL HIGH

A-LINK FREQ

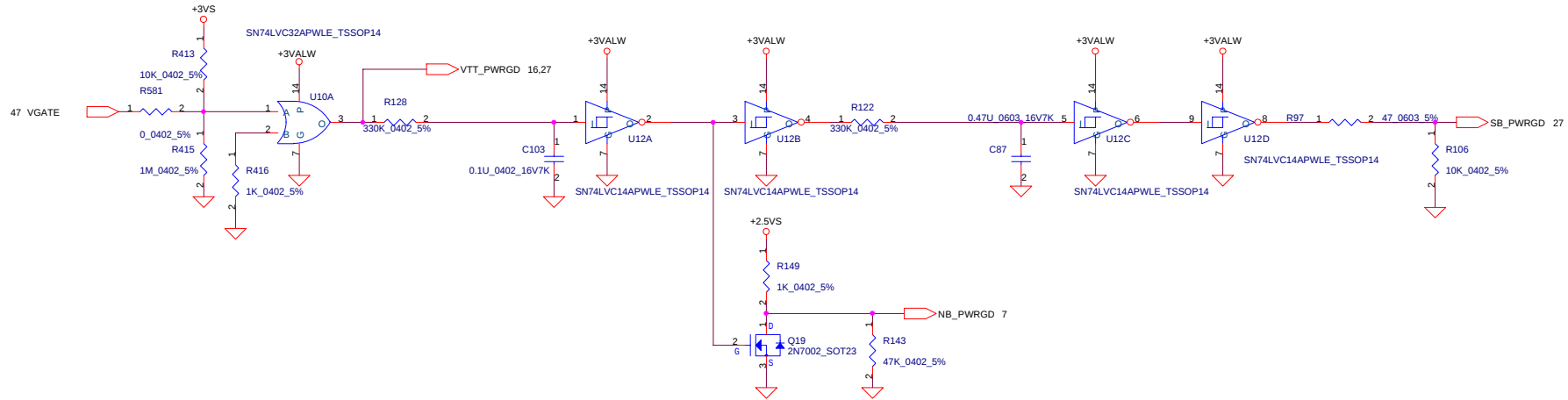
**

PCI33/66# = HIGH	66MHZ
PCI33/66# = LOW	33MHZ

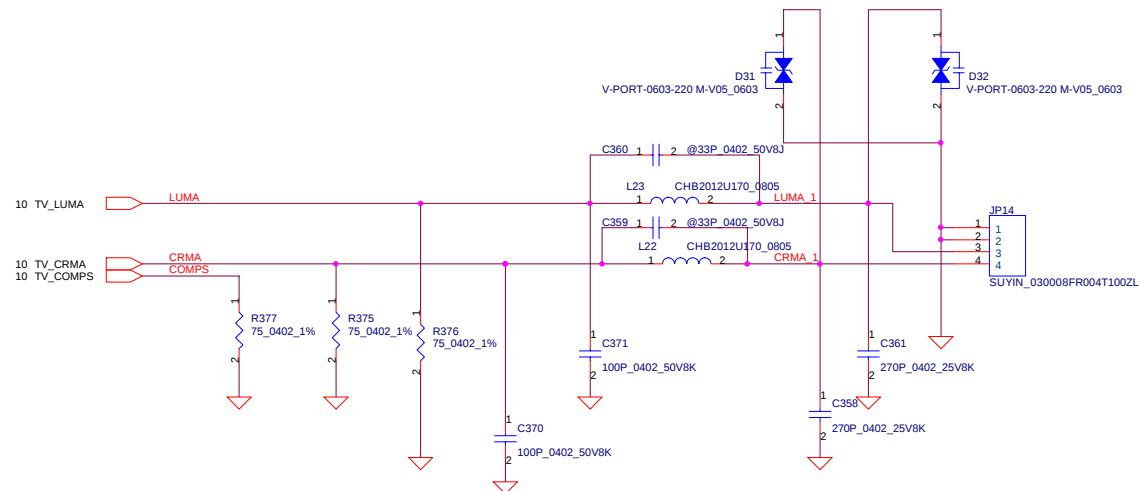


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Compal Electronics, Inc.			
Title			
Clock Generator			
Size	Document Number	Rev	
	LA-2051	0.1A	
Date:	星期三, 八月 27, 2003	Sheet	16 of 51



TV-OUT CONN.

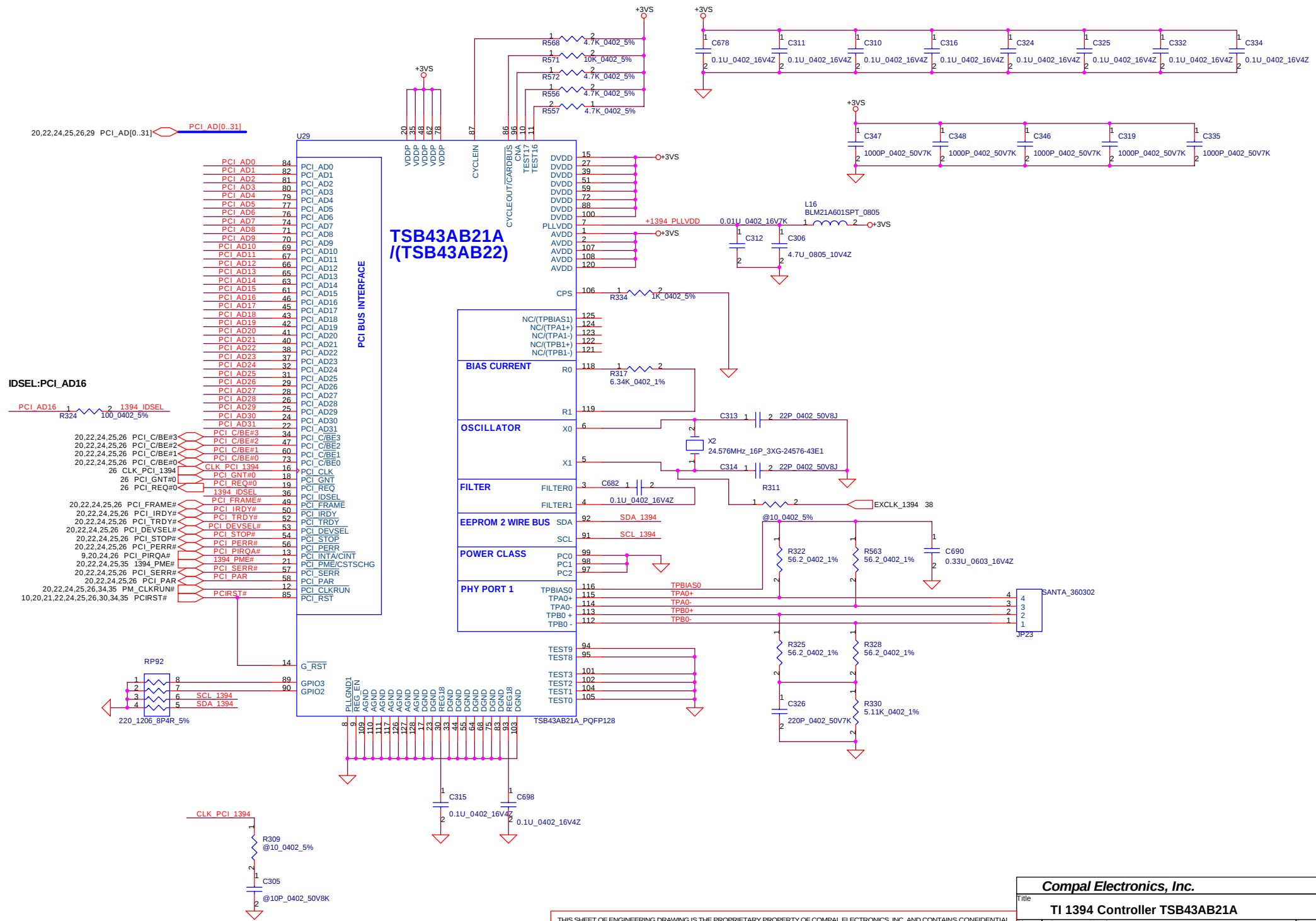


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Compal Electronics, Ltd.			
Title			
CH-7011& TV-CONN.			
Size	Document Number		Rev
Customer	LA-2051		0.1A
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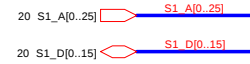
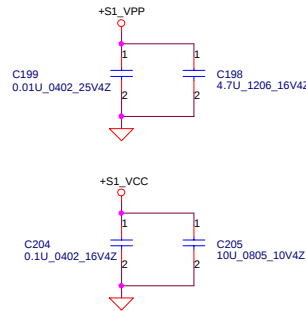
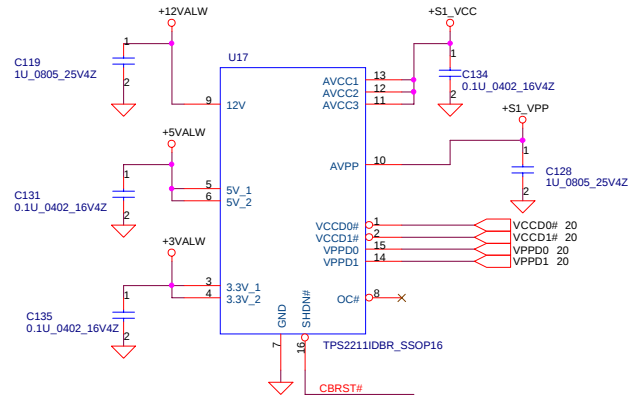
TSB43AB21A (TSB43AB22)

PCI BUS INTERFACE

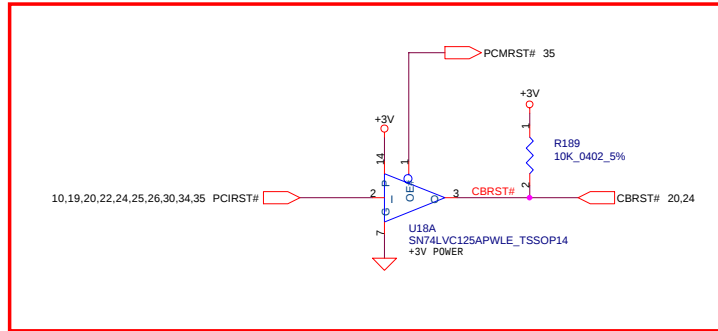
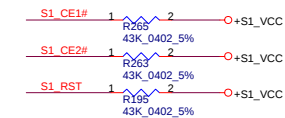
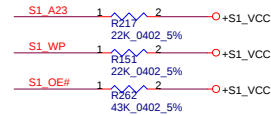
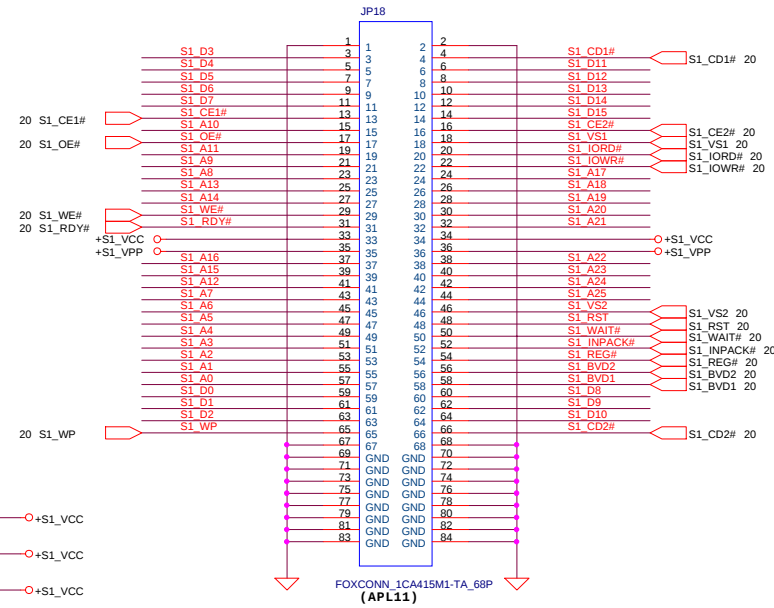


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PCMCIA Power Controller



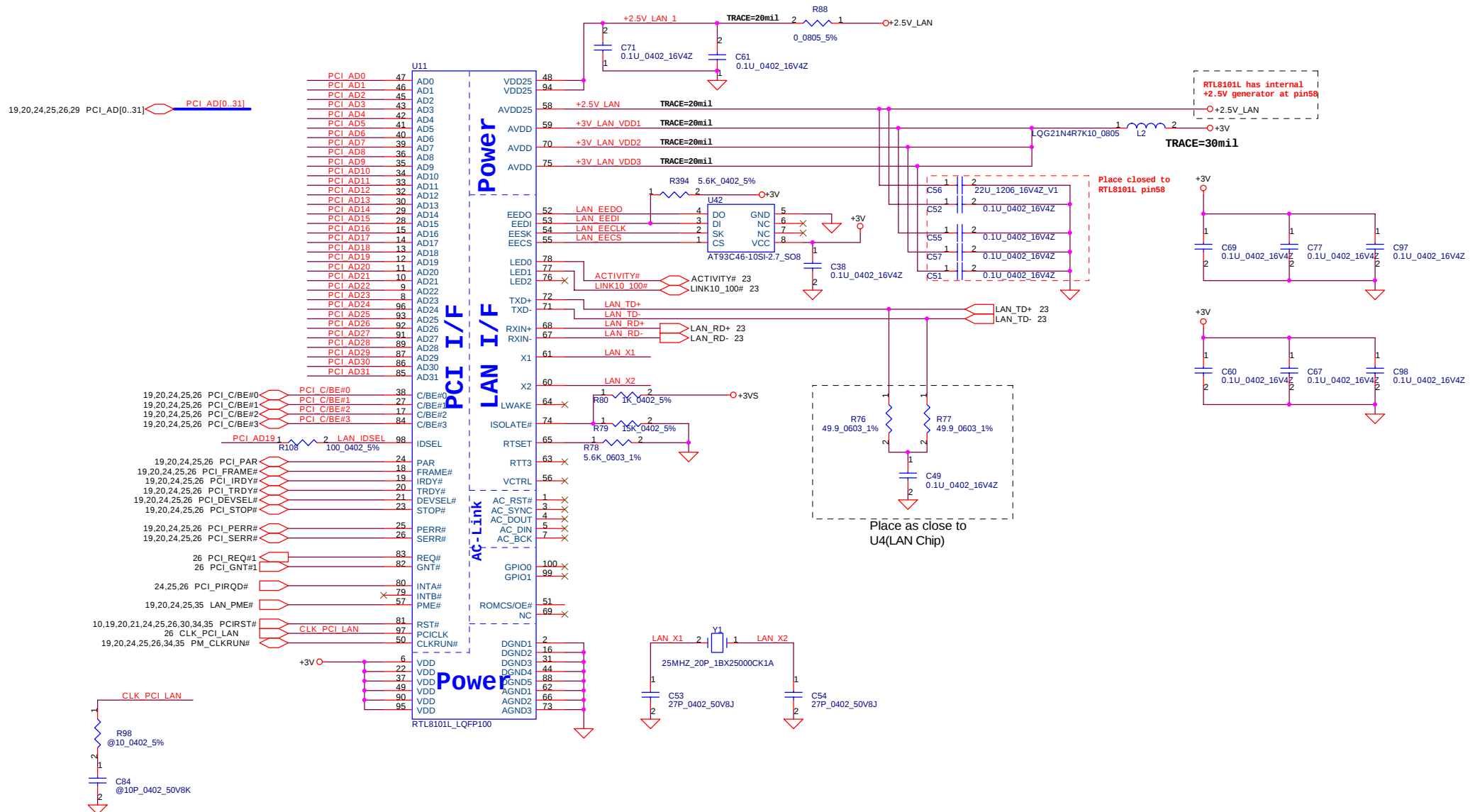
CardBus Socket



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Compal Electronics, Ltd.			
Title			
PCMCIA SOCKET			
Size	Document Number	Rev	
Cus#	LA-2051	0.1A	
Date:	星期二, 八月 27, 2003	Sheet	21 of 51

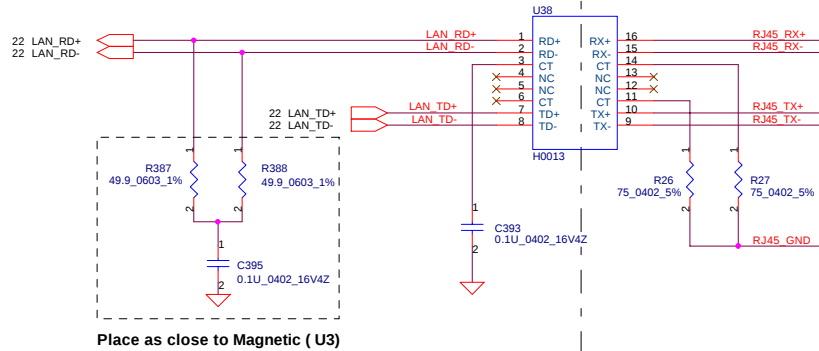
LAN AD19 REQ#1/GNT#1 PCI_PIRQD#



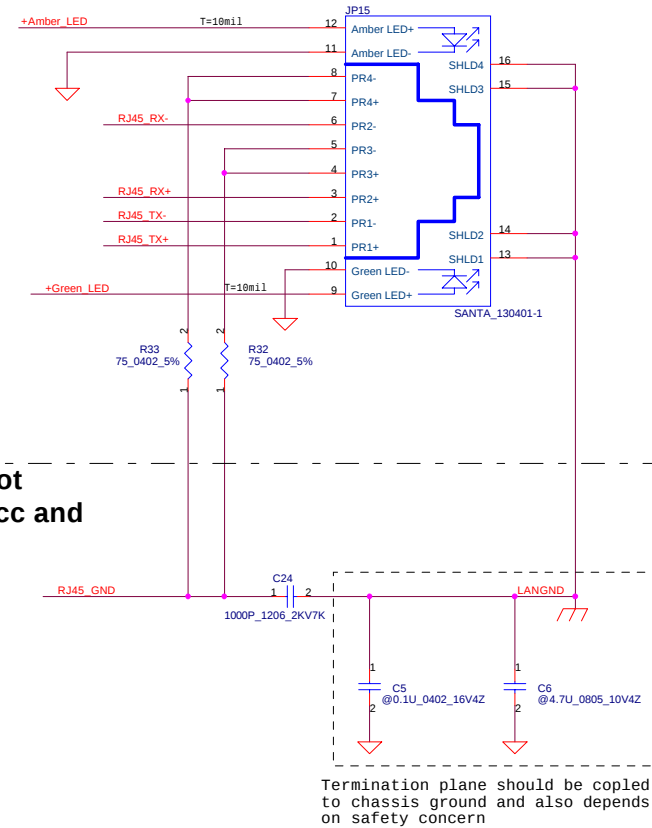
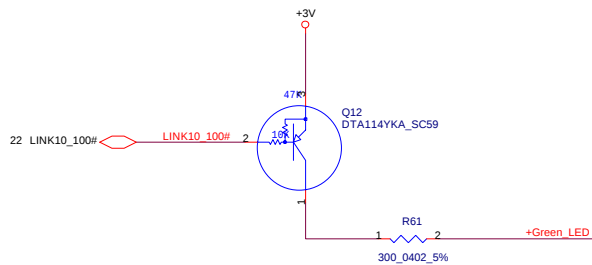
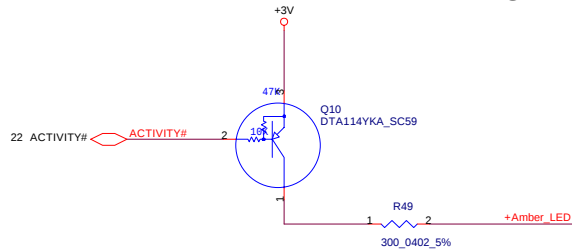
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Keep Out 40mil

Layout Note
H0013 pls close to
conn.



LAYOUT NOTICE: This area do not
connect to power plan include Vcc and
GND in any layer

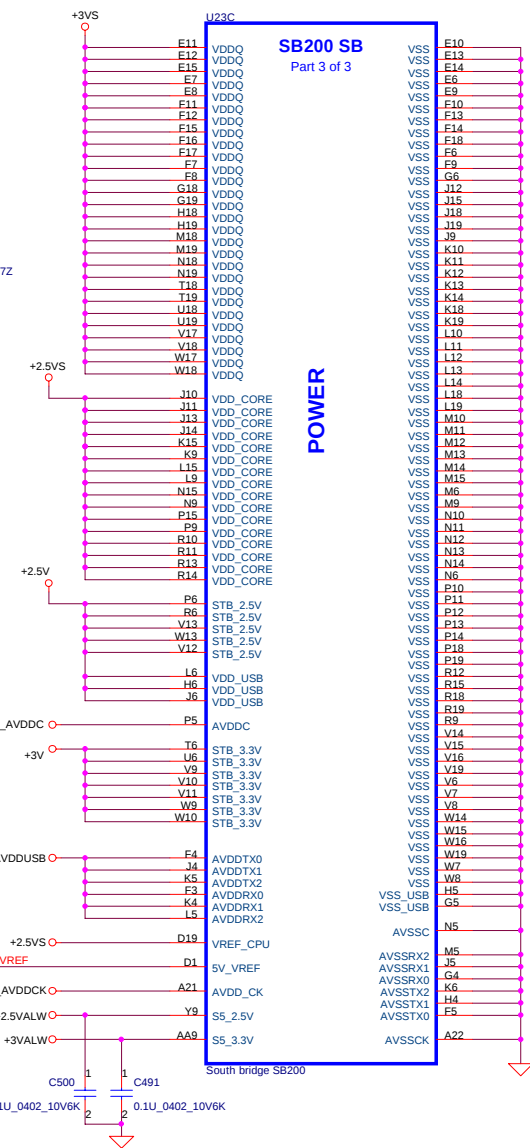
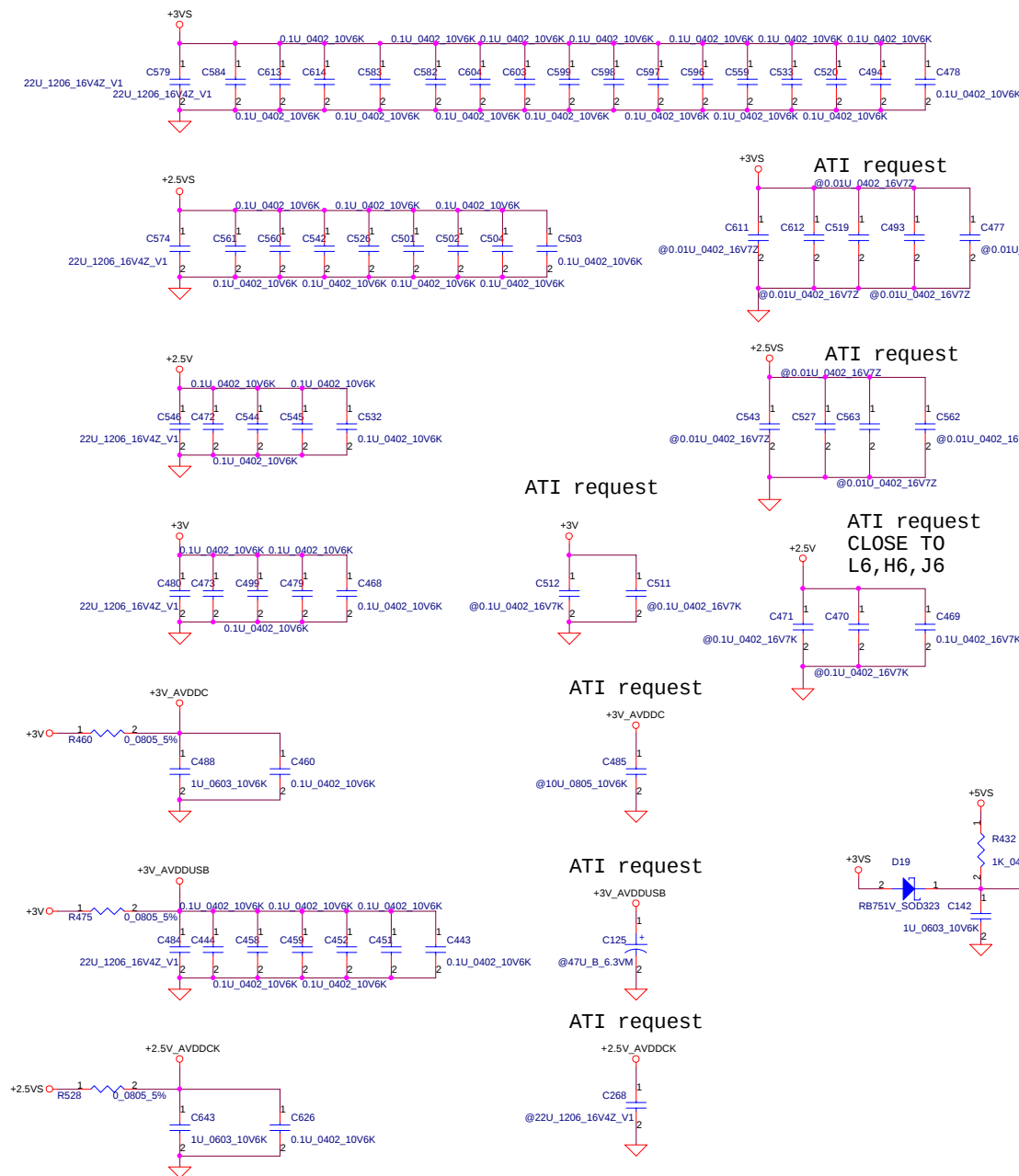


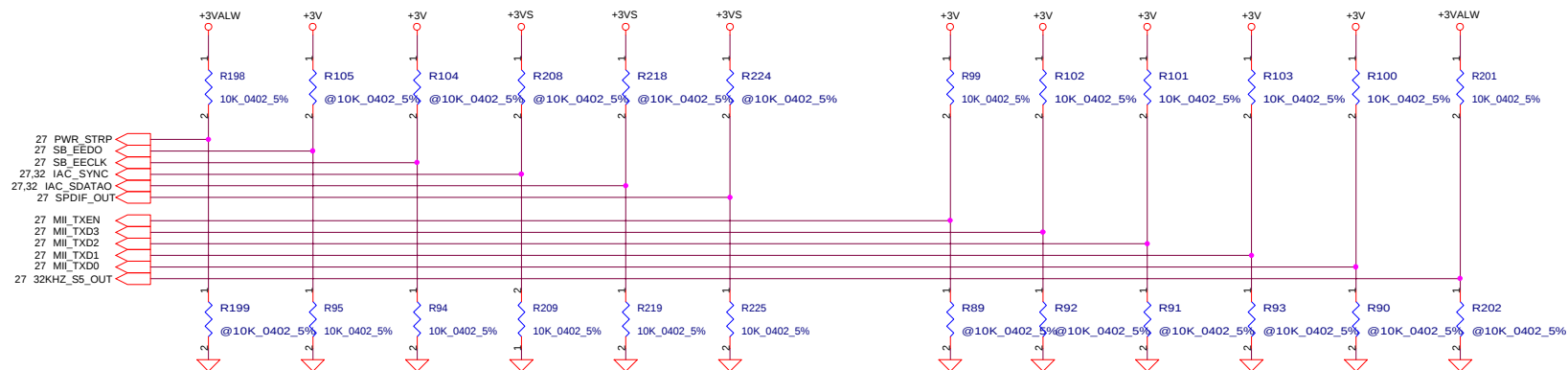
Compal Electronics, Ltd.

RJ11/RJ45 Connector

Title	Document Number	Rev
Size	LA-2051	0.1A
Date	星期三, 八月 27, 2003	Sheet 23 of 51

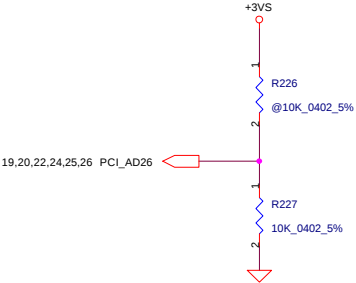
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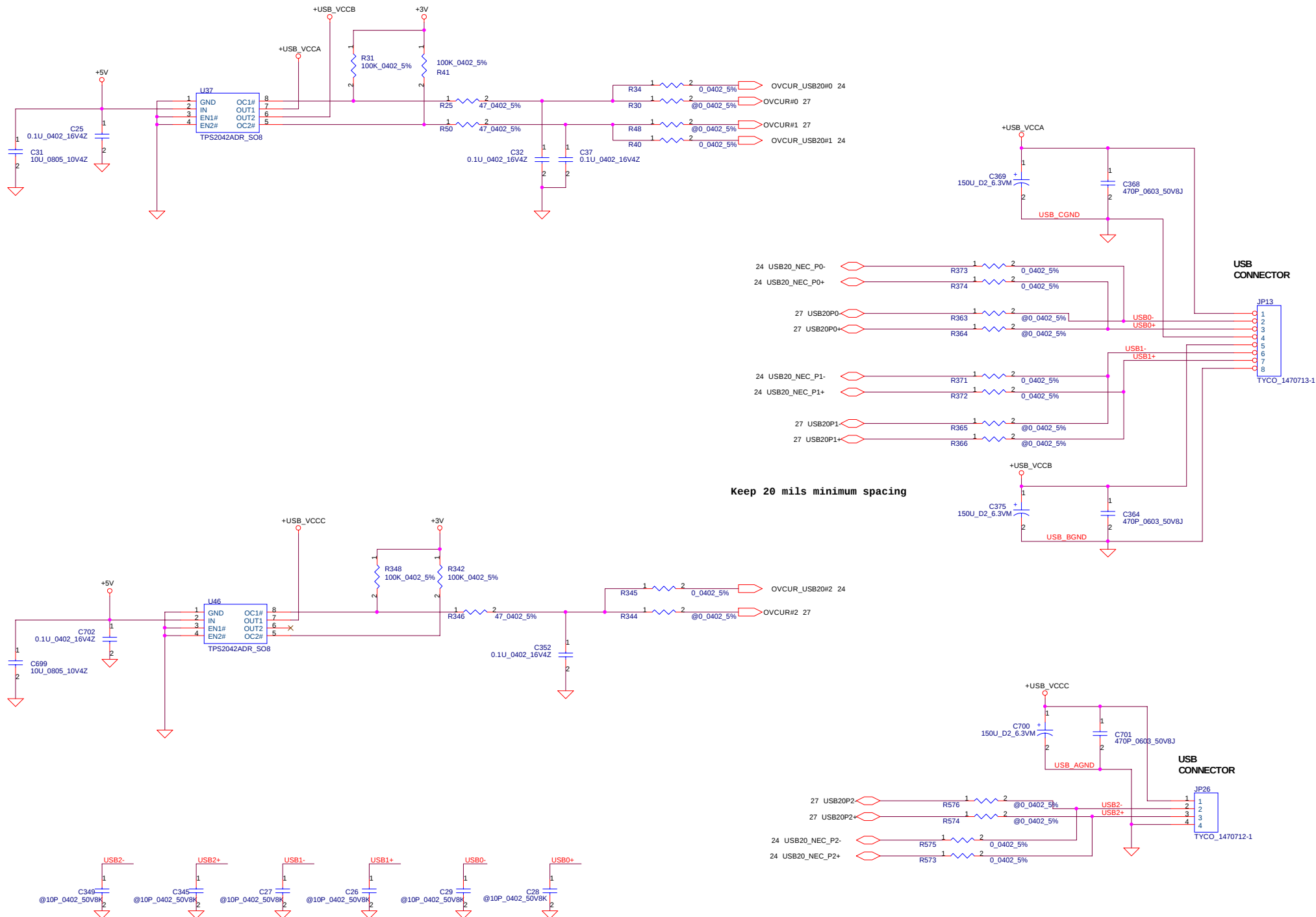


REQUIRED SYSTEM STRAPS

	PWR_STRP	IGN DEBUG EEDO	EECK	AC_SYNC	AC_SDOUT	SPDIF_OUT	SPEEDSTEP CPU_STP#	FREQLTCH TX_EN	ETHERNET TXD[3:0]	32KHZ_S5
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	ROM ON PCI BUS	INIT ACTIVE HIGH	33MHz NB BUS	SIO 24MHz	ENABLE SPEED STEP	DISABLE CPU FREQ SETTING DEFAULT	PROCESSOR FREQ MULTIPLIER	32KHZ OUTPUT FROM SB200 (INT RTC) DEFAULT
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	ROM ON LPC BUS DEFAULT	INIT ACTIVE LOW (PIII) DEFAULT	HI SPEED A-LINK DEFAULT	SIO 48MHz DEFAULT	DISABLE SPEED STEP DEFAULT	ENABLE CPU FREQSETTING		32KHZ INPUT TO SB200 (EXT RTC)



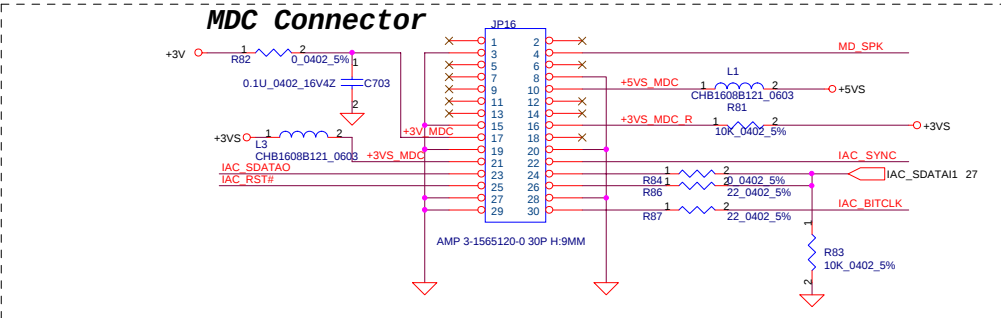
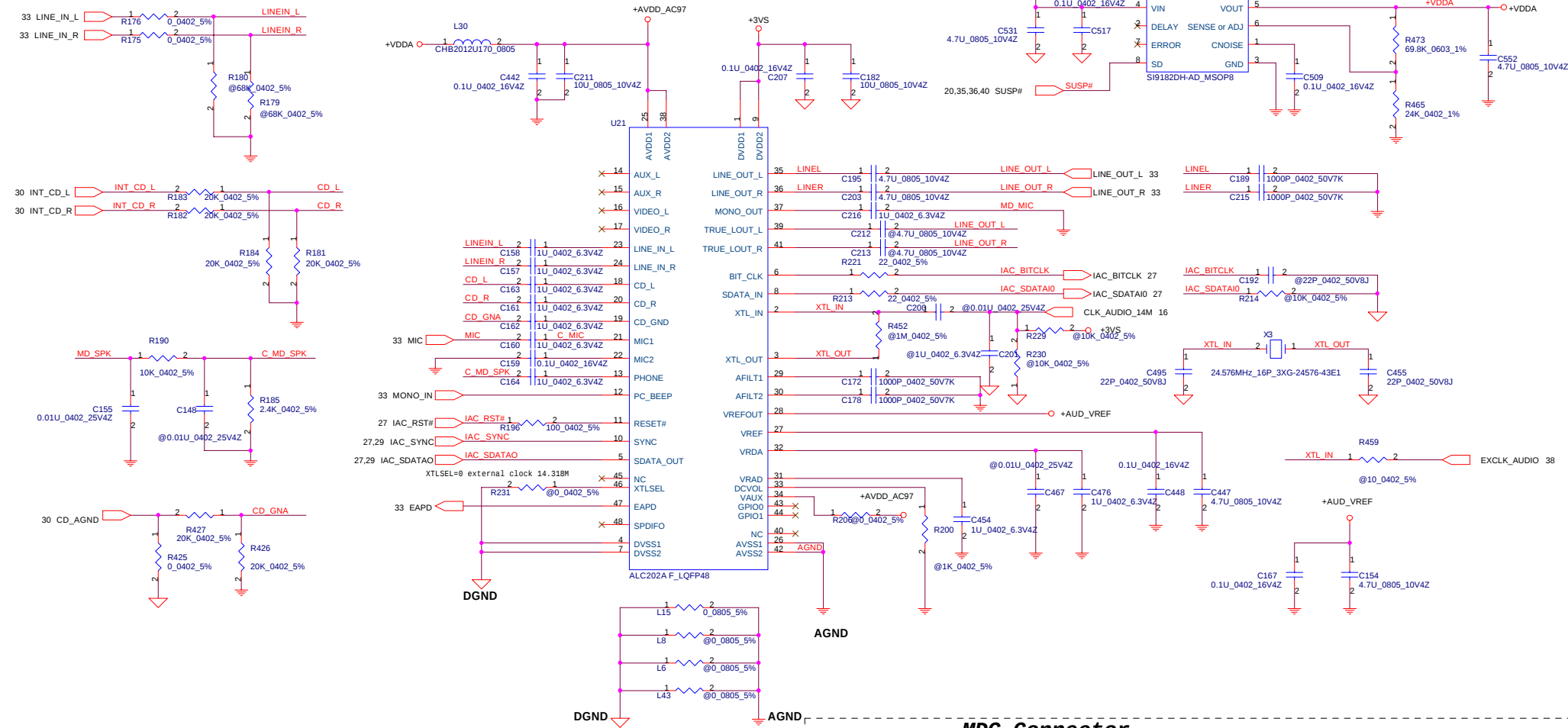
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Compal Electronics, Ltd.			
Title			
USB & Bluetooth			
Size	Document Number		Rev
Cuspart	LA-2051		0.1A
Date:	星期三, 八月 27, 2003		Sheet 31 of 51

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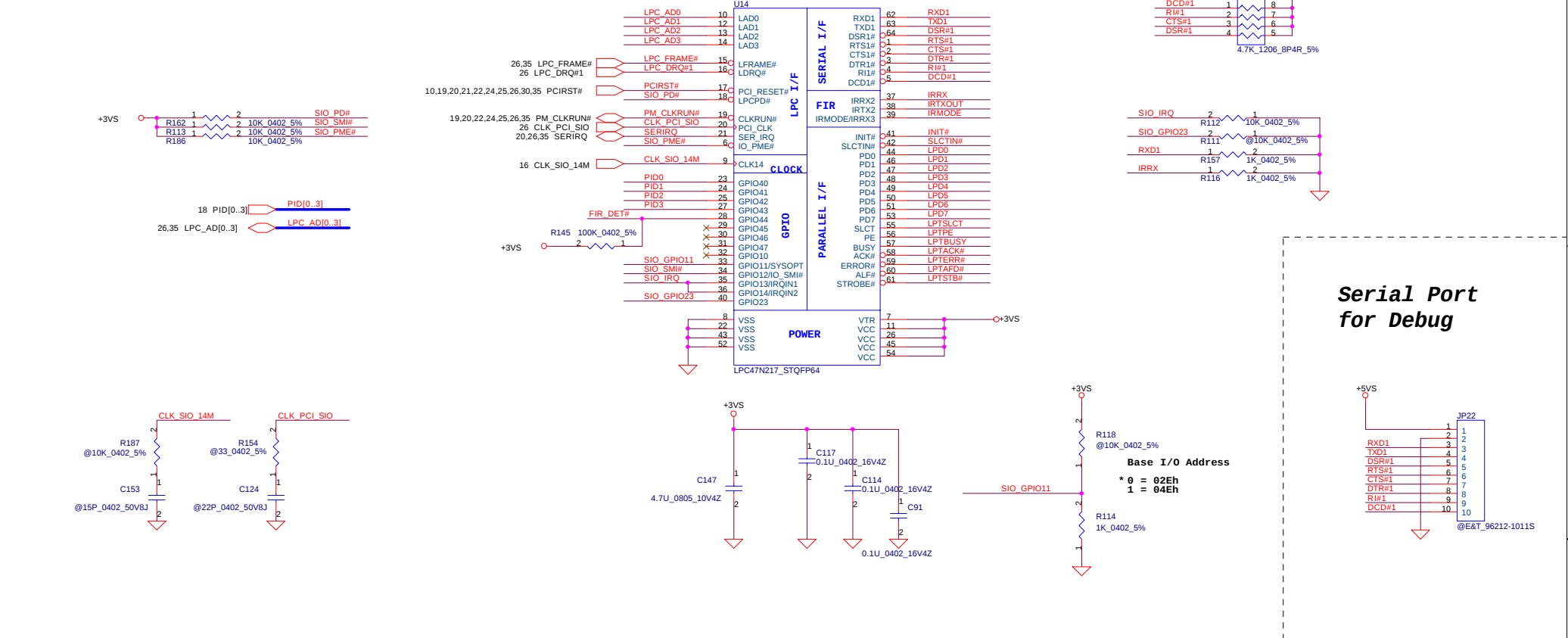
AC97 Codec



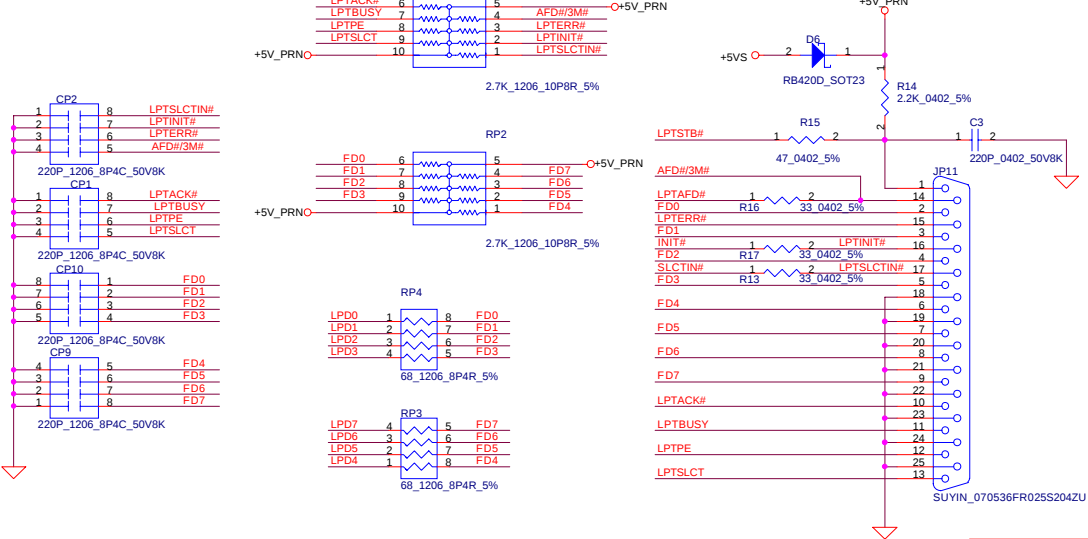
Compal Electronics, Ltd.			
Title			
AC97 Codec ALC202			
Size	Document Number	Rev	
Custom	LA-2051	0.1A	
Date:	星期三, 八月 27, 2003	Sheet	32 of 51

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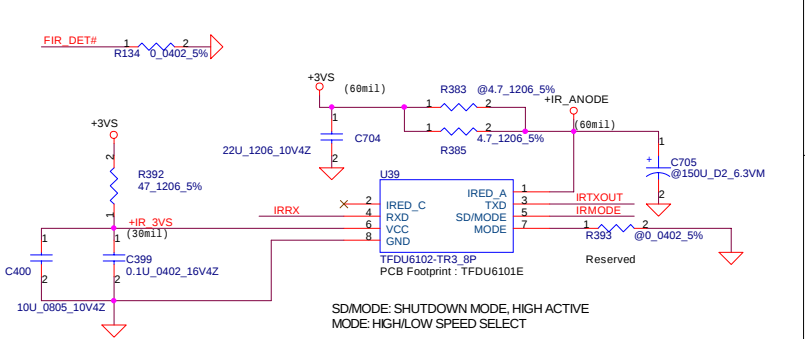
SUPER I/O SMsC LPC47N217



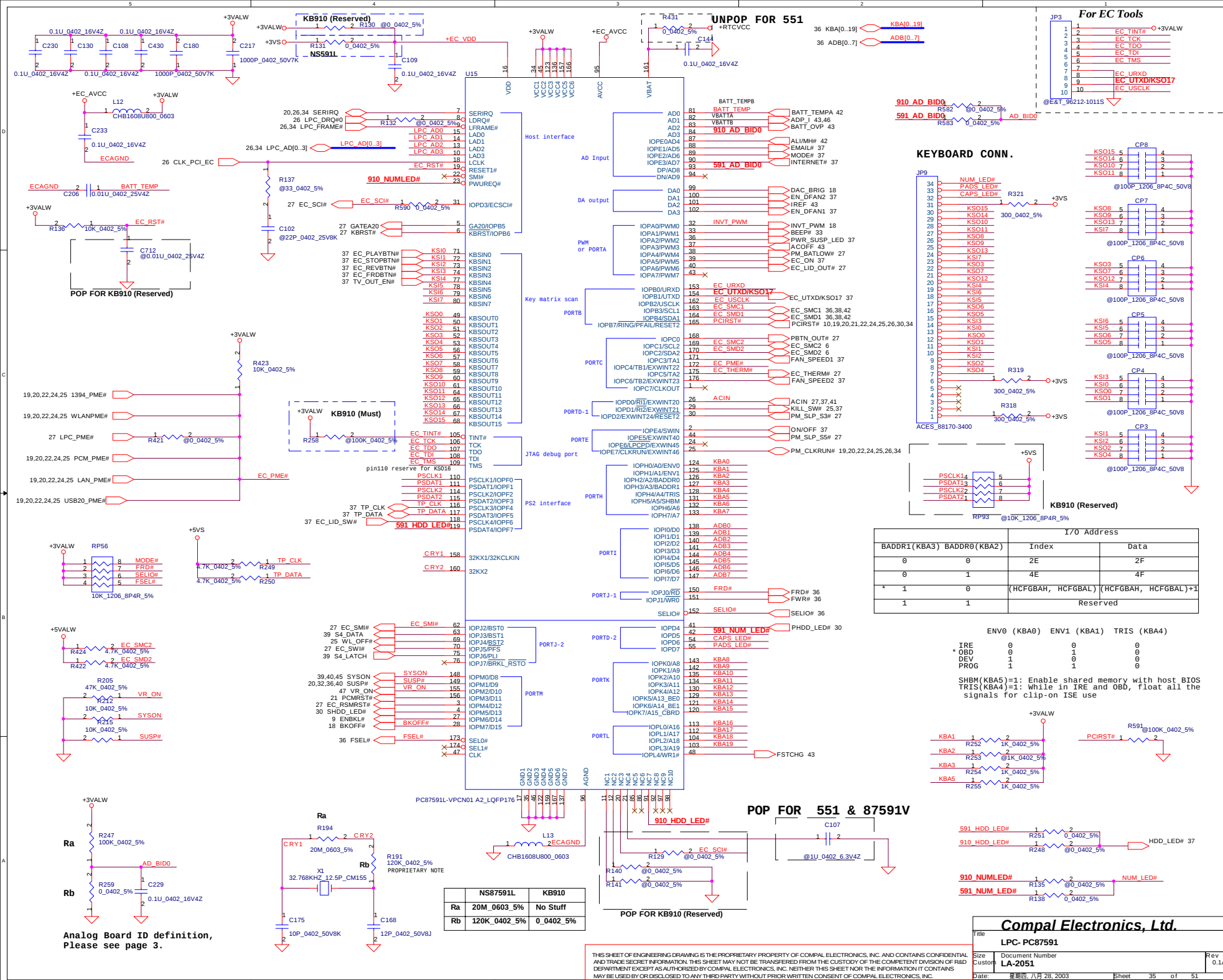
Parallel Port

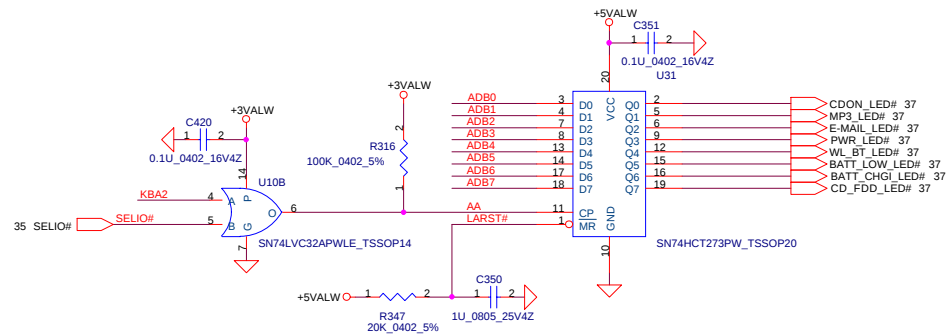


FIR Module

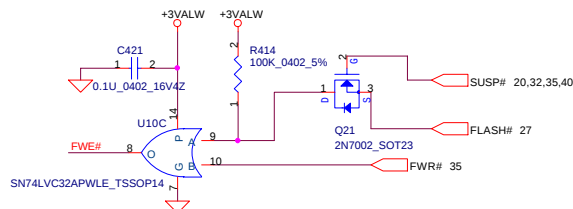


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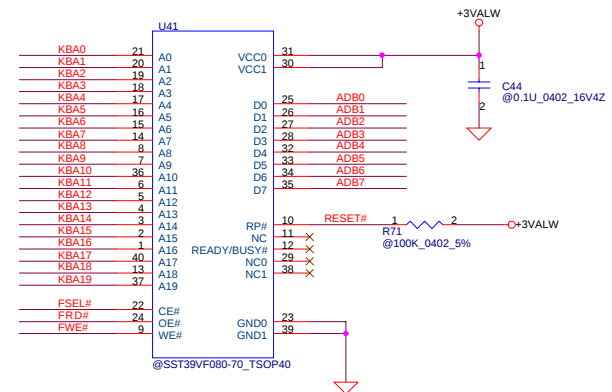
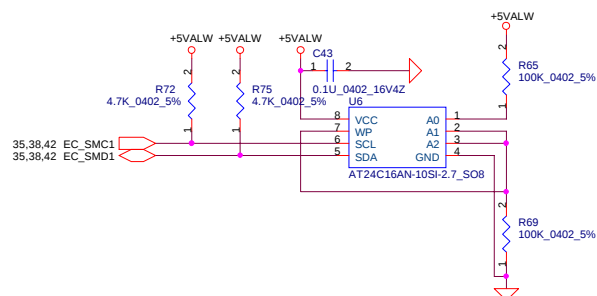
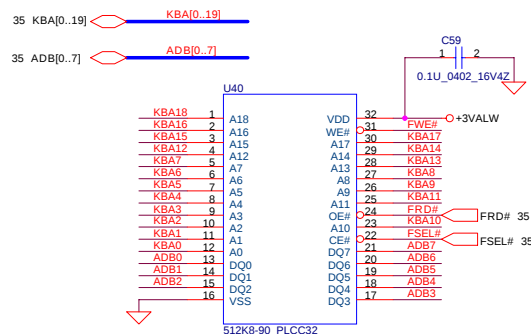




System BIOS



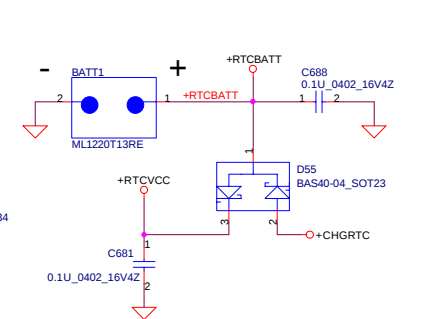
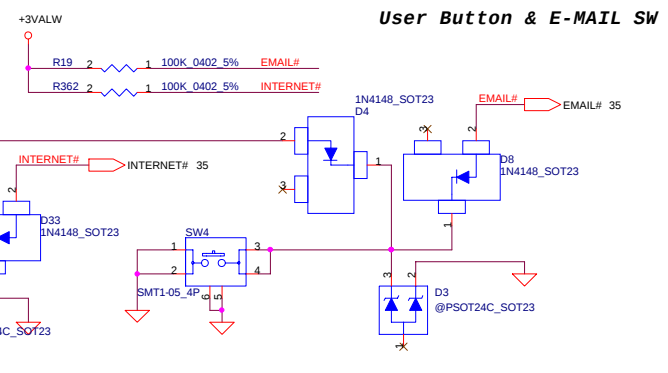
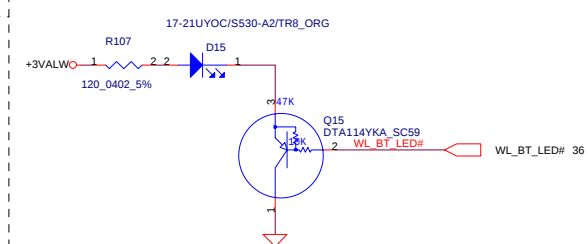
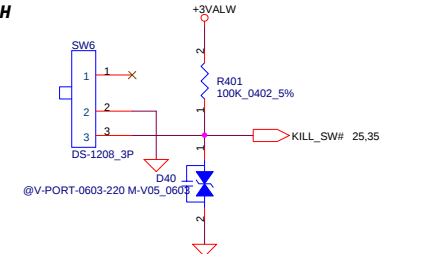
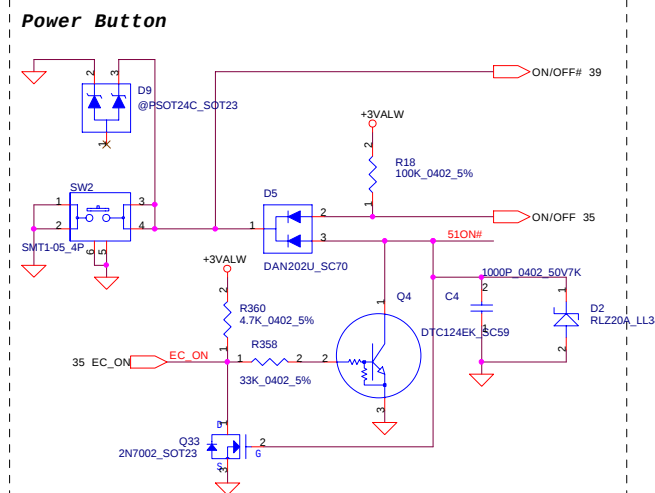
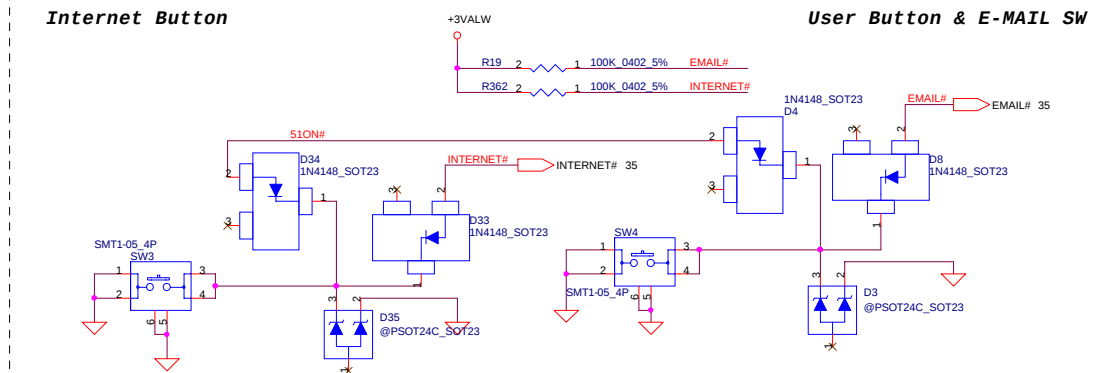
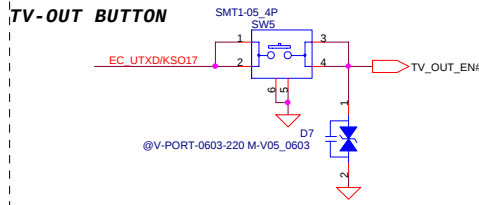
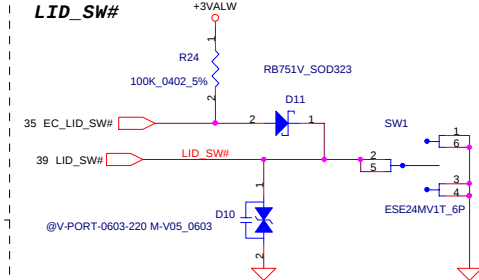
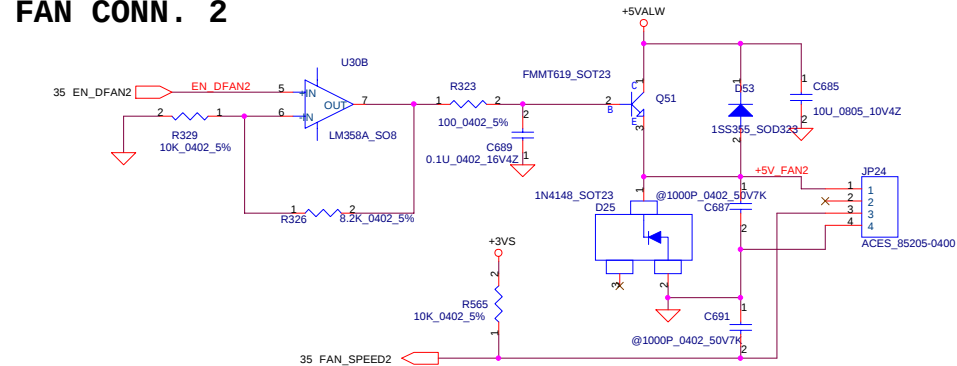
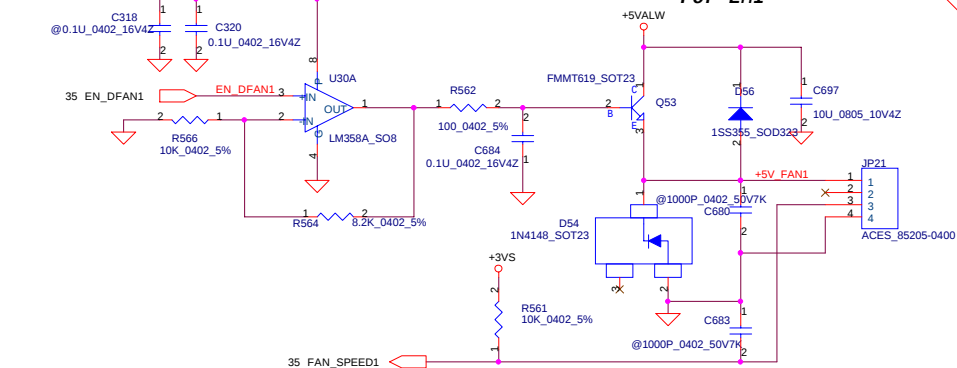
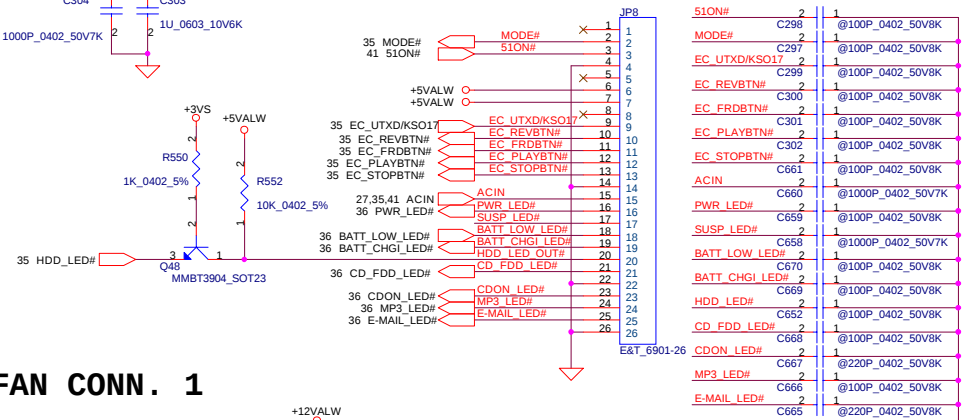
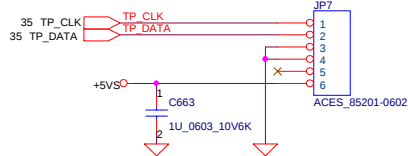
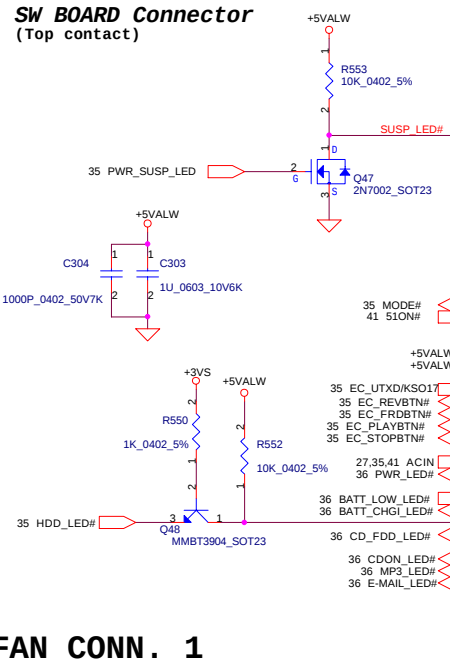
SMBus EEPROM



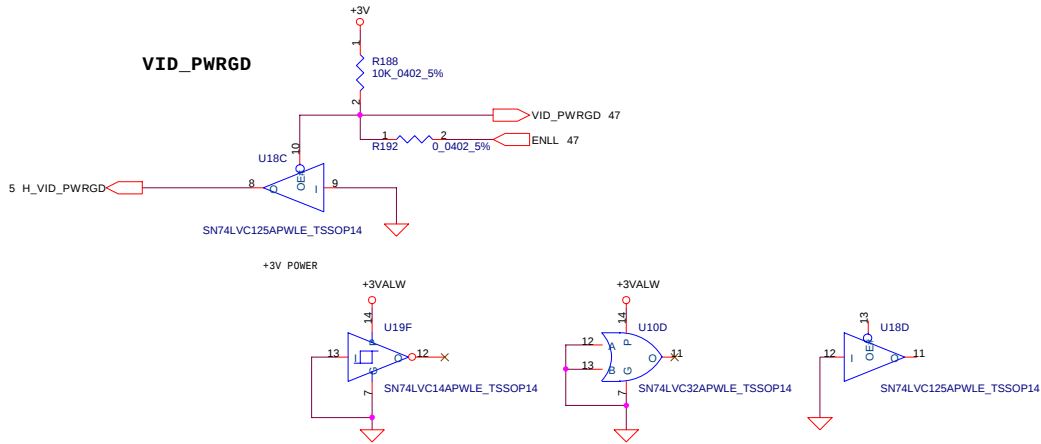
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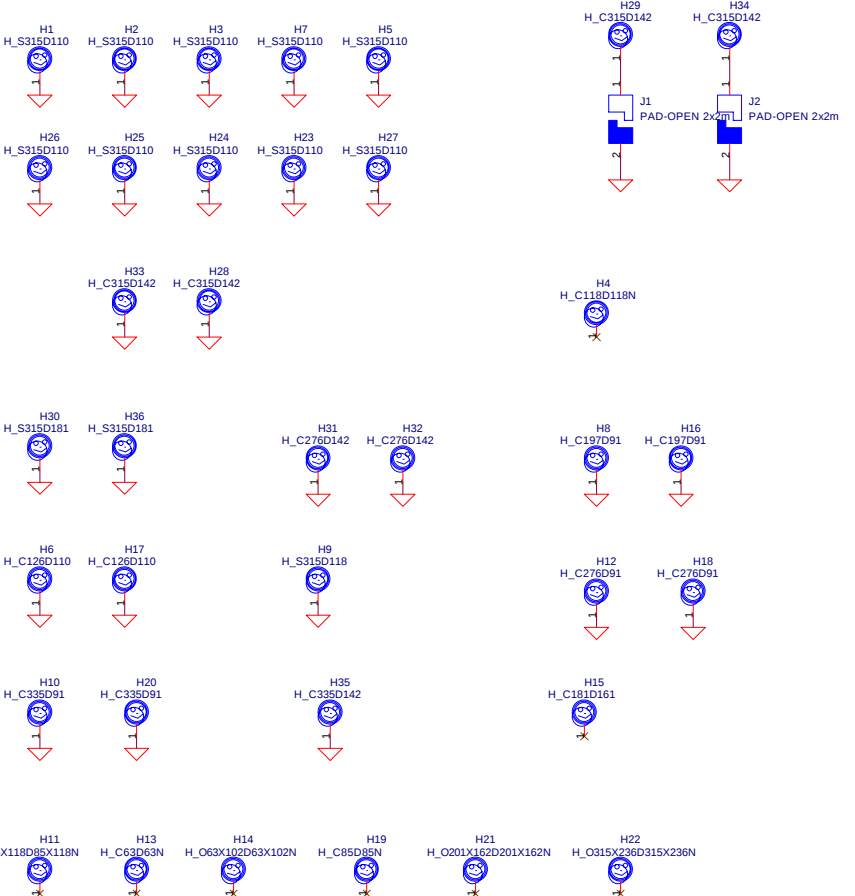
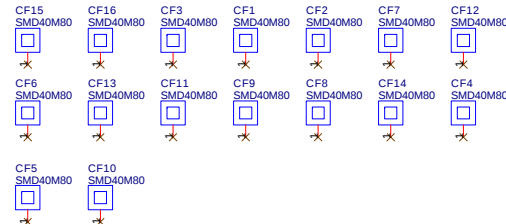
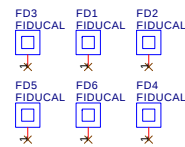
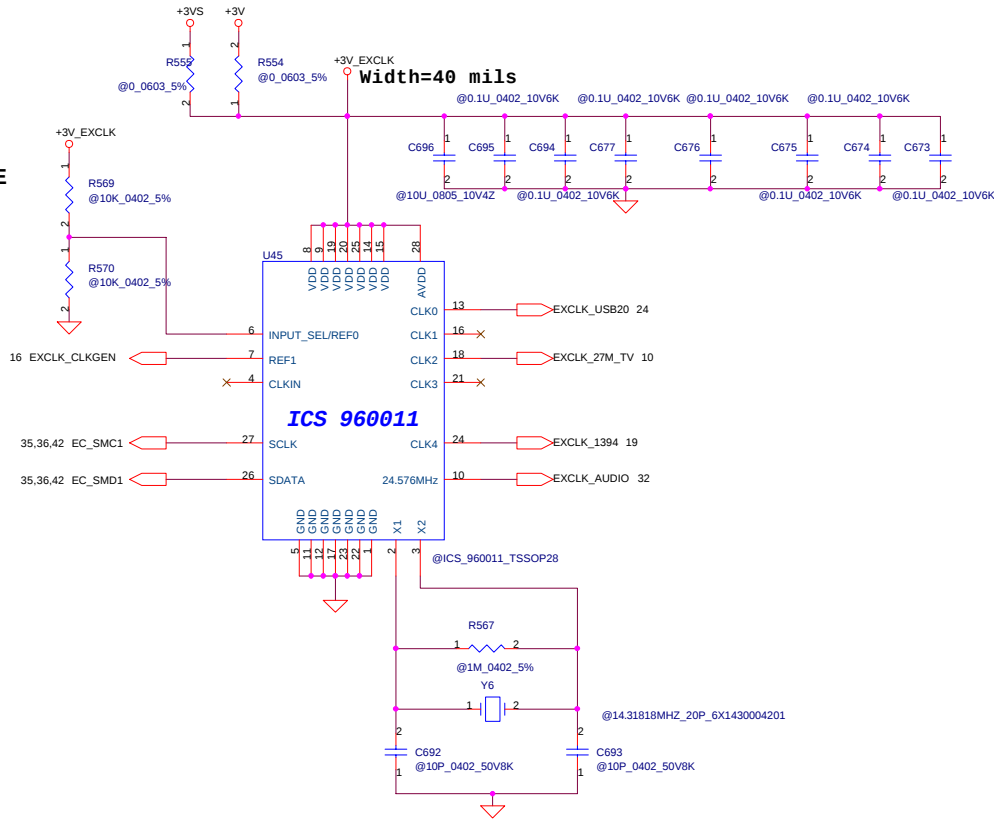
Title			
BIOS & Ext.I/O			
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VID_PWRGD

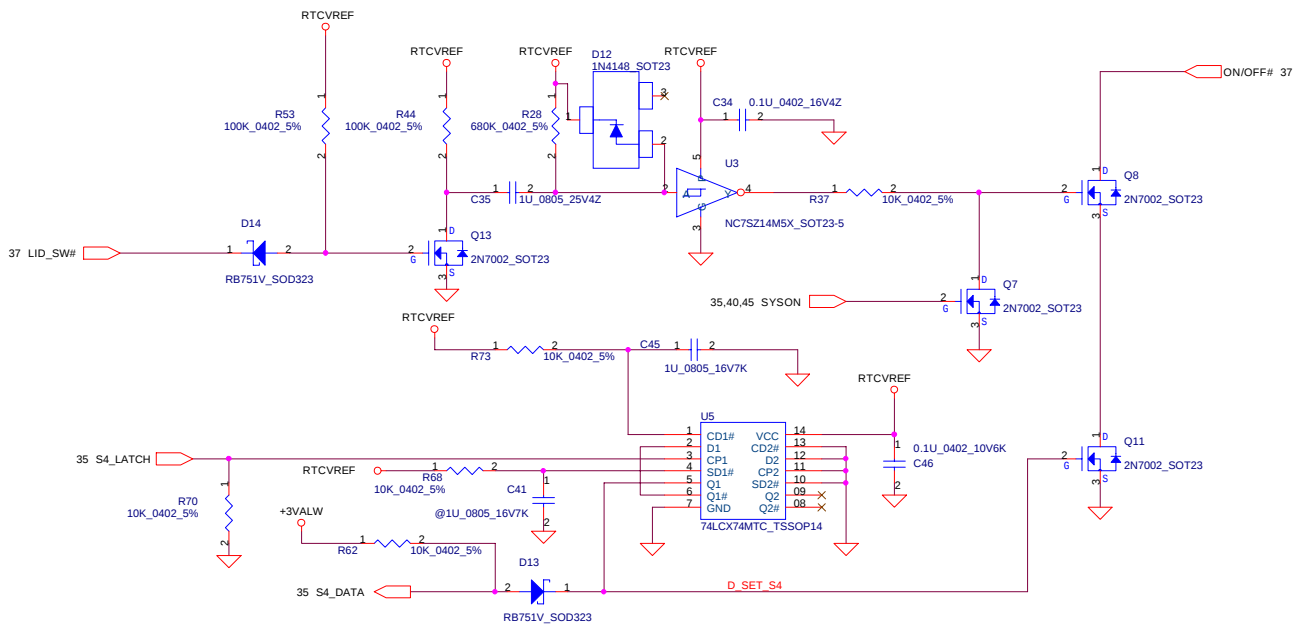


SS ENABLE
HIGH: ?
LOW: ?



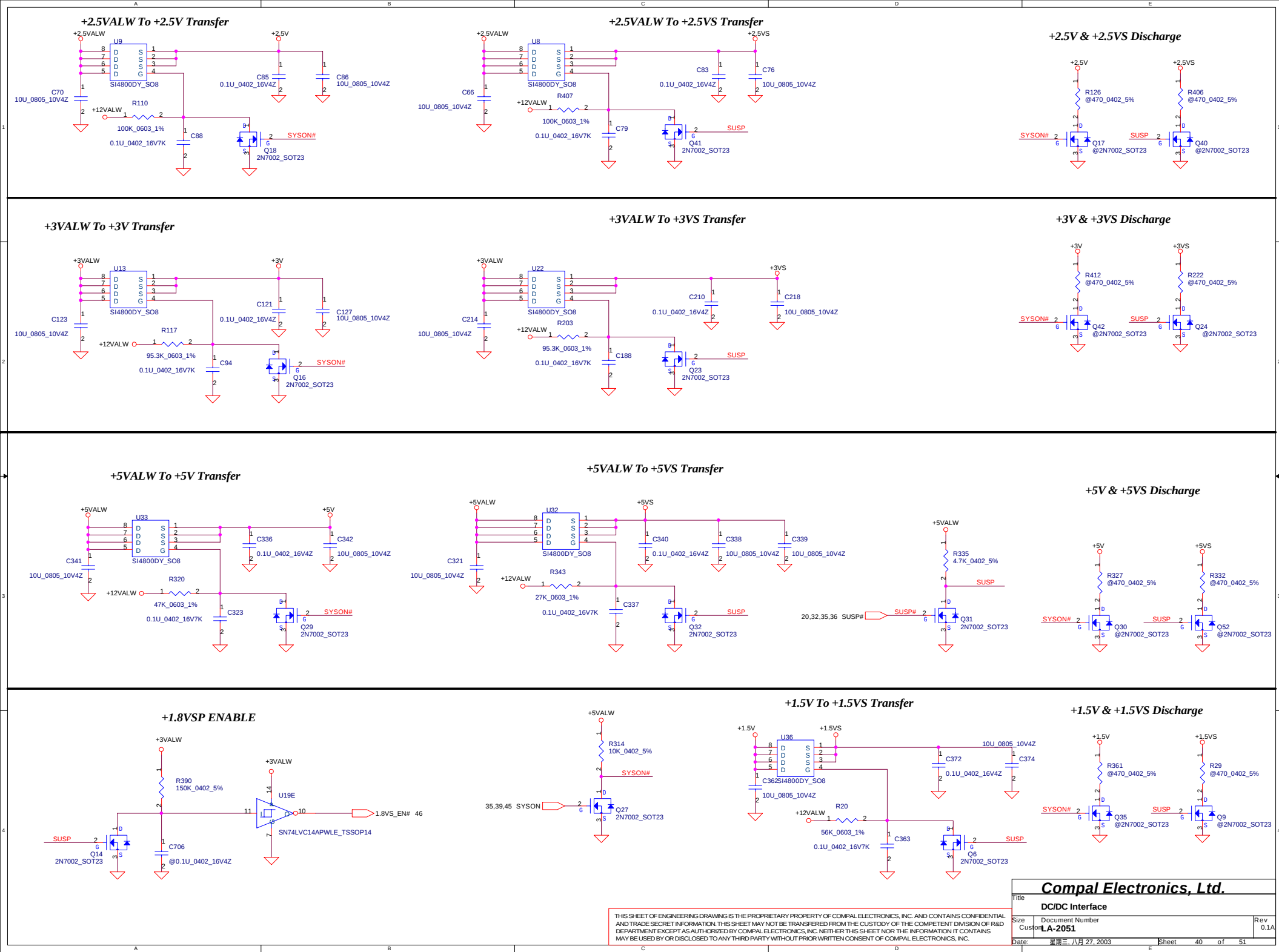
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Compal Electronics, Ltd.			
Title			
PowerGood			
Size	Document Number	Rev	
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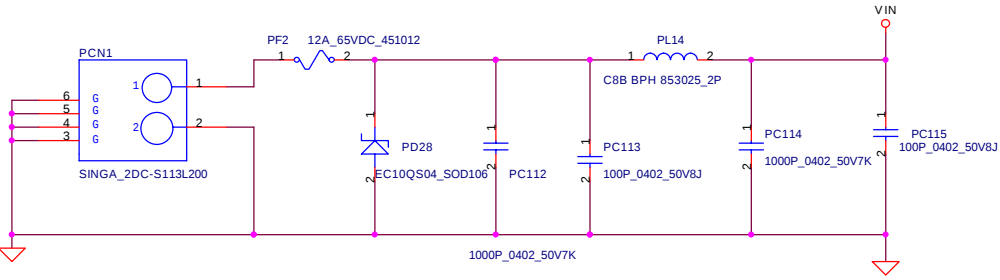
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Compal Electronics, Ltd.			
Title			
BATT-Mode-Hibernation			
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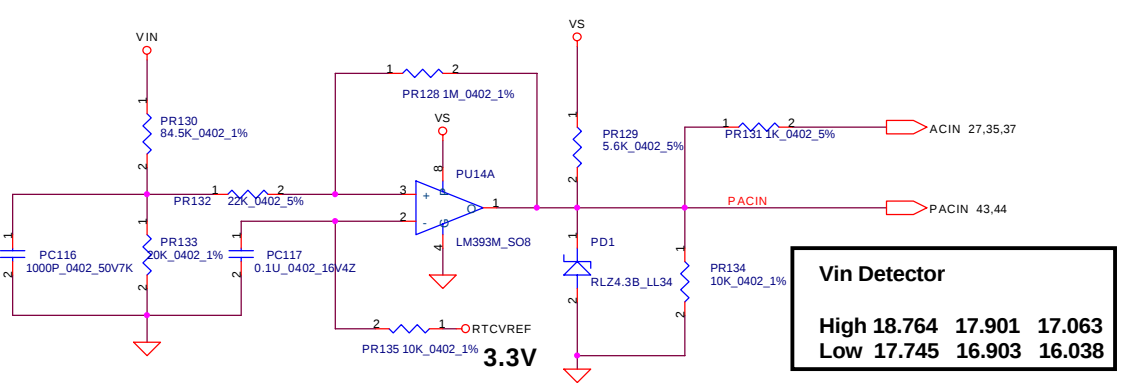


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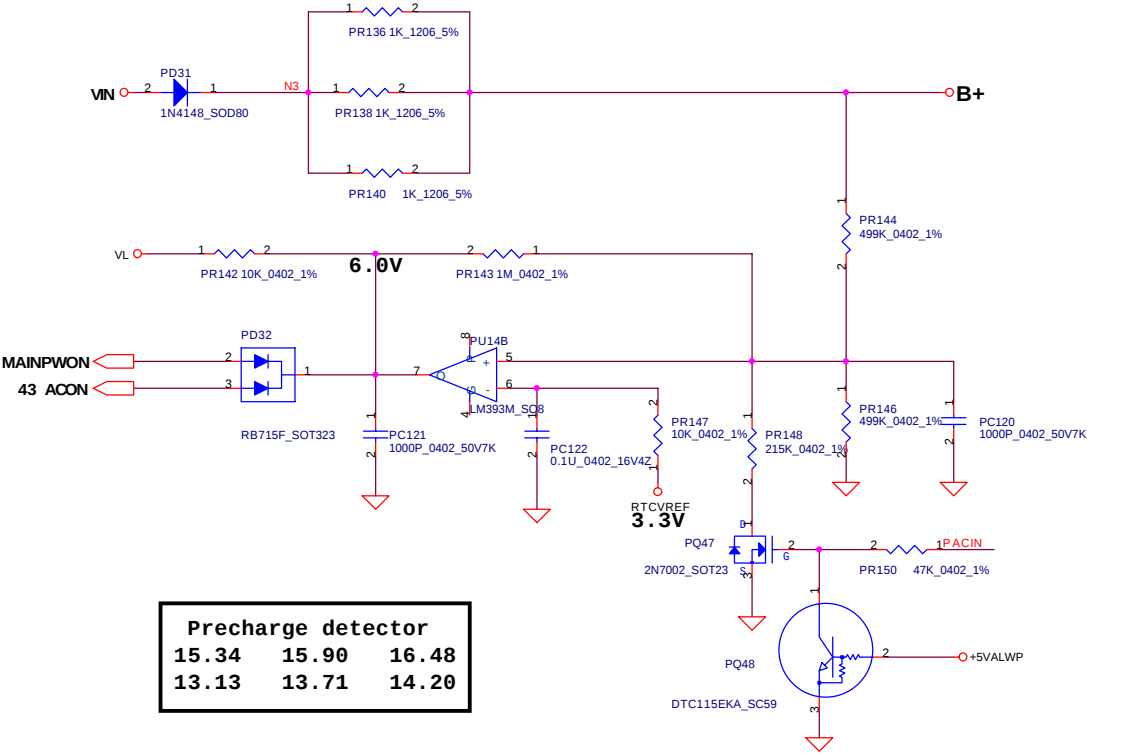
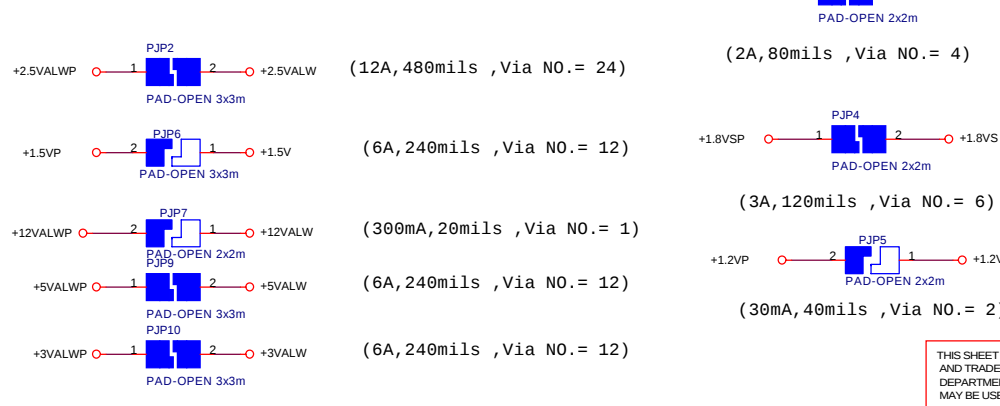
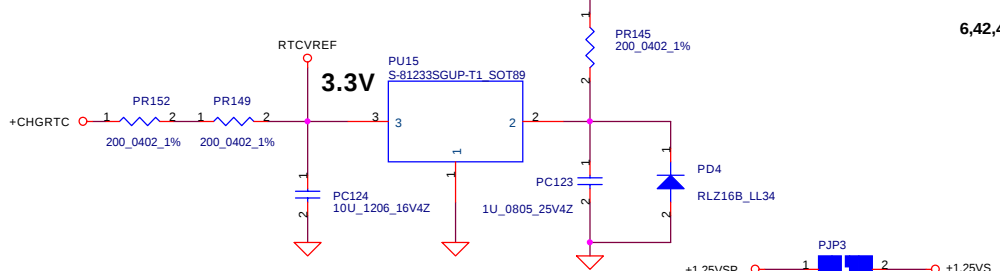
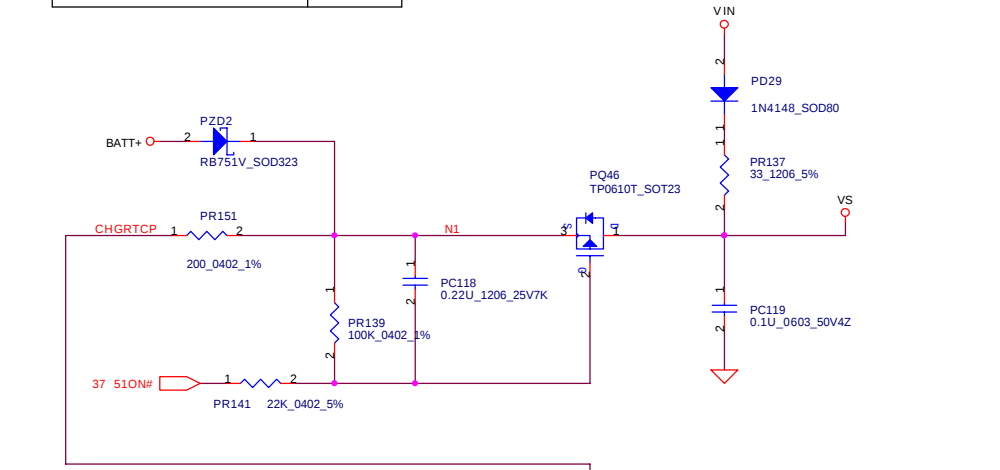
Compal Electronics, Ltd.			
DC/DC Interface			
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SINGA_2DC-S133L200	120W
SINGA_2DC-S726B201	90W

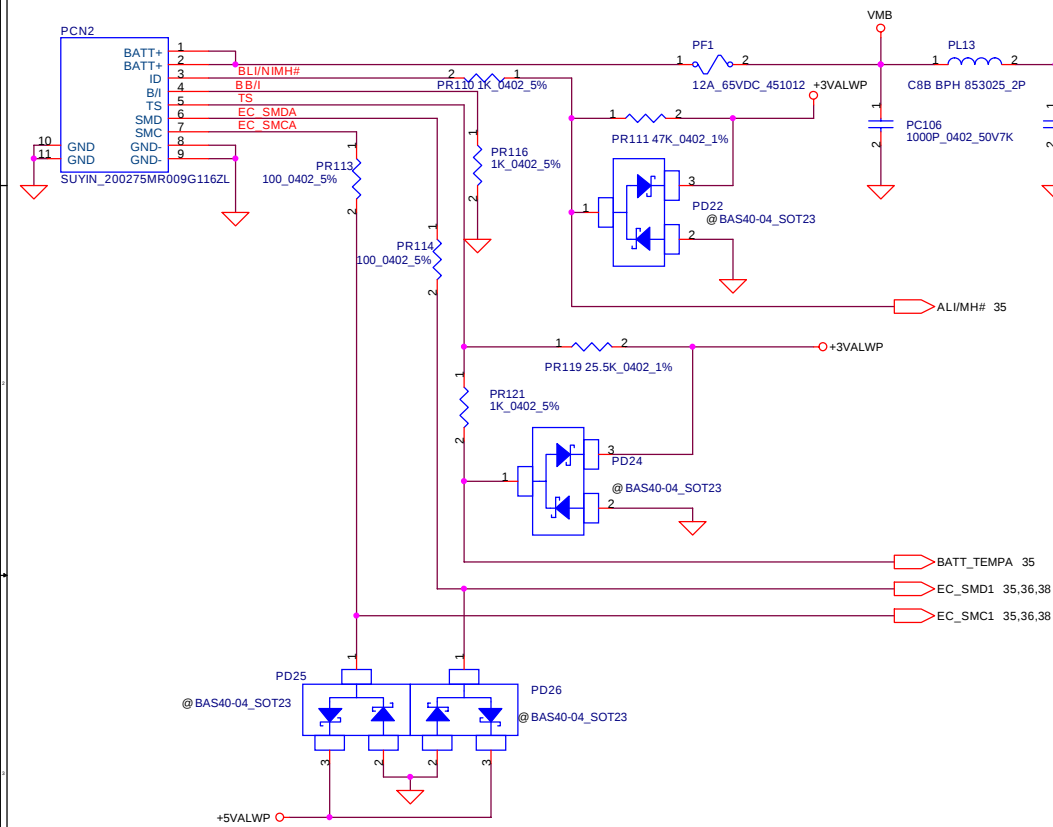


Vin Detector			
High	18.764	17.901	17.063
Low	17.745	16.903	16.038

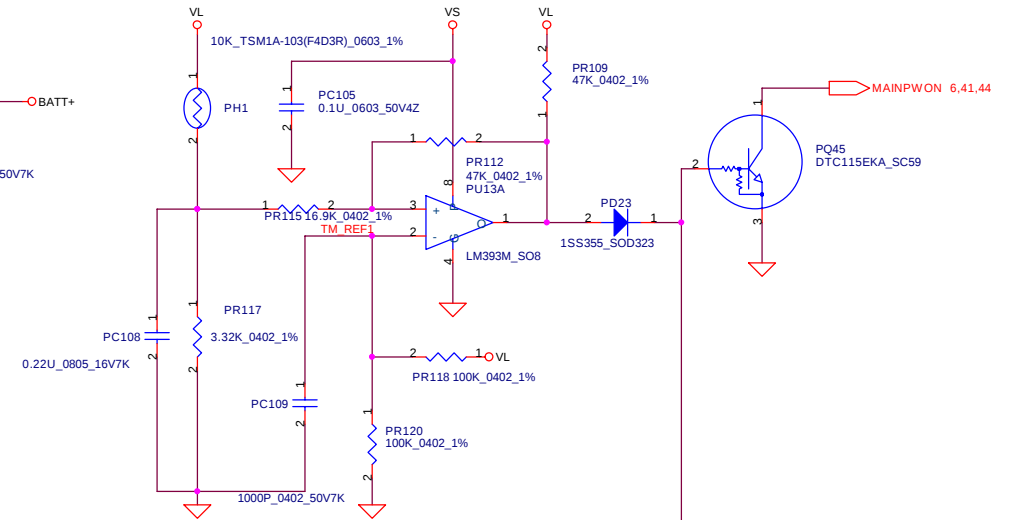


Precharge detector		
15.34	15.90	16.48
13.13	13.71	14.20

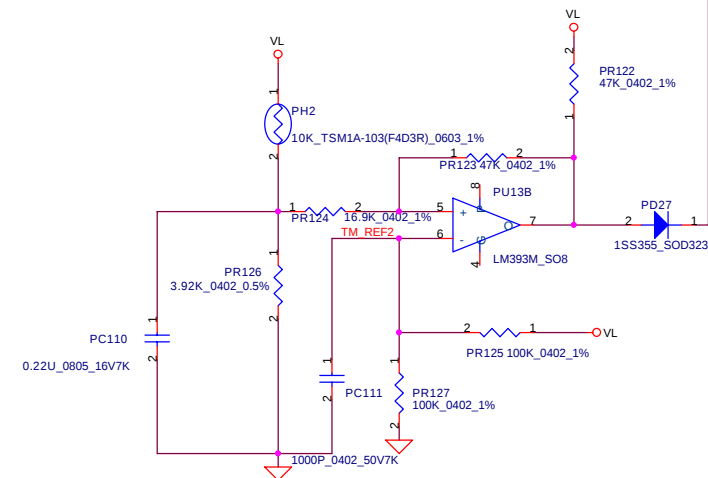
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PH1 under CPU bottom side :
CPU thermal protection at 84 degree C
Recovery at 44(45) degree C



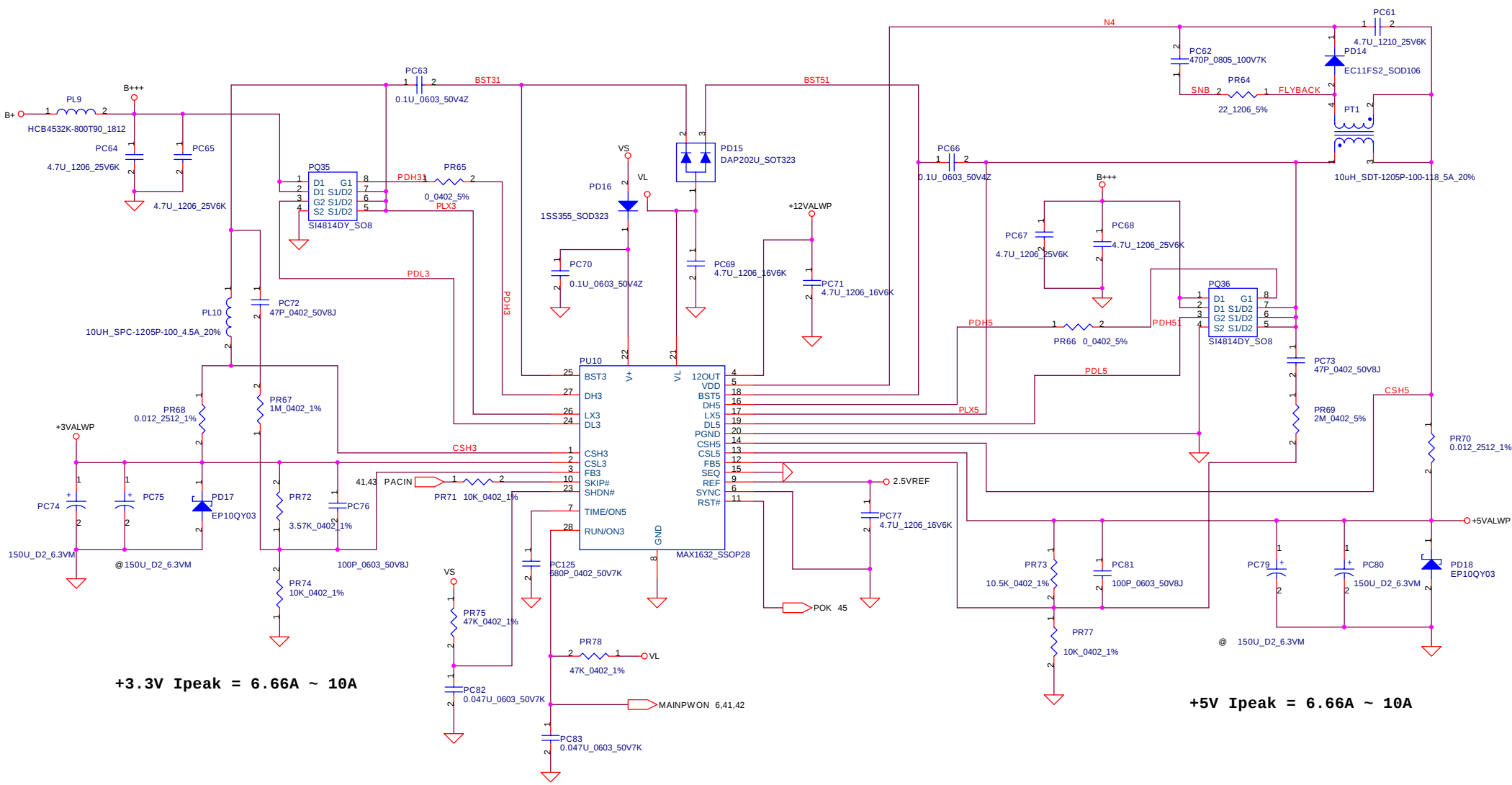
PH2 near main Battery CONN :
BAT. thermal protection at 78 degree C
Recovery at 39(40) degree C



Compal Electronics, Ltd.

Title			
BATTERY CONN / OTP			
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+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

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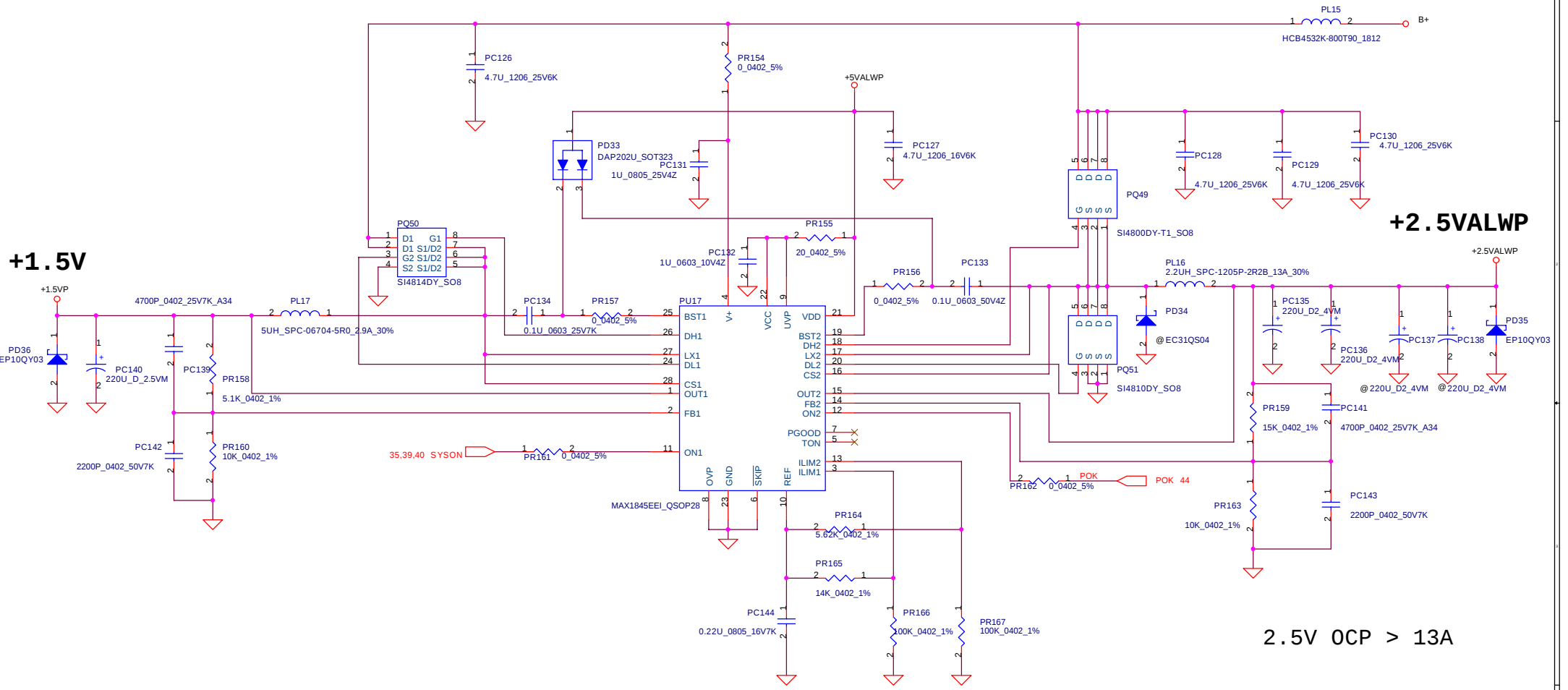
Compal Electronics, Ltd.			
Title			
5V/3V/12V			
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+2.5VALWP/+1.5VP

+1.5V

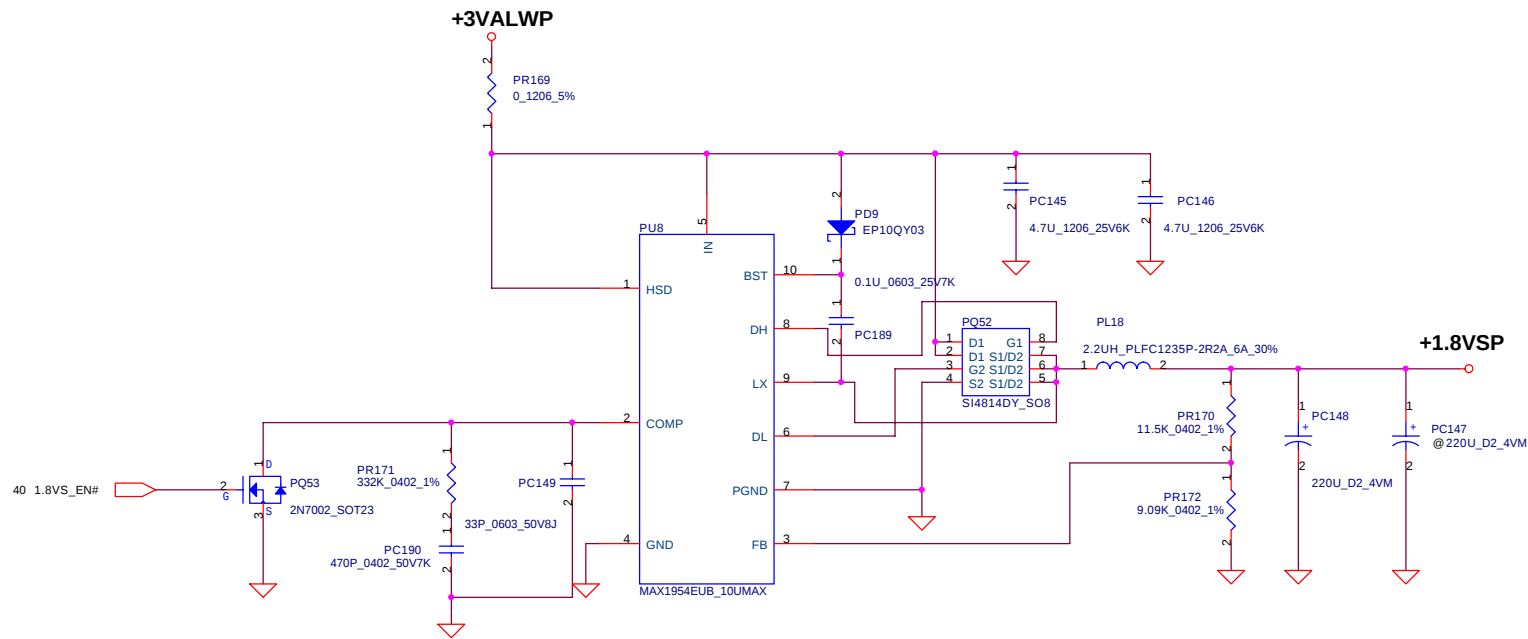
+2.5VALWP

2.5V OCP > 13A

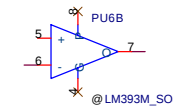
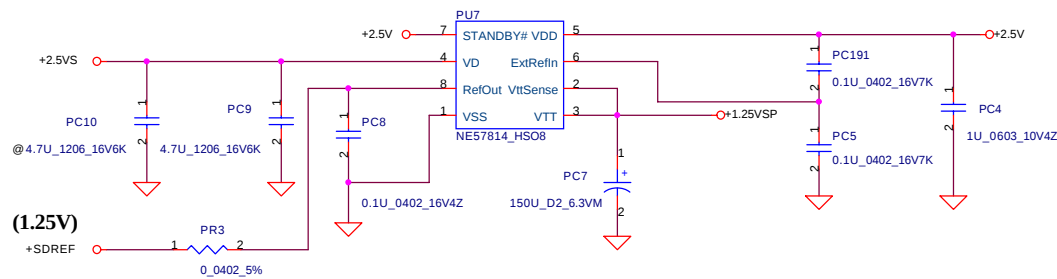
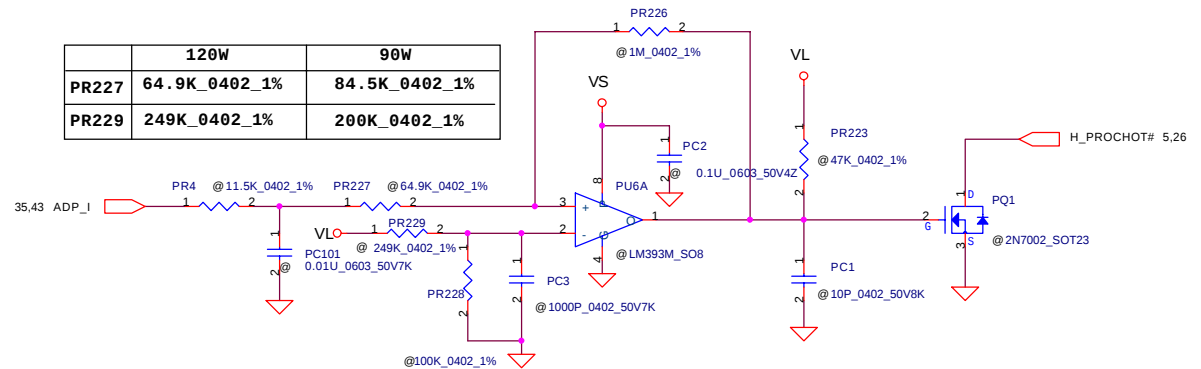


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Compal Electronics, Ltd.				
Title				
+2.5VALWP/1.5VP				
Size	Custom	Document Number	Rev	
LA-2051			0.1A	
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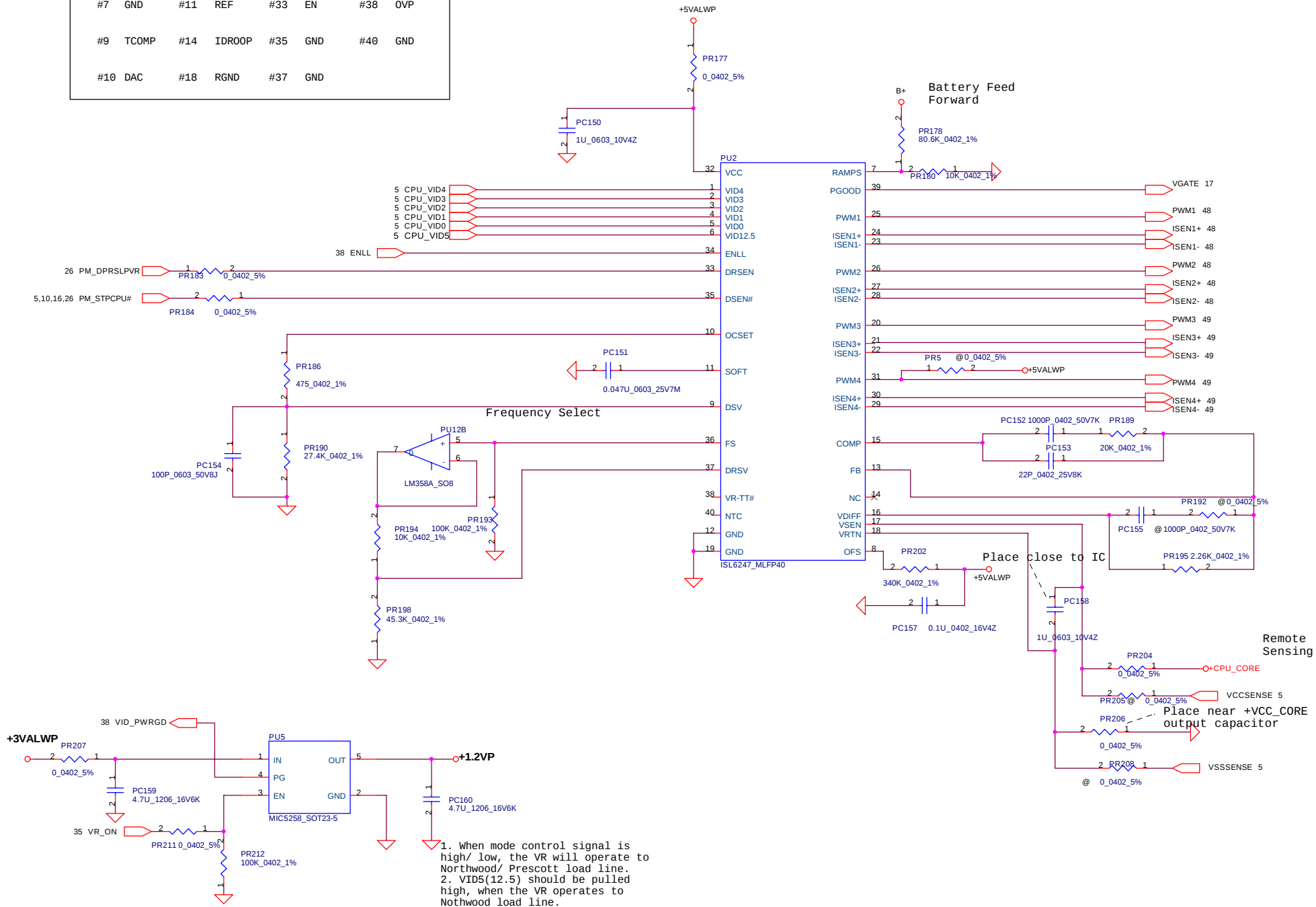


	120W	90W
PR227	64.9K_0402_1%	84.5K_0402_1%
PR229	249K_0402_1%	200K_0402_1%



Different Pin Definition for ISL6561 in PU9

#7	GND	#11	REF	#33	EN	#38	OVP
#9	TCOMP	#14	IDROOP	#35	GND	#40	GND
#10	DAC	#18	RGND	#37	GND		



BOOTSELECT=1 PRESCOTT

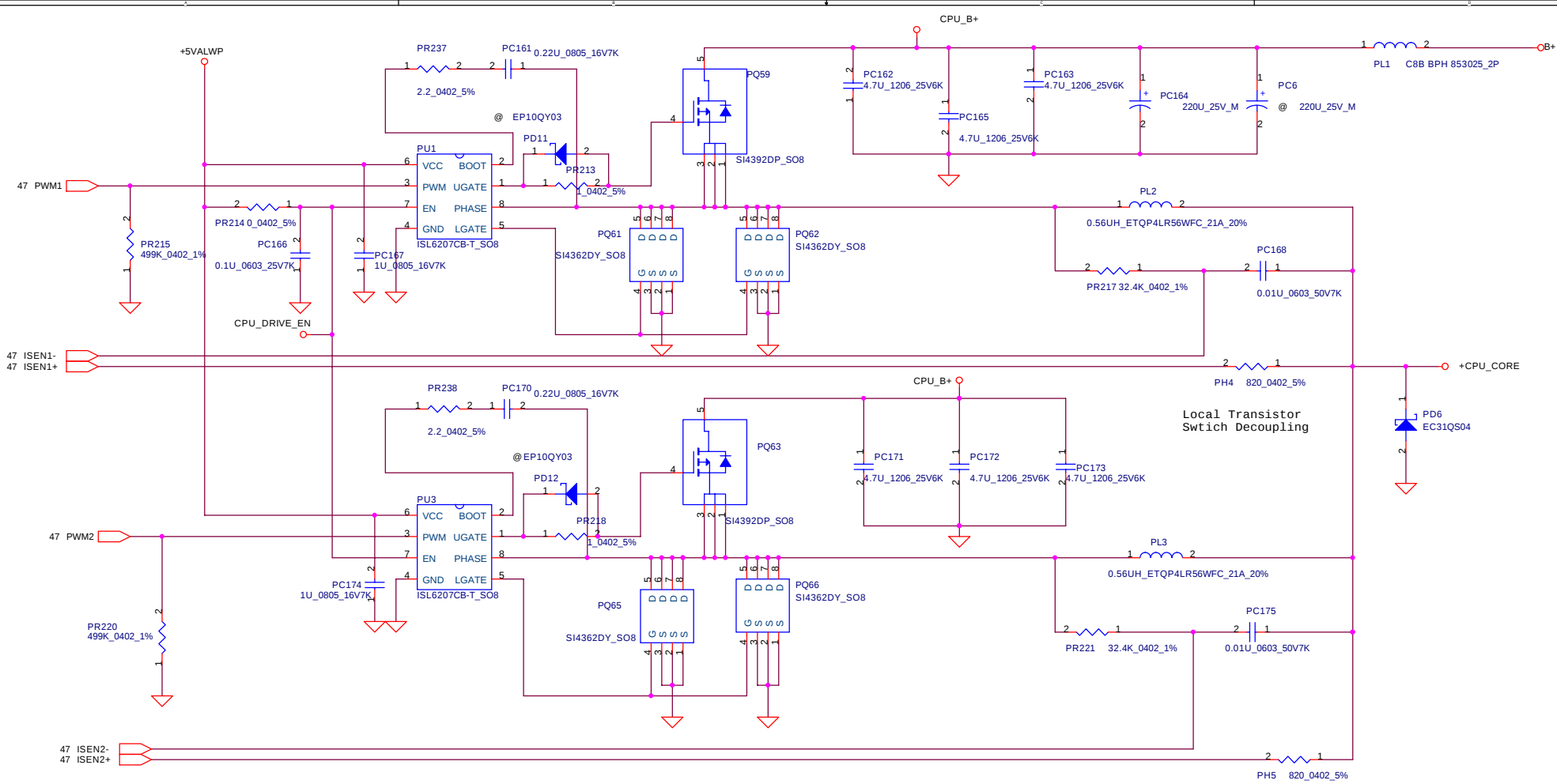
BOOTSELECT=0 NORTHWOOD

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Compal Electronics, Ltd.

Title			CPU_CORE Controller	
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Rev 0.1A

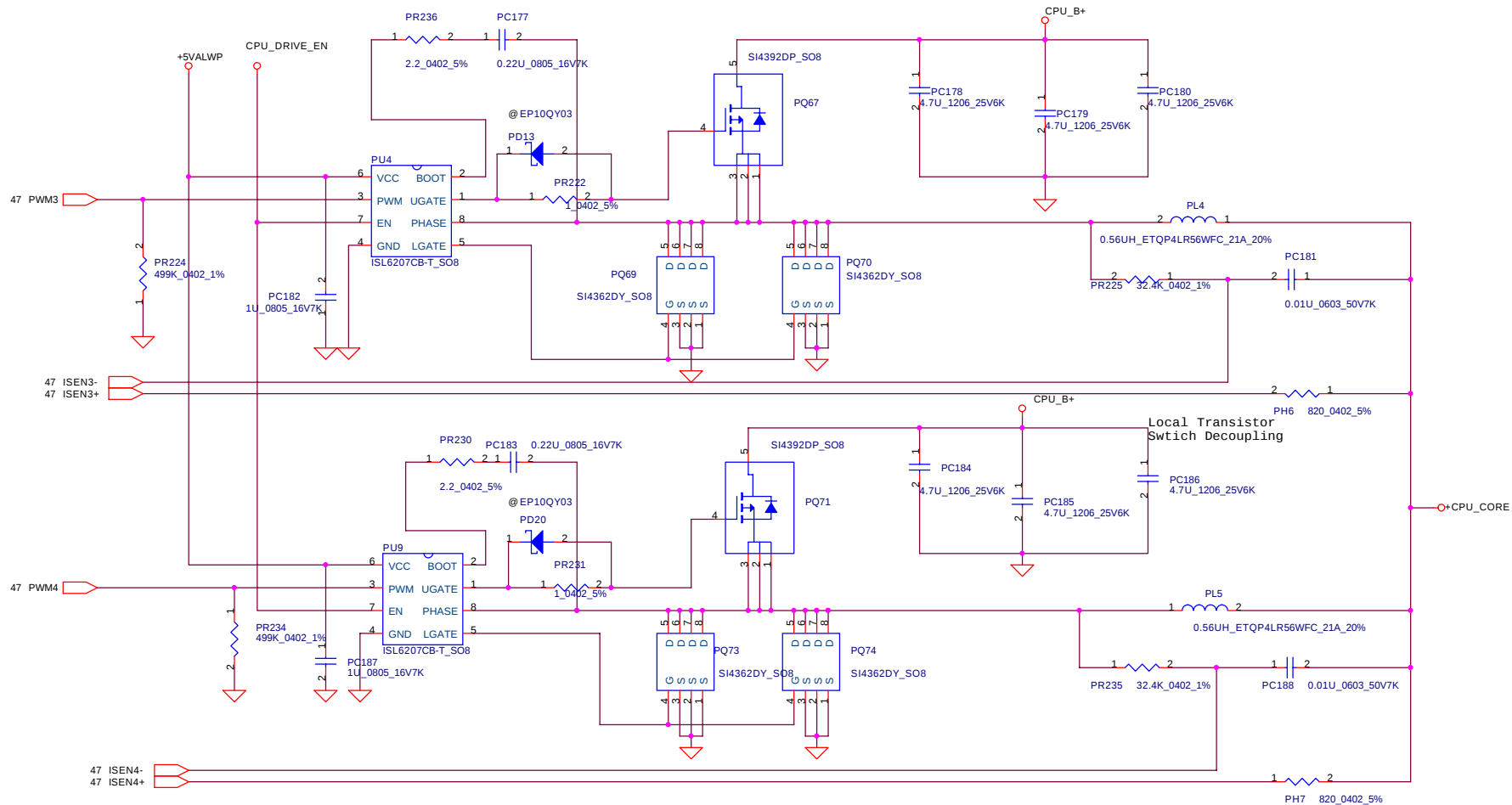


Compal Electronics, Ltd.

CPU_CORE Power stage

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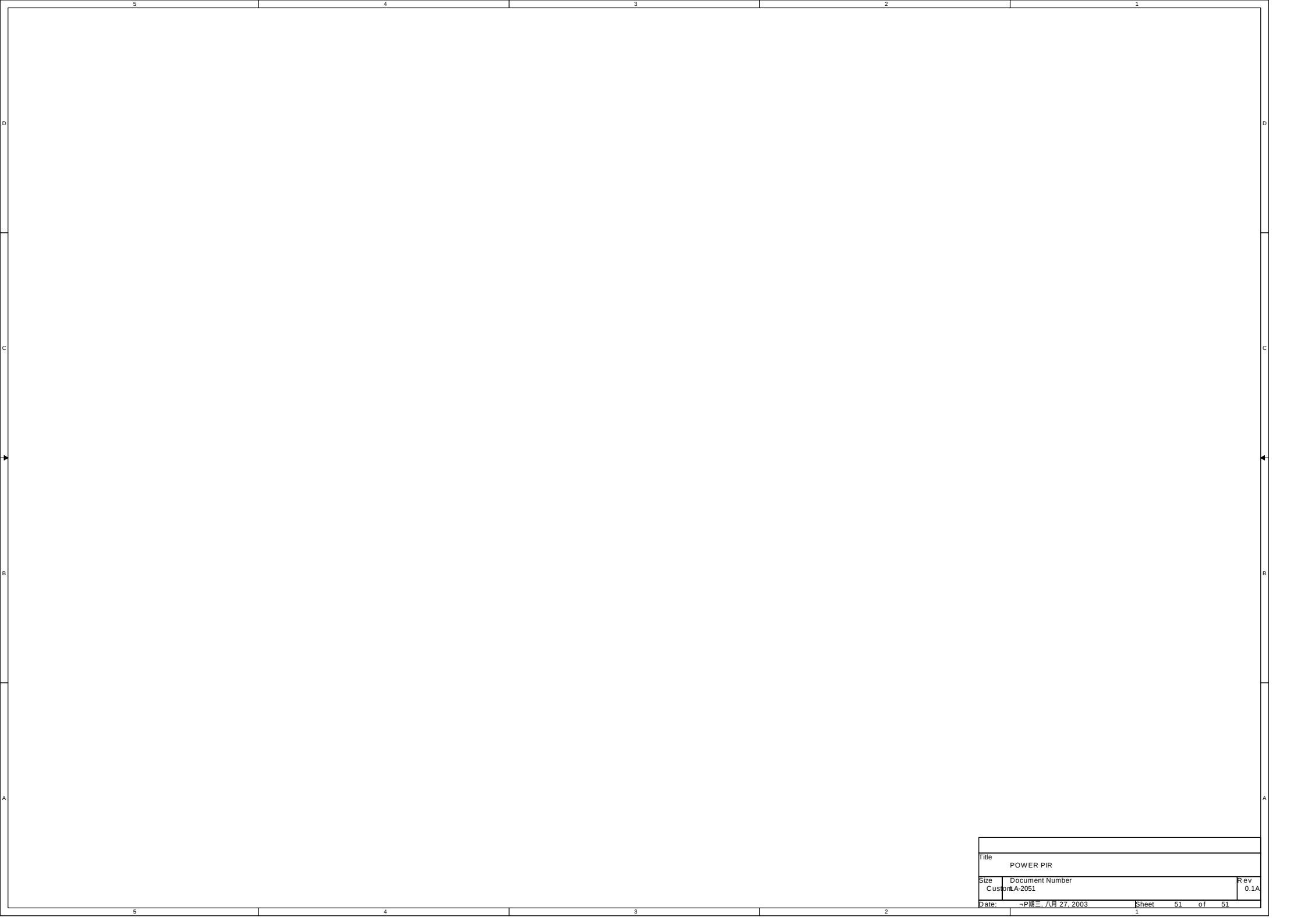
Compal Electronics, Ltd.

Title		CPU_CORE Power stage	
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Compal Electronics, Ltd.		
Title		
HW PIR		
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Title			
POWER PIR			
Size	Document Number		
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		1	