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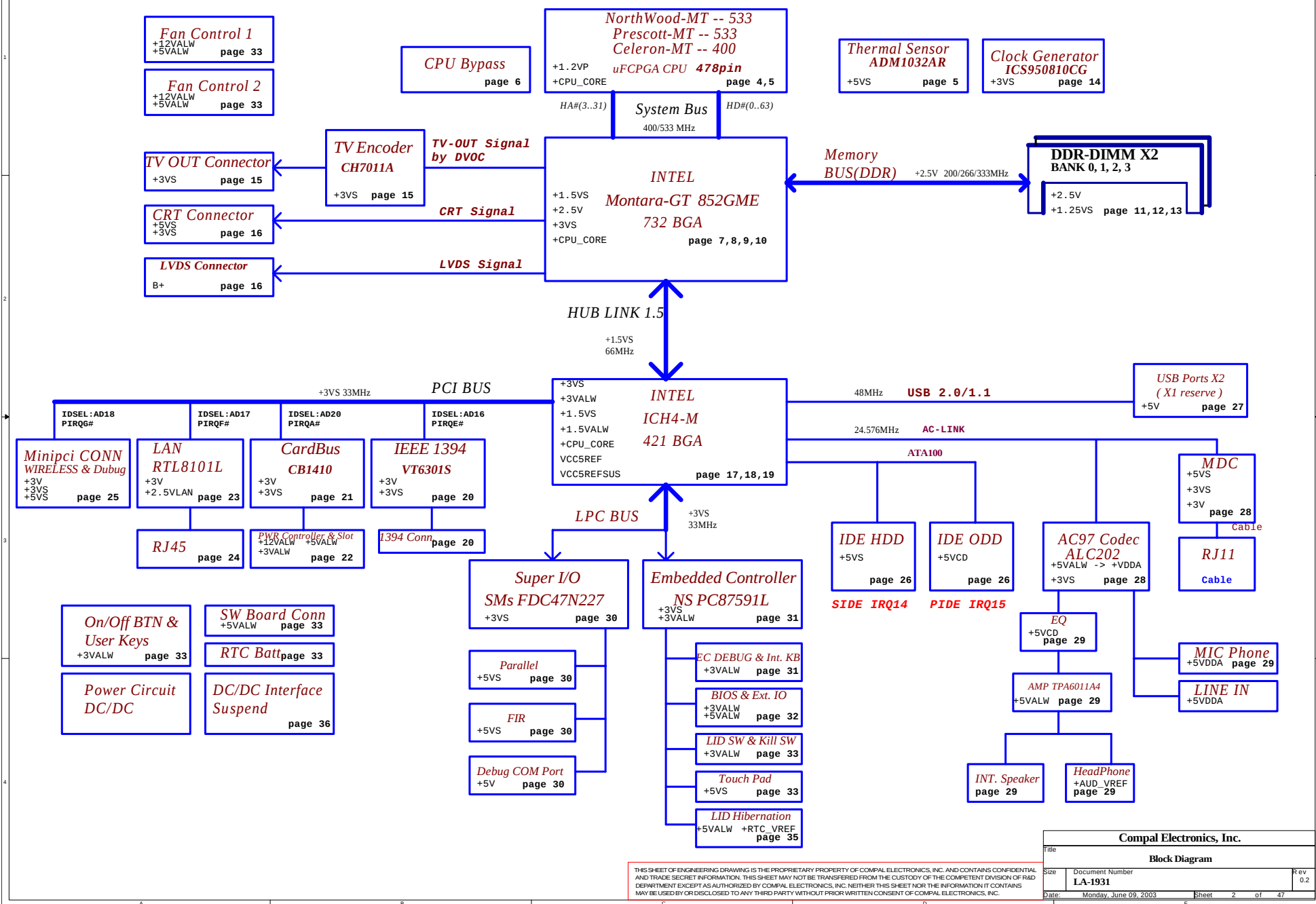
MODEL NAME : DBL10 -- Sapporo X
COMPAL P/N : DA8BL10L000
PCB NO : LA-1931
Revision : 0.2

DBL10 -- Sapporo X Schematics Document
uFCBGA/uFCPGA NorthWood MT
2003-06-09 0.2 Gerber Out Version

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Model : DBL10 -- Sapporo X



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.2V	1.2V switched power rail for CPU AGTL Bus	ON	ON	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON
+RTCBATT	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices (follow PCI IRQ routing plannig ver0.2.04)

Device	IDSEL#	REQ#/GNT#	Interrupts - (ICH4-M)
CardBus (ENE-CB1410)	AD20	2	PIRQA#
IEEE 1394 (VIA-VT6301S)	AD16	0	PIRQE#
LAN (Realtek-RTL8101L)	AD17	3	PIRQF#
Mini-PCI	AD18	1/1	PIRQG#

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16)	1010 000X b

EC SM Bus2 address

Device	Address
ADM1032	1001 100X b

ICH4 SM Bus address

Device	Address
CLK GEN (ICS-950810)	1101 001X

Power Managment table

Signal \ State	+1.5VALW +3VALW +5VALW +12VALW	+5V +3V +2.5V +1.2V	+5VS +3VS +1.5VS +CPU_CORE +1.25VS
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

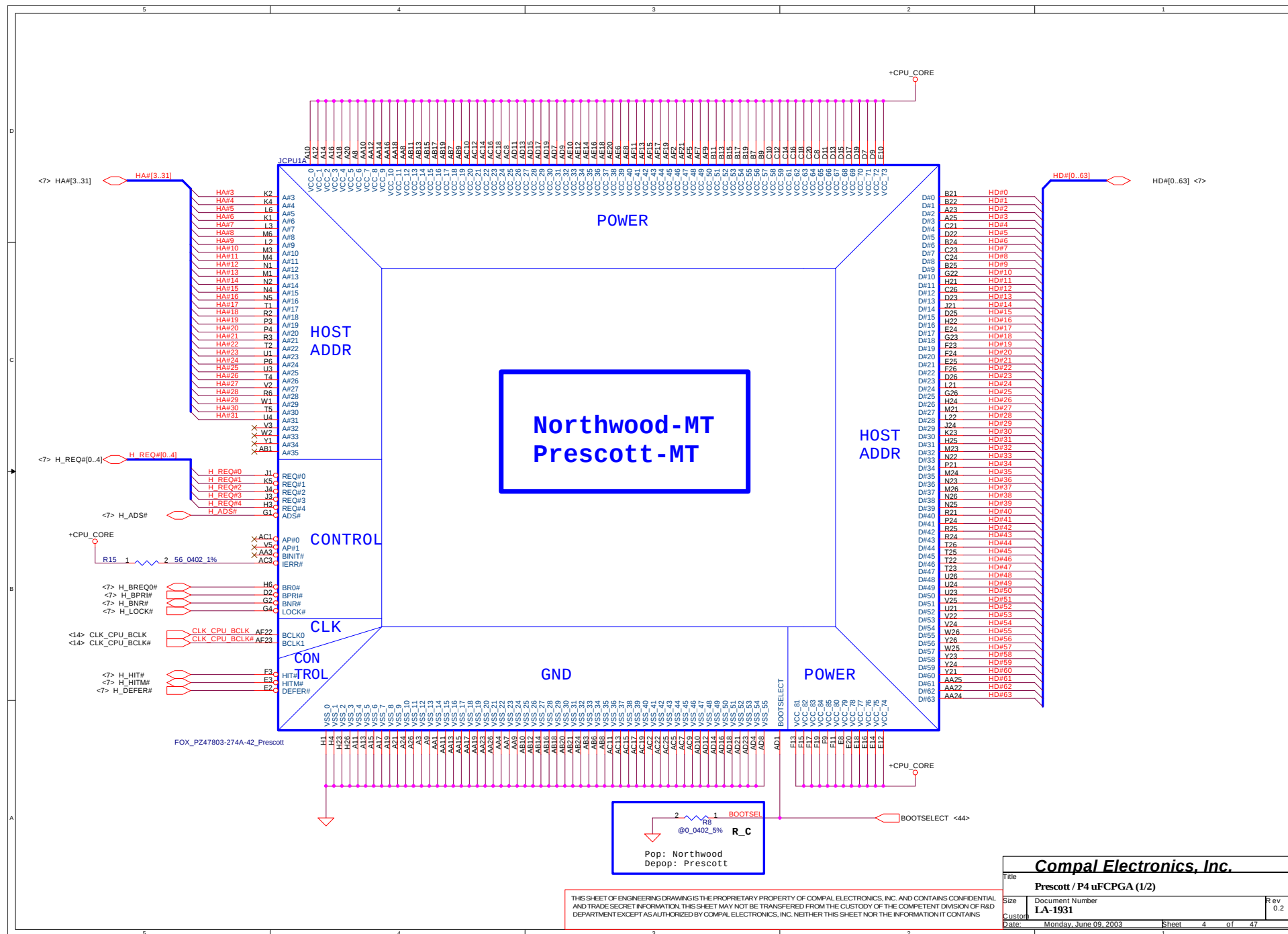
Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 1%	0.216 V	0.250 V	0.289 V
2	18K +/- 1%	0.436 V	0.503 V	0.538 V
3	33K +/- 1%	0.712 V	0.819 V	0.875 V
4	56K +/- 1%	1.036 V	1.185 V	1.264 V
5	100K +/- 1%	1.453 V	1.650 V	1.759 V
6	200K +/- 1%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

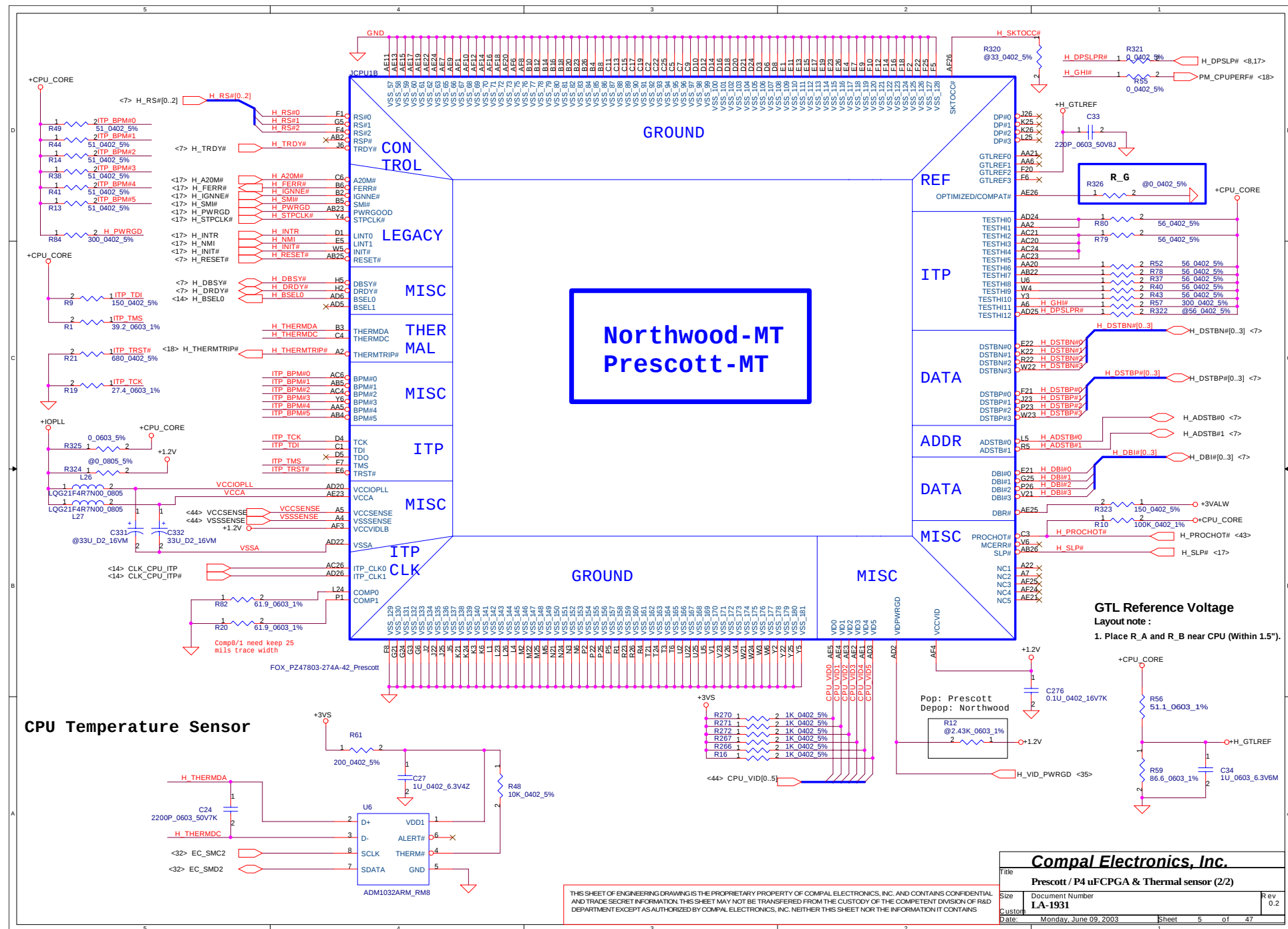
Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

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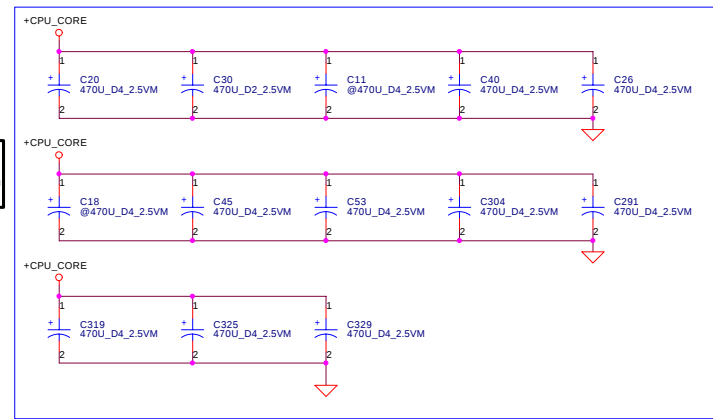
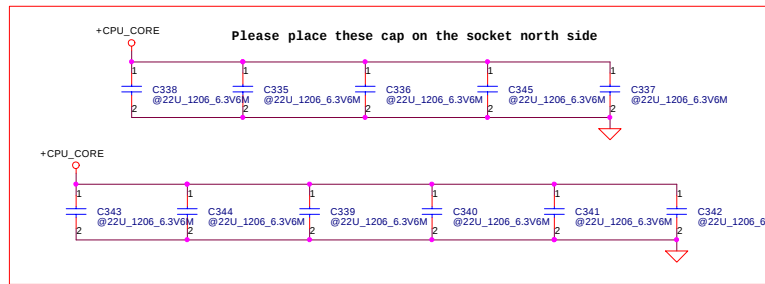
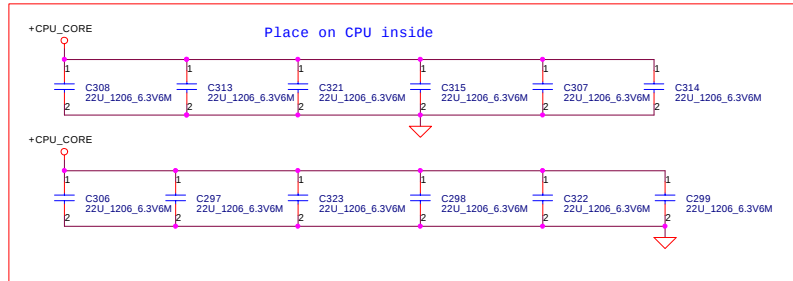
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Title			
Prescott / P4 uFCPGA (1/2)			
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LA-1931			
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Layout note :
Place close to CPU. Use 2~3 vias per PAD.
Place 22uF caps x31 pcs, populated 14pcs.

Layout note :
Place close to CPU power and ground pin as possible (<1inch)

For Desktop's CPU:
470uFx15/12mOhm H=1.8 each
Total 0.923m ohm



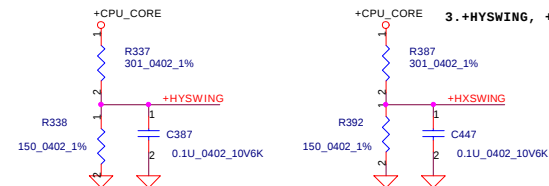
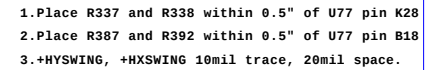
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Title			
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CPU Decoupling CAP.			
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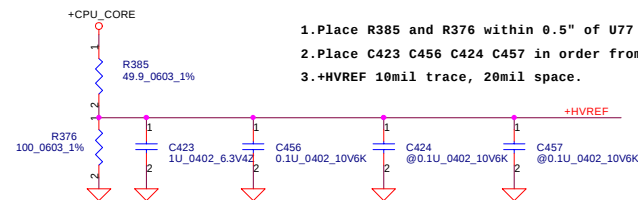


HOST

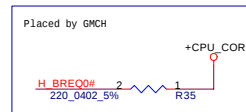
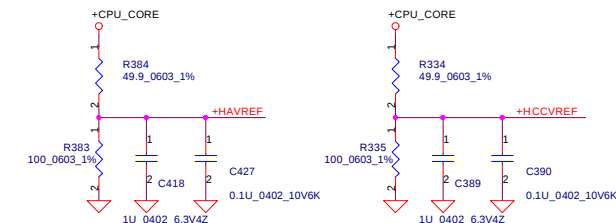
HUB I/F



- 1.Place R385 and R376 within 0.5" of U77 pin K21 J21 J17
- 2.Place C423 C456 C424 C457 in order from U77 to divider
- 3.+HVREF 10mil trace, 20mil space.



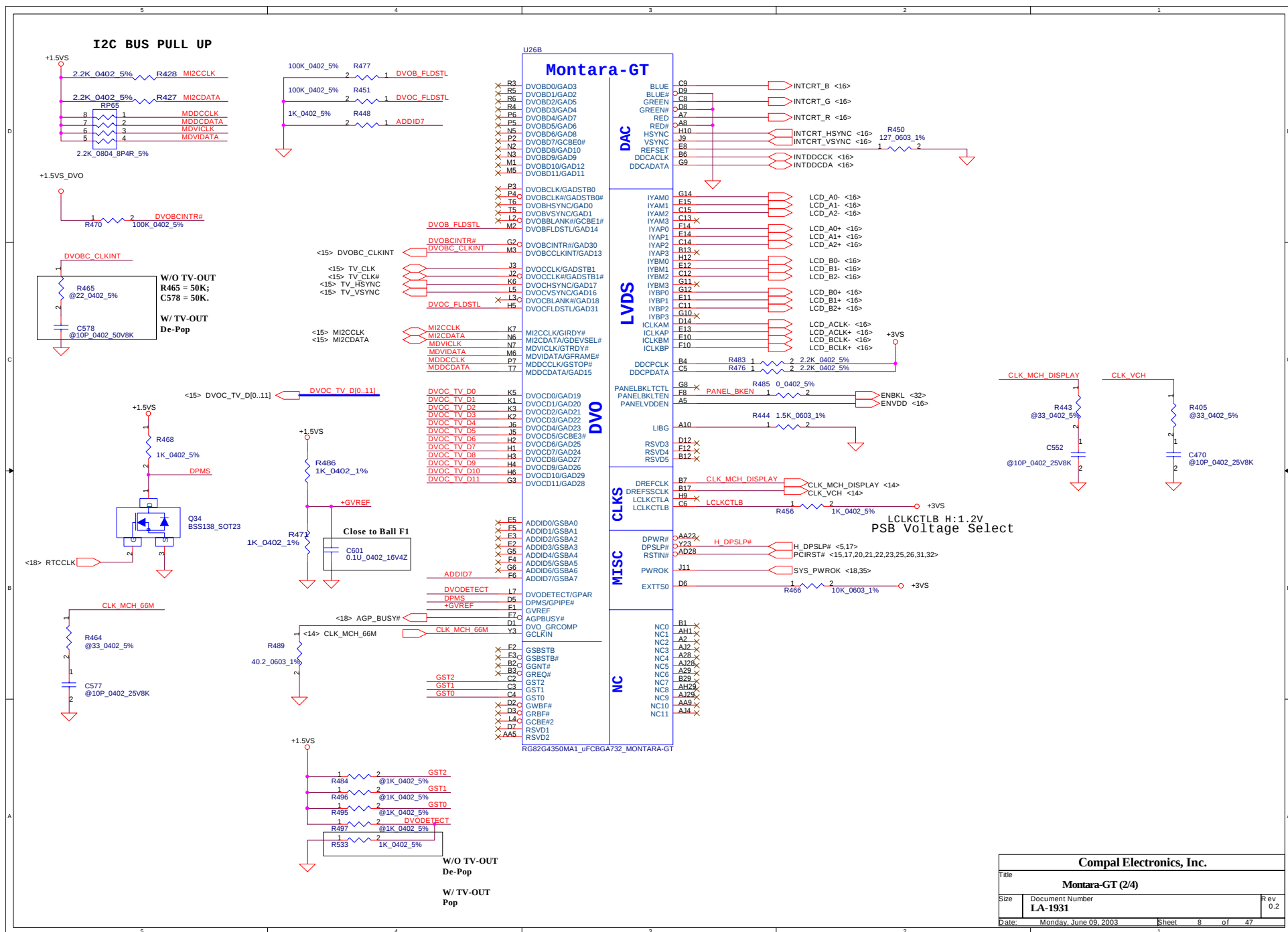
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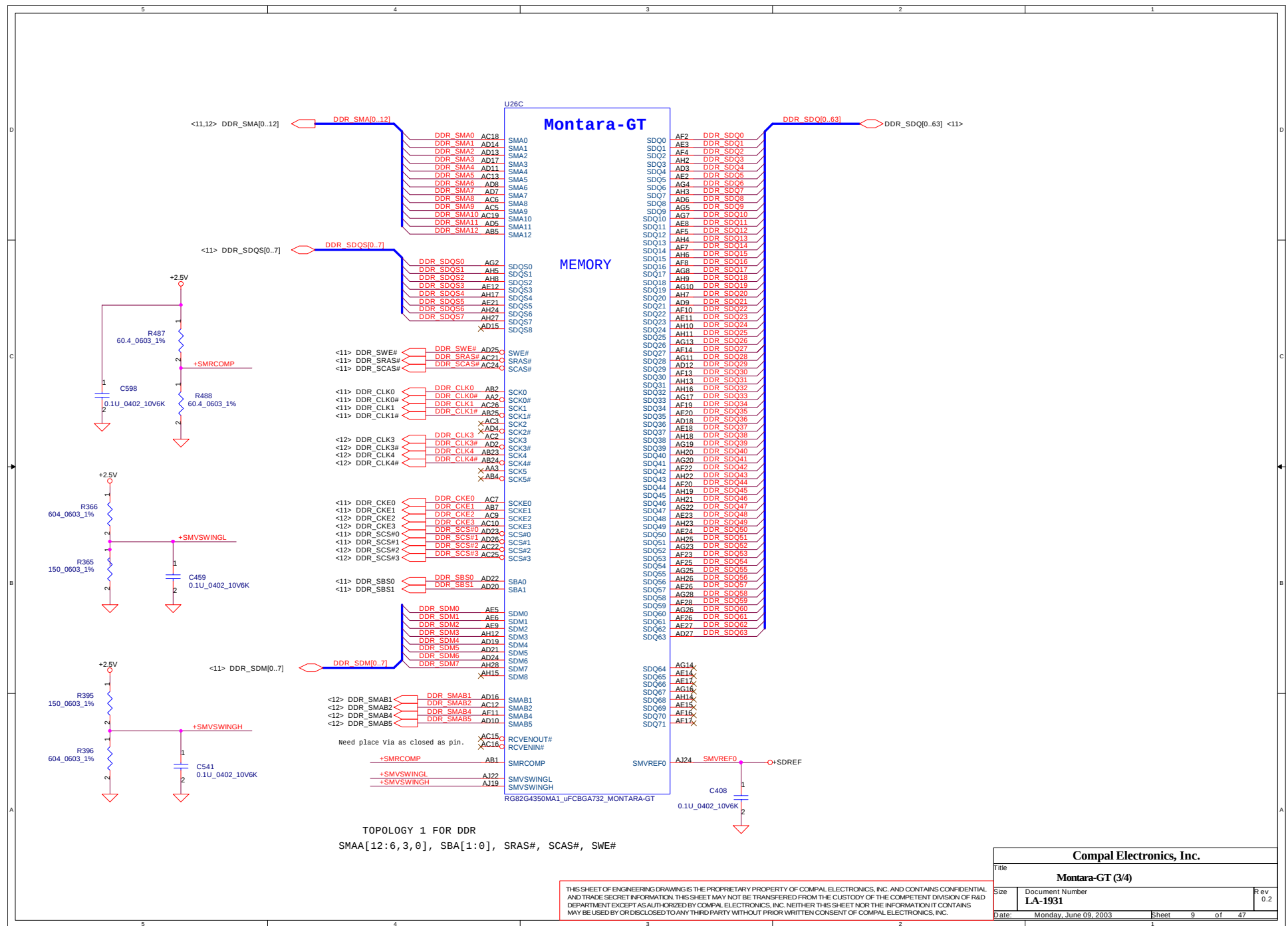


The schematic diagram illustrates the HUB Reference Voltage circuit. It is powered by a +1.5VS supply. The circuit includes three resistors: R455 (80.6_0402_1%), R491 (111_0603_1%), and R490 (40.2_0603_1%). There are four capacitors: C588 (0.01uF_0402_25V7Z), C593 (0.1uF_0402_10V6K), C592 (0.01uF_0402_25V7Z), and C591 (0.1uF_0402_10V6K). The circuit generates two signals: +HUB_PSWING and +HUB_VREF. The +HUB_PSWING signal is derived from the +1.5VS supply through R455 and C588. The +HUB_VREF signal is derived from the +HUB_PSWING signal through R491 and C593. The +HUB_VREF signal is also connected to the +HUB_PSWING signal through R490 and C591.

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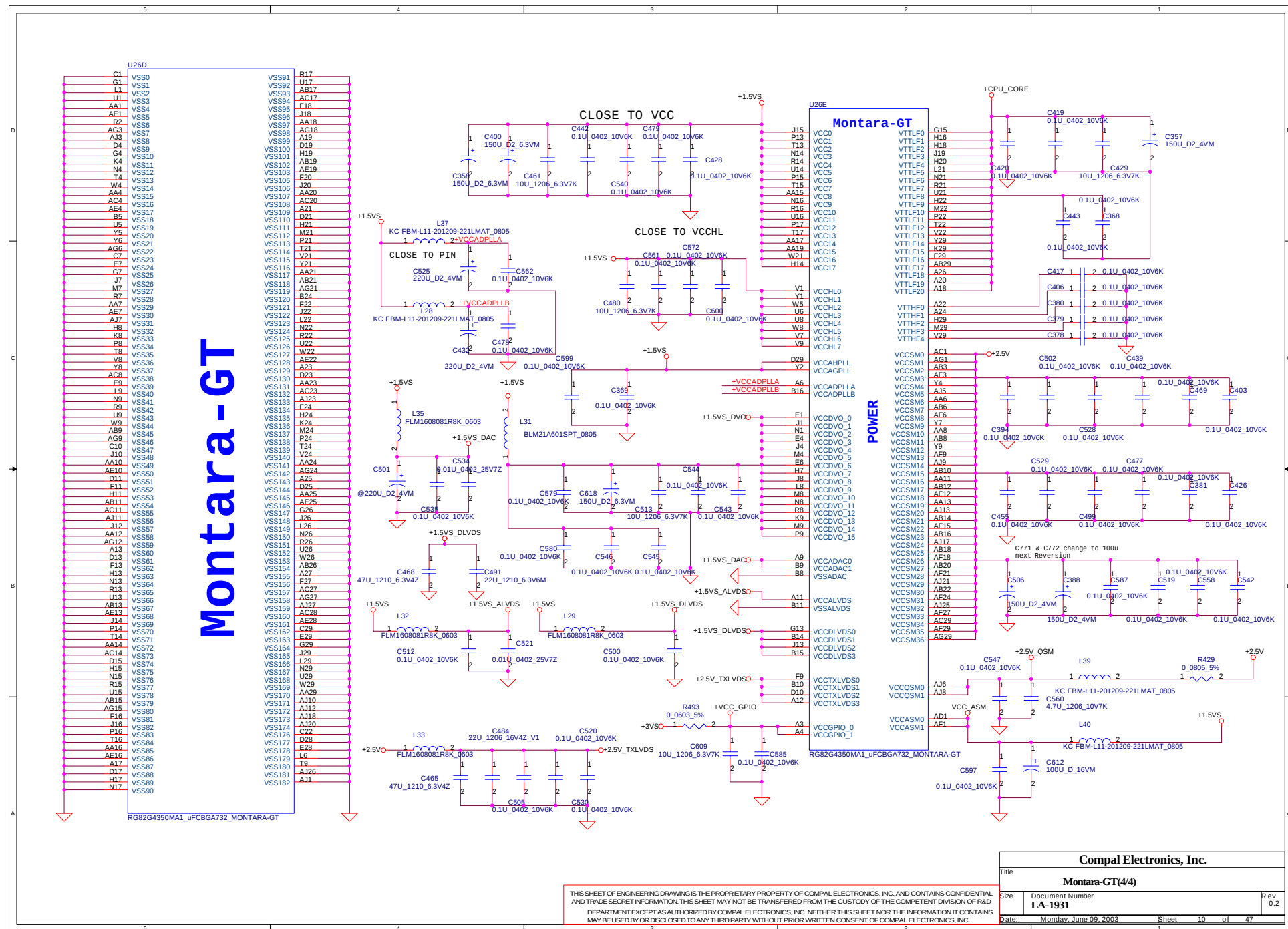
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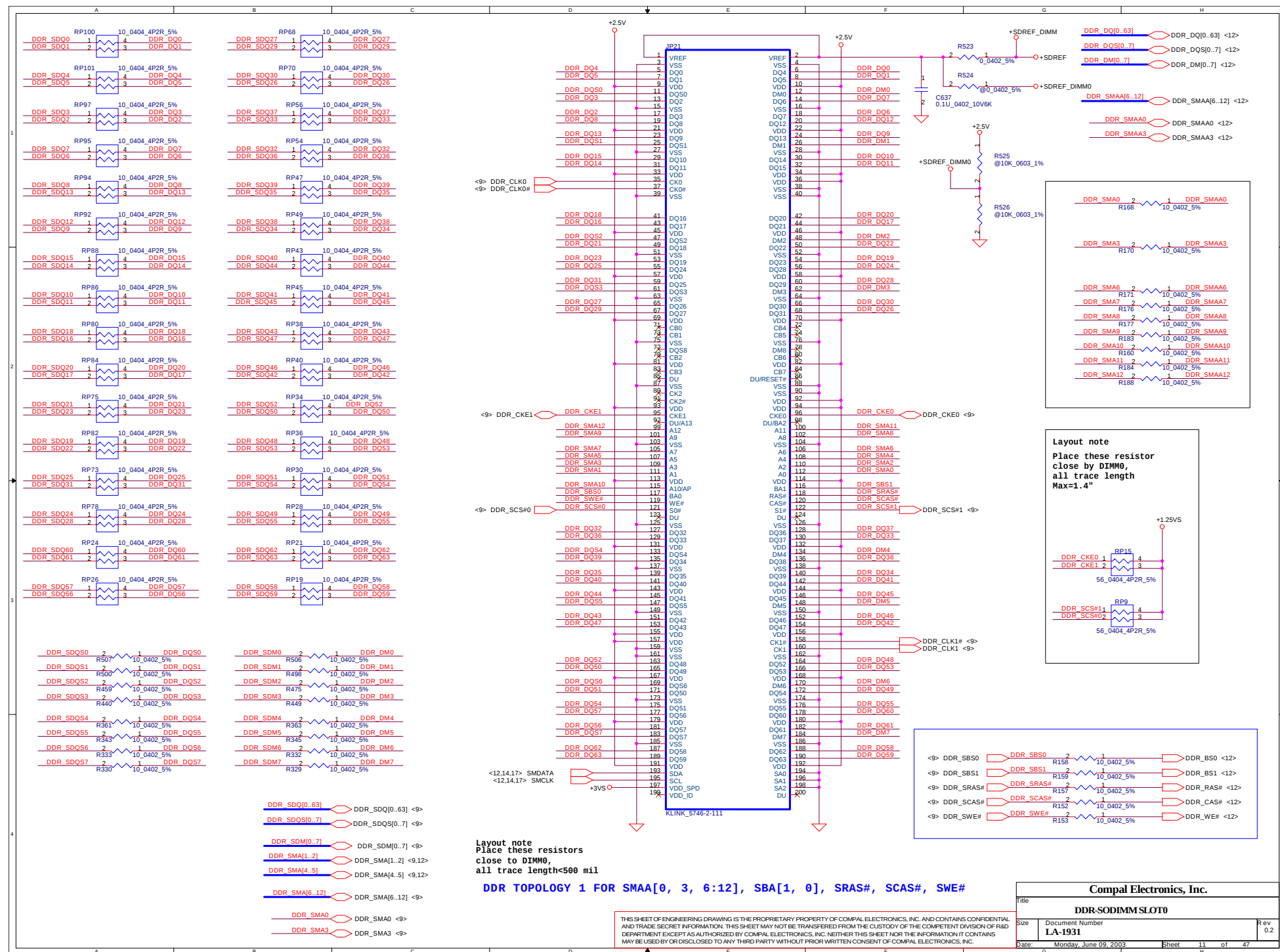




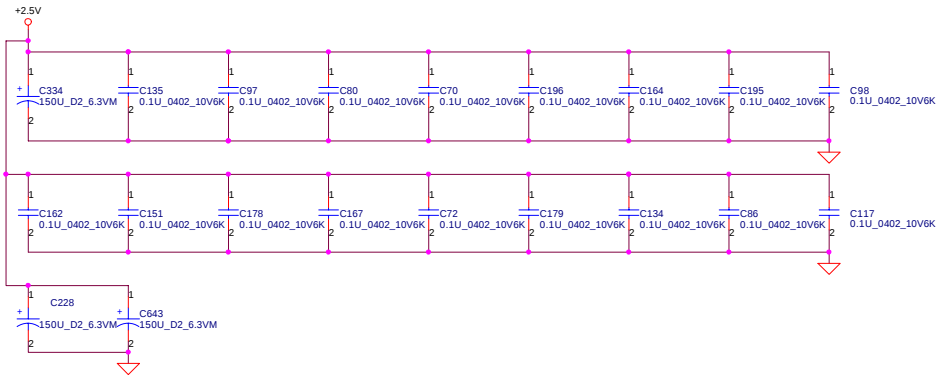
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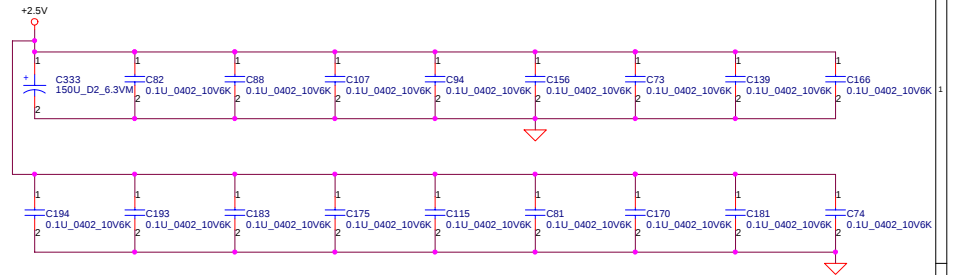
Layout note :
Distribute as close as possible
to DDR-SODIMM0.



Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25VS



Layout note :
Distribute as close as possible
to DDR-SODIMM1.

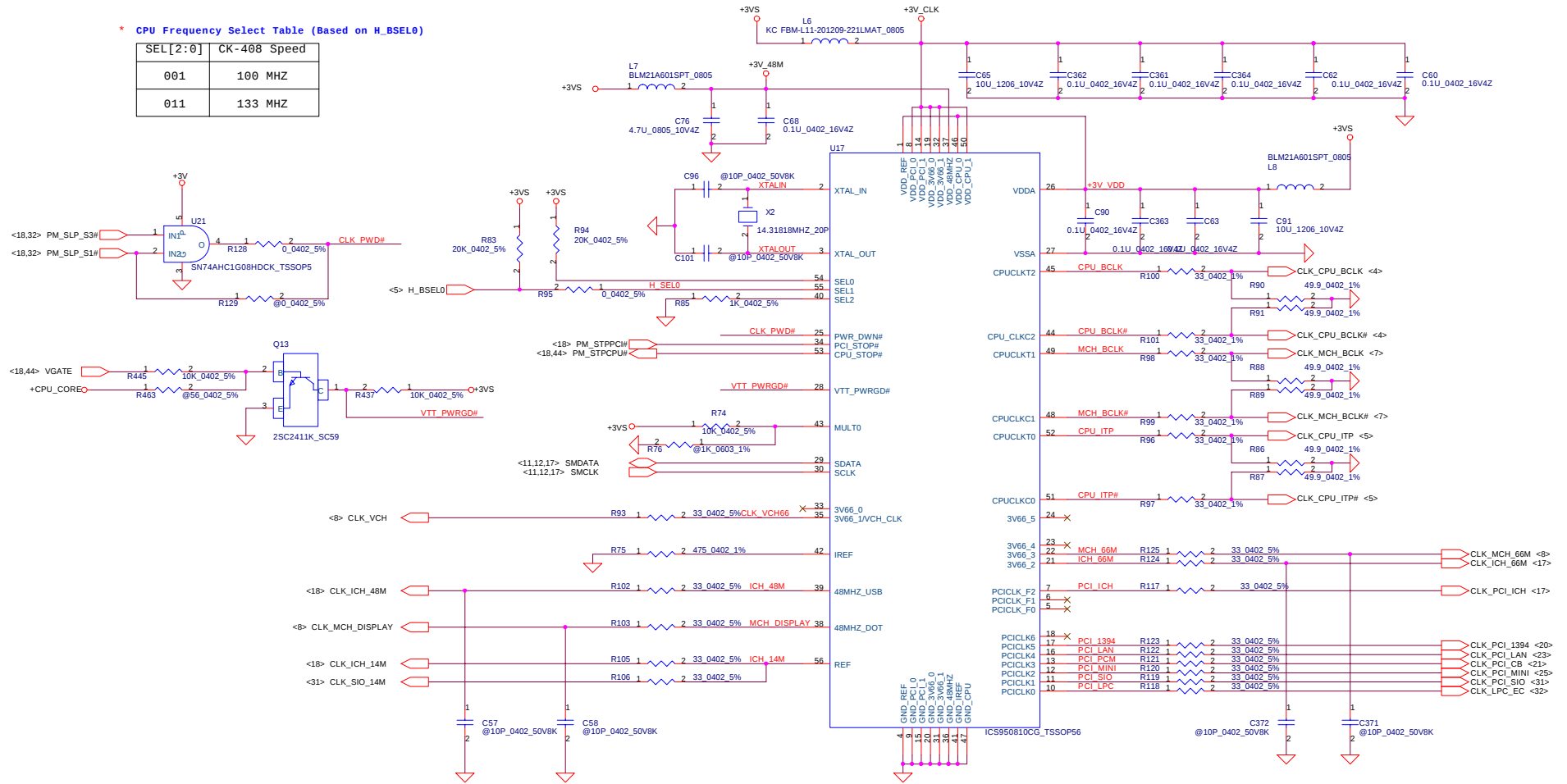


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Title			
DDR SODIMM Decoupling			
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* CPU Frequency Select Table (Based on H_BSEL0)

SEL[2:0]	CK-408 Speed
001	100 MHZ
011	133 MHZ



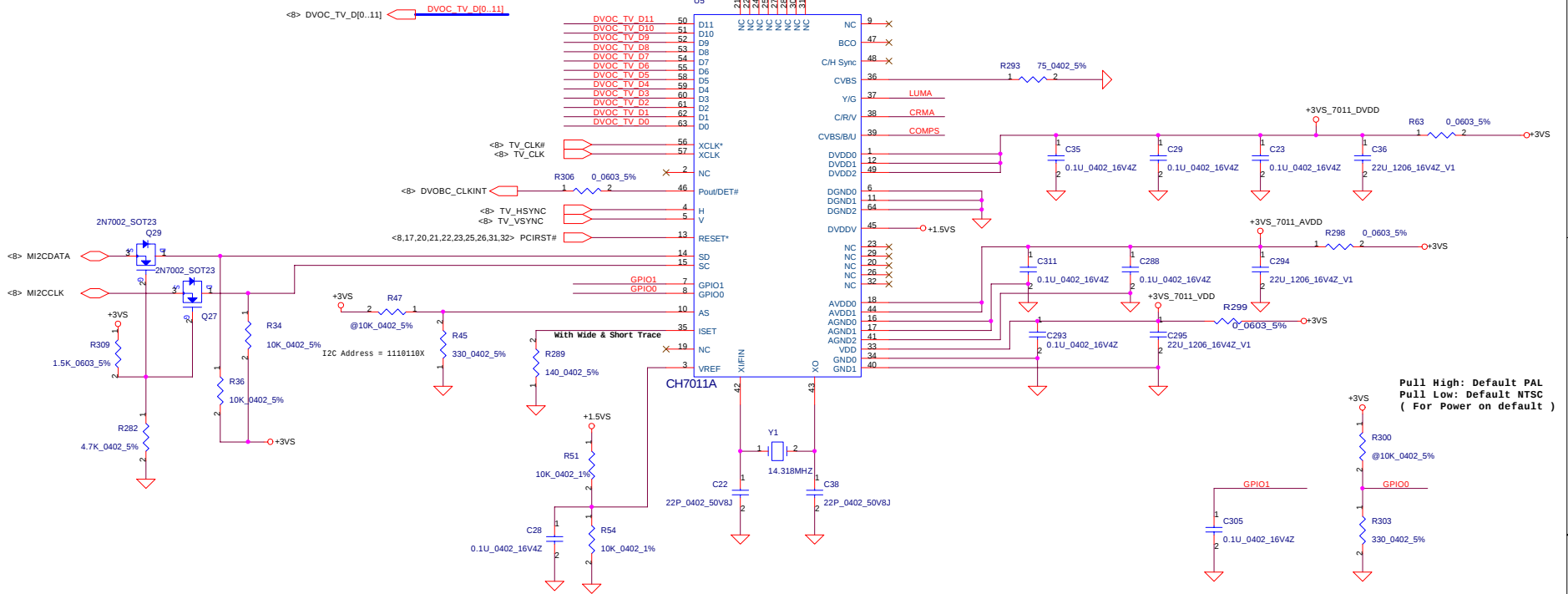
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Clock Generator

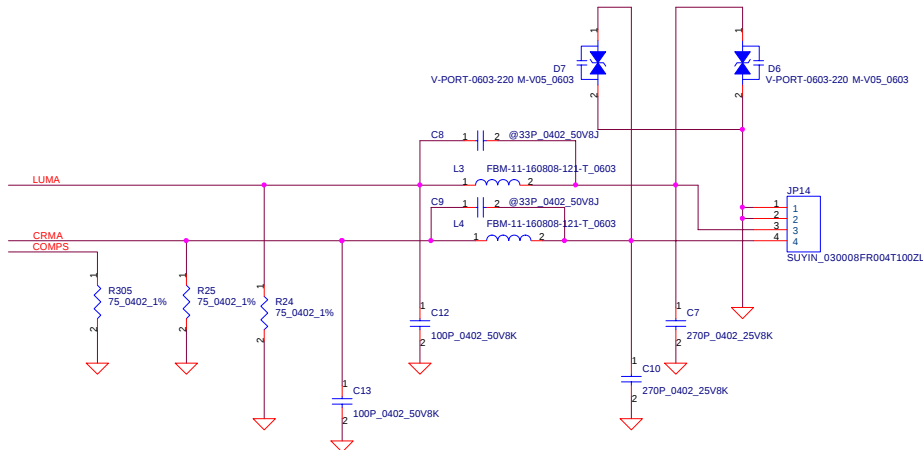
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CH-7011A



TV-OUT CONN.



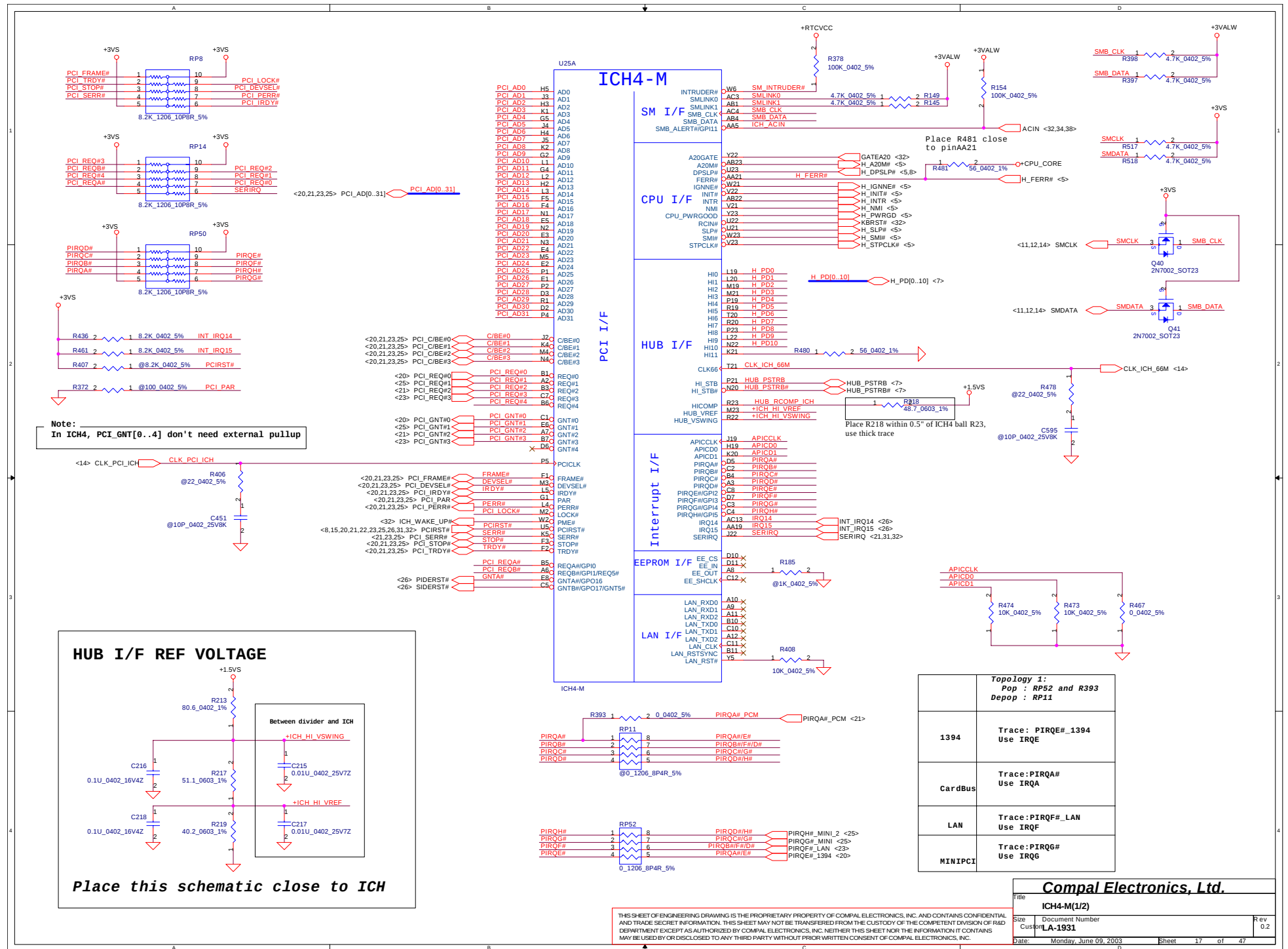
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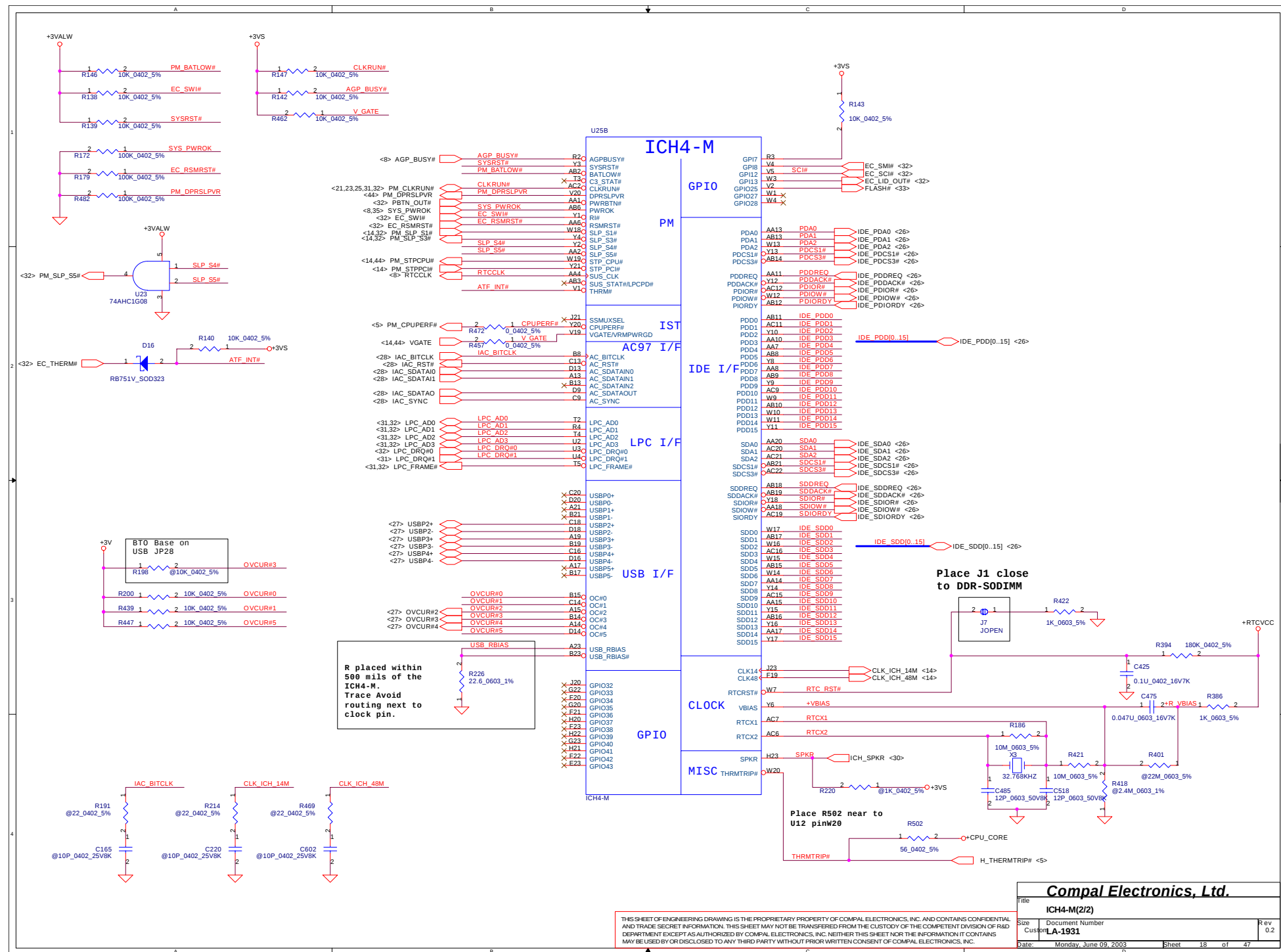
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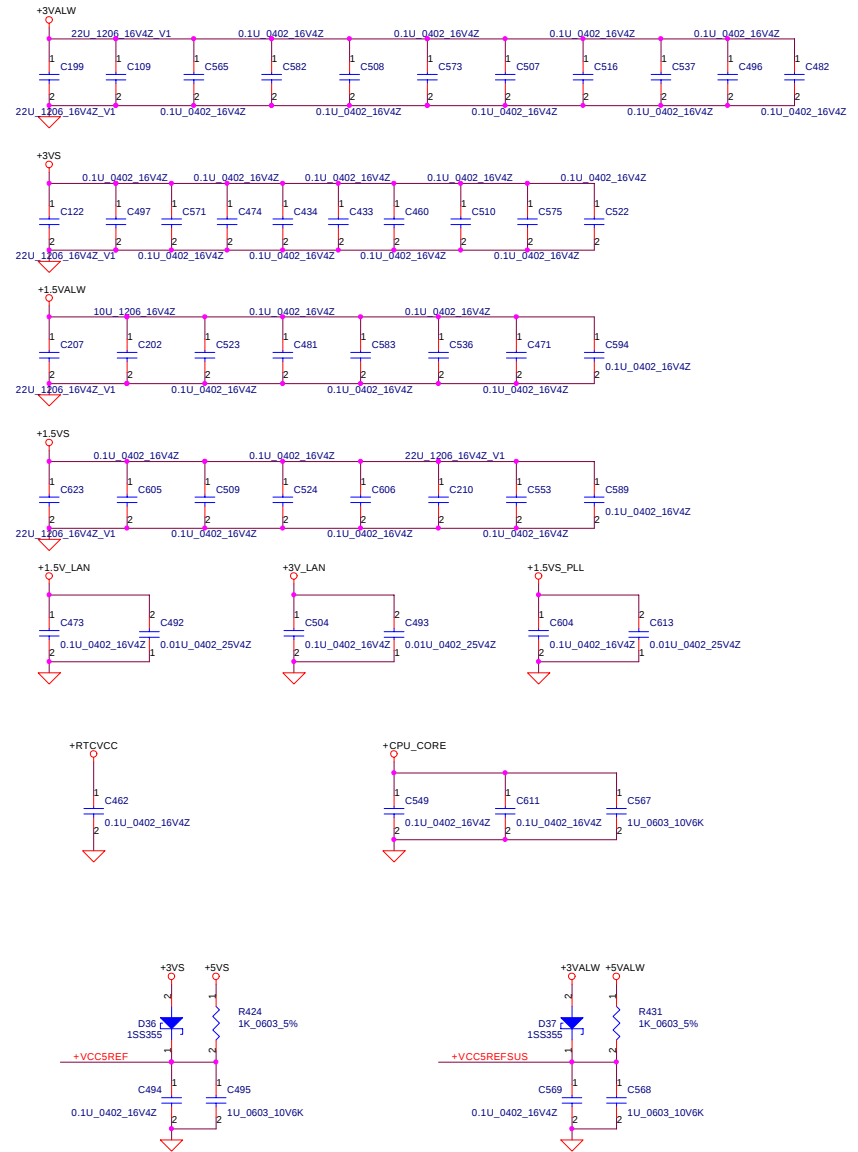
CH-7011& TV-CONN.

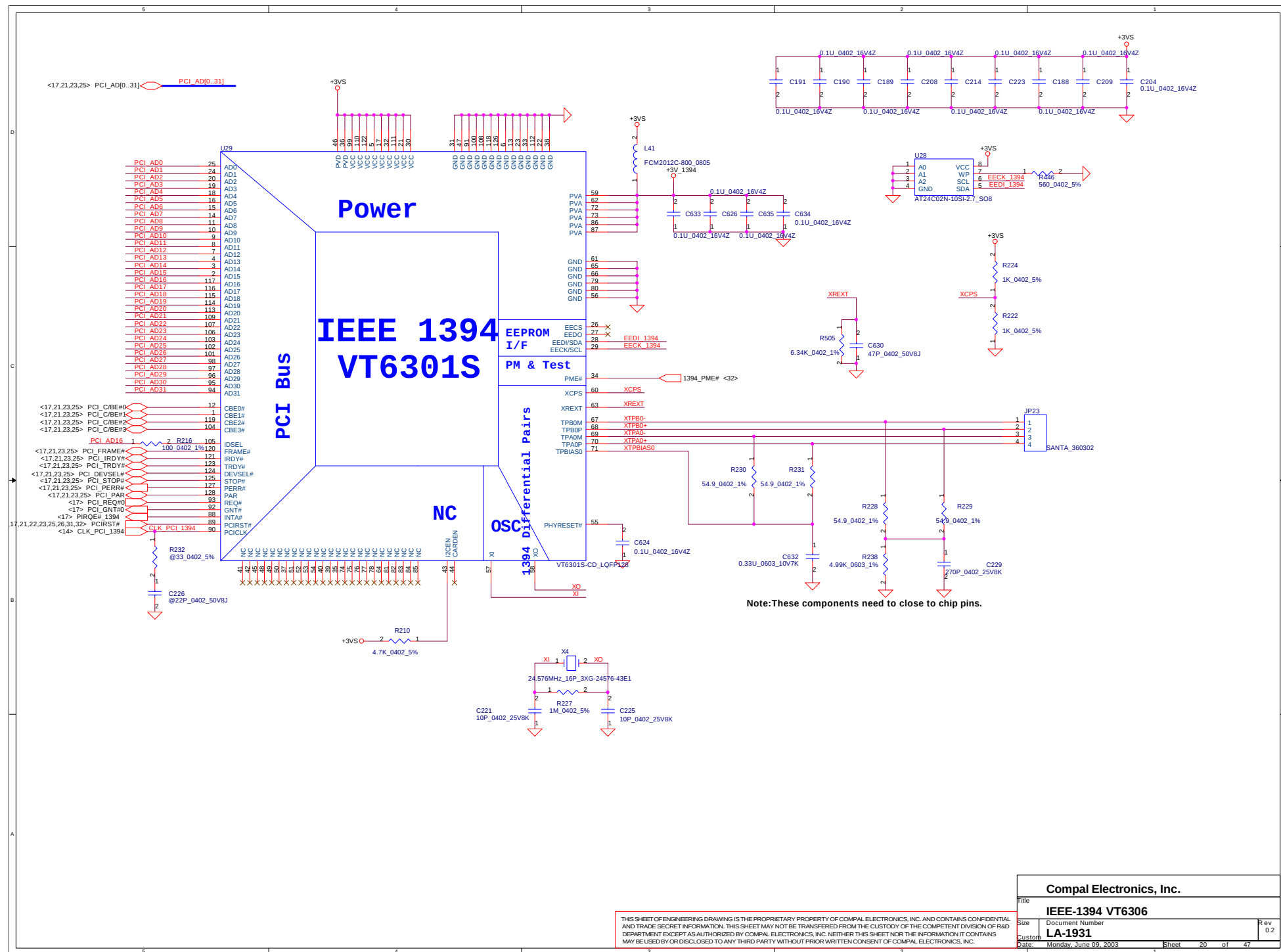
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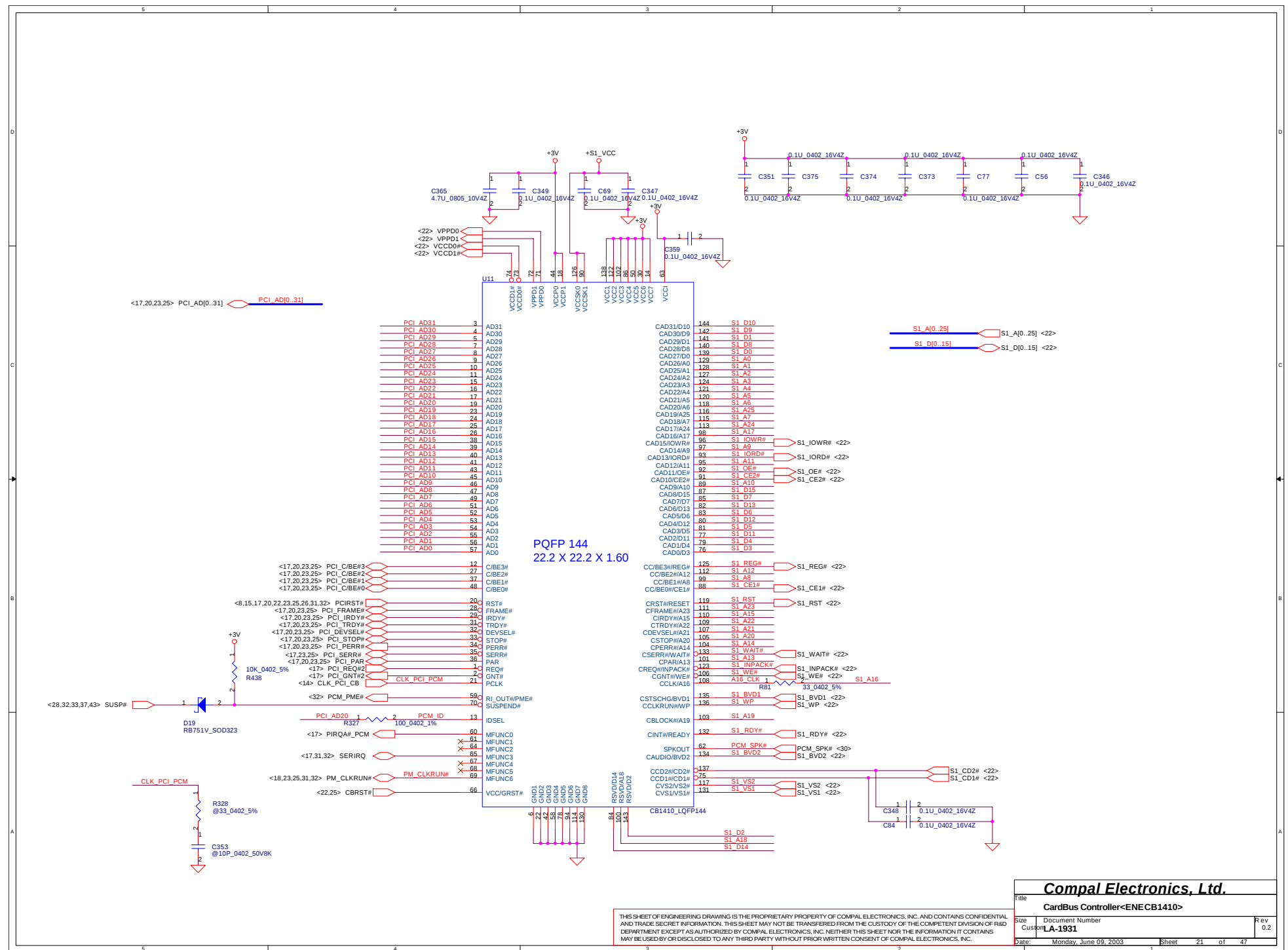
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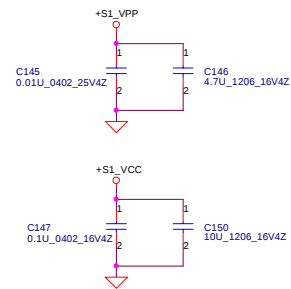










[illegible]

<21> S1_A[0..25]  S1_A[0..25]

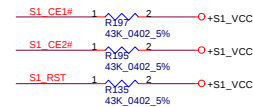
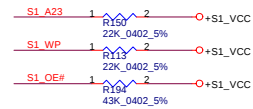
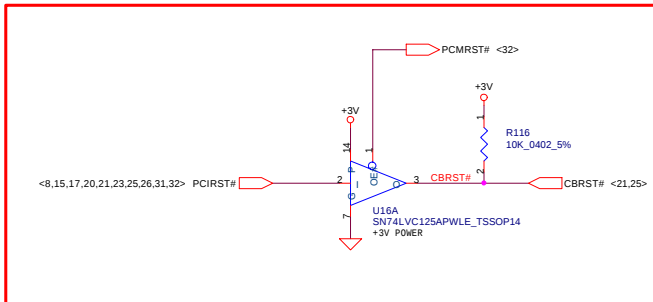
<21> S1_D[0..15]  S1_D[0..15]

Pin-to-pin connection diagram for the FOXCONN_1CA415M1-TA_6BP (APL111) component. The diagram shows two 84-pin connectors, JP18 and JP19, connected to a central component. Pin 1 of JP18 is connected to Pin 1 of JP19, and so on, up to Pin 84. The diagram also shows the internal connections of the component, including the S1_VCC and S1_VPP pins, and the S1_VS2, S1_RST, S1_WAIT#, S1_INPACK#, S1_REG#, S1_BVD2, S1_BVD1, S1_D9, S1_D10, and S1_CD2# pins.

Legend:

- +S1_VCC
- +S1_VPP
- +S1_VS2
- +S1_VS1
- +S1_VS0
- +S1_VS3
- +S1_VS4
- +S1_VS5
- +S1_VS6
- +S1_VS7
- +S1_VS8
- +S1_VS9
- +S1_VS10
- +S1_VS11
- +S1_VS12
- +S1_VS13
- +S1_VS14
- +S1_VS15
- +S1_VS16
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- +S1_VS82
- +S1_VS83
- +S1_VS84

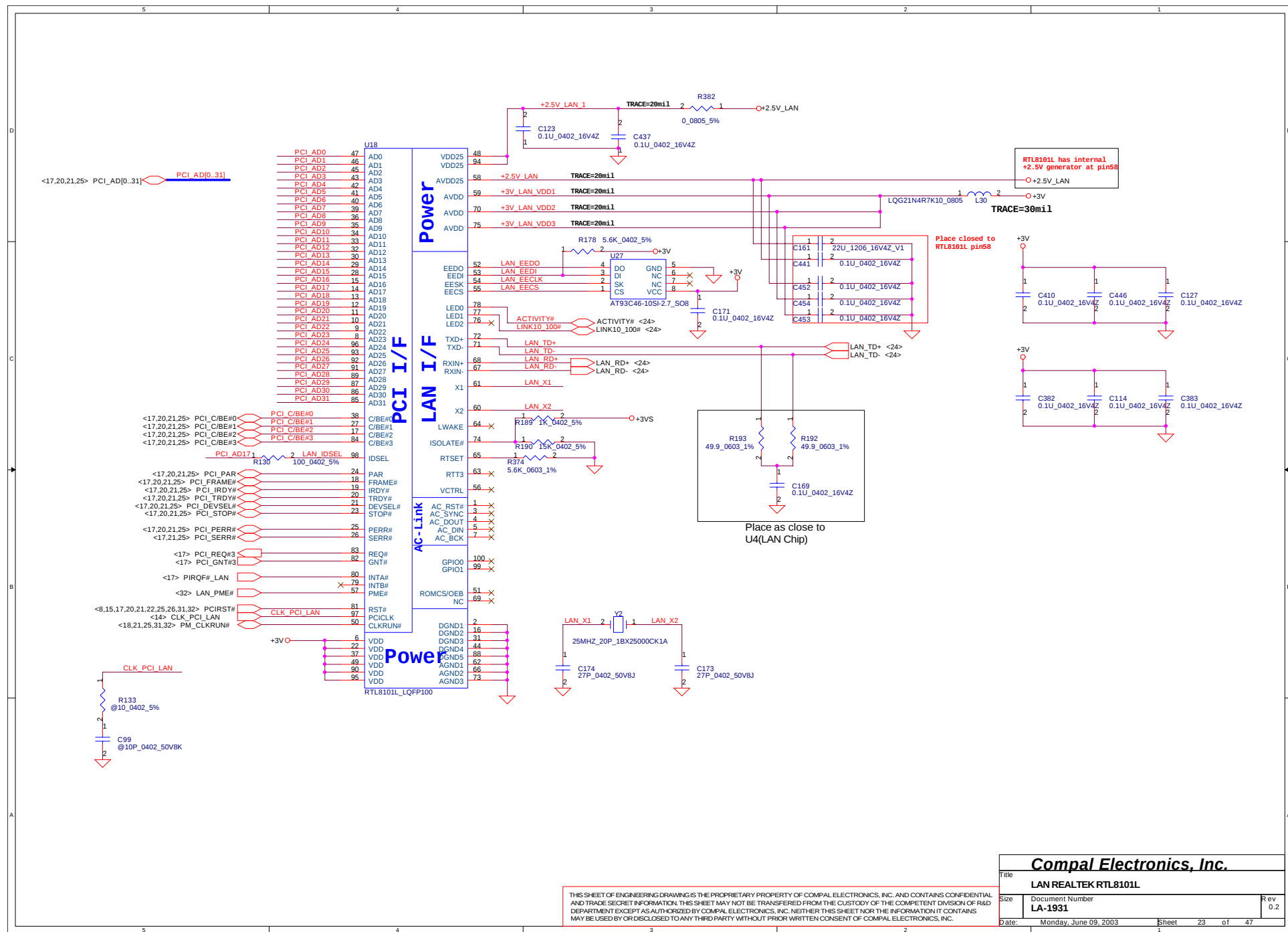
FOXCONN_1CA415M1-TA_6BP (APL111)



PCMCIA SOCKET

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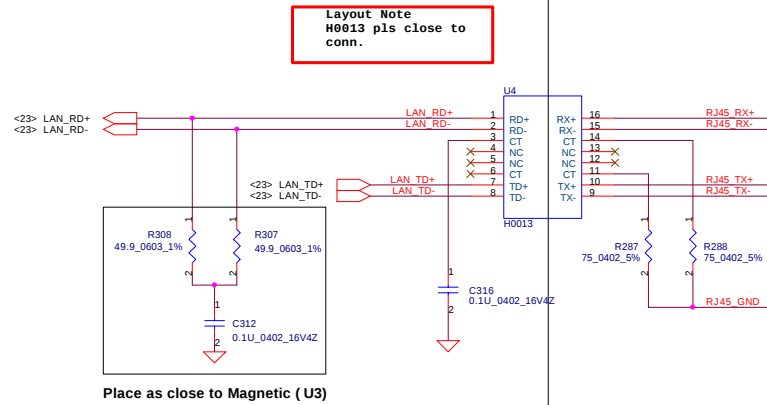
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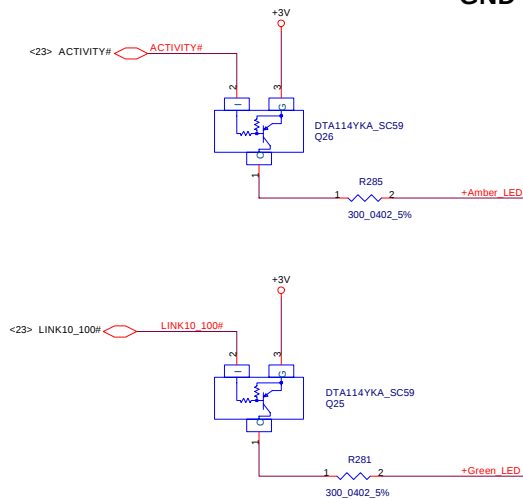
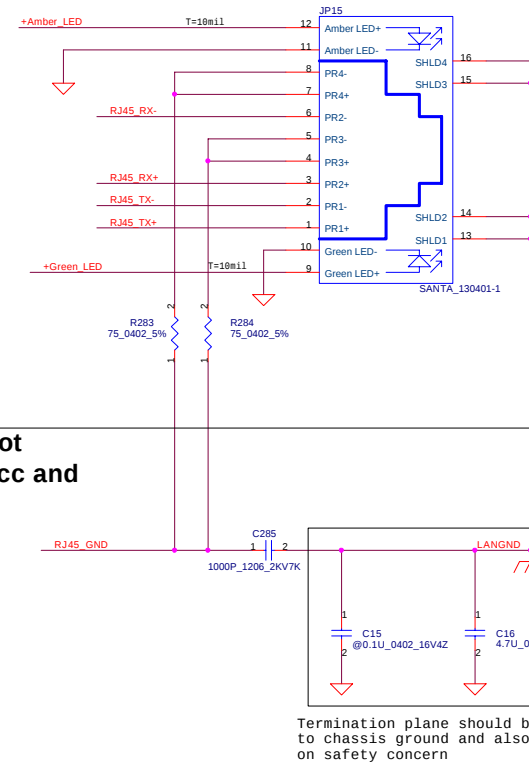
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Keep Out 40mil



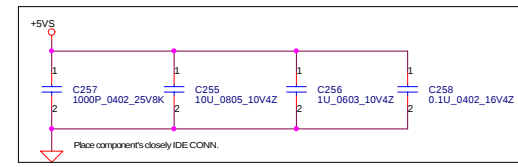
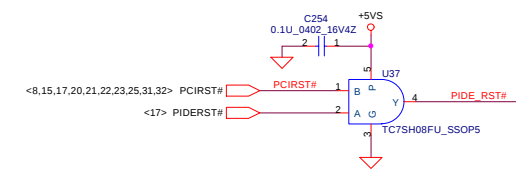
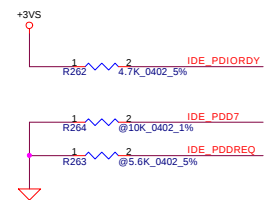
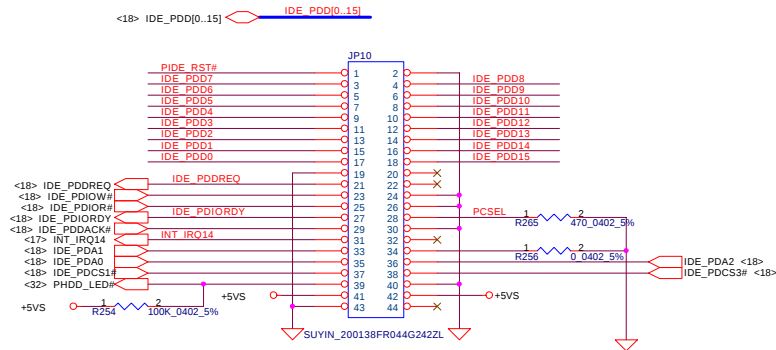
LAYOUT NOTICE: This area do not connect to power plan include Vcc and GND in any layer



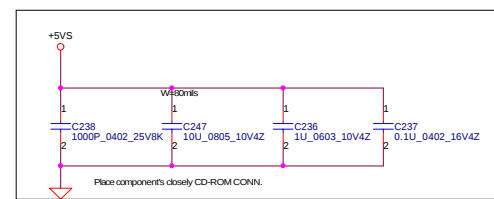
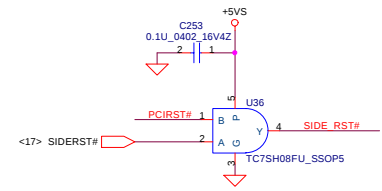
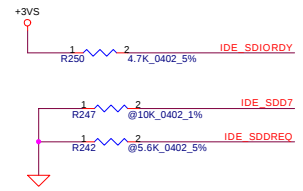
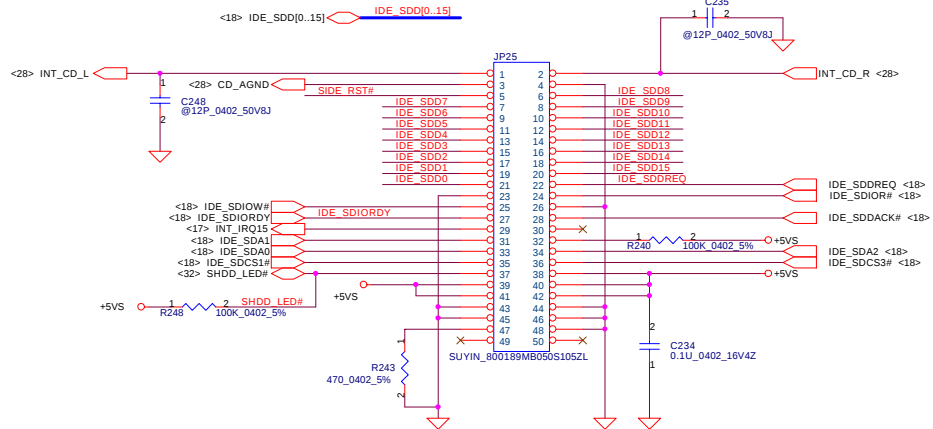
Compal Electronics, Ltd.			
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IDE Module CONN.

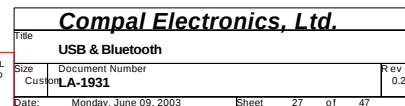
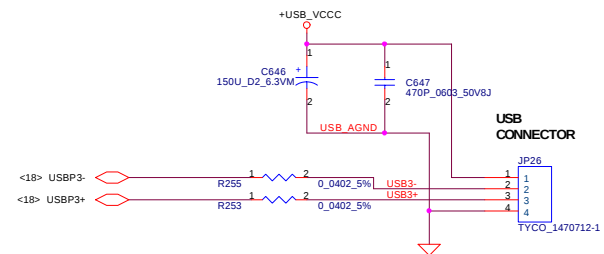
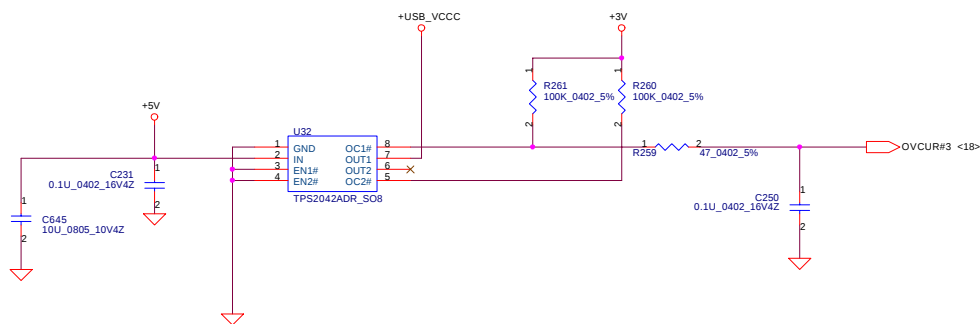


CD-ROM Module CONN.



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IDE & CD-ROM Connector			
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[illegible]

MDC Connector

The diagram illustrates the MDC Connector (JP17) with 30 pins. The connections are as follows:

- Pin 1:** Connected to +3V through resistor R66 (0.0402_5%).
- Pin 2:** Connected to +3VS through inductor L5 and capacitor CHB1608B121_0603.
- Pin 3:** Connected to +3VS_MDC.
- Pin 4:** Connected to +5VS_MDC through inductor L25 and capacitor CHB1608B121_0603.
- Pin 5:** Connected to +3VS_MDC_R through resistor R313 (10K_0402_5%).
- Pin 6:** Connected to +3VS_MDC.
- Pin 7:** Connected to IAC_SYNC.
- Pin 8:** Connected to IAC_SYNC.
- Pin 9:** Connected to IAC_SYNC.
- Pin 10:** Connected to IAC_SYNC.
- Pin 11:** Connected to IAC_SYNC.
- Pin 12:** Connected to IAC_SYNC.
- Pin 13:** Connected to IAC_SYNC.
- Pin 14:** Connected to IAC_SYNC.
- Pin 15:** Connected to IAC_SYNC.
- Pin 16:** Connected to IAC_SYNC.
- Pin 17:** Connected to IAC_SYNC.
- Pin 18:** Connected to IAC_SYNC.
- Pin 19:** Connected to IAC_SYNC.
- Pin 20:** Connected to IAC_SYNC.
- Pin 21:** Connected to IAC_SYNC.
- Pin 22:** Connected to IAC_SYNC.
- Pin 23:** Connected to IAC_SYNC.
- Pin 24:** Connected to IAC_SYNC.
- Pin 25:** Connected to IAC_SYNC.
- Pin 26:** Connected to IAC_SYNC.
- Pin 27:** Connected to IAC_SYNC.
- Pin 28:** Connected to IAC_SYNC.
- Pin 29:** Connected to IAC_SYNC.
- Pin 30:** Connected to IAC_SYNC.

Additional components and connections include:

- MD_SPK:** Signal line connected to Pin 1.
- +5VS_MDC:** Power supply line connected to Pin 4.
- +3VS_MDC_R:** Power supply line connected to Pin 5.
- +3VS_MDC:** Power supply line connected to Pin 3 and 6.
- IAC_SYNC:** Signal line connected to Pins 7-30.
- IAC_SDATA1<18>:** Signal line connected to Pin 7.
- IAC_BITCLK:** Signal line connected to Pin 7.
- AMP 3-1565120-0 30P H9MM:** Connector block connected to the bottom of the JP17 header.

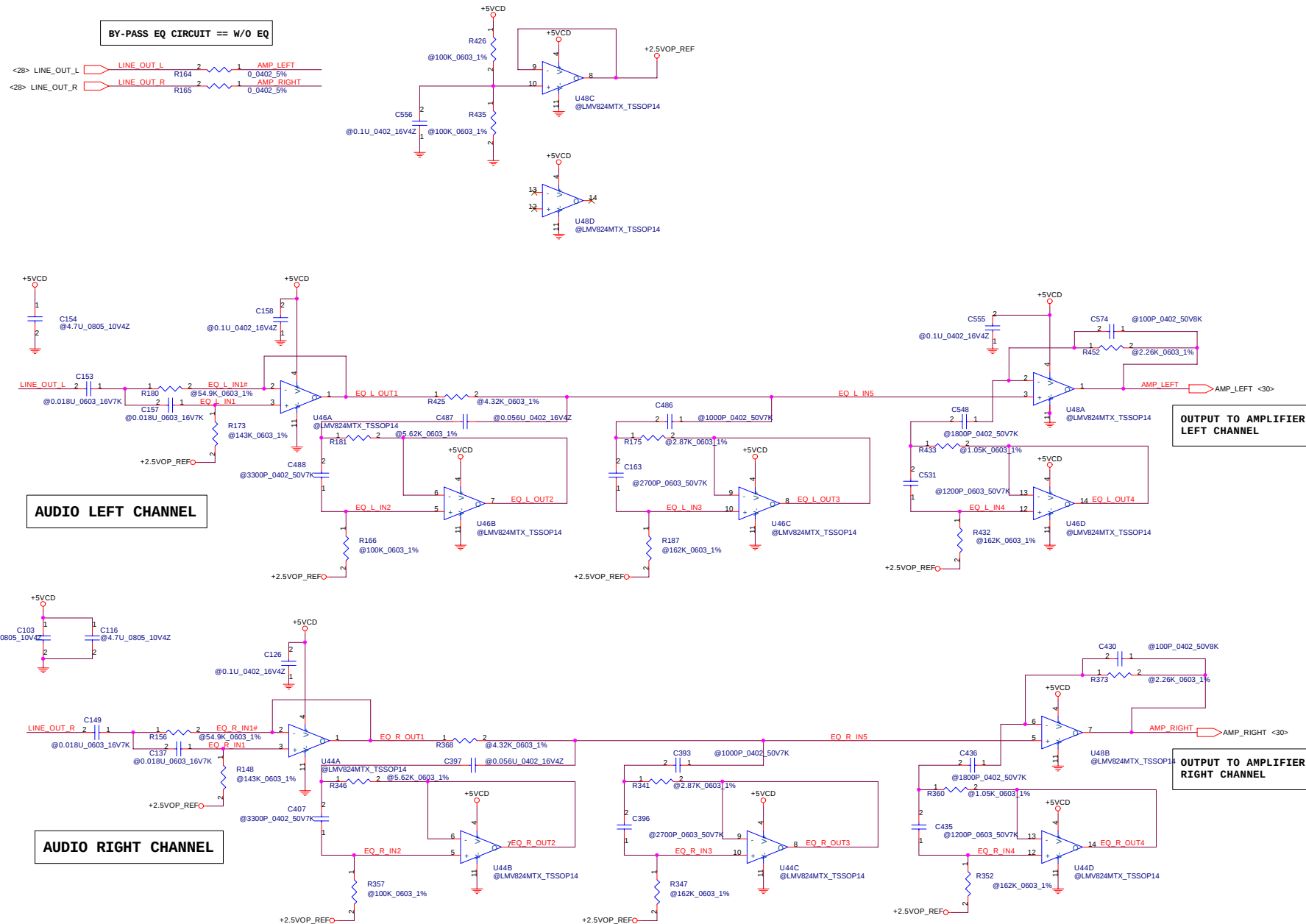
COMPAL ELECTRONICS, INC. 3000 N. 10TH AVE. SUITE 100, DENVER, CO 80202

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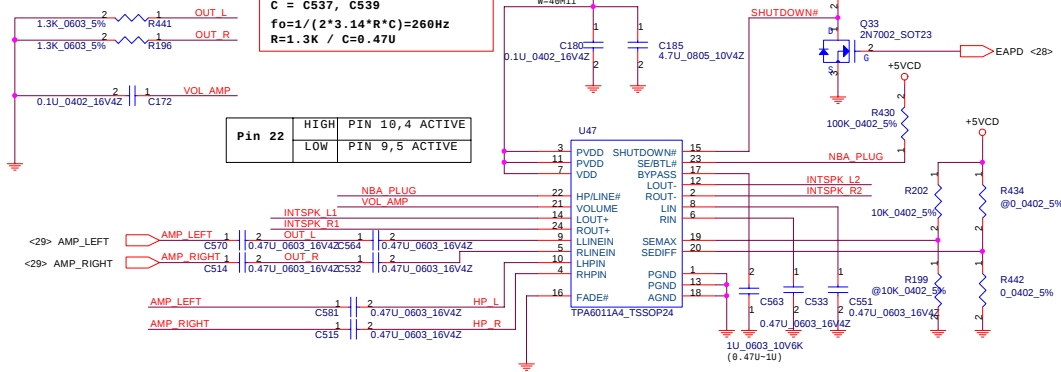
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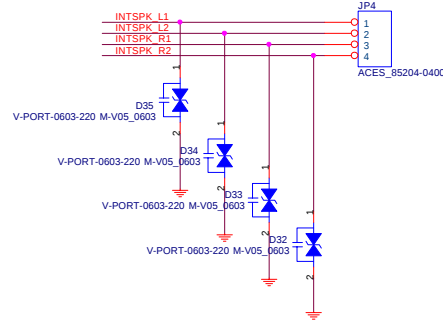
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Audio AMP

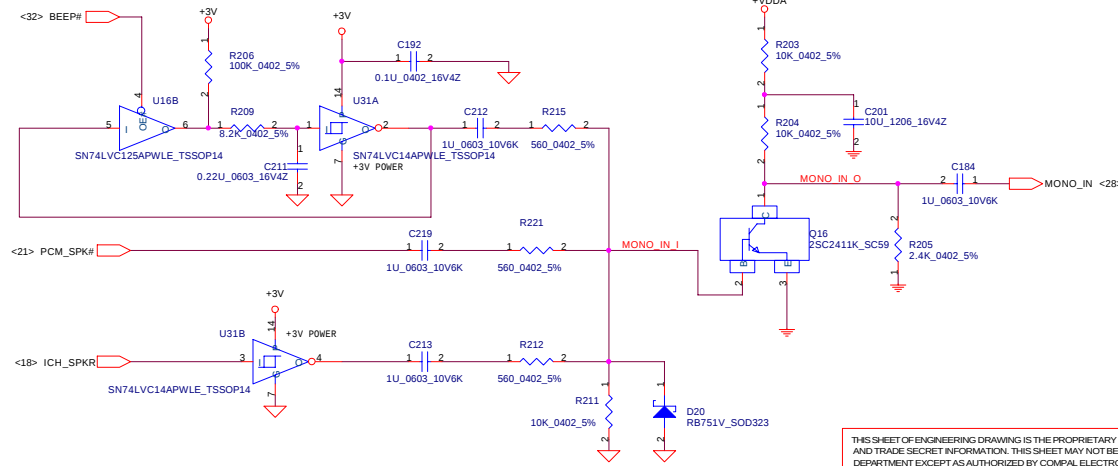
W/EQ Depop R385 & R386
C537=C539=0
W/O EQ R385=R386= 1.3K Ohm
C537=C539= 0.47U
R = R385, R386
C = C537, C539
 $f_o = 1 / (2 * 3.14 * R * C) = 260\text{Hz}$
R=1.3K / C=0.47U



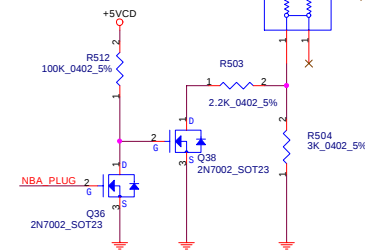
Speaker Connector



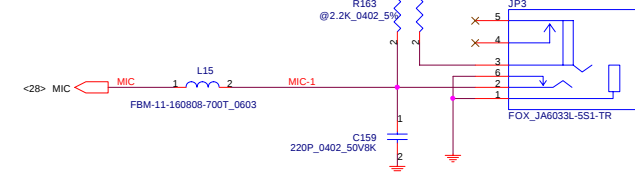
System Sound



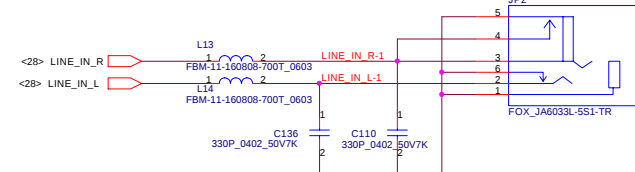
VR - A-Type



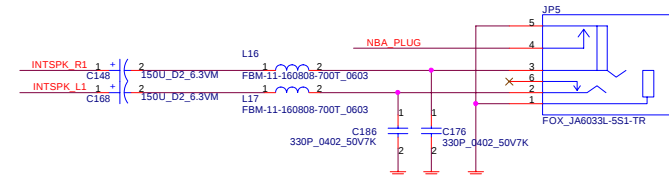
MICROPHONE IN JACK



LINE IN JACK



HEADPHONE OUT JACK



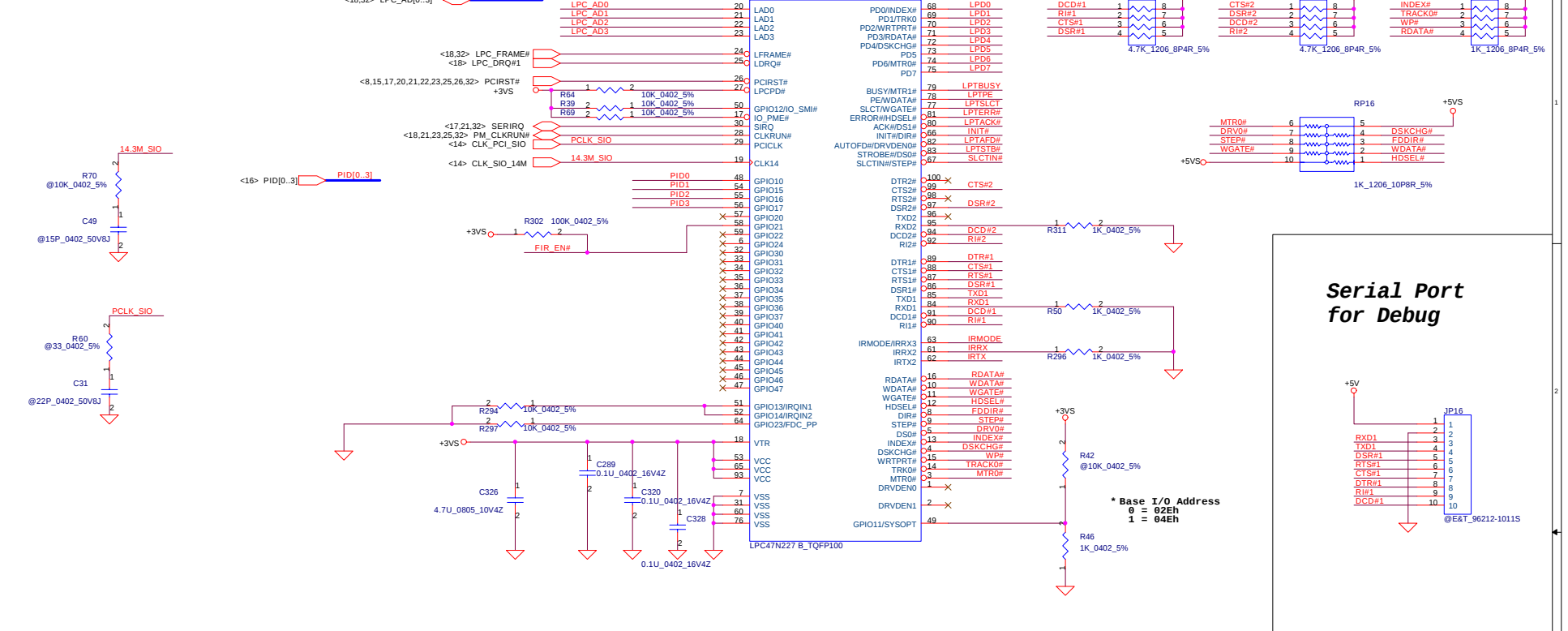
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Audio AMP & JACK

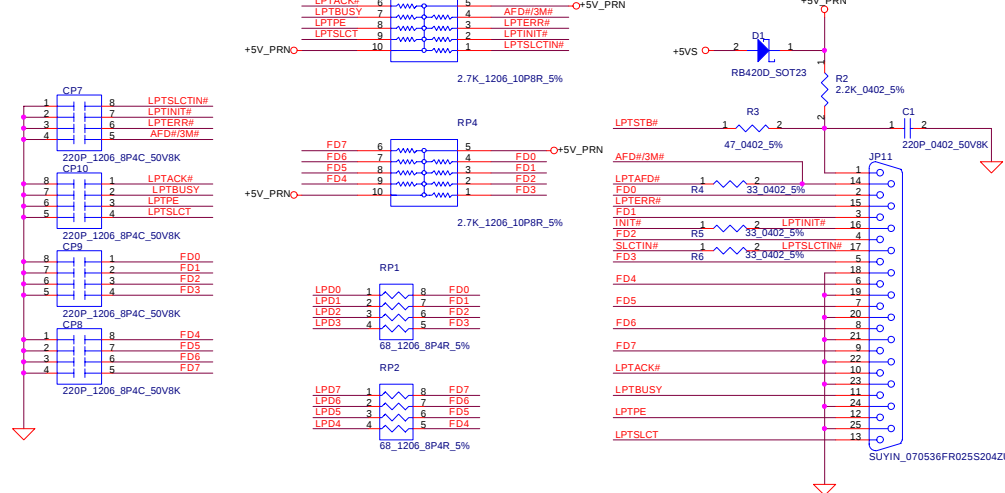
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SUPER I/O SMC FDC47N227



Parallel Port



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LPC-Super I/O

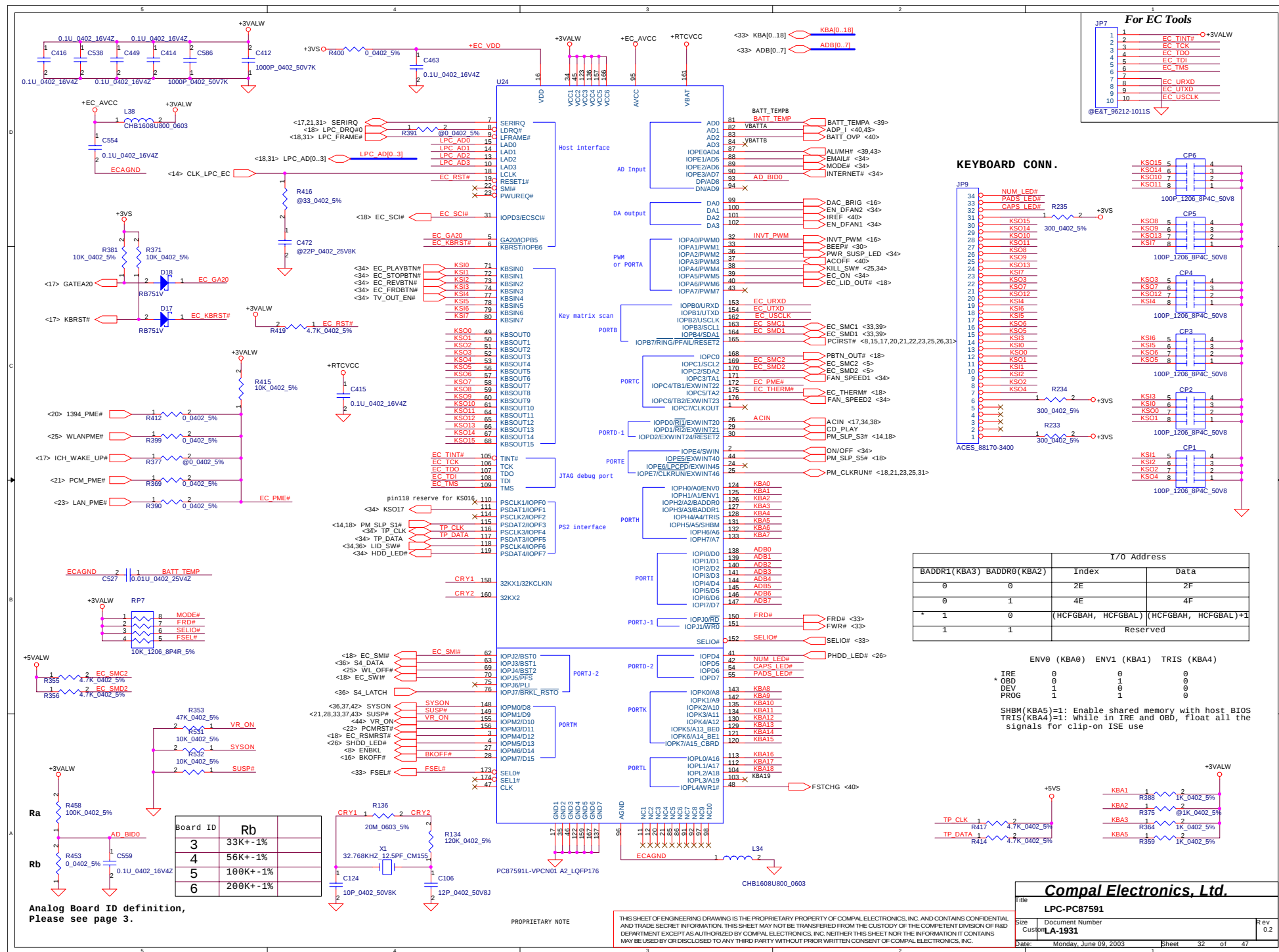
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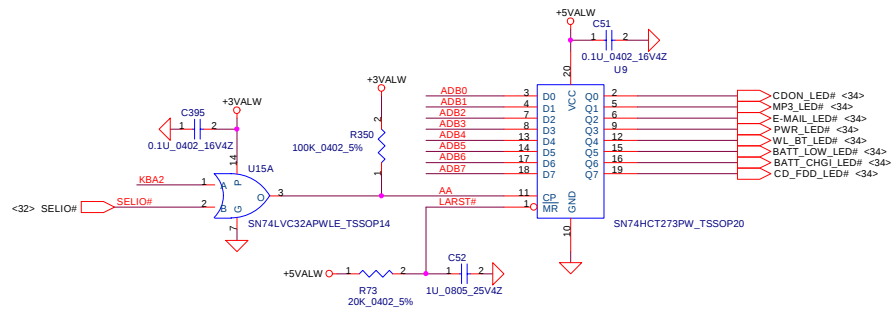
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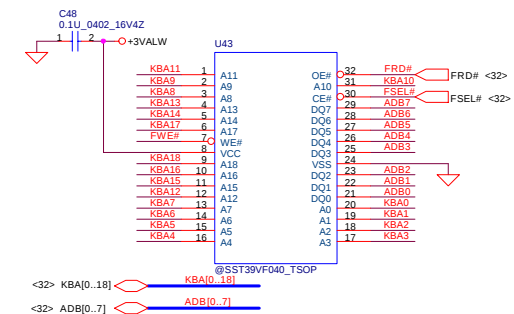
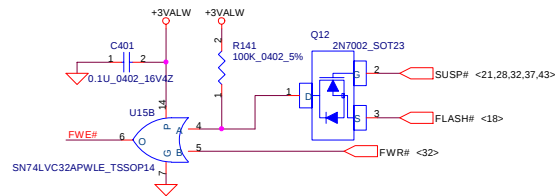
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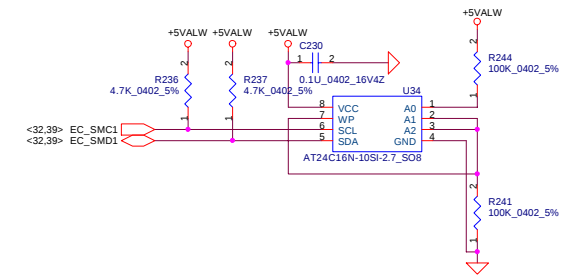
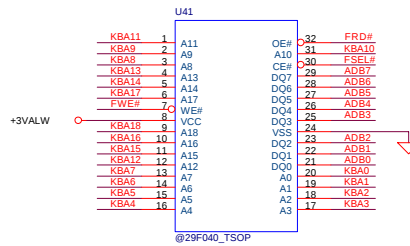
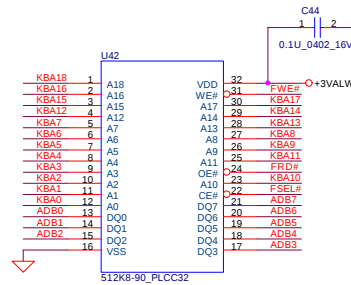




System BIOS



SMBus EEPROM



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BIOS & Ext.I/O

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SW BOARD Connector
(Top contact)

5VALW
R522
10K_0402_5%

SUSP_LED#

<32> PWR_SUSP_LED

Q43
2N7002_SOT23

<32> MODE#
<38> S10N#

+5VALW
C614
1U_0603_10V6K

+3VS
R494
1K_0402_5%

+5VALW
R499
10K_0402_5%

<32> HDD_LED#

Q35
MMBT3904_SOT23

<33> BATT_LOW_LED#
<33> BATT_CHGL_LED#
<33> CD_FDD_LED#
<33> CDON_LED#
<33> MP3_LED#
<33> E-MAIL_LED#

FAN CONN

+12VALW

C642
0.1U_0402_16V4Z

C640
0.1U_0402_16V4Z

<32> EN_DFAN1

R510
10K_0402_5%

U49A
LM358A_SO8

R514
8.2K_0402_5%

R501
100_0402_5%

C620
0.1U_0402_16V4Z

IN4148

<32> FAN_SPEED1

+3VS
R516
10K_0402_5%

FAN CONN. 2

U49B
LM358A_SO8

<32> EN_DFAN2

R509
10K_0402_5%

R511
8.2K_0402_5%

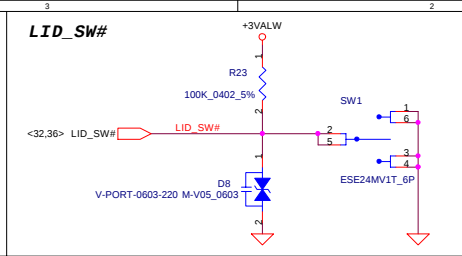
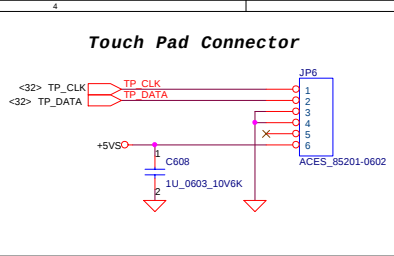
R508
100_0402_5%

C631
0.1U_0402_16V4Z

IN4148

<32> FAN_SPEED2

+3VS
R354
10K_0402_5%



Kill SWITCH

SW6

1 2 3

DS-1208_3P

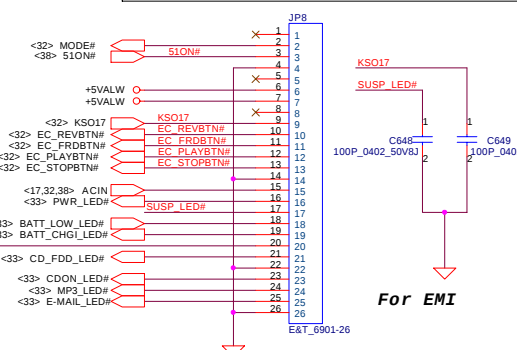
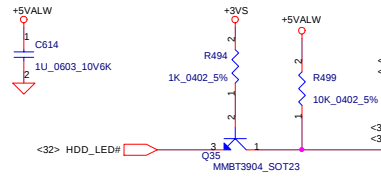
+3VVALW

R68
100K_0402_5%

KILL_SW# <25,32>

D10
V-PORT-0603-220 M-V05_0603

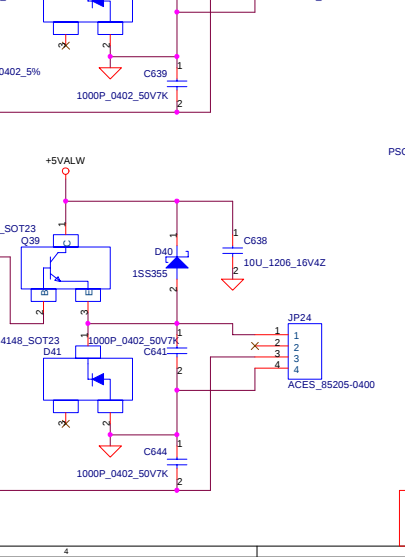
Ground



FAN_CONN

FAN CONN. 2

The schematic diagram for FAN CONN. 2 shows two fan speed control circuits. The top circuit uses an LM358A_S08 op-amp (U49B) to drive a 10K resistor (R516) connected to +3V5, with a feedback network of 100K (R508) and 0.1uF (C631) capacitors. The bottom circuit uses a similar op-amp (U49B) to drive a 10K resistor (R354) connected to +3V5, with a feedback network of 100K (R354) and 0.1uF (C631) capacitors. Both circuits are connected to a 5V supply and a 3V5 supply.



TV-OUT BUTTON

Schematic diagram of the TV-OUT button circuit. The circuit includes a KSO17 crystal connected to an SMT1-05_4P SW5 switch. The switch is controlled by a 50V8J signal. The output of the switch is connected to a TV_OUT_EN# pin, which is also connected to a D2 diode (V-PORT-0603-220 M-V05_0603) and a ground symbol.

WIRELESS ACTIVE AMB LED

HP HSMG-C170 AMB 8895

D11

R109

+3VALW

120_0402_5%

Q4

DTA114YKA_SOT23

18K

WL_BT_LED#

WL_BT_LED#

2

Internet Button

The schematic diagram for the Internet Button circuit shows the following components and connections:

- Power Supply:** A 3V3V supply is connected to the circuit.
- Resistor:** A 0.0603_5% resistor (R275) is connected in series with the 3V3V supply.
- MOSFET:** A Q22 MOSFET is used as a switch, controlled by the 3V3V supply.
- Diodes:** Two 1N4148 diodes (D28 and D25) are used for signal conditioning.
- Switch:** An SMT1-05_4P SW3 switch is used to manually trigger the circuit.
- Output:** The circuit output is connected to a PSOT24C_SOT23 D26 component, which is then connected to a 3V3V supply.

User Button & E-MAIL SW

The diagram illustrates the internal wiring of a user button and email switch. It features a 4-pin connector with the following connections:

- Pin 1:** Labeled **EMAIL#**, connected to a 100K 0402 5% resistor and the input of a 1N4148_SOT23 diode (D3).
- Pin 2:** Labeled **INTERNET#**, connected to a 100K 0402 5% resistor and the input of a 1N4148_SOT23 diode (D4).
- Pin 3:** Connected to a 1N4148_SOT23 diode (D3) and a PSOT24C_SOT23 component (D5).
- Pin 4:** Connected to a PSOT24C_SOT23 component (D5) and a switch (SW4).

The circuit is powered by a 3.3V supply and ground. The components are labeled as follows:

- 100K 0402 5%:** Two resistors connected to pins 2 and 3.
- 1N4148_SOT23:** Two diodes, D3 and D4.
- PSOT24C_SOT23:** A component labeled D5.
- SW4:** A switch connected to pin 1 and pin 2.

[illegible]

RTC BATT

ML1220T13RE

+RTCBATT

C224
0.1u_0402_16V4Z

D21
BAS40-04_SOT23

+RTCCVCC

C222
0.1u_0402_16V4Z

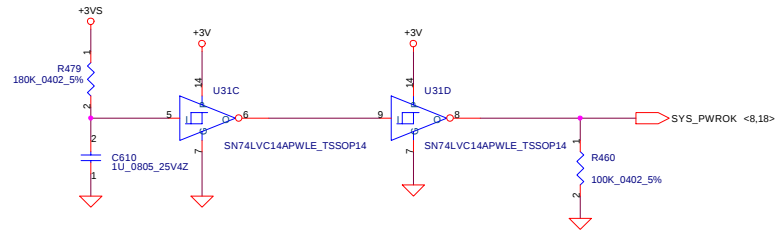
+CHGRTCT

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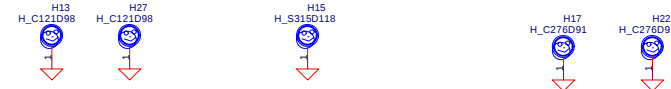
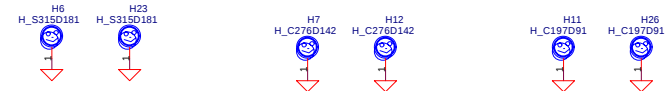
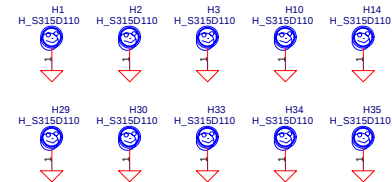
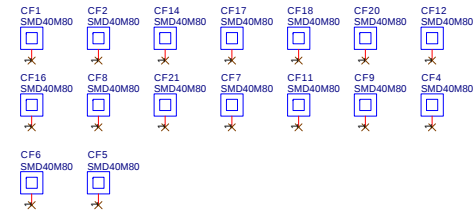
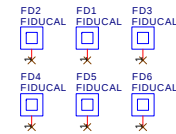
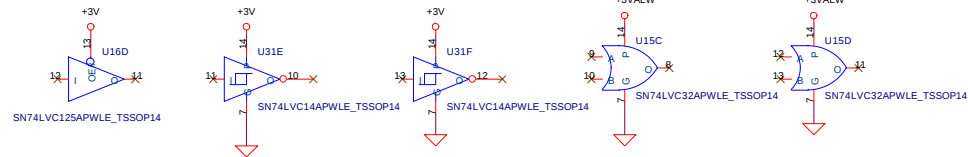
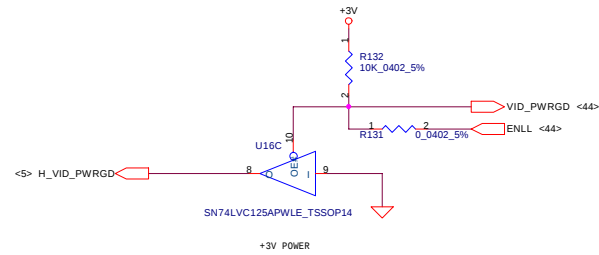
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Power Good Circuit



VID_PWRGD

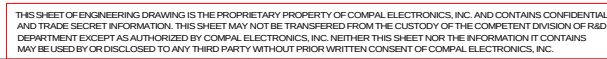


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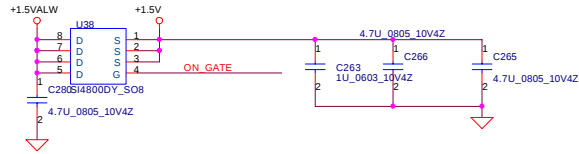
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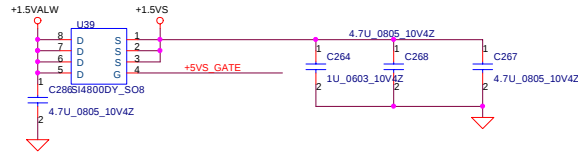
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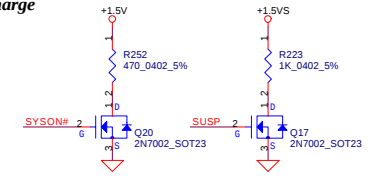
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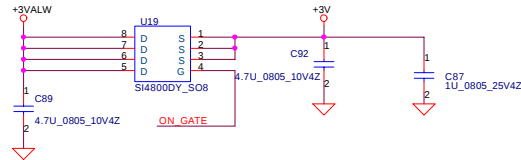
+1.5VALW To +1.5VS Transfer



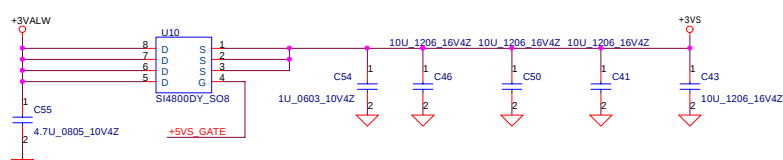
+1.5V & +1.5VS Discharge



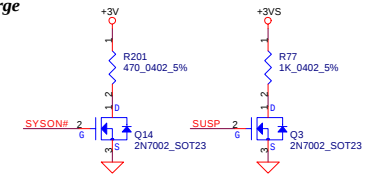
+3VALW To +3V Transfer



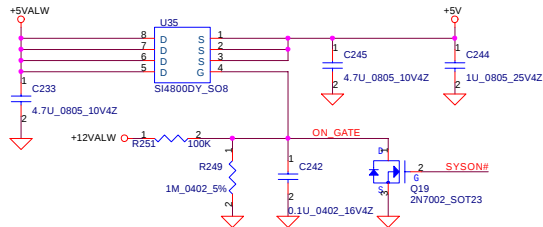
+3VALW To +3VS Transfer



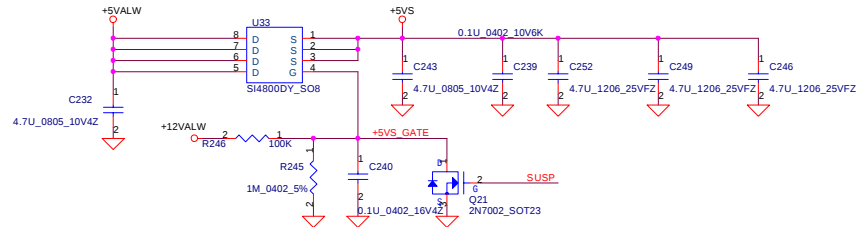
+3V & +3VS Discharge



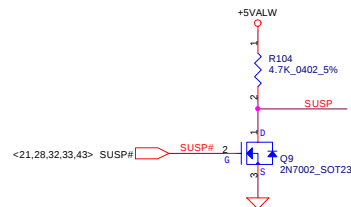
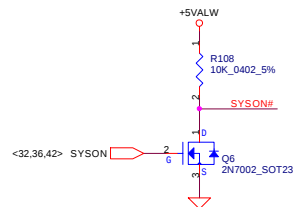
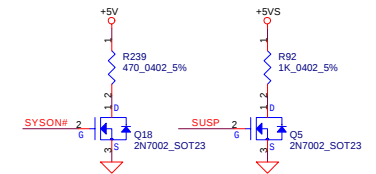
+5VALW To +5V Transfer



+5VALW To +5VS Transfer

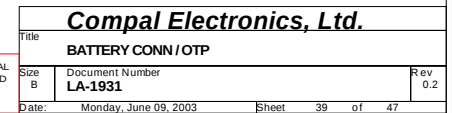
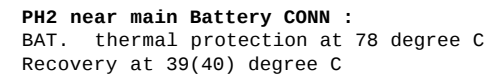
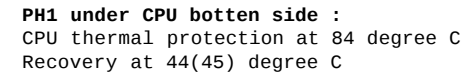


+5V & +5VS Discharge

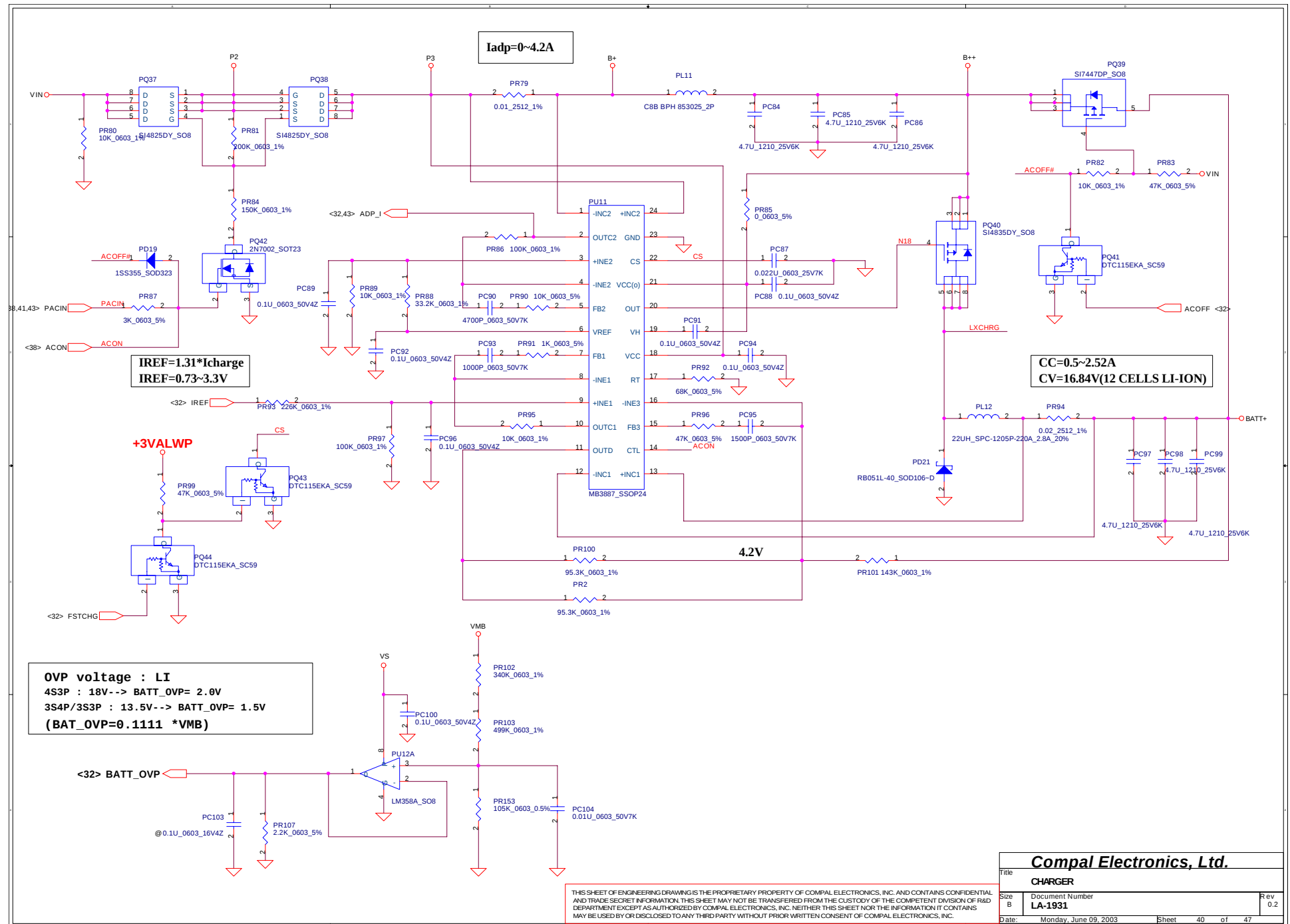


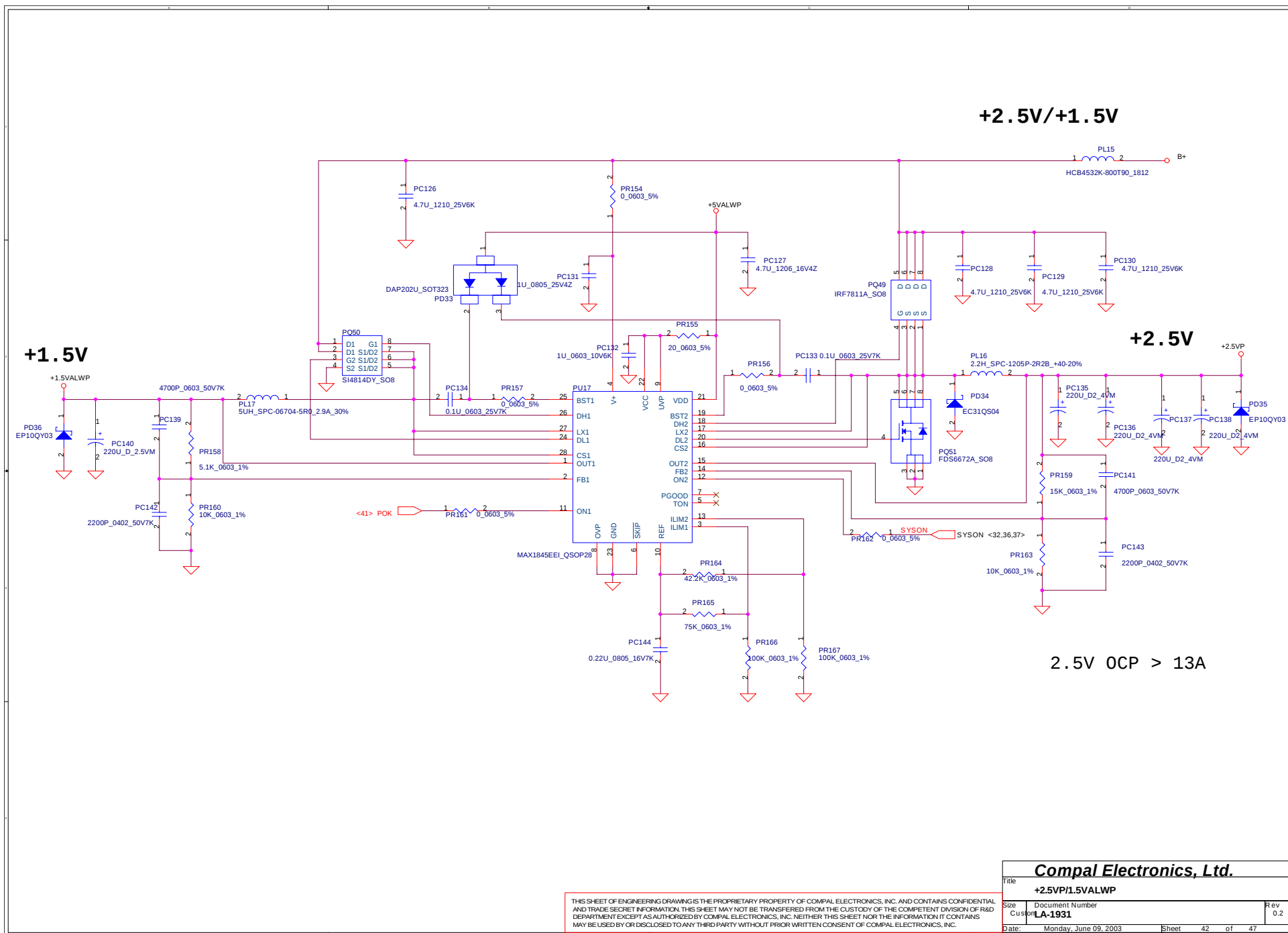
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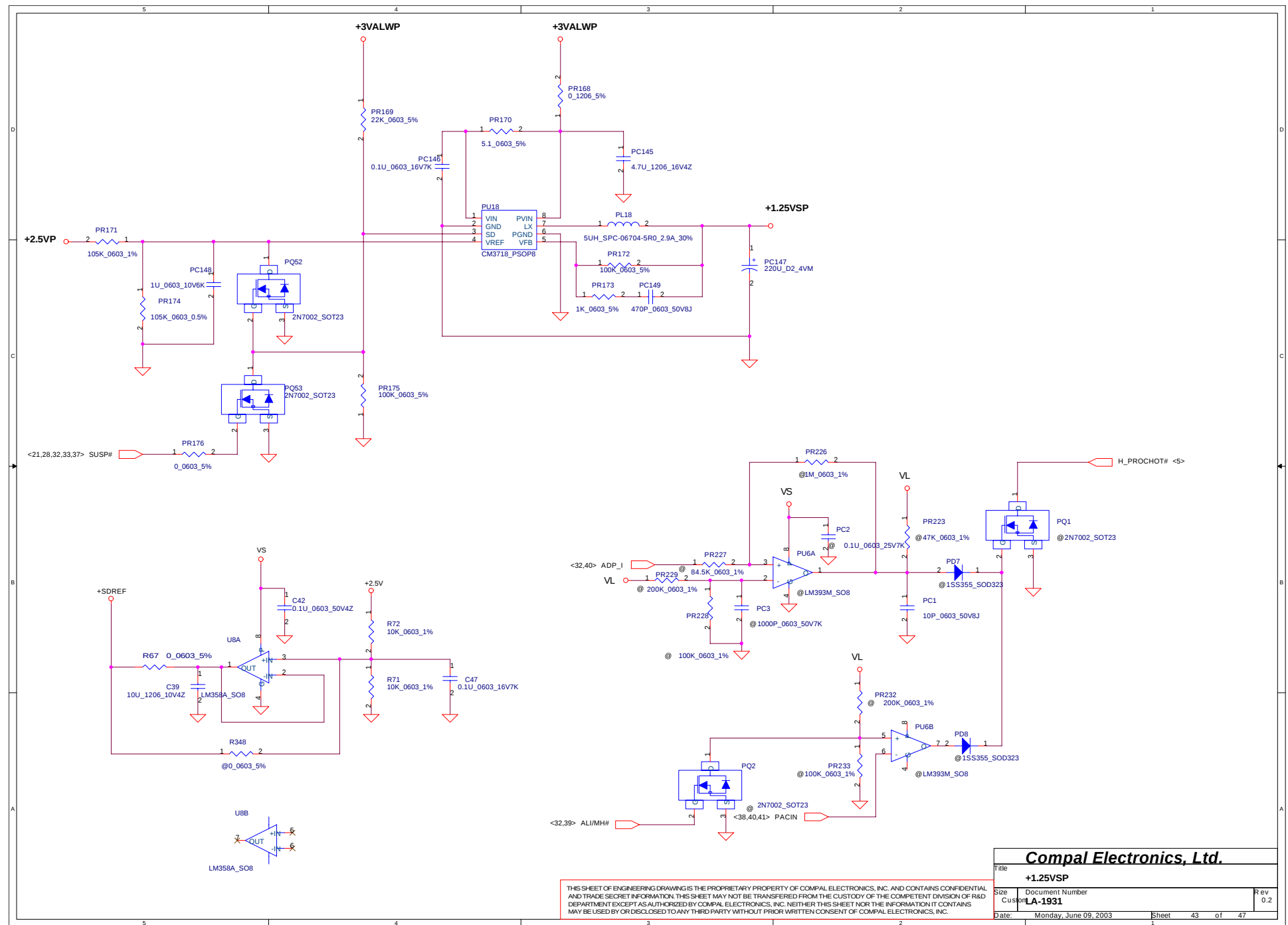
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DC/DC Interface			
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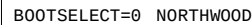
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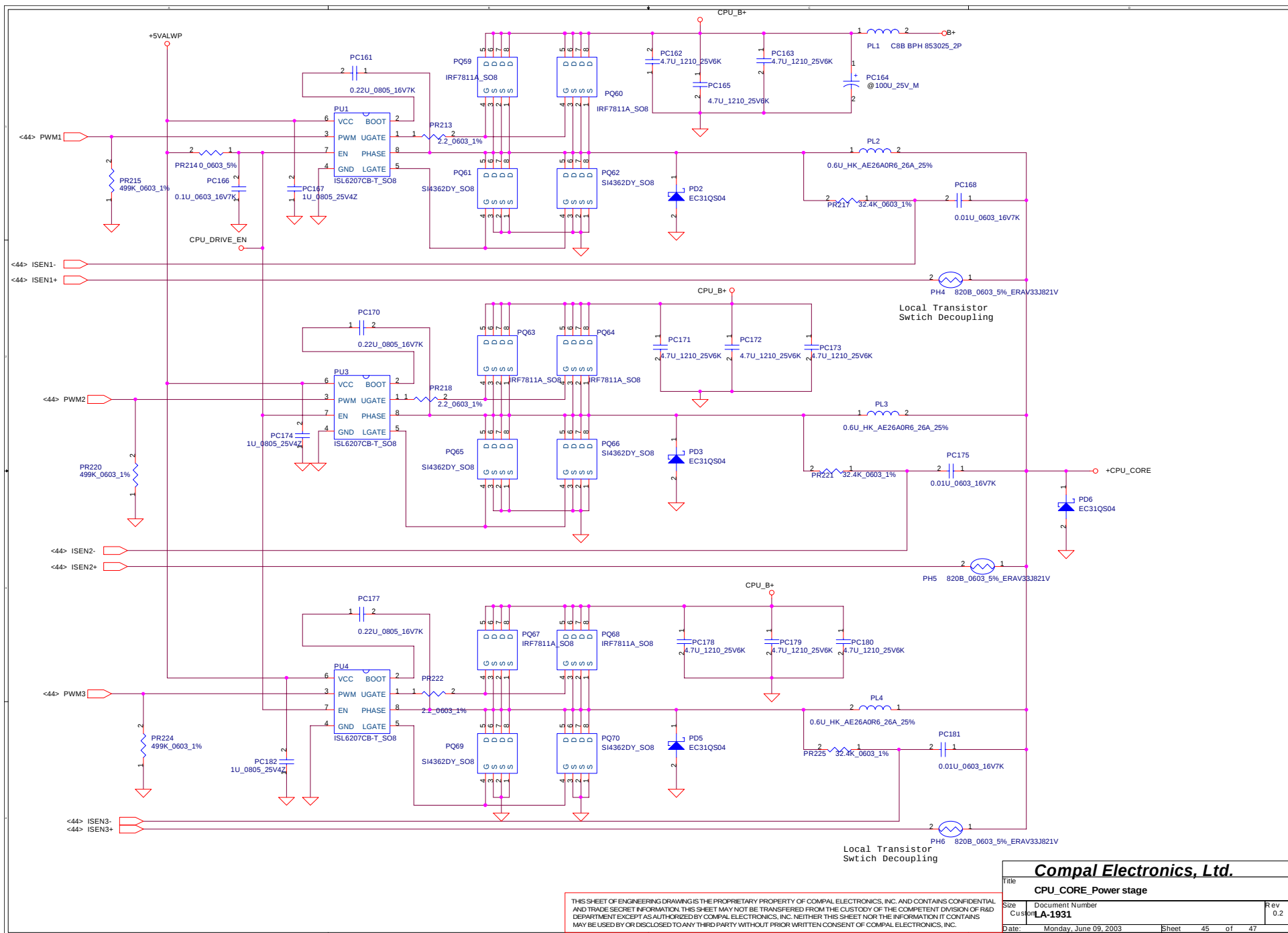




#7	GND	#11	REF	#33	EN	#38	OVP
#9	TCOMP	#14	IDROOP	#35	GND	#40	GND
#10	DAC	#18	RGND	#37	GND		



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CPU_CORE Power stage		
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Date	Page	Description
04/10	21	Delete Power interface short line.
04/13	21, 22	Change Card Bus controller as one slote CB1410
	11, 12	Swap RAM data signals.
04/16	29	Add EQ circuit
	43	Add throtoutling circuit.
	26, 31	Add FIR and Remove SW DJ cicuit
04/24	17	Add R569 and R570 for Layout Request. Move Signal IRQE#~H# from RP92 to RP91 and del RP92.
	14	CLK-GEN. pin 1(VDD_REF) and pin 46(VDD_CPU_0) change power plan as +3V_VDD. Suggestion from ICS
		C249 and C251 change power plane as +3VDD
04/25	45	PL4 swap pin1 and pin2.
	6	Change CPU Decoupling CAP. from 22U_1210_6.3V6M to 22U_1206_6.3V6M (H=1.6)
	32	1. EC GPIO signal HDD_LED# move from pin114 to pin119. 2. Add signal PM_SLP_S1# on EC GPIO pin115.
	28	Q44 for +5VCD change part name as U55
04/28	8	Del R73, cause it duplicate pull high.
	27	Change C478 and C488 from 150U to 10U
	36	Change R480 from 560K to 620K Ohm
	4	Add R571 for BOOTSELECT
	5	Add R573 for OPTIMIZED/COMPAT#
	18	Add R572 for signal PM DPRSLPVR
04/29		Rename from Layout
04/30	33	R73 0402 -> 0603 and C52 0805 -> 0603
	16	C2, C5, C259, C3, C4, C6, C260, C261 and C262 Link CIS.
	5	Thermal Sensor : Del R62, R61 8.2K-->200Ohm and power +5VS -> +3VS, C27 value 0.1U -> 1U, Sensor power rout direction : +3VS -> R61 -> C27.1 -> U6.1
	17	Add Q40 and Q41, R517 and R518 for SMBus isolate solution.
05/01	8	Change CRT_HSYNC -> INTCRT_HSYNC and CRT_VSYNC -> INTCRT_VSYNC on MGCH terminal.
05/02	33	Remove dummy net on SUSP#.
	16	R28, C277, C278 and C279 modify P/N for CIS link
	17	C215 and C217 modify P/N for CIS link
	22	C145 modify P/N for CIS link
	20	Remove dummy net on XI
	14	R83 and R94 modify P/N for CIS link
05/03	32	CP4 pin2 add connected to GND
05/05	42	PR151 pin1 SYSON signal --> MAINPWON
	8	Swap U26.B6 (INTDDCDA) and U26.G9 (INTDDCCK) --> U26.B6 (INTDDCCK) and U26.G9 (INTDDCDA)
	9	+SDREF circuit move to page 44
	6	Modify Cap.s location same with Layout
	14	Change R129 net from PM_SLP_S3# to PM_SLP_S1#
	16	Add R519 and R520 for EC protect
05/06	20	EEDI_LAN --> EEDI_1394; EECK_LAN --> EECK_1394
	27	Remove R26. Delete USBEN# and U3.3, U3.4, U32.3 and U32.4 connect to GND. Delete R30, R279, R258 and R257. Change C273, C284 and C646 220U -->150U.
	42	PR151 pin1 SYSON signal --> POK; PU10 pin 11 output POK.
	5	R324 size 0603 -> 0805
	32	U24.175 ATF_INT# --> EC_THERM#
05/07	28	Add L42 between GND and AGND by EMI request.
	17	R408, remove @ for Intel comment.
	5	R56 60.4_0603_1% --> 51.1_0603_1%; R59 102_0603_1% -> 86.6_0603_1%
05/08	35	H19 GNDA -> GND; H31 GND -> GNDA
	37	C242 0.01U -> 0.1U.
	11	JP21 DDR-SO-DIMM link with CIS.
	29	De-pop EQ components, add @ symbol on components.

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Date	Page	Description
05/12	35	Change H31 GND --> AGND and H19 AGND --> GND
	37	R104 and R108 power plane changed, +3VALW --> +5VALW
05/29	40	Change PR100 47.5K-->95.3K
		PR100 47.5K-->95.3K;PQ37,PQ38,PQ39 SI4835DY-->SI4825DY
		PR79 0.015-->0.01; PR86 10K-->100K ;PR90 4.7K-->10K; PR88 29.4K-->33.2K
		Add PR2 95.3K
	38	Change PCN1 90W-->120W
	20	U29 Pin 37 pull up with 4.7K Ohm --> U29 Pin 43
		change X4 footprint same as X2
	16	Add Protect circuit for EC (Add D42, D43 ,D44 and R521)
	32	PWR_SUSP_LED# --> PWR_SUSP_LED
	34	Add reverse circuit for PWR_SUSP_LED (Add Q43 and R522).
	23	change Y2 footprint same as X2
	36	change J1 ~ J6 footprint from JUMP_2MM to 2MM
05/30	35	Add H41 and change H13 H27 size.
06/02	38	Change PL14 value
	39	Change PL13 value
	45	Change PL1 value
	40	Change PQ39 and PL11 value
	11	Add R523, R524, R525 and R526, Del R515
	12	Add R527, R528, R529 and R530
06/03	6	Delete C281, C287, C300, C309, C317, C324, C327 and C330.
06/05	34	Add C648 and C649 for EMI request
	32	Add R531 and R532 for EC floating issue
	8	Add R533 for DVO device detect

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