Compal Confidential

Fortworth20 EDW10 Schematic Document

Intel Protability Processor with ATi RC300ML + IXP150

2004-05-26

REV: 1.0

Compal Electronics, Inc.		
Title: Cover Sheet		
Size: B	Document Number: LA-2301	Rev: 1.0
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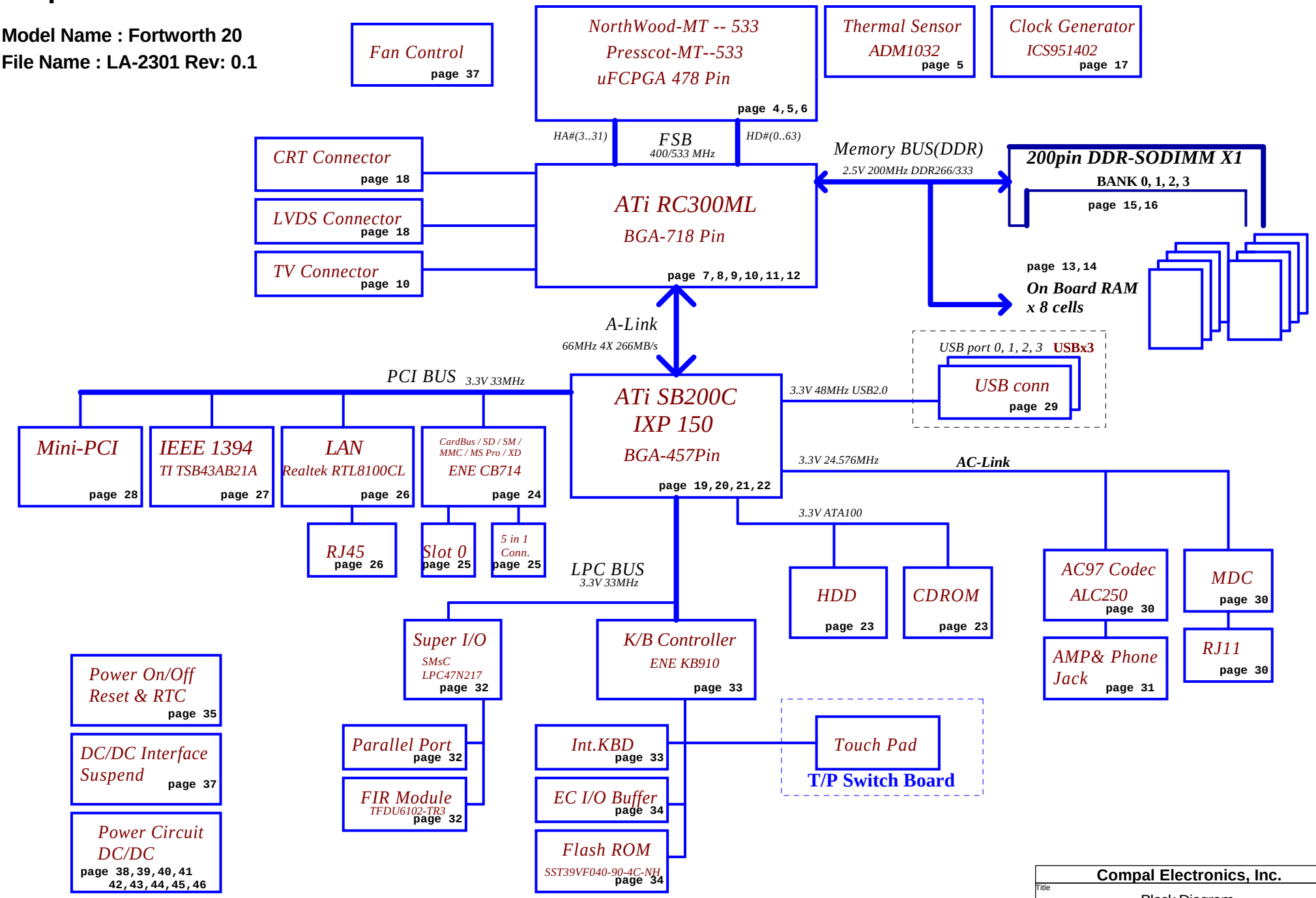
Compal confidential

Model Name : Fortworth 20
File Name : LA-2301 Rev: 0.1

Block Diagram



Compal Electronics, Inc.		
Title: Block Diagram		
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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_VID	1.2V rail for Processor VID	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VALW	2.5V always on power rail	ON	ON*	ON*
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
NB Internal VGA	N/A	N/A	A
1394	AD16	0	A
LAN	AD19	1	D
CARD BUS	AD20	2	A
5 in 1	AD20	2	B
Mini-PCI	AD18	3	C/D

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16)	1010 000X b

EC SM Bus2 address

Device	Address
ADM1032	1001 100X b
ALC250	0000 000X b

I2C / SMBUS ADDRESSING

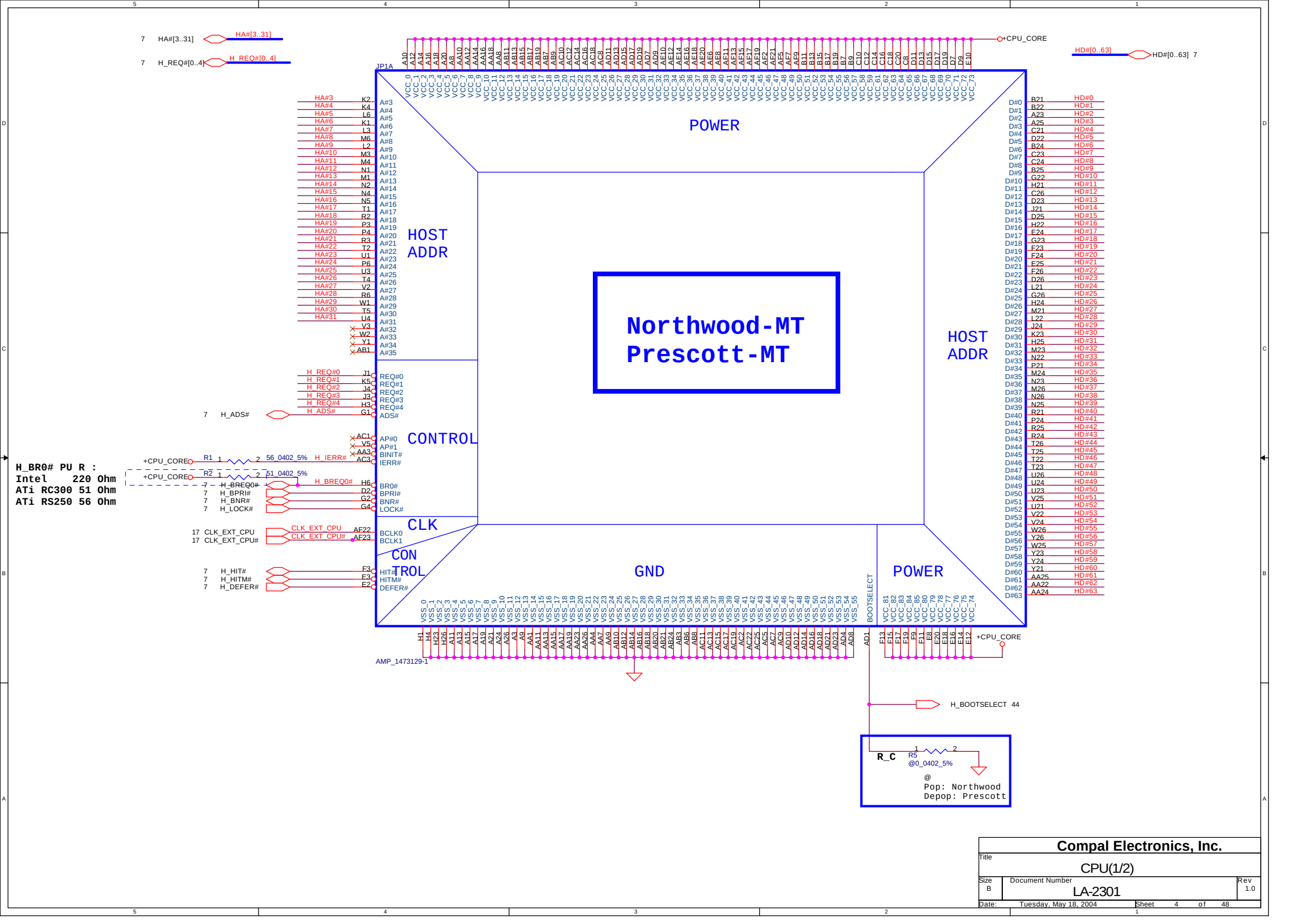
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 1 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 X

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	



H_BR0# PU R :
Intel 220 Ohm
ATi RC300 51 Ohm
ATi RS250 56 Ohm

Compal Electronics, Inc.		
Title: CPU(1/2)		
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Northwood-MT
Prescott-MT

GTL Reference Voltage

1. < 1.5" from the CPU Ball.
2. 220P cap. has to be closed to the ball as possible.
3. Intel: 0.63VCC.
   ATi: 0.66VCC.

Pop: Northwood Imp: 50 Ohm
Depop: Prescott Imp:60 Ohm

for mobile CPU

Intel 852GME RDDP 560hm.
ATi RC300 510hm
ATi RS250 56 Ohm

R25 ->
Pop: Prescott
Depop: Northwood

width= 10mil

51.1 Ohm for Northwood,
61.9 Ohm for Prescott

Place within 1.5" from CPU

CPU Temperature Sensor

ADM1032ARM_RM8

Compal Electronics, Inc.

Title	CPU(2/2)	
Size B	Document Number LA-2301	Rev 1.0
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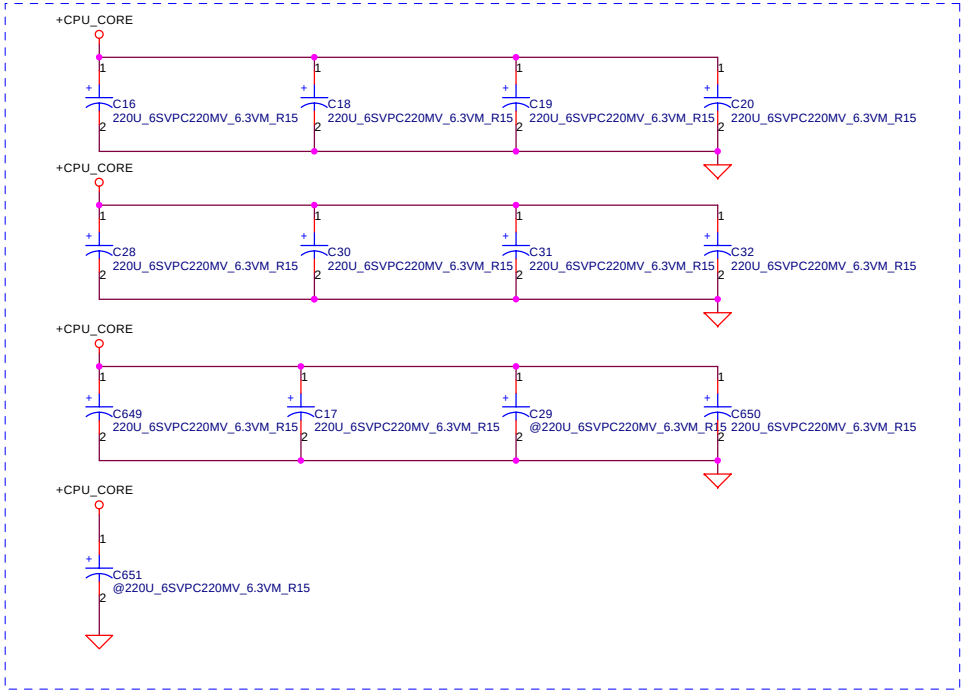
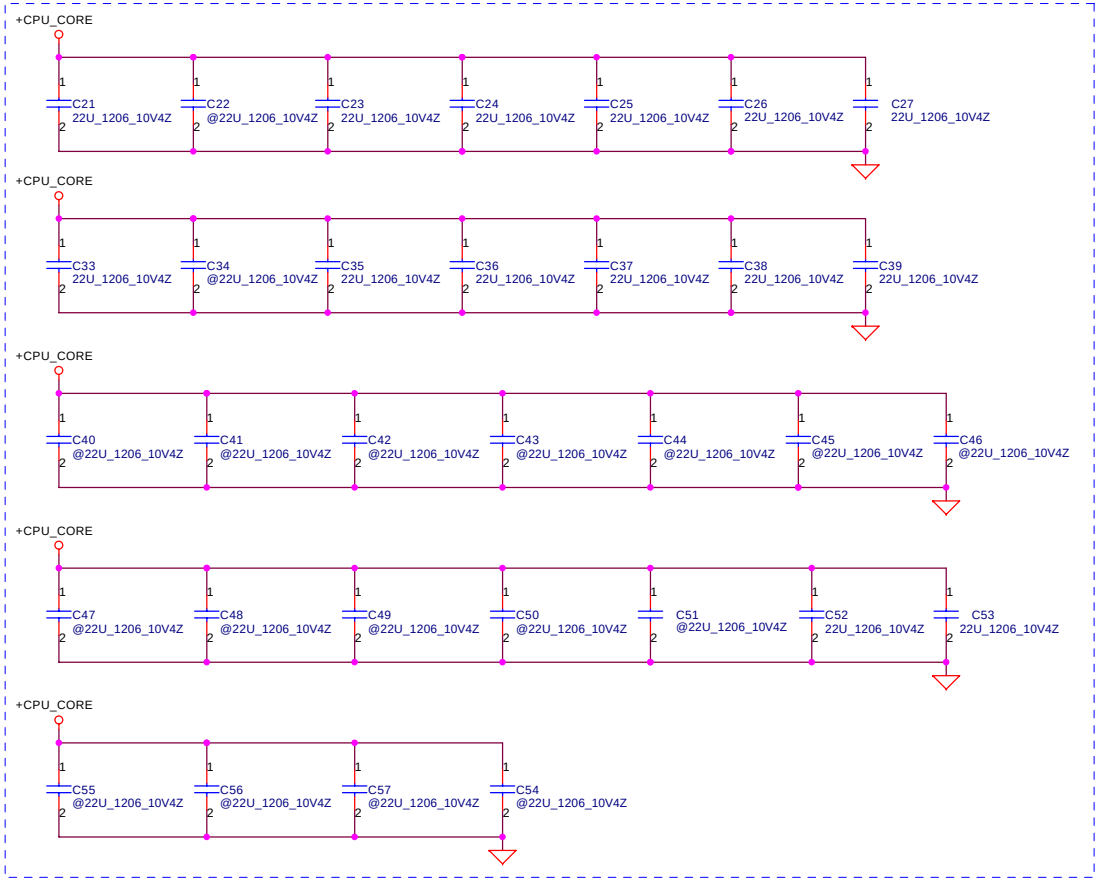
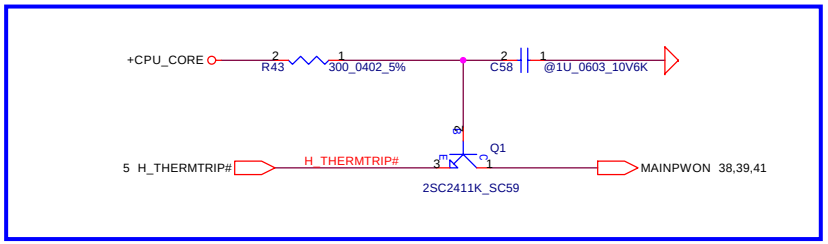




Layout note :

Place close to CPU power and ground pin as possible (<1inch)

Sanyo : SGA27221300 (220uF, 13m Ohm)



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Title: CPU Decoupling		
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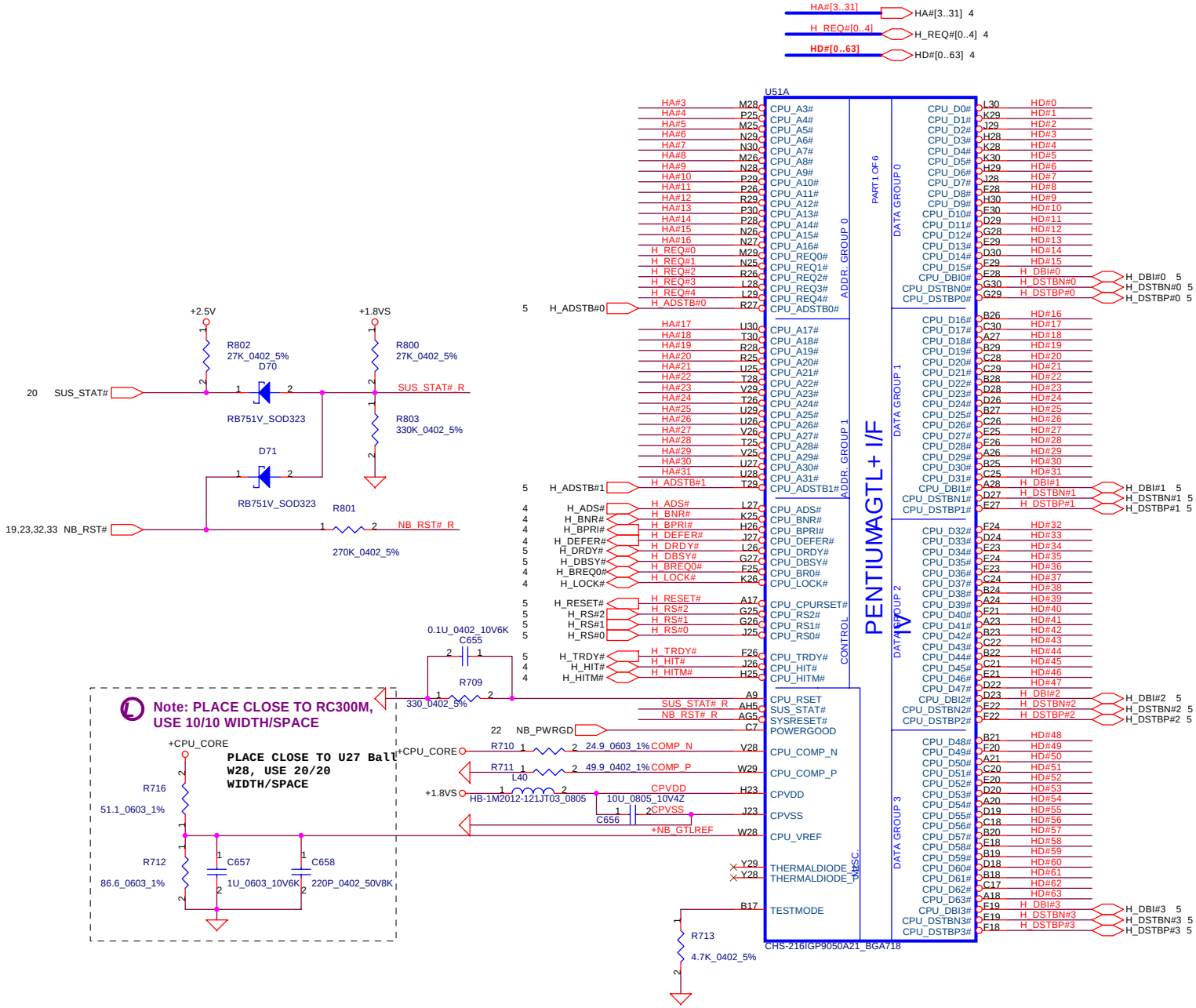

Compal Electronics, Inc.			
Title: ATi RC300ML-HOST(1/5)			
Size: B	Document Number: LA-2301		Rev: 1.0
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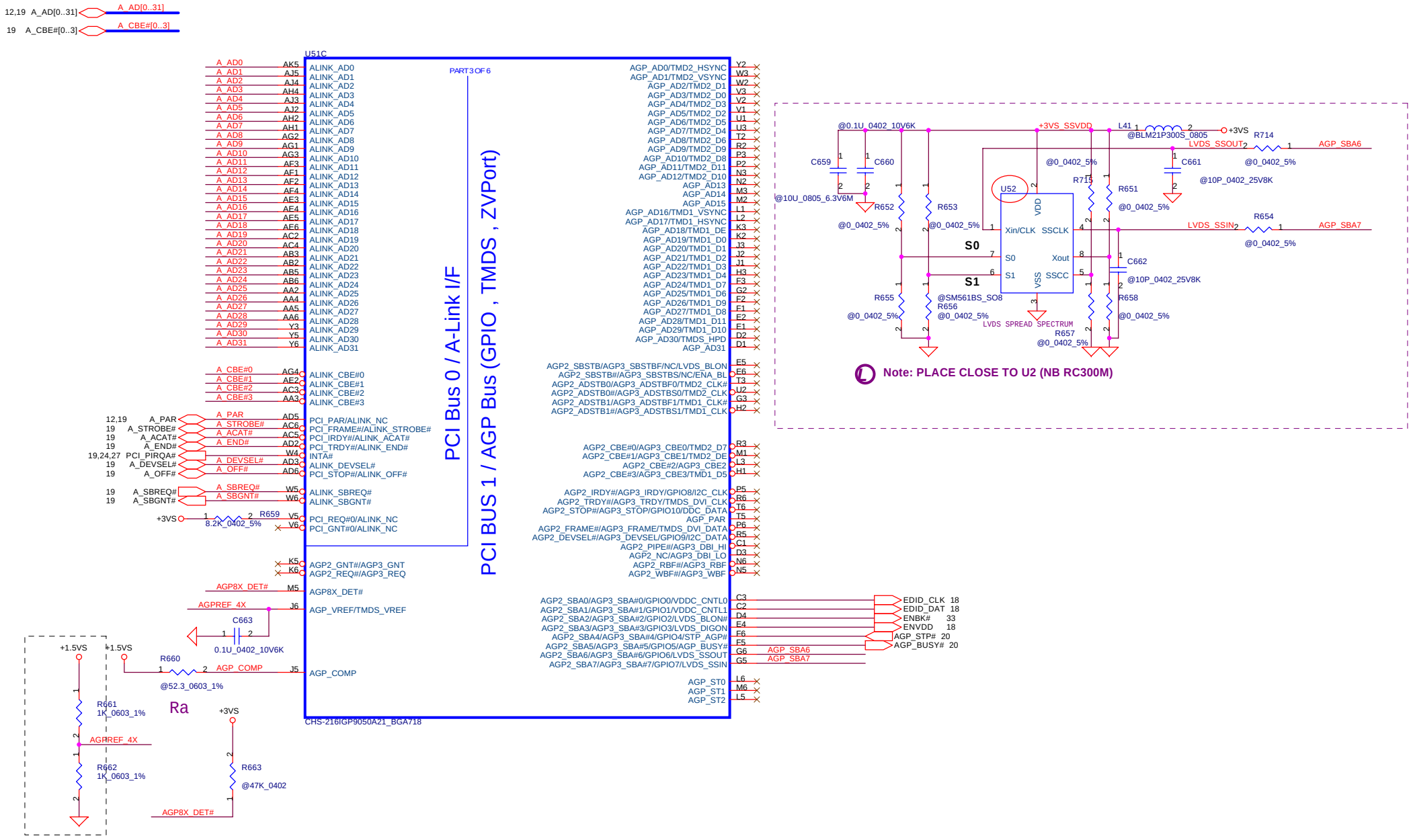

Compal Electronics, Inc.		
Title: ATi RC300ML-A-LINK/AGP(2/5)		
Size: Custom	Document Number: LA-2301	Rev: 1.0
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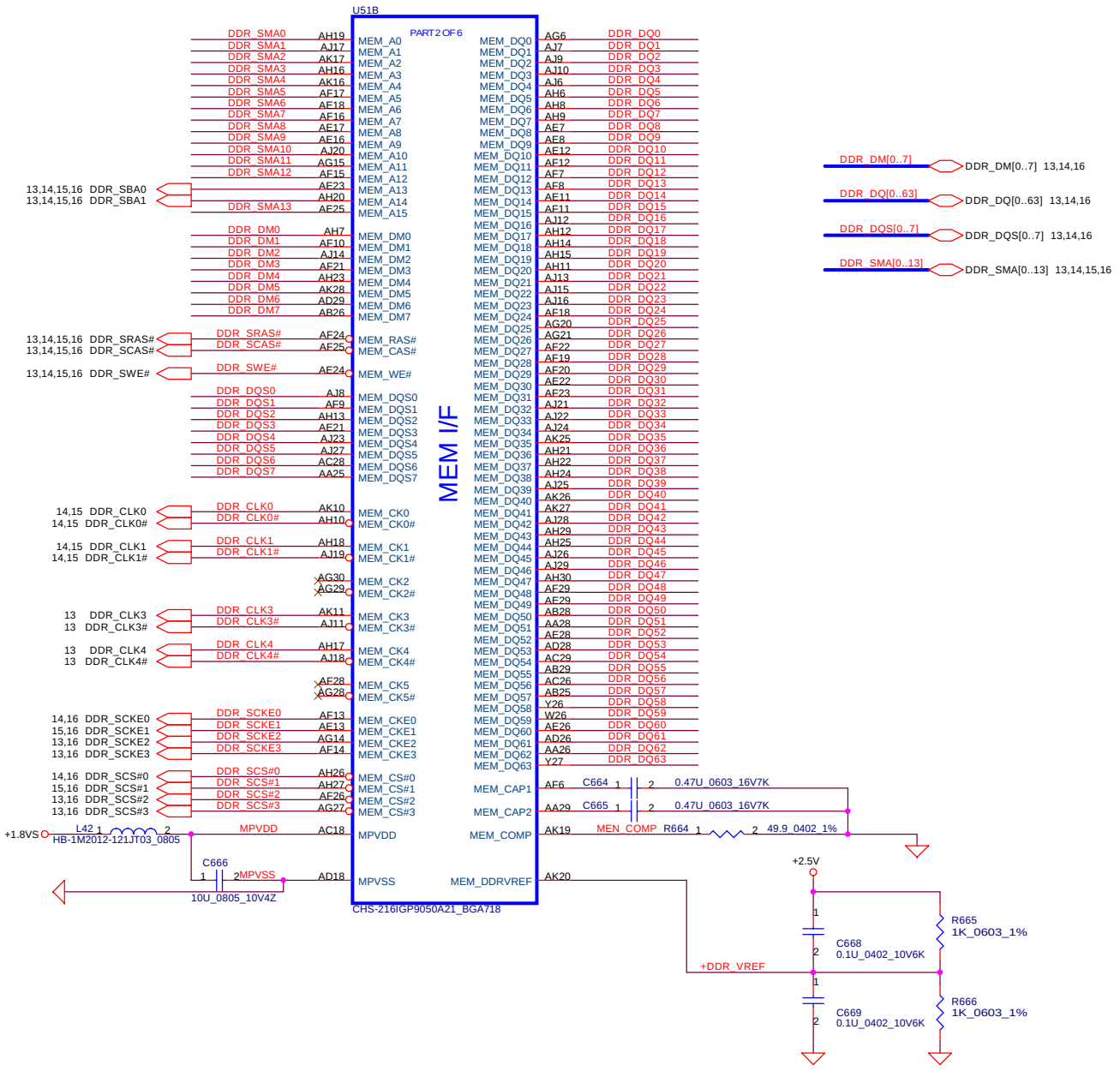

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Title: ATi RC300ML-DDR(3/5)		
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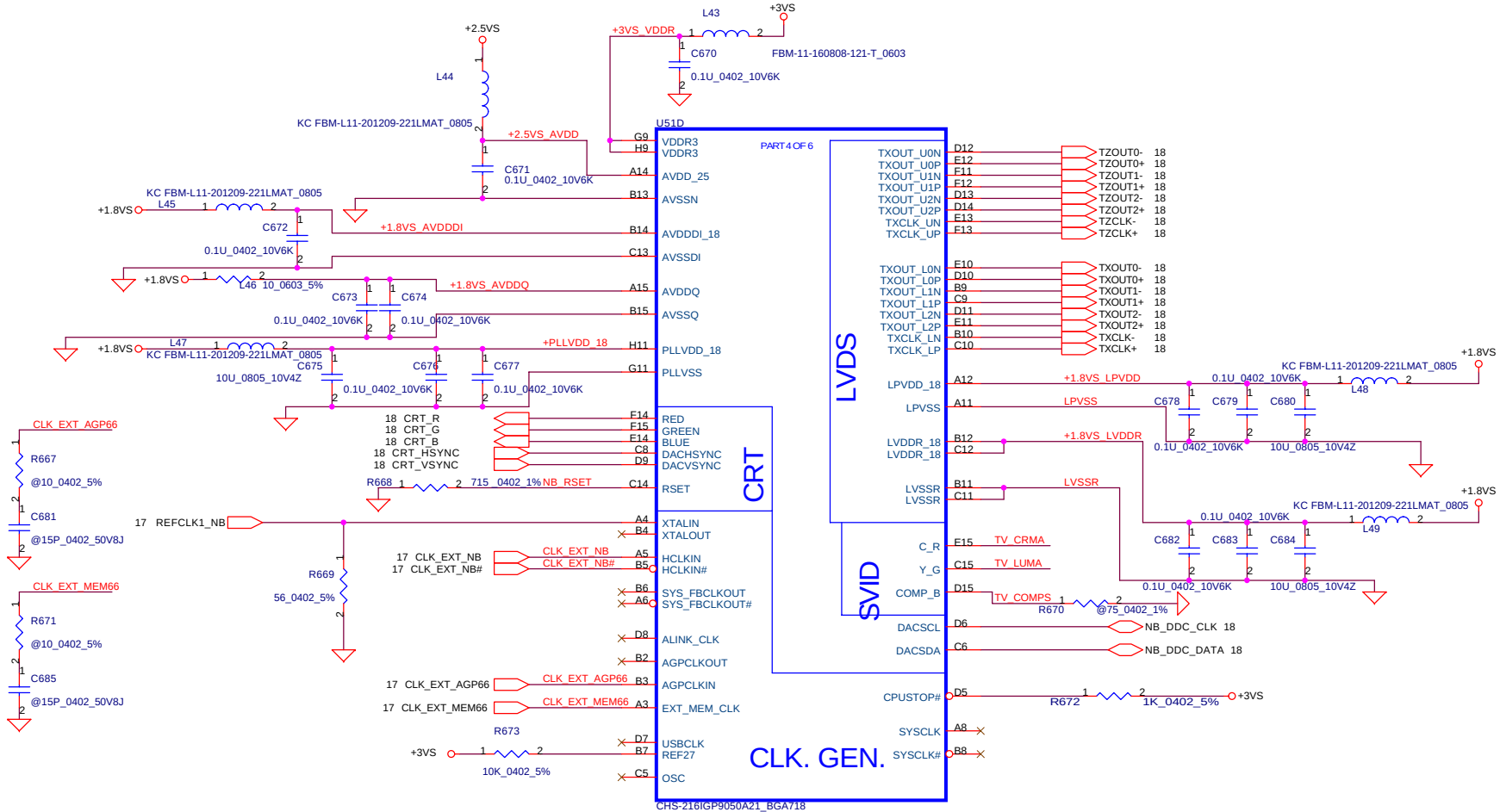
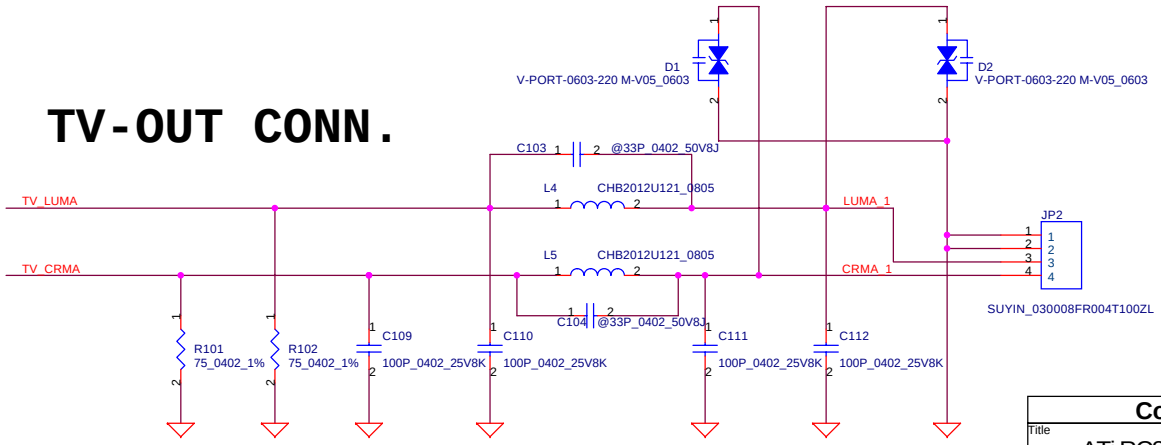


TV-OUT CONN.



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Title	ATi RC300ML-VEDIO(4/5)
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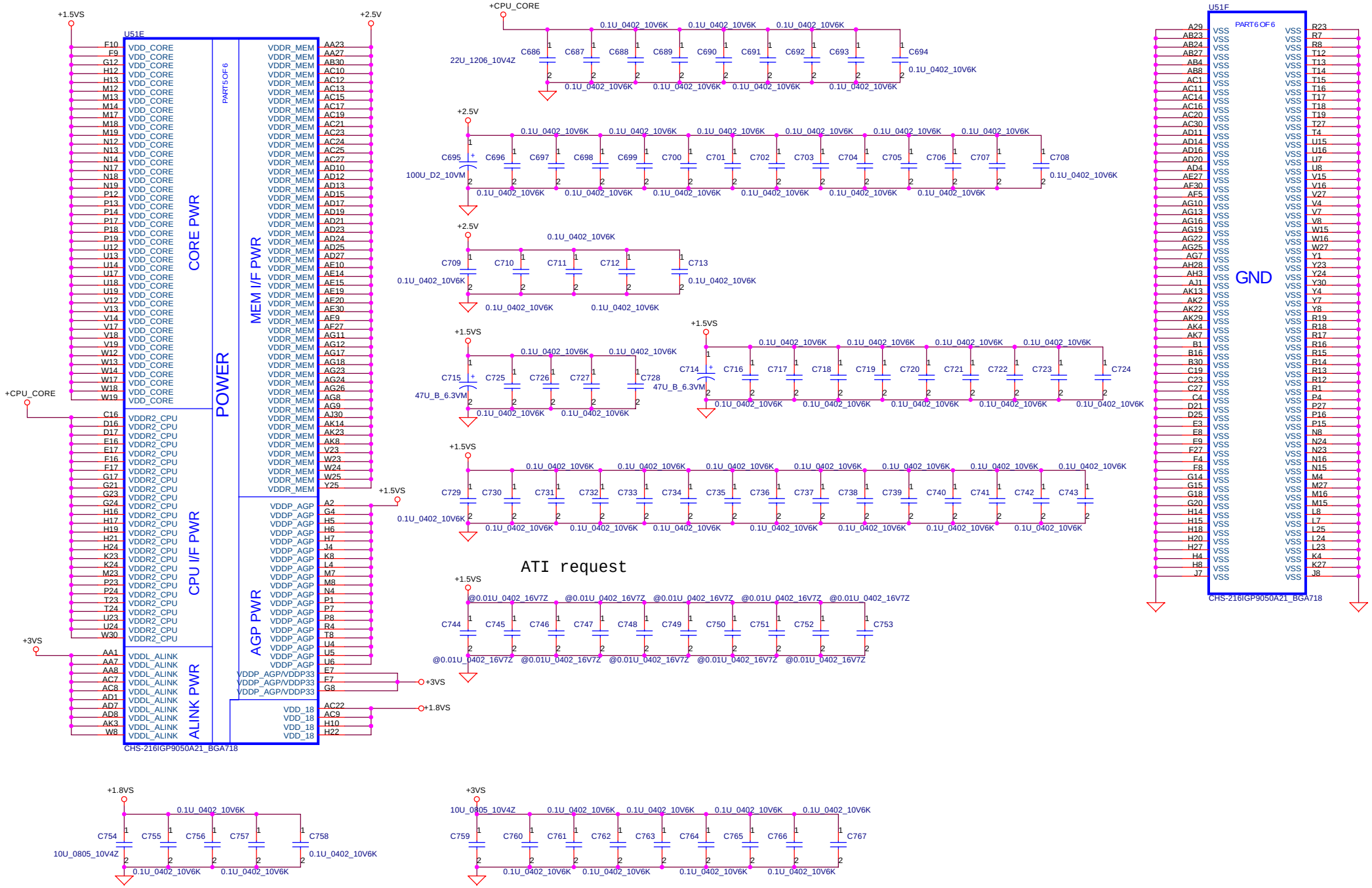

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Title: ATi RC300ML-Power(5/5)		
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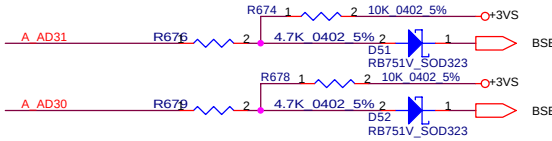
A_CBE#[0..3] A_CBE#[0..3] 8,19

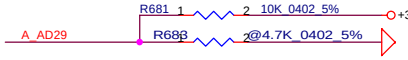
8,19 A_AD[0..31] A_AD[0..31]



A_AD[31..30] : FSB CLK SPEED

DEFAULT: 01

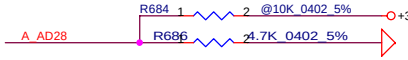
00: 100 MHZ
01: 133 MHZ
10: 200MHZ
11:166 MHZ



A_AD29: STRAP CONFIGURATION

DEFAULT:1

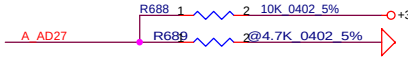
0: REDUCEDE SET
1: FULL SET(internal Pull high)



A_AD28: SPREAD SPECTRUM ENABLE

DEFAULT:0

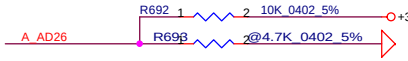
0: DISABLE
1: ENABLE



A_AD27: FrcShortReset#

DEFAULT: 1

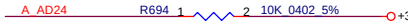
0: TEST MODE
1: NORMAL
MODE



A_AD26 : ENABLE IOQ

DEFAULT: 1

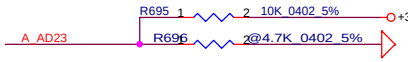
0: IOQ=1
1:
IOQ=12



A_AD24 : MOBILE CPU SELECT

DEFAULT: 1

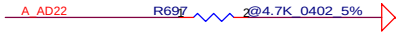
0: BANIAS CPU
1: OTHER CPU



A_AD23 : CLOCK BYPASS DISABLE

DEFAULT: 1

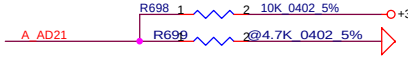
0: TEST MODE
1: NORMAL(internal Pull high)



A_AD22 : OSC PAD OUTPUT PCICLK

DEFAULT : 1

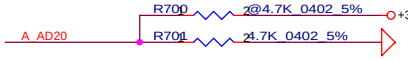
0:PCICLK OUT
1: OSC CLK OUT



A_AD21 : AUTO_CAL ENABLE

DEFAULT : 1

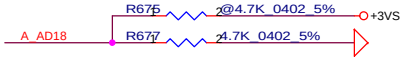
0: DISABLE
1: ENABLE



A_AD20 : INTERNAL CLK GEN ENABLE

DEFAULT : 0

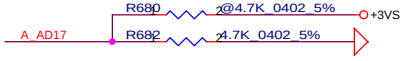
0: DISABLE
1: ENABLE



A_AD18 : ENABLE PHASE CALIBRATION

DEFAULT: 0

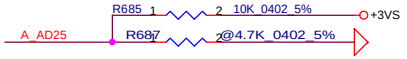
0: DISABLE
1:ENABLE



A_AD25/A_AD17 : CPU VOLTAGE[1..0]

DEFAULT: 0

00: 1.05V
01: 1.35V
11: 1.75V
10: 1.45V

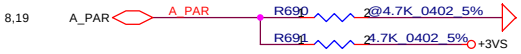


A_AD25/A_AD17 : CPU VOLTAGE[1..0]

DEFAULT: 10

00: 1.05V
01: 1.35V
11: 1.75V
10: 1.45V

AD25=1 DESTOP CPU
AD25=0 MOBILE CPU
AD17--DON'T CARE



PAR: EXTENDED DEBUG MODE

DEFAULT : 1

0: DEBUG MODE
1: NORMAL

Compal Electronics, Inc.		
Title: ATi RC300ML-SYS. CONFIG.		
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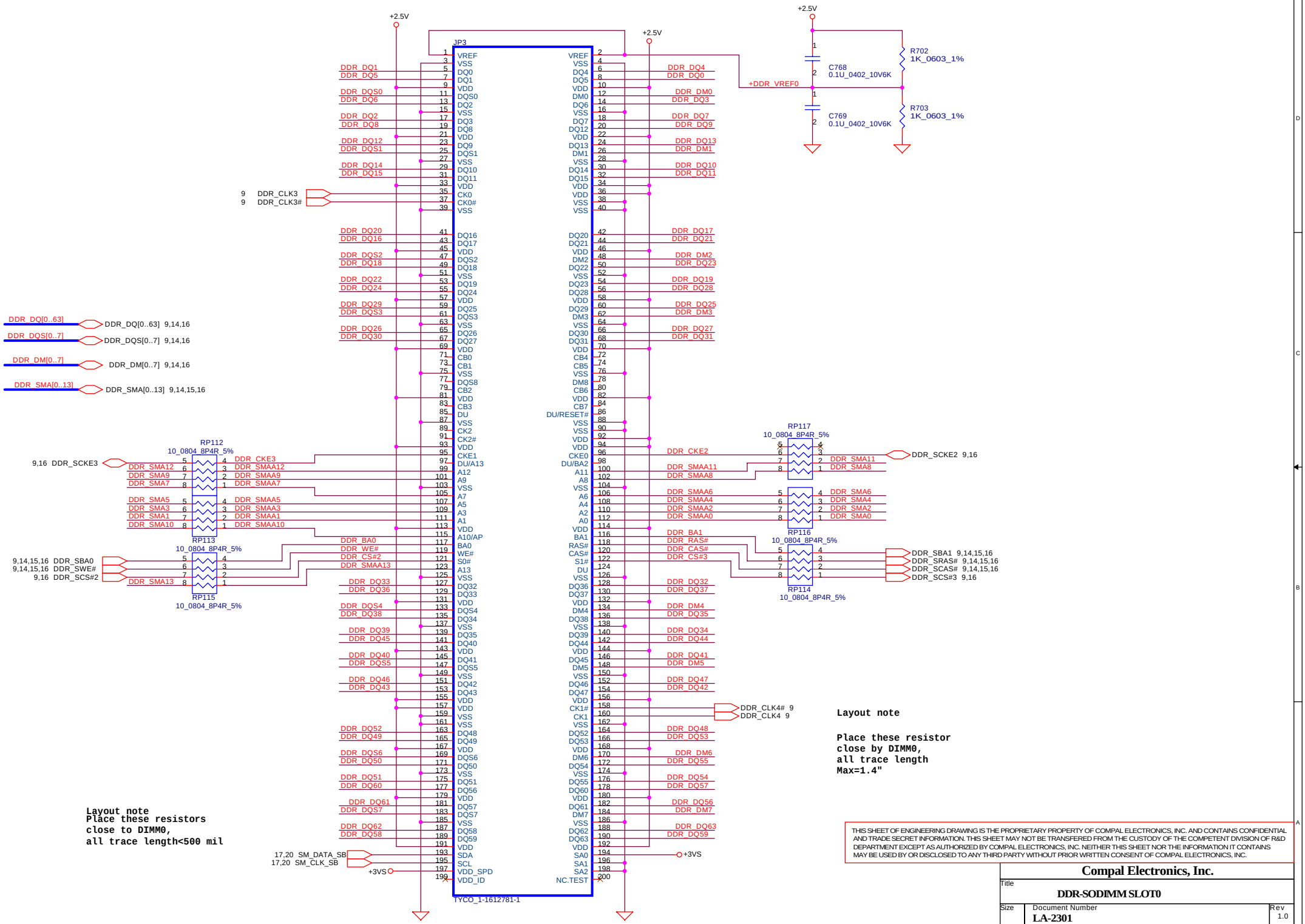

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Title	DDR-SODIMM SLOT0	
Size	Document Number LA-2301	Rev 1.0
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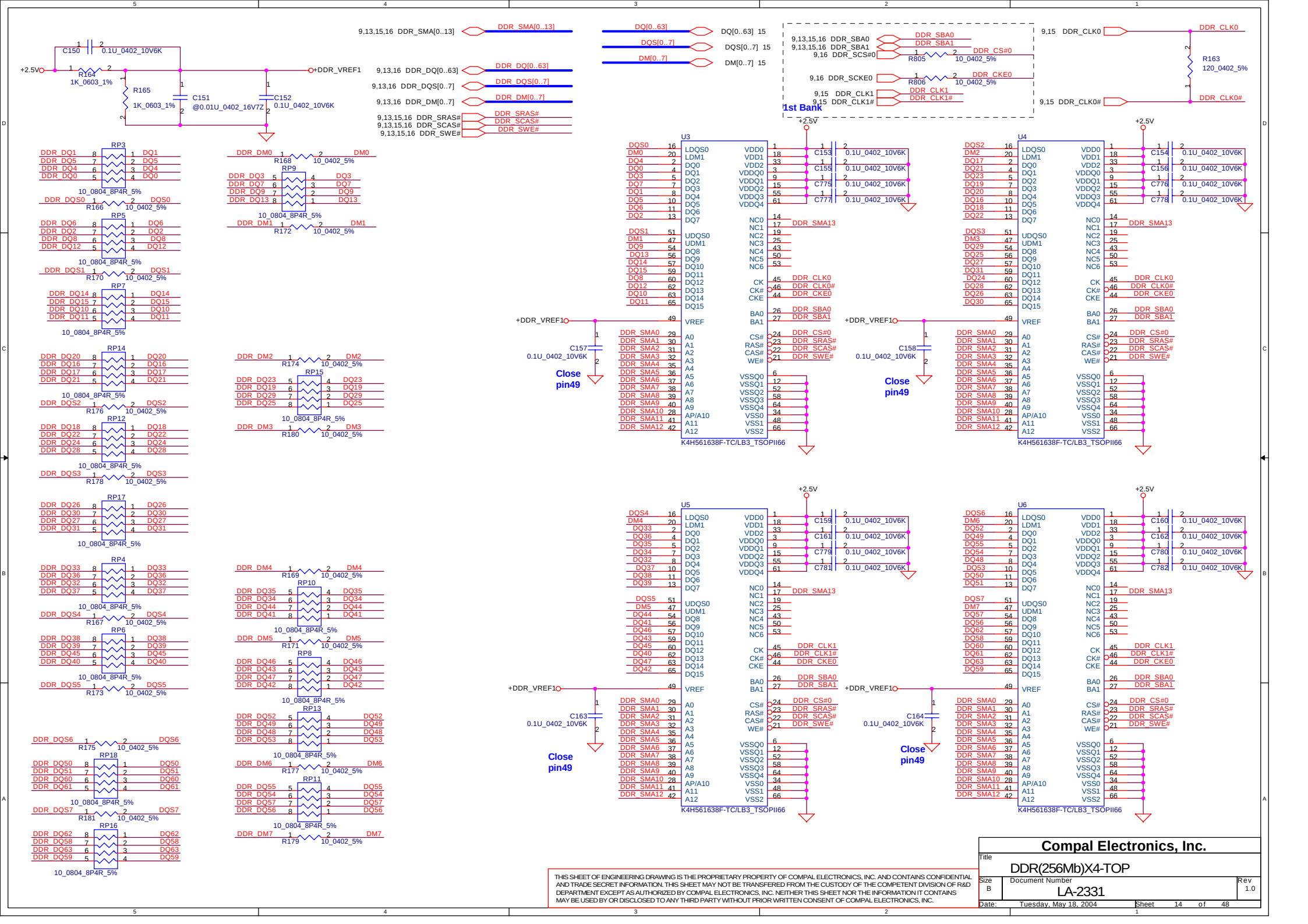

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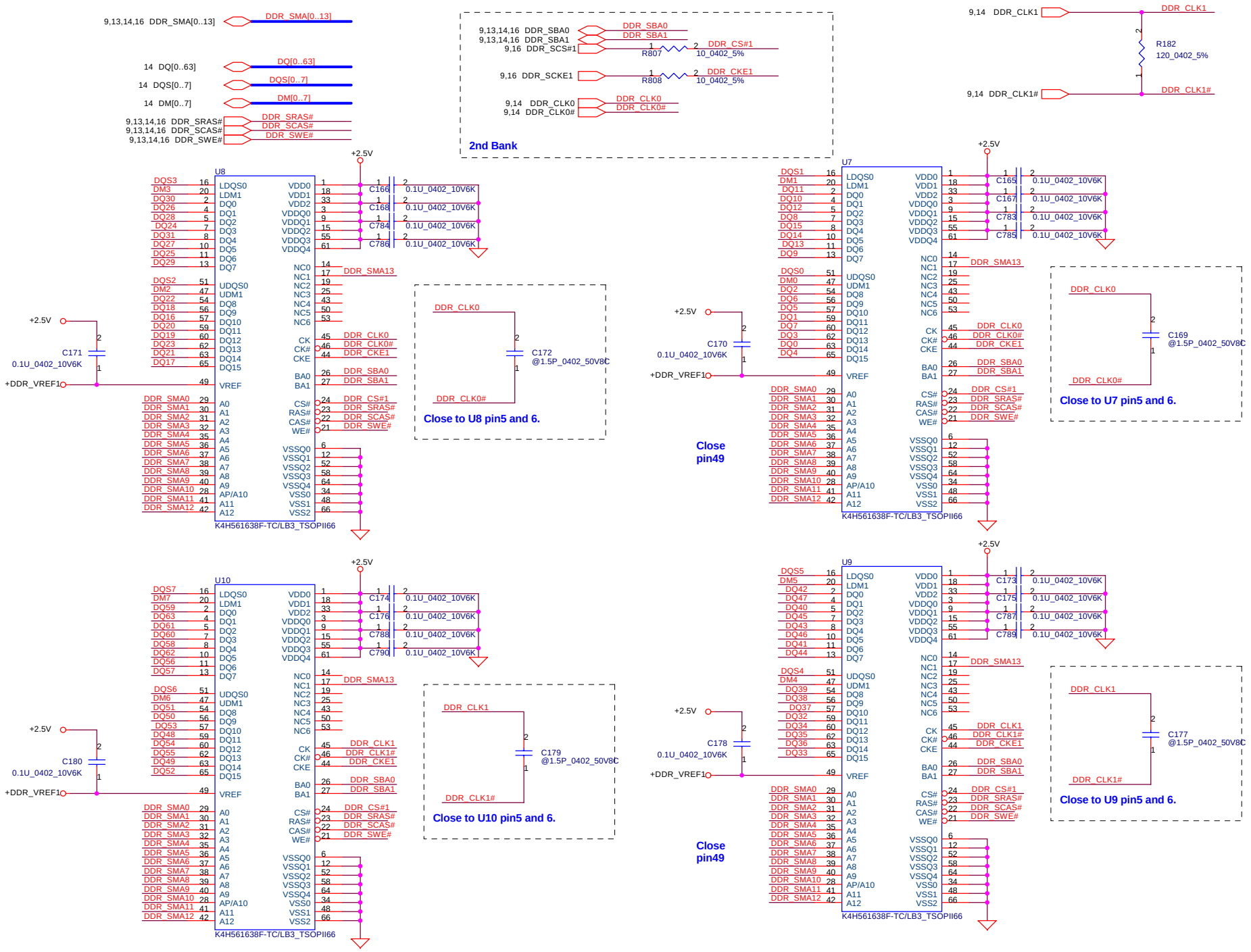
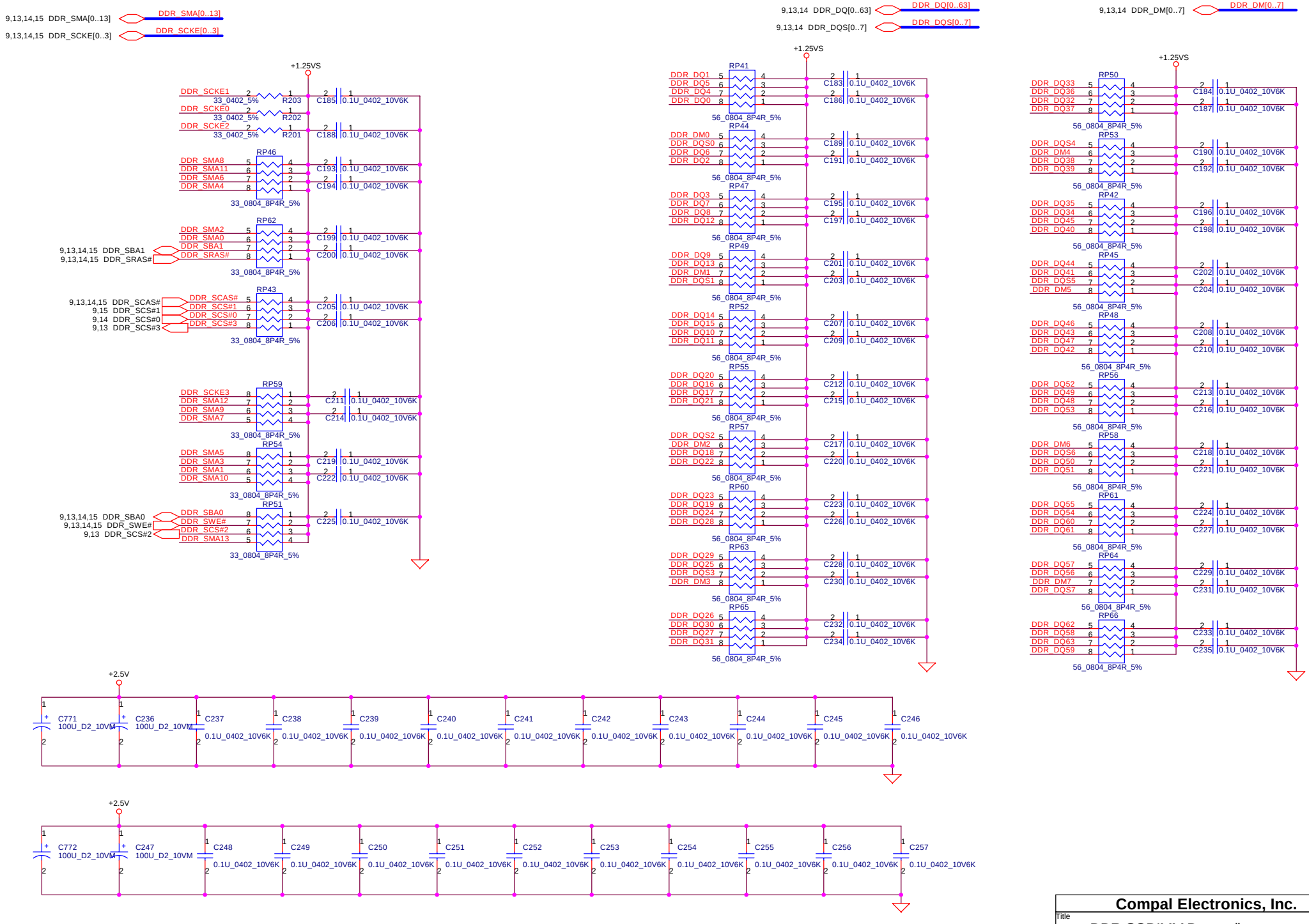
Title	DDR(256Mb)X4-TOP	
Size B	Document Number LA-2331	Rev 1.0
Date: Tuesday, May 18, 2004	Sheet 14 of 48	



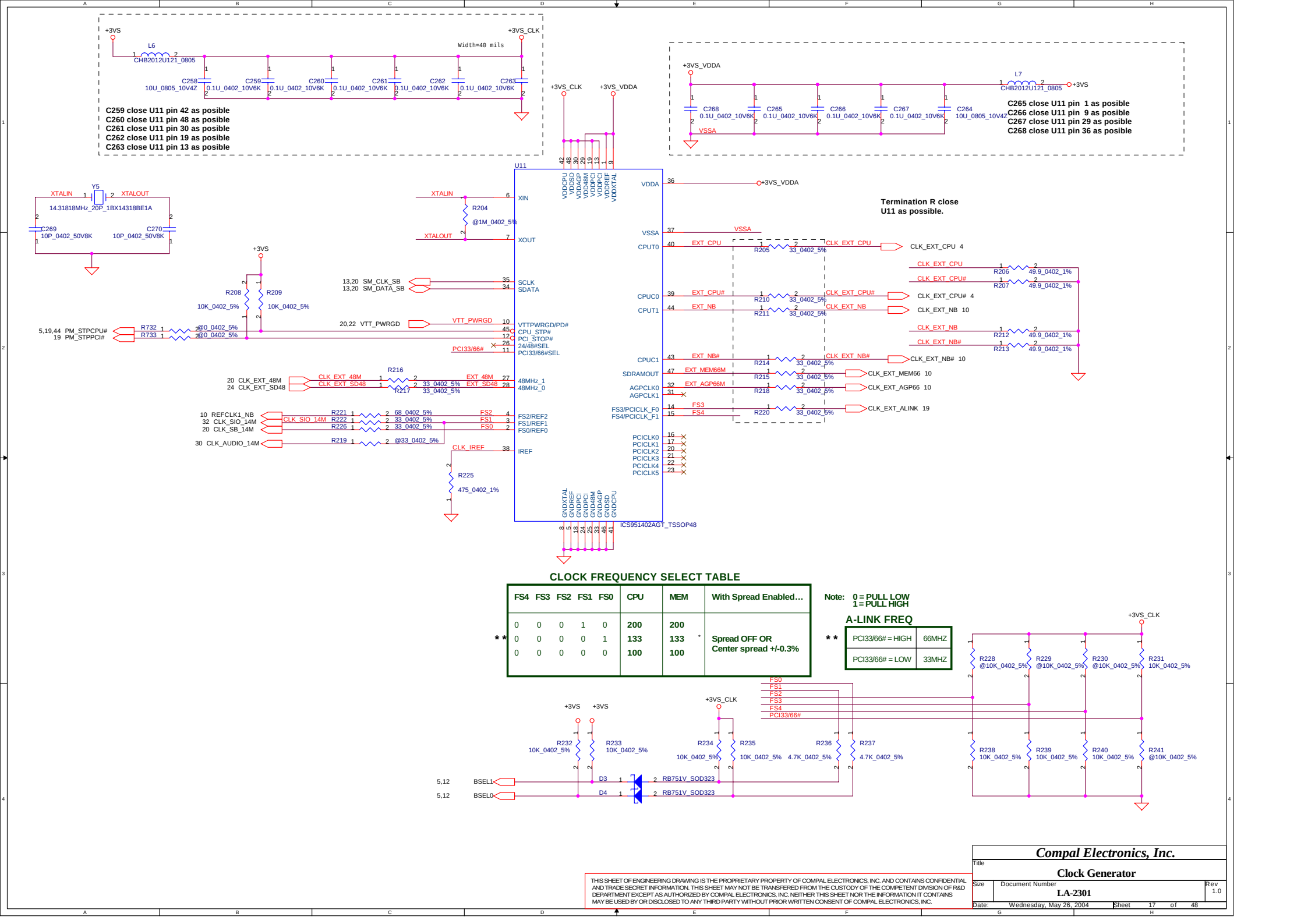
Compal Electronics, Inc.

Title	DDR(256Mb)X4-BTN	
Size B	Document Number LA-2331	Rev 1.0
Date: Tuesday, May 18, 2004	Sheet 15 of 48	



Compal Electronics, Inc.

Title	DDR-SODIMM Decoupling	
Size B	Document Number LA-2301	Rev 1.0
Date: Tuesday, May 18, 2004	Sheet 16 of 48	



CLOCK FREQUENCY SELECT TABLE

	FS4	FS3	FS2	FS1	FS0	CPU	MEM	With Spread Enabled…
	0	0	0	1	0	200	200	
**	0	0	0	0	1	133	133	Spread OFF OR
	0	0	0	0	0	100	100	Center spread +/-0.3%

Note: 0 = PULL LOW
1 = PULL HIGH

A-LINK FREQ

PCI33/66# = HIGH	66MHZ
PCI33/66# = LOW	33MHZ

Compal Electronics, Inc.
Title: Clock Generator
Size: Document Number: LA-2301
Rev: 1.0
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SI2302DS: N CHANNEL
VGS: 4.5V, RDS: 85 mOHM
VGS: 2.5V, RDS: 115mOHM
Id(MAX): 2.8A
VGS(MAX): +-8V

Width: 40mils

CRT Connector

Close to CRT connector

Compal Electronics, Inc.		
Title: LVDS, CRT& TV CONN		
Size: B	Document Number: LA-2301	Rev: 1.0
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Layout note:
Trace length of PCI_CLK_R + PCI_CLK_FB should be less than 200 mils.

U14A
SB150 SB
Part 1 of 3
CHS-215IXP150-11_BGA457

GPOC3#	GPOC2#	GPIO1			
RAM_SEL2	RAM_SEL1	RAM_SEL0	Size	Vendor	Cells
0	0	0	256M(16X16)	SAM	8
0	0	1	256M(16X16)	HYN	8
0	1	0	256M(16X16)	Elpida	8
0	1	1	256M(16X16)	Infienon	8
1	0	0	512M(32X16)	SAM	8
1	0	1	512M(32X16)	HYN	8
1	1	0	512M(32X16)	Elpida	8
1	1	1	512M(32X16)	Infienon	8

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Title: IXP150(1/4)- PCI/CPU/LPC

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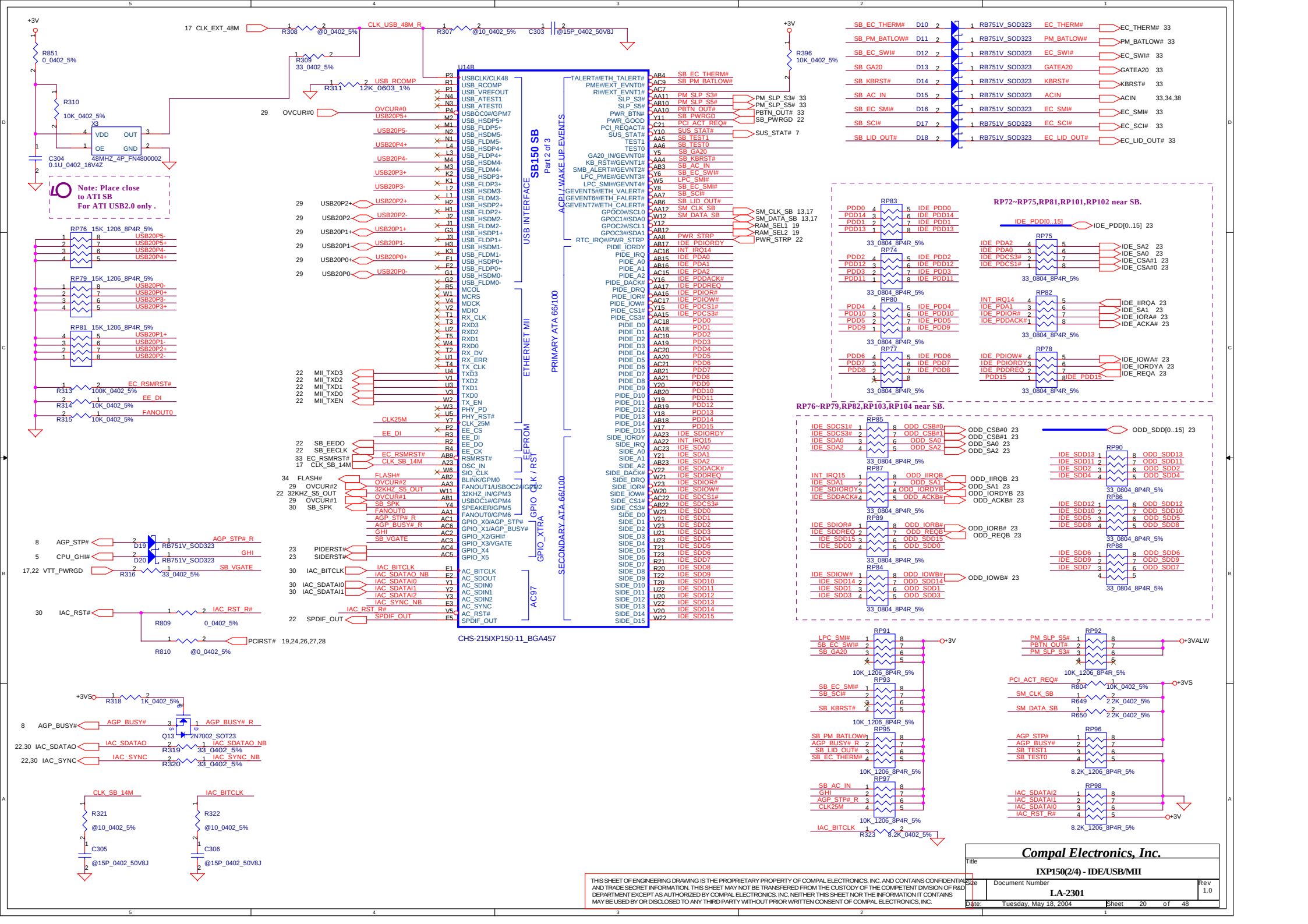
U14B
SB150 SB
Part 2 of 3
CHS-215IXP150-11_BGA457
USB INTERFACE
ETHERNET MII
EEPROM
GPIO CLK / RST
GPIO_XTRA
AC97
ACPI/WAKE UP EVENTS
PRIMARY ATA 66/100
SECONDARY ATA 66/100
Note: Place close to ATI SB For ATI USB2.0 only .
RP72~RP75,RP81,RP101,RP102 near SB.
RP76~RP79,RP82,RP103,RP104 near SB.
Compal Electronics, Inc.
IXP150(2/4) - IDE/USB/MII
LA-2301
Tuesday, May 18, 2004
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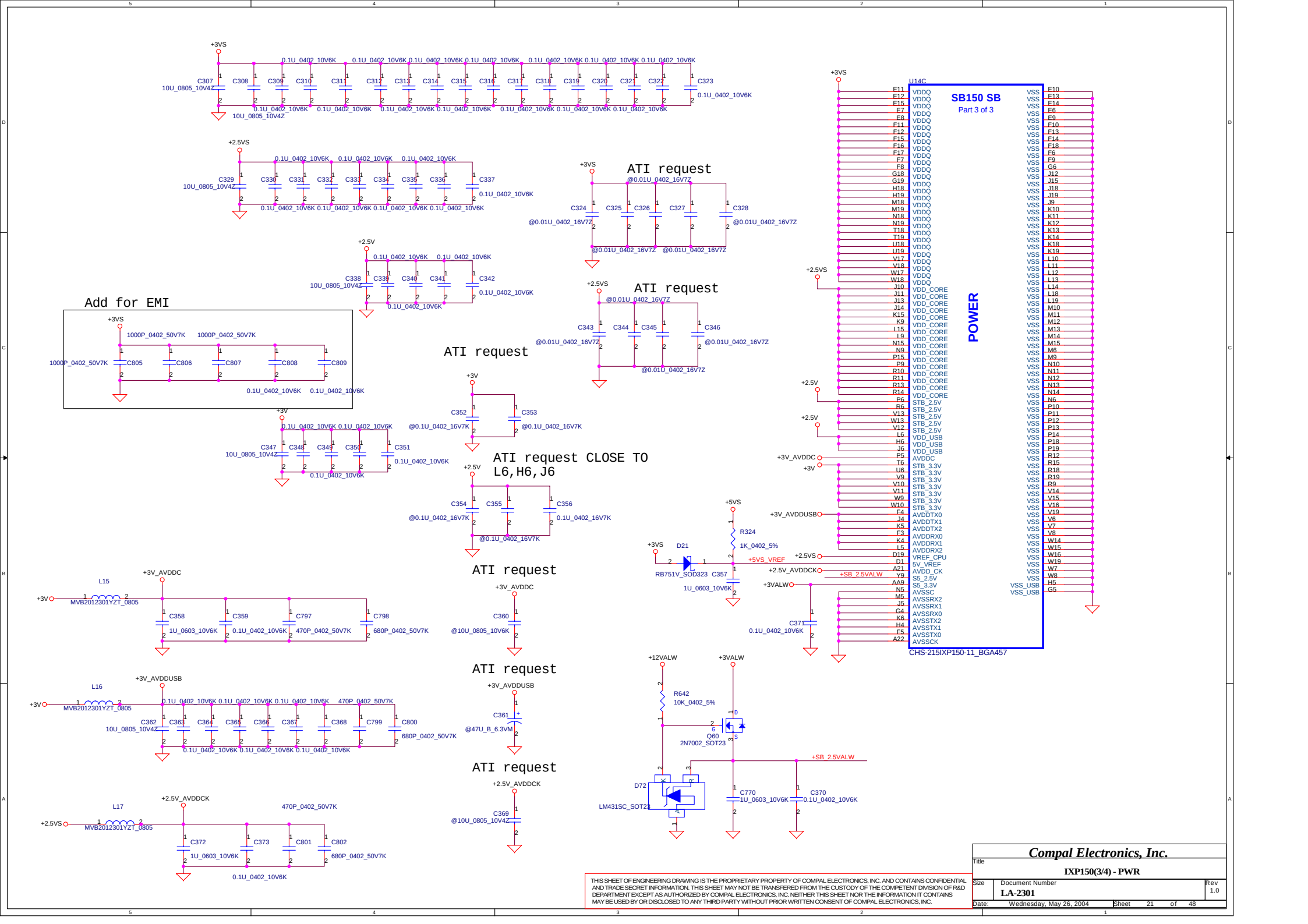

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Title	IXP150(3/4) - PWR	
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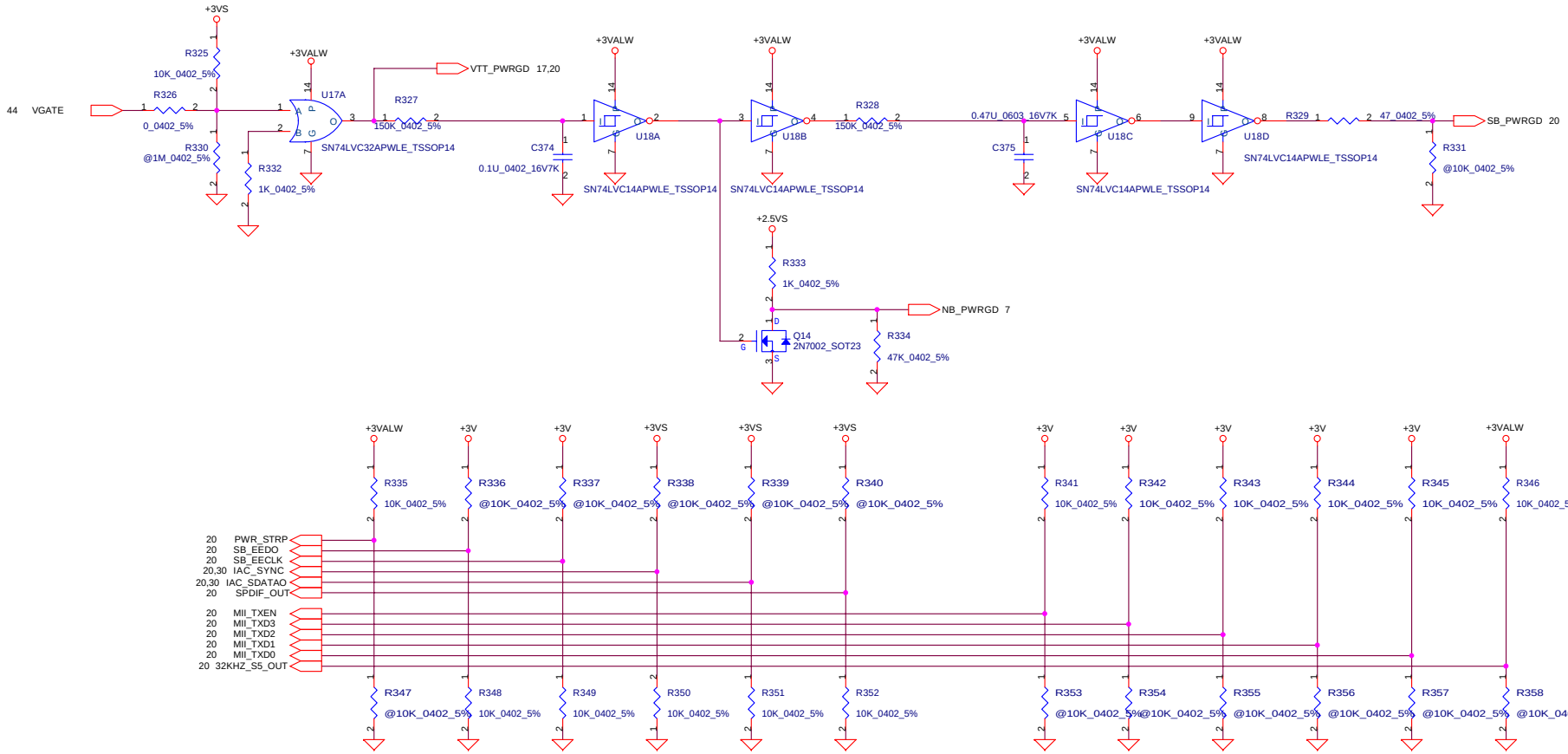
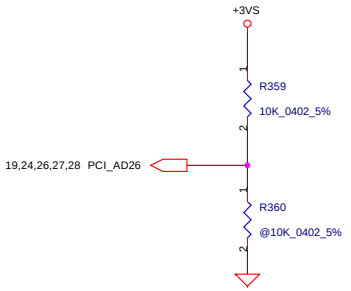


REQUIRED SYSTEM STRAPS

	PWR_STRP	IGN DEBUG EEDO	EECK	AC_SYNC	AC_SDOUT	SPDIF_OUT	SPEEDSTEP CPU_STP#	FREQLTCH TX_EN	ETHERNET TXD[3:0]	32KHZ_S5
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	ROM ON PCI BUS	INIT ACTIVE HIGH	33MHz NB BUS	SIO 24MHz	ENABLE SPEED STEP	DISABLE CPU FREQ SETTING DEFAULT	PROCESSOR FREQ MULTIPLIER	32KHZ OUTPUT FROM SB200 (INT RTC) DEFAULT
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	ROM ON LPC BUS DEFAULT	INIT ACTIVE LOW (PIII) DEFAULT	HI SPEED A-LINK DEFAULT	SIO 48MHz DEFAULT	DISABLE SPEED STEP DEFAULT	ENABLE CPU FREQSETTING		32KHZ INPUT TO SB200 (EXT RTC)



Compal Electronics, Inc.

Title: IXP150(4/4) - STRAPS

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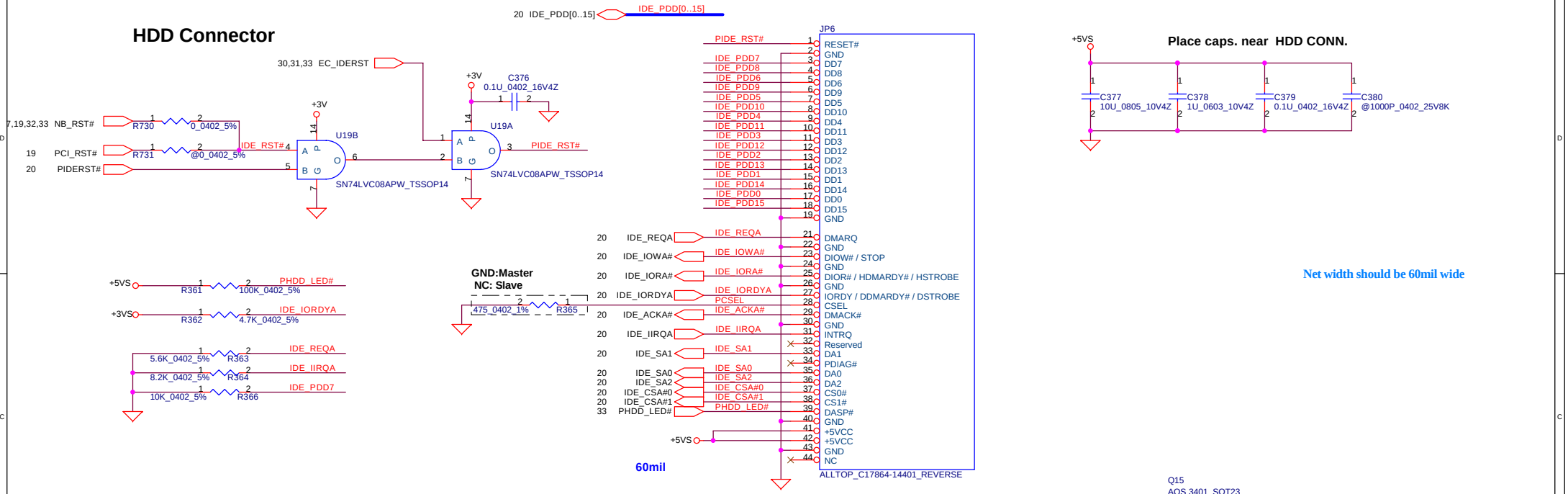
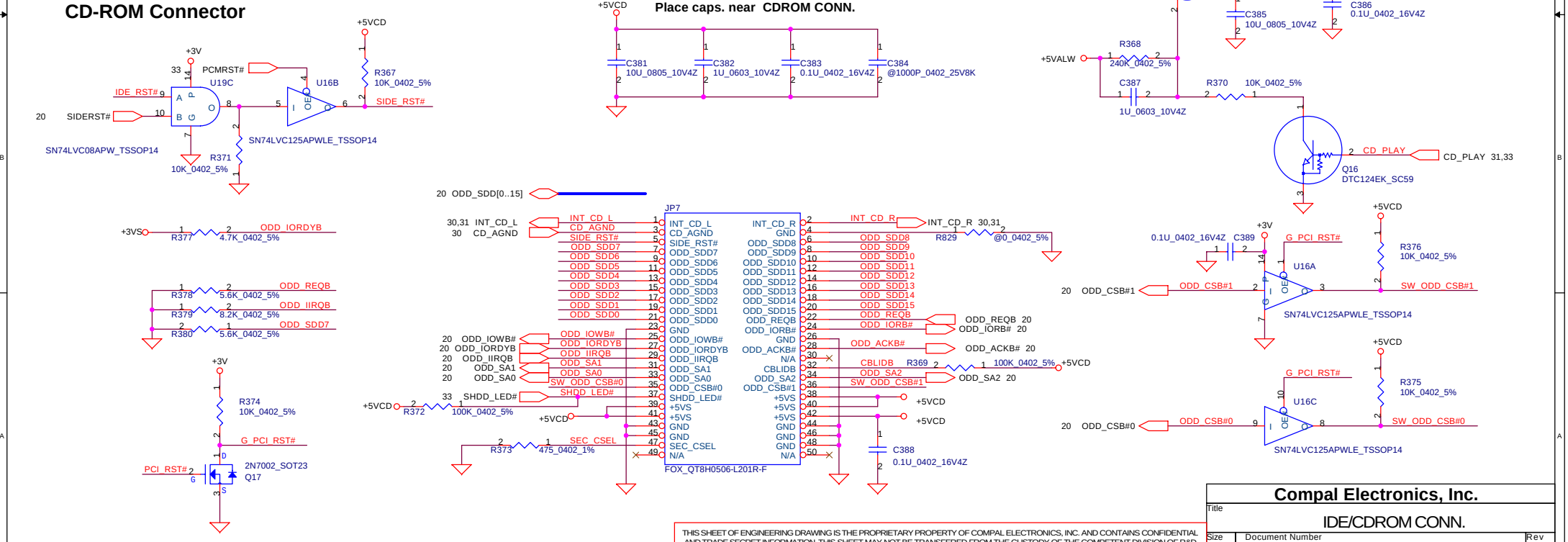
HDD Connector



CD-ROM Connector



Compal Electronics, Inc.		
Title: IDE/CDROM CONN.		
Size: B	Document Number: LA-2301	Rev: 1.0
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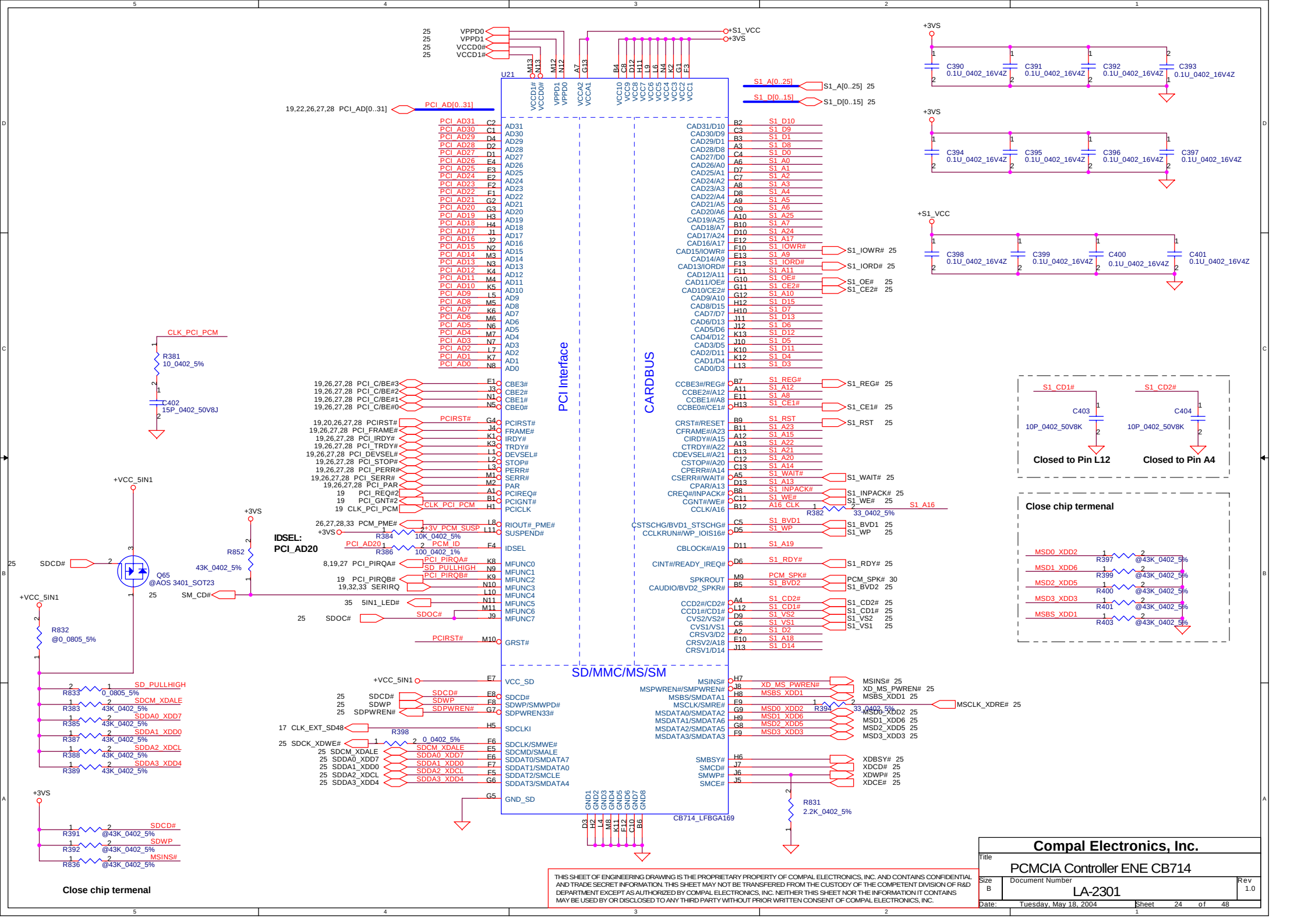

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Compal Electronics, Inc.

Title	PCMCIA Controller ENE CB714	
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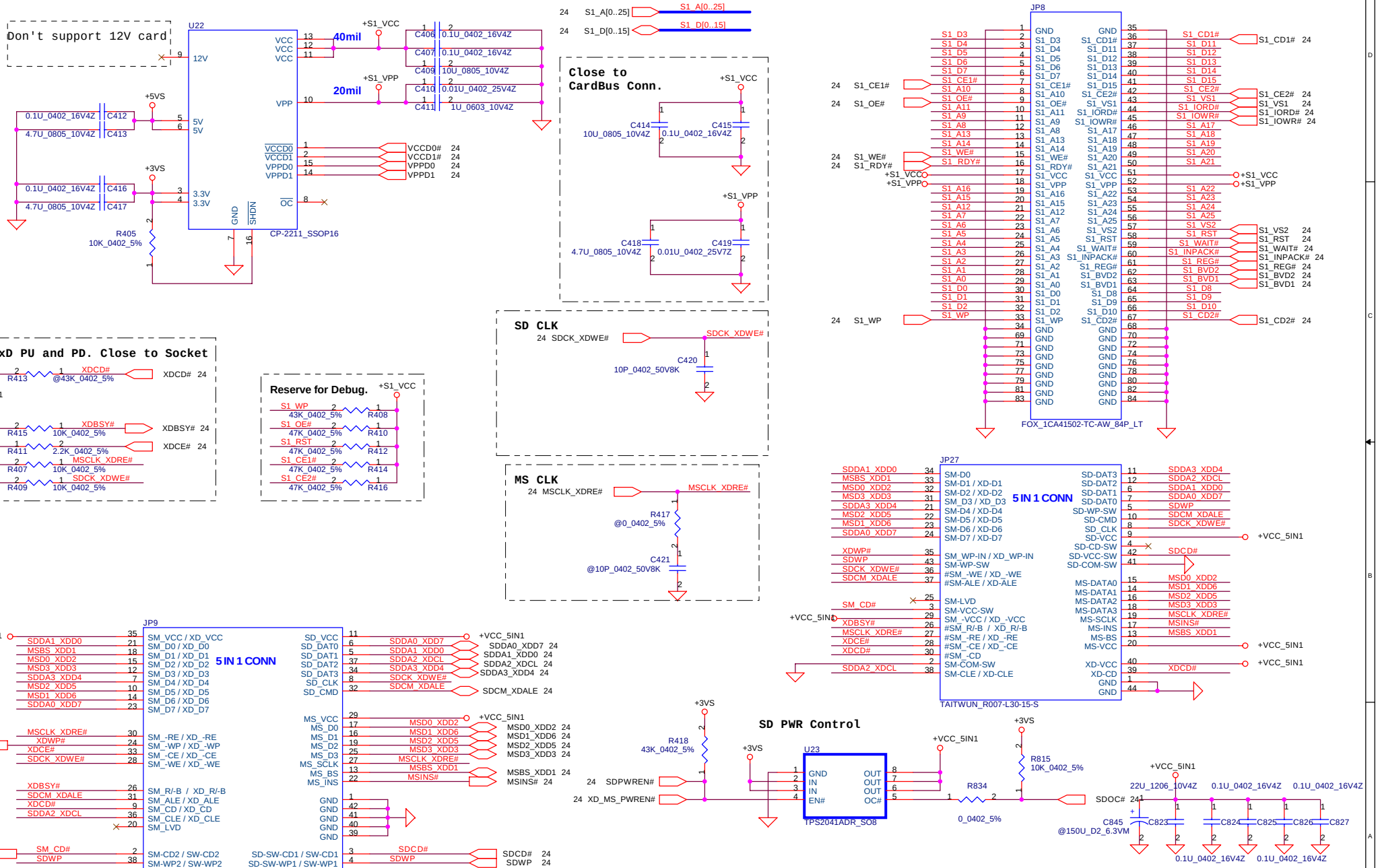
PCMCIA Power Controller

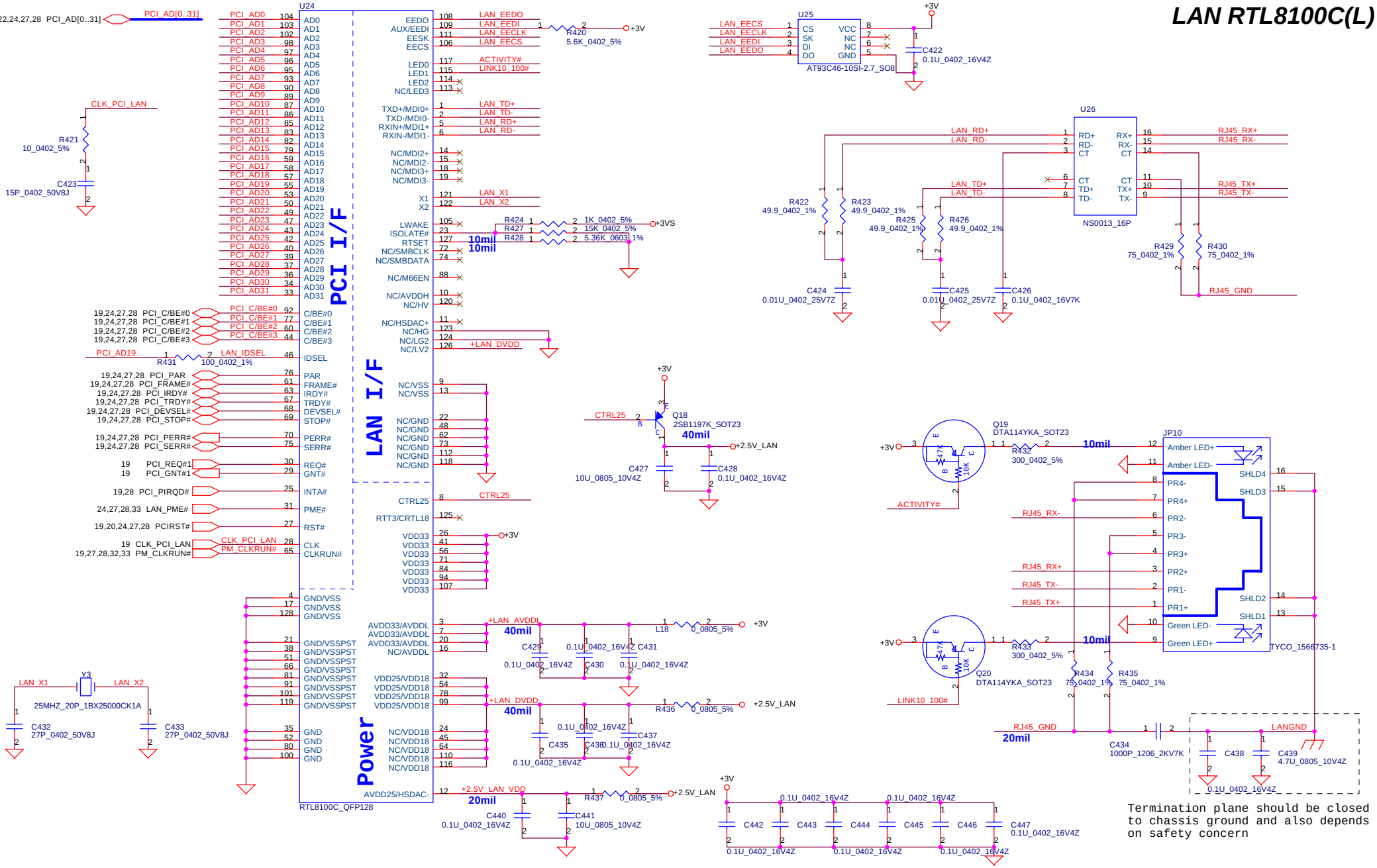
CardBus Socket



Compal Electronics, Inc.

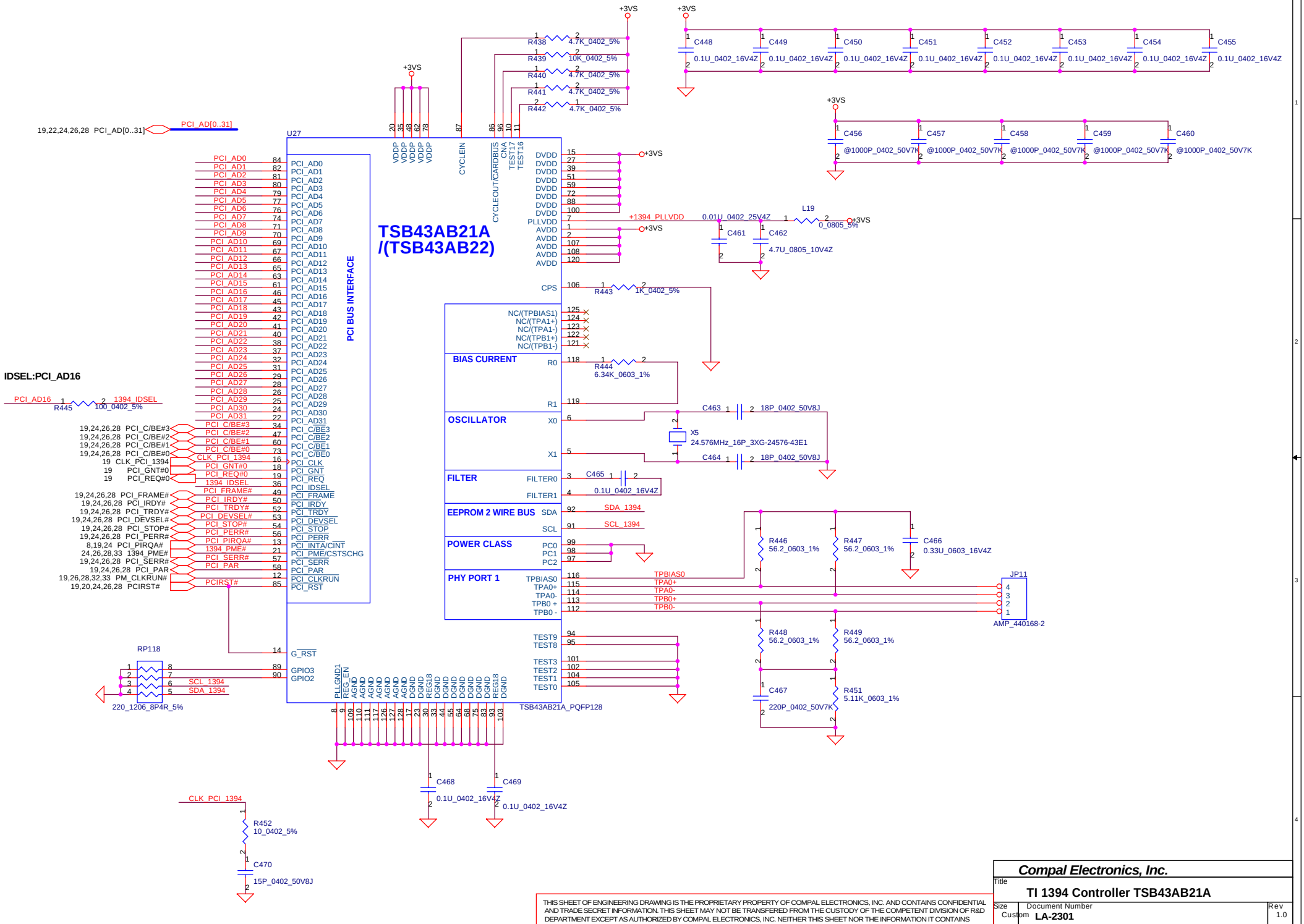
Title	PCMCIA Socket	
Size B	Document Number LA-2301	Rev 1.0
Date: Tuesday, May 18, 2004	Sheet 25 of 48	

LAN RTL8100C(L)



Compal Electronics, Inc.

Title	LAN REALTEK RTL8100CL	
Size	Document Number LA-2301	Rev 1.0
Date: Wednesday, May 26, 2004	Sheet 26 of 48	


TSB43AB21A
/(TSB43AB22)
PCI BUS INTERFACE
IDSEL:PCI_AD16
BIAS CURRENT
OSCILLATOR
FILTER
EEPROM 2 WIRE BUS
POWER CLASS
PHY PORT 1
TSB43AB21A_PQFP128
220_1206_8P4R_5%
AMP_440168-2
Compal Electronics, Inc.
TI 1394 Controller TSB43AB21A
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Size Custom
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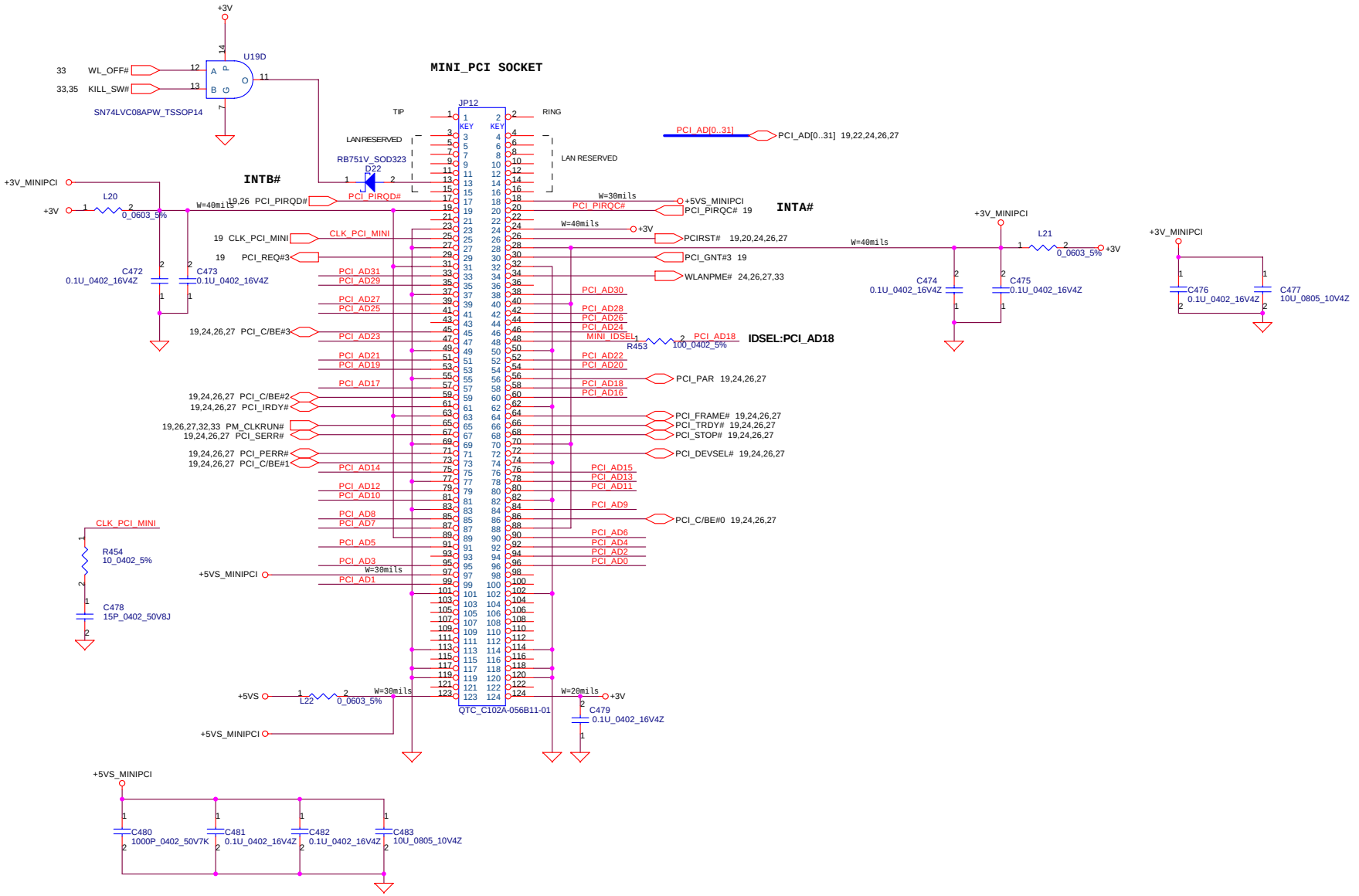

Compal Electronics, Ltd.

Title	Mini PCI Slot	
Size: Custom	Document Number: LA-2301	Rev: 1.0
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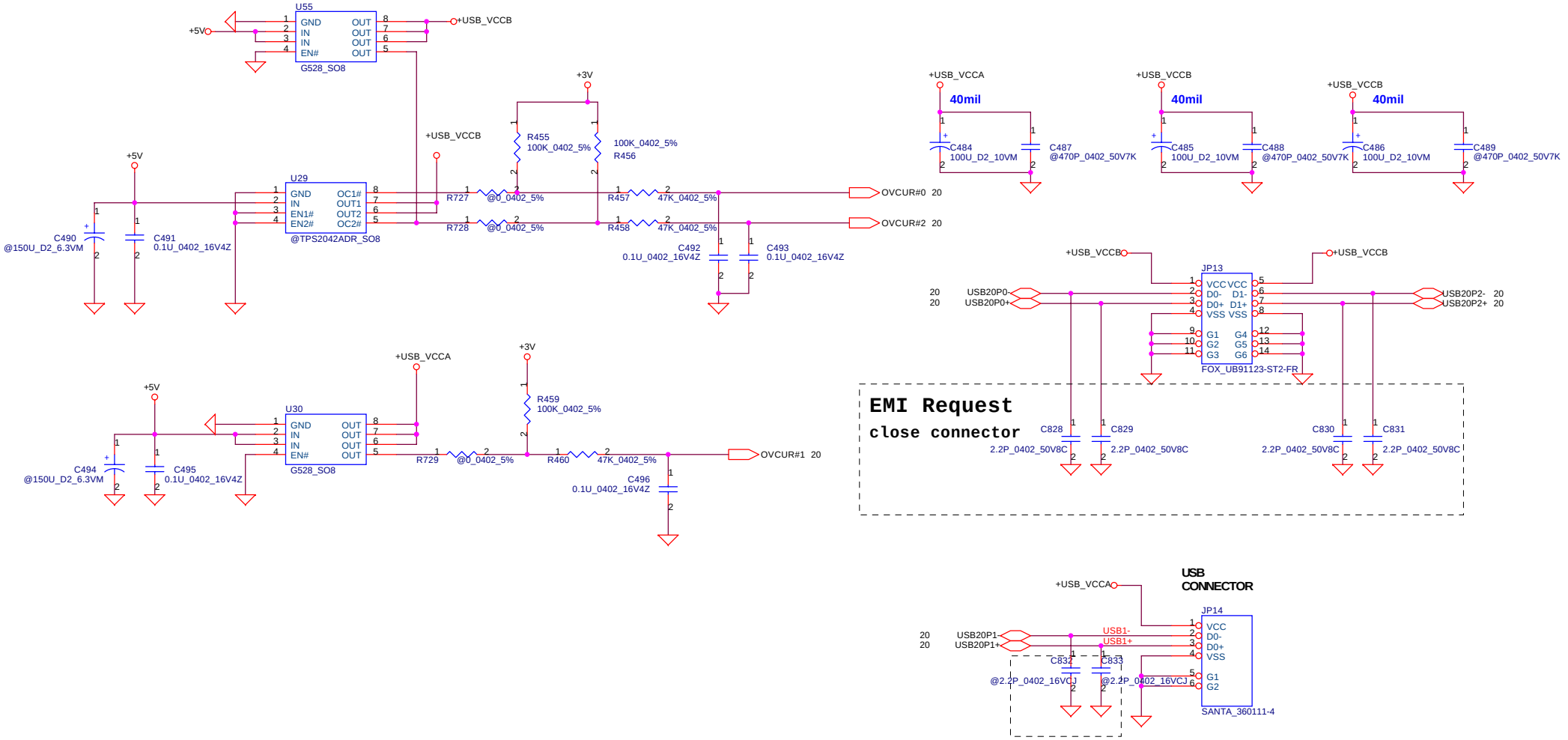

Compal Electronics, Inc.		
Title: USB/PCI-Debug		
Size: B	Document Number: LA-2301	Rev: 1.0
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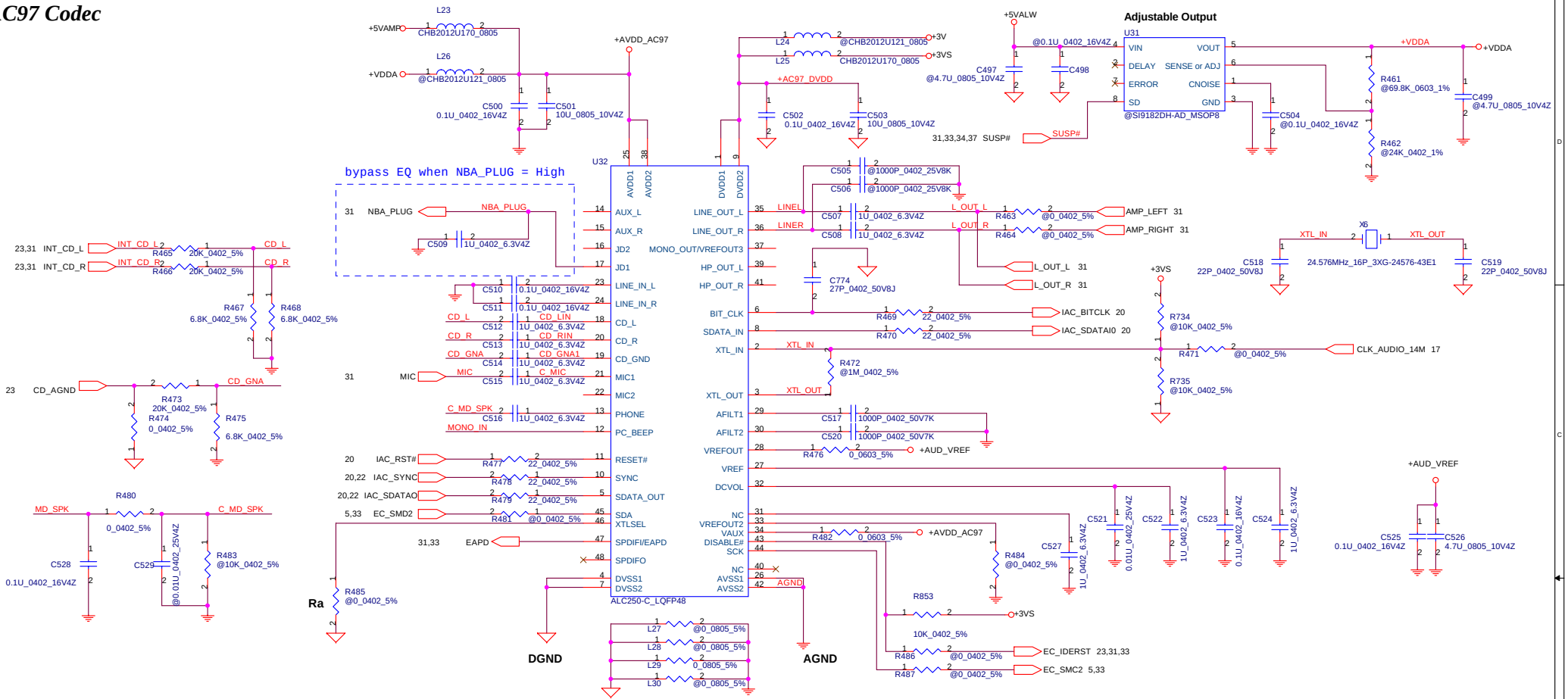
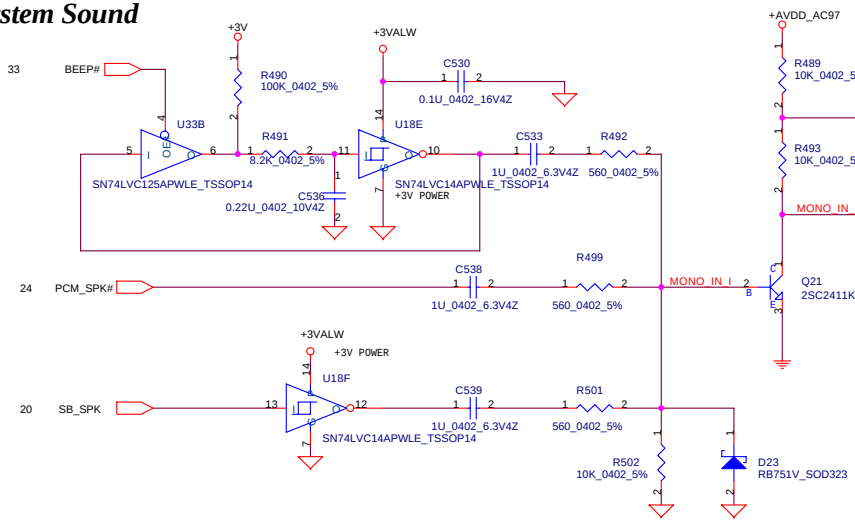
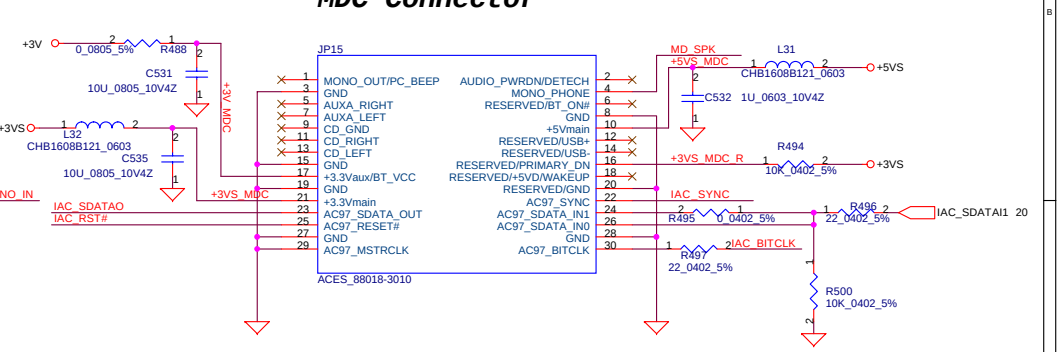
AC97 Codec



System Sound



MDC Connector



Compal Electronics, Ltd.	
Title: AC97 Codec ALC250	
Size: Custom	Document Number: LA-2301
Rev: 1.0	
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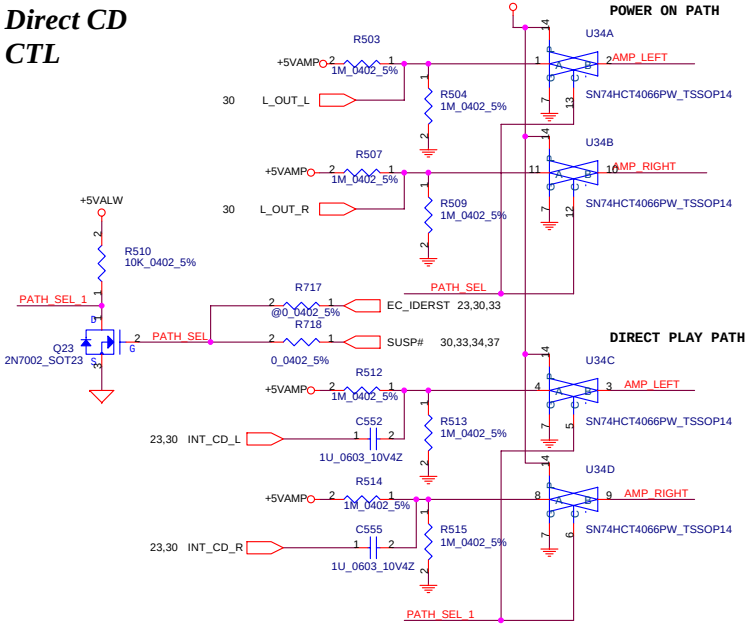
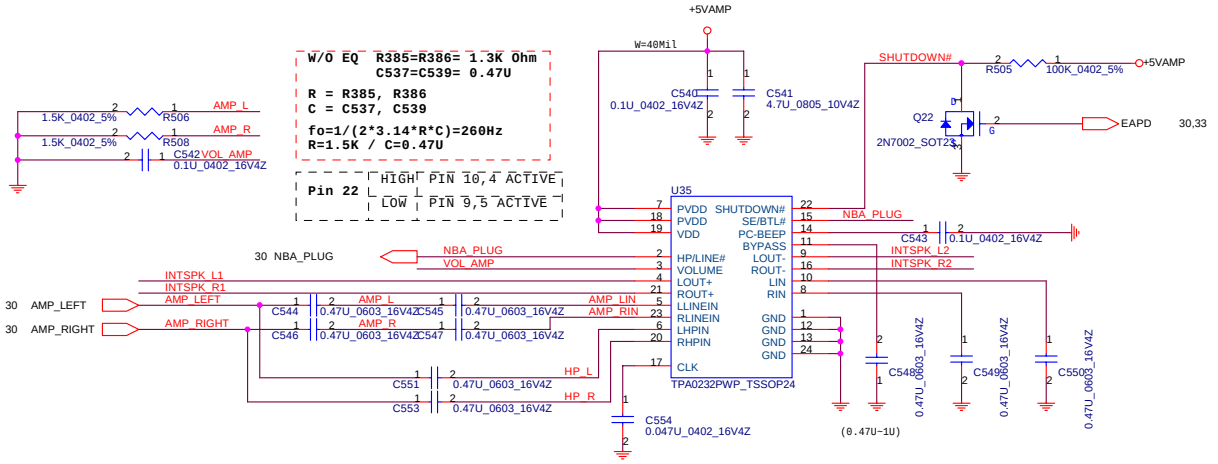
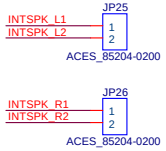
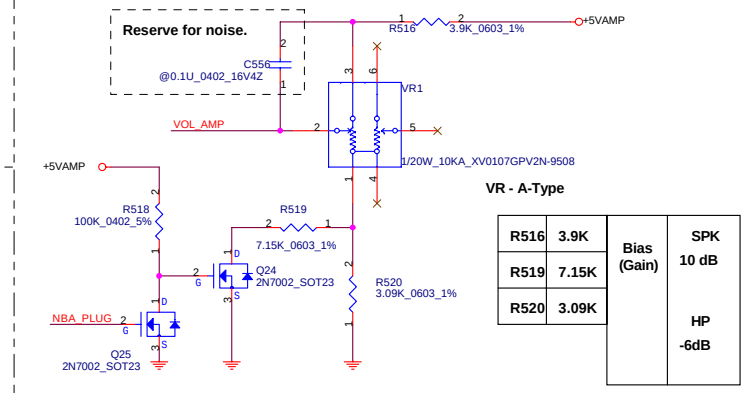
Direct CD CTL



Audio AMP

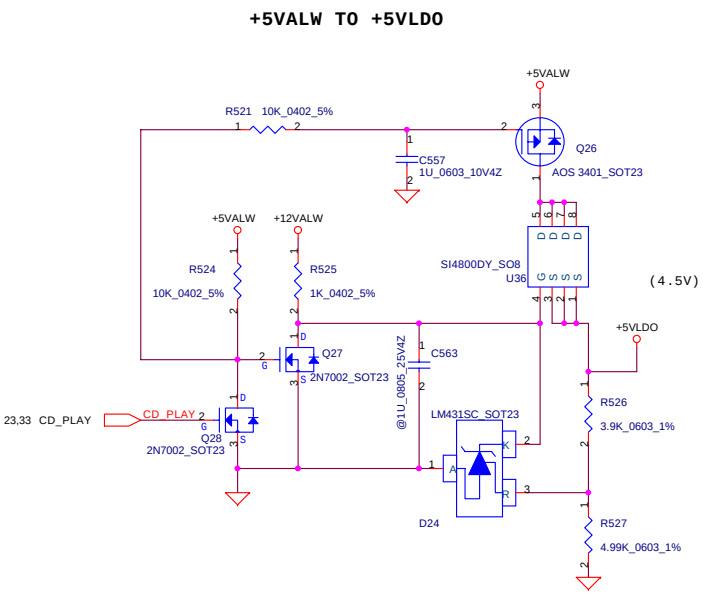


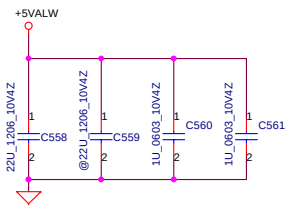


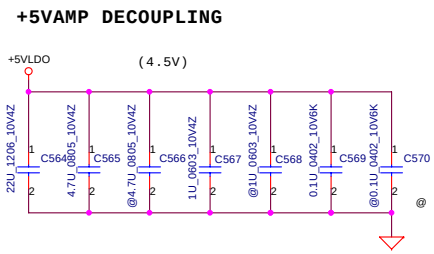


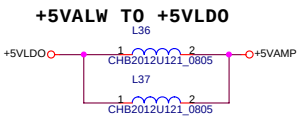
		Bias (Gain)	SPK 10 dB
R516	3.9K		
R519	7.15K		HP -6dB
R520	3.09K		

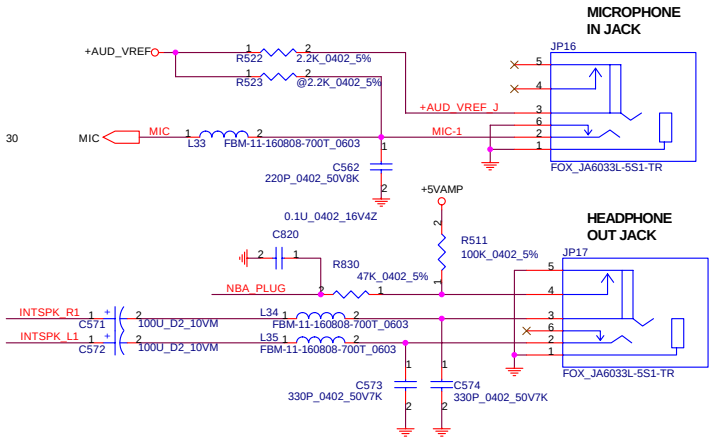
Regulator for AMP











Compal Electronics, Ltd.

Title: Audio AMP & JACK

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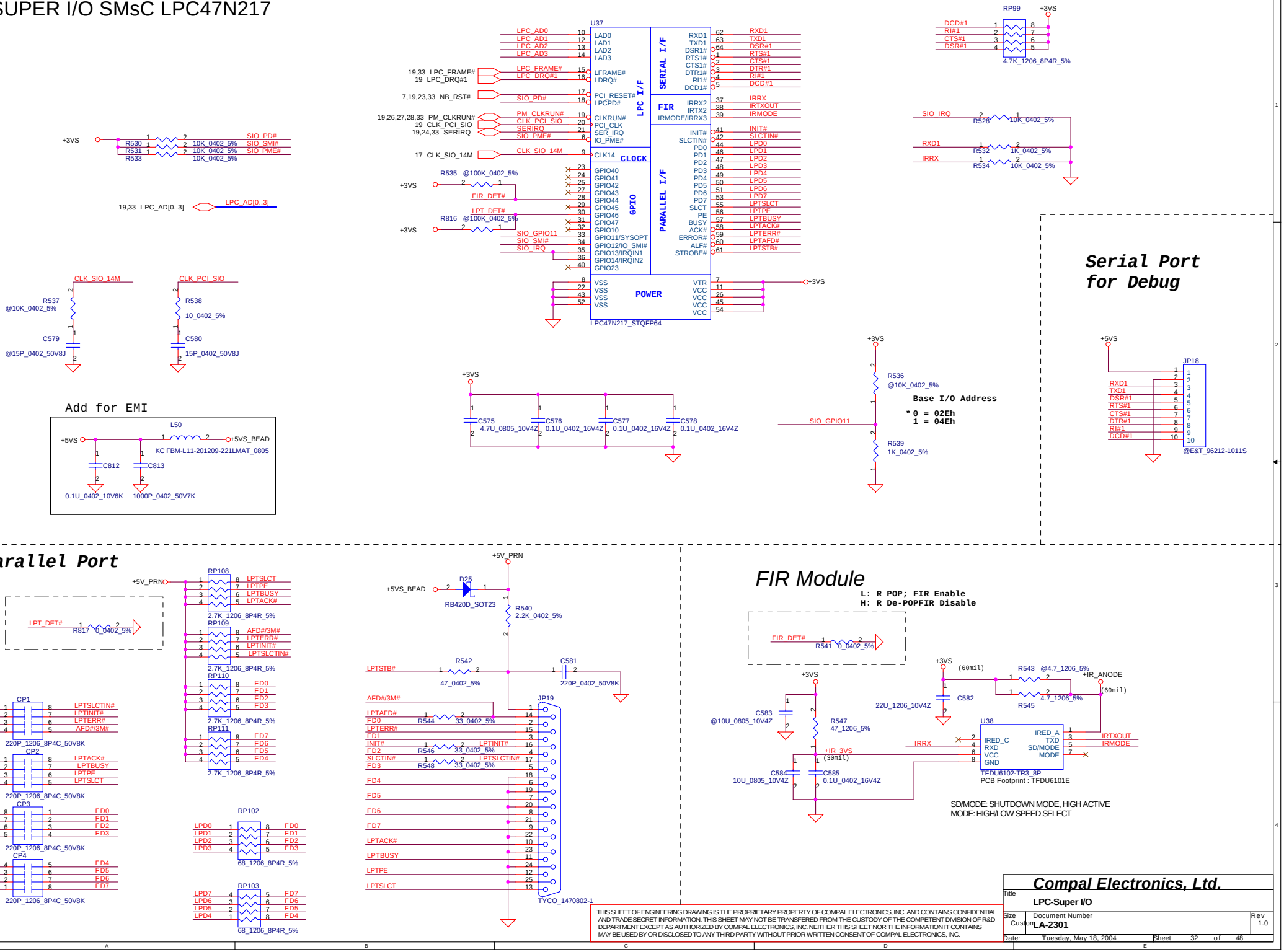
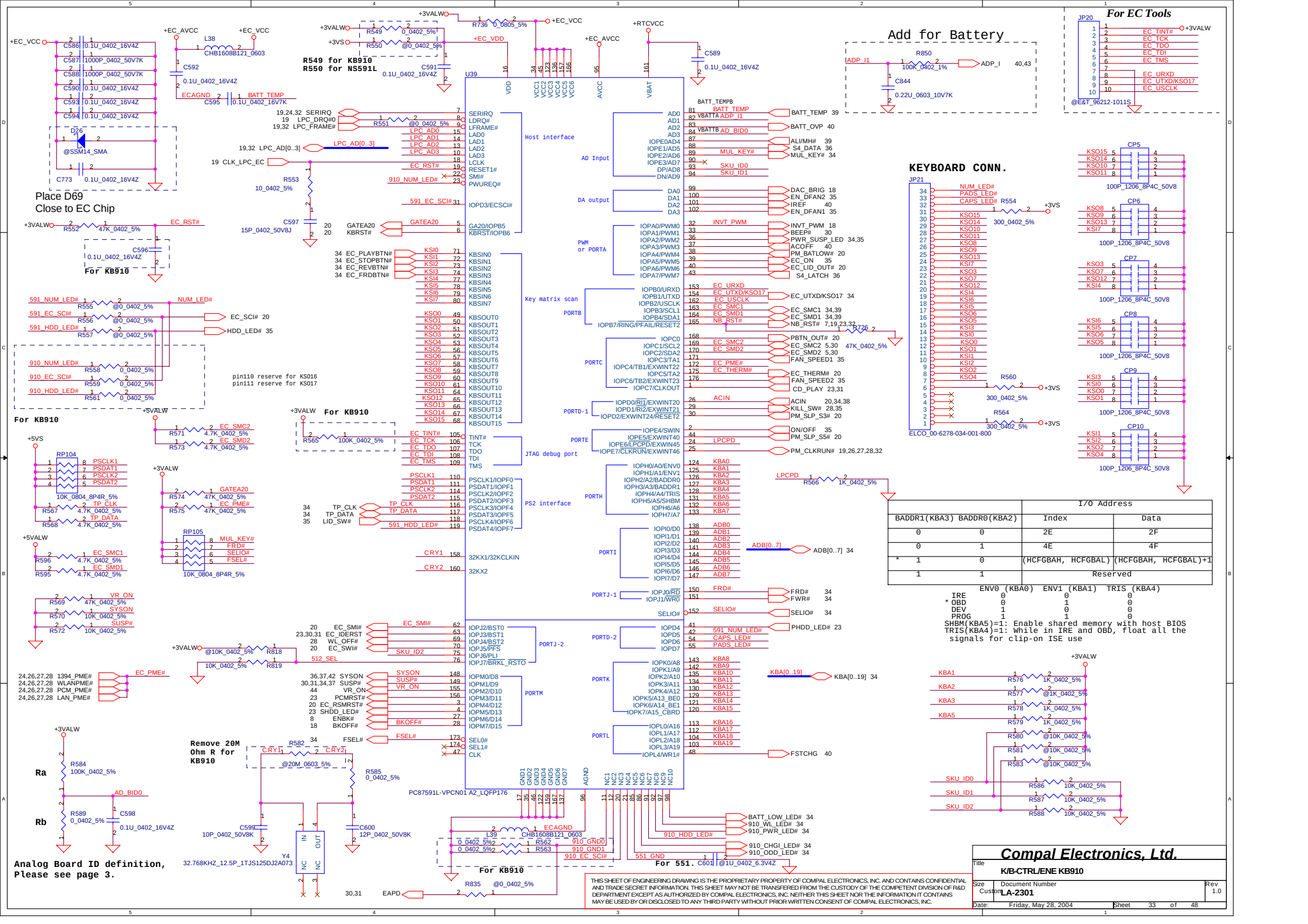
SUPER I/O SMsC LPC47N217



Compal Electronics, Ltd.		
Title: LPC-Super I/O		
Size: Custom	Document Number: LA-2301	Rev: 1.0
Date: Tuesday, May 18, 2004	Sheet 32 of 48	


For EC Tools
JP20
EC_TINT#
EC_TCK
EC_TDO
EC_TDI
EC_TMS
EC_URXD
EC_UTXD/KSO17
EC_USCLK
@E&T_96212-1011S
Add for Battery
ADP_I1
R850
100K_0402_1%
ADP_I 40,43
C844
0.22U_0603_10V7K
U39
PC87591L-VPCN01 A2_LQFP176
Host interface
AD Input
DA output
PWM or PORTA
Key matrix scan
PORTB
PORTC
PORTD-1
PORTE
JTAG debug port
PS2 interface
PORTH
PORTI
PORTJ-1
PORTJ-2
PORTD-2
PORTK
PORTM
PORTL
KEYBOARD CONN.
JP21
ELCO_00-6278-034-001-800
I/O Address
BADDR1(KBA3) BADDR0(KBA2) Index Data
0 0 2E 2F
0 1 4E 4F
* 1 0 (HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1
1 1 Reserved
ENV0 (KBA0) ENV1 (KBA1) TRIS (KBA4)
IRE 0 0 0
* OBD 0 1 0
DEV 1 0 0
PROG 1 1 0
SHBM(KBA5)=1: Enable shared memory with host BIOS
TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use
For KB910
Place D69
Close to EC Chip
Remove 20M Ohm R for KB910
Analog Board ID definition, Please see page 3.
pin110 reserve for KSO16
pin111 reserve for KSO17
Compal Electronics, Ltd.
K/B-CTRL/ENE KB910
LA-2301
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Friday, May 28, 2004
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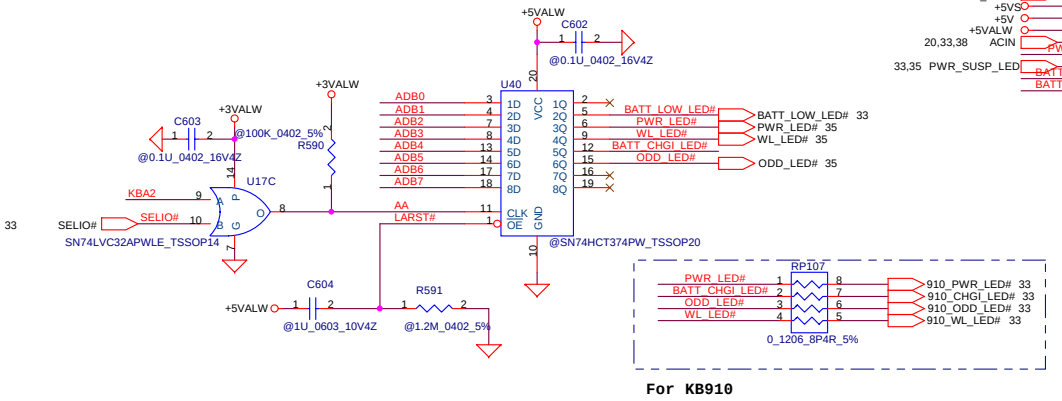
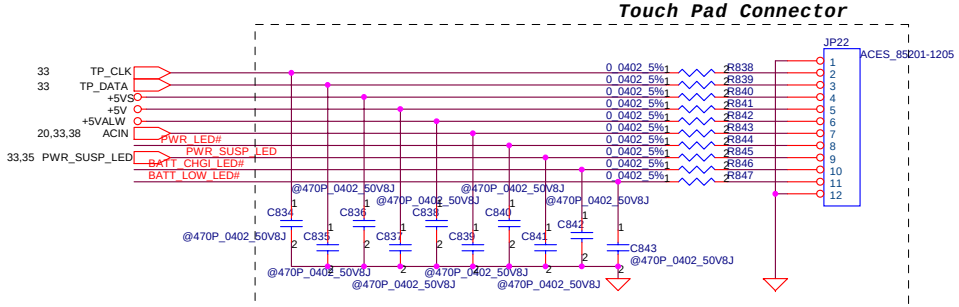
Extension IO



For KB910

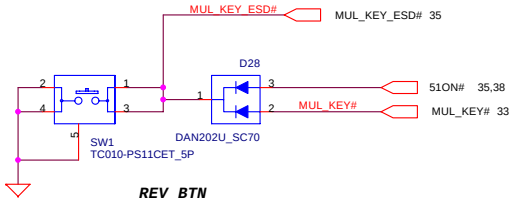
Touch Pad Connector



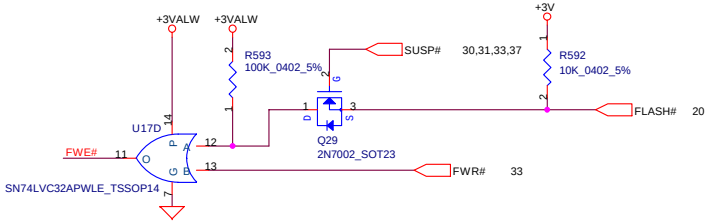
EMI Request

close connector

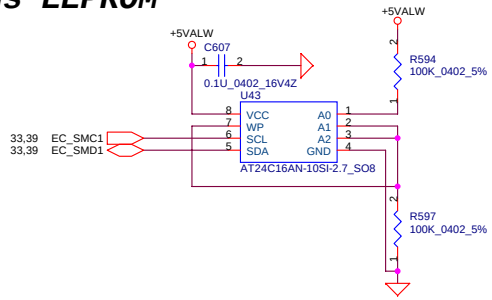
For MP3 / BUTTON LOCK / CD-PLAY



System BIOS



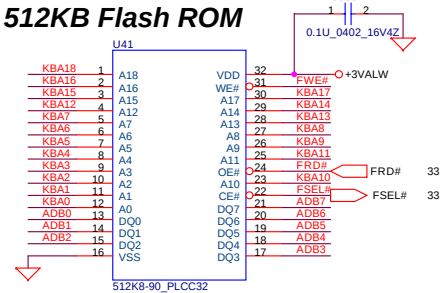
SMBus EEPROM



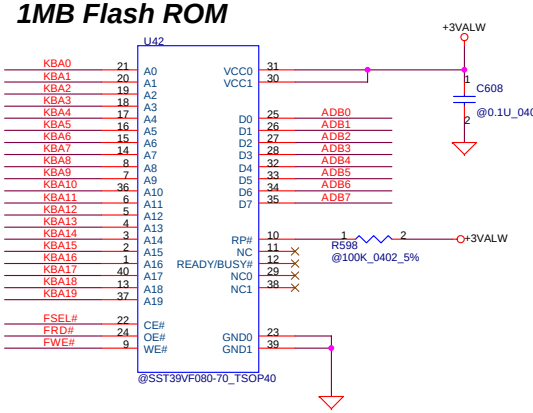
33 KBA[0..19] KBA[0..19]

33 ADB[0..7] ADB[0..7]

512KB Flash ROM



1MB Flash ROM

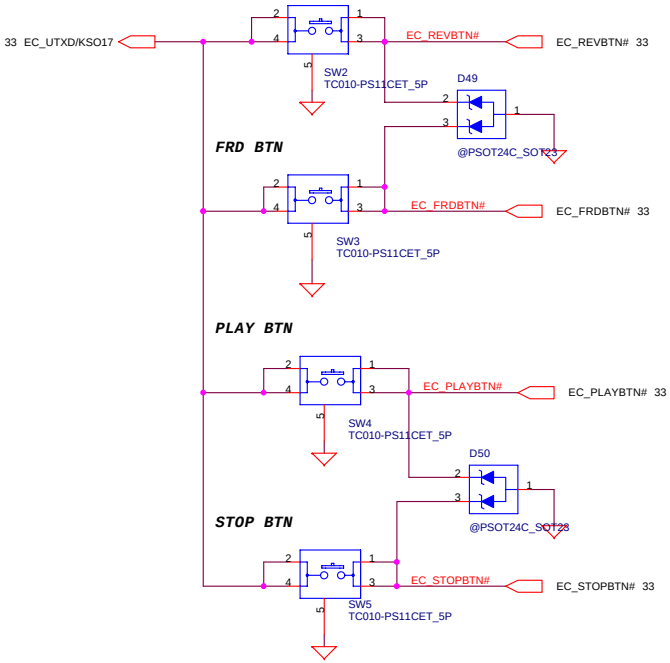


REV BTN

FRD BTN

PLAY BTN

STOP BTN



Compal Electronics, Ltd.

Title: BIOS & Ext.I/O

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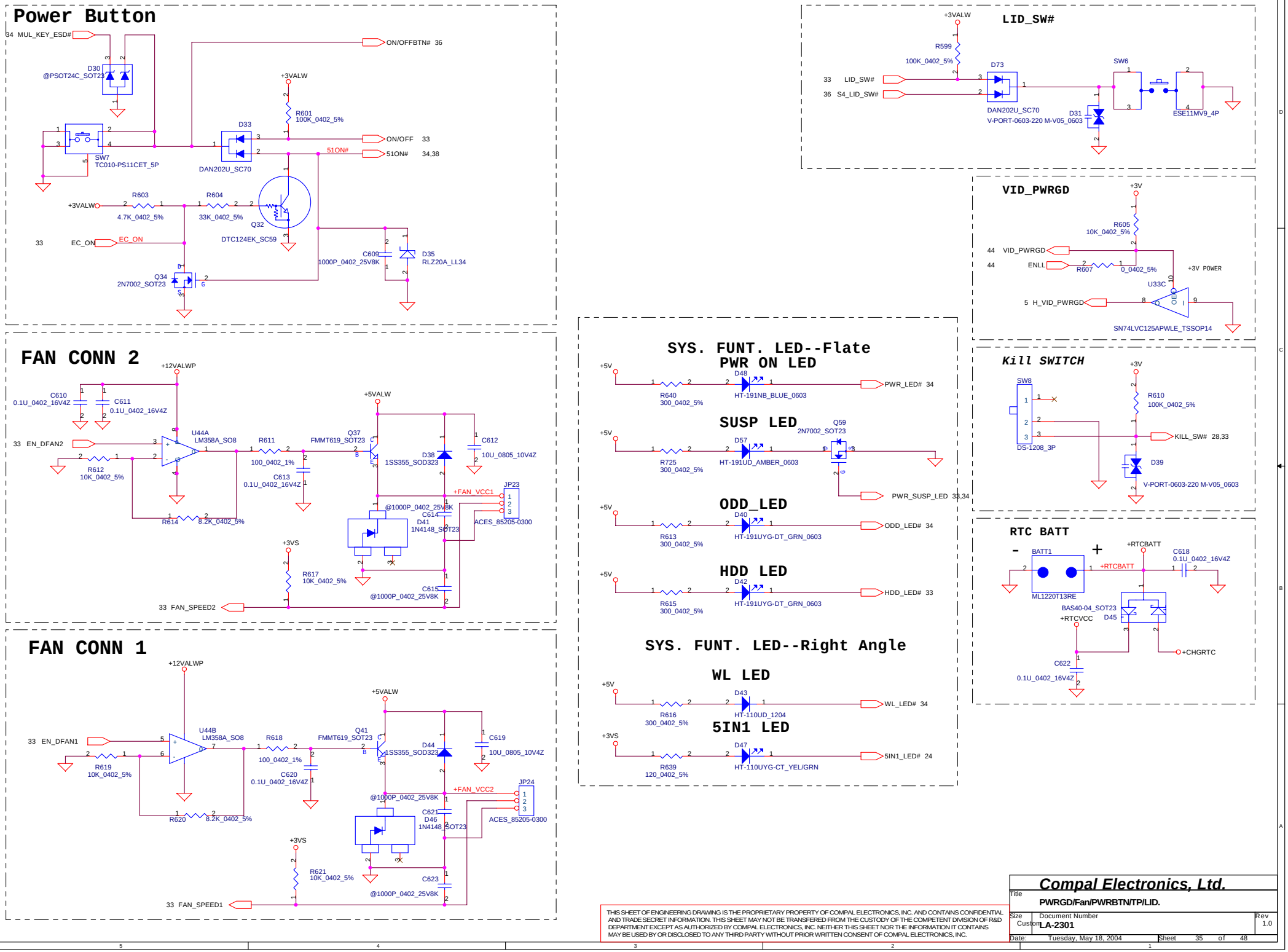

Compal Electronics, Ltd.		
Title: PWRGD/Fan/PWRBTN/TP/LID.		
Size: Custom	Document Number: LA-2301	Rev: 1.0
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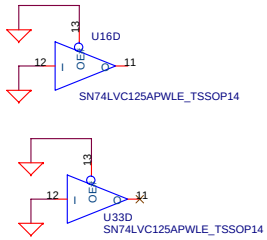


H20 H_S315D110
H23 H_S315D110
H21 H_S315D110
H22 H_S315D110
H24 H_S315D110
H27 H_S315D110
H25 H_S315D110
H26 H_S315D110
H28 H_S394D110
H29 H_S394D110
H33 H_C146D63
H34 H_C315D169
H36 H_S394D110

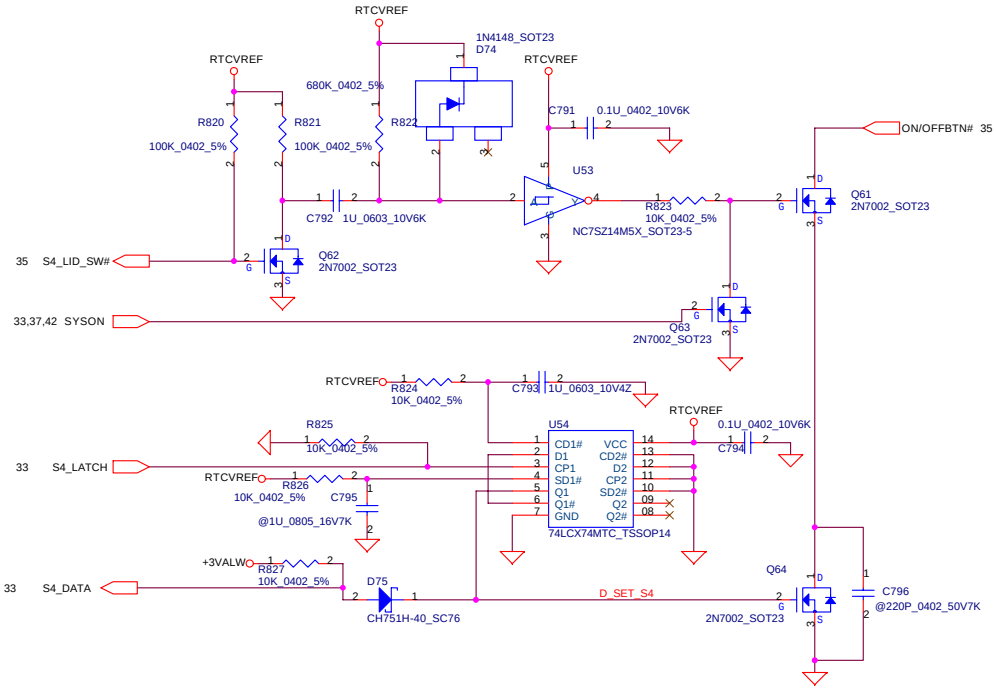
H1 H_C394D177
H4 H_C394D177
H2 H_C394D177
H3 H_C394D177
H5 H_C315D91
H8 H_C315D91
H6 H_C315D91
H7 H_C315D91
H9 H_C315D181
H10 H_C315D181
H11 H_C315D169
H19 H_O224X146D146X67
H32 H_S354D181
H18 H_C276D169

FD1 FIDUCAL
FD2 FIDUCAL
FD3 FIDUCAL
FD4 FIDUCAL
FD5 FIDUCAL
FD6 FIDUCAL

CF1 SMD40M80
CF2 SMD40M80
CF3 SMD40M80
CF4 SMD40M80
CF5 SMD40M80
CF6 SMD40M80
CF7 SMD40M80
CF8 SMD40M80
CF9 SMD40M80
CF10 SMD40M80
CF11 SMD40M80
CF12 SMD40M80
CF13 SMD40M80
CF14 SMD40M80

M1 H_O201X148D201X148N
M2 H_C79D79N
M3 H_O118X79D118X79N
M4 H_C148D148N
M5 H_C138D138N

Battery mode Hibernation



Compal Electronics, Ltd.

Title	ScrewHole	
Size: Custom	Document Number: LA-2301	Rev: 1.0
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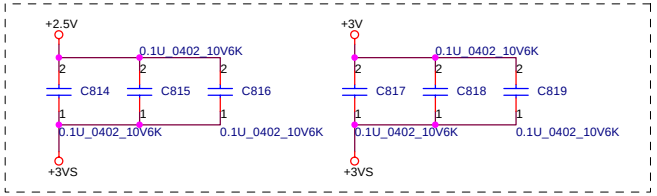
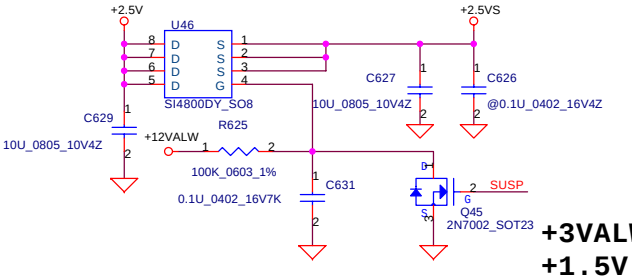
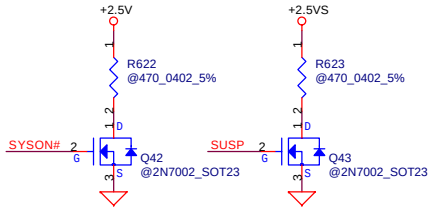
Add for EMI



+2.5V To +2.5VS Transfer

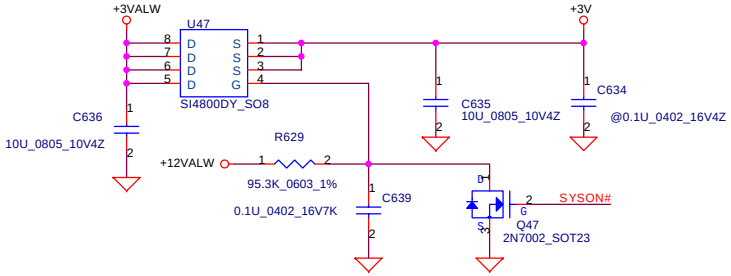


+2.5V & +2.5VS Discharge

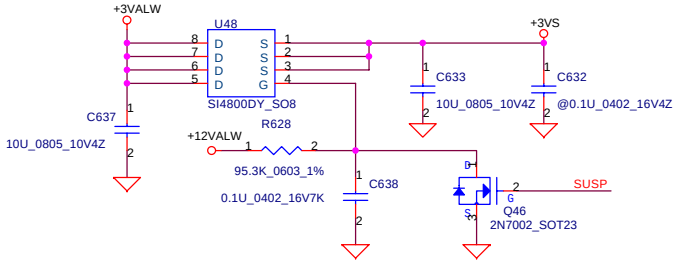


+3VALW AND +2.5VALW MUST RISING SAME TIME
+1.5V MUST DELAY AFTER +2.5V

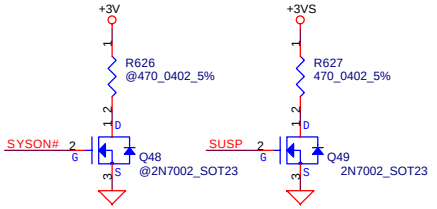
+3VALW To +3V Transfer



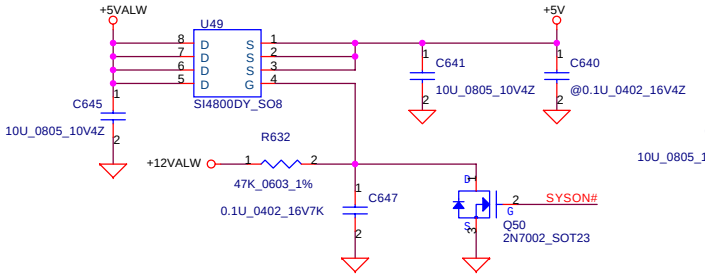
+3VALW To +3VS Transfer



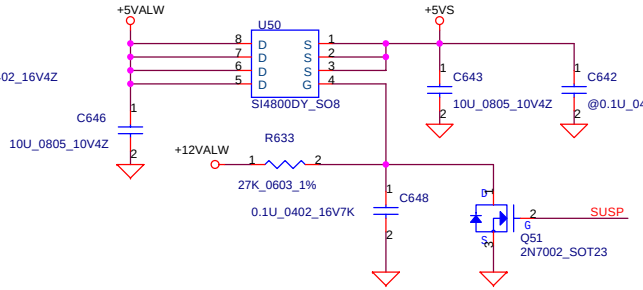
+3V & +3VS Discharge



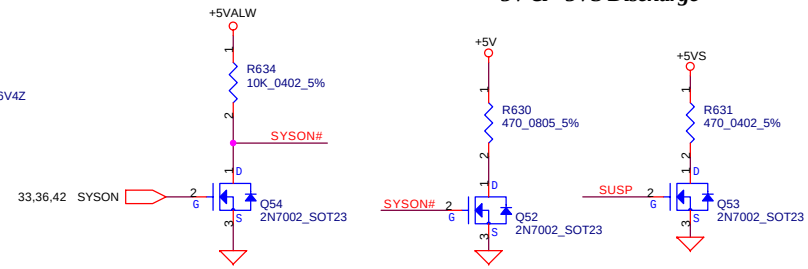
+5VALW To +5V Transfer



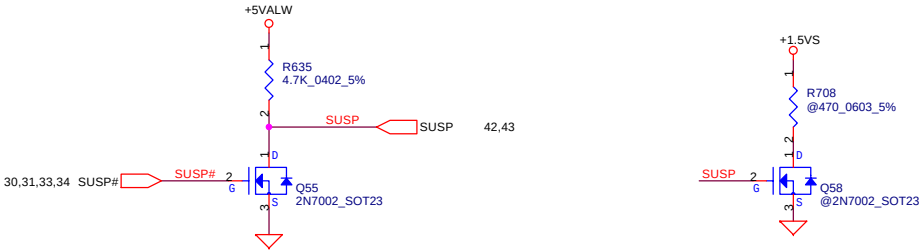
+5VALW To +5VS Transfer



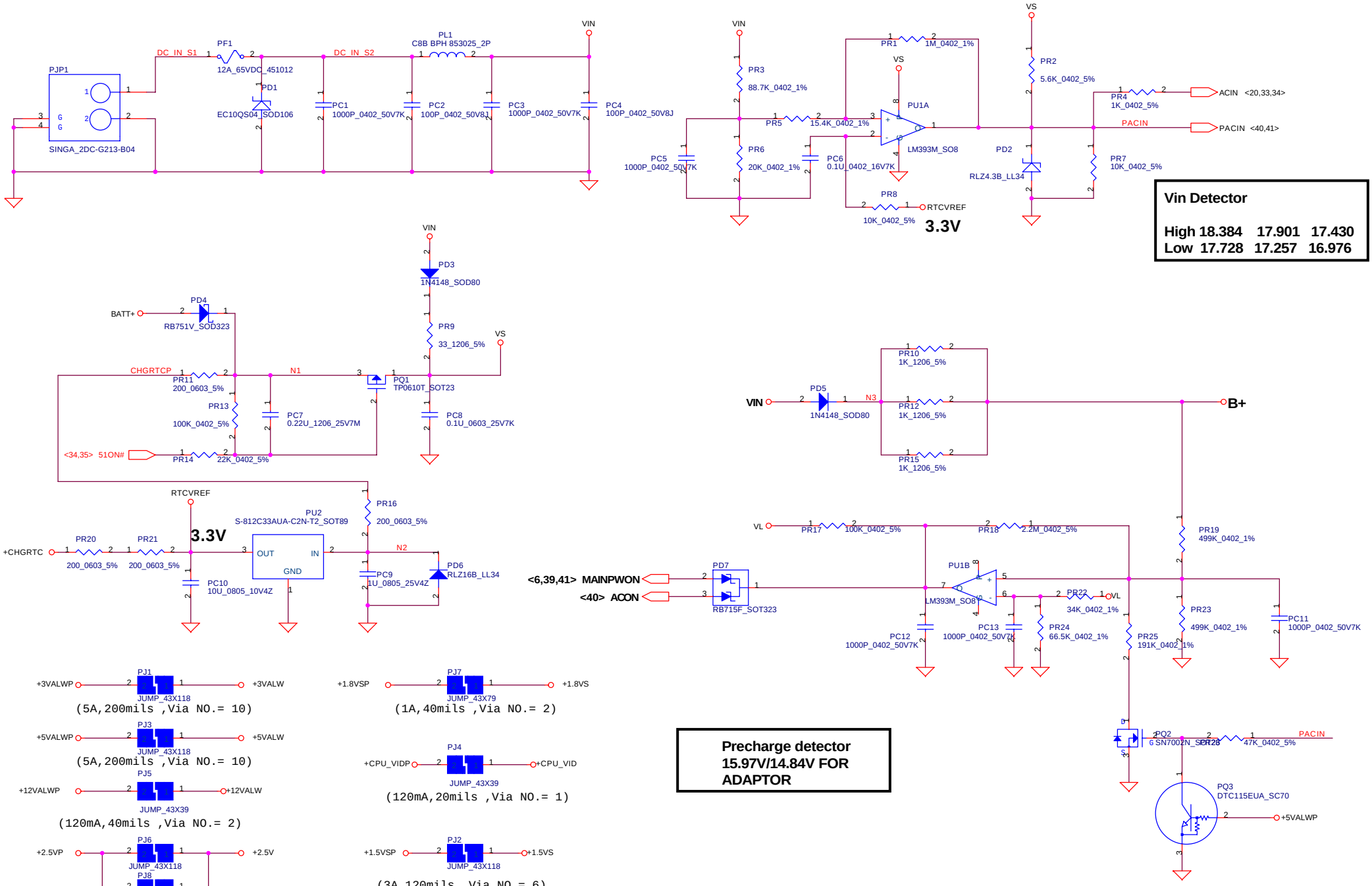
+5V & +5VS Discharge



+1.5VS Discharge

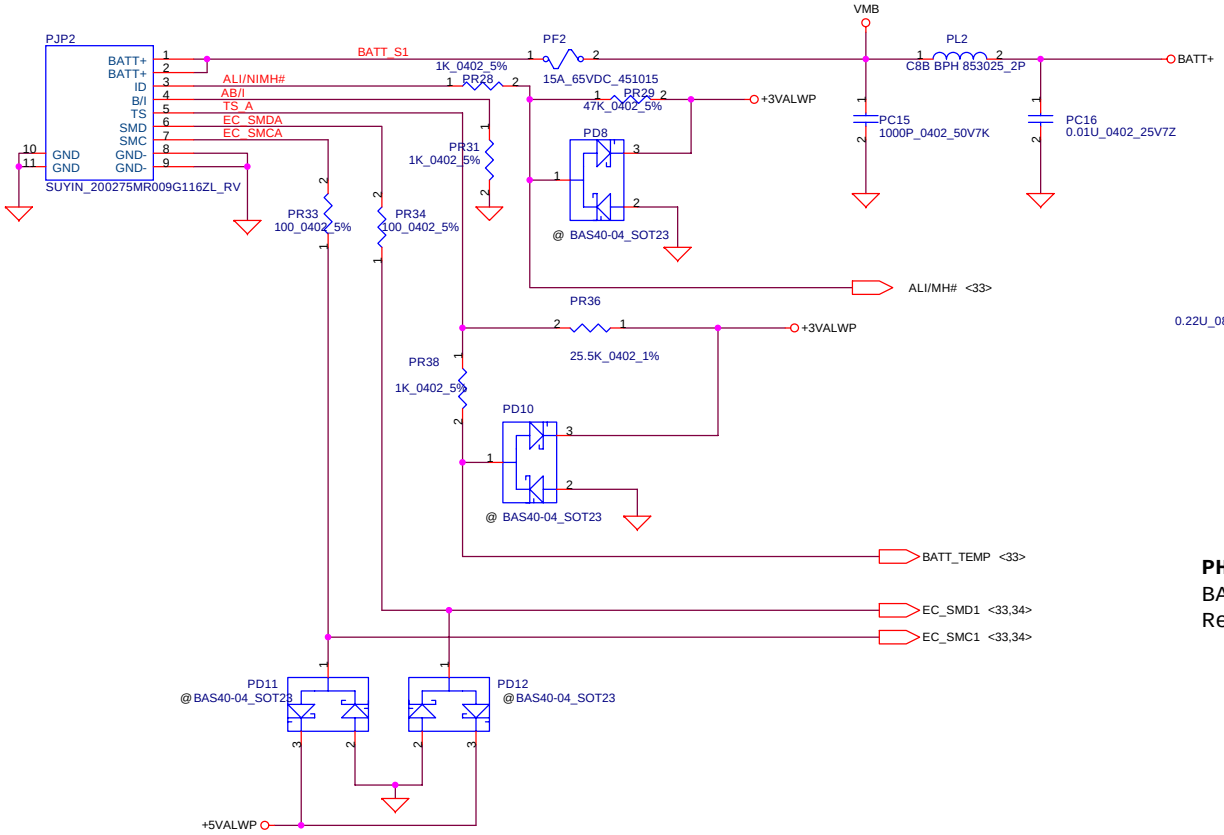


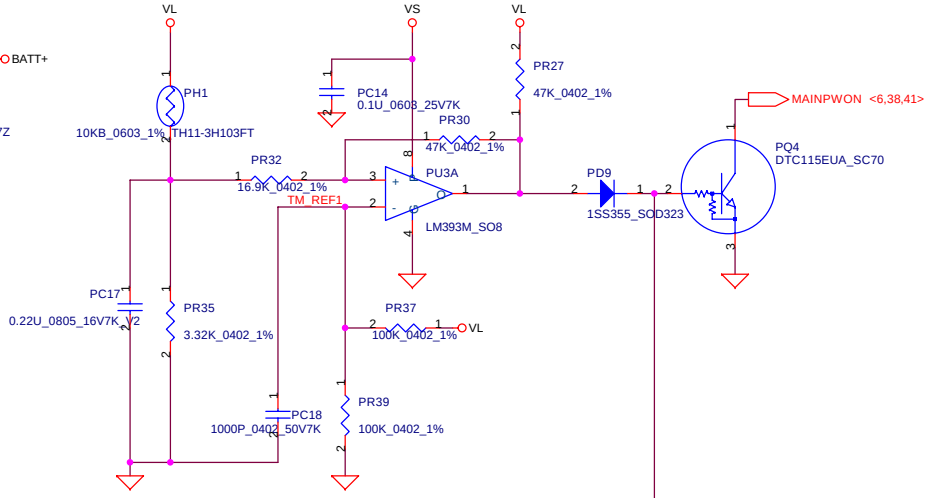
Compal Electronics, Inc.		
Title: DC-DC Circuit Interface		
Size: B	Document Number: LA-2301	Rev: 1.0
Date: Friday, May 28, 2004	Sheet 37 of 48	



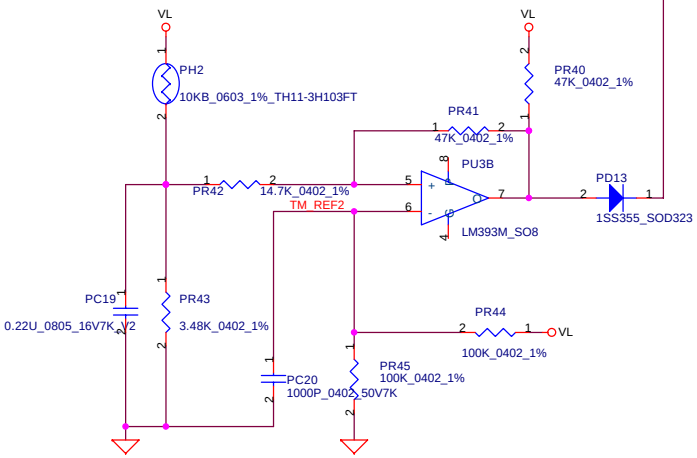
Compal Electronics, Inc.
Title: DCIN & DETECTOR
Size: Document Number: LA-2331
Rev: 1.0
Date: Tuesday, May 18, 2004
Sheet 38 of 48

PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C





PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C



Compal Electronics, Inc.		
Title: BATTERY CONN / OTP		
Size	Document Number: LA-2331	Rev: 1.0
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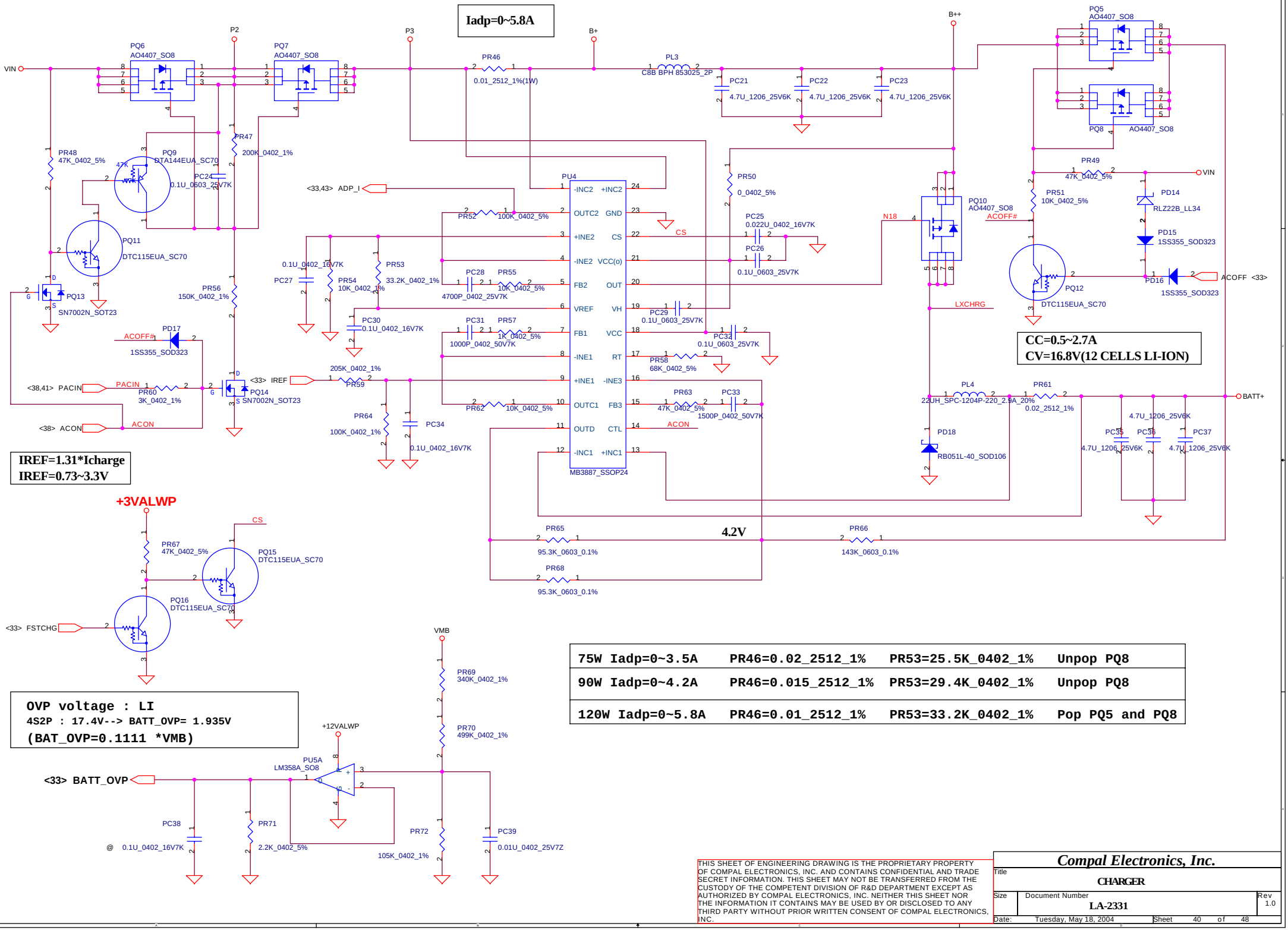

75W Iadp=0~3.5A	PR46=0.02_2512_1%	PR53=25.5K_0402_1%	Unpop PQ8
90W Iadp=0~4.2A	PR46=0.015_2512_1%	PR53=29.4K_0402_1%	Unpop PQ8
120W Iadp=0~5.8A	PR46=0.01_2512_1%	PR53=33.2K_0402_1%	Pop PQ5 and PQ8

Compal Electronics, Inc.
Title: CHARGER
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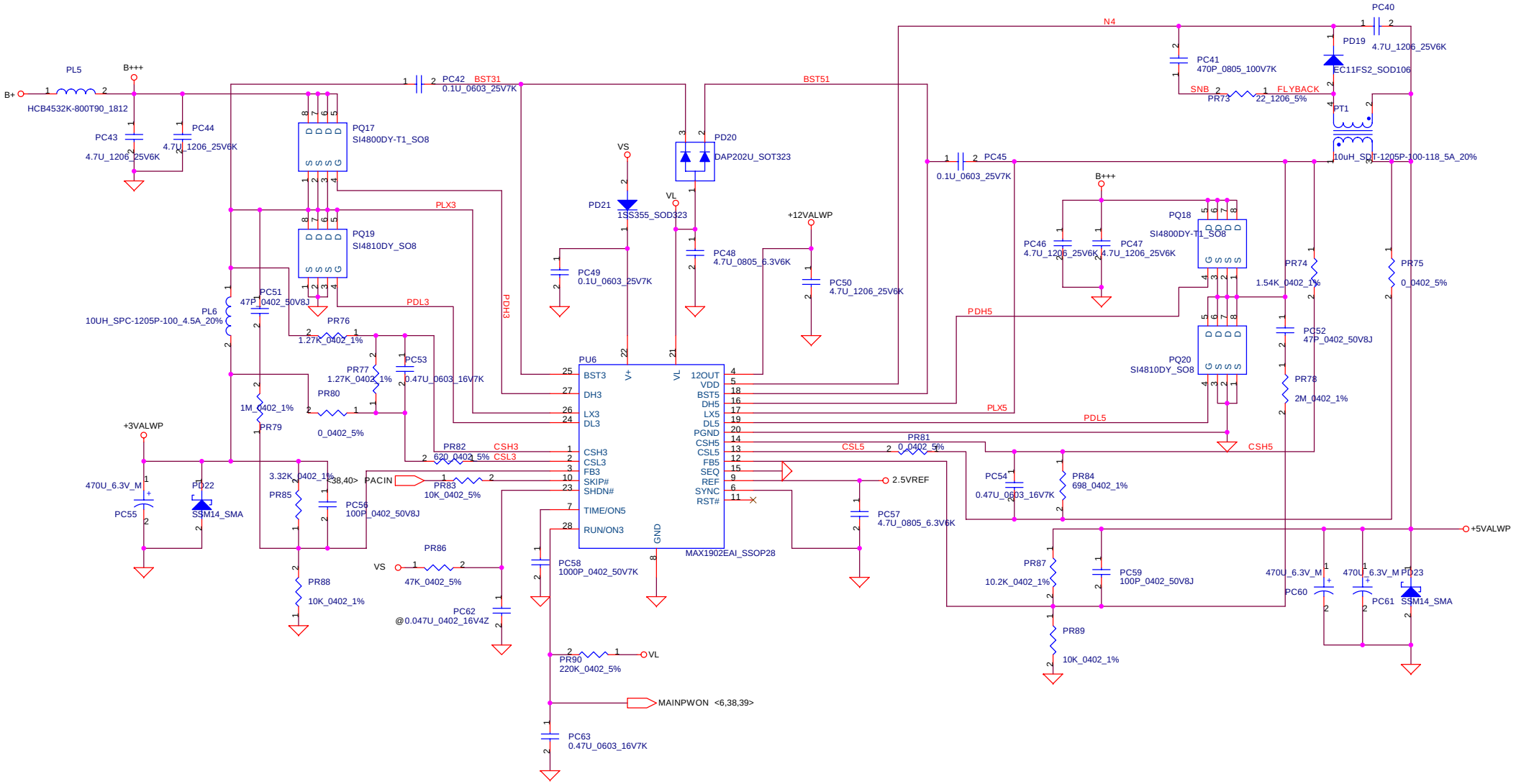
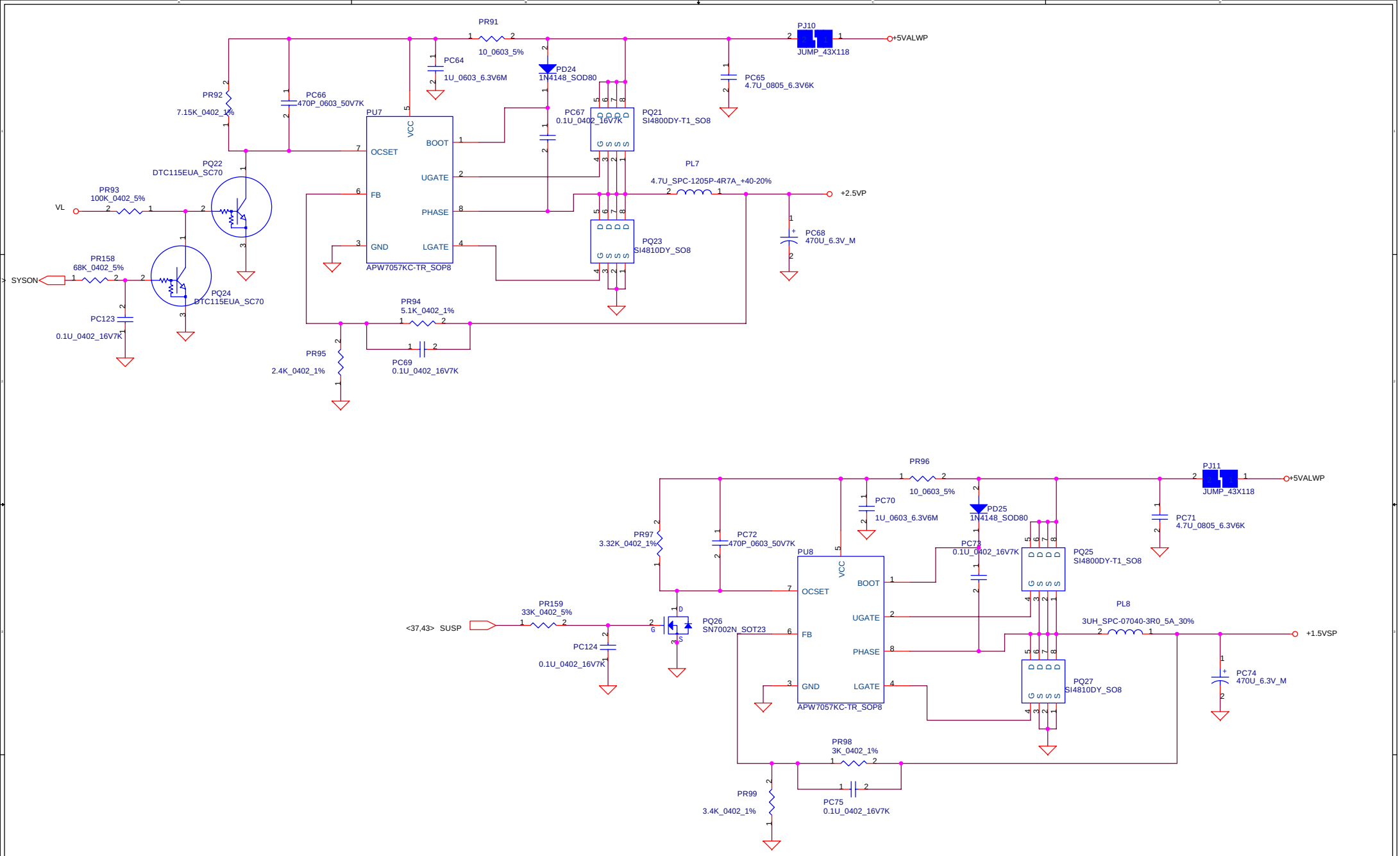


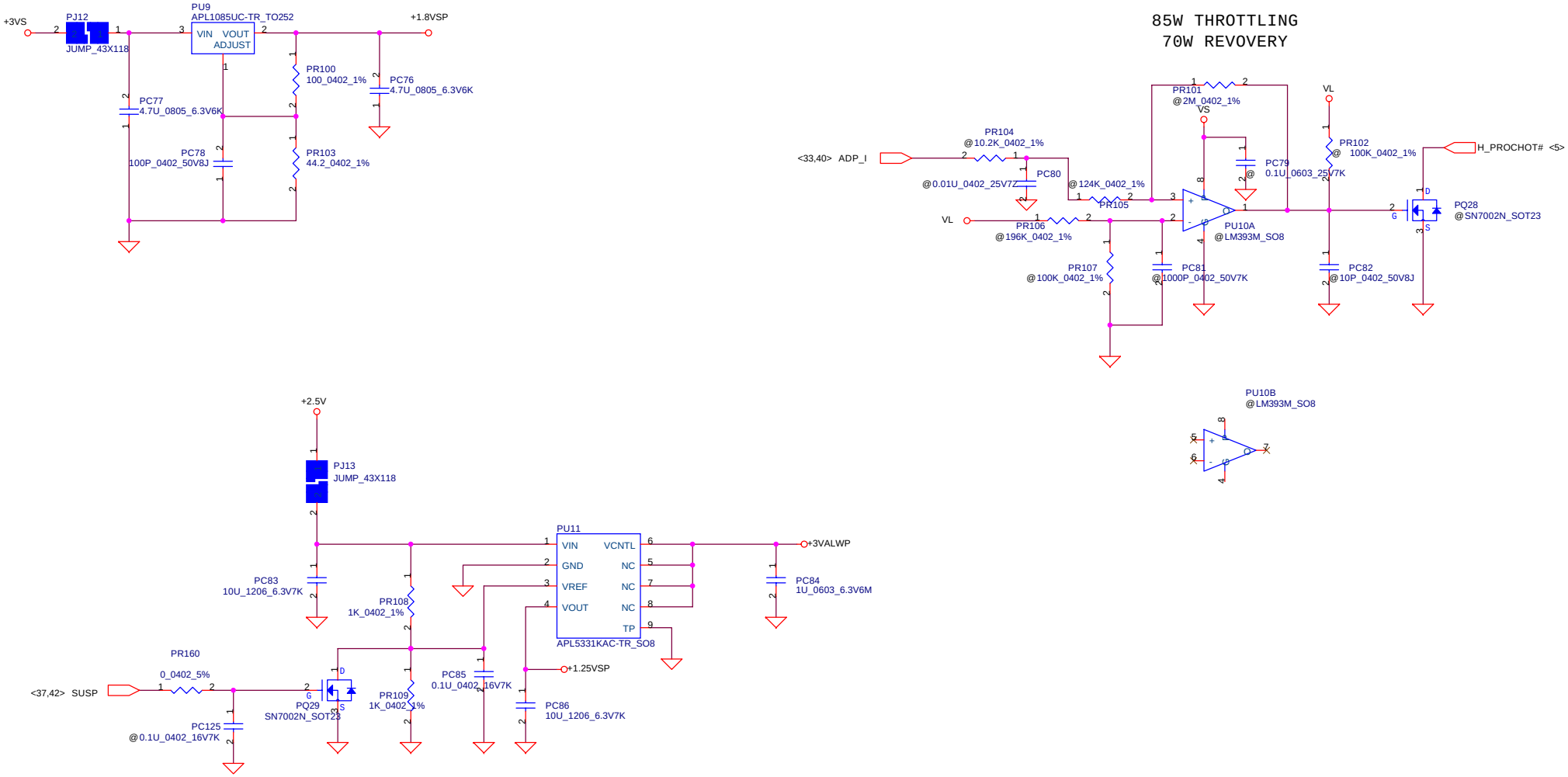
Compal Electronics, Inc.

Title	5V/3.3V/12V	
Size	Document Number: LA-2331	Rev: 1.0
Date: Tuesday, May 18, 2004	Sheet 41 of 48	

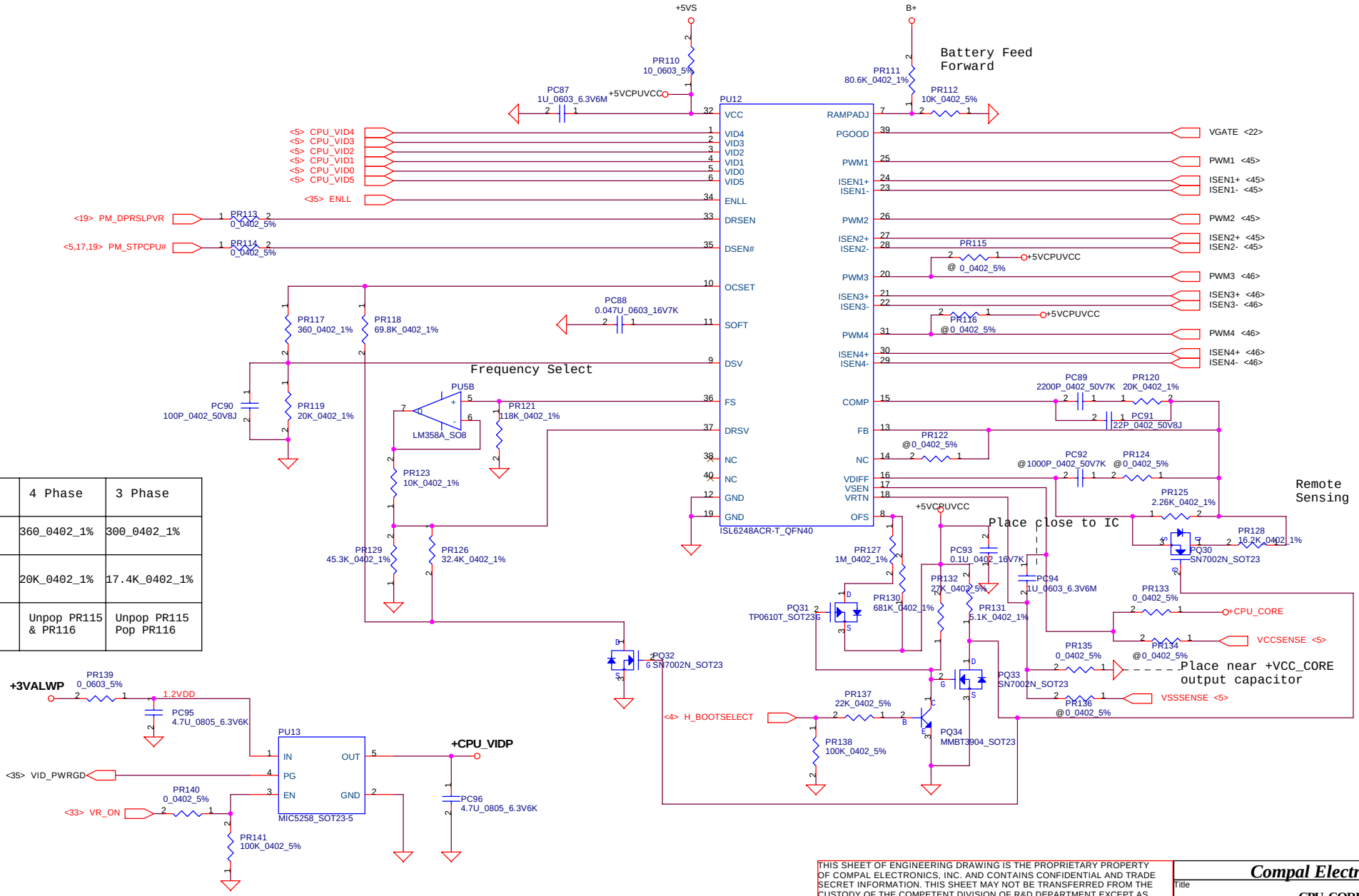


Compal Electronics, Inc.

Title	2.5V/1.5V	
Size	Document Number: LA-2331	Rev: 1.0
Date: Tuesday, May 18, 2004	Sheet 42 of 48	



Compal Electronics, Inc.		
Title: 1.8V/1.25V/PROCHOT		
Size	Document Number: LA-2331	Rev: 1.0
Date: Tuesday, May 18, 2004	Sheet 43 of 48	



	4 Phase	3 Phase
PR117	360_0402_1%	300_0402_1%
PR119	20K_0402_1%	17.4K_0402_1%
Others	Unpop PR115 & PR116	Unpop PR115 Pop PR116

Compal Electronics, Inc.
Title: CPU_CORE (1)
Size: Document Number: LA-2331
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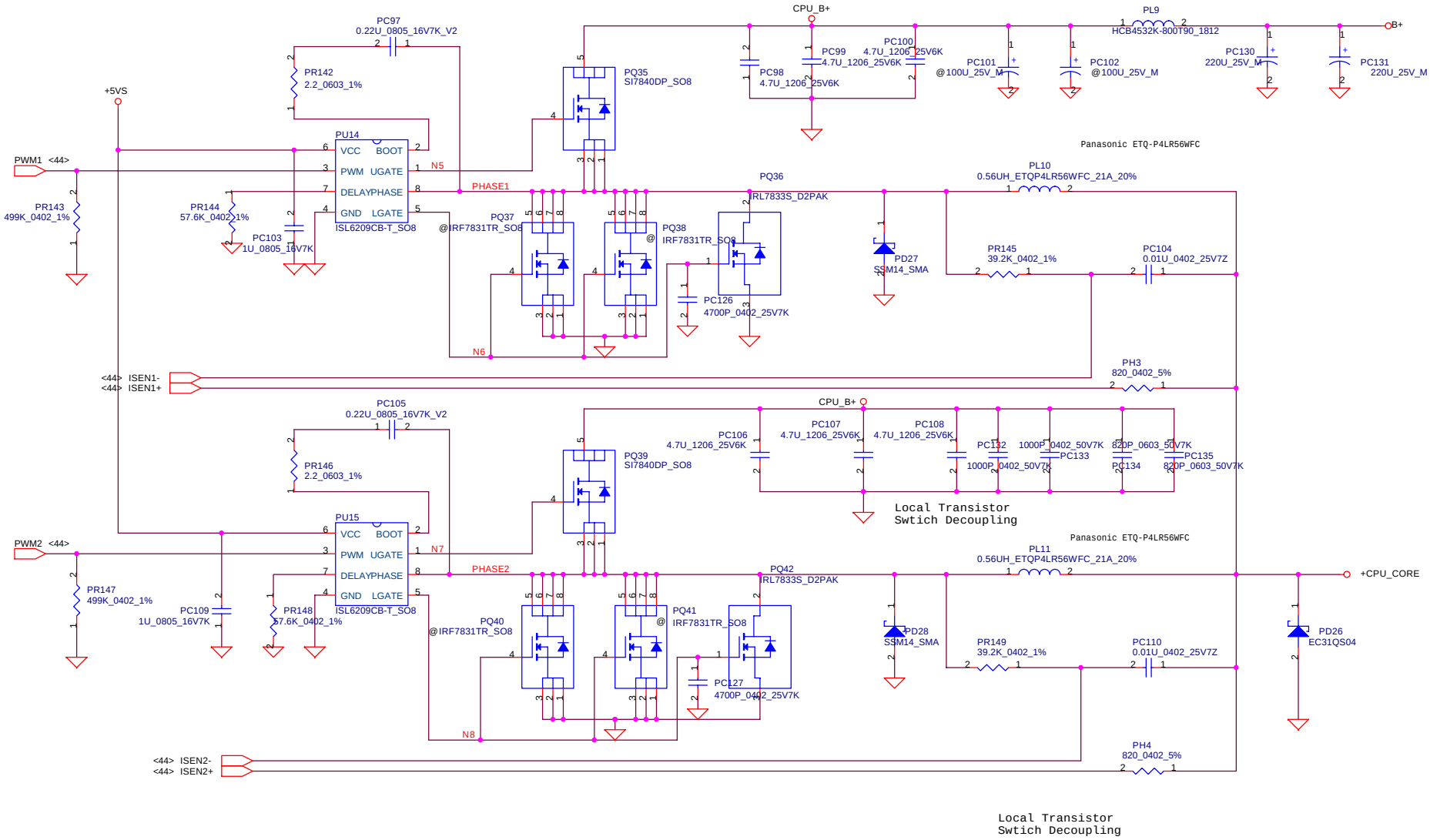

Compal Electronics, Inc.

Title: **CPU_CORE (2)**

Size	Document Number	Rev
		1.0

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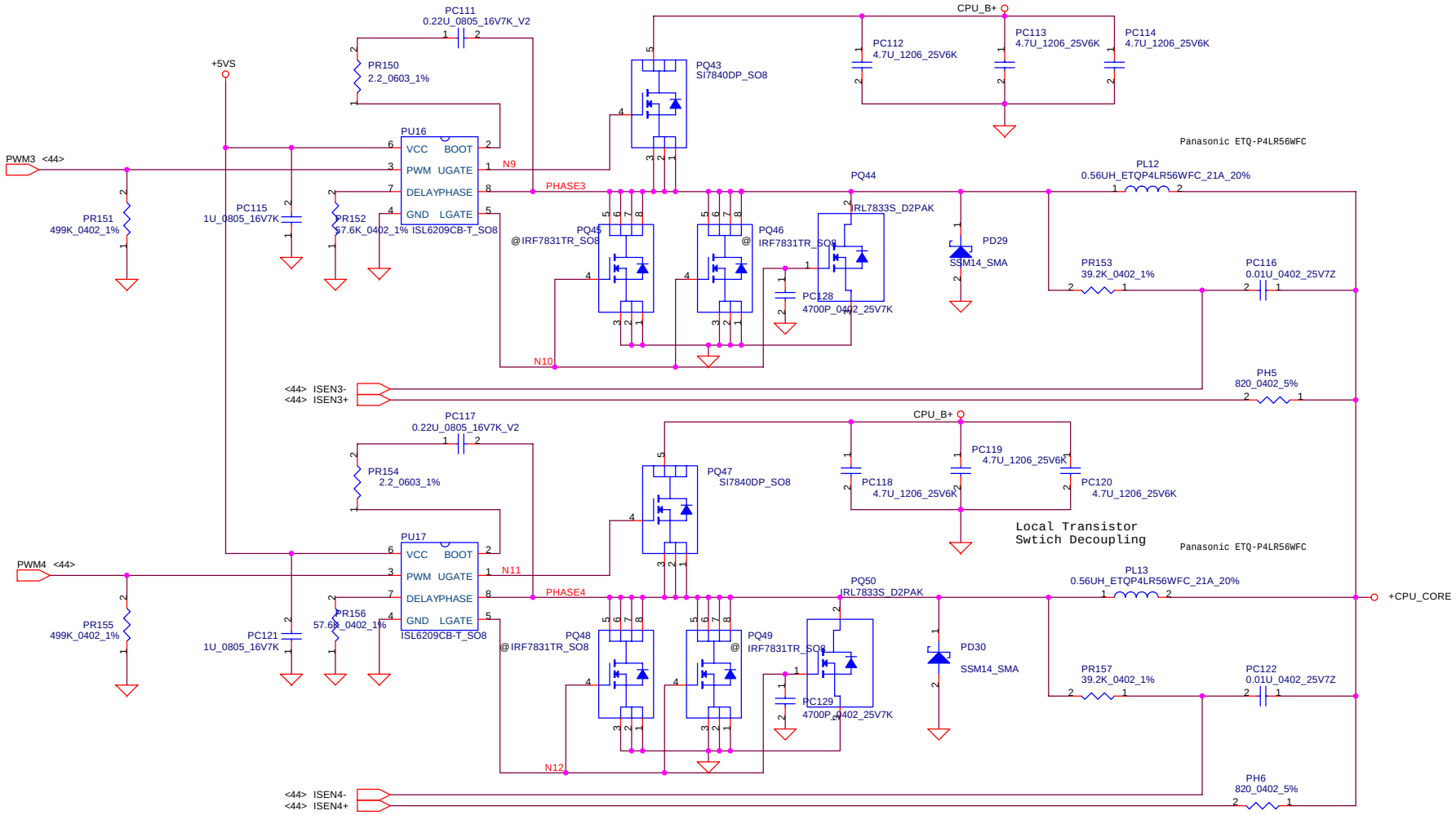

Compal Electronics, Inc.

Title	CPU_CORE (2)	
Size	Document Number	Rev 1.0
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REV 0.2

Date	Page	Description	Location
03/10	P.14,15	Add 16 Cap in on board DDR chip VDD pin	ADD C775 ~ C790
03/10	P.18	Del L9 & change L8 to bead for EMI	DEL L9 Change L8 to Bead
03/15	P.19	Redefine On board DDR strap pin	DEL R643, R646
03/15	P.21	Change SB +2.5valw power design	DEL R641 ADD Q60,D72
03/15	P.25	Change 5 In 1 connector	Change JP9
03/15	P.32	Add Parallel Port detect strap pin	ADD R817
03/15	P.27	Change 1394 connector footprint	NONE
03/16	P.33	Change EC SMbus2 pull high plwer plan from +5VALW to +3V	NONE
03/16	P.36	Add Battery Hibernation circuit	ADD U54,Q61 ~ Q64,U53,D75,D74,R822,R823 ~ R827,C791, C794,C792, C793,R820,R821

REV 0.3

04/5	P.23	Change ODD Conn. layout	
04/6	P.23	Del pull high resistor in SIO for with FIR & LPT	Unmount R535,R816
04/6	P.24	Add SMWP# Pull Low	Add R831
04/6	P.24	Add SDDA0~SDDA3 pull low	Add R833
04/12	P.30;31	Change SWDJ design	DEL R481,R486,R487,R463,R464,L24
04/12	P.30;31	Change SWDJ design	Add Q23,U34,C552,C555,R510,R503,R504,R507,R509,R512,R513,R514,R515,L25,R718

REV 0.4

04/22	P.35	Swap FAN1 & FAN2	
04/22	P.33	change SMBUS2 pull high from +3V to +5VALW	
04/22	P.25	Change XDBSY# power plan from +3VS to +5in_VCC	
04/22	P.25	Change SD_CLK damping value	Change R398 from 33ohm to 0ohm
04/29	P.20	For EMI request	Change USB 48MHZ R309 from 0 to 33
04/29	P.29	For EMI request	Add C828,C829,C830,C831,C832,C833
04/29	P.34	For EMI request	Add R838,R839,R840,R841,R842 Add R843,R844,R845,R846,R847 with Bead C834,C835,C836,C837,C838,C839,C840,C841,C842,C843
04/29	P.29	For POWER request	Add R850,C844
05/03	P.25	Change 5 in 1 design	Del R391,R392,R397,R399,R400,R401,R403,R413 Change R415,R407 FROM 43K TO 10K Change R411,R831 FROM 43K TO 2.2K Change R409 FROM 2.2K TO 10K Change R418 FROM 10K TO 43K
05/03	P.29	ADD CODEC DISABLE PULL HIGH	Add R853
05/03	P.29	LCD power up soft start	Change R246 from 150k to 200k & add C272
05/03	P.29	Change USB power switch	Change U55,U30 to G528
05/03	P.24	Change SM_CD# deaign	Add R852
05/03	P.25	Del PCMCIA 12V Cap	Del C408
05/06	P.20	Change USB 12.4K to 12K to improve USB signal quality	Change R311 from 12.4K to 12K

REV 1.0

05/06	P.25	Reserve Q65 and C845 and change C823 to 1206 size	
05/16	P.25	Change Audio CLK from CLK GEN to Crystal	Add X6,C518,C519 Del R471,R485,R219
05/26	P.21	Change R324 from 100 ohm to 1k ohm solve ODD noice issue	

PWR PIR LIST

EVT2

page	Reason for change	Modify list
45	Change material for ME limit	Change PC101 from 220U_25V(10X10.5) to 100U_25V(6.3X7.7)
45,46	For CPU transient and loadline	Change PR145,PR149,PR153,PR157 from 34.8K to 39.2K Change PR130 from 340K to 681K
45,46	Change material's tolerance	Change PC103,PC109,PC115,PC121 from Y5V to X7R
45,46	Intersil suggest	Add PD27,Pd28,PD29,PD30(SSM14) Add PC126,PC127,PC128,PC129(3300P)
Create 90W BOM		
38,42,43	Add bead for EMI require	Add PL14,PL15,PL16,PL17,PL18
38	Modify ACIN detect signal	Change PR3 from 88.7K to 84.5K Change PR5 from 15.4K to 22K Change PR48 from 150K_5% to 47K_5%
41	Adjust 3.3V and 5V OCP	Change PR76 from 1.27K to 1.87K Change PR77 from 1.27K to 3.74K Change PR82 from 620 to 1.24K Change PR74 from 1.54K to 1.27K Change PR84 from 698 to 1.82K
42	Add 2.5V delay for HW require	Change PR158 from 0 to 68K Add 0.1u at PC123
42	Modify 1.5V OCP point	Change PR97 from 3.32K to 2.8K Change PL8 from 5u to 3u
42	Add 1.5V delay for HW require	Change PR159 from 0 to 33K Add 0.1u at PC124
45	Add CAP at CPU_CORE input for EMI	Add 1000P at PC132,PC133 Add 820P at PC134,PC135
42,43	Delete bead for EMI	Delete PL14~PL18 and change to jumper

DVT

45	Change CPU_CORE input CAP	Delete PC101 Add 220U_25V(10X10.5) at PC130,131
45,46	Add 2.2 ohm at CPU_CORE driver's boost for EMI	Change PR142,PR146,PR150,PR154 to 2.2_0603_1%
38,39	Change to common parts	Change PC7 to 0.1U_0805_25V change PC17,PC19 to 0.22U_0805_16V

Compal Electronics, Inc.
Title: EDW10 PIR LIST
Size: B | Document Number: FortWorth 20 | Rev: 1.0
Date: Tuesday, May 18, 2004 | Sheet 48 of 48