

Compal Confidential

Fortworth Banias EAL20 LA-2461 Schematic

uFC-PGA Dothan / Montara-GM+
M11P-128M VRAM / ICH4-M

2004-08-17

REV: 1.0

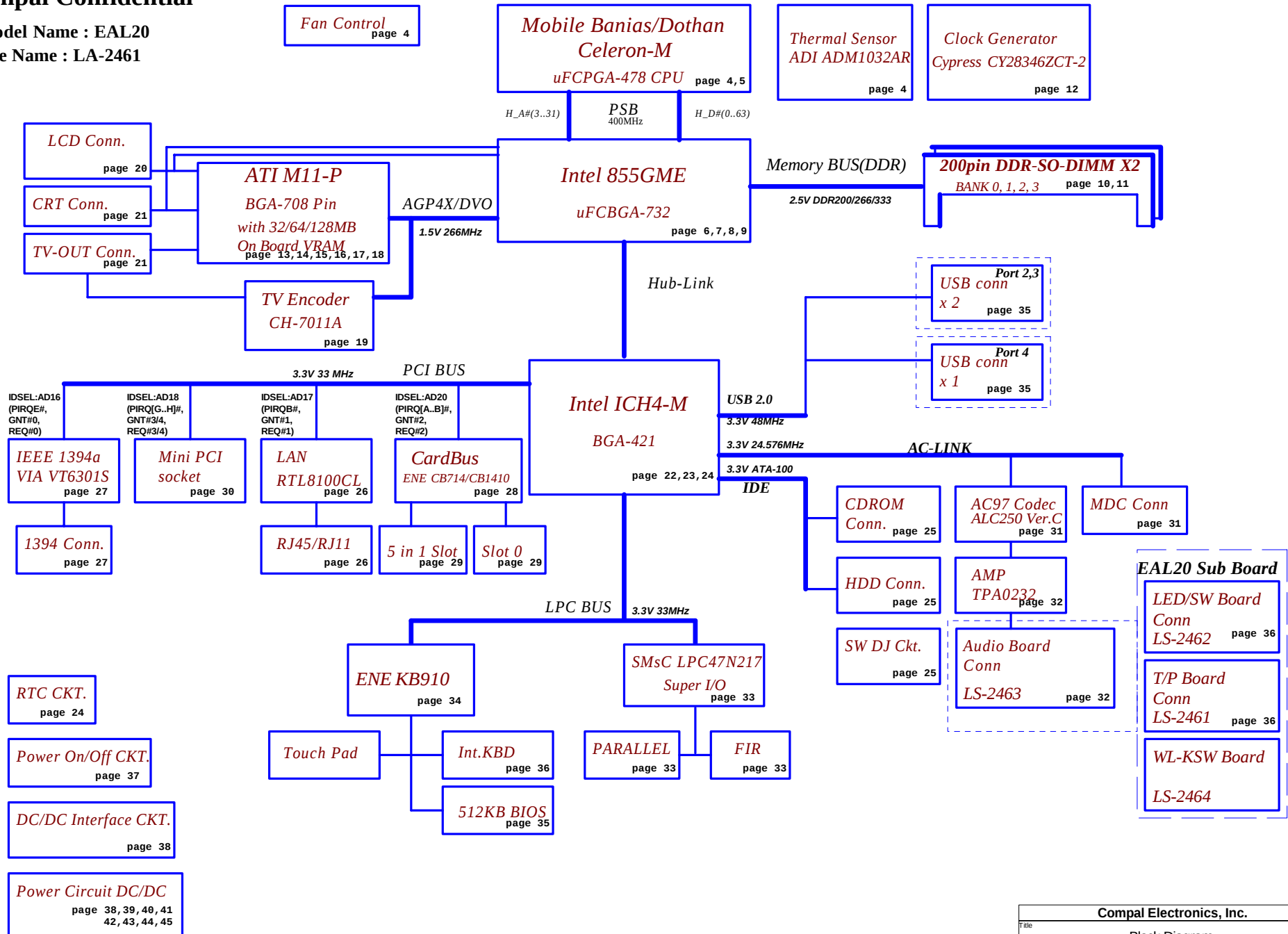
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Model Name : EAL20

File Name : LA-2461



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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V rail for Processor I/O	ON	OFF	OFF
+1.25VS	1.25V switched power rail for DDR Vtt	ON	OFF	OFF
+VGA_CORE	1.2V/1.0V switched power rail for VGA core power	ON	OFF	OFF
+1.35VS	1.35V switched power rail for GMCH core power	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail for AGP interface	ON	OFF	OFF
+1.8VS	1.8V switched power rail for CPU PLL & Hub-Link	ON	OFF	OFF
+2.5V	2.5V power rail for system DDR	ON	ON	OFF
+2.5VS	2.5V power rail for VGA DDR	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V switched power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTC/VCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

ICH4-M I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 X
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 X

KB910 I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
SM1 24C16	A0H	1 0 1 0 0 0 0 X b
SM1 SMART BATTERY	16H	0 0 0 1 0 1 1 X b
SM2 ADM0132 CPU THERMAL MONITOR	98H	1 0 0 1 1 0 0 X b
SM2 ALC250 AUDIO CODEC	00H	0 0 0 0 0 0 0 X b

External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
1394	D0	AD16	0	E
LAN	D1	AD17	1	F
CARD BUS	D4	AD20	2	A
5IN1	D4	AD20	2	B
Mini-PCI	D2	AD18	3,4	G,H
AGP BUS	N/A	AGP_DEVSEL#	N/A	A

Symbol note:



:means digital ground.



:means analog ground.



@ :means reserved.

Fortworth Banias Comparison Table

Item	* Descrite	UMA	Page
VGA	ATI M11P	UMA	13 ~ 16
VRAM	128MB/64MB	NA	13 ~ 14
TV Encoder	NA	CH7011A	19

Board ID Table for AD channel

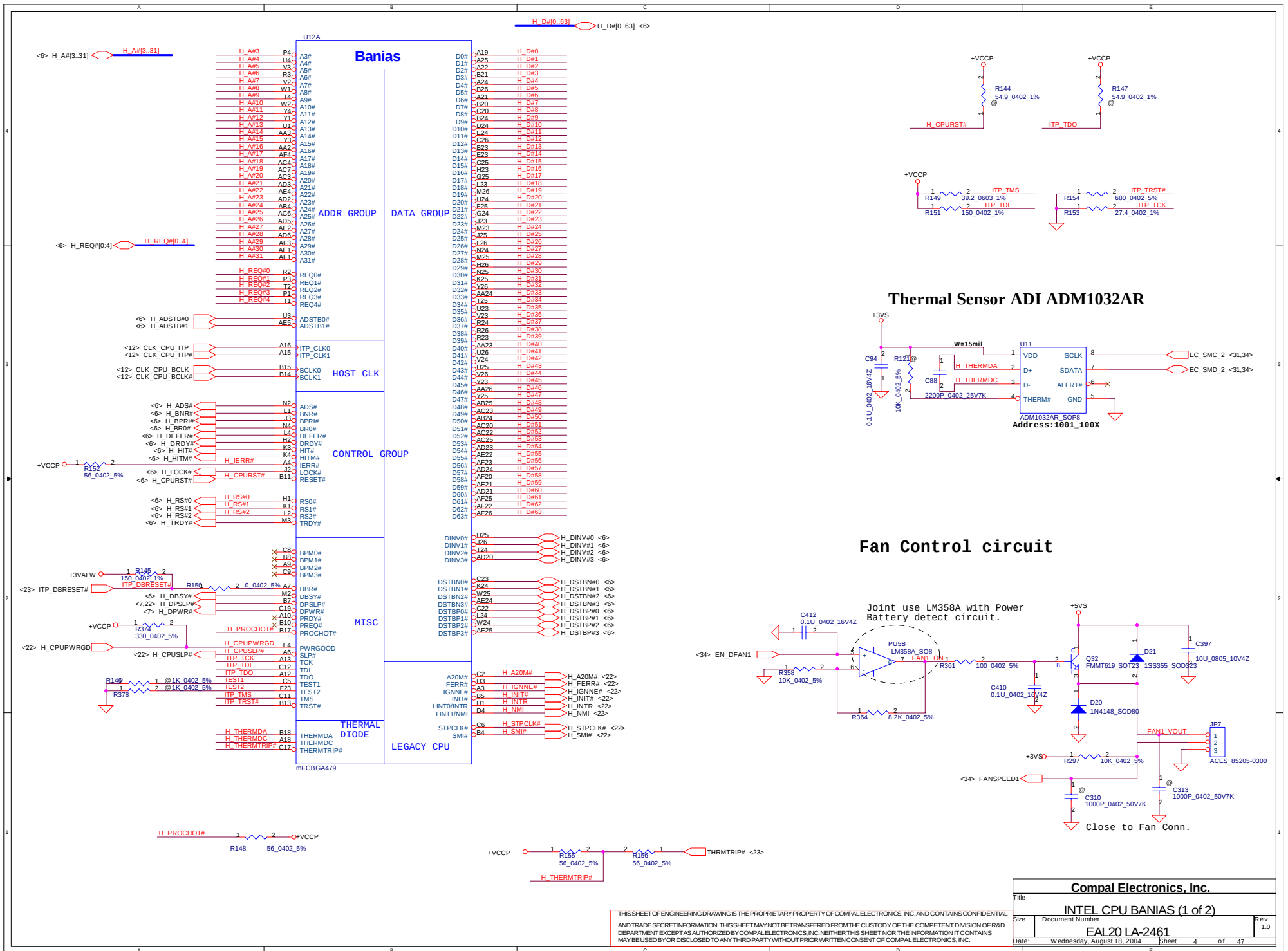
Vcc	3.3V +/- 5%			
Ra	10K +/- 5%			
BID/PID	Rb/Rc	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	1.412 V	1.486 V	1.560 V
2	18K +/- 5%	2.015 V	2.121 V	2.227 V
3	33K +/- 5%	2.406 V	2.533 V	2.659 V
4	56K +/- 5%	2.660 V	2.800 V	2.940 V
5	NC	3.135 V	3.300 V	3.465 V

Board ID	PCB Revision
* 0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

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Dothan VCCA update(WW45 2003)
Dothan B-Step support 1.5V only for VCCA

Resistor placed within
0.5" of CPU pin.Trace
should be at least 25
miles away from any
other toggling signal.

Resistor placed within
0.5" of CPU pin.Trace
should be at least 25
miles away from any
other toggling signal.

Banias
POWER, GROUND, RESERVED SIGNALS AND NC

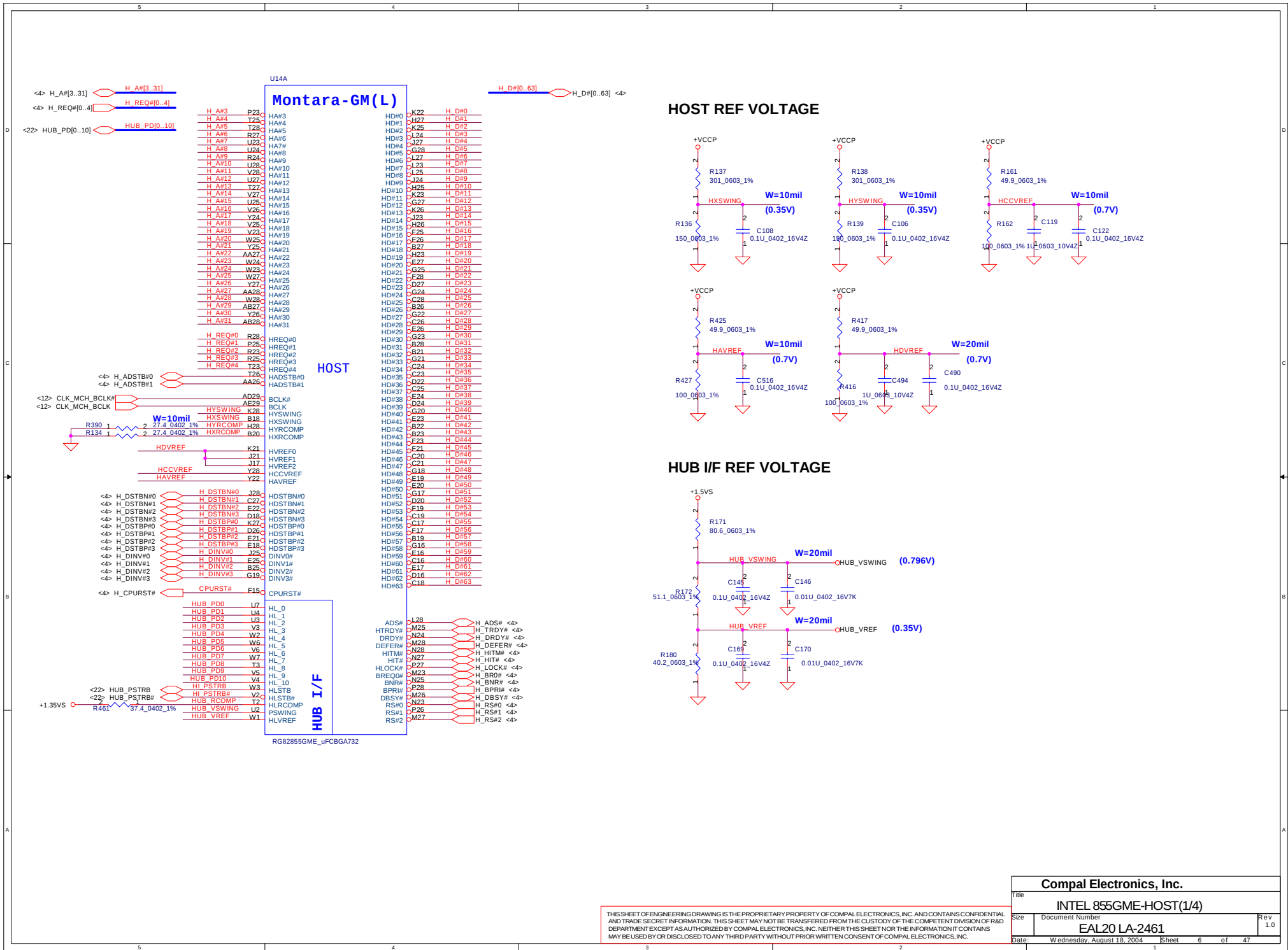
Vcc-core Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	4X220uF	12m ohm/4	3.5nH/4
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35

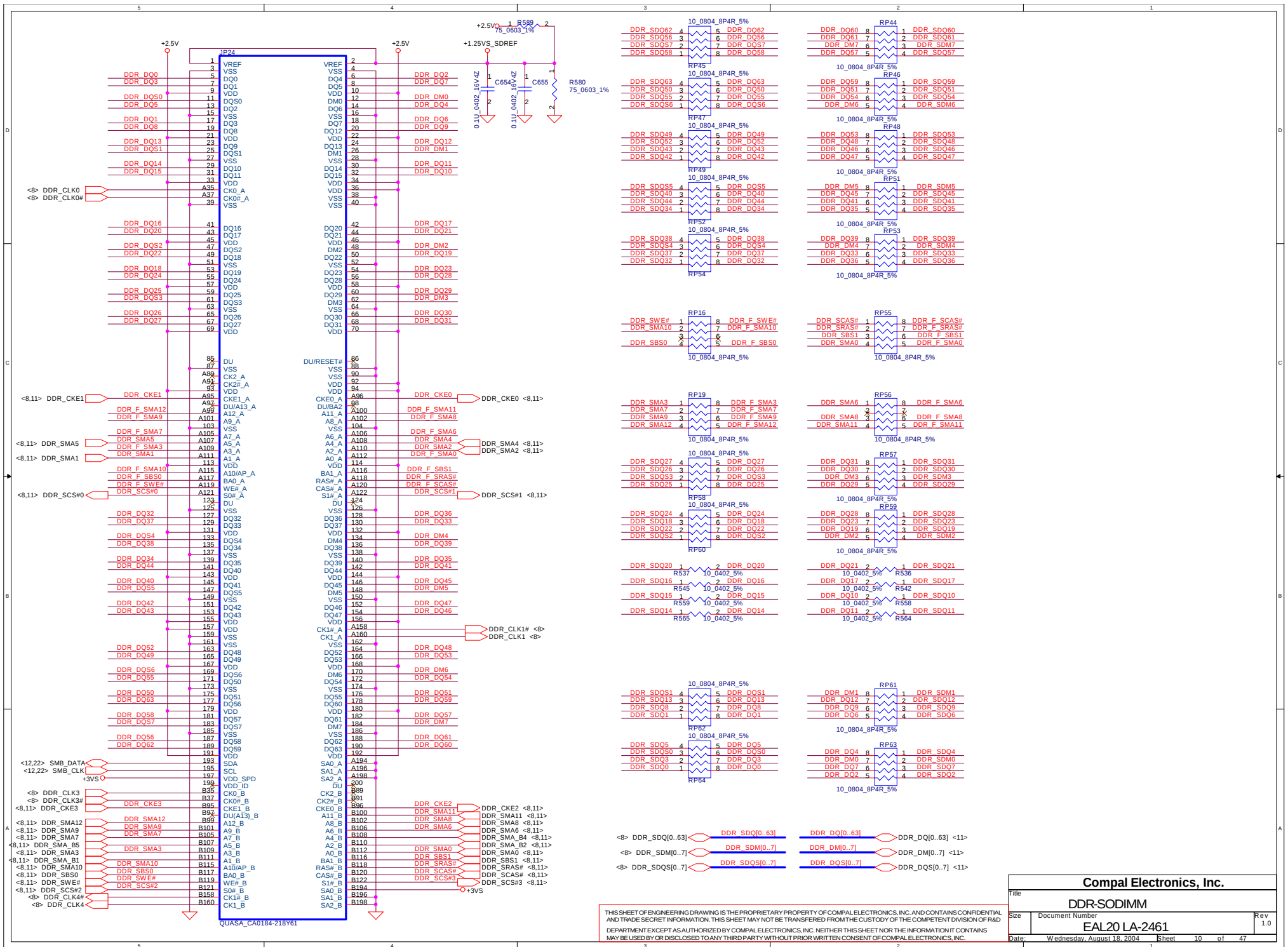
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INTEL CPU BANIAS (2 of 2)

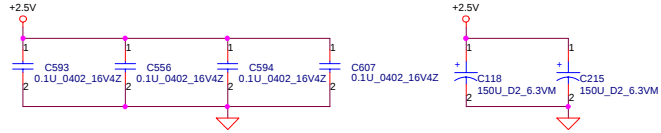
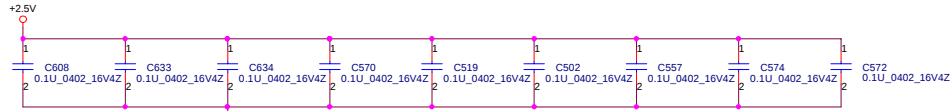
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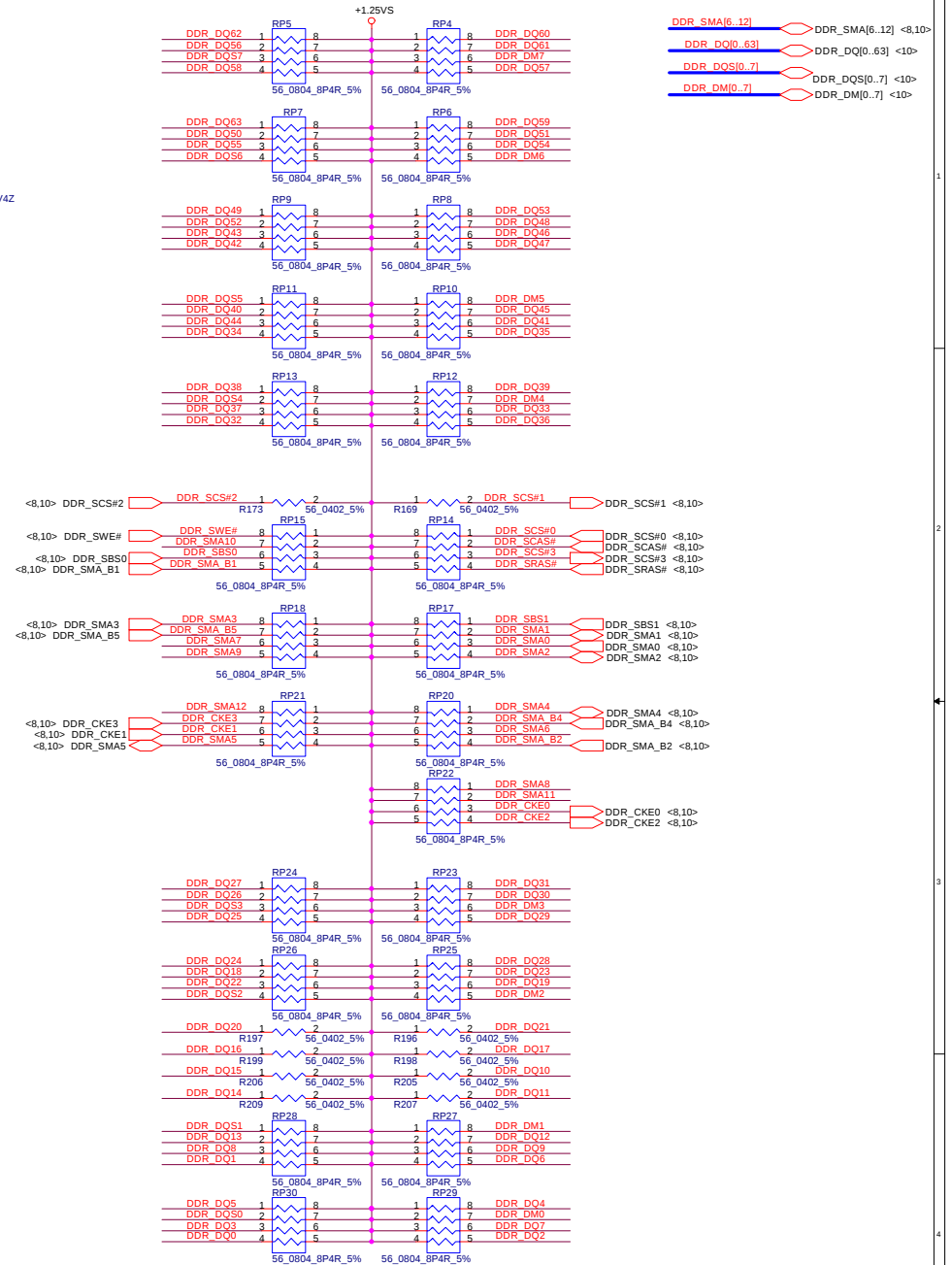
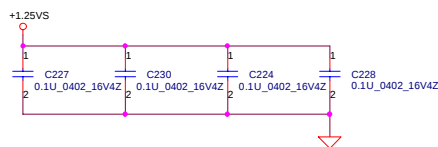
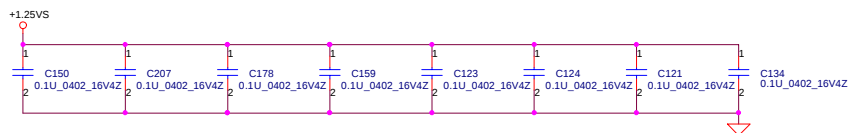
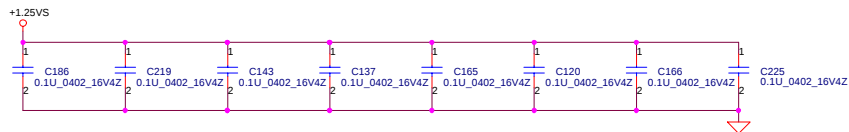
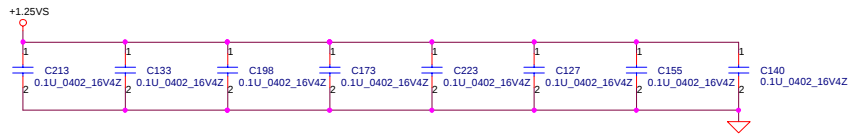
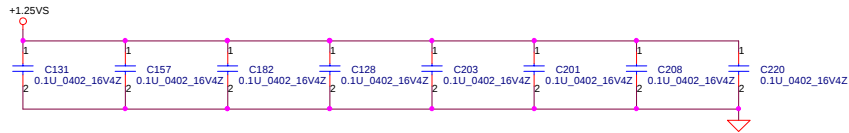
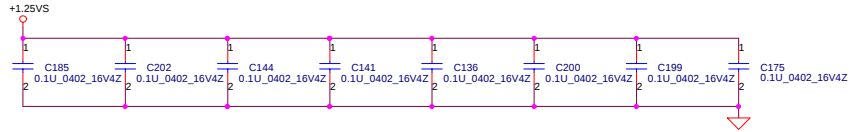




Layout note:
Distribute as close as possible to DDR-SODIMM.



Layout note:
Place one cap close to every 2 pull up resistors termination to +1.25V



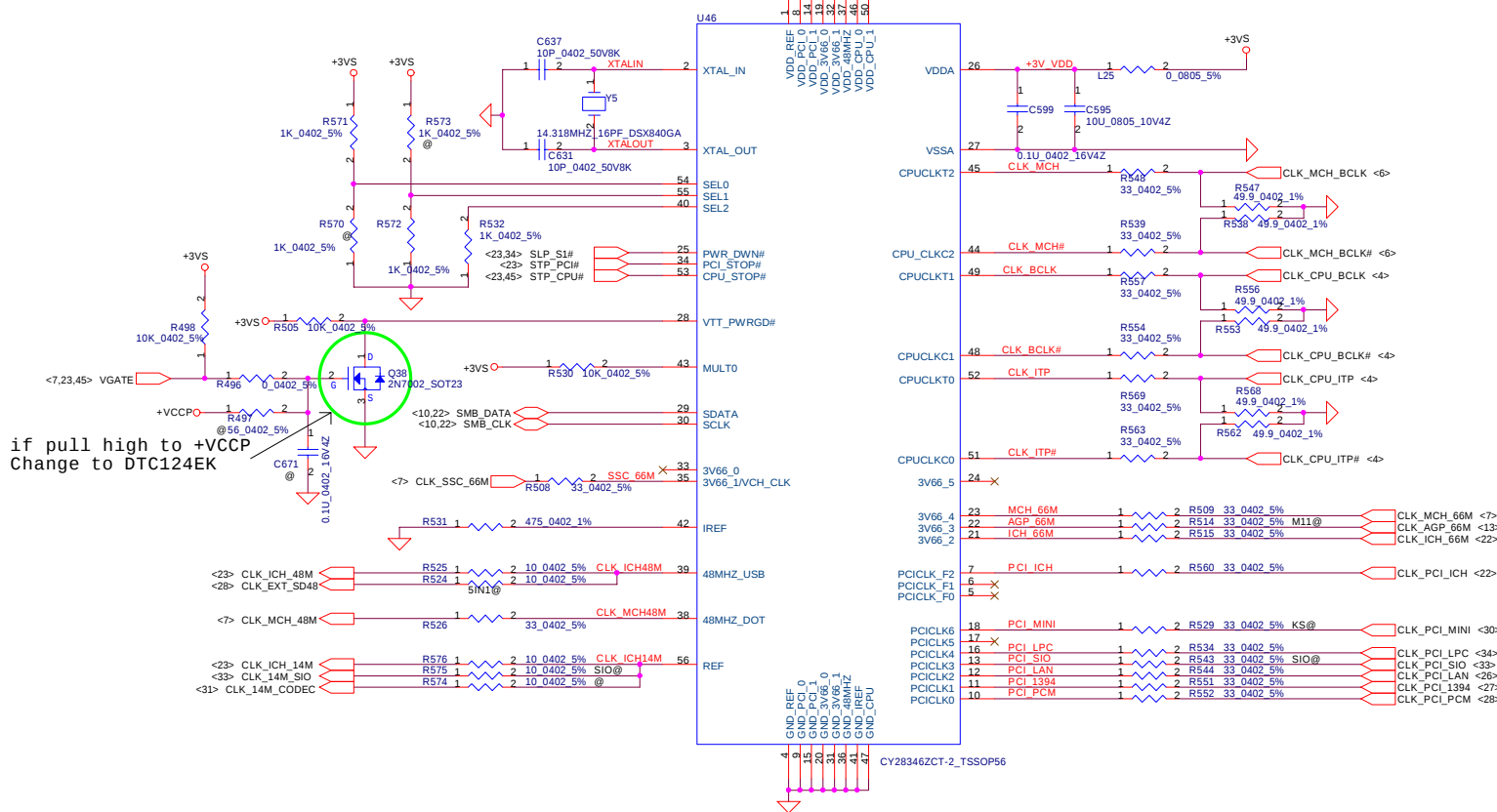
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Title			
DDR SODIMM Decoupling			
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Clock Generator

SEL2	SEL1	SEL0	CPUCLK[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00 *
0	1	0	200.00	200.00
0	1	1	133.33	133.33

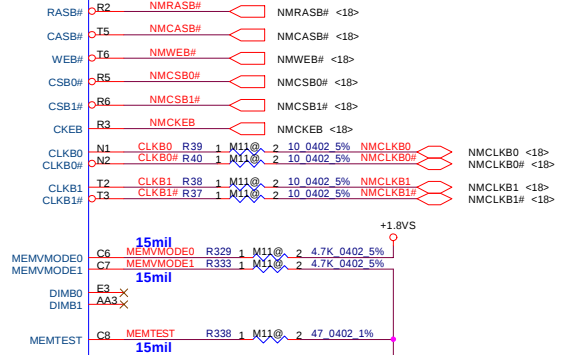
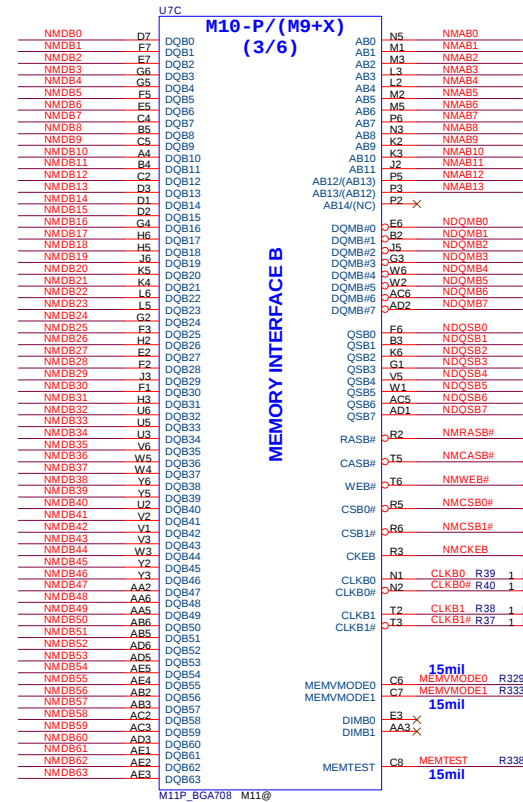
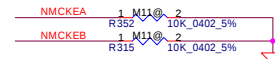
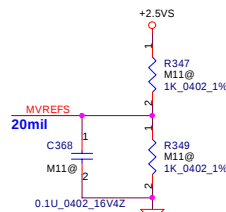
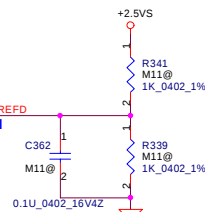
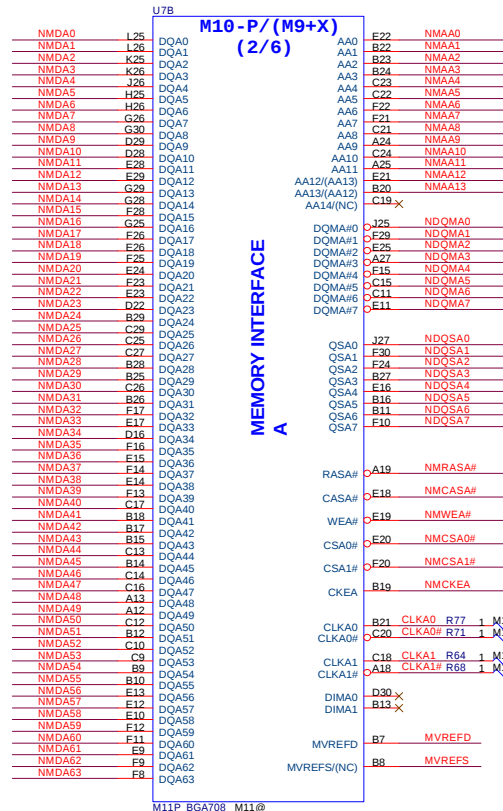


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Clock Generator			
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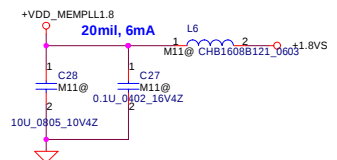
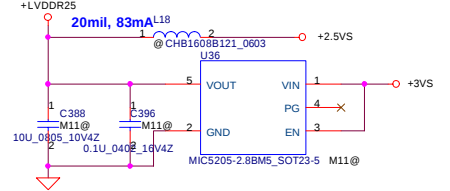
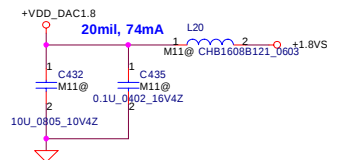
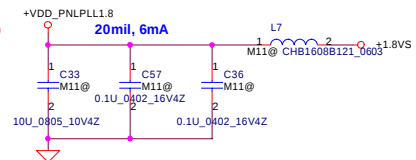
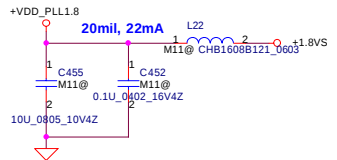
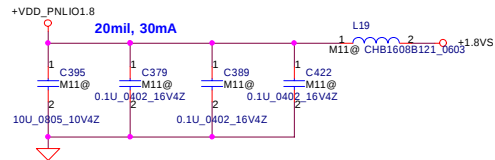
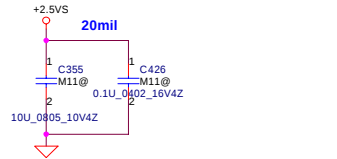
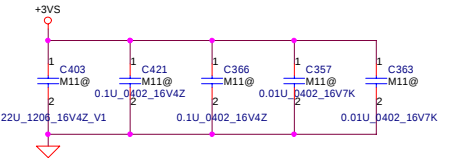
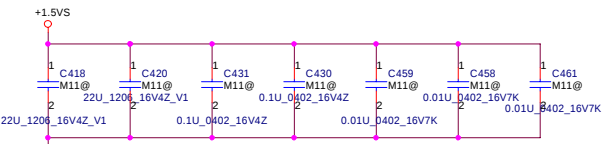
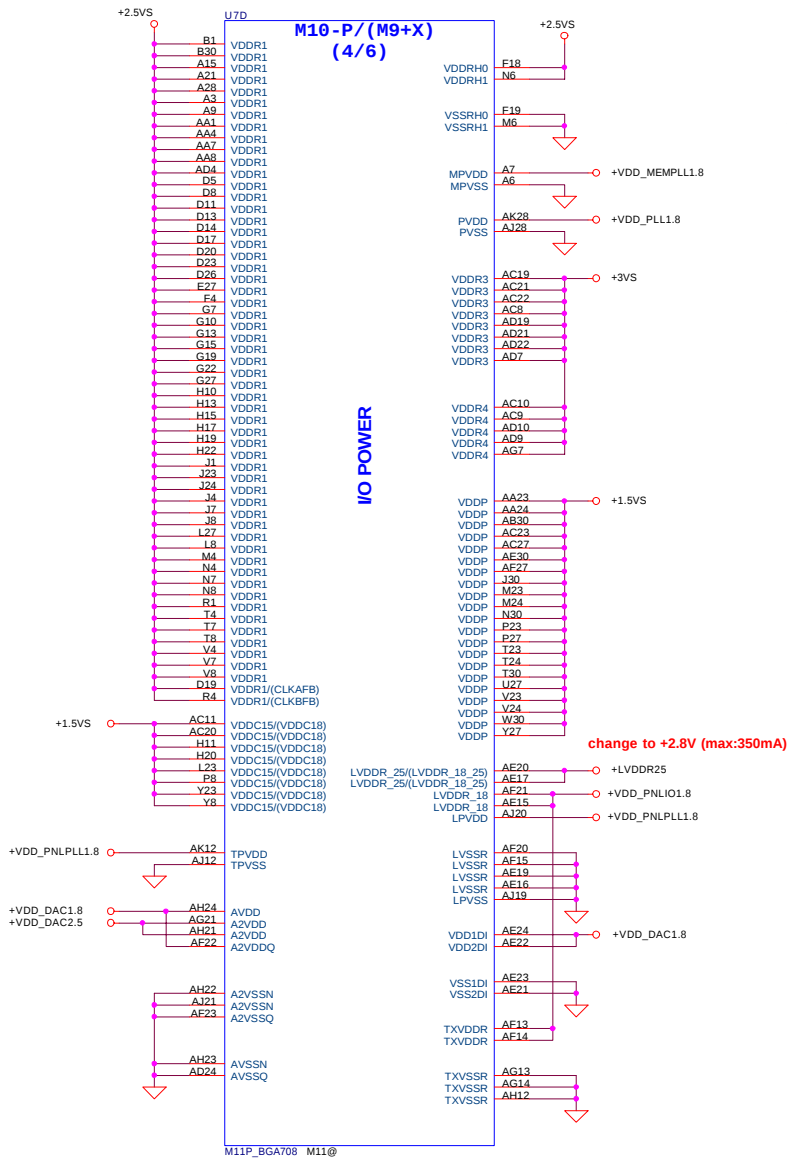
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<17> NMAA[0..13]  NMAA[0..13]
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<17> NDQSA[0..7]  NDQSA[0..7]

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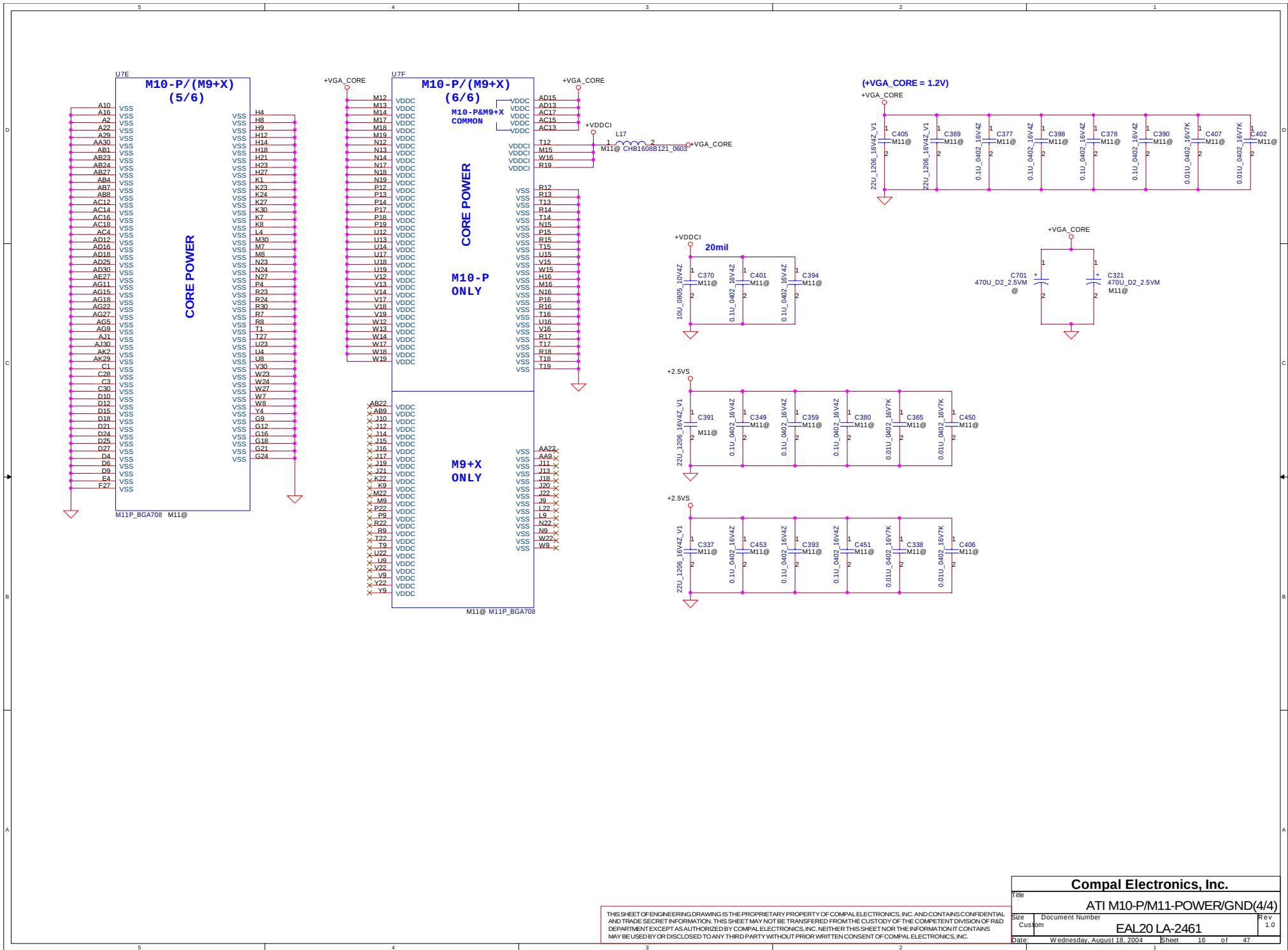
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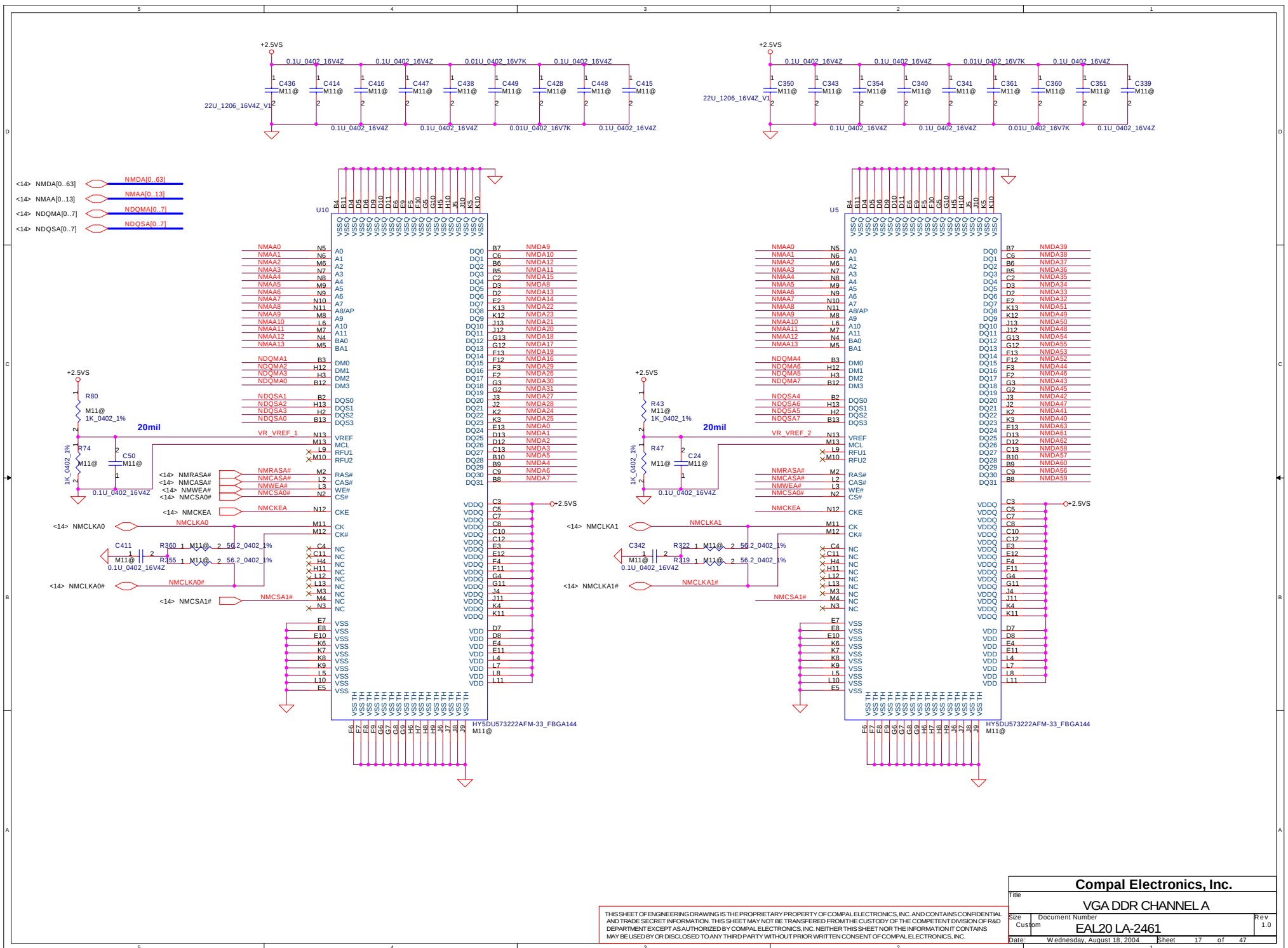
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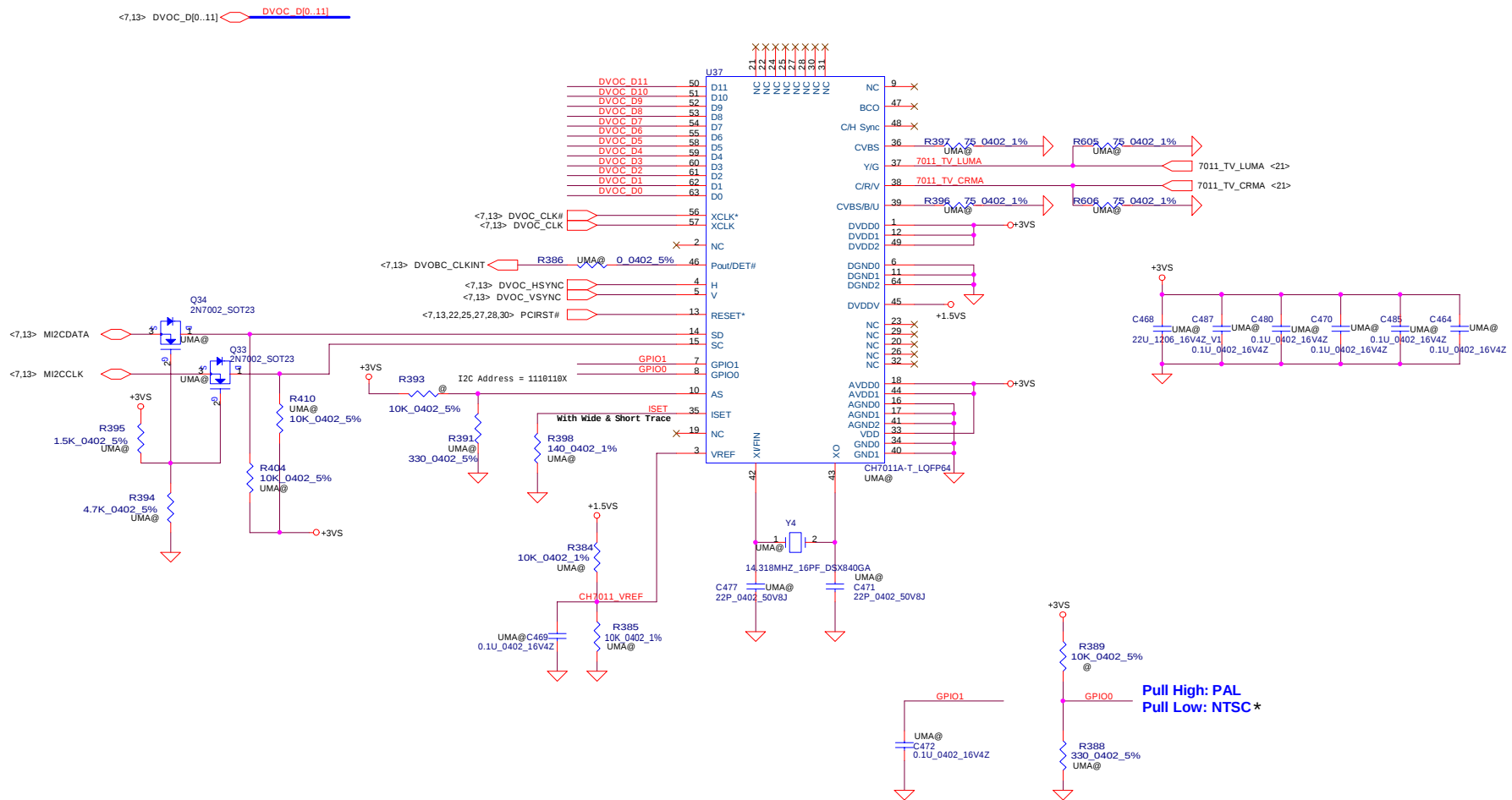
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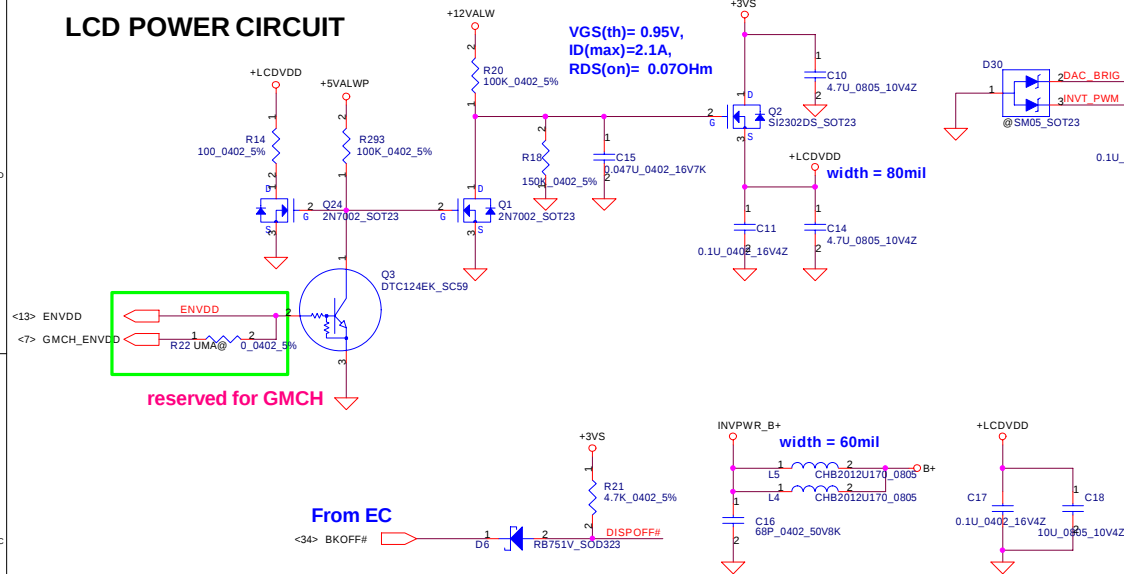
TV Encoder

remove this page when use M11P



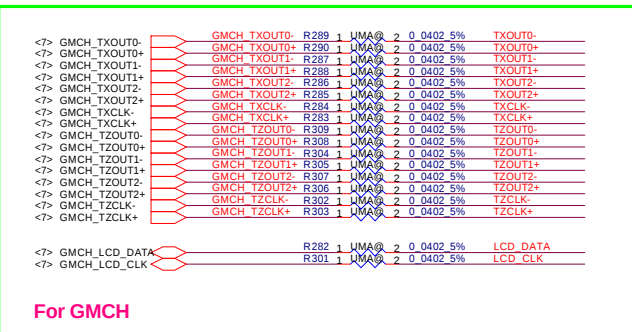
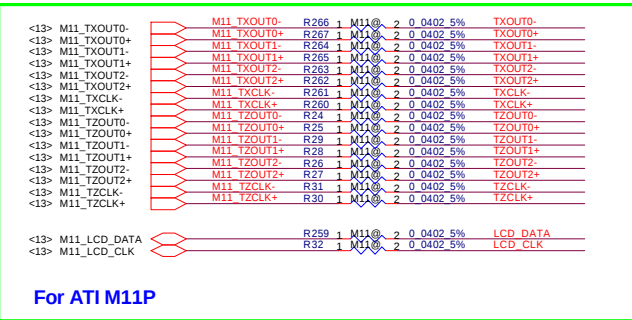
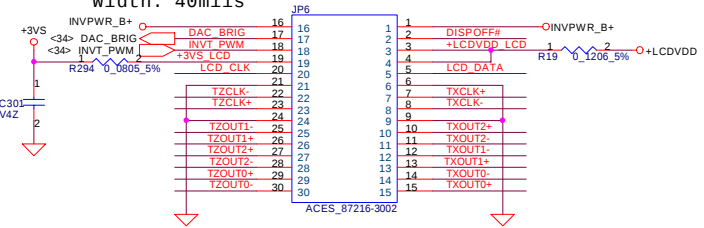
Pull High: PAL
Pull Low: NTSC*

LCD POWER CIRCUIT

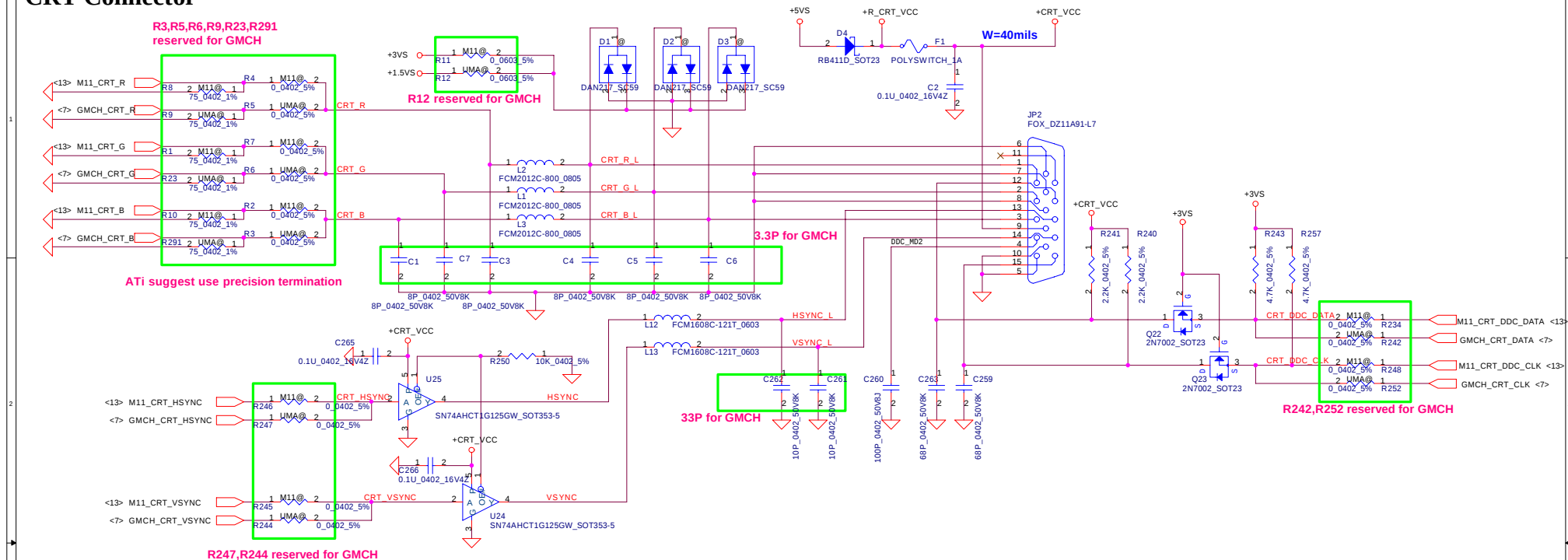


LCD CONN.

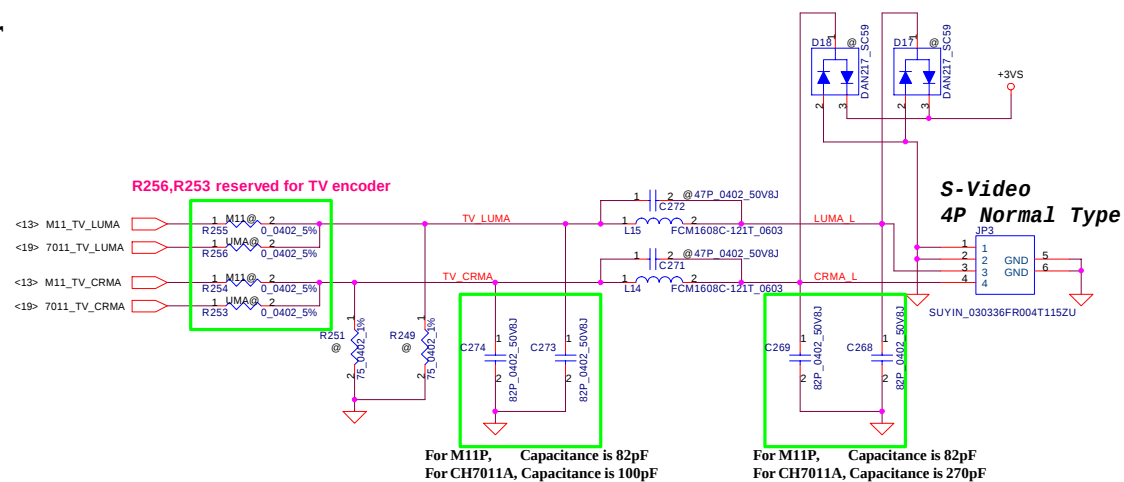
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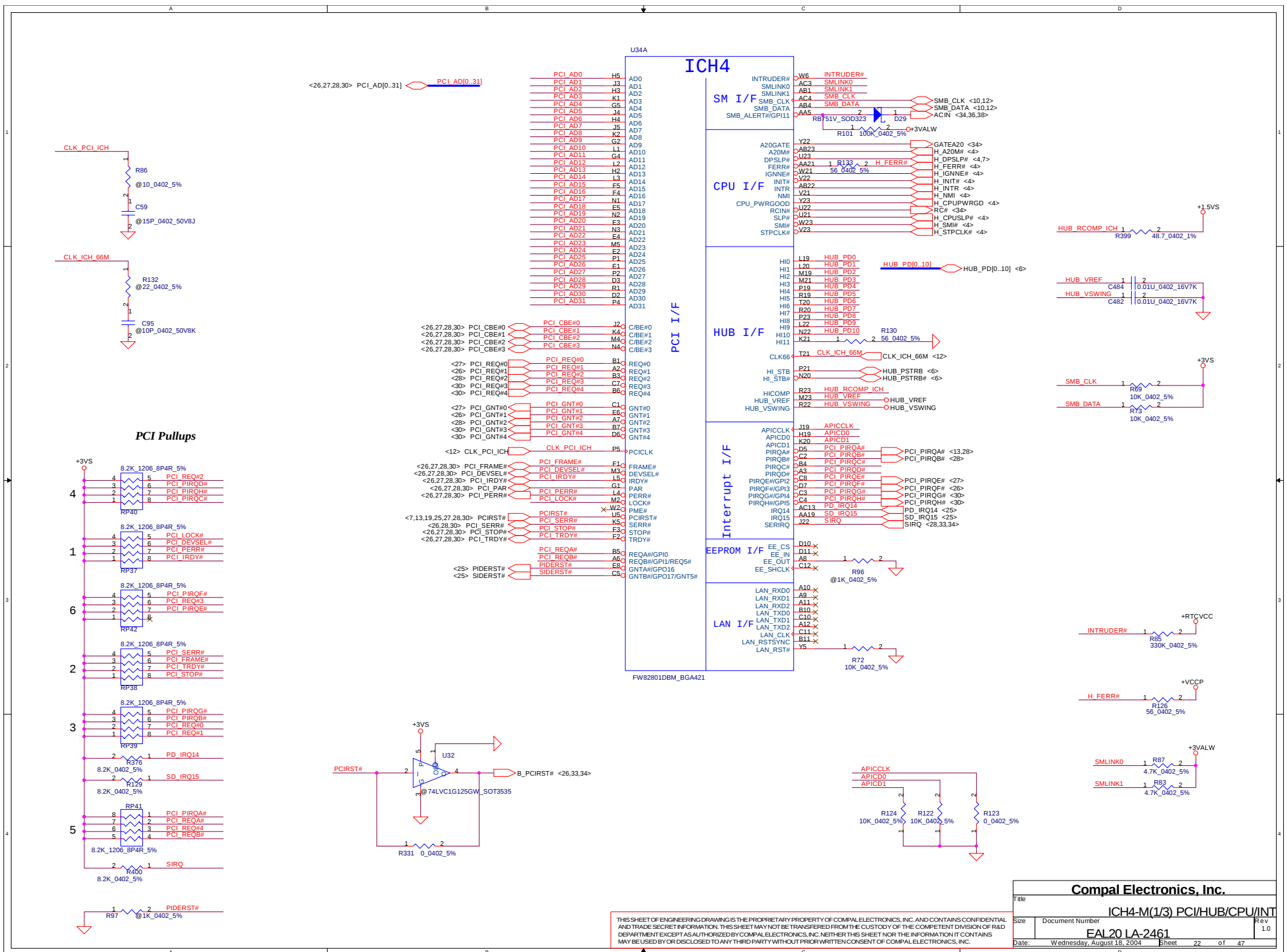


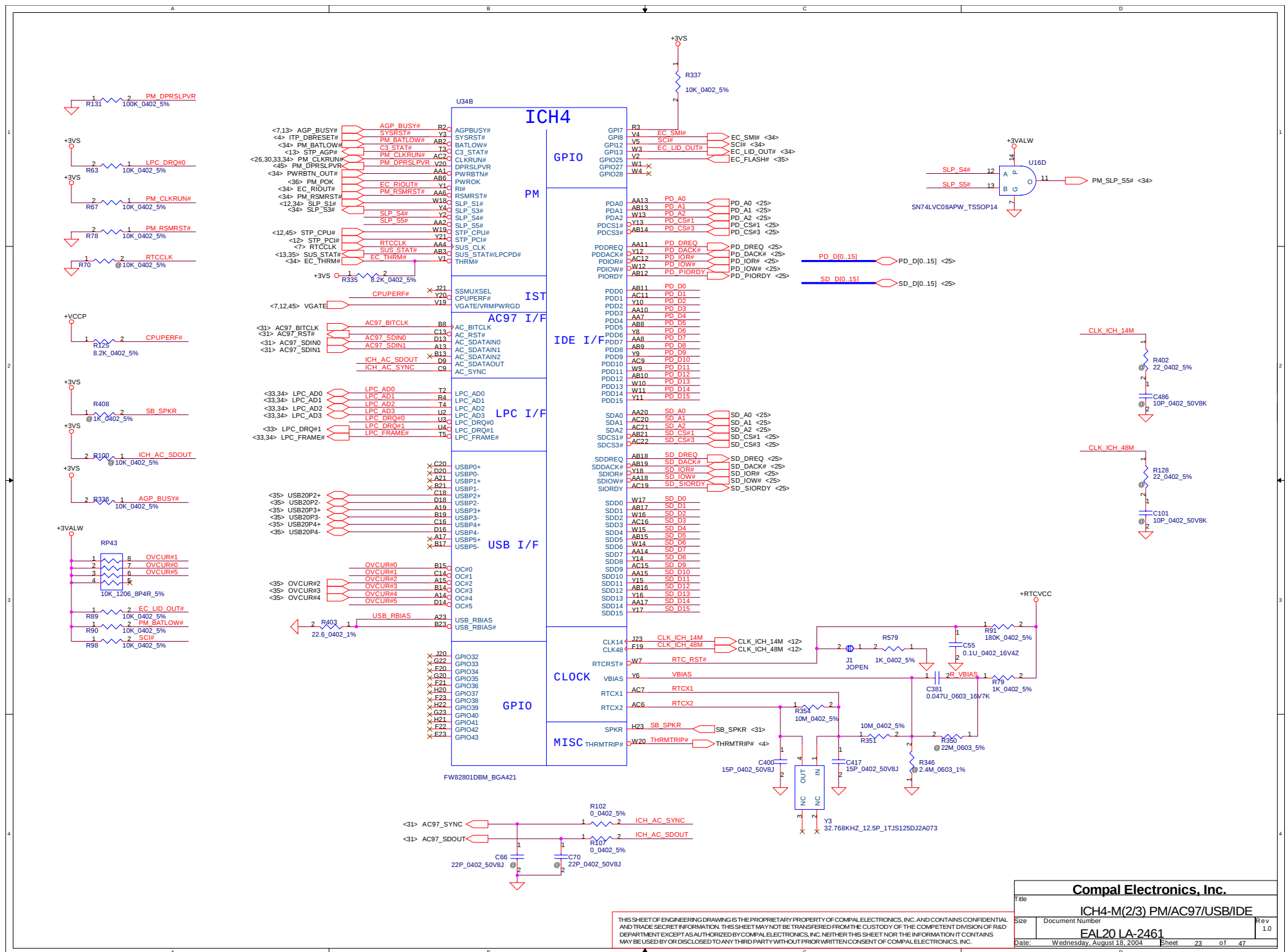
CRT Connector



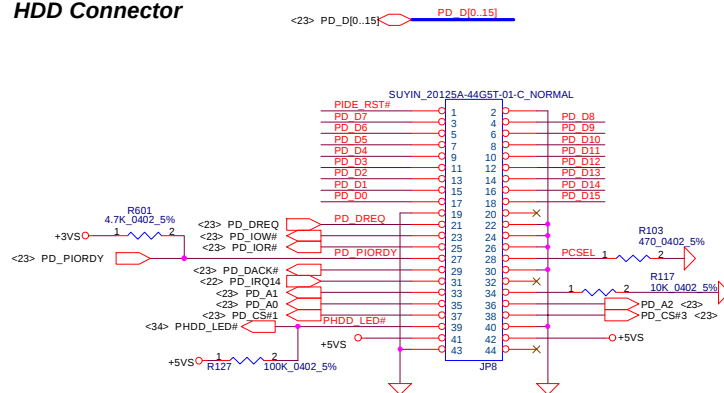
TV-Out Connector



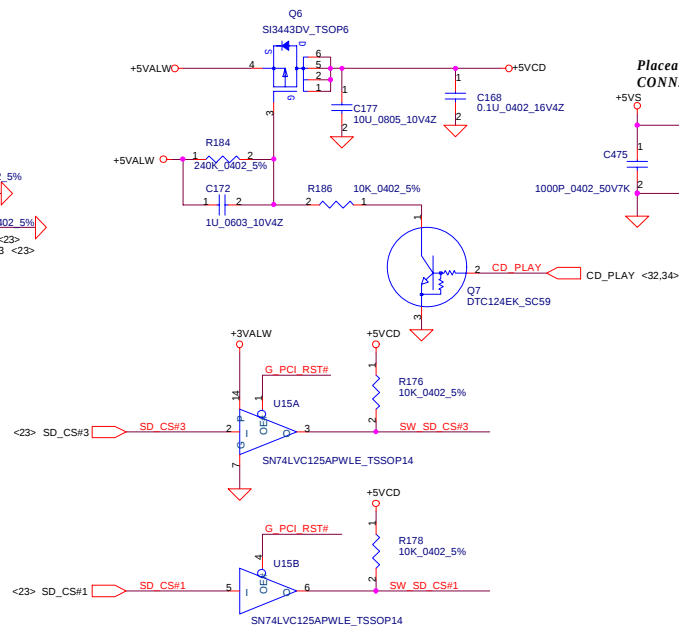




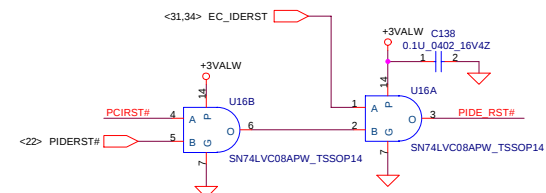
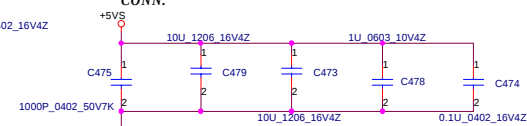
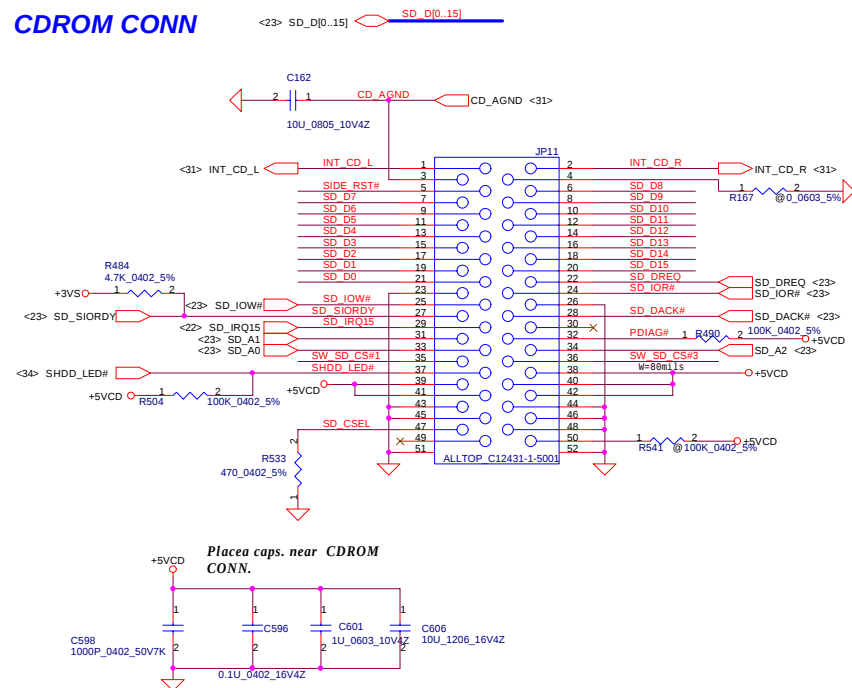
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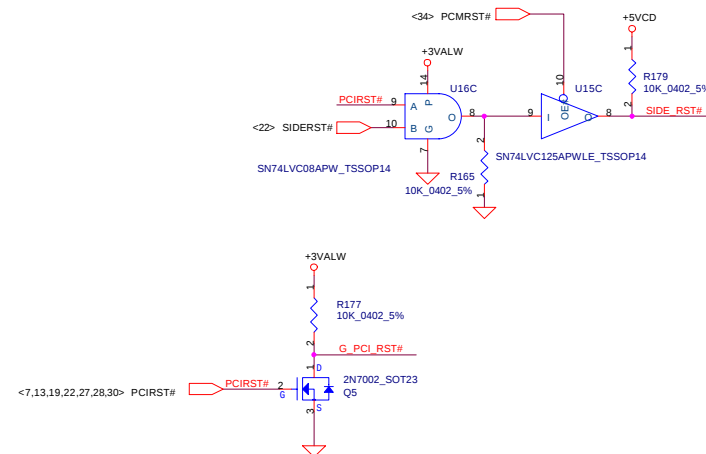
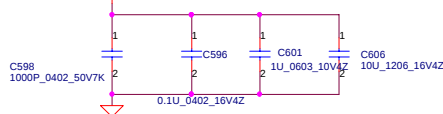
This is reverse type conn, PIDE_RST# connect to pin44.
After connector library ready,
correct connection is PIDE_RST# connect to pin1!

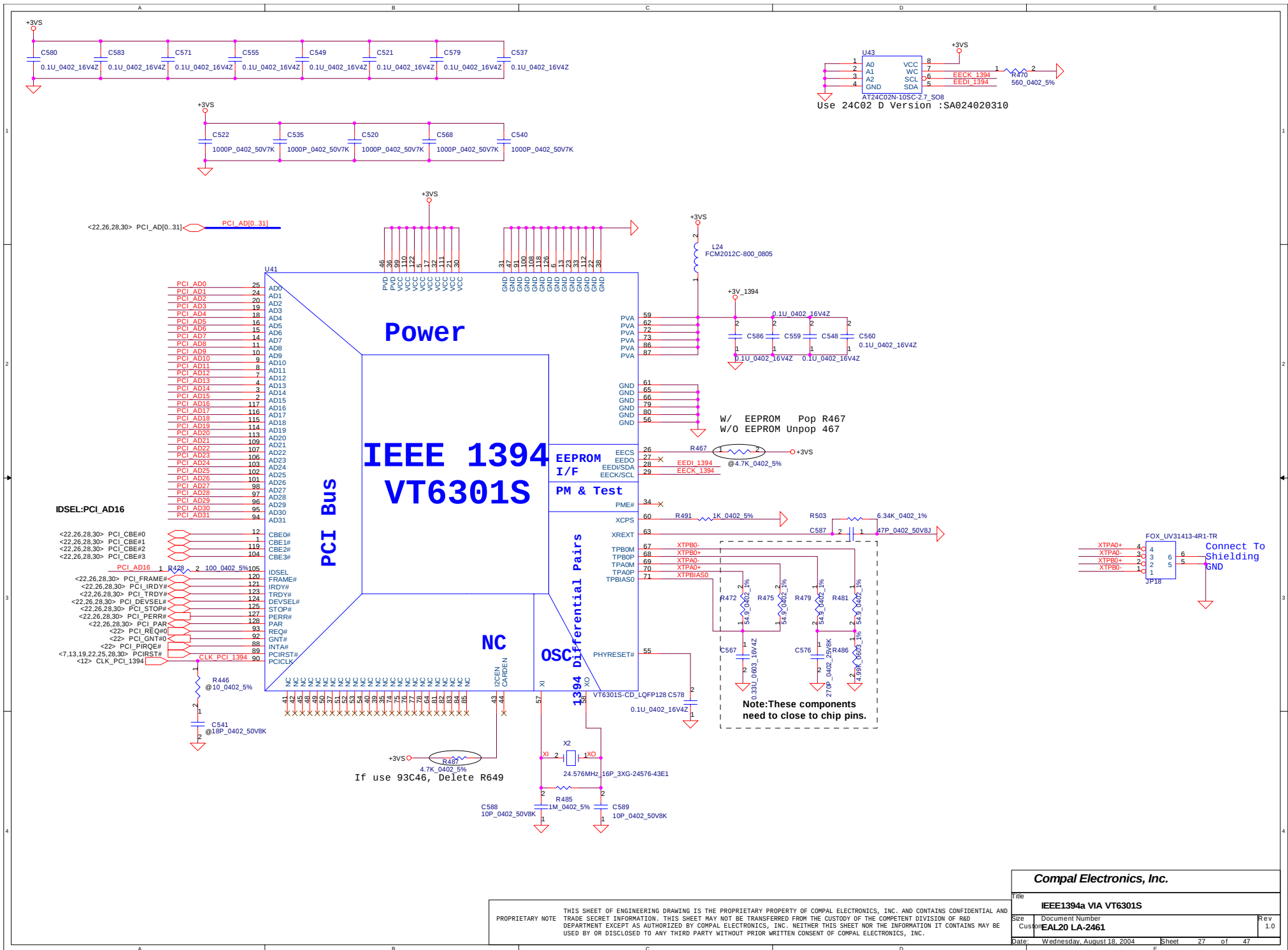


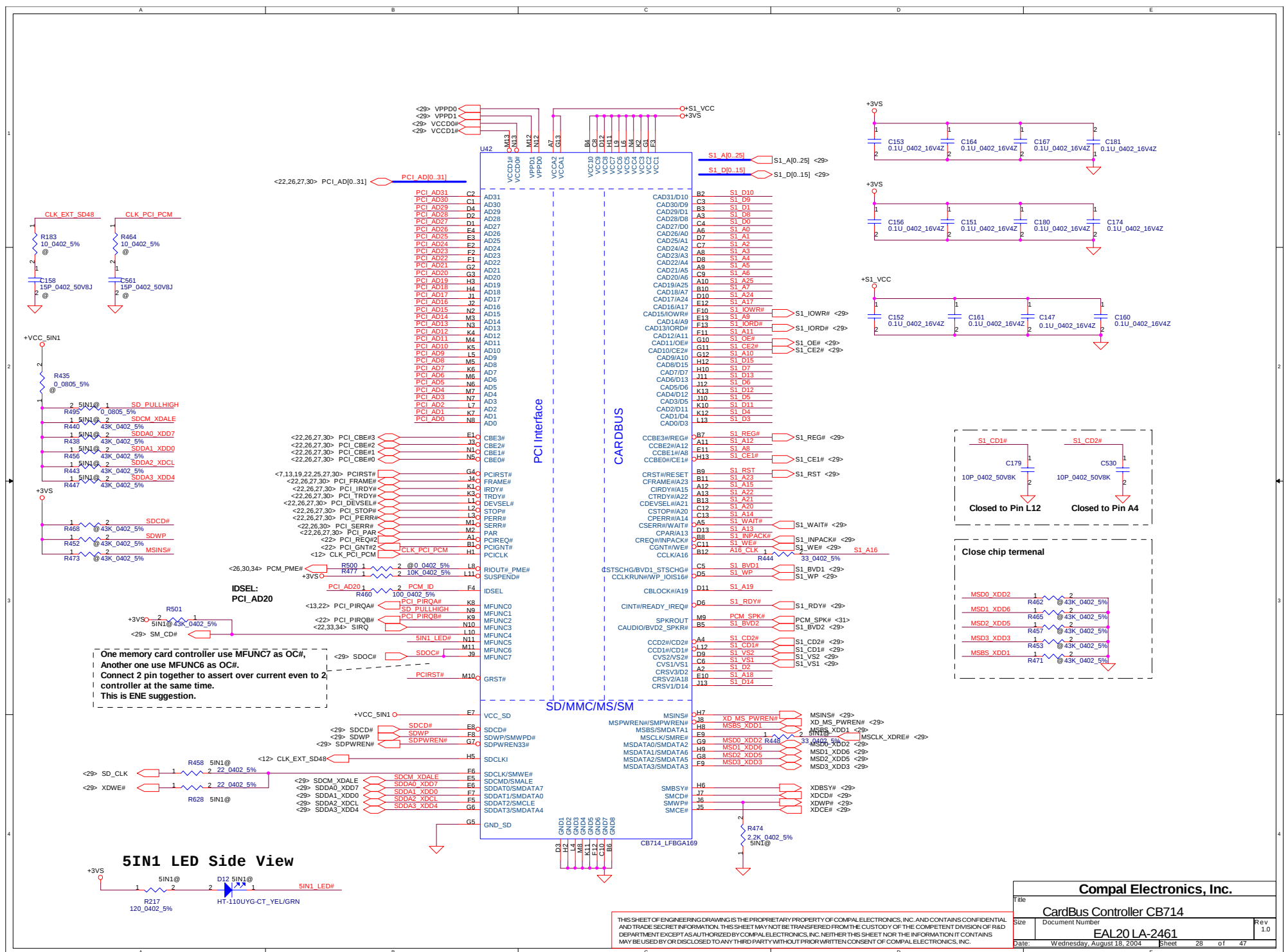
Placea caps. near HDD
CONN.

**CDROM CONN**

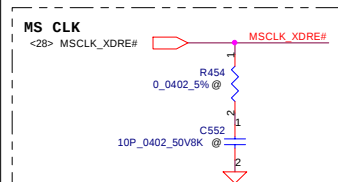
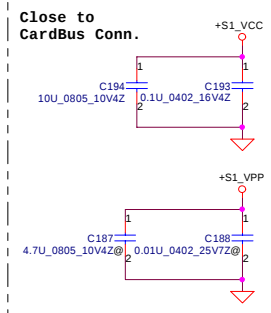
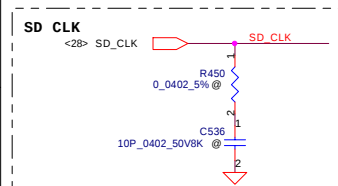
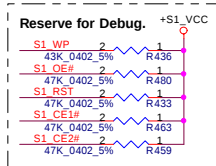
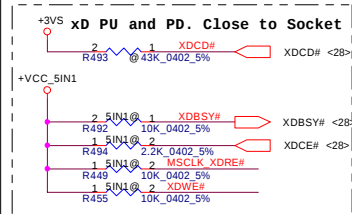
*Place caps. near CDROM
CONN.*







The schematic diagram illustrates the power supply connections for the CP2211D3-SSOP16 chip (U18). The chip has pins for VCC (13, 12, 11), VPP (10), and GND (7, 16). Power supply rails are shown: +5V (pins 5, 6), +3V (pins 3, 4), and +1V (pin 10). Decoupling capacitors C217, C222, C216, and C221 are connected to the +5V, +3V, and +1V rails. A 10K_0402_5% resistor R195 is connected between pins 1 and 2. The chip is connected to a CP2211D3-SSOP16 component.



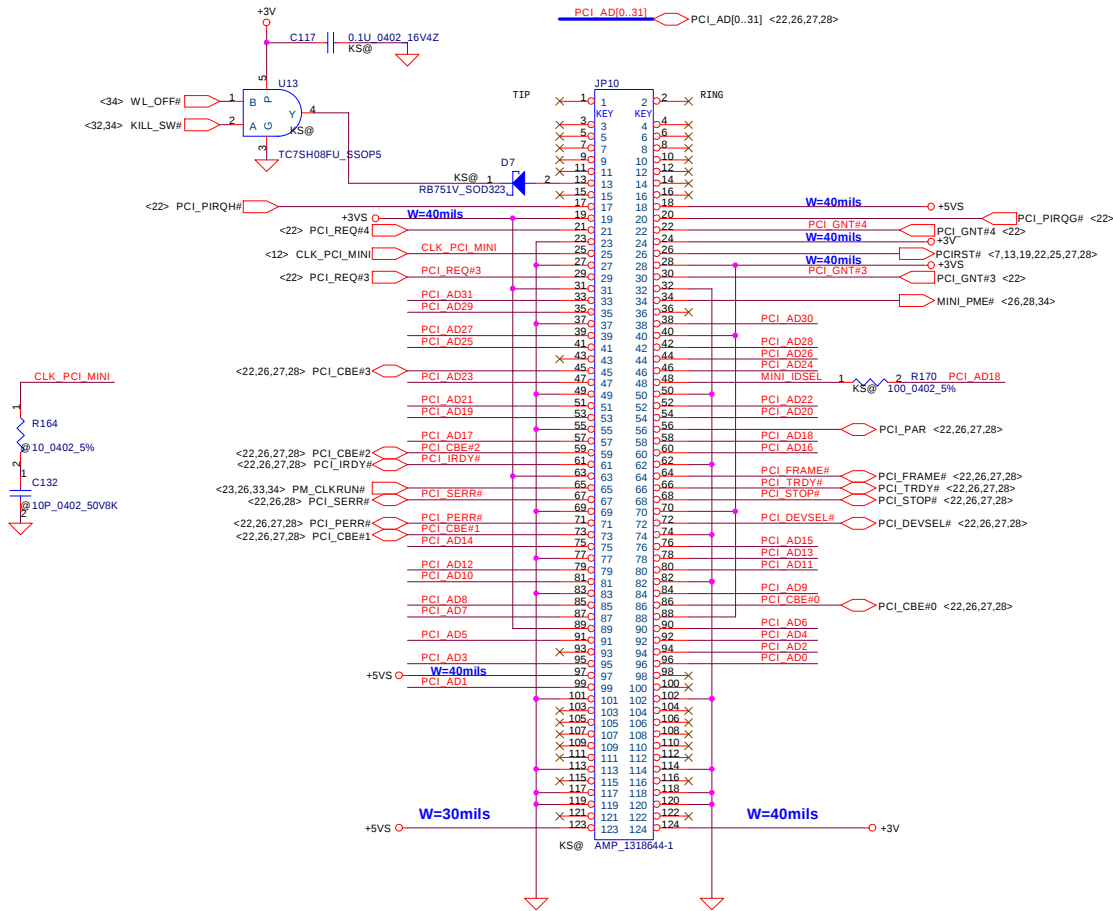
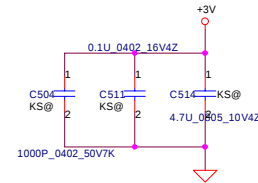
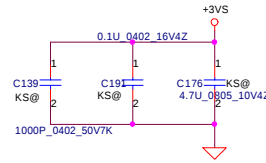
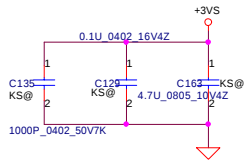
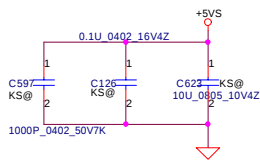
Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
S1_D3	2	GN	2	CD14 / CDD1#	36	S1_CD1#	36
S1_D4	3	D3 / CAD0	3	D11 / CAD3	37	S1_D11	37
S1_D5	4	D4 / CAD1	4	D12 / CAD4	38	S1_D12	38
S1_D6	5	D5 / CAD2	5	D13 / CAD5	39	S1_D13	39
S1_D7	6	D6 / CAD5	6	D14 / RFU	40	S1_D14	40
S1_CE1#	7	D7 / CAD7	7	D15 / CAD8	41	S1_D15	41
S1_A10	8	CE1# / CBCE0#	8	CE2# / CAD10	42	S1_CE2#	42
S1_OE#	9	A10 / CAD9	9	VS1# / CVS1	43	S1_VS1	43
S1_A9	10	OE# / CAD11	10	IORD# / CAD13	44	S1_IORD#	44
S1_A8	11	A11 / CAD12	11	IOWR# / CAD15	45	S1_IOWR#	45
S1_A13	12	A9 / CAD14	12	A17 / CAD16	46	S1_A17	46
S1_A14	13	A8 / CCBAR1	13	A18 / RFU	47	S1_A18	47
S1_A14	14	A13 / CPAR	14	A19 / CBLOCK#	48	S1_A19	48
S1_WE#	15	WE# / CGNT#	15	A20 / CSTOP#	49	S1_A20	49
S1_RDY#	16	A14 / CPER#	16	A21 / CDEVEL#	51	S1_A21	51
S1_VCCO	17	IREQ# / CINT#	17	VCC	52	S1_VCC	52
S1_VPP0	18	VCC	18	VPP2	53	S1_VPP	53
S1_A16	19	A16 / CLK	19	A22 / CTRDY#	54	S1_A22	54
S1_A15	20	A15 / CIRDY#	20	A23 / CFRAME#	55	S1_A23	55
S1_A12	21	A12 / CBCE2#	21	A24 / CAD17	56	S1_A24	56
S1_A7	22	A7 / CPER#	22	A25 / CAD19	57	S1_A25	57
S1_A6	23	A6 / CAD20	23	VS2# / CVS2	58	S1_VS2	58
S1_A5	24	A5 / CAD21	24	RESET / CRS7#	59	S1_RST	59
S1_A4	25	A4 / CAD22	25	WAIT# / CSERR#	60	S1_WAIT#	60
S1_A3	26	A3 / CAD23	26	INPACK# / CREQ#	61	S1_INPACK#	61
S1_A2	27	A2 / CAD24	27	REG# / CBCE3#	62	S1_REG#	62
S1_A1	28	A1 / CAD25	28	SPKR# / CAUDIO	63	S1_BVD2	63
S1_A0	29	A0 / CAD26	29	STSCHG# / CTSCHG	64	S1_D8	64
S1_D0	30	D0 / CAD27	30	D8 / CAD28	65	S1_D9	65
S1_D1	31	D1 / CAD28	31	D9 / CAD30	66	S1_D10	66
S1_D2	32	D2 / RFU	32	D10 / CAD31	67	S1_D11	67
S1_WP	33	IOIS16# / CLCKRUN#	33	CD2# / CCD2#	68	S1_CD2#	68
S1_WP	34	GND	34	GND	69	S1_CD2#	69
S1_A[0..25]	69	GND	69	GND	70	S1_CD2#	70
S1_D[0..15]	71	GND	71	GND	72	S1_CD2#	72
S1_A[0..25]	73	GND	73	GND	74	S1_CD2#	74
S1_D[0..15]	75	GND	75	GND	76	S1_CD2#	76
S1_A[0..25]	77	GND	77	GND	78	S1_CD2#	78
S1_D[0..15]	79	GND	79	GND	80	S1_CD2#	80
S1_A[0..25]	81	GND	81	GND	82	S1_CD2#	82
S1_D[0..15]	83	GND	83	GND	84	S1_CD2#	84
S1_A[0..25]	85	GND	85	GND	86	S1_CD2#	86
S1_D[0..15]	87	GND	87	GND	88	S1_CD2#	88

Figure 1-10: Pin Connections for 5IN1@

Pin connections for 5IN1@:

- SDA1_XDD0, MSB5_XD01, MS00_XD02, MS03_XD03, DDA3_XD04, MS02_XD05, MS01_XD06, DDA0_XD07
- XDWP#, SDWP#, XDWE#, SDCM_XDALE
- SM_CD#, XCBST#, MSCL_XDR#, XDCE#, XDCD#, SDDA2_XDCL
- MSB5_XD01, MS00_XD02, MS03_XD03, MSCL_XDR#, MSINS#, MSB5_XD01, XDCD#, SDDA2_XDCL
- +VCC_5IN1, GND, 5IN1@

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Cardbus Slot & 5in1 Socket			
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AC97 Codec

Use to isolate +5VALW and +AC97_DVDD

Use to isolate +5VALW and +AC97_DVDD

UnPopped: Clock source from X'tal
Popped: Clock source from Clock Gen

Place these components close to Codec

Direct CD CTL

POWER ON PATH

DIRECT PLAY PATH

PATH SEL 1

PATH SEL 2

PATH SEL 3

PATH SEL 4

PATH SEL 5

PATH SEL 6

PATH SEL 7

PATH SEL 8

PATH SEL 9

PATH SEL 10

PATH SEL 11

PATH SEL 12

PATH SEL 13

PATH SEL 14

PATH SEL 15

PATH SEL 16

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PATH

System Sound

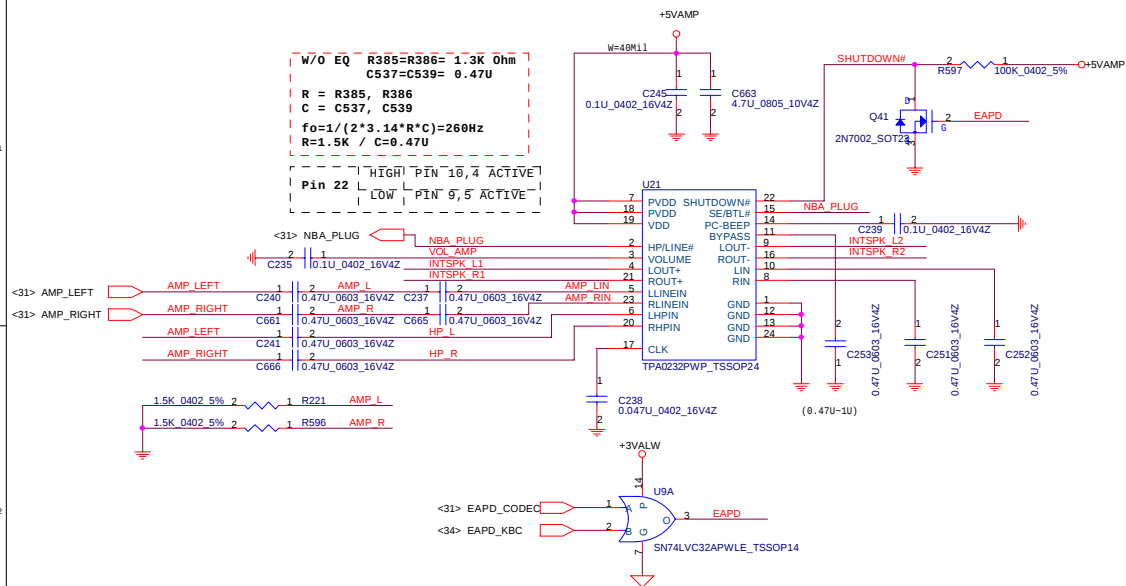
The schematic diagram illustrates the System Sound circuit, featuring three input channels (BEEP#, PCM_SPK#, SB_SPKR#) and a common output path. The circuit is powered by +3V and +3VALW supplies, with various capacitors (C206, C209, C211, C212) and resistors (R200, R202) for timing and signal conditioning. The output is connected to a 1U_0402_6.3V4Z capacitor (C647) and a 10K resistor (R591).

Components and Connections:

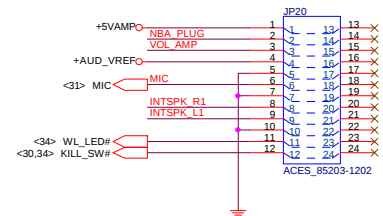
- Inputs:** BEEP#, PCM_SPK#, SB_SPKR#.
- Op-Amps:** U15D (SN74LVC125APWLE_TSSOP14), U17A (SN74LVC14APWLE_TSSOP14), U17B (SN74LVC14APWLE_TSSOP14).
- Resistors:** R189 (100K_0402_5%), R193 (100K_0402_5%), R200 (560_0402_5%), R201 (560_0402_5%), R202 (560_0402_5%), R203 (10K_0402_5%), R581 (10K_0402_5%), R591 (2.4K_0402_5%).
- Capacitors:** C206 (0.1U_0402_16V4Z), C209 (1U_0402_6.3V4Z), C211 (0.22U_0402_10V4Z), C212 (1U_0402_6.3V4Z), C647 (1U_0402_6.3V4Z), C659 (10U_0805_10V4Z).
- Transistors:** Q42 (2SC2411K_N SC95), D8 (RB751V_SOD323).
- Power Supplies:** +3V, +3VALW, +AVDD_AC97, +3V POWER.

MDC Connector

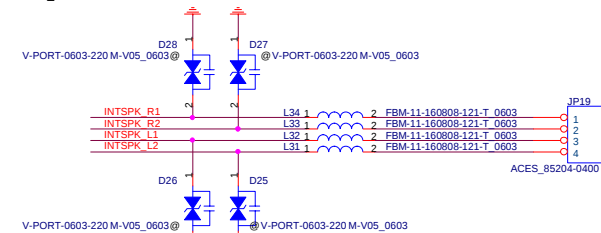
Audio AMP



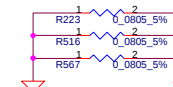
Audio Board Connector



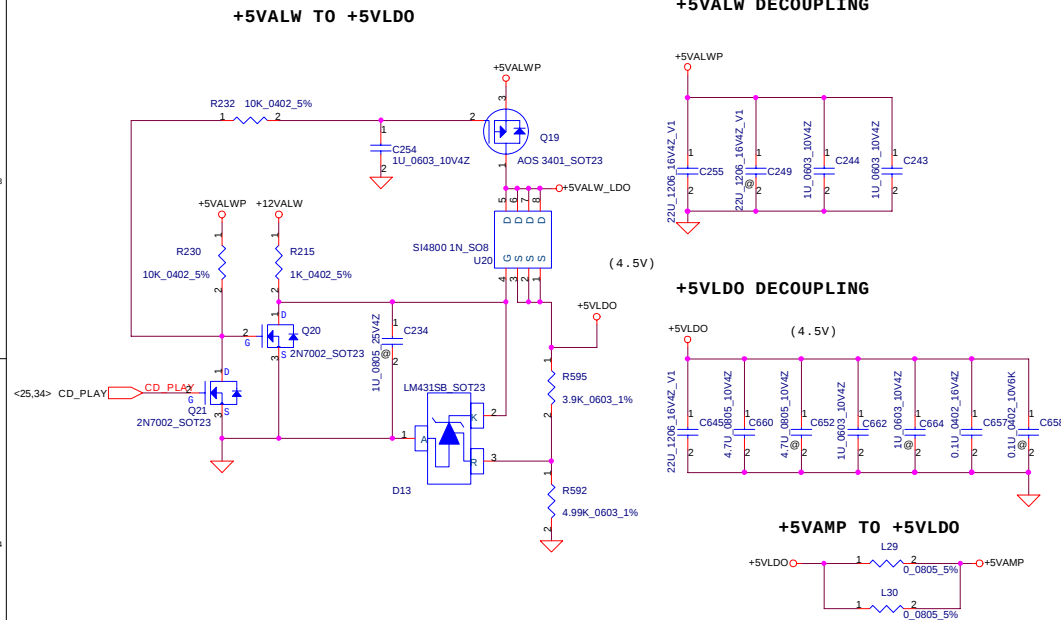
Speaker Connector



Moat Bridge



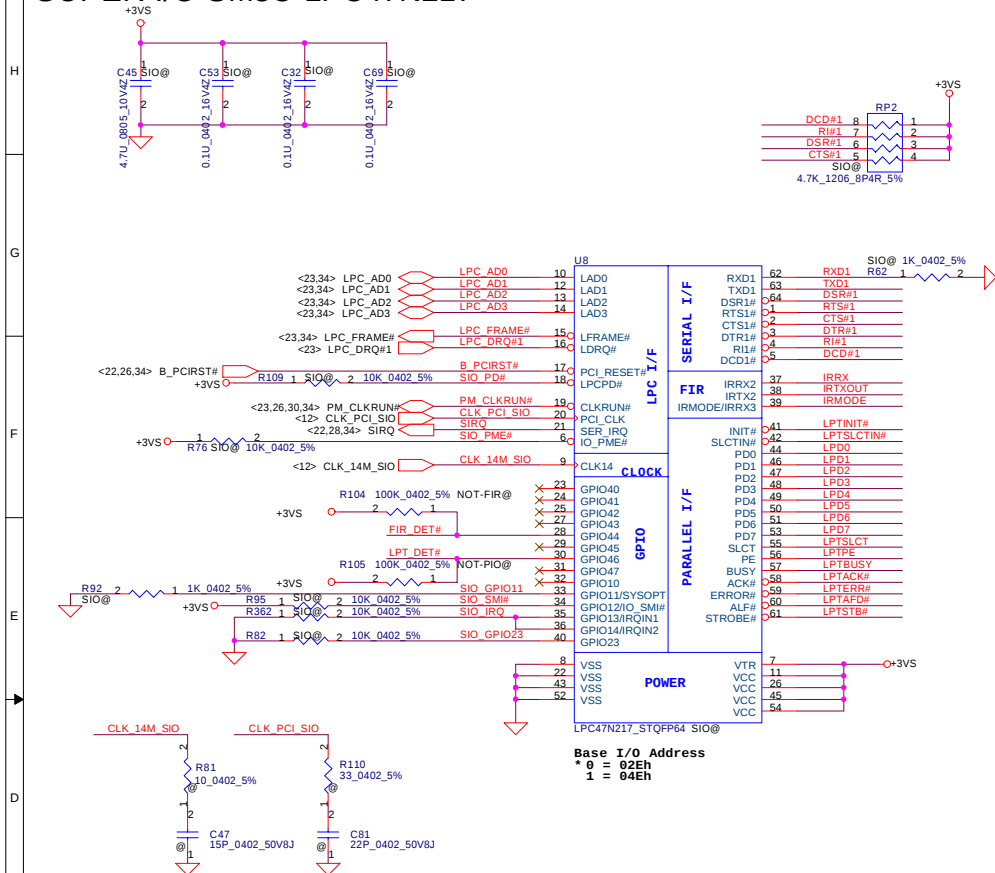
Regulator for AMP



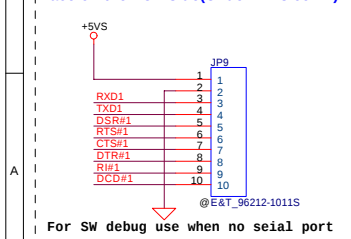
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AMP & Audio Jack			
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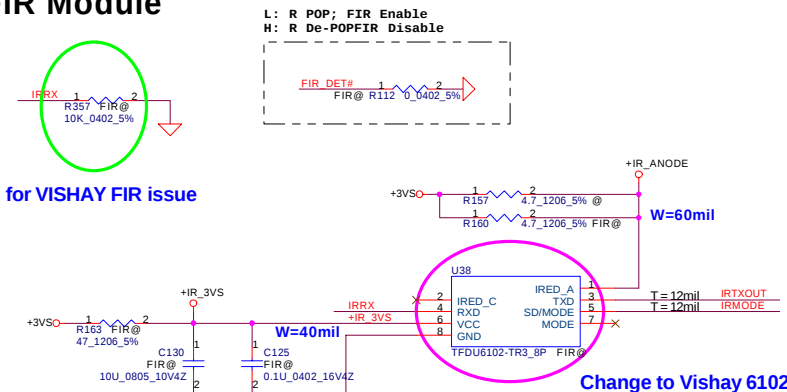
SUPER I/O SMsC LPC47N217



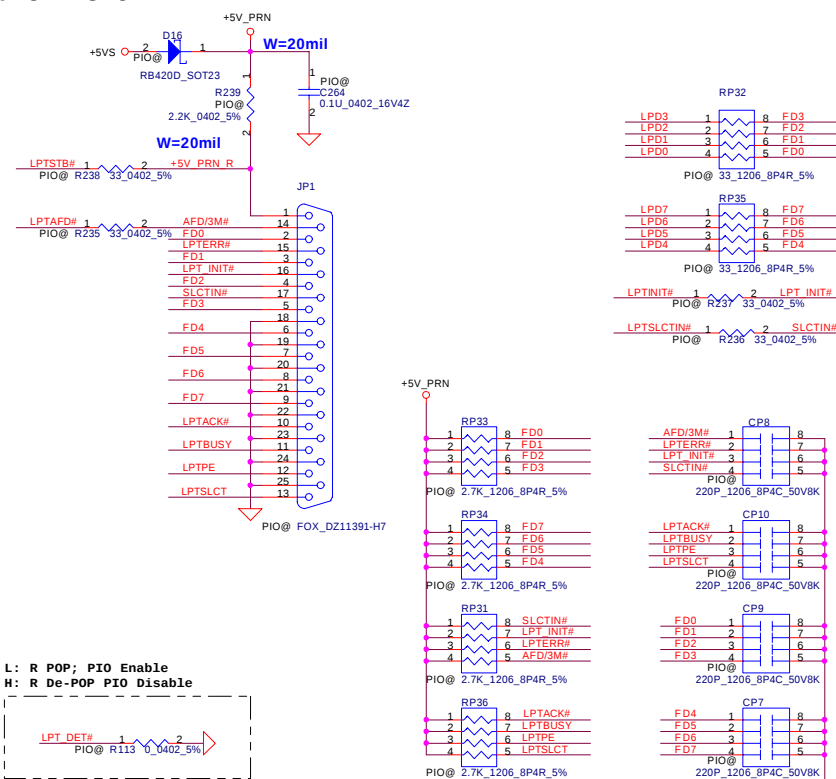
Place on the TOP side(Under MDC conn.)



FIR Module



Parallel Port



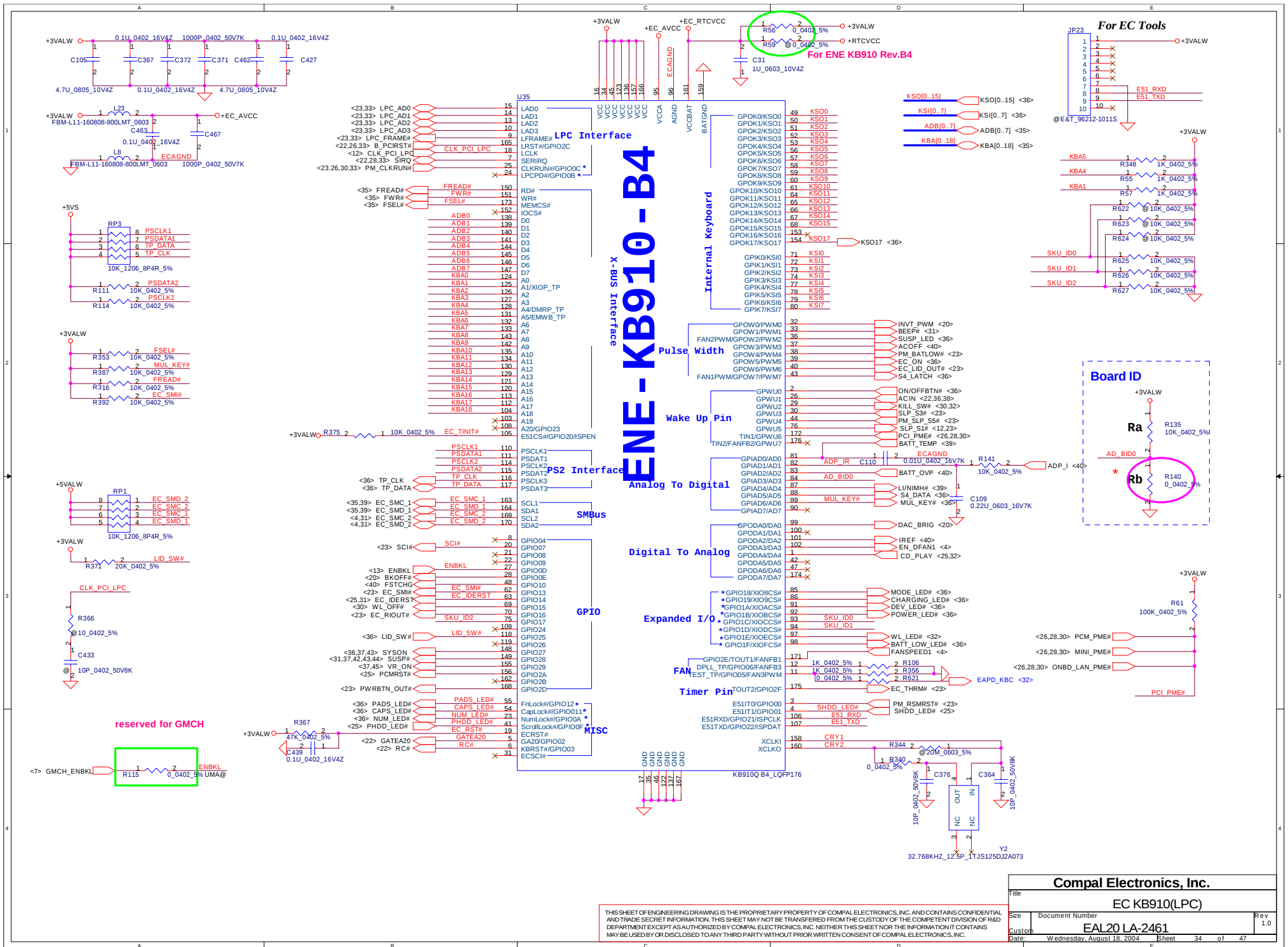
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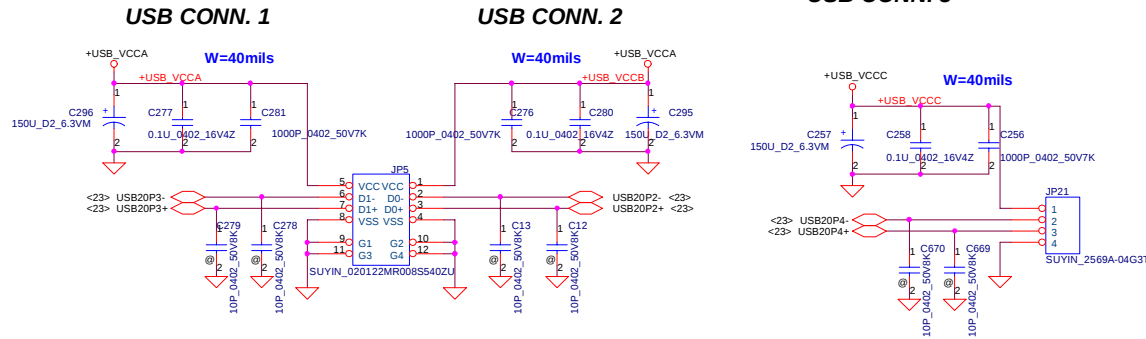
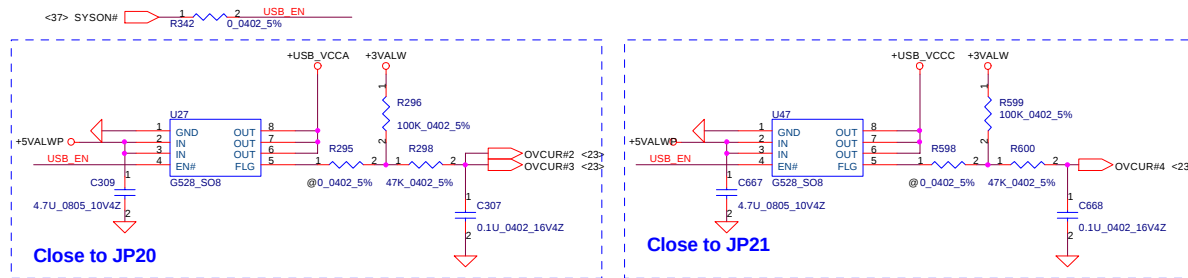
SMsC LAP47N217 SIO,PIO,FIR

EAL20 LA-2461

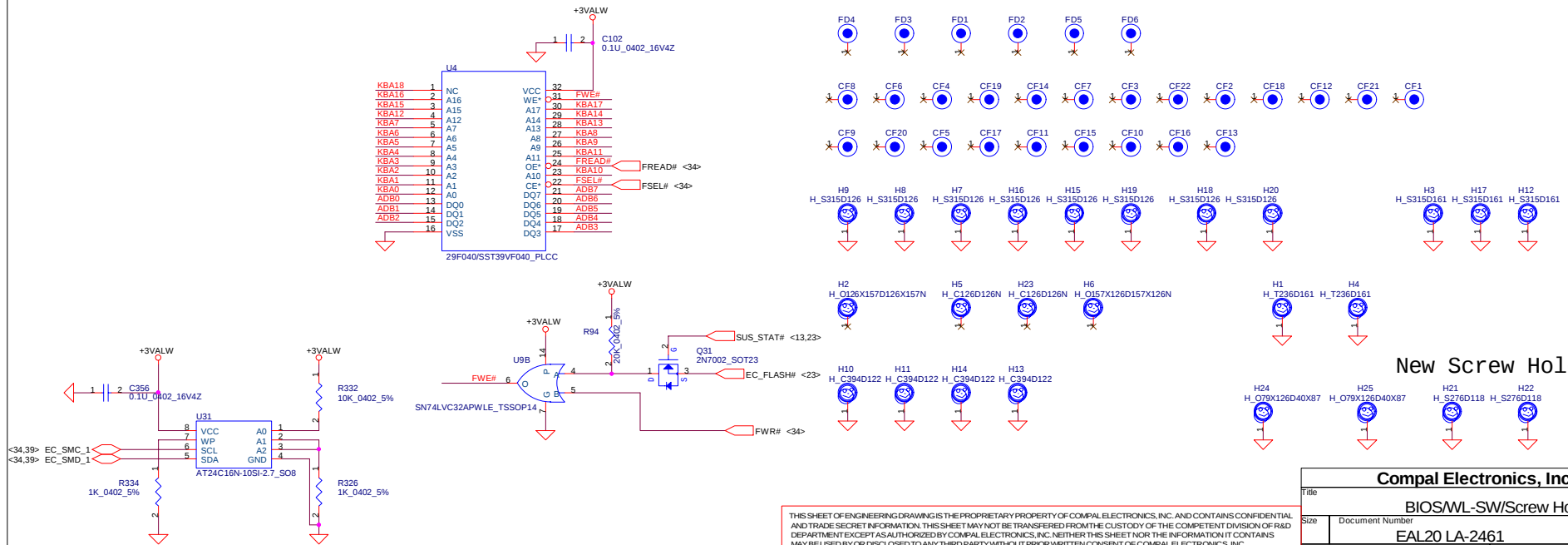
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512kB Flash ROM



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BIOS/ML-SW/Screw Hole/USB

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[illegible]

SW/LED Connector

The diagram illustrates the SW/LED Connector (JP15) and its connections. The connector is a 14-pin header. The connections are as follows:

- Pin 1: PWR_LED# (mode LED) - connected to C613 (0.1U_0402_16V4Z) and a diode.
- Pin 2: PWR_SUSP_LED (device LED) - connected to a diode.
- Pin 3: EC_STOPBTN#
- Pin 4: EC_PLAYBTN#
- Pin 5: EC_FRDBTN#
- Pin 6: EC_REVBTN#
- Pin 7: EC_UTXDKS017
- Pin 8: KSI17 <34>
- Pin 9: KSI0 <34>
- Pin 10: KSI3 <34>
- Pin 11: KSI2 <34>
- Pin 12: KSI17 <34>
- Pin 13: MUL_KEY_ESD#
- Pin 14: ON/OFF

The connector is labeled C613 and 0.1U_0402_16V4Z. The LEDs are labeled MODE_LED# <34> and DEV_LED# <34>. The buttons are labeled EC_STOPBTN#, EC_PLAYBTN#, EC_FRDBTN#, EC_REVBTN#, EC_UTXDKS017, KSI17, KSI0, KSI3, KSI2, and KSI17. The connector is labeled D9 and 3.51_ON#. The connector is labeled DAN2020_SC70. The connector is labeled ACES_85203-1402. The connector is labeled MUL_KEY# <34>.

Touch Pad Connector

ACES_85203-1202

24 23 22 21 20 19 18 17 16 15 14 13

12 11 10 9 8 7 6 5 4 3 2 1

TP_CLK <34>
TP_DATA <34>
+5V
+5V
+5VAL
ACIN <22.34.38>
POWER_LED# <34>
SUSP_LED <34>
CHARGING_LED# <34>
BATT_LOW_LED# <34>
PWR_LED#
PWR_SUSP_LED

+5V
C232
0.1uF 0402_16V4Z

TP1T

Battery mode Hibernation

[illegible][illegible]

Power OK Circuit

The schematic diagram illustrates a Power OK circuit. It consists of two comparators, U17C and U17D, both SN74LVC14APWLE_TSSOP14. The first comparator (U17C) has its non-inverting input (pin 14) connected to +3VALW and its inverting input (pin 7) connected to a voltage divider consisting of a 180K resistor (R212) and a 1uF capacitor (C229) connected to +3VS. The output of U17C (pin 6) is connected to the non-inverting input (pin 14) of the second comparator (U17D). The inverting input (pin 7) of U17D is connected to ground. The output of U17D (pin 9) is connected to a voltage divider consisting of a resistor (R188) and a capacitor connected to ground. The final output of the circuit is PM_POK <23>.

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Title			
S4R,LID,PIO,SYS CONN			
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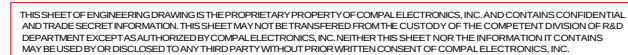
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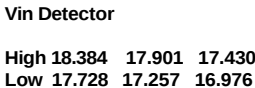


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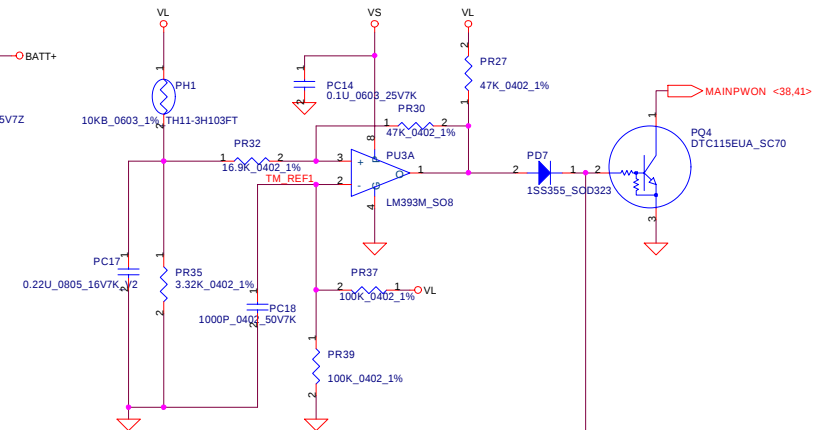
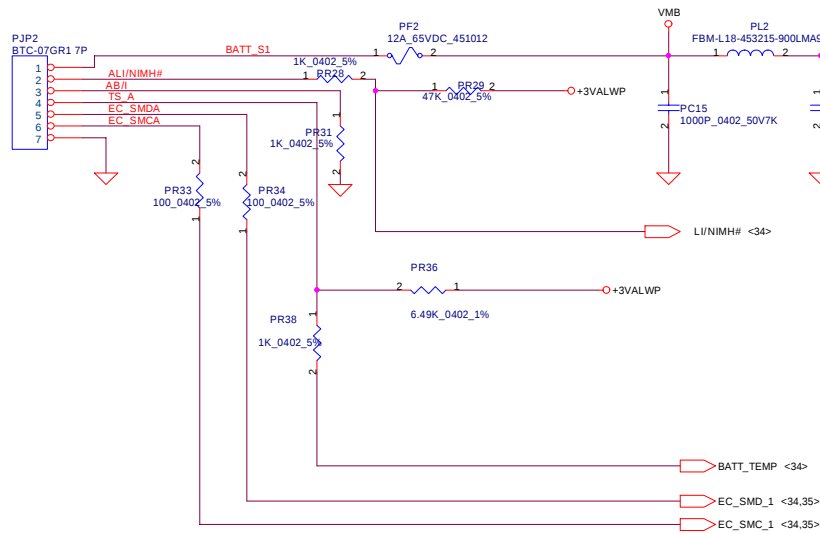




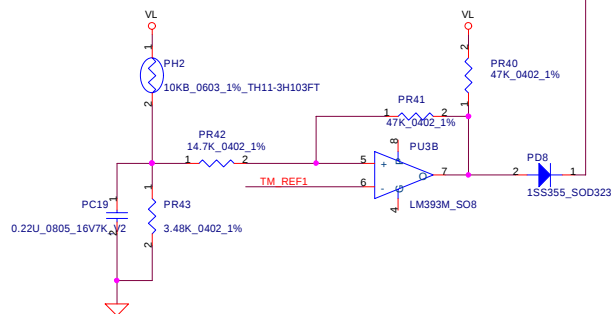
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DCIN and DETECTOR			
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PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C



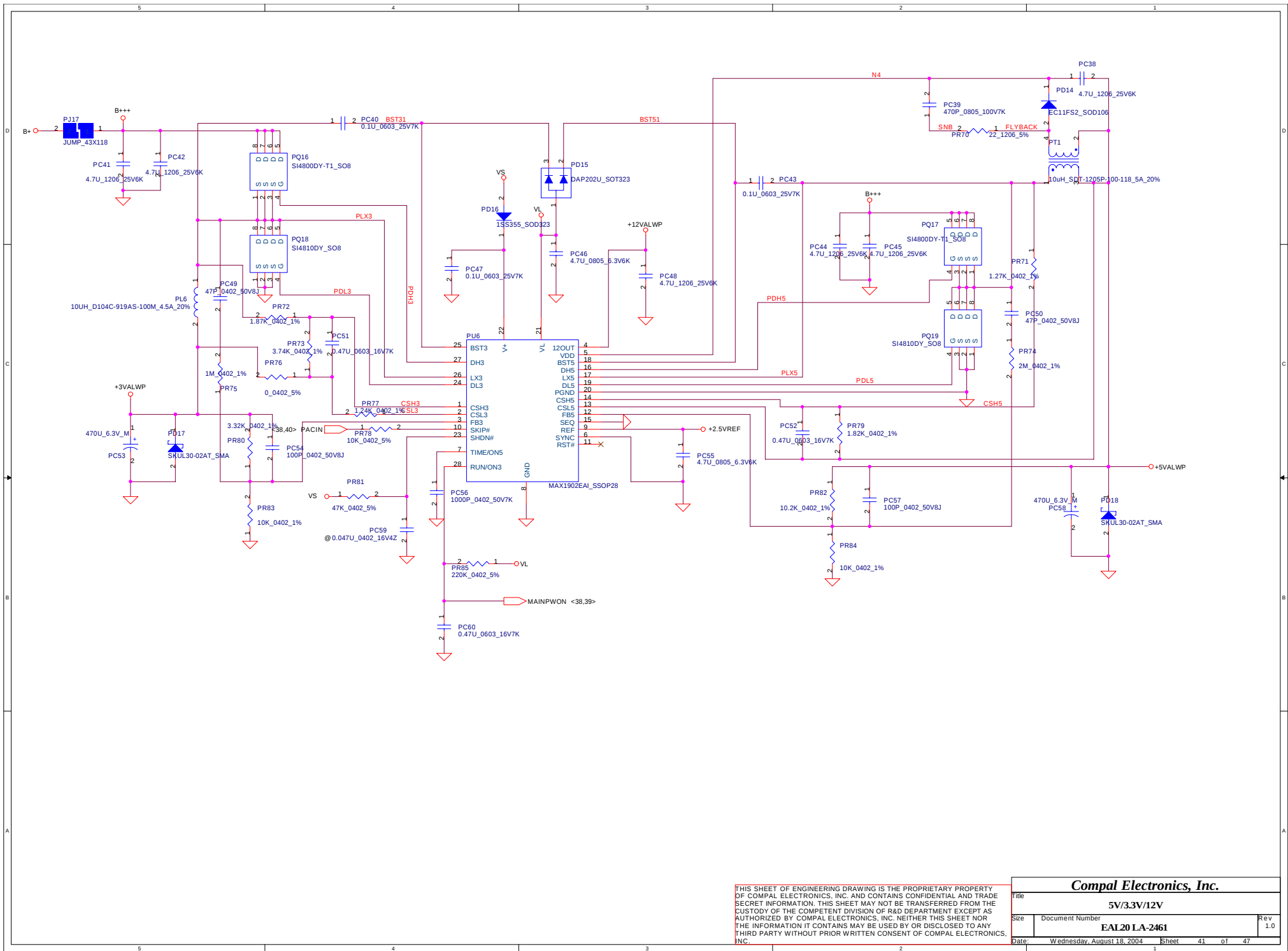
PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C



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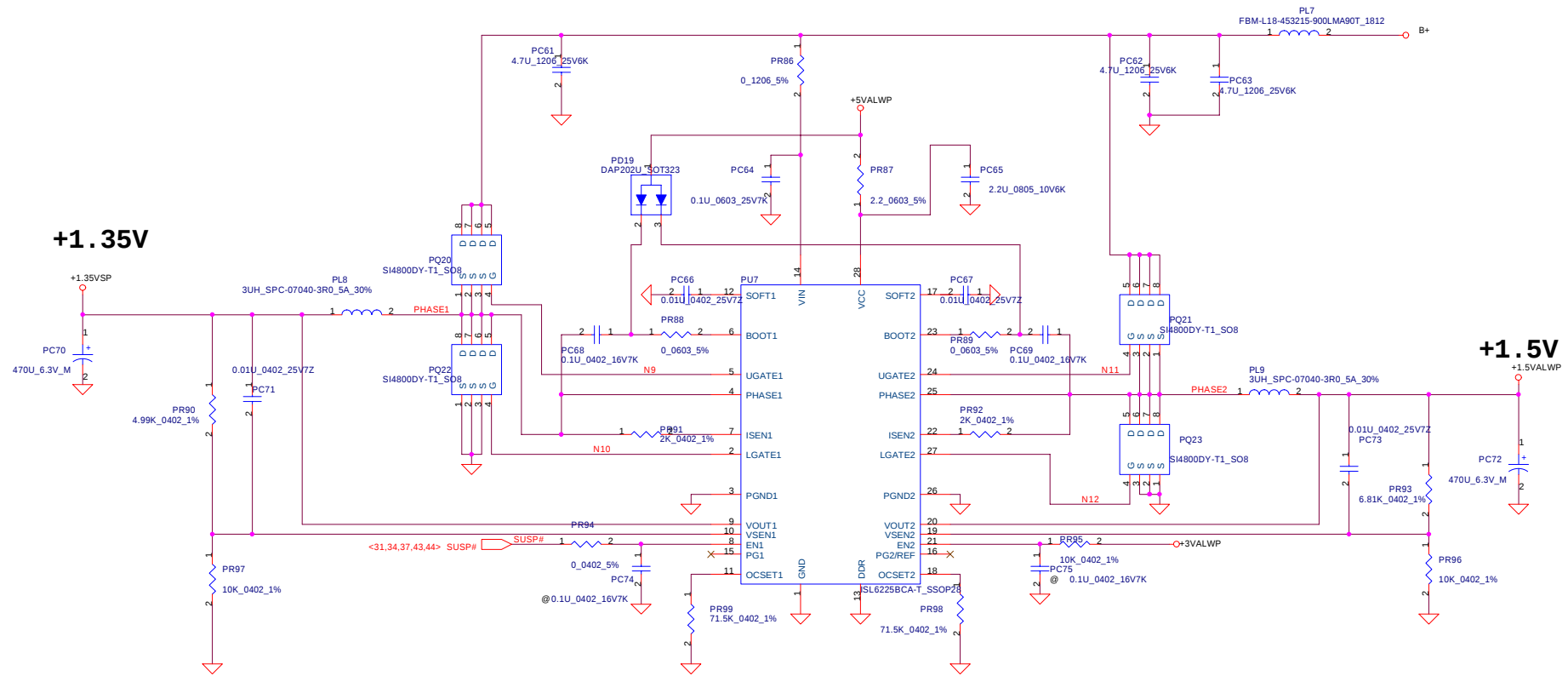
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BATTERY CONN / OTP			
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	EAL20 LA-2461	1.0	
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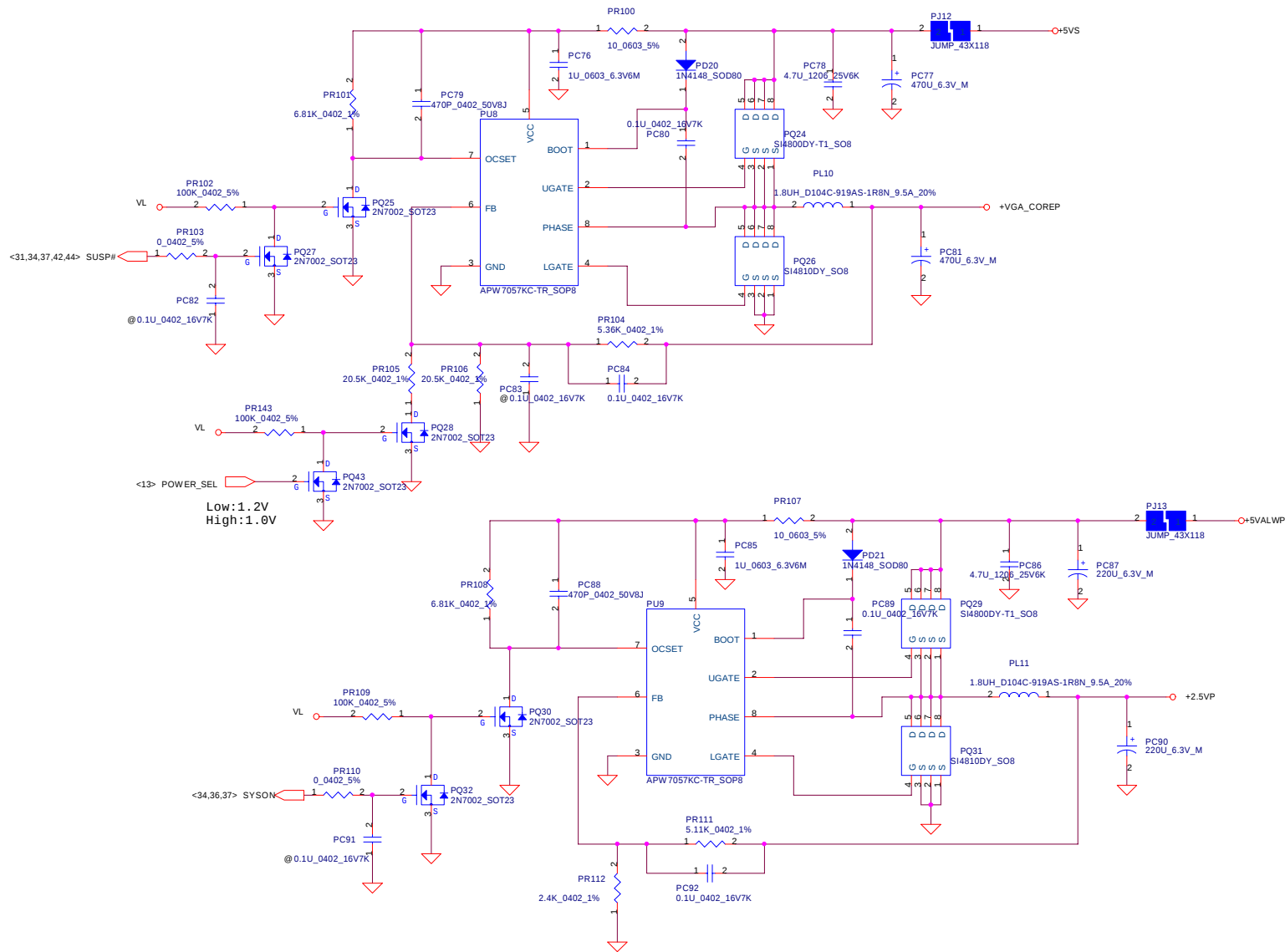
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Title		5V/3.3V/12V	
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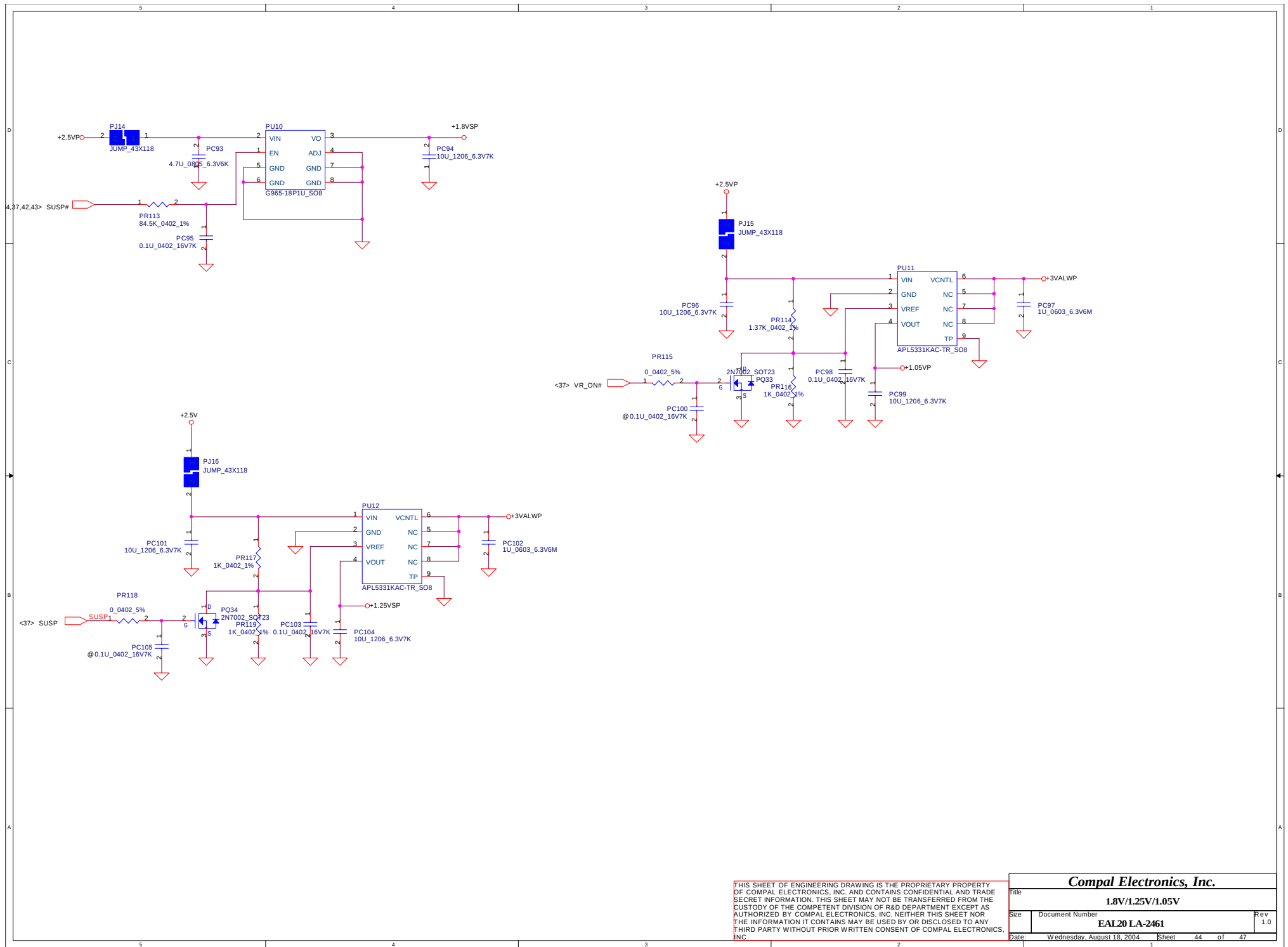
Compal Electronics, Inc.			
Title		1.35V/1.5V	
Size	Document Number	EAL20 1A-2461	
Date:	Wednesday, August 18, 2004	Sheet	42 of 47
		Rev	1.0

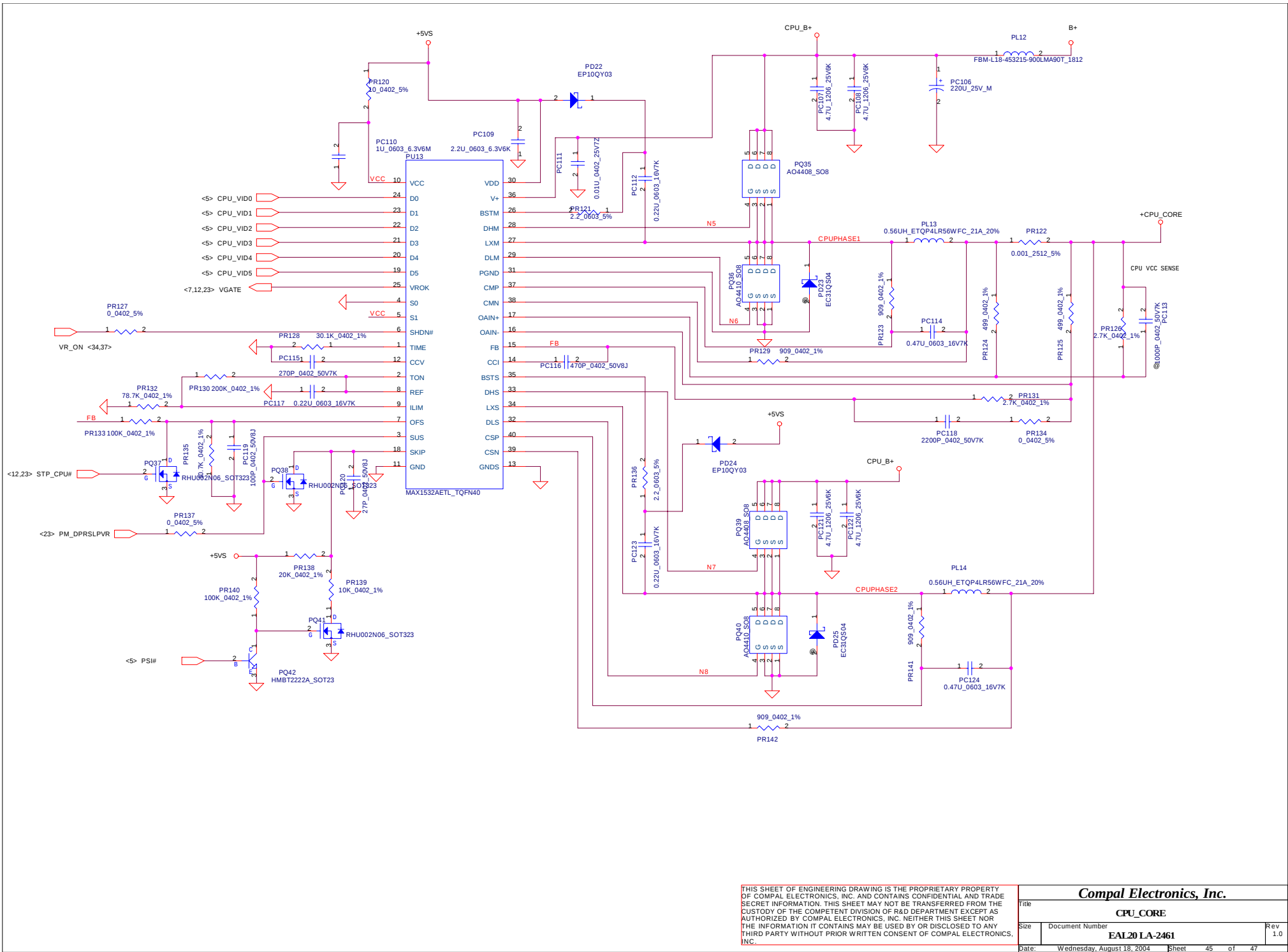


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Title			25V/VGA_CORE	
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PWR PIR LIST

EVT

page	Reason for change	Modify list
41	Improve design margin	Change PD17,PD18 from SSM14 to SKUL30-02AT
43	Change 2.5V,VGA_CORE OCP to 8A	Change PR101,PR108 from 5.11K to 6.81K
39	Improve design margin	Change PF2 rating from 7A to 12A

DVT

43	Reverse POWER_SEL signal level for HW request	Add PR143(100K),PQ43
41	Adjust 3.3V OCP	Change PR72 from 1.27K to 1.87K_0402_1% Change PR73 from 1.27K to 3.74K_0402_1% Change PR77 from 620 to 1.24K_0402_1%
41	Adjust 5V OCP	Change PR71 from 1.54K to 1.27K_0402_1% Change PR79 from 698 to 1.82K_0402_1%
43	Change choke for design margen	Change PL10,PL11 from 4.7UH to 1.8UH
44	Add 1.8V delay time for HW	Change PR113 from 0 to 84.5K_0402_1% Add 0.1U at PC95
45	For EMI requirement	Change PR121,PR136 from 0 to 2.2_0603_5%
45	Adjust CPU_CORE voltage	Change PR126,PR131 from 3K to 2.7K_0402_1%
42	Modify 1.5V enable signal for HW request	Change PR95 from 0 to 10K_0402_1%

PVT

43	Modify PL10 and PL11 Footprint	
38	Change DC-IN Jack as "SINGA_2DC-G213-B04_4P"	
41	Change PL5 as PJ17	
43	Raise VGA_CORE voltage to 1.21V for HW requirement	Change PR104 from 5.11K_0402_1% to 5.36K_0402_1%
45	Adjust CPU_CORE voltage	Change PC118 from 0.022U to 2200P

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Title		
EAL20 PIR LIST		
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EAL20 LA-2461 SCHEMATIC CHANGE LIST REVISION CHANGE: 0.1 TO 0.2					EAL20 LA-2461 SCHEMATIC CHANGE LIST REVISION CHANGE: 0.2 TO 0.3				
NO DATE PAGE MODIFICATION LIST					NO DATE PAGE MODIFICATION LIST				
PURPOSE					PURPOSE				
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1	6/23	P31	POP R521	CODEC CLOCK SOURCE FROM CLOCK_GEN	1	7/15	P19	CHANGE R389,R393 BOM STRUCTURE FROM UMA@ TO @	REMOVE IN UMA SKU
2	6/23	P35	CHANGE R342.1 CONNECTION FROM SYSON TO SYSON#	CHANGE USB POWER TO LOW ACTIVE	2	7/20	P16	RESERVE D2 SIZE CAP C701 ON +VGA_CORE PLANE	ADD ONE MORE BULK CAP FOR VGA CORE
3	6/23	P29	CHANGE R492.2 PULL HIGH FROM +3VS TO +VCC_5IN1	CHANGE PULL HIGH POWER	3	7/20	P28	ADD D12,R217,R438,R440,R443,R447,R448,R456,R458,R474 ,R495,R501 BOM STRUCTURE 5IN1@	CHANGE BOM STRUCTURE TO CONTROL BOM
4	6/23	P36	SWAP PIN OF JP16	CHANGE JP16 DIRECTION			P29	ADD C518,C585,C592,C617,C618,R449,R455,R492,R494,R502 ,R520,R528,JP13,U44 BOM STRUCTURE 5IN1@	
5	6/23	P12	RESERVE C671	ADD CAP TO CONTROL VGATE RISING TIME	4	7/20	P12	ADD R524 BOM STRUCTURE 5IN1@	
6	7/05	P12	CHANGE CLK_PCI_ICH CONNECT FROM U49.11 TO U49.7	CHANGE ICH PCI CLK SOURCE TO FREE RUN			P31	NEW ADD R619 BETWEEN L_OUT_L AND AMP_LEFT	ADD RES TO BYPASS MUX
			CHANGE CLK_PCI_1394 CONNECT FROM U49.7 TO U49.11	CLOCK, TO SOLVE SYSTEM CAN NOT SHUTDOWN ISSUE			P31	NEW ADD R620 BETWEEN L_OUT_R AND AMP_RIGHT	
7	7/05	P29	CHANGE 5IN1 CONNECTOR FROM TAIQOL TO TAITWAN	CHANGE CONNECTOR VENDOR	5	7/20	P12	CHANGE R574 TO RESERVE	CHANGE AC CODEC CLOCK SOURCE
8	7/06	P29	DEL R251,R249	DEL 75OHM TERMINATION			P31	CHANGE R527,R521 TO RESERVE	
		P13	ADD R603,R604	ADD 75OHM TERMINATION CLOSE TO CHIP	6	7/20	P31	CHANGE X3,C610,C619 TO MOUNT	
		P19	RESERVE R605,R606	RESERVE 75OHM TERMINATION CLOSE TO CHIP			P34	CHANGE U45.47 NET NAME FROM EAPD TO EAPD_CODEC	USE KBC TO MUTE AMP
9	7/06	P22	INSERT D29 BETWEEN GPI11 AND ACIN	PREVENT SB LEAKAGE DURING DC-IN			P32	NEW ADD R621 BETWEEN EAPD_KBC AND U35.11	
				TO SOLVE POWER BOTTON NO FUNCTION ISSUE			P32	ADD U9A, CONNECT U9A.1 TO EAPD_CODEC,U9A.2 TO EAPD_KBC	
10	7/06	P13	ADD R317 100K_0402_5% PULL DOWN POWER_SEL	PREVENT SIGNAL FLOATING	7	7/21	P34	U9A.3 TO EAPD	ADD SKU ID FUNCTION FOR EC RECOGNIZES
11	7/06	P29	CHANGE R528 CONNECTION	FOR CUSTOMER REQUEST				RESERVE R622.2,R623.2,R624.2 PULL HIGH TO +3VALW	
12	7/06	P36	DEL CP1-CP6, ADD C329,C672-C697	FOR EMI REQUEST				NEW ADD R625.2,R626.2,R627.2 PULL LOW TO GND	
13	7/06	P36	CHANGE Q16.1 CONNECT TO ON/OFF	TO CORRECT LID SW FUNCTION				ADD SKU_ID0 CONNECT BETWEEN U35.93,R622.1,R625.1	
14	7/06	P20	CHANGE R294 FROM 0603 TO 0805,R19 FROM 0805 TO 1206	TO INCREASE RATING				ADD SKU_ID1 CONNECT BETWEEN U35.94,R623.1,R626.1	
15	7/07	P31	RESERVE 1M_0402_5% R607-R614,HCT4066 U48	TO CONTROL POWER ON/OFF AUDIO CD PATH	8	7/26	P28	ADD SKU_ID2 CONNECT BETWEEN U35.75,R624.1,R627.1	
			RESERVE 10K_5%_0402_R615,0_0402_5% R617,RESERVE R616	ADD MUX SW CONTROL			P29	Modify "5IN1@ " to "5IN1@"	
16	7/07	P12	ADD L35 BETWEEN +3VS AND +3VS_CLK	FOR CUSTOMER REQUST			P29	Modify "5IN1@ " to "5IN1@"	
17	7/08	P37	CHANGE C554 FROM 0.01U TO 0.1U	CHANGE POWER ON SEQUENCE			P30	Modify "KS@ " to "KS@"	
			CHANGE U19.4 NET FROM RUNON TO 5VS_ON				P33	Modify R157 remark from "FIR@" to "@"	
			ADD R618,Q44,C700, ADD 5VS_ON NET	CONTROL +5VS CONTROL GATE			P21	Modify JP3 footprint from	
18	7/09	P06	CHANGE R461 FROM 27.4 TO 37.4OHM	CHANGE RESISTANCE FOR 855GME	9	7/29	P36	"SUYIN_030336FR004T115ZU_4P_EAL20" to	
19	7/09	P26	CHANGE C325 FROM 0.01U TO 0.1U,R292 FROM 5.9K TO 5.36K	CHANGE R,C TO PASS LAN TEST			P35	"030336FR004T115ZU_4P_EAL20"	
20	7/09	P29	CHANGE CP2211 U18 FROM C1 TO D3 VERSION	CHANGE FOR MATERIAL EOL				Shift SW/LED Connector signal up one pins, leave	
								JP15.11 as NC.	
								Add 3 screw hole, H23(H_C126D126N), H24 and H25	
								(H_079X126D40X87)	
								H23 for M/B location Keeping.	
								H24 and H25 for Double USB holding.	
					10	7/31	P20	L5 and L4 change as 0_0805_5%	
							P31	L9 and L11 change as 0_0603_5%, L26, L27 and L28	
								change as 0_0805_5%	
							P32	L29 and L30 change as 0_0805_5%, L26, L31, L32, L33 and	
								L34 change as 0_0603_5%	
							P28	SDCK_XDWE# saperate SD_CLK and XDWE#, add R628 for	Some card can't detect because reflection
								XDWE#	
							P29	R455.2 and JP13.36 SDCK_XDWE# change XDWE#.	
								R450.1 and JP13.8 SDCK_XDWE# change SD_CLK.	
							XXX	Update schematic name from LA2641 to LA2461.	
					11	8/02	P20	Add D30 for EMI ESD test fail.	
							P32	L31, L32, L33 and L34 change as Bead.	
							P04	Delete P@ on PU5B.	
					12	8/03	P19	Update R396 and R397 as 75_0402_1%.	
					12	8/04	P13	Update R603, R604 and R365 as 75_0402_1%.	