

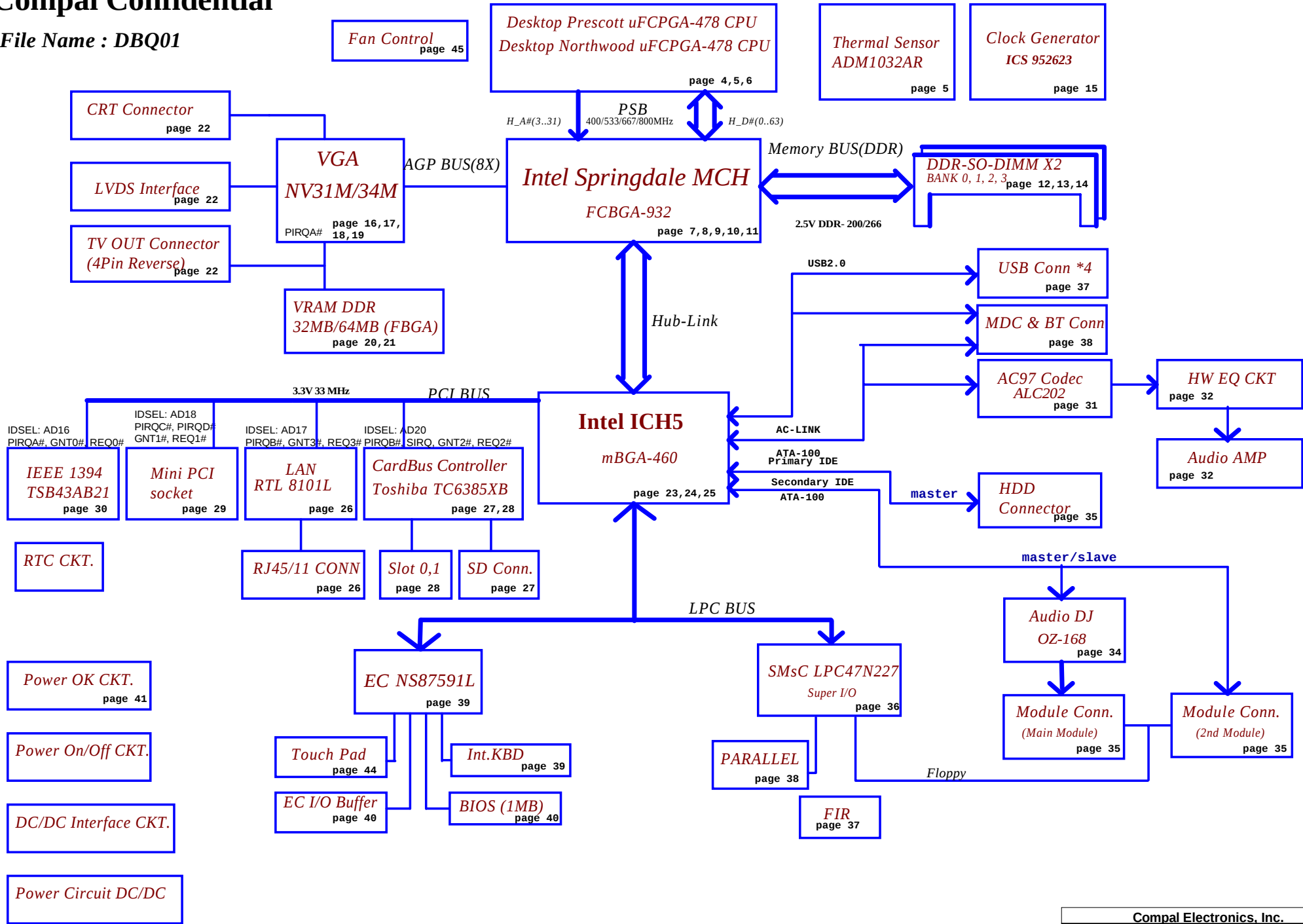
DBQ01 Rev0.1 Schematics Document

Intel Prescott uFCPGA-478 / P4 Northwood

with Springdale / ICH5 / nVIDIA NV34M/31M chipset

2003/07/01

Compal Electronics, Inc.			
Title			
Cover Sheet			
Size B	Document Number LA-2041		Rev 0.1
Date:	~P期三, 七月 09, 2003		Sheet 1 of 56



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_VID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VTT_GMCH	+1.225V (Prescott) / +1.45V (Northwood)	ON	OFF	OFF
+VGA_CORE	1.3V switched power rail for VGA chip	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 4X/8X	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
VGA			PIRQA
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB
Mini-PCI	AD18	1/4	PIRQC/PIRQD
1394	AD16	0	PIRQA
SD	AD22		

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b	OZ168	0011 0100 b
(24C04)	1011 000Xb		

ICH5 SM Bus address

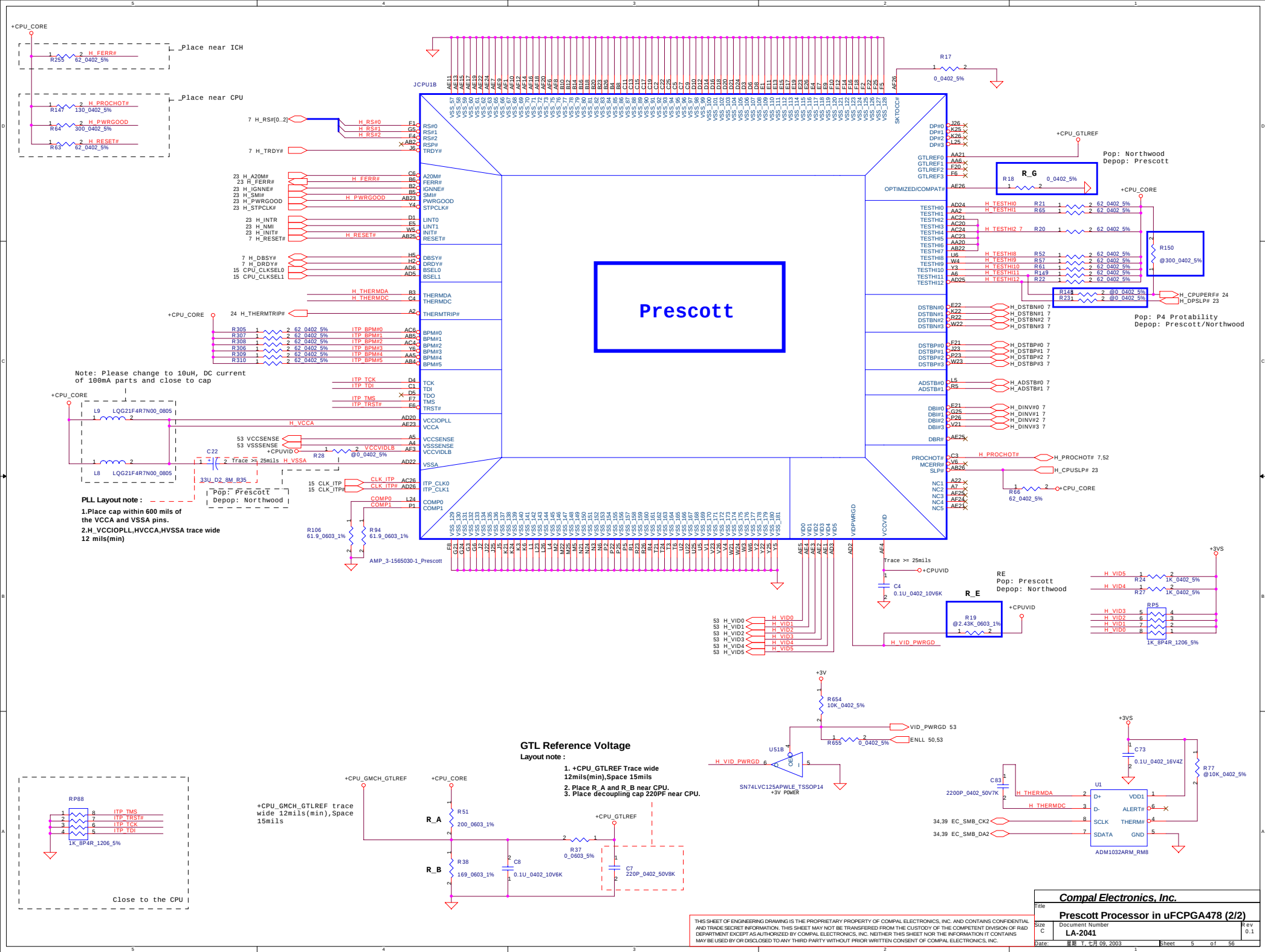
Device	Address
Clock Generator (ICS 952623)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 001Xb

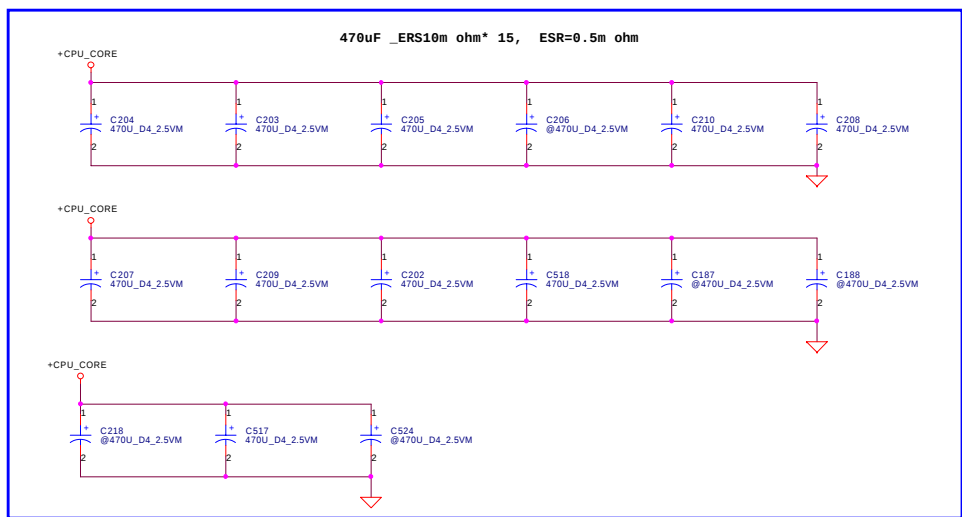
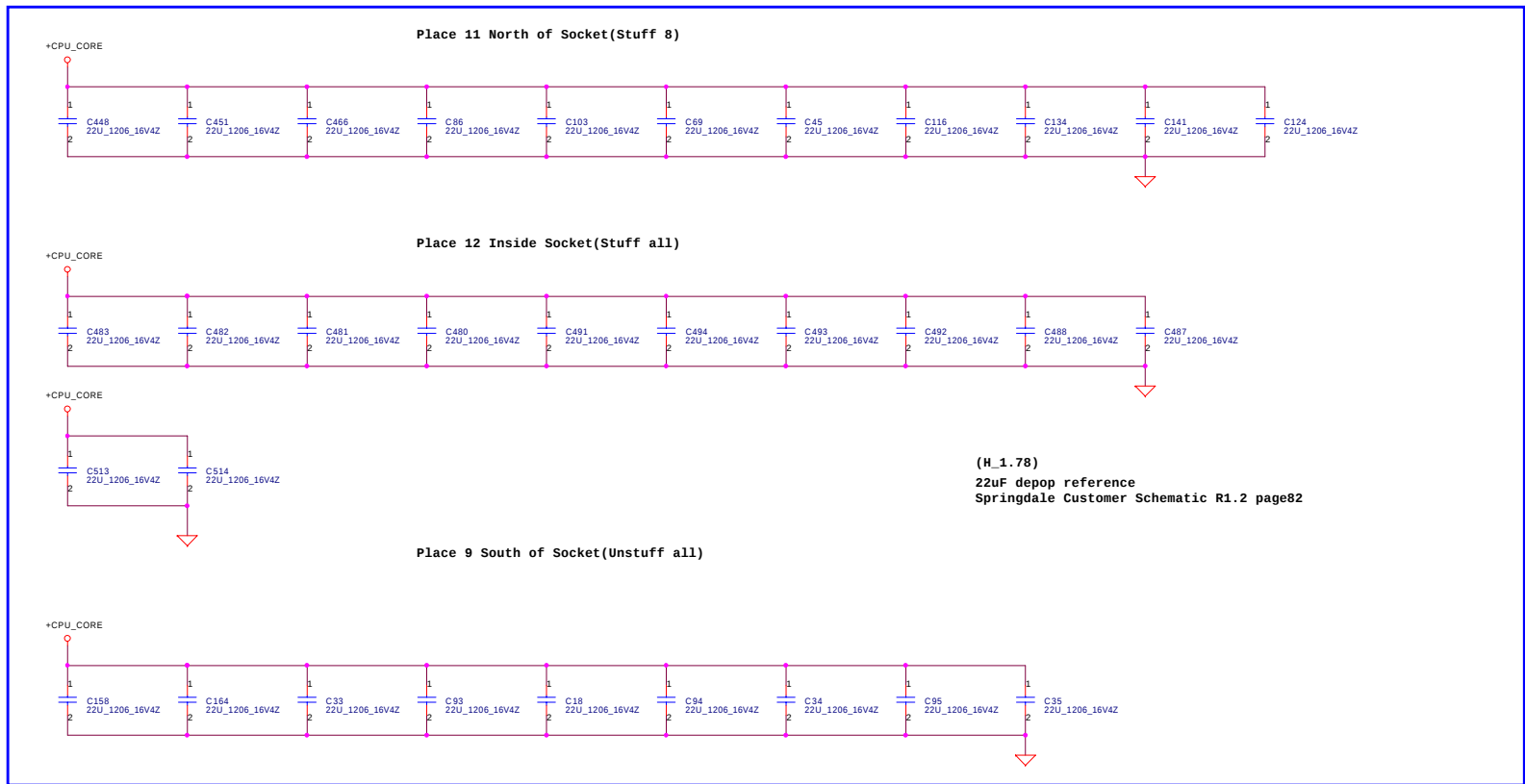
STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

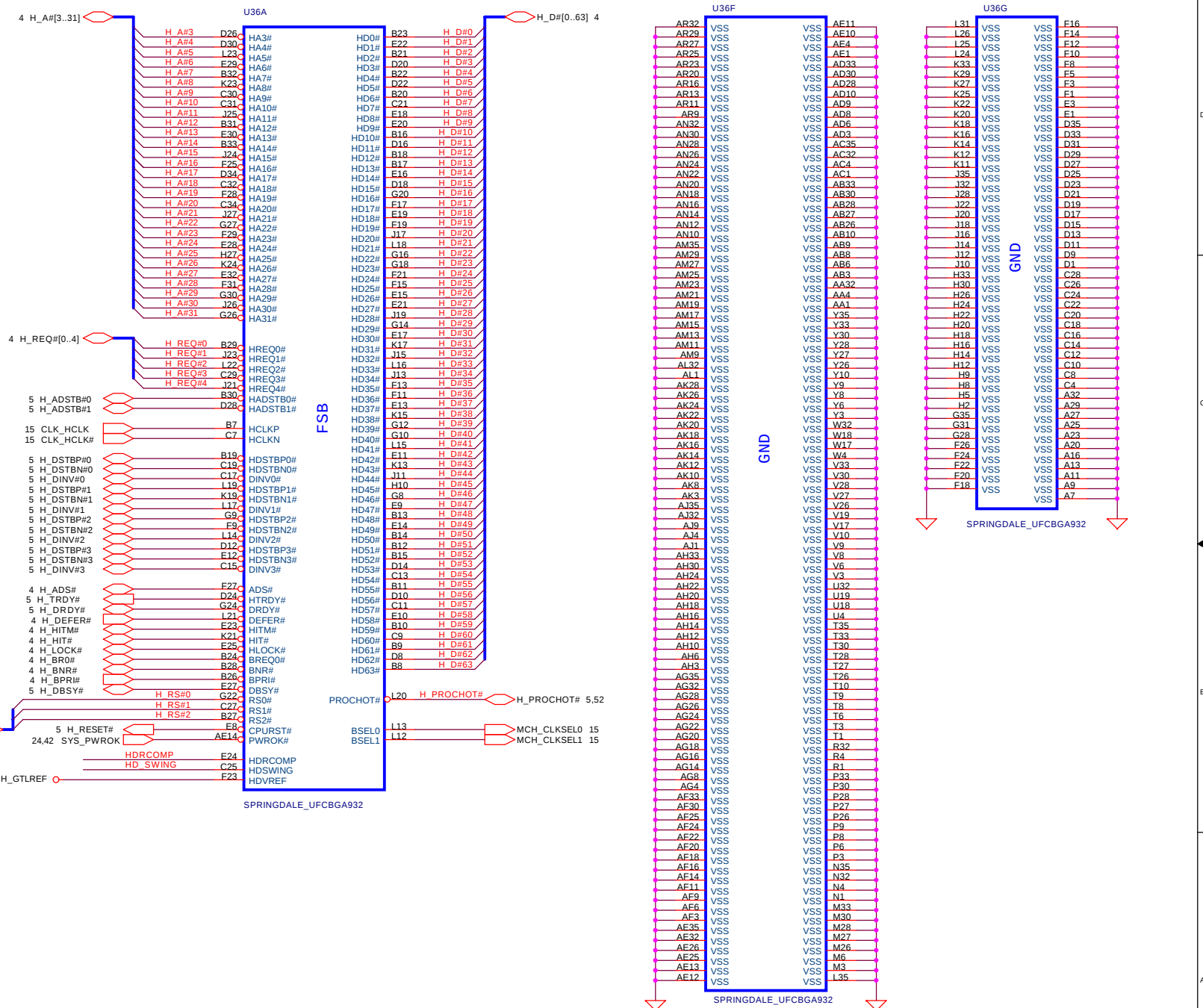
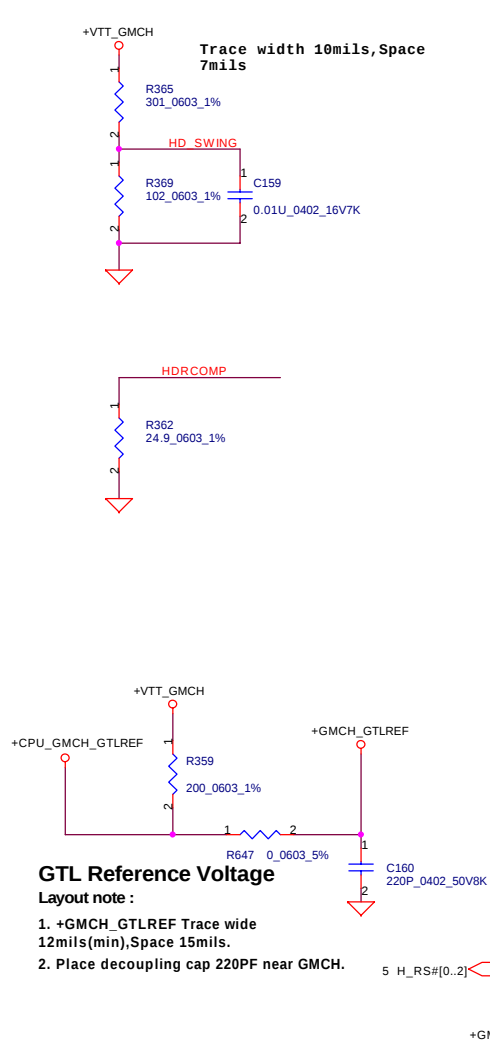
Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	





Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11
(12474)page239

Decoupling Reference Requirement:
560uF Polymer, ESR:5m ohm(each) * 10
22uF X5R * 32



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12,14 DDRA_SMA[0..12] **DDRA SMA[0..12]**

U36B

DDRA SMA0 A134
DDRA SMA1 AL33
DDRA SMA2 AK29
DDRA SMA3 AN31
DDRA SMA4 AL30
DDRA SMA5 AL26
DDRA SMA6 AL28
DDRA SMA7 AN25
DDRA SMA8 AP26
DDRA SMA9 AP24
DDRA SMA10 AJ33
DDRA SMA11 AN23
DDRA SMA12 AN21

SMAA_A0
SMAA_A1
SMAA_A2
SMAA_A3
SMAA_A4
SMAA_A5
SMAA_A6
SMAA_A7
SMAA_A8
SMAA_A9
SMAA_A10
SMAA_A11
SMAA_A12

SDQS_A0
SDM_A0
SDQ_A0
SDQ_A1
SDQ_A2
SDQ_A3
SDQ_A4
SDQ_A5
SDQ_A6
SDQ_A7

AN11
AP12
AP10 DDRA SDQ0
AP11 DDRA SDQ1
SDQ_A2
AM12 DDRA SDQ2
AN13 DDRA SDQ3
AM10 DDRA SDQ4
AL10 DDRA SDQ5
AL12 DDRA SDQ6
AP13 DDRA SDQ7

DDRA_SDQS0 12,14
DDRA_SDM0 12,14

SDQS_A1
SDM_A1
SDQ_A8
SDQ_A9
SDQ_A10
SDQ_A11
SDQ_A12
SDQ_A13
SDQ_A14
SDQ_A15

AP15
AP16
AP14 DDRA SDQ8
AM14 DDRA SDQ9
AL18 DDRA SDQ10
AP19 DDRA SDQ11
AL14 DDRA SDQ12
AN15 DDRA SDQ13
AP18 DDRA SDQ14
AM18 DDRA SDQ15

DDRA_SDQS1 12,14
DDRA_SDM1 12,14

SDQS_A2
SDM_A2
SDQ_A16
SDQ_A17
SDQ_A18
SDQ_A19
SDQ_A20
SDQ_A21
SDQ_A22
SDQ_A23

AP23
AM24
AP22 DDRA SDQ16
AM22 DDRA SDQ17
AL24 DDRA SDQ18
AN27 DDRA SDQ19
AP21 DDRA SDQ20
AL22 DDRA SDQ21
AP25 DDRA SDQ22
AP27 DDRA SDQ23

DDRA_SDQS2 12,14
DDRA_SDM2 12,14

SDQS_A3
SDM_A3
SDQ_A24
SDQ_A25
SDQ_A26
SDQ_A27
SDQ_A28
SDQ_A29
SDQ_A30
SDQ_A31

AM30
AP30
AP28 DDRA SDQ24
AP29 DDRA SDQ25
AP23 DDRA SDQ26
AM33 DDRA SDQ27
AM28 DDRA SDQ28
AN29 DDRA SDQ29
AM31 DDRA SDQ30
AN34 DDRA SDQ31

DDRA_SDQS3 12,14
DDRA_SDM3 12,14

SDQS_A4
SDM_A4
SDQ_A32
SDQ_A33
SDQ_A34
SDQ_A35
SDQ_A36
SDQ_A37
SDQ_A38
SDQ_A39

AF34
AF31
AH32 DDRA SDQ32
AG34 DDRA SDQ33
AF32 DDRA SDQ34
AD32 DDRA SDQ35
AH31 DDRA SDQ36
AG33 DDRA SDQ37
AE34 DDRA SDQ38
AD34 DDRA SDQ39

DDRA_SDQS4 12,14
DDRA_SDM4 12,14

SDQS_A5
SDM_A5
SDQ_A40
SDQ_A41
SDQ_A42
SDQ_A43
SDQ_A44
SDQ_A45
SDQ_A46
SDQ_A47

V34
W33
AC34 DDRA SDQ40
AB31 DDRA SDQ41
V32 DDRA SDQ42
V31 DDRA SDQ43
AD31 DDRA SDQ44
AB32 DDRA SDQ45
U34 DDRA SDQ46
U33 DDRA SDQ47

DDRA_SDQS5 12,14
DDRA_SDM5 12,14

SDQS_A6
SDM_A6
SDQ_A48
SDQ_A49
SDQ_A50
SDQ_A51
SDQ_A52
SDQ_A53
SDQ_A54
SDQ_A55

M32
M34
T34 DDRA SDQ48
T32 DDRA SDQ49
K34 DDRA SDQ50
K32 DDRA SDQ51
T31 DDRA SDQ52
P34 DDRA SDQ53
L34 DDRA SDQ54
L33 DDRA SDQ55

DDRA_SDQS6 12,14
DDRA_SDM6 12,14

SDQS_A7
SDM_A7
SDQ_A56
SDQ_A57
SDQ_A58
SDQ_A59
SDQ_A60
SDQ_A61
SDQ_A62
SDQ_A63

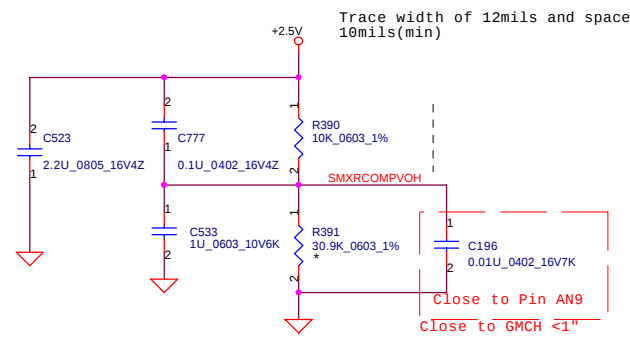
H31
H32
J33 DDRA SDQ56
H34 DDRA SDQ57
E33 DDRA SDQ58
F33 DDRA SDQ59
K31 DDRA SDQ60
J34 DDRA SDQ61
G34 DDRA SDQ62
F34 DDRA SDQ63

DDRA_SDQS7 12,14
DDRA_SDM7 12,14

DDR Channel A

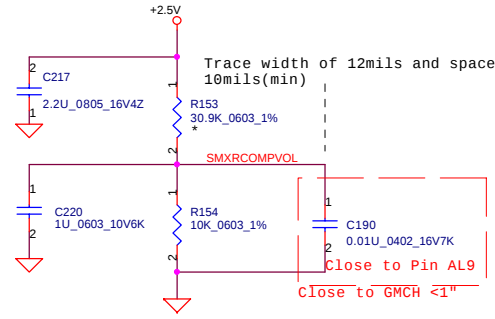
SPRINGDALE_UFCBGA932

DDRA_SDQ[0..63] **DDRA_SDQ[0..63]** 12,14

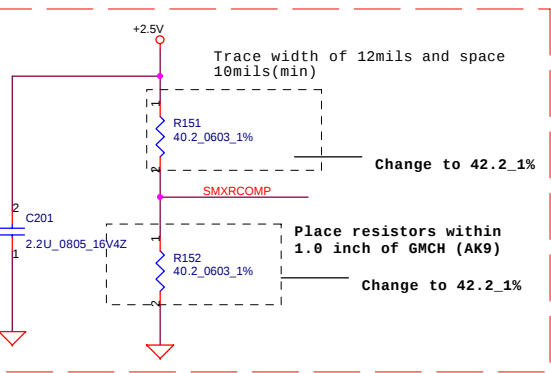
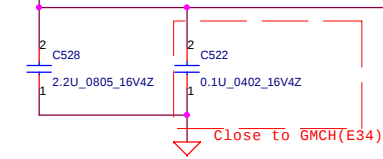


* Change to 31.12K

Follow Intel design guide
R1.11(12474) page124,125

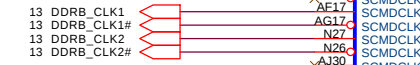
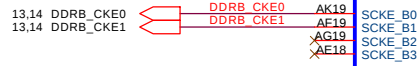
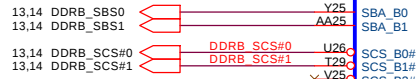
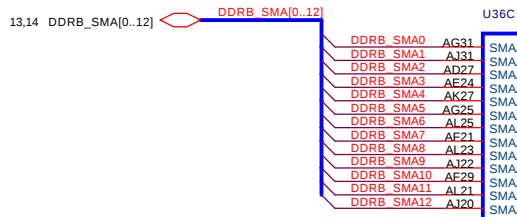


+SM_VREF_A **+SM_VREF_A trace width of 12mils and space 12mils(min)**

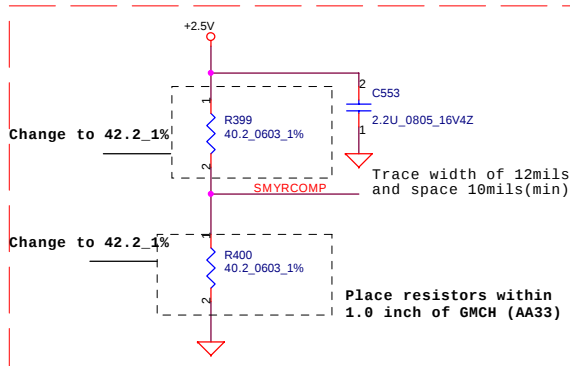
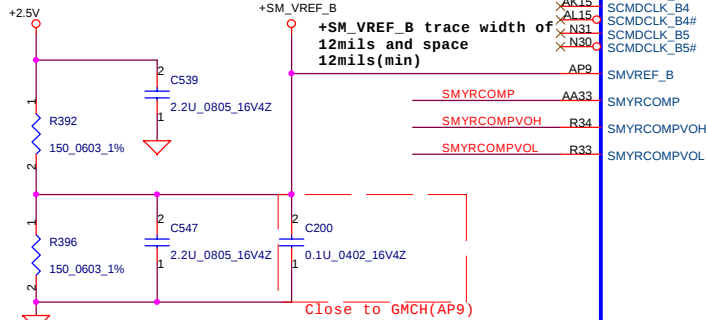


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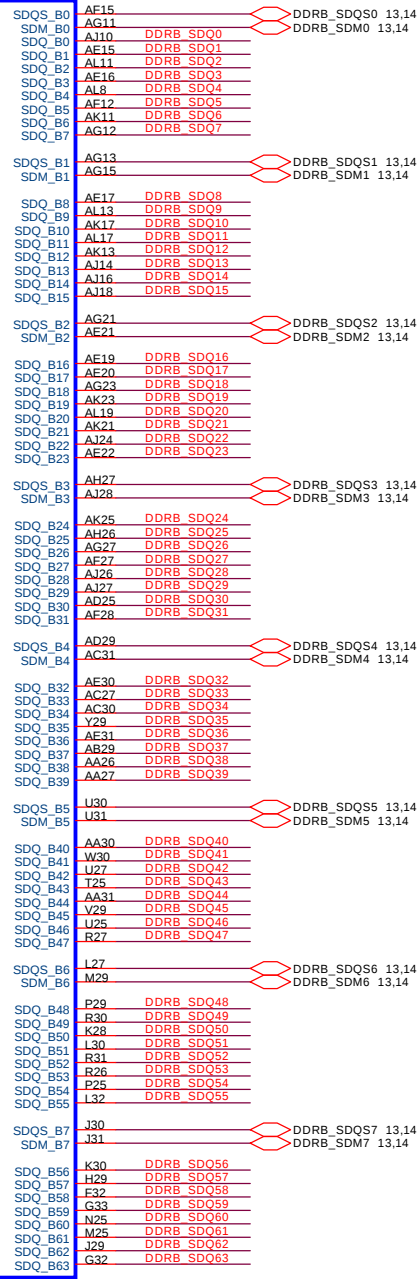
Compal Electronics, Inc.			
Springdale-DDR Interface-A(2/5)			
Title	Size B	Document Number	Rev 0.1
LA-2041		Date: ~P期三, 七月 09, 2003	Sheet 8 of 56



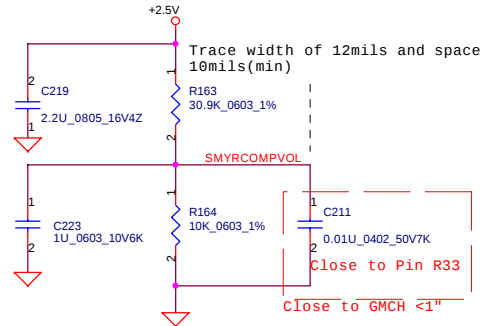
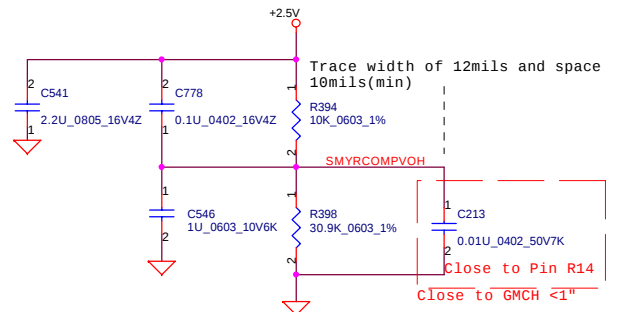
SM_VREF_B and SM_VREF_A are connected inside GMCH.



DDR Channel B



SPRINGDALE_UFCBGA932

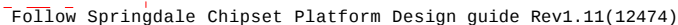
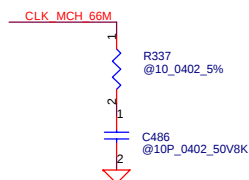
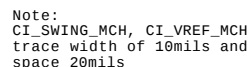
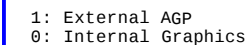


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Springdale-DDR Interface-B(3/5)

Size	Document Number	Rev
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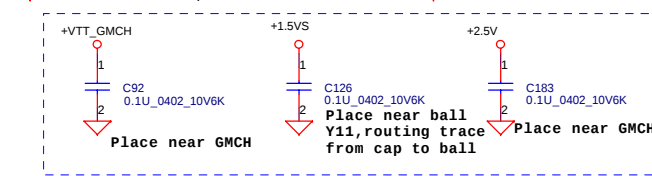
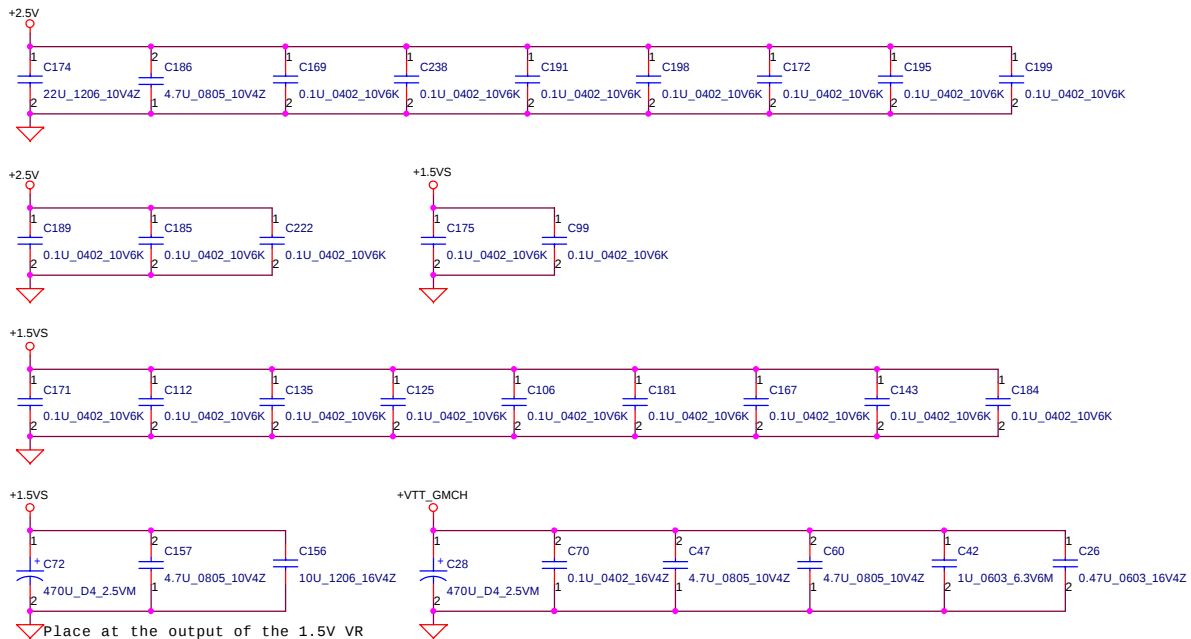
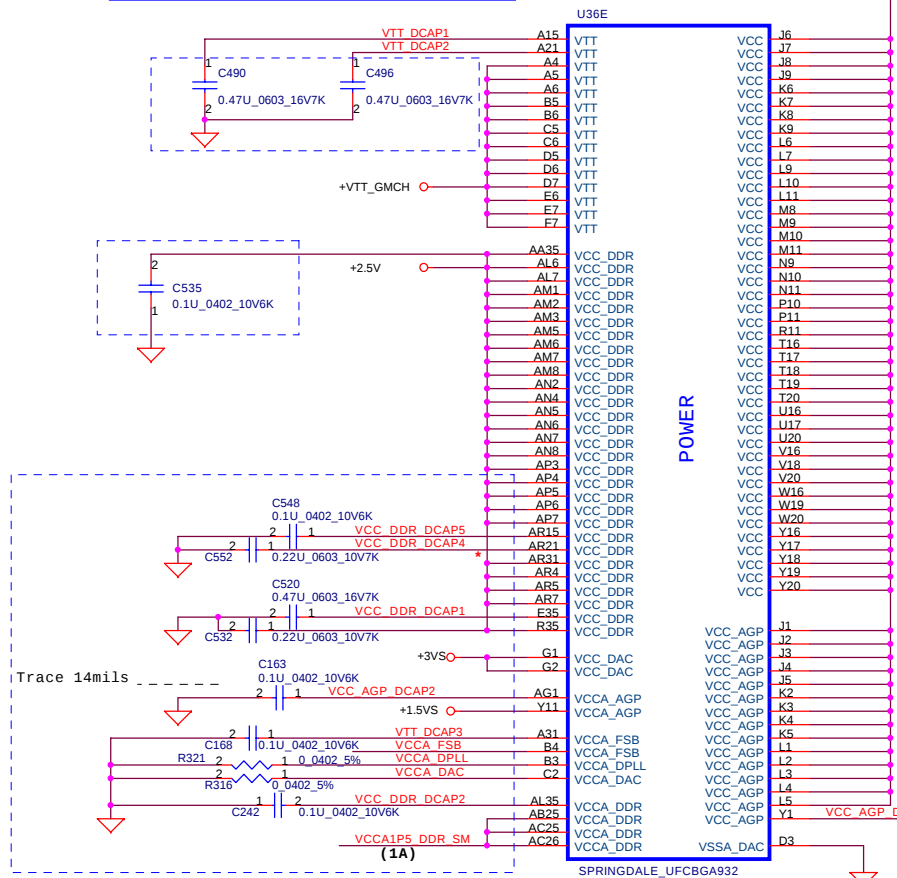
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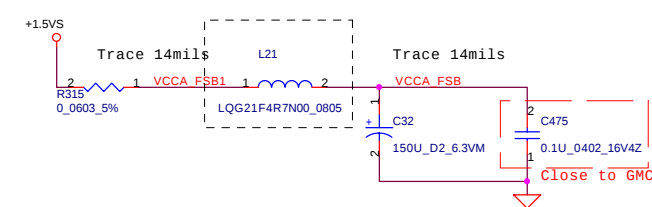
Note:
Springdale Customer Schematic R1.2 page18
AGP_SWING only had 0.1u cap ; But Springdale
Chipset Platform Design guide Rev1.11(12474)
page138 had a 0.01uf cap. need confirm with
Intel.



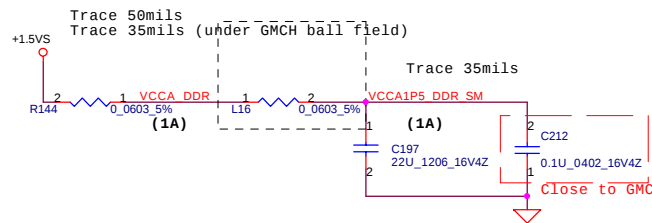
Note:
Placed less than 100 mils from ball
Route to GMCH ball without via



Note: Please change to 0.82uH, DC current of 30mA parts and close to cap



Note: Please change to 1uH(0.54uH-D-IN), DC current of 1000mA parts and close to cap



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Springdale-Decoupling (5/5)			
Title	Document Number	Rev	0.1
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Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11
(12474)page246,248

Decoupling Reference Document:
Springdale Customer Schematic R1.2 page84

DDR_B_VREF trace width of
12mils and space 12mils(min)

- 9,14 DDRB_SDQ[0..63] DDRB_SDQ[0..63]
9,14 DDRB_SDQS[0..7] DDRB_SDQS[0..7]
9,14 DDRB_SMA[0..12] DDRB_SMA[0..12]
9,14 DDRB_SDM[0..7] DDRB_SDM[0..7]

System Memory Decoupling caps

Decoupling Reference Document:
Springdale Customer Schematic R1.2 page26
each Channel(two DIMMs) requirement 0.1uF*24

DEBUG PORT

SO-DIMM 2 REVERSE

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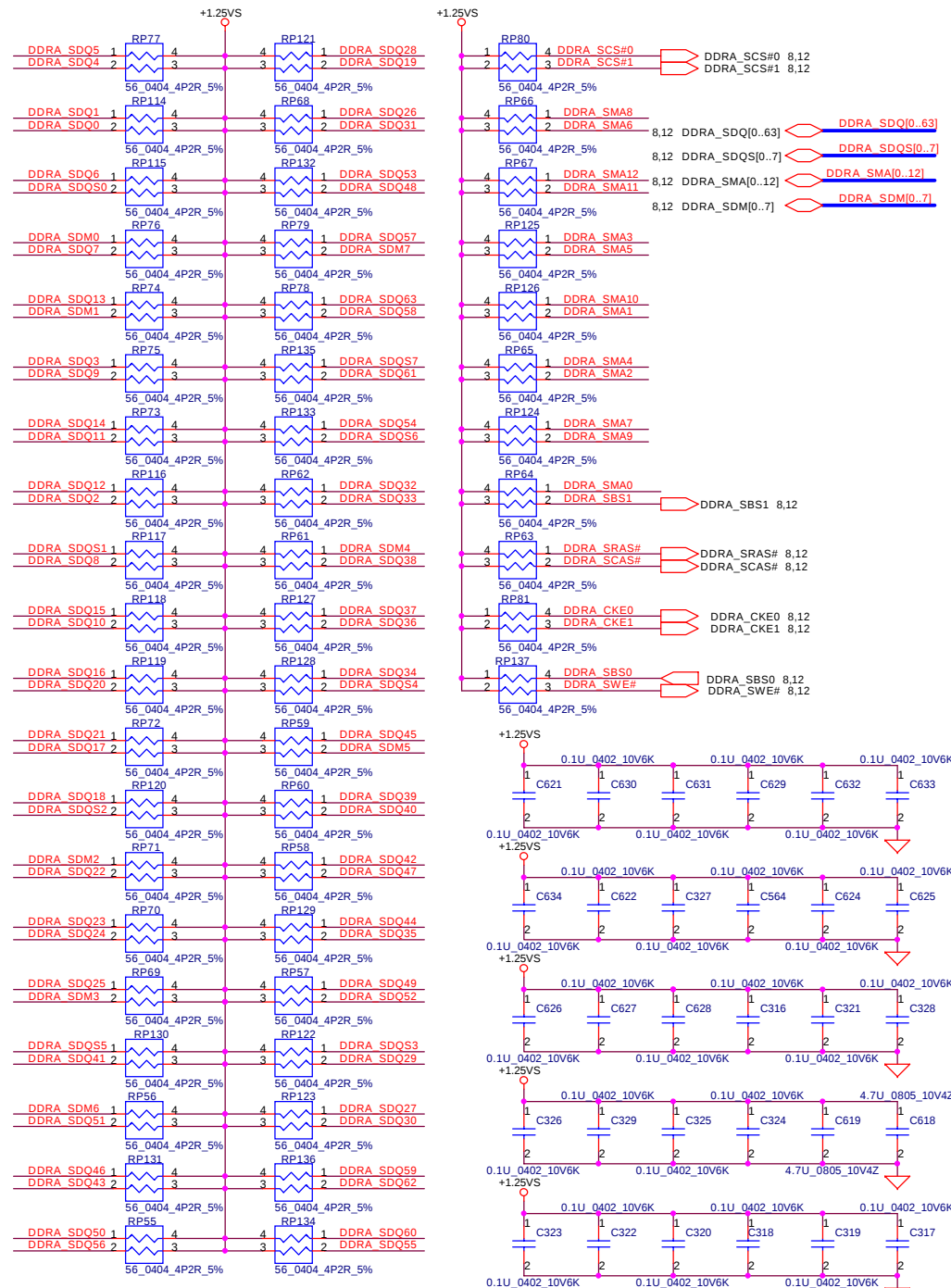
Compal Electronics, Inc.

DDR-SODIMM SLOT2

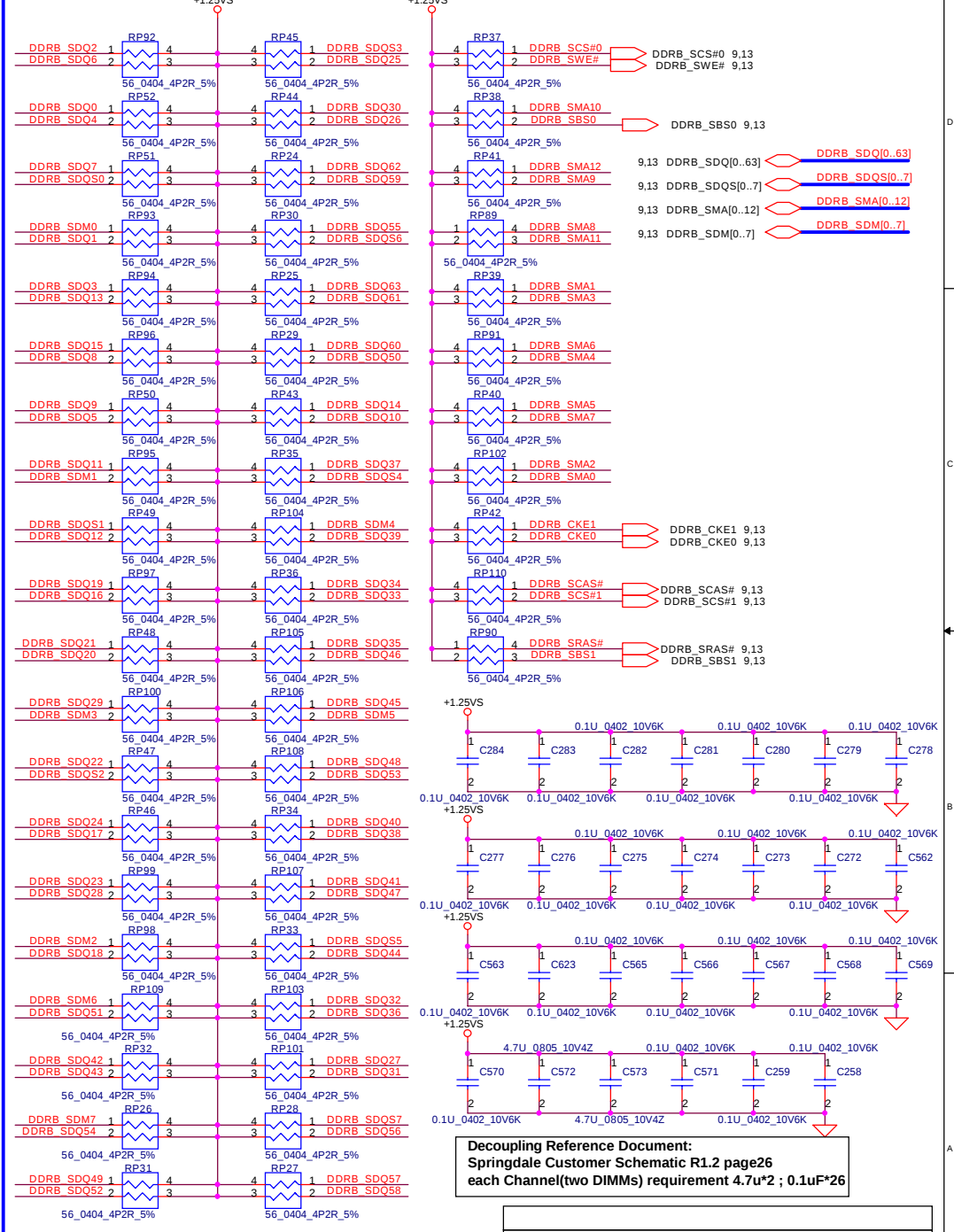
LA-2041

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Channel A(DIMM0) Termination resistors & Decoupling caps



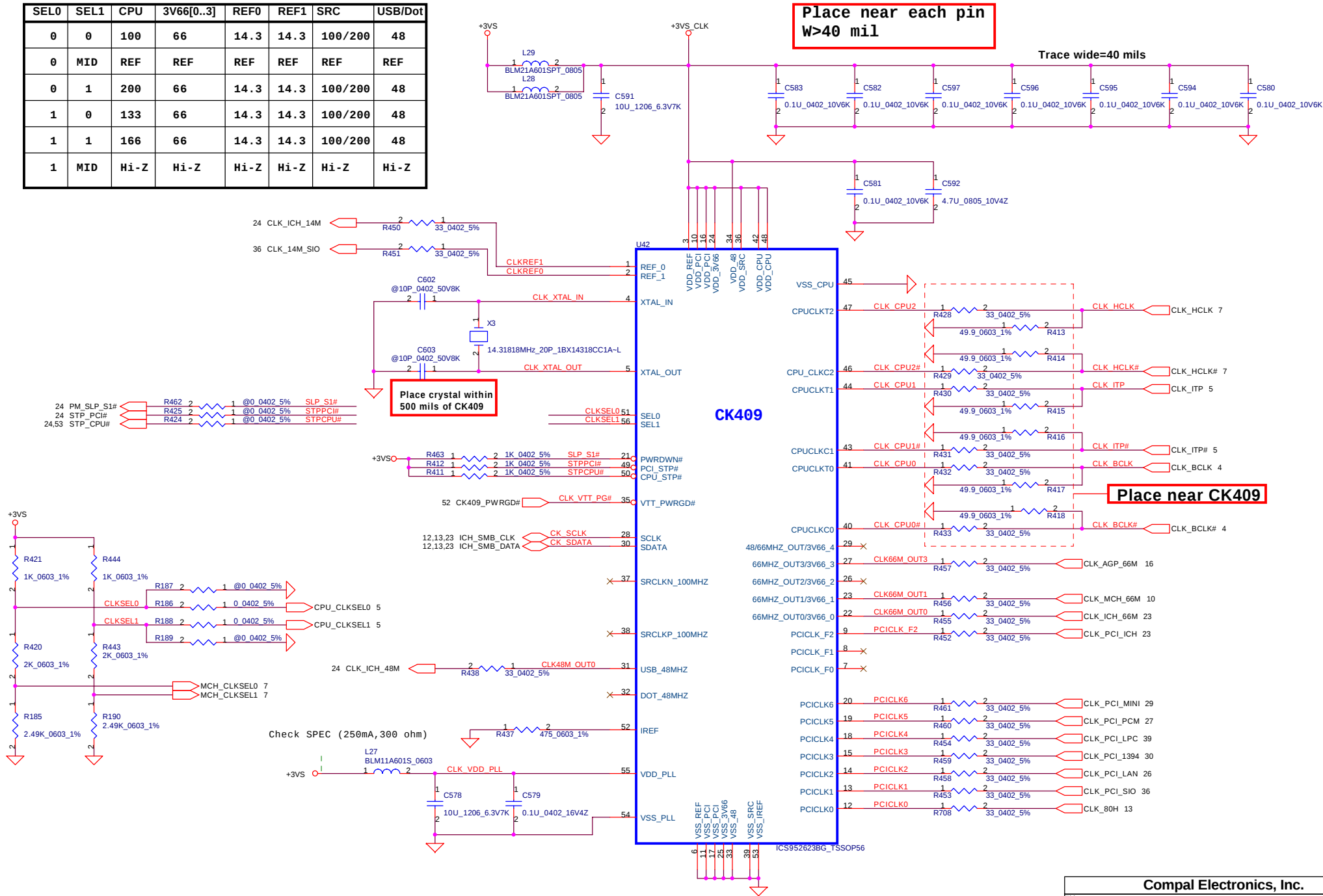
Channel B(DIMM1) Termination resistors & Decoupling caps



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Title		
DDR Termination Resistors		
Size	Document Number	Rev
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SEL0	SEL1	CPU	3V66[0..3]	REF0	REF1	SRC	USB/Dot
0	0	100	66	14.3	14.3	100/200	48
0	MID	REF	REF	REF	REF	REF	REF
0	1	200	66	14.3	14.3	100/200	48
1	0	133	66	14.3	14.3	100/200	48
1	1	166	66	14.3	14.3	100/200	48
1	MID	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z



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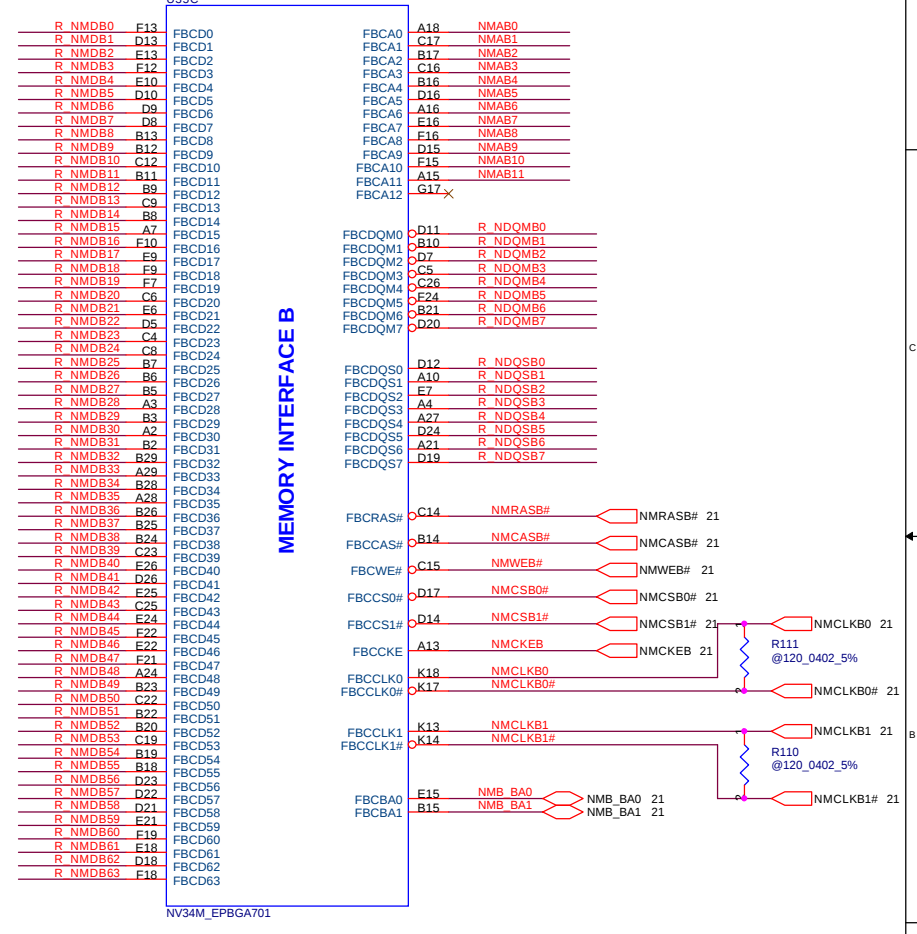
Compal Electronics, Inc.			
Clock Generator			
Title	Size	Document Number	Rev
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20 R_NDQMA[0..7] R_NDQMA[0..7]
20 R_NDQSA[0..7] R_NDQSA[0..7]
20 NMAA[0..11] NMAA[0..11]
20 R_NMDA[0..63] R_NMDA[0..63]

21 R_NDQMB[0..7] R_NDQMB[0..7]
21 R_NDQSB[0..7] R_NDQSB[0..7]
21 NMAB[0..11] NMAB[0..11]
21 R_NMDB[0..63] R_NMDB[0..63]



MEMORY INTERFACE
A



MEMORY INTERFACE
B



[illegible]

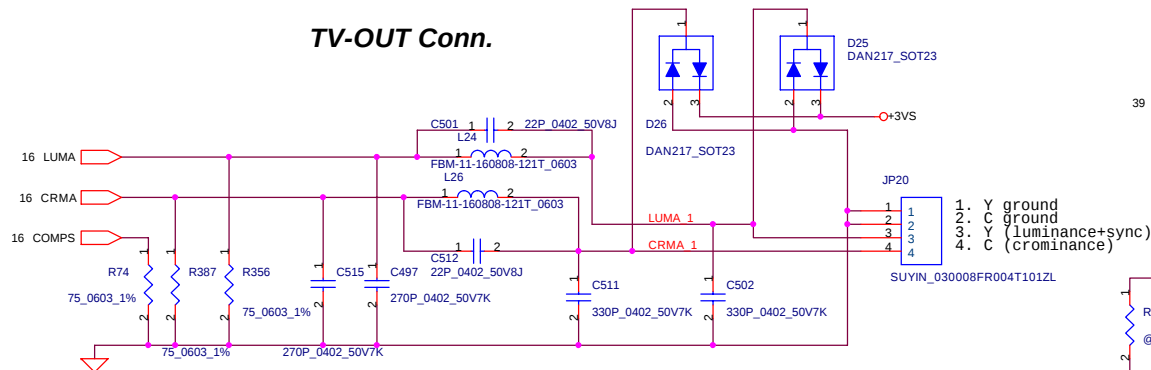
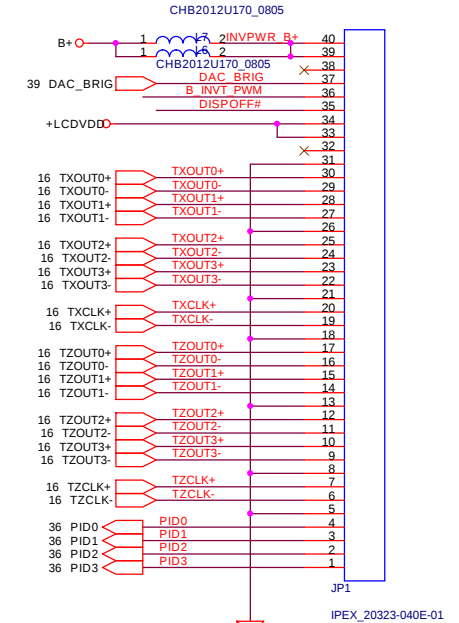
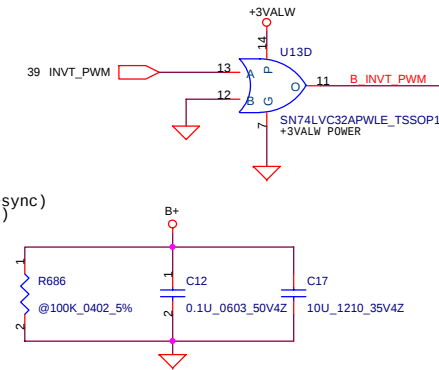
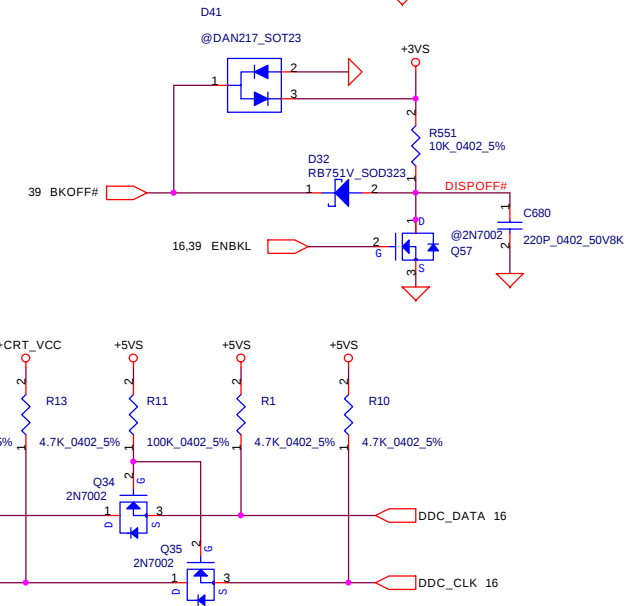
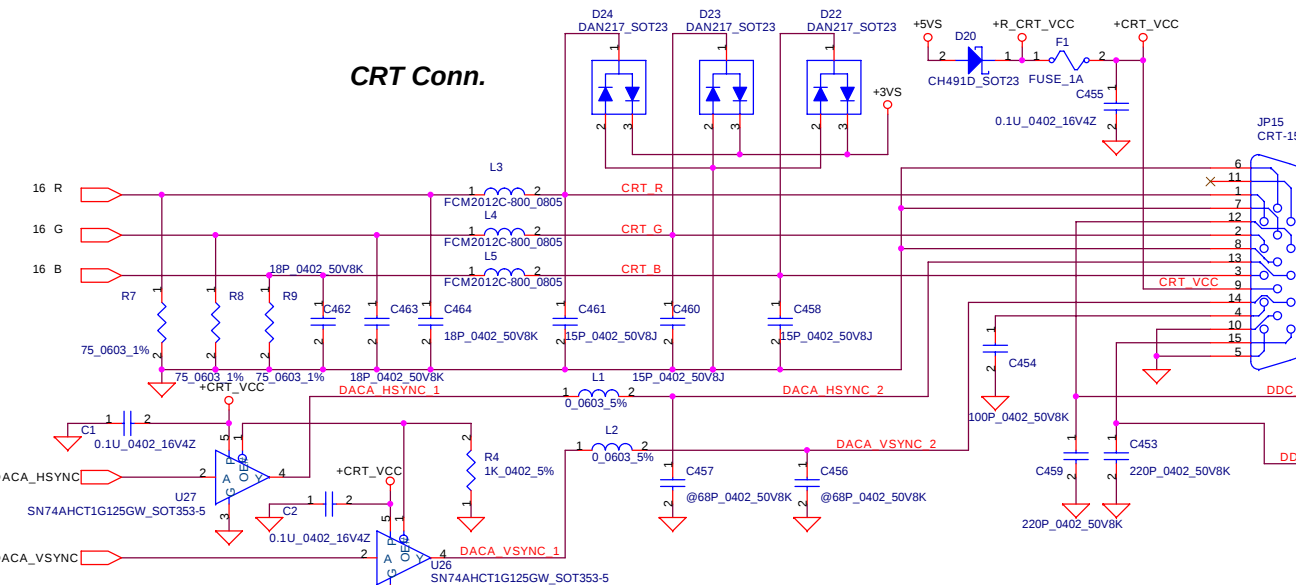
Compal Electronics, Inc.			
Title			
VGA DDR FOR CHANNEL B			
Size	Document Number		Rev
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CRT, TV-OUT & LVDS CONNECTOR

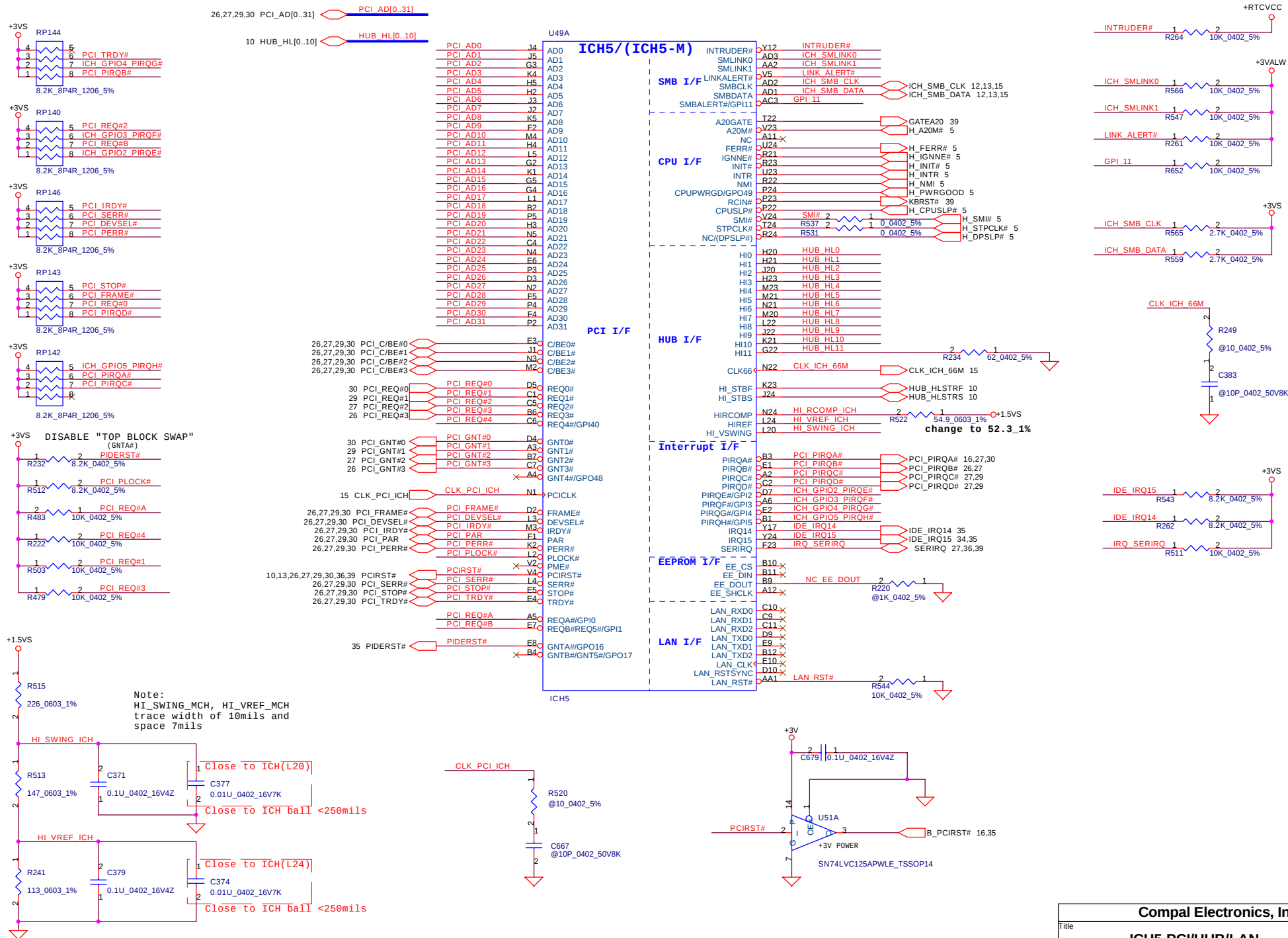
TV-OUT Conn.**LVDS Conn.****CRT Conn.**

Compal Electronics, Inc.

Title	CRT,TV-OUT & LVDS Connector
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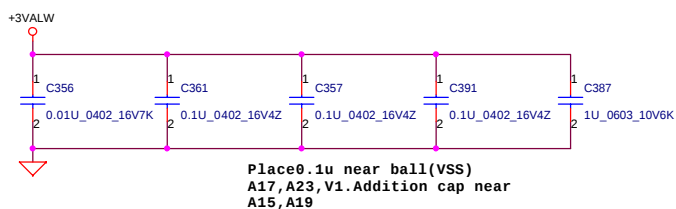
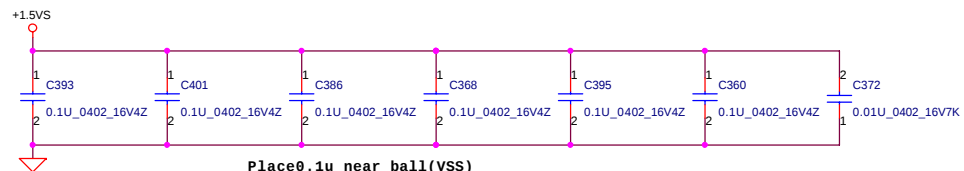
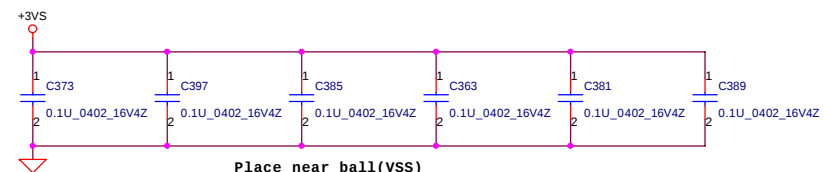
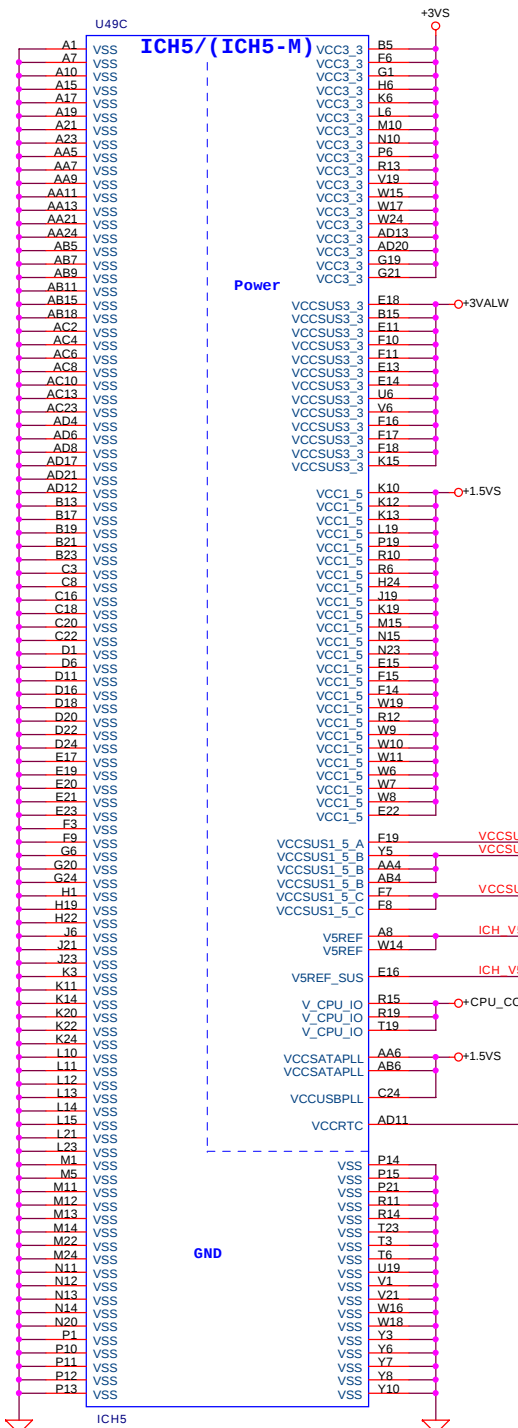
Size B	Document Number LA-2041	Rev 0.1
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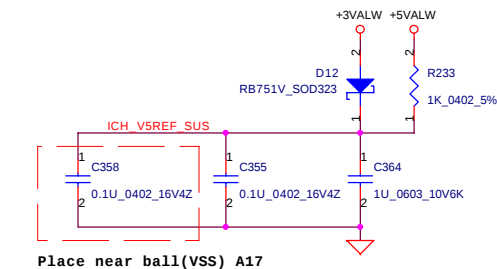
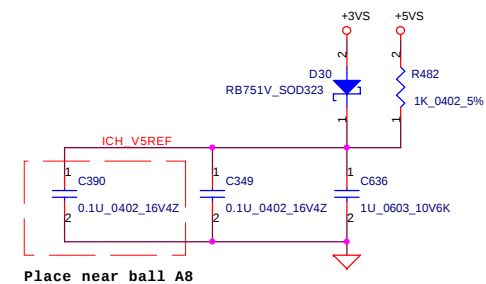
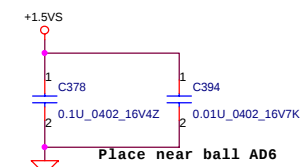
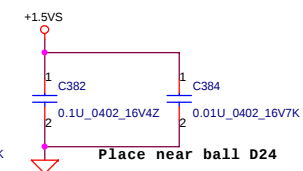
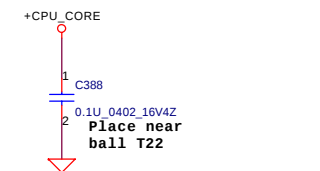
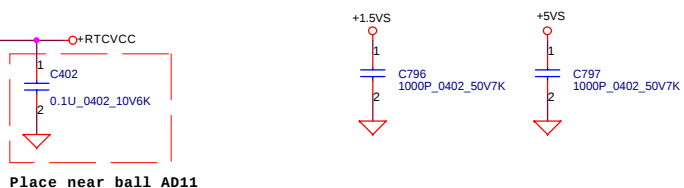
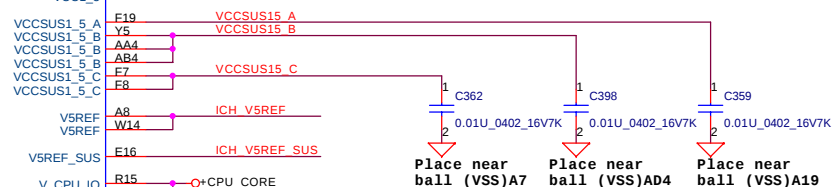


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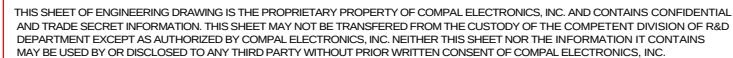
Compal Electronics, Inc.		
Title ICH5-PCI/HUB/LAN		
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Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11
(12474)page278



Compal Electronics, Inc.



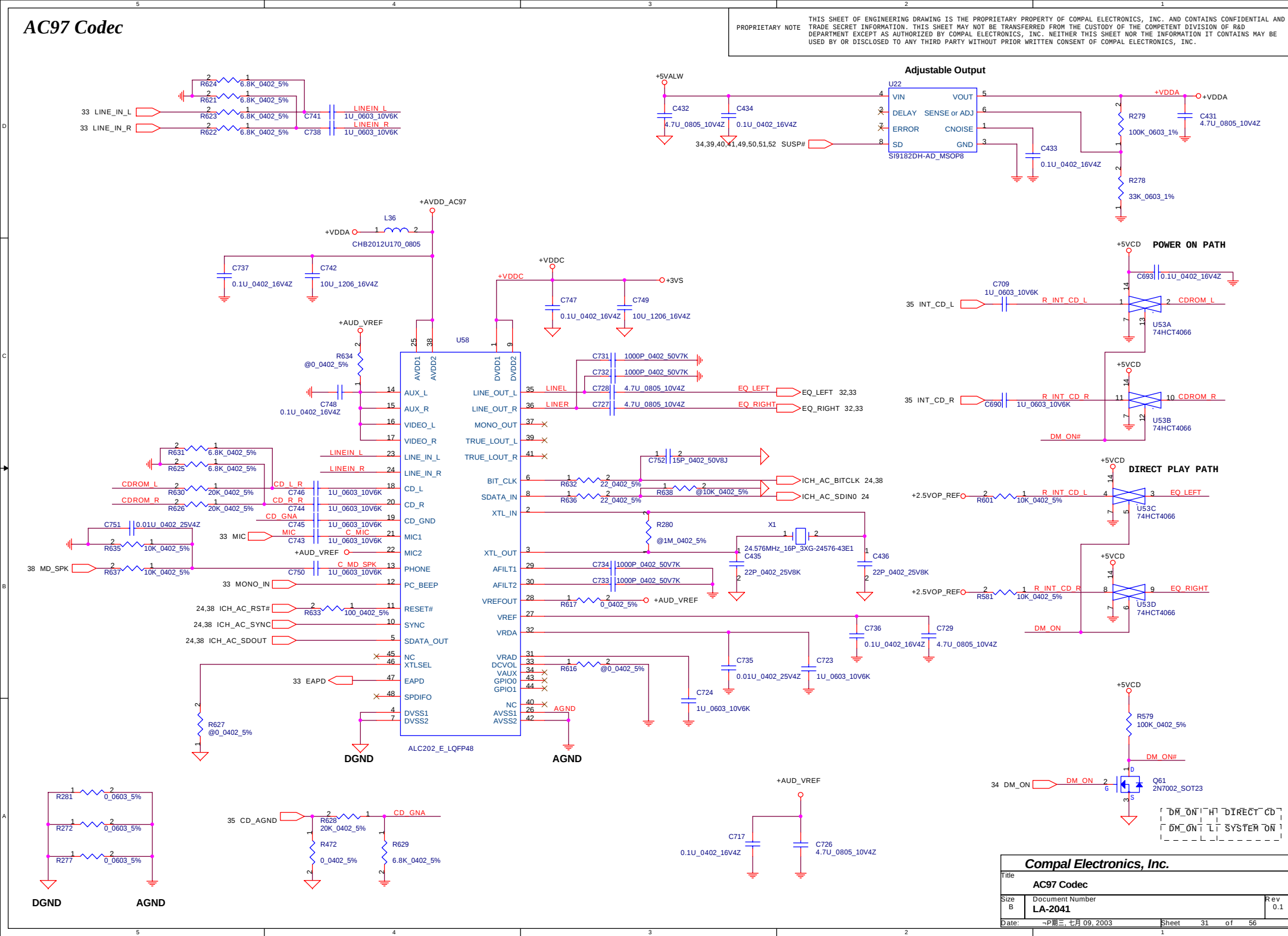
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Size	Document Number	Rev
	LA-2041	0.1

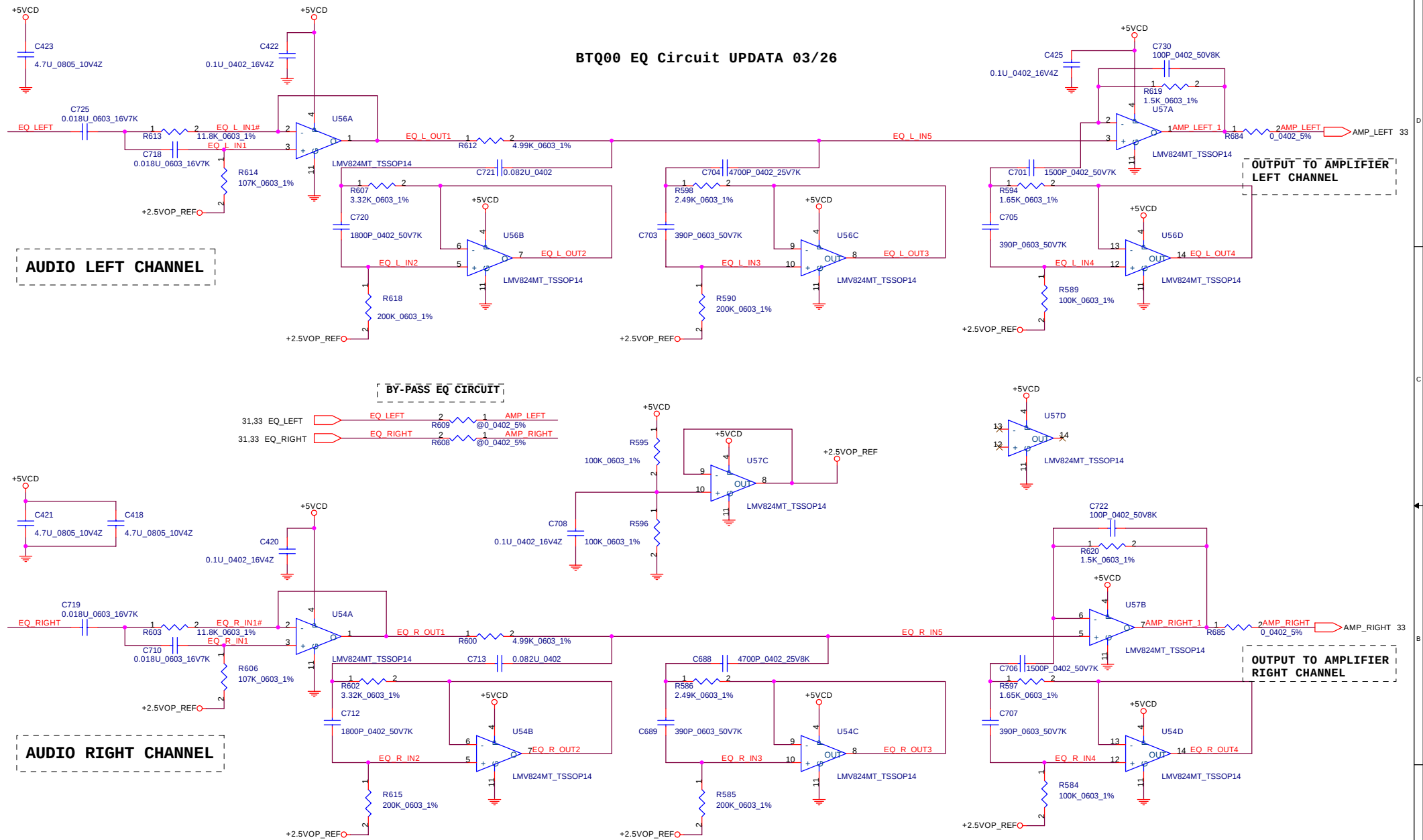
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AC97 Codec

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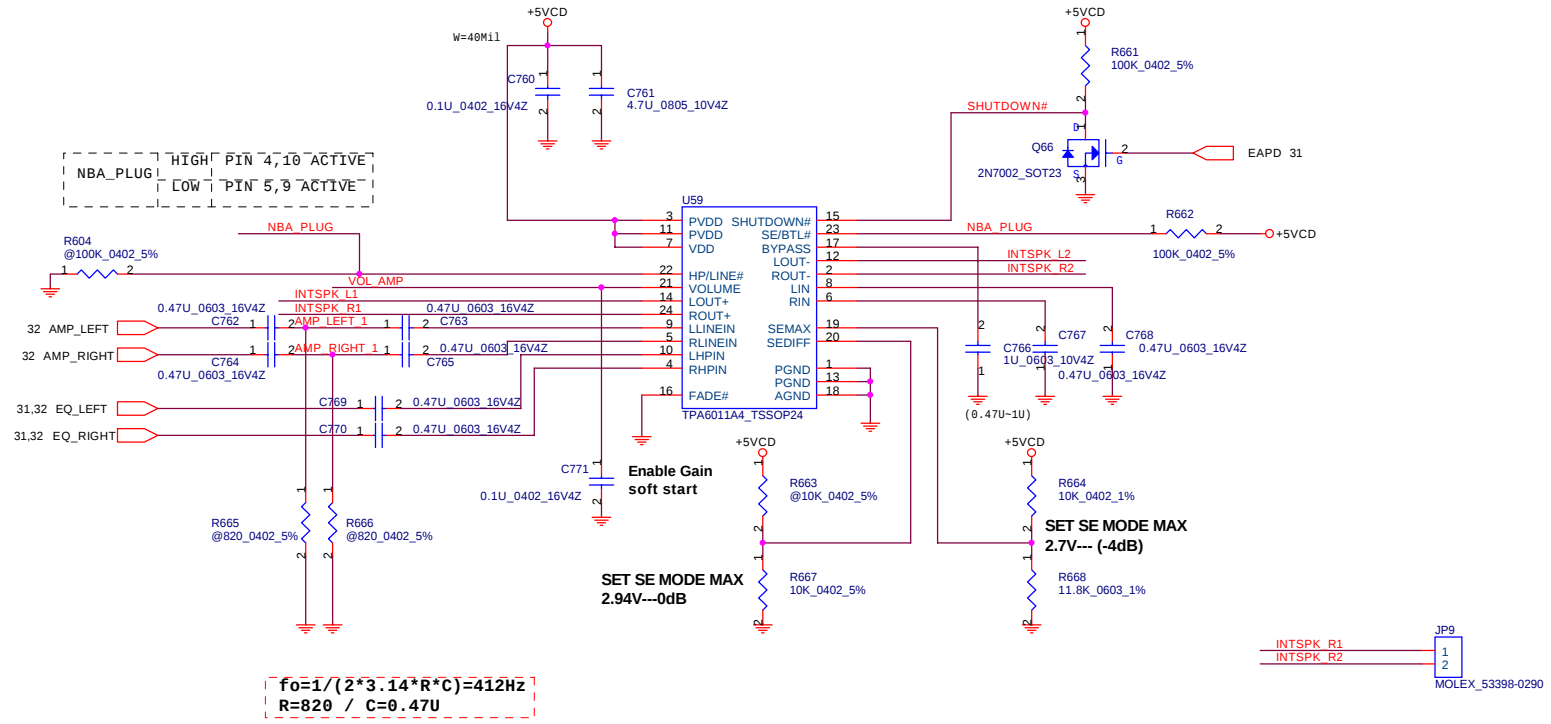
BTQ00 EQ Circuit UPDATA 03/26



Compal Electronics, Inc.		
Title	HAREWARE EQ	
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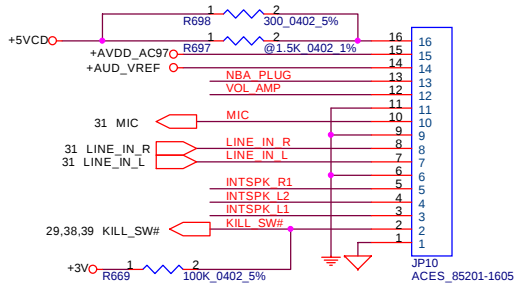
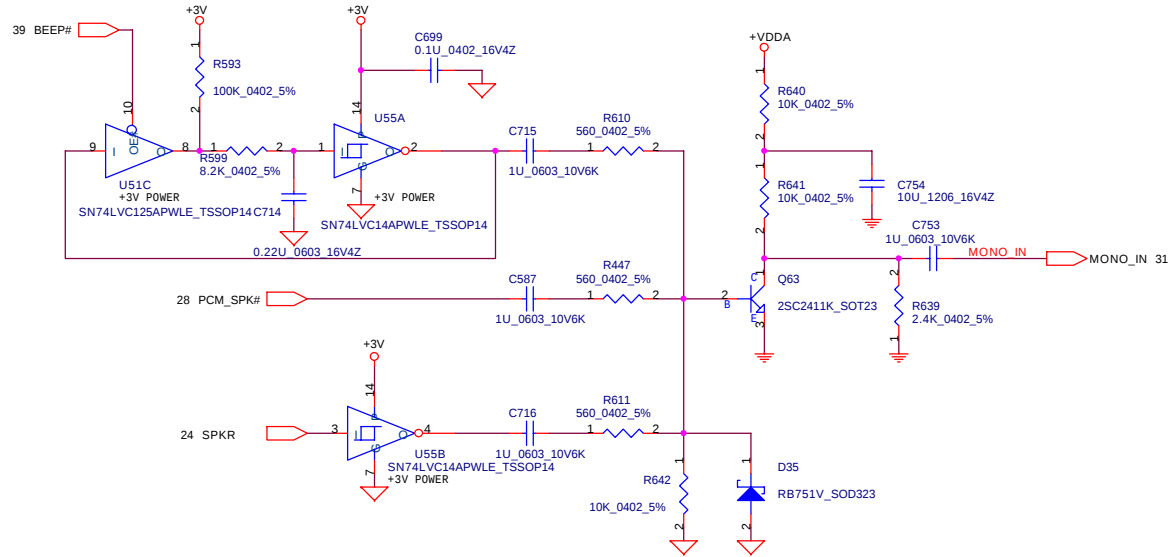
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Audio AMP



AUDIO Board Conn.

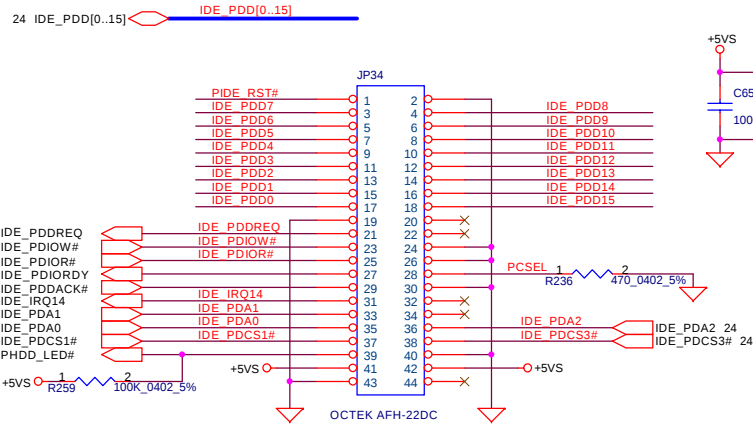
R697(1.5K)-----10dB
R698(300)-----14dB



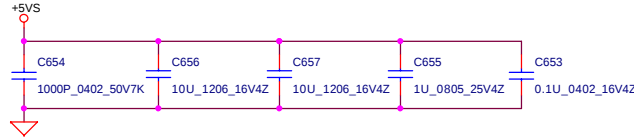
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Compal Electronics, Inc.			
Title			
AMP & Audio Jack			
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HDD CONNECTOR



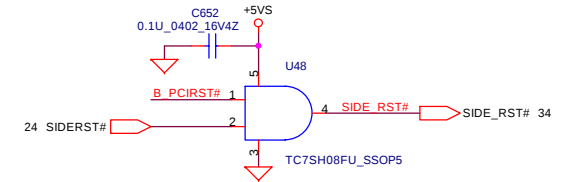
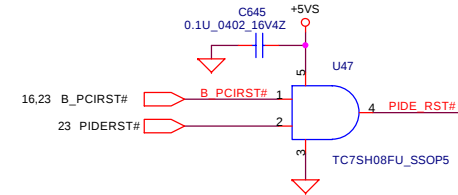
Place caps. near HDD
CONN.



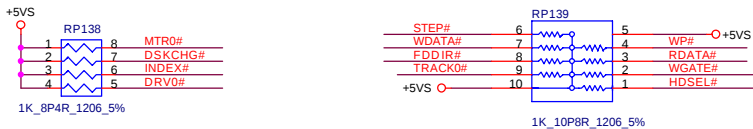
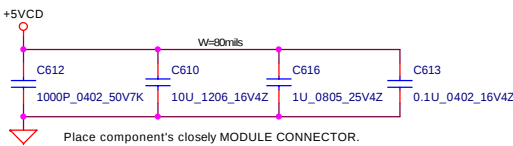
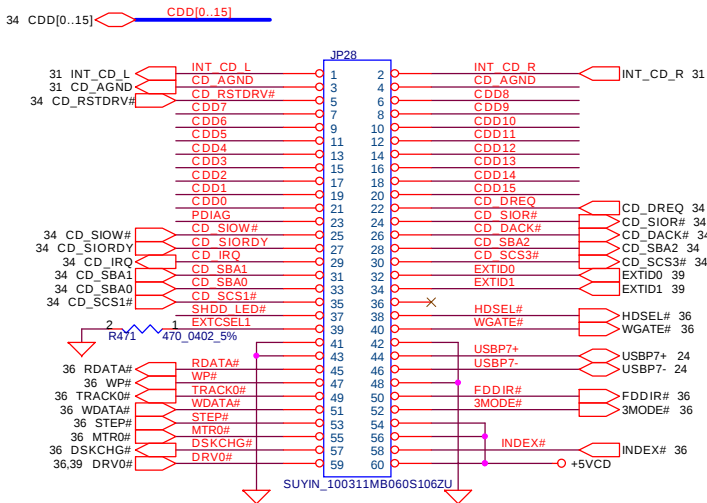
EXTID1	EXTID0	Module
0	0	CDROM
0	1	FDD
1	0	HDD
1	1	TV Tuner/No Module

EXTID3	EXTID2	Module
0	0	CDROM
0	1	FDD
1	0	HDD
1	1	TV Tuner/No Module

IDE,CD-ROM Module CONN.

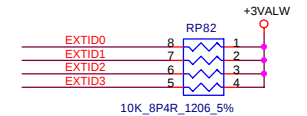
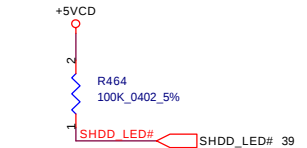
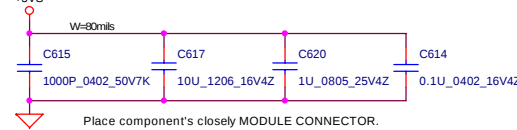
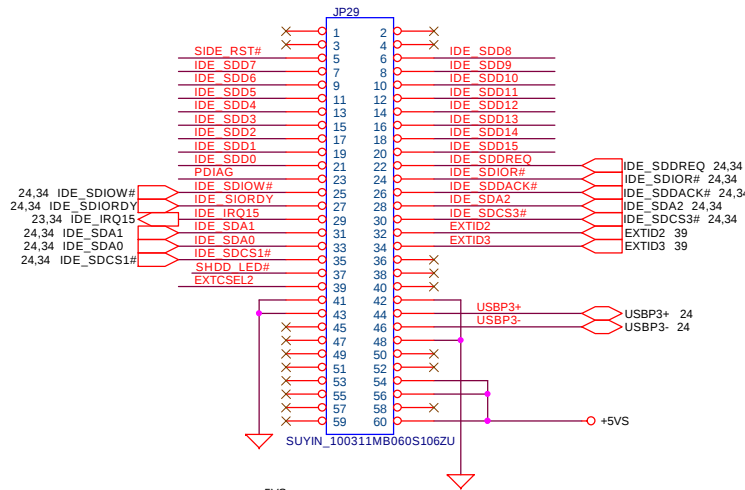


Main Module Conn. (Master)



2nd Module Conn. (Slave)

24,34 IDE_SDD[0..15] IDE_SDD[0..15]



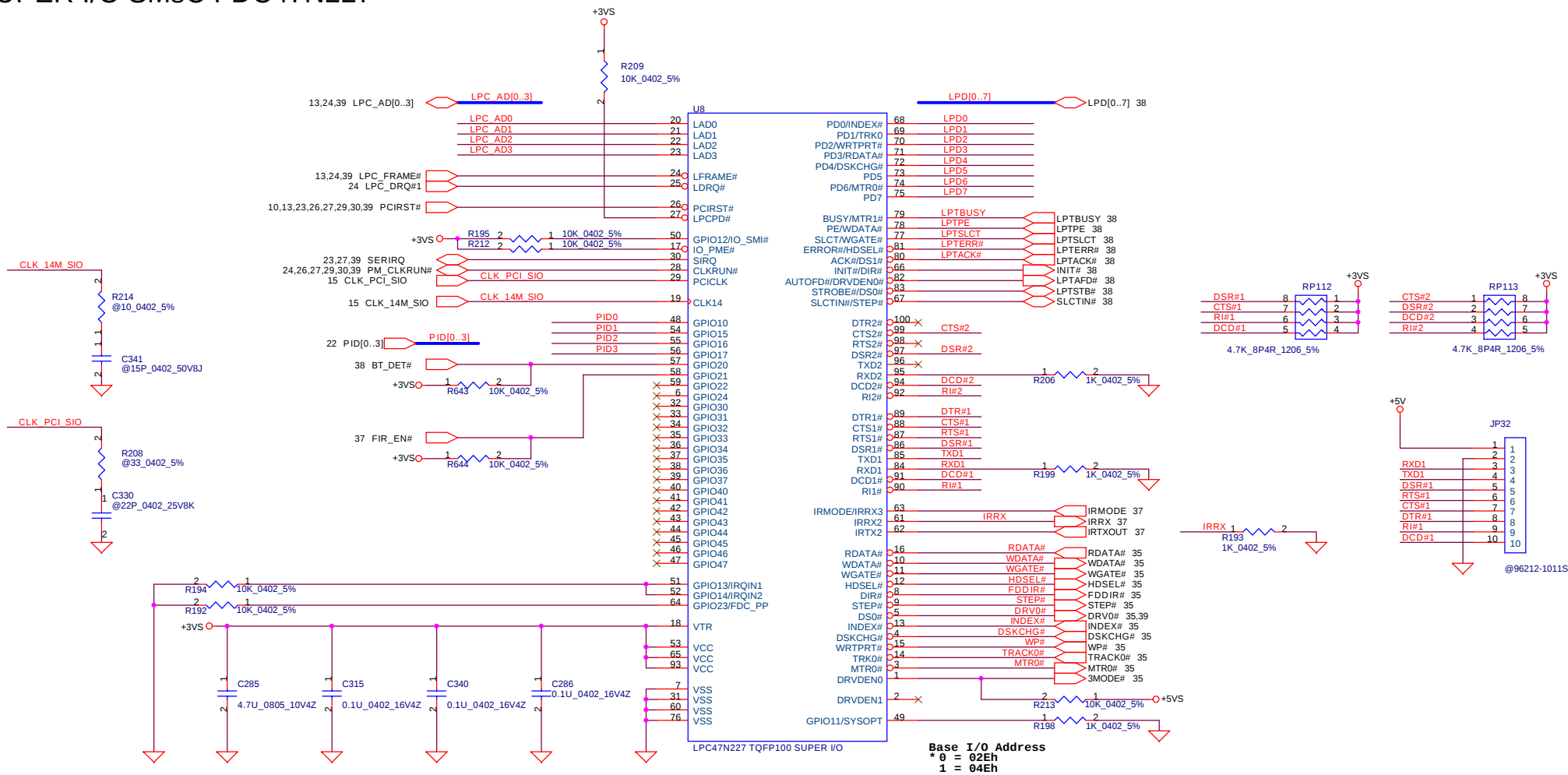
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IDE/ FDD MODULE CONN.

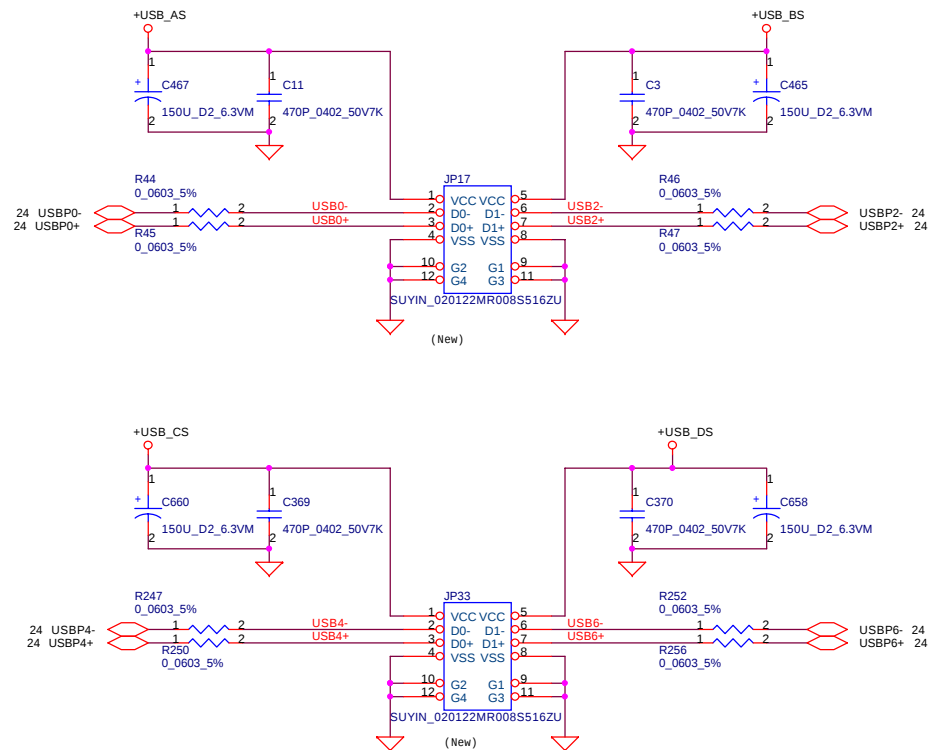
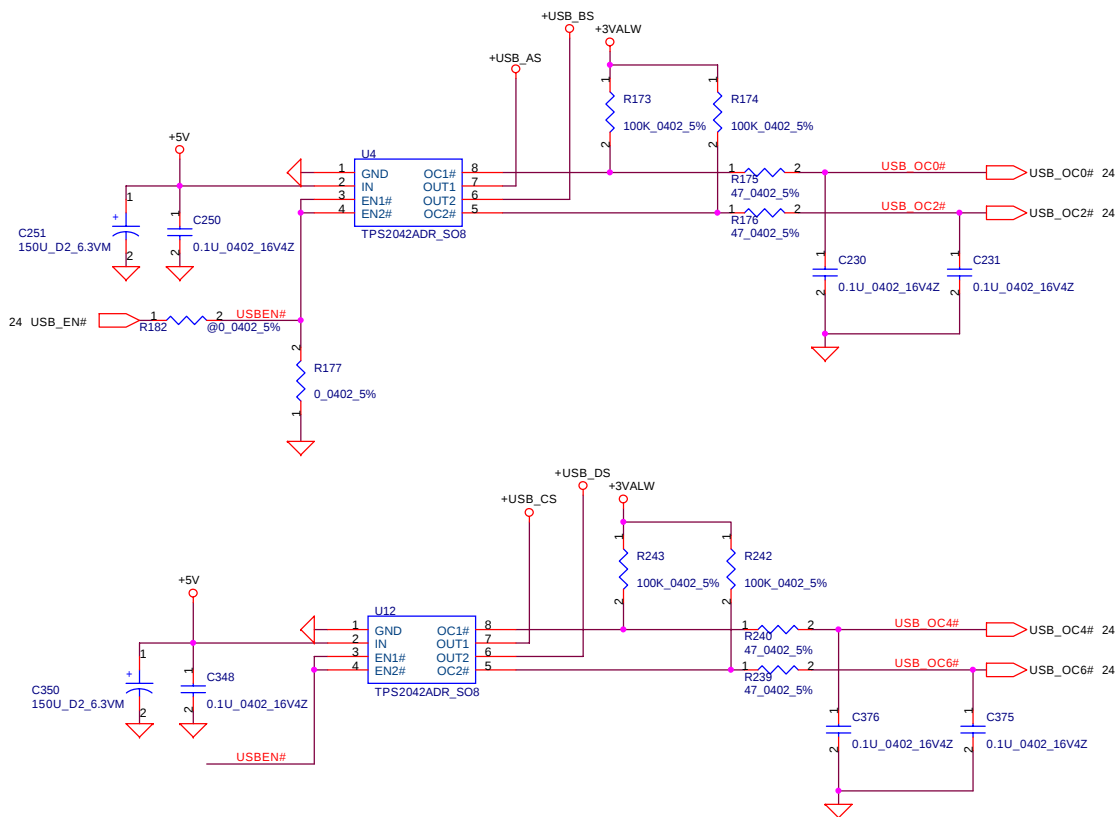
Size	Document Number	Rev
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SUPER I/O SMC FDC47N227

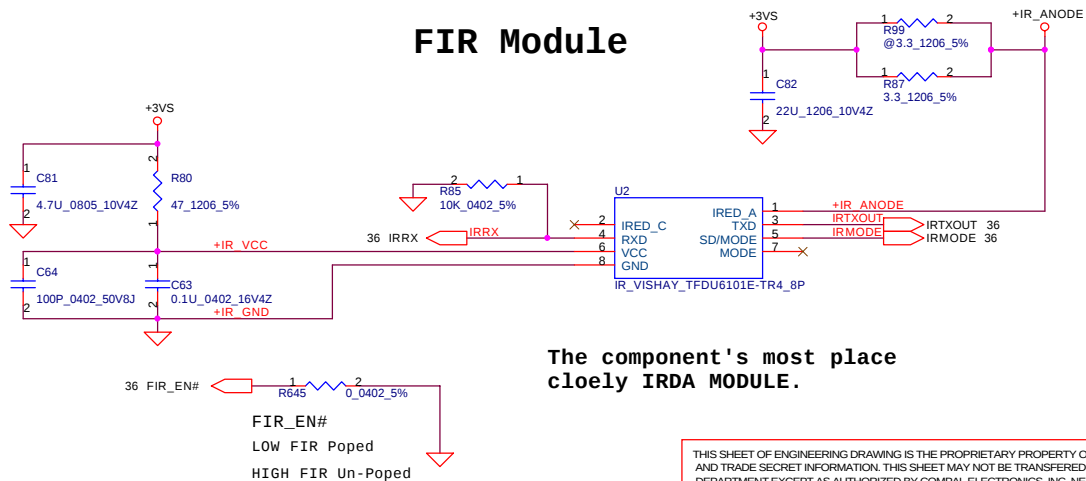


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SUPER I/O			
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FIR Module



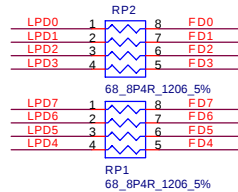
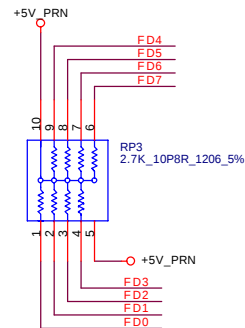
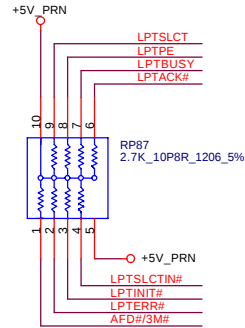
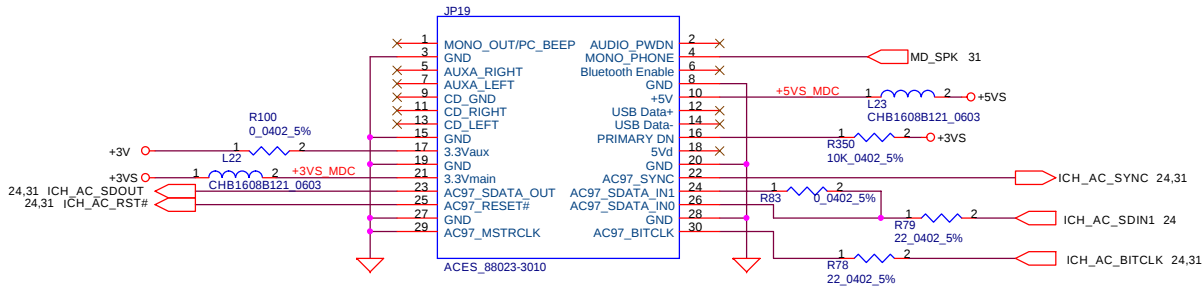
The component's most place
cloely IRDA MODULE.

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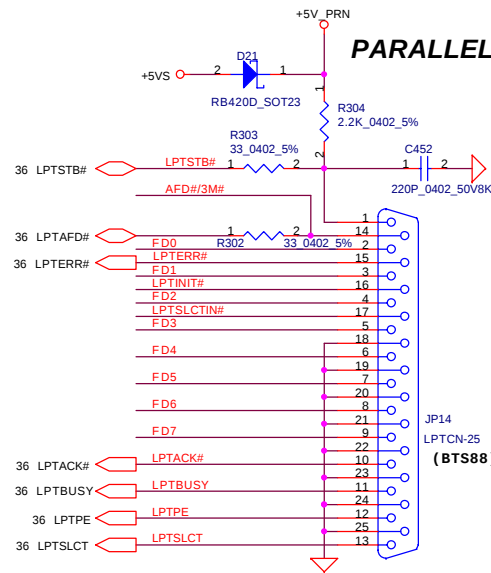
Compal Electronics, Inc.

Title			
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Size B	Document Number	Rev	
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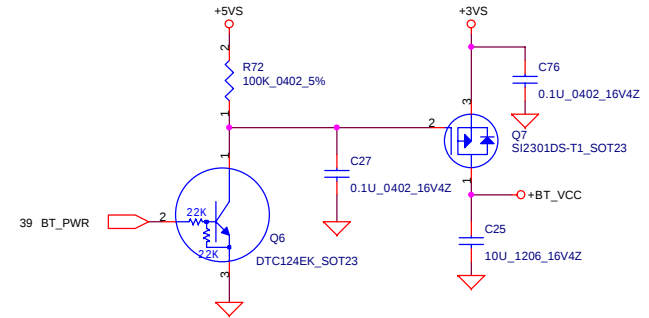
MDC CONN.



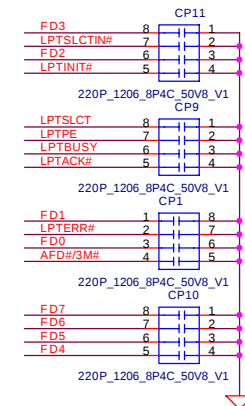
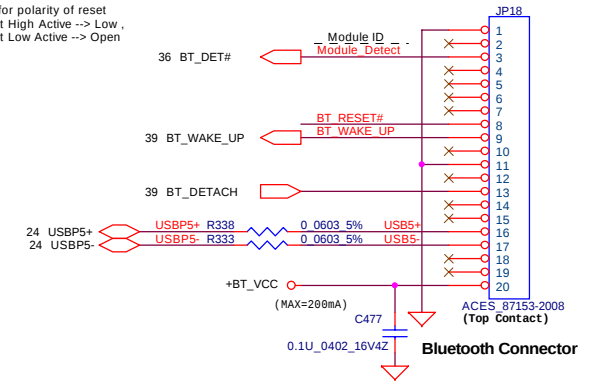
PARALLEL PORT



BlueTooth Interface



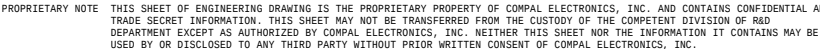
Module ID
Indication for polarity of reset
Reset input High Active --> Low
Reset input Low Active --> Open

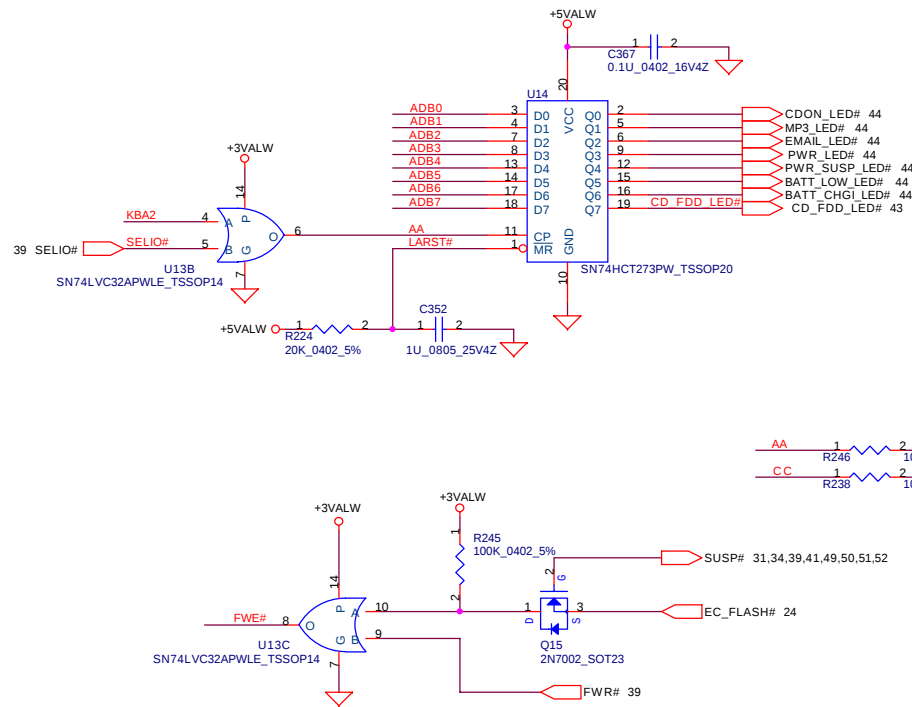


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Title			
PARALLEL/MDC PORT			
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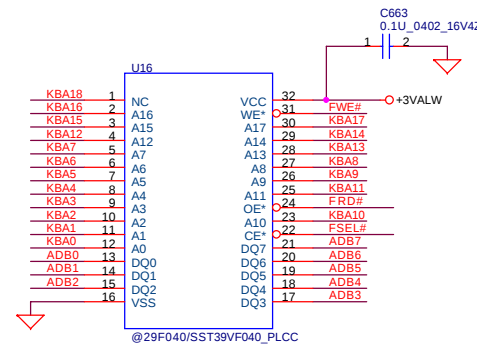
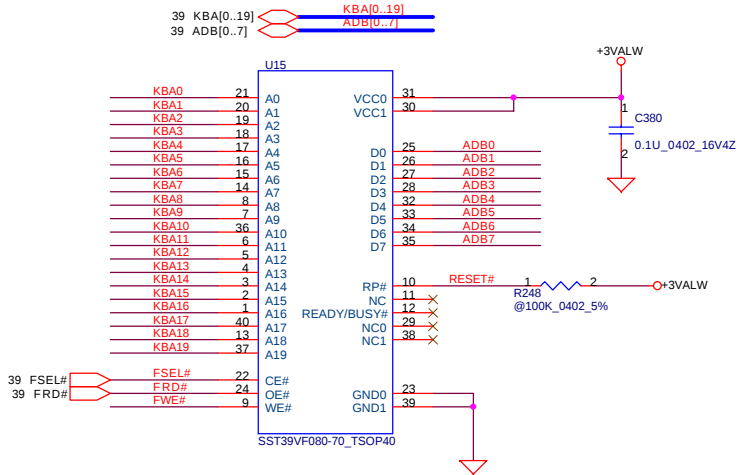
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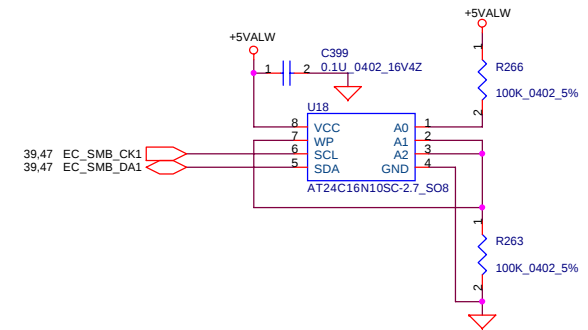
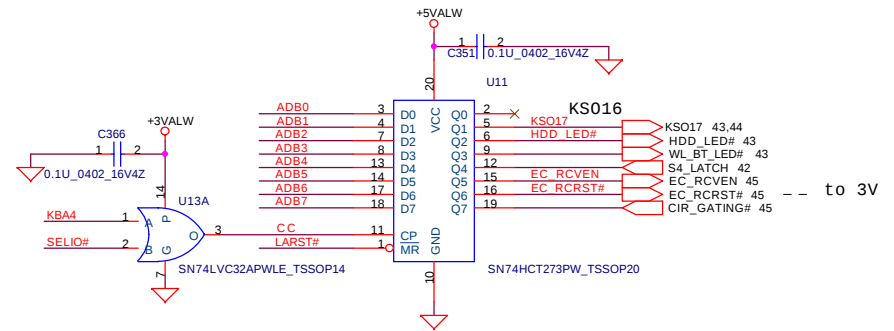


1MB Flash ROM

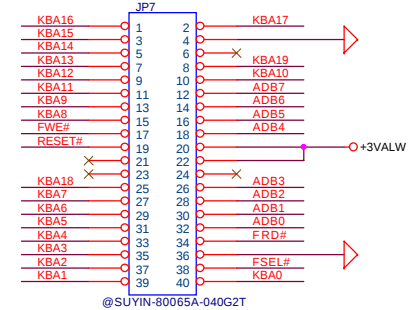
512KB Flash ROM



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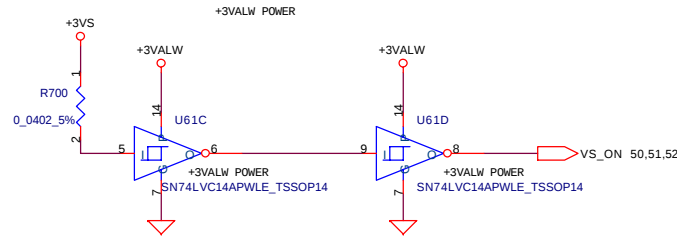
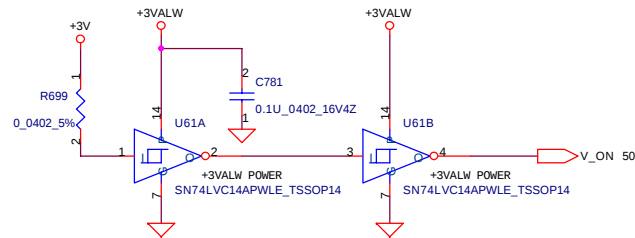
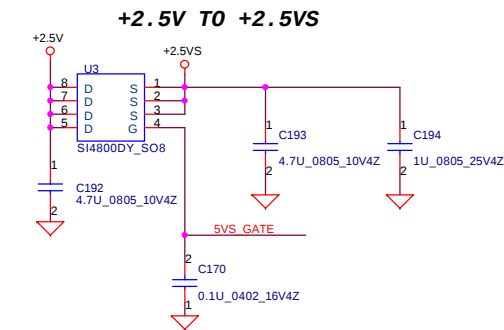
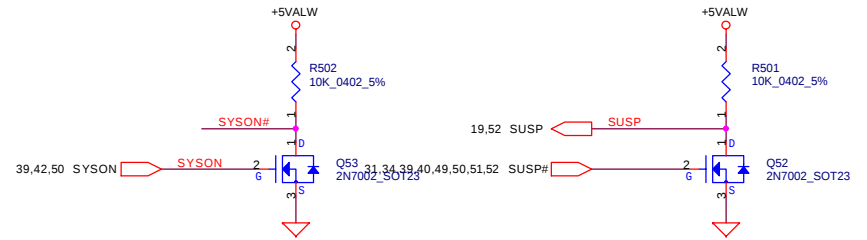
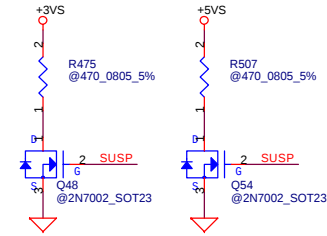
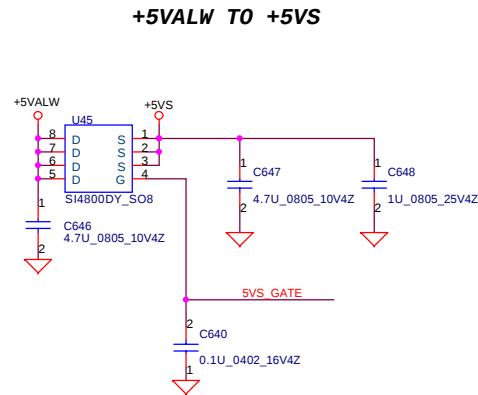
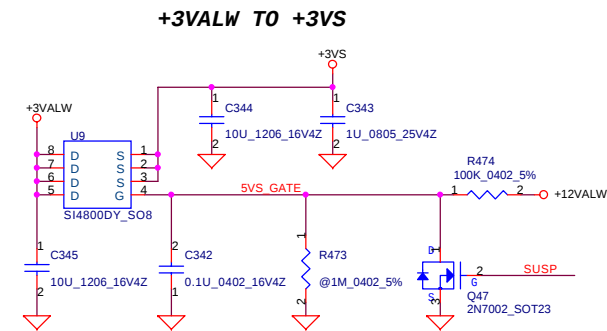
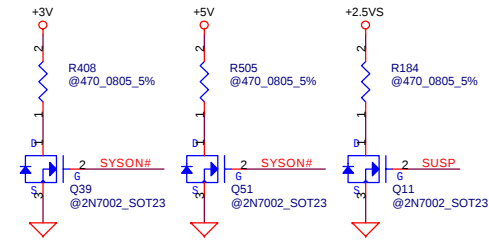
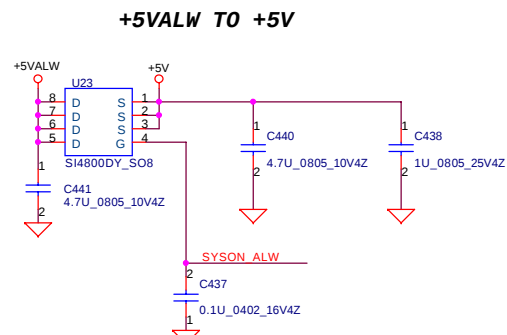
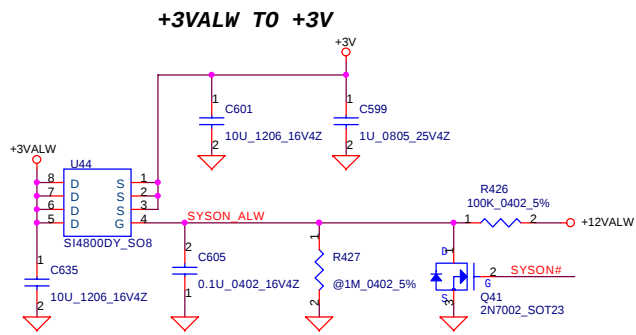


Flash ROM Socket Conn.



Compal Electronics, Inc.

Title			
BIOS & EXT. I/O PORT			
Size	Document Number	Rev	
B	LA-2041	0.1	
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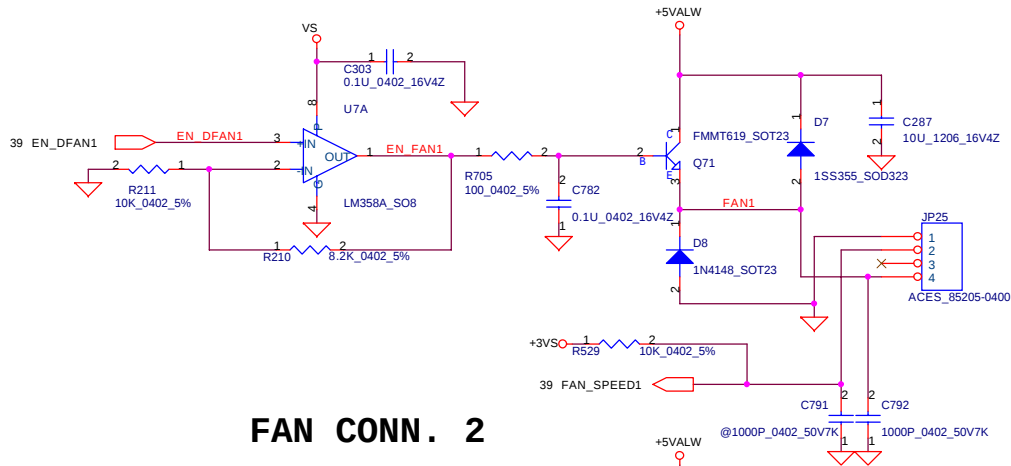


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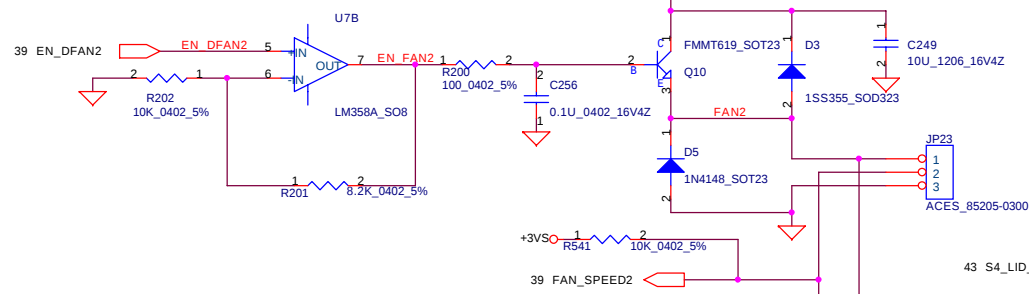
Title		
POWER CONTROL CKT		
Size B	Document Number	Rev
	LA-2041	0.1
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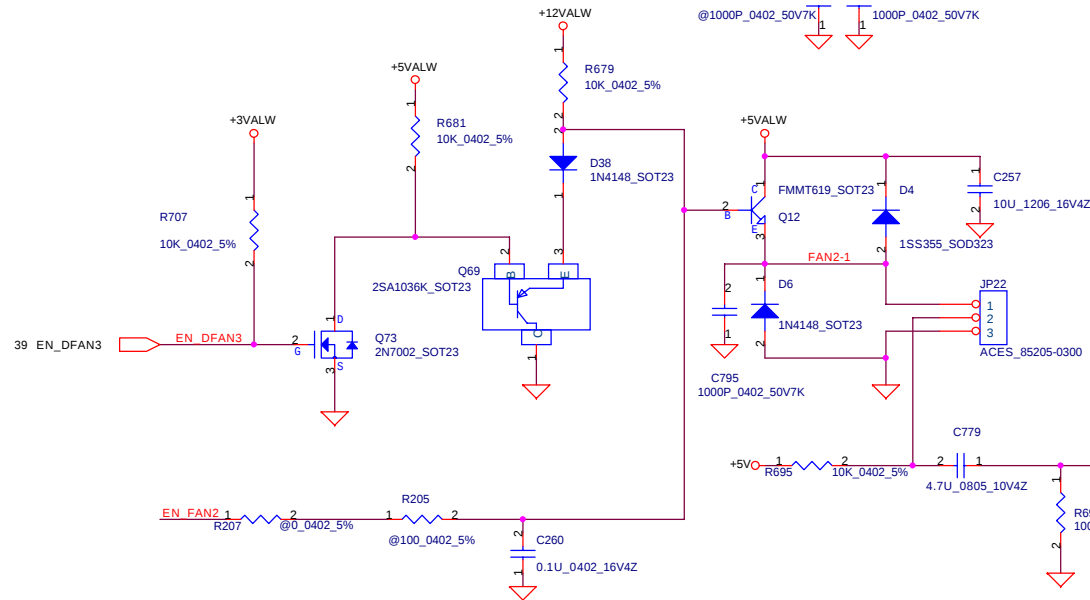
FAN CONN. 1



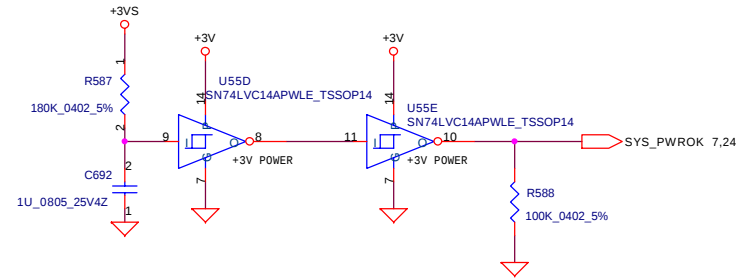
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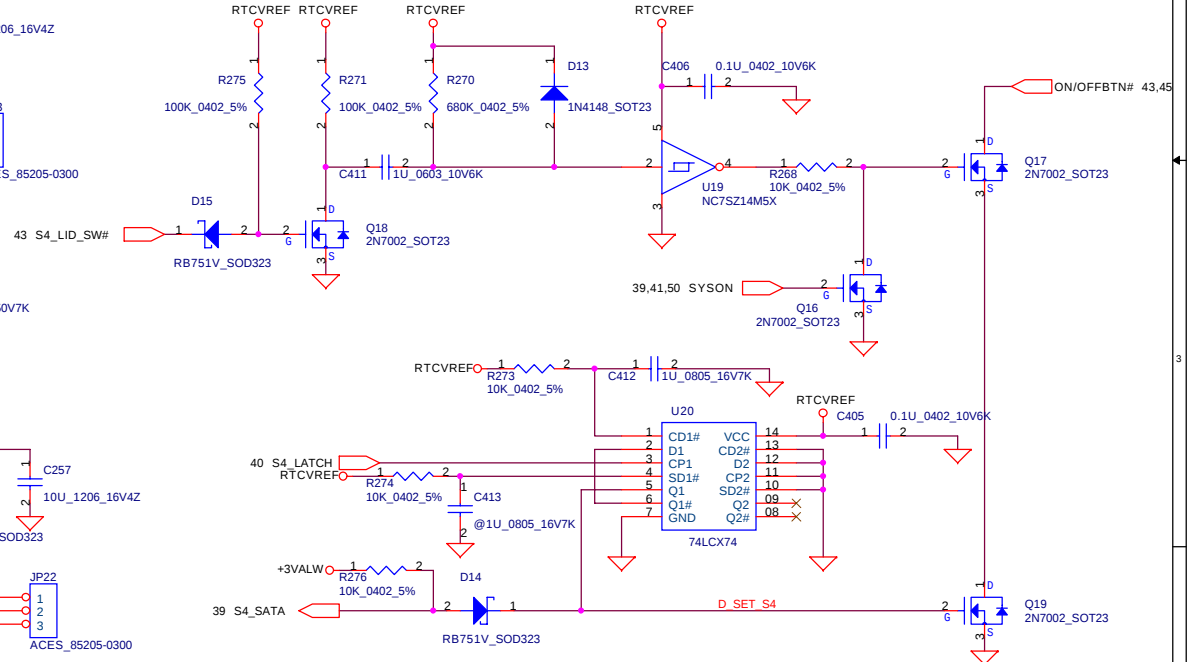
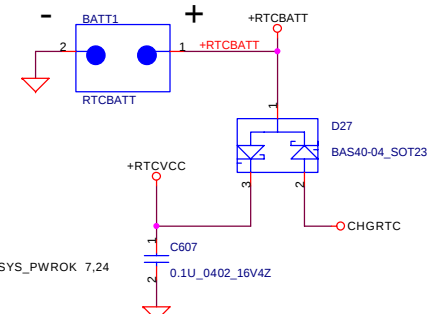
FAN CONN. 3



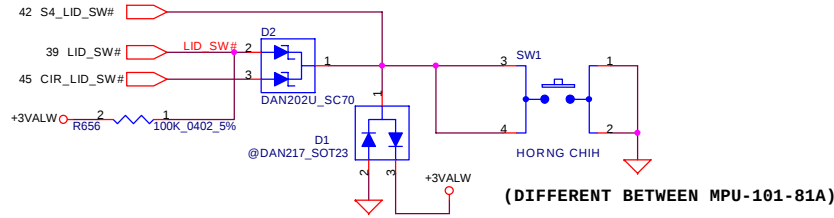
Power ON Circuit



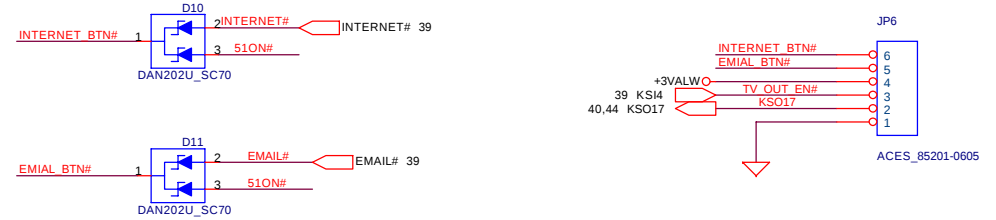
RTC Battery



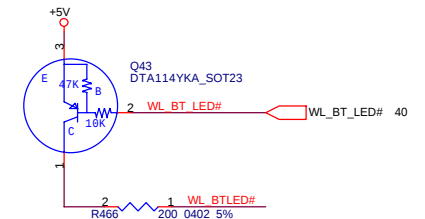
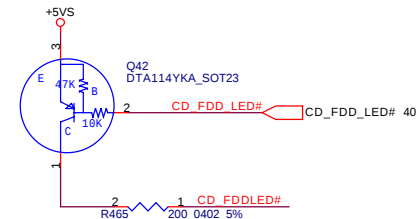
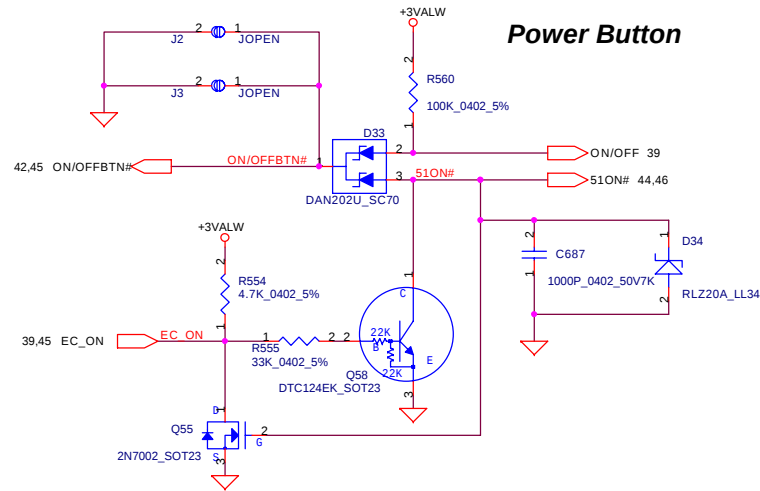
LID Switch



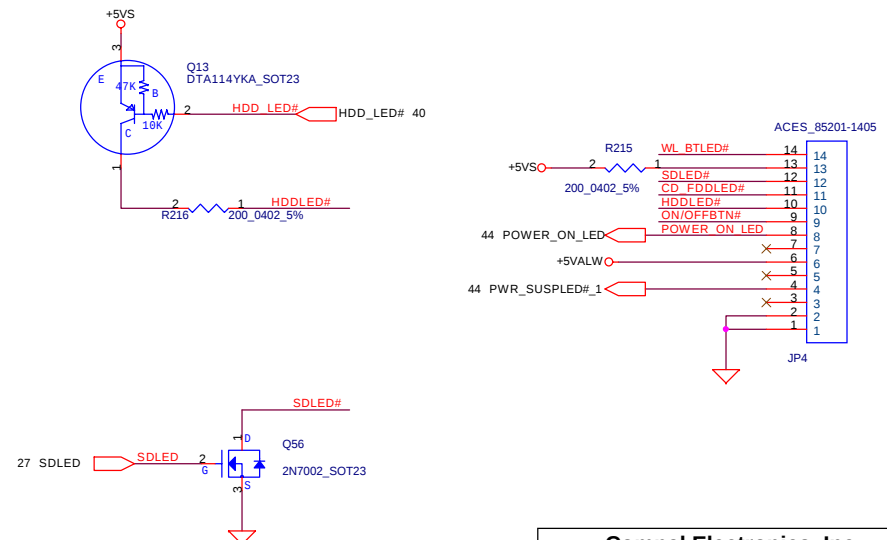
Button FPC Conn.



Power Button



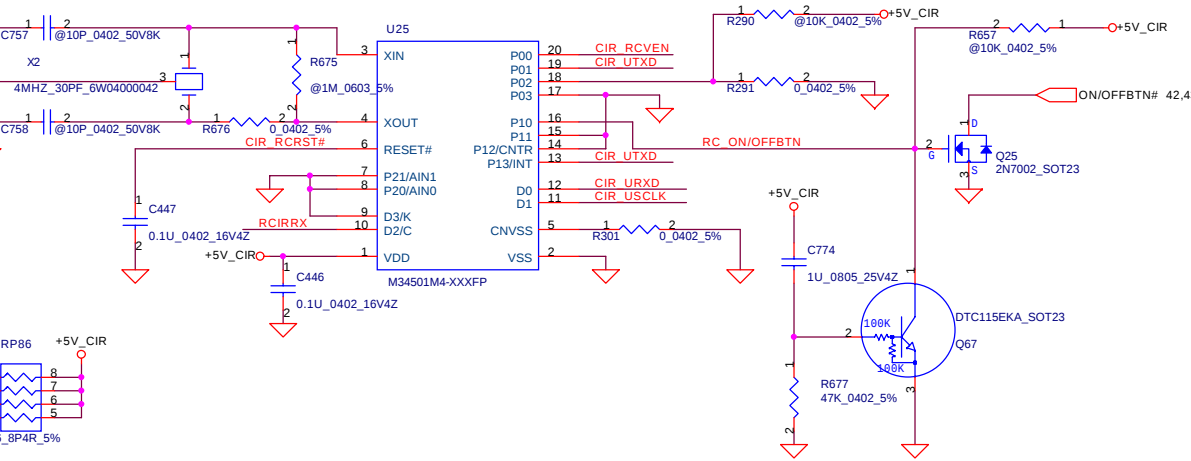
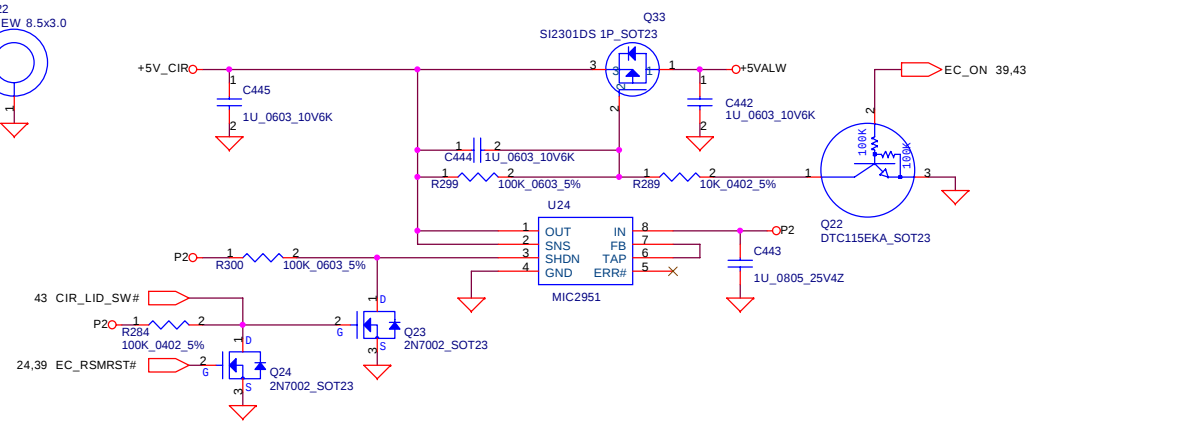
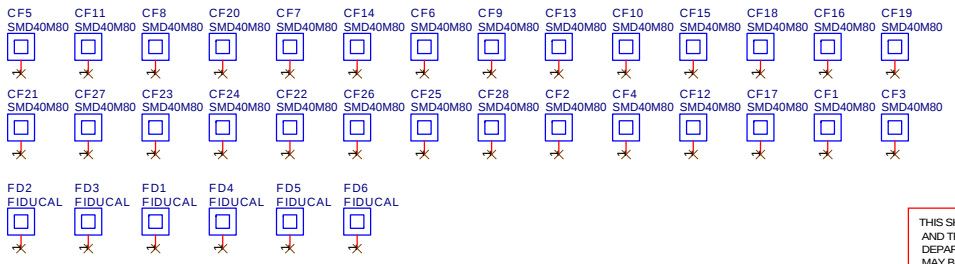
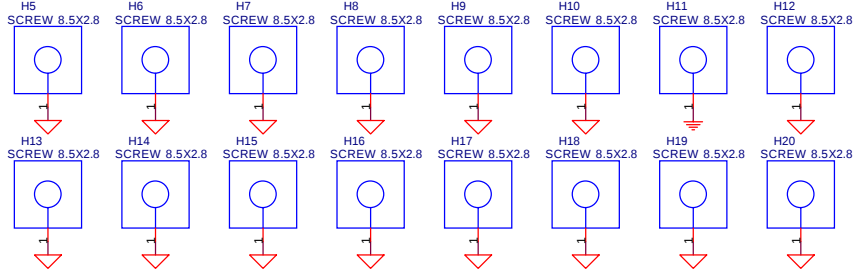
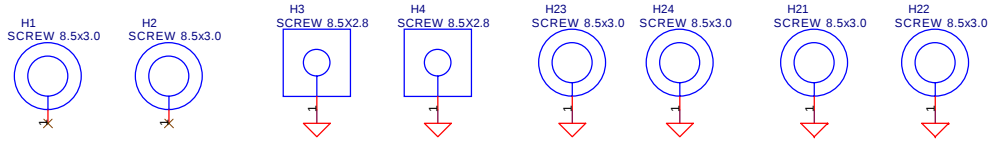
Power FPC Conn.



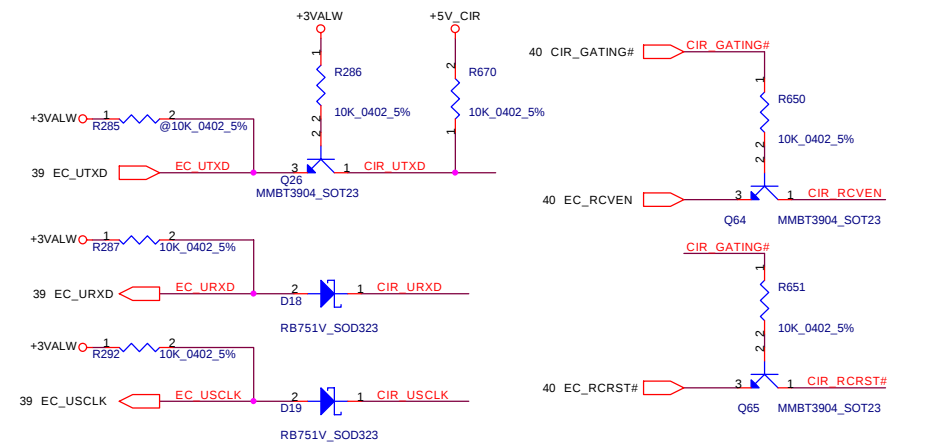
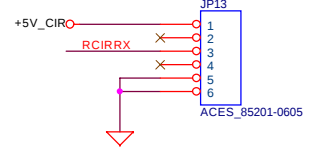
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Compal Electronics, Inc.

Title		
Switches & Connectors		
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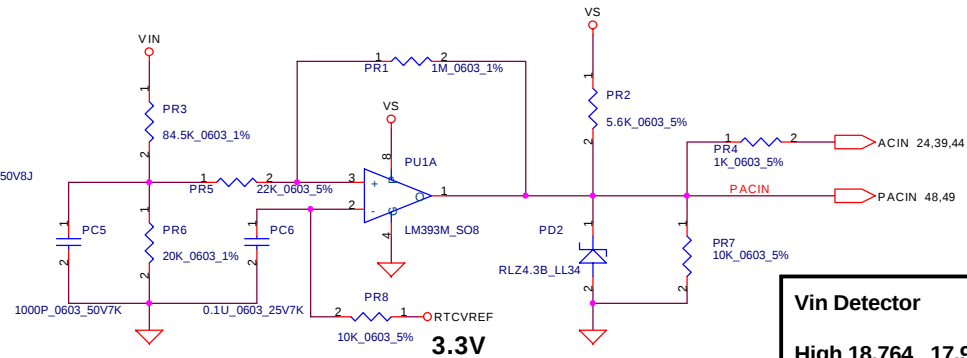
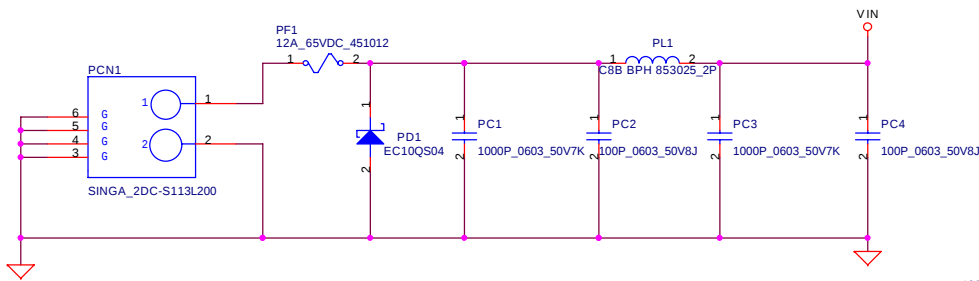


CIR Reciever Board Conn.



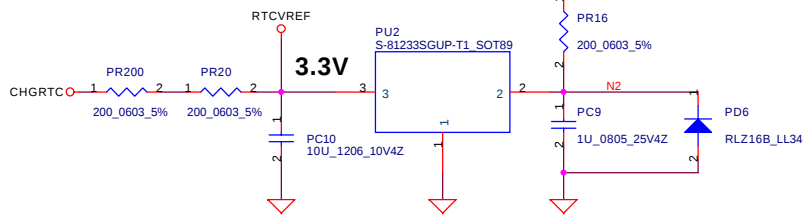
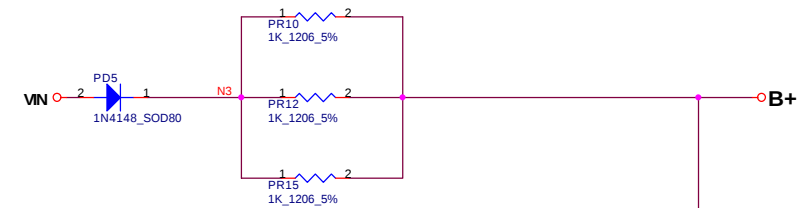
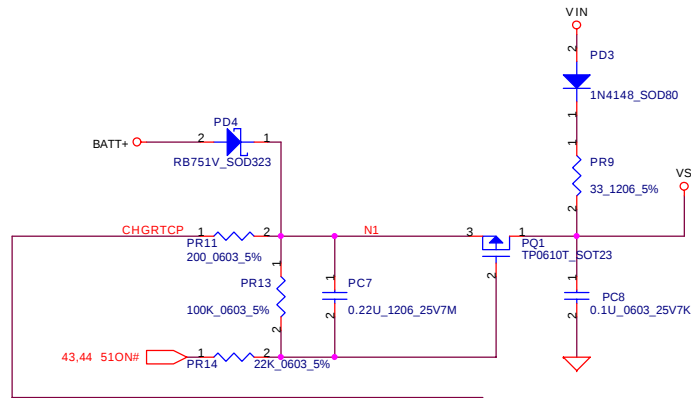
Compal Electronics, Inc.		
Title	CIR & Screws	
Size	Document Number	Rev
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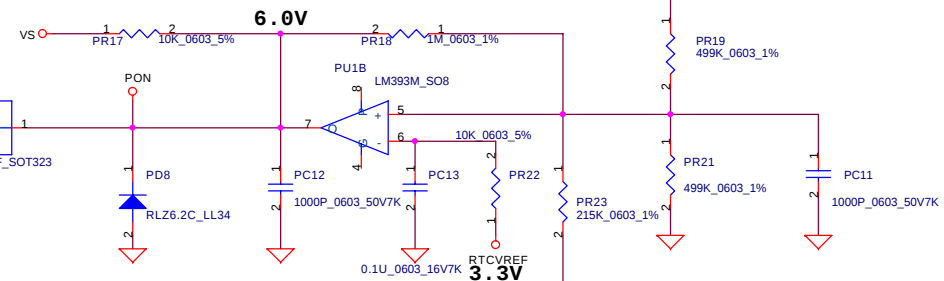


Vin Detector

High 18.764 17.901 17.063
Low 17.745 16.903 16.038

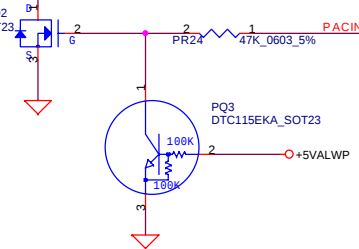
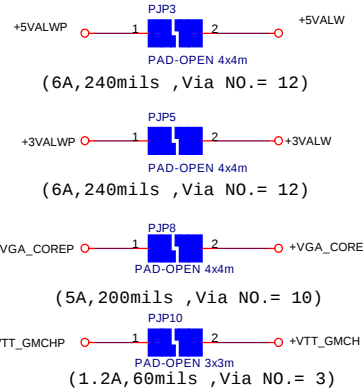
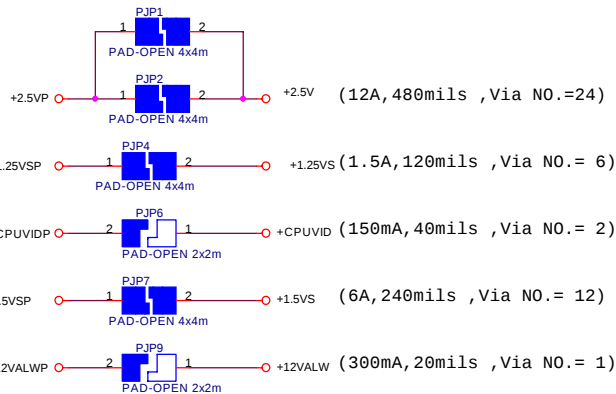


47.49 MAINPWON
48 ACON



Precharge detector

15.34 15.90 16.48
13.13 13.71 14.20

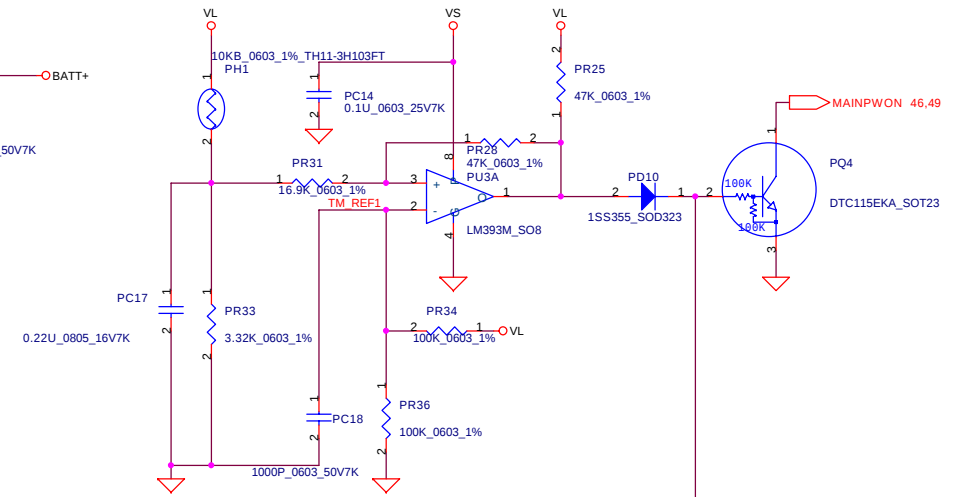


Compal Electronics, Inc.

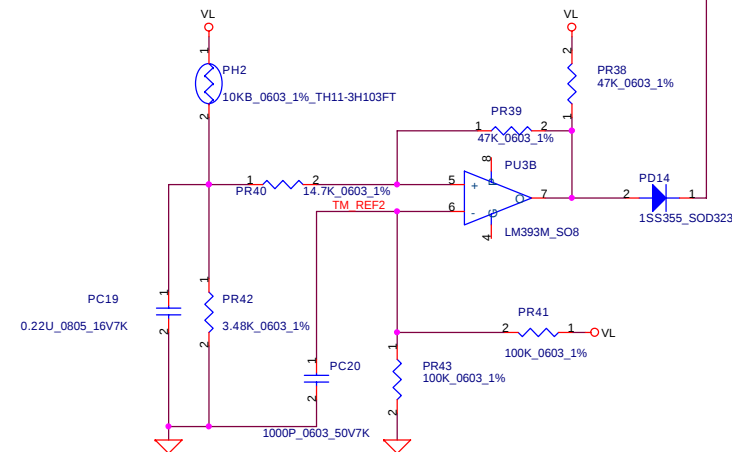
Title		
DCIN & DETECTOR		
Size	Document Number	Rev
	LA-2041	0.1
Date:	-P 星期三, 七月 09, 2003	Sheet 46 of 56

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PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C

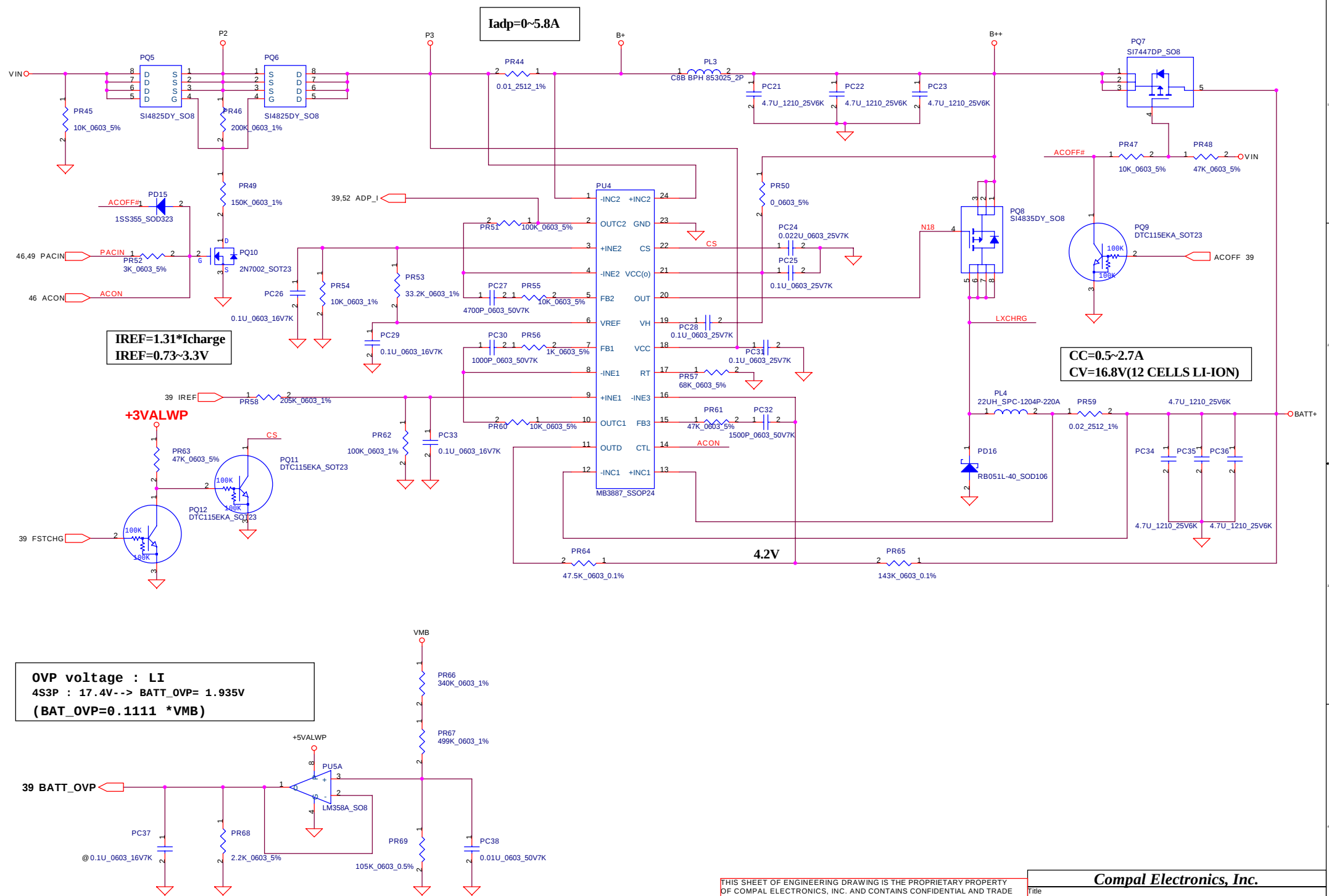


Compal Electronics, Inc.

BATTERY CONN /OTP

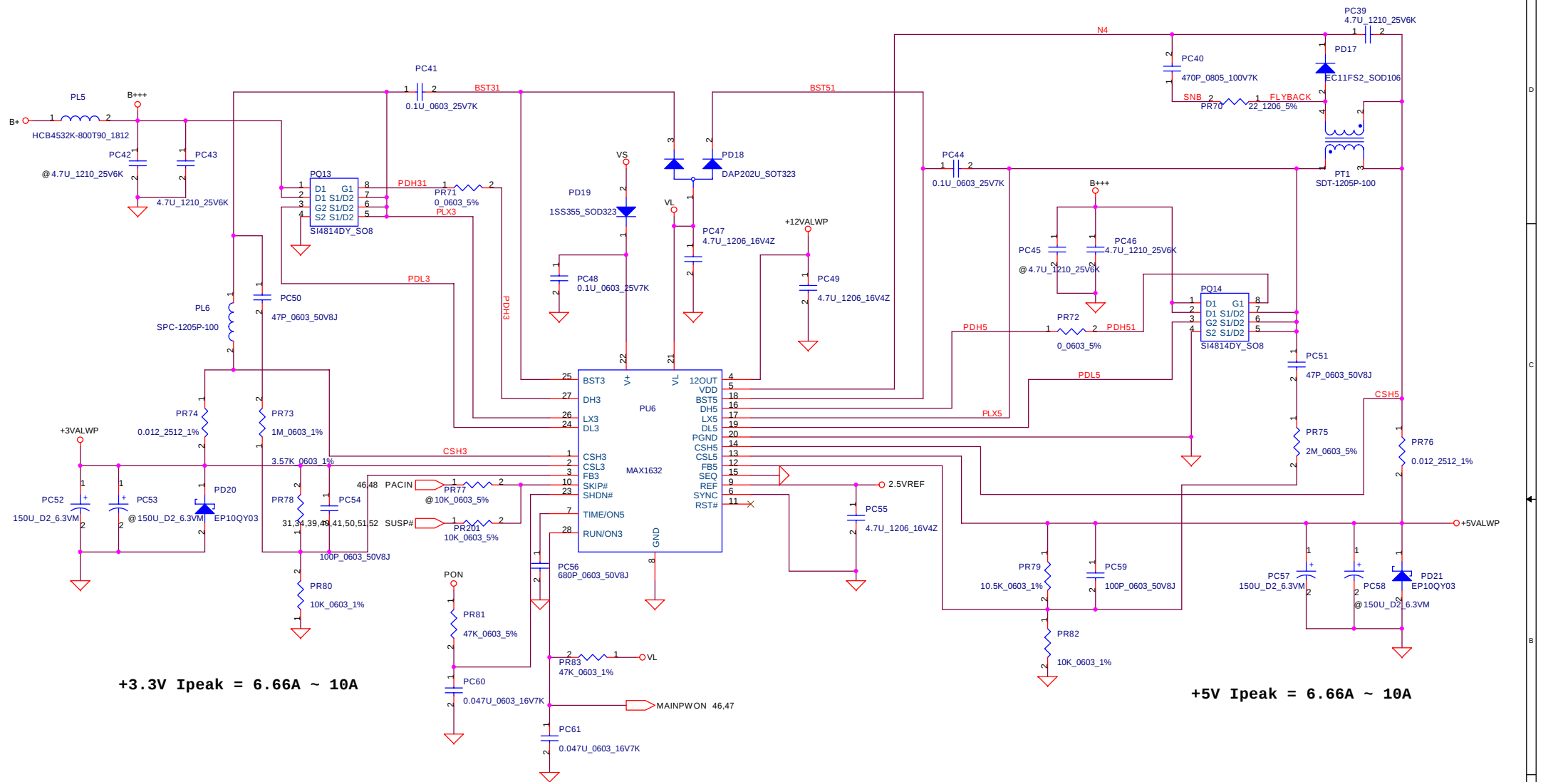
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Compal Electronics, Inc.			
CHARGER			
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+3.3V Ipeak = 6.66A ~ 10A

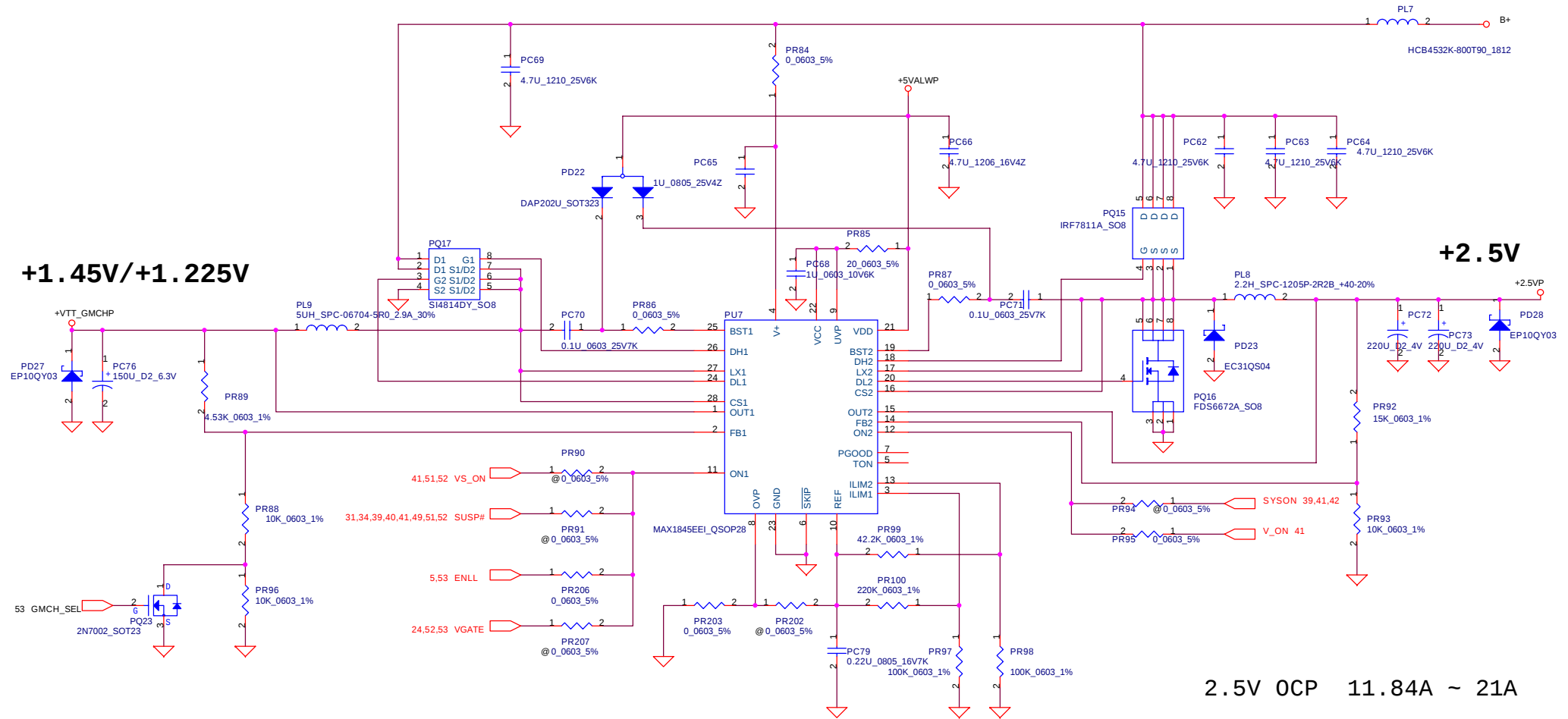
+5V Ipeak = 6.66A ~ 10A

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Compal Electronics, Inc.		
Title		
5V/3.3V/12V		
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+2.5V/+VTT_GMCHP

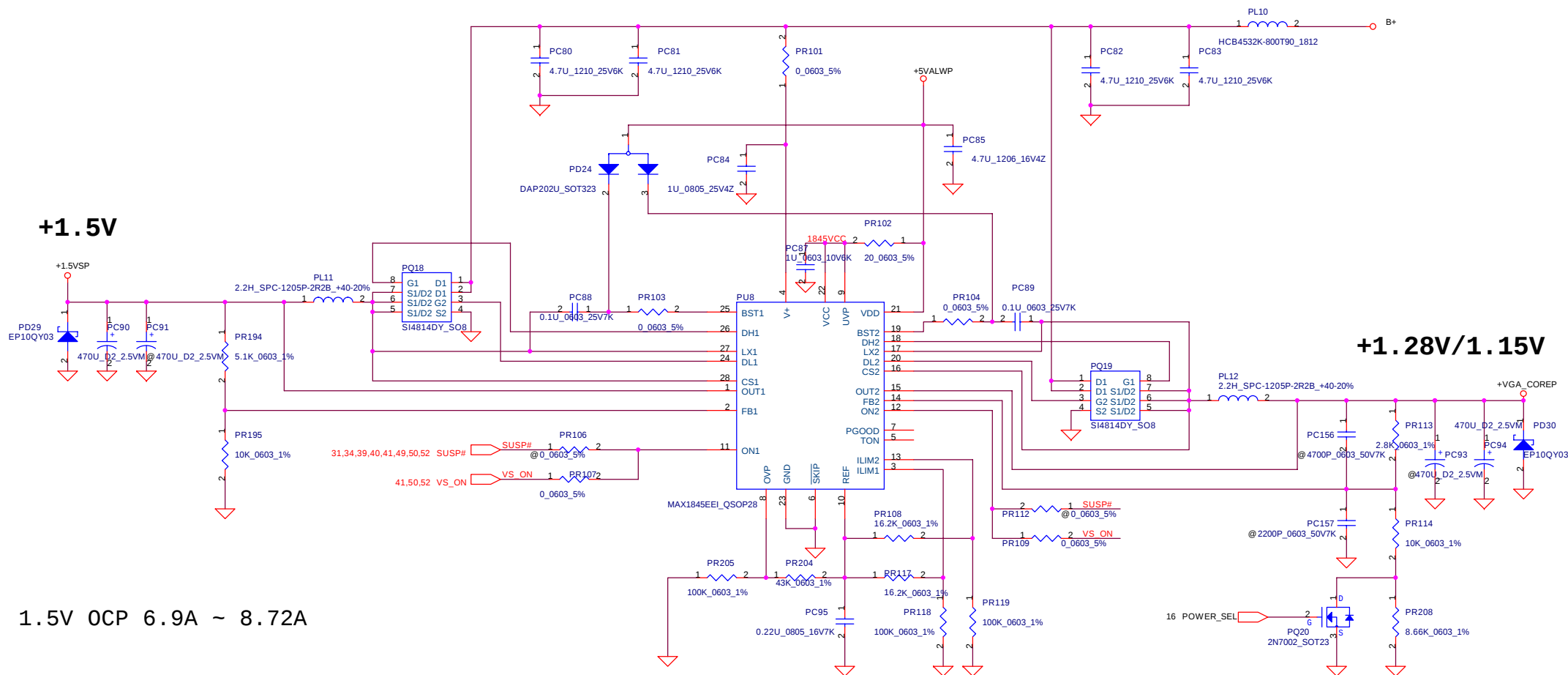
+1.45V/+1.225V



GMCH_SEL=0	PRESCOTT	VTT_GMCH=1.225V	OCP 1.92A ~ 3.71A
GMCH_SEL=1	NORTHWOOD	VTT_GMCH=1.45V	OCP 1.98A ~ 3.78A

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Compal Electronics, Inc.			
Title		DDR_25V/VTT_GMCH	
Size		Document Number	
		LA-2041	
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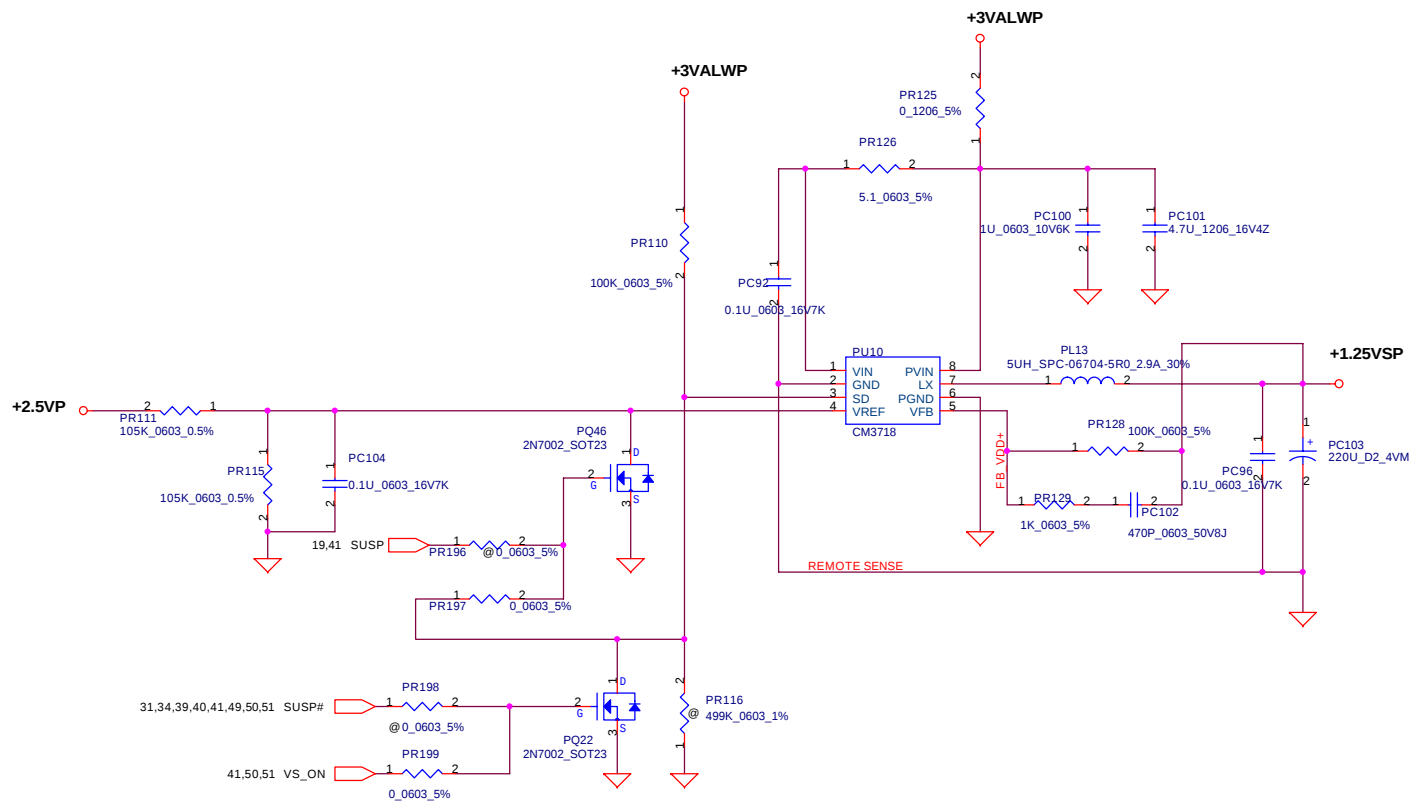
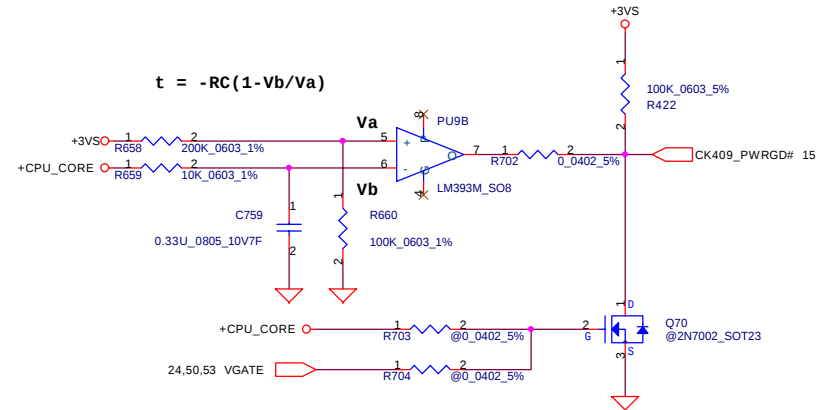
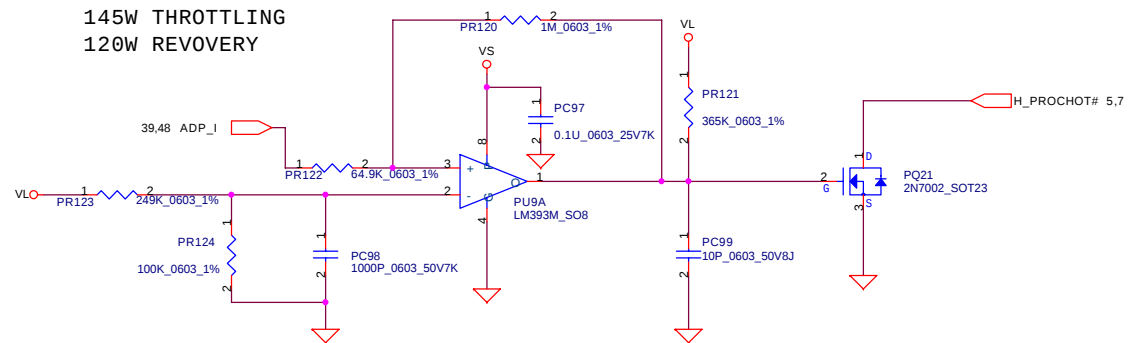
NV34M Ultra			
POWER_SEL=1	VOUT=1.28V	OCP 7.1A ~ 8.9A	PR113=2.8K_0603_1%
POWER_SEL=0	VOUT=1.15V	OCP 6.85A ~ 8.7A	PR208=8.66K_0603_1%

NV31			
POWER_SEL=1	VOUT=1.27V	OCP 7.1A ~ 8.9A	PR113=2.7K_0603_1%
POWER_SEL=0	VOUT=1V	OCP 6.85A ~ 8.7A	Unpop PR208

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Compal Electronics, Inc.			
Title VGA_CORE/1.5V			
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145W THROTTLING 120W RECOVERY

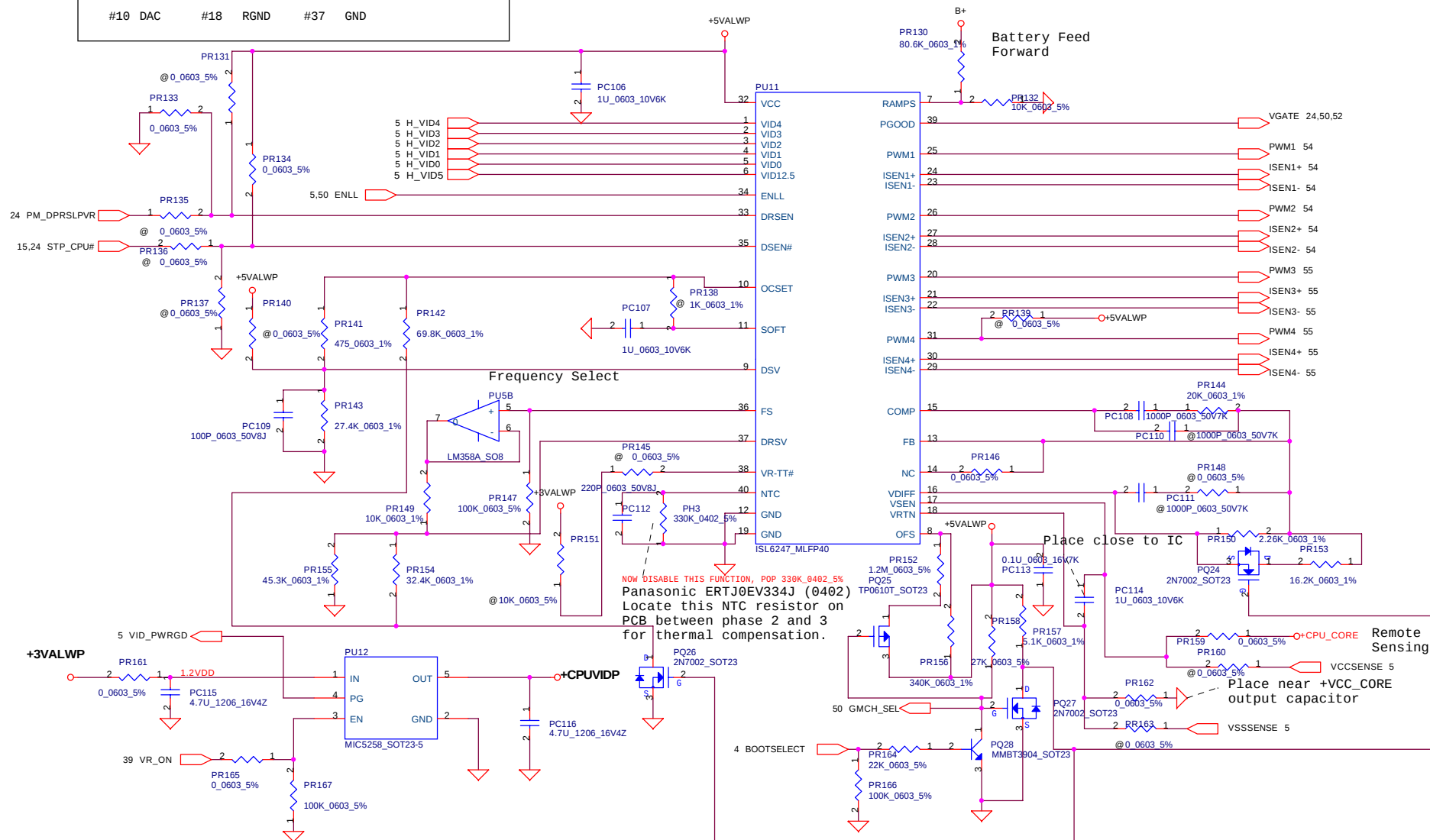


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Compal Electronics, Inc.			
Title			
DDR_1.25V/CLOCK THROTTLING			
Size	Document Number		Rev
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Different Pin Definition for ISL6561 in PU9

#7	GND	#11	REF	#33	EN	#38	OVP
#9	TCOMP	#14	IDROOP	#35	GND	#40	GND
#10	DAC	#18	RGND	#37	GND		



1. When mode control signal is high/ low, the VR will operate to Northwood/ Prescott load line.
2. VID5(12.5) should be pulled high, when the VR operates to Northwood load line.

BOOTSELECT=1 PRESCOTT

BOOTSELECT=0 NORTHWOOD

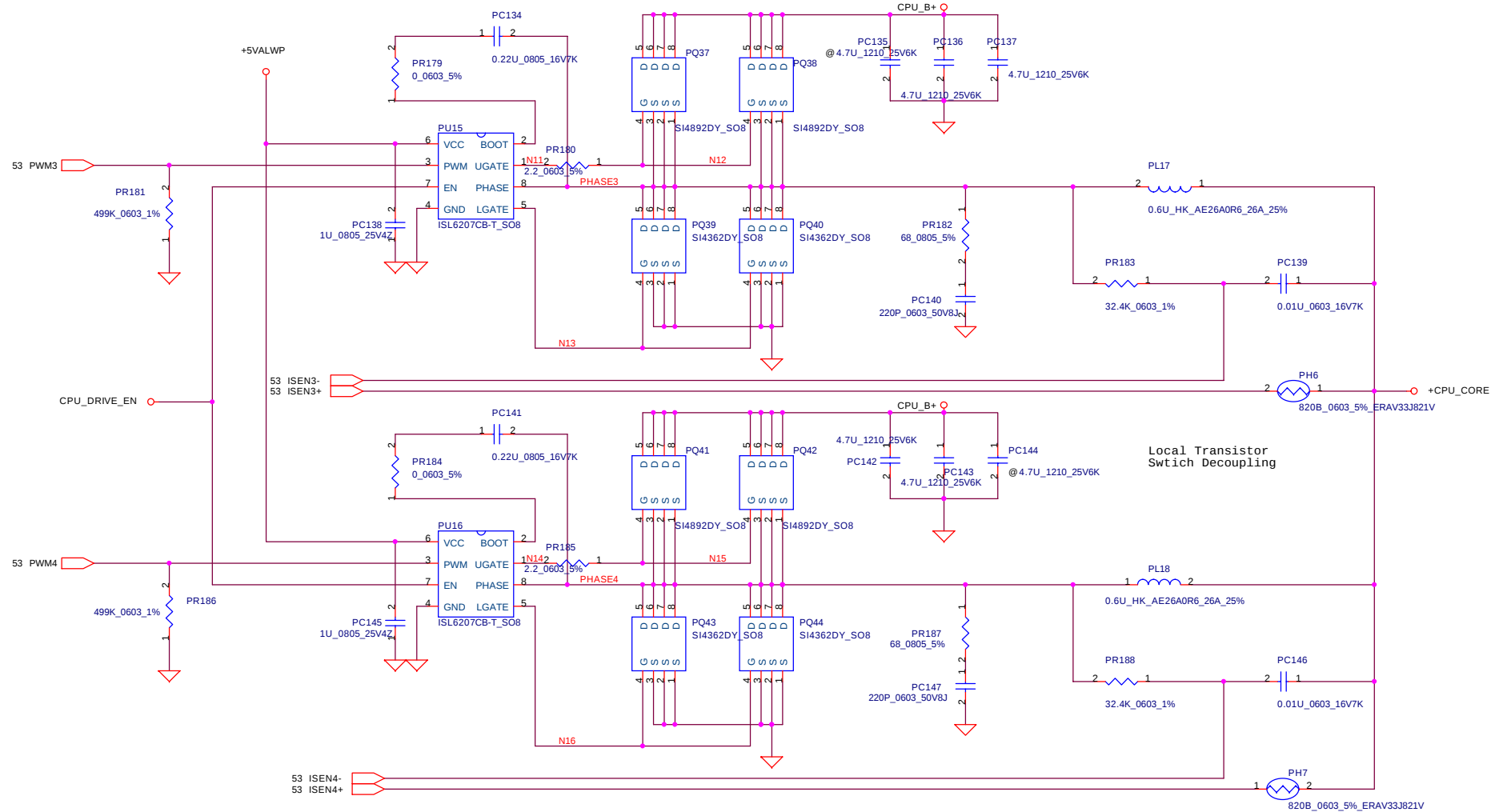
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Compal Electronics, Inc.

CPU_CORE Controller

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Compal Electronics, Inc.			
Title			
CPU_CORE Power stage 2			
Size			
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DBQ01 PIR LIST

***** Rev0.1 PIR List *****

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Compal Electronics, Inc.		
Title		
DBQ01 PIR LIST		
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