

LongBeach 100

LA-2451 REV 0.3 Schematic

Desktop LGA-775 Package

RC400M(RU400M)+SB400+ATI M22P/M24P(64/128MB VRAM)

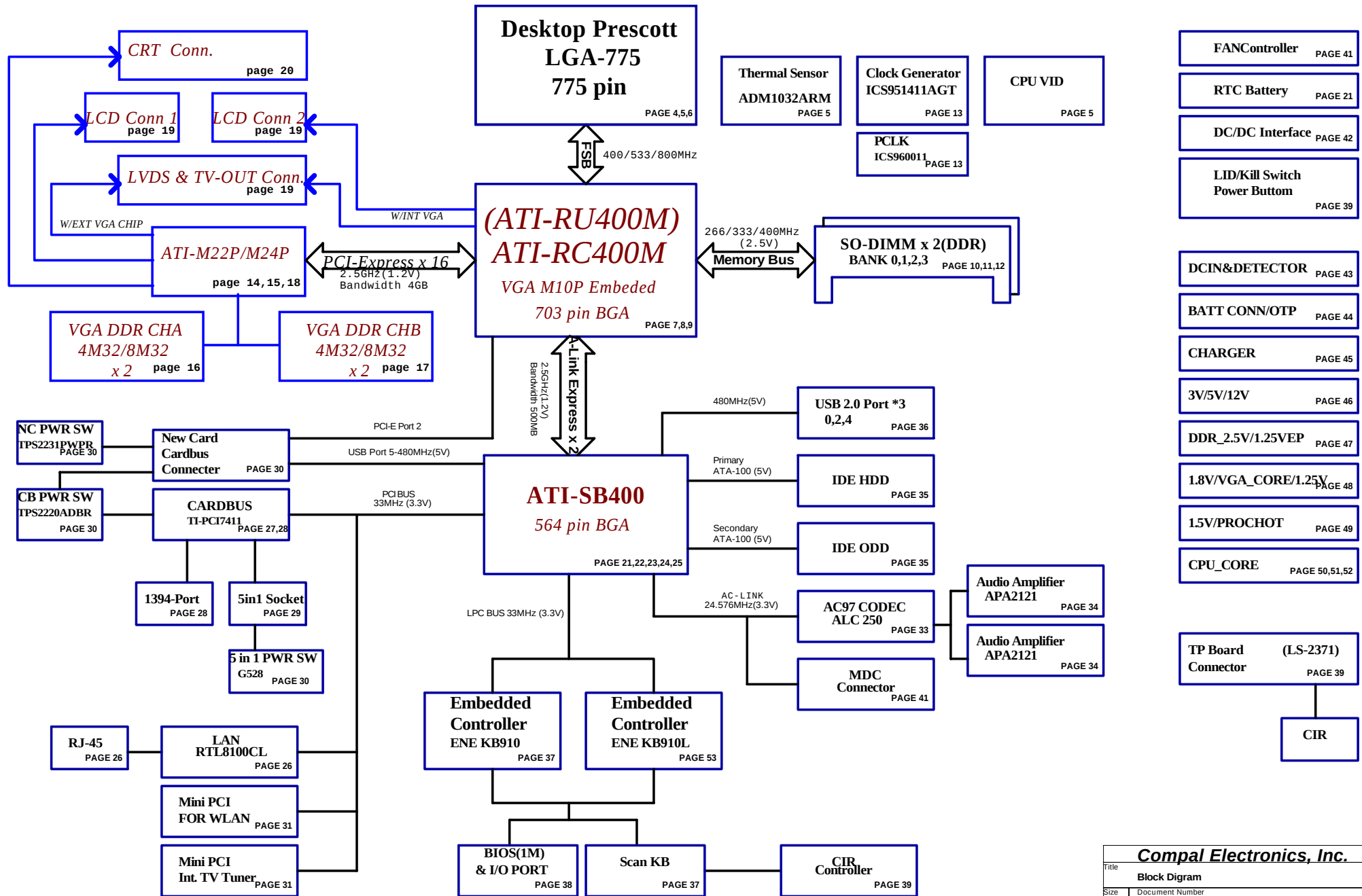
2004-09-01<A>

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EAQ11 LA-2451

FUNCTION BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VGA_CORE	1.0V/1.2V switched power rail for VGA chip	ON	OFF	OFF
+1.2VS	1.2VS for PCI-Express	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 8X	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#GNT#	Interrupts
CardBus(PCI7411)	AD20	2	PIRQA/PIRQB/PIRQC/PIRQD
LAN	AD22	1	PIRQG/PIRQC
Mini-PCI(WLAN)	AD18	3	PIRQF:PIRQG/PIRQC:PIRQD
Mini-PCI(TV-Tuner)	AD23	4	PIRQH:PIRQE/PIRQD:PIRQA

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b	ICS960011	1101 110X b
(24C84)	1011 000Xb		

EC SM Bus2 address

SB400 SM Bus address

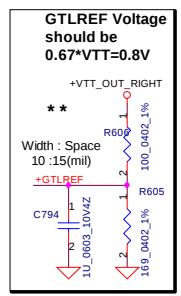
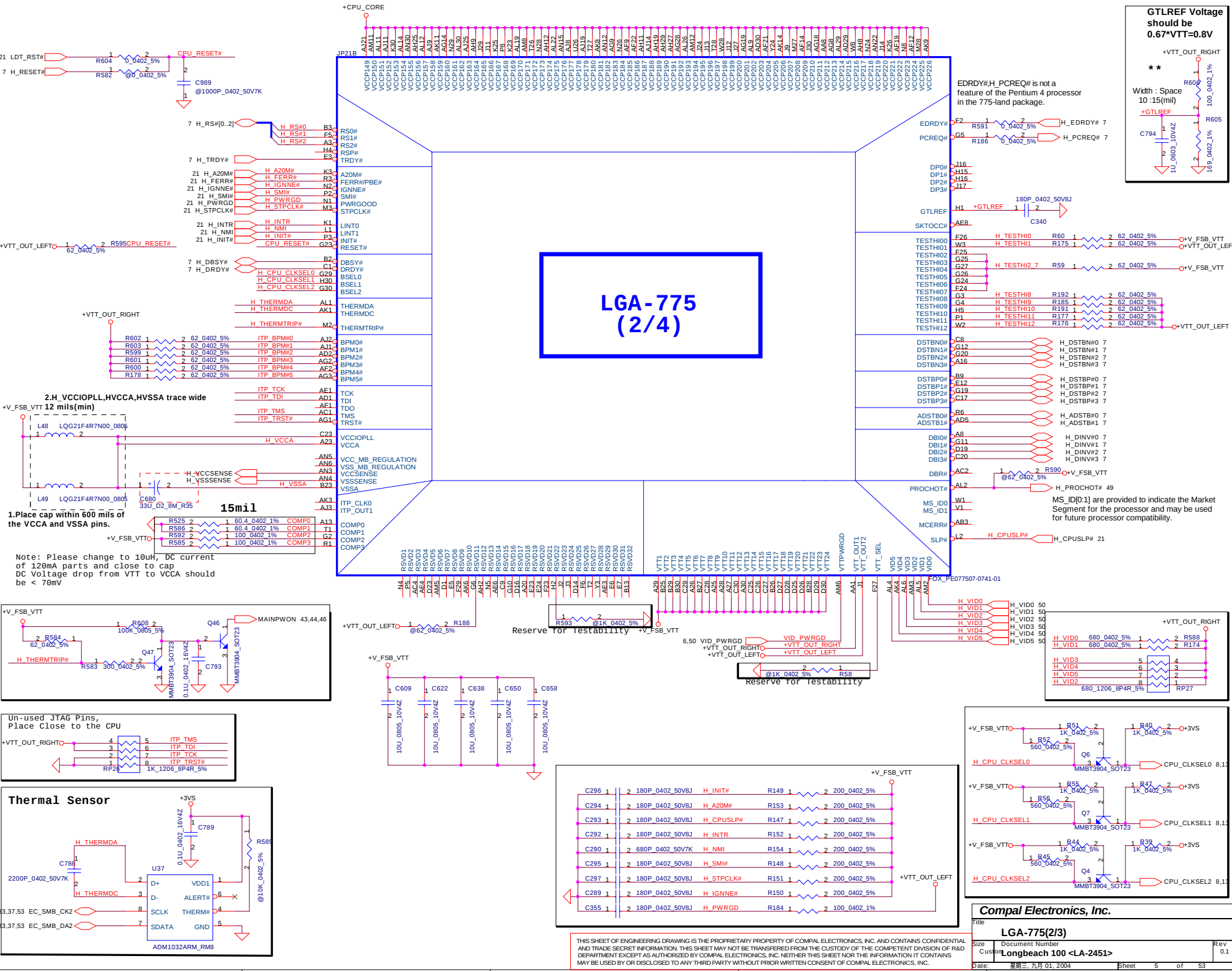
Device	Address
Clock Generator (ICS951411VGLFT)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 001Xb

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

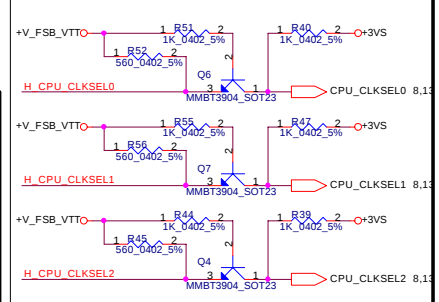
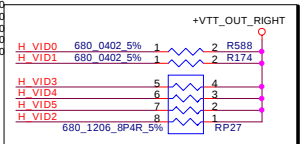
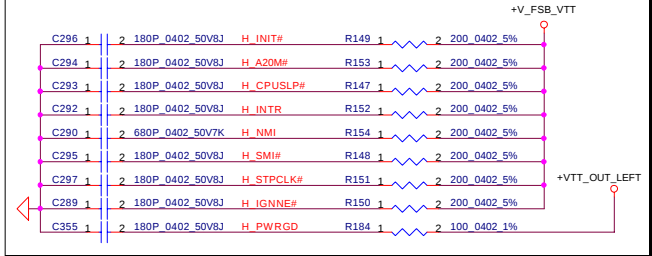
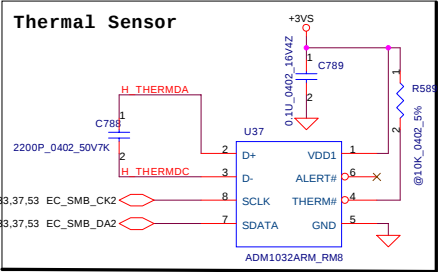
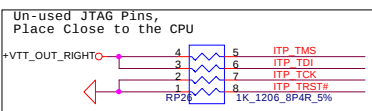
Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	



LGA-775
(2/4)

Note: Please change to 10uH, DC current of 120mA parts and close to cap DC voltage drop from VTT to VCCA should be < 70mV



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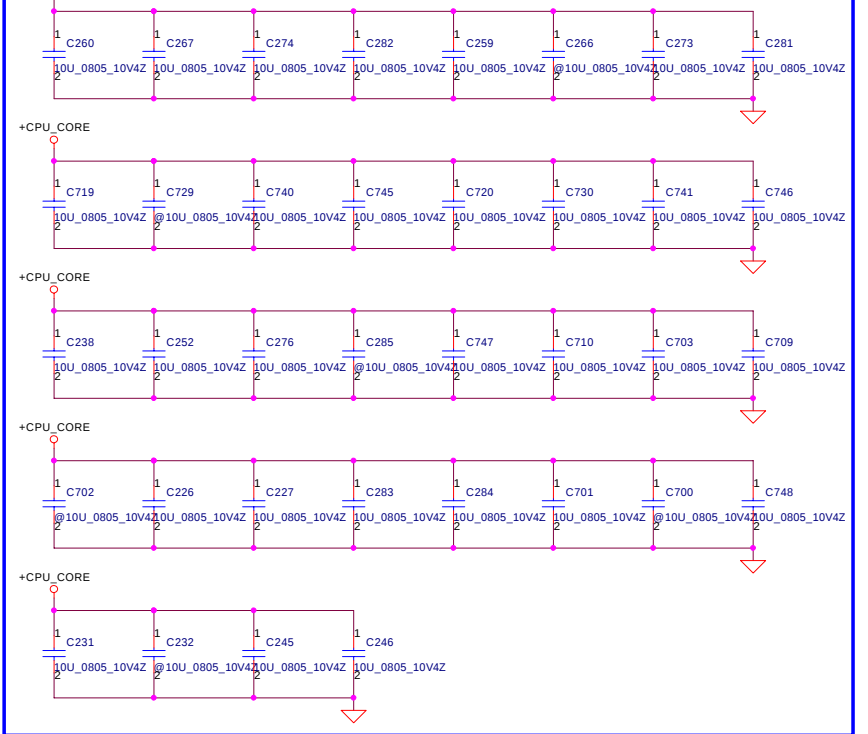
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Size		Document Number	
Customer		Longbeach 100 <LA-2451>	
Date		Rev	
2004.09.01		0.1	
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H29This pin in CPU is GTLREF_SEL, but not VSS.

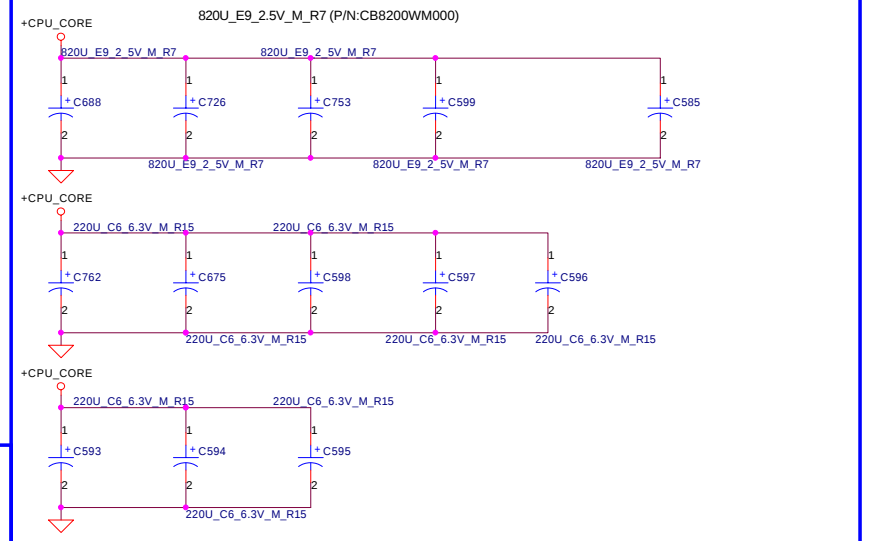
Reserve for testability
P4 Processor output GTLREF_SEL = 0

Place all 100 0805 6.3V6M of 8 pcs inside CPU socket cavity
Place all 100 0805 6.3V6M of 8 pcs on another side of CPU socket cavity



SANYO OS-CON 820uF _ERS7m ohm* 6

SANYO OS-CON 820uF _ERS13m ohm* 8



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LGA-775(3/3)

Document Number
Longbeach 100 <LA-2451>

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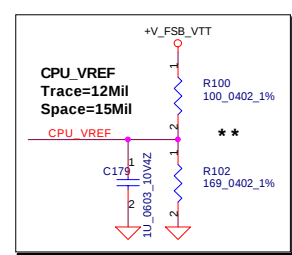
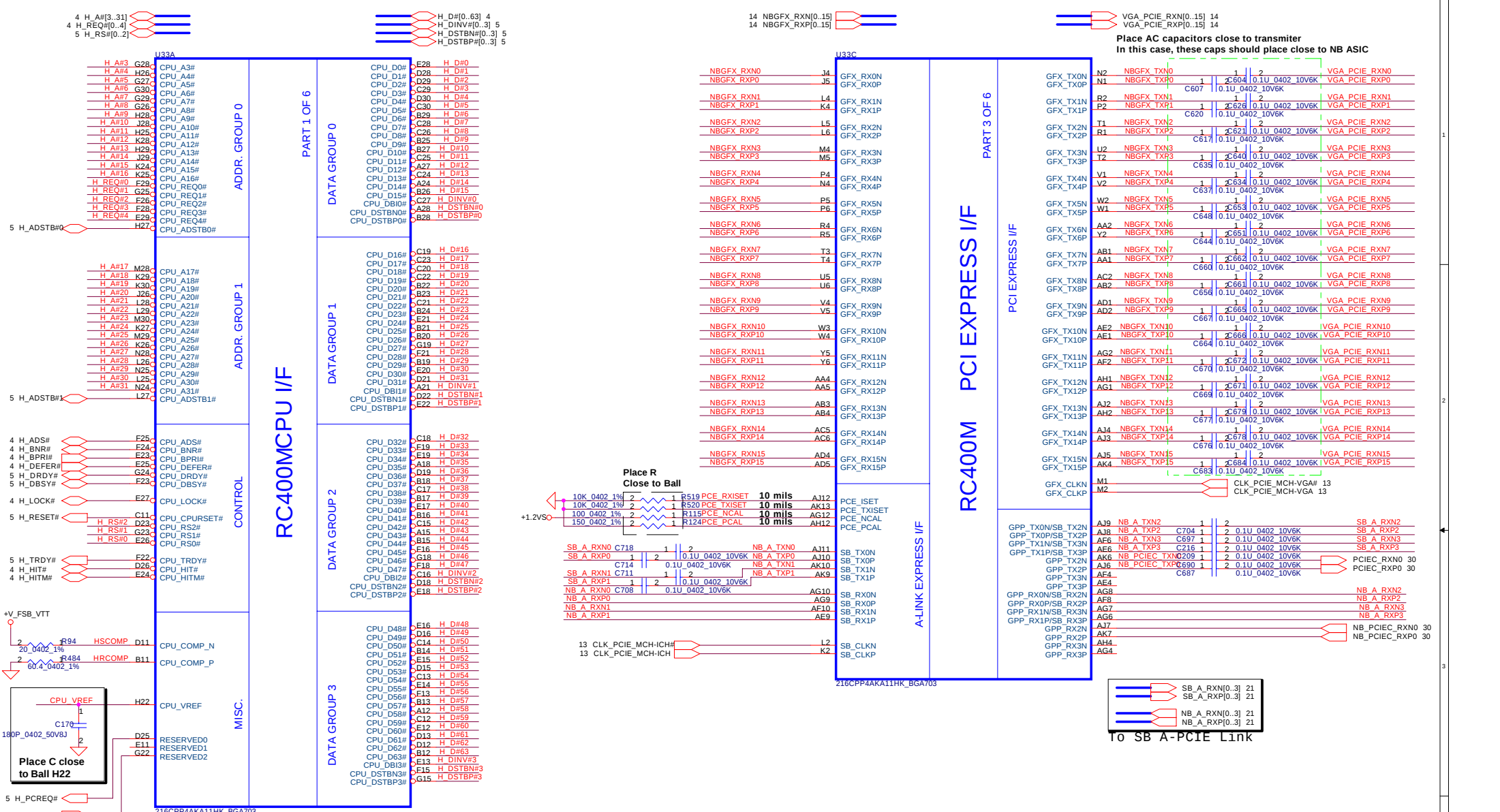
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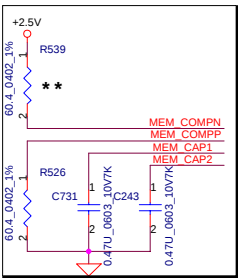
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Decoupling Reference Document:
Grantsdale Chipset Platform Design guide Rev1.2
(15434)Page263

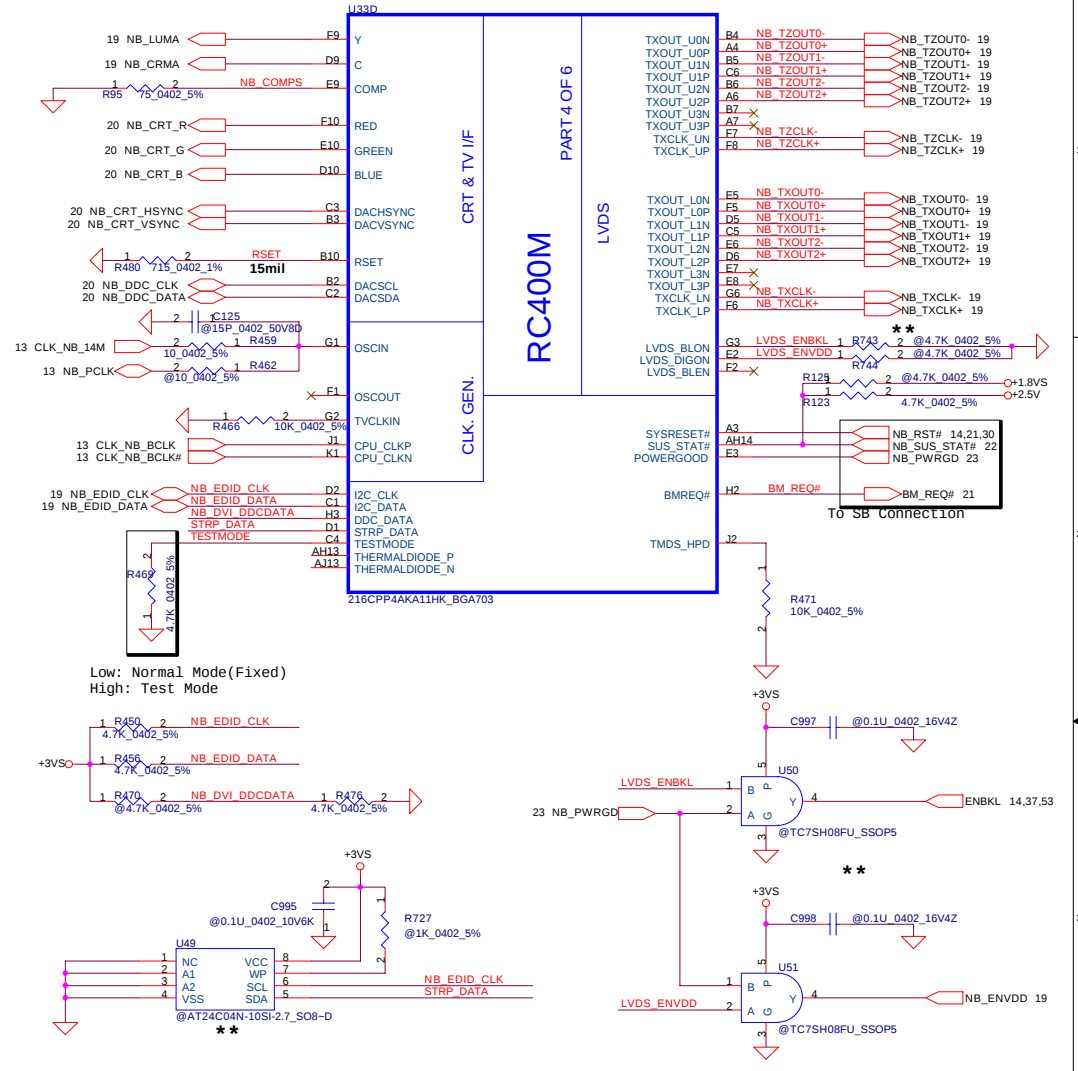
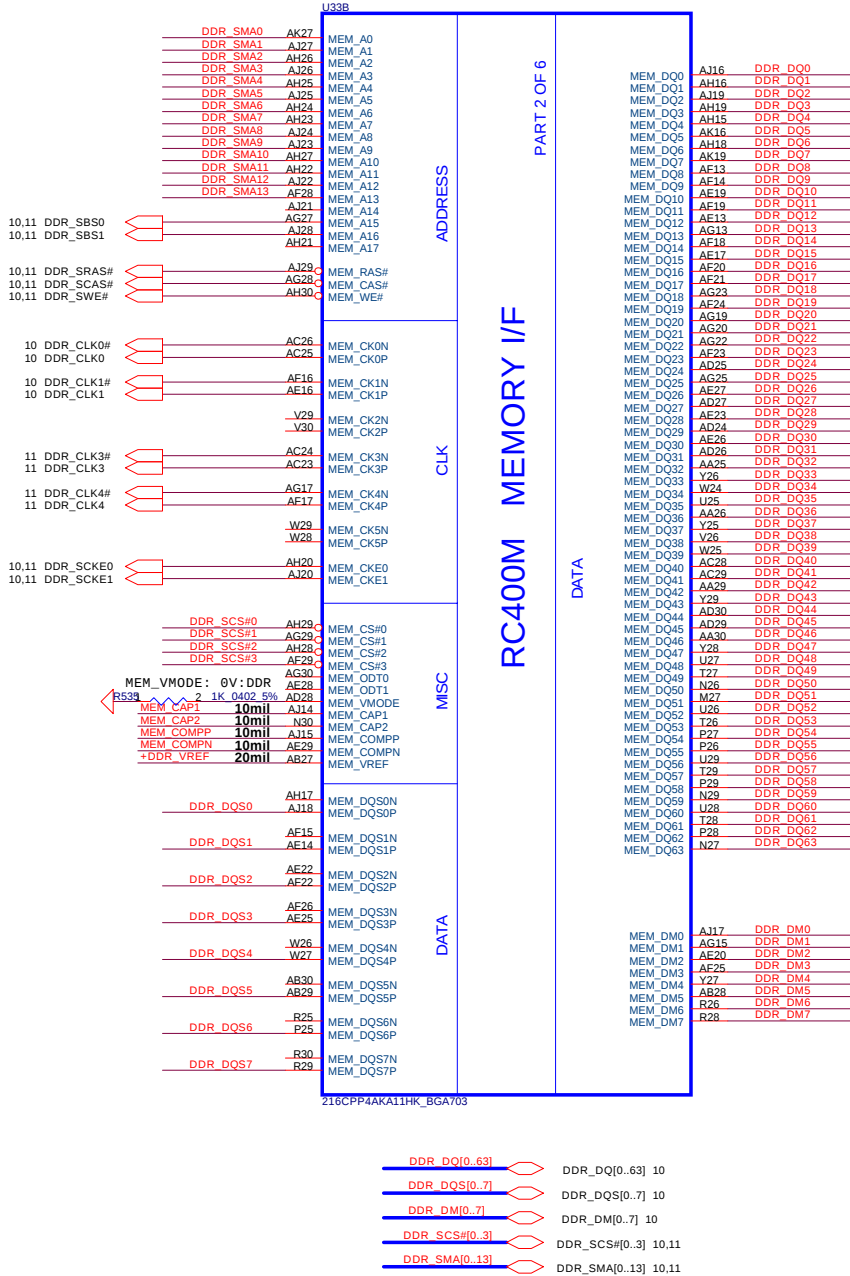
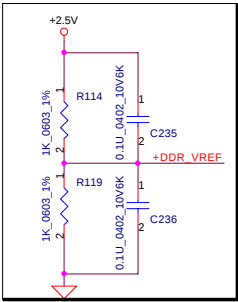
Decoupling Reference Requirement:
560uF Polymer, ESR:6m ohm(each) * 10
22uF X5R * 8
10uF X5R * 10

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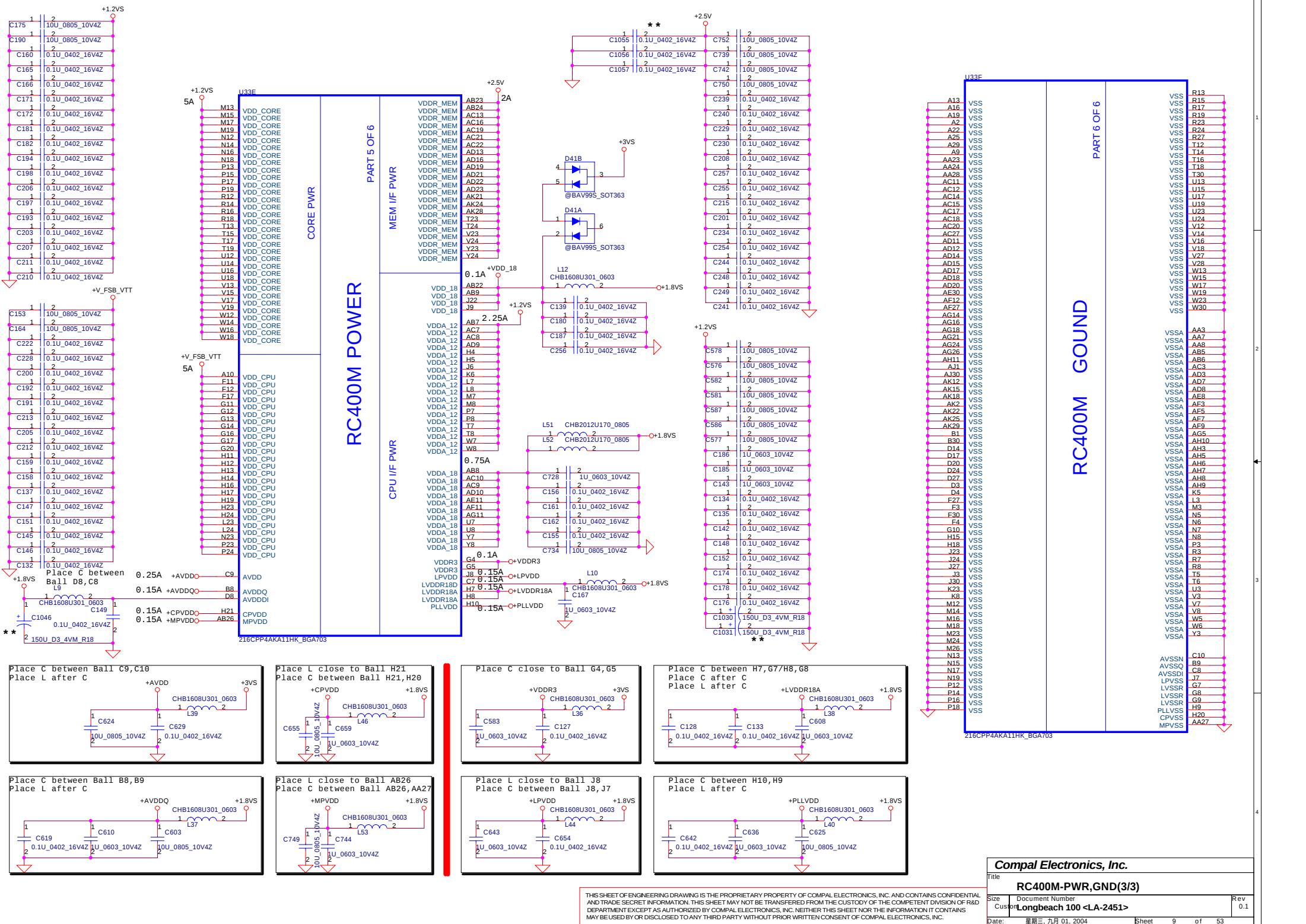




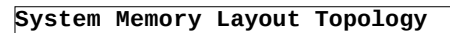
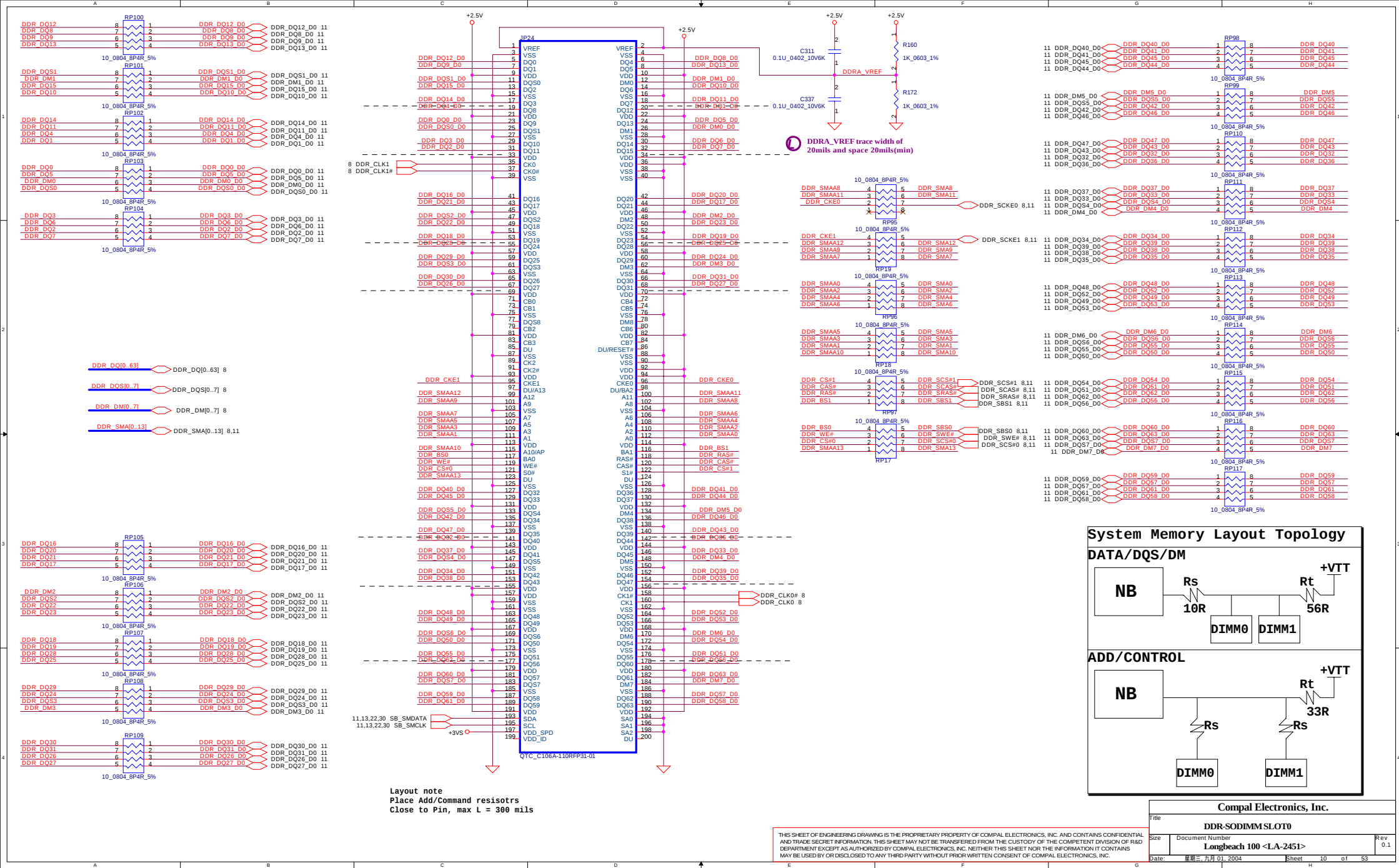
Place these R and C
close to relative Ball.



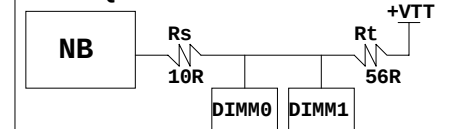
NB STRAPING PINS			
BM_REQ#	R467 1	2 4.7K 0402 5%	CPU_CLKSEL2 5.13
NB_CRT_HS	R468 1	2 4.7K 0402 5%	CPU_CLKSEL1 5.13
NB_CRT_VSYNC	R469 1	2 4.7K 0402 5%	CPU_CLKSEL0 5.13
NB_DDC_CLK: CPU VCC SEL DEFAULT: 1 1: DESKTOP CPU 0: MOBILE CPU			
STRP_DATA: DEBUG STRAP DEFAULT: 1 0: MEMORY CHANNEL STRAPING 1: EPROM STRAPING			



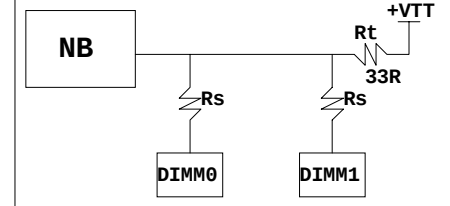
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DATA/DQS/DM



ADD/CONTROL

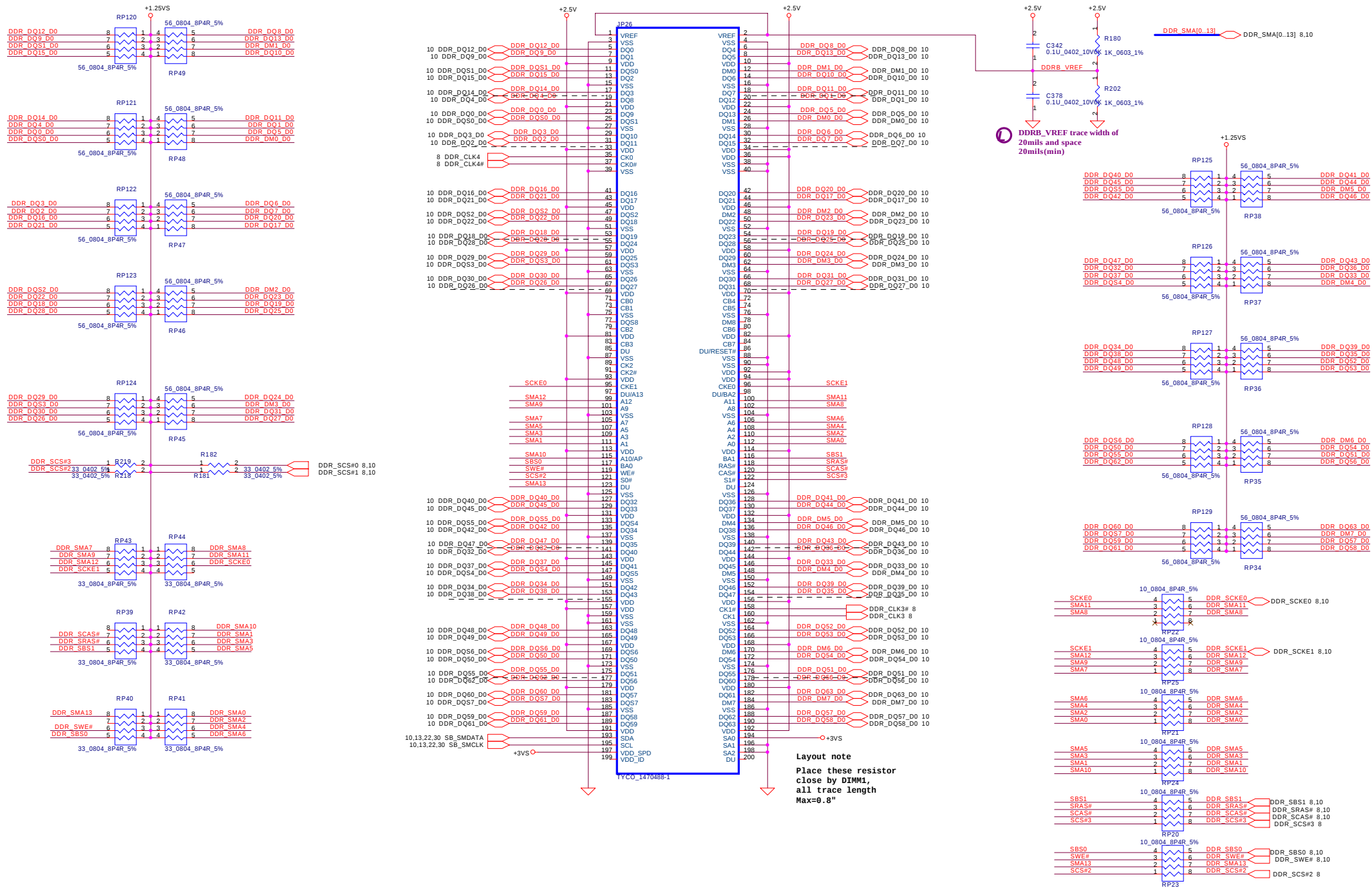


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DDR-SODIMM SLOT0

Title			
DDR-SODIMM SLOT0			
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	Longbeach 100 <LA-2451>	0.1	
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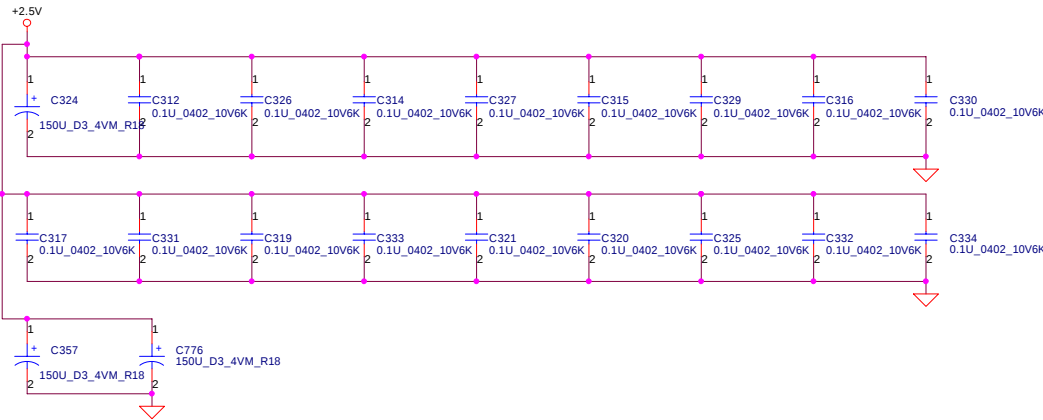
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DDR-SODIMM SLOT1		
File	Document Number	Rev 0.1
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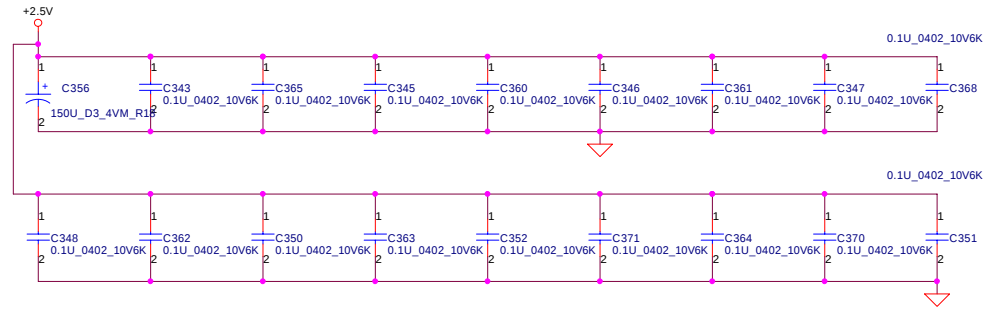
Layout note :
Distribute as close as possible
to DDR-SODIMM0.



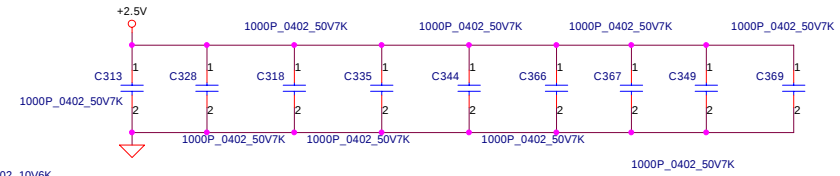
Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25VS



Layout note :
Distribute as close as possible
to DDR-SODIMM1.



Layout note :
for EMI solution

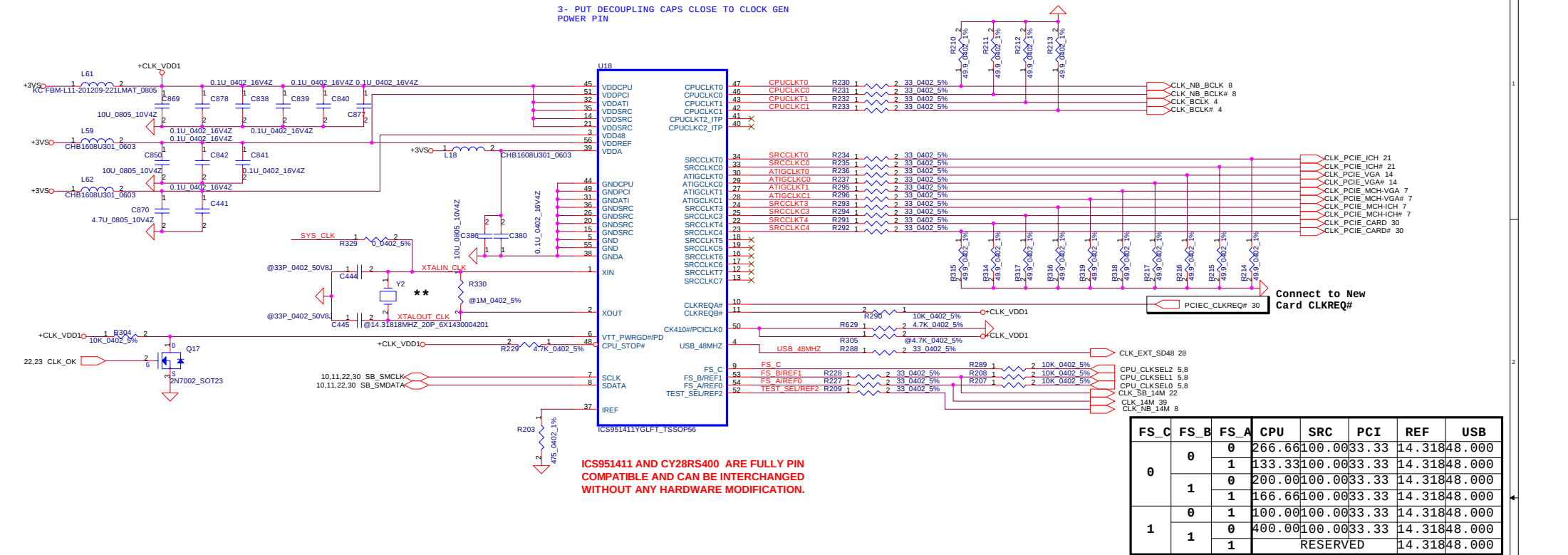


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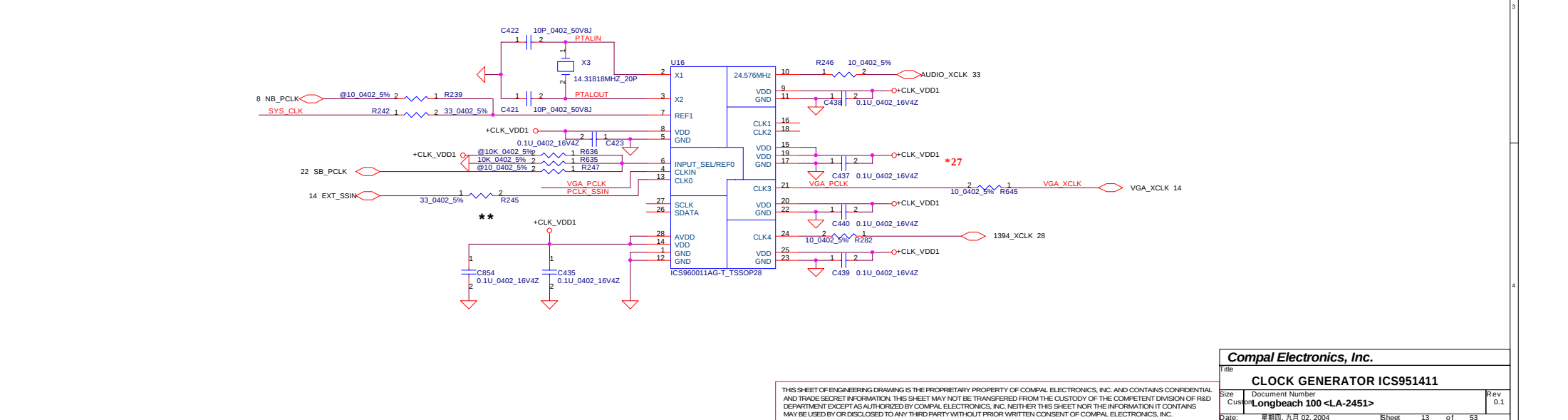
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DDR SODIMM Decoupling			
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Clock Generator

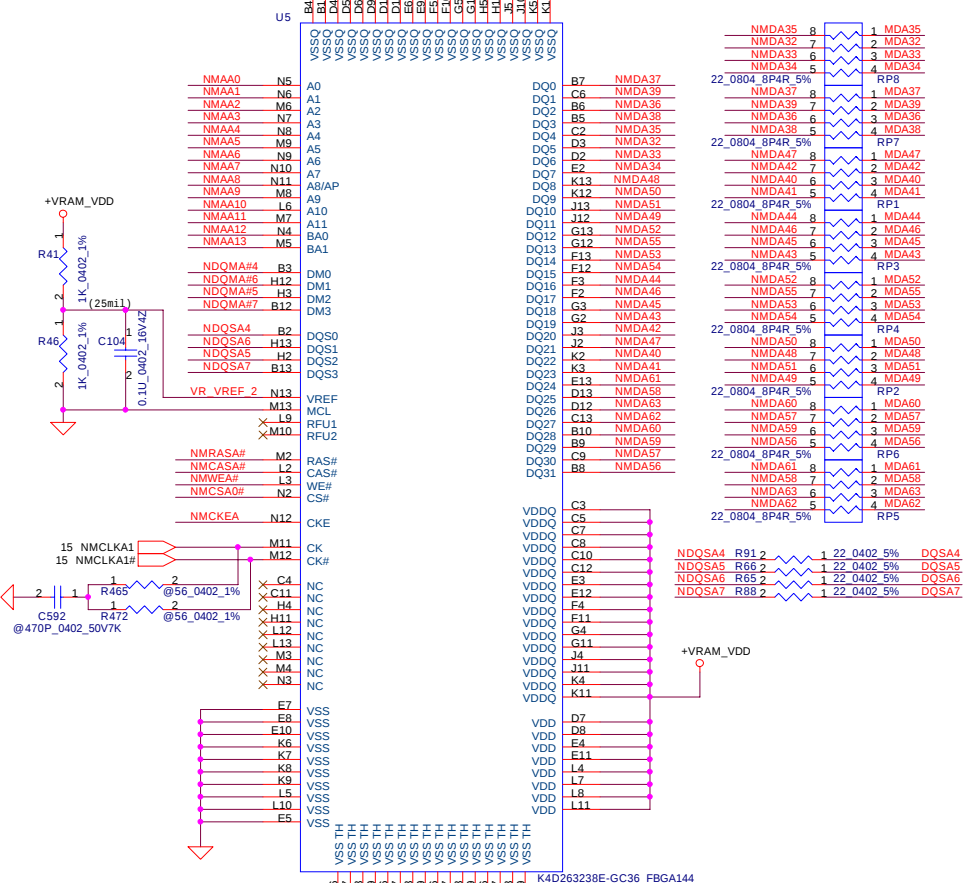
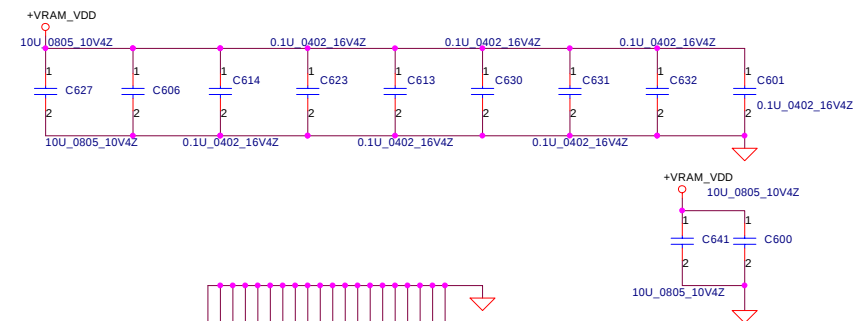
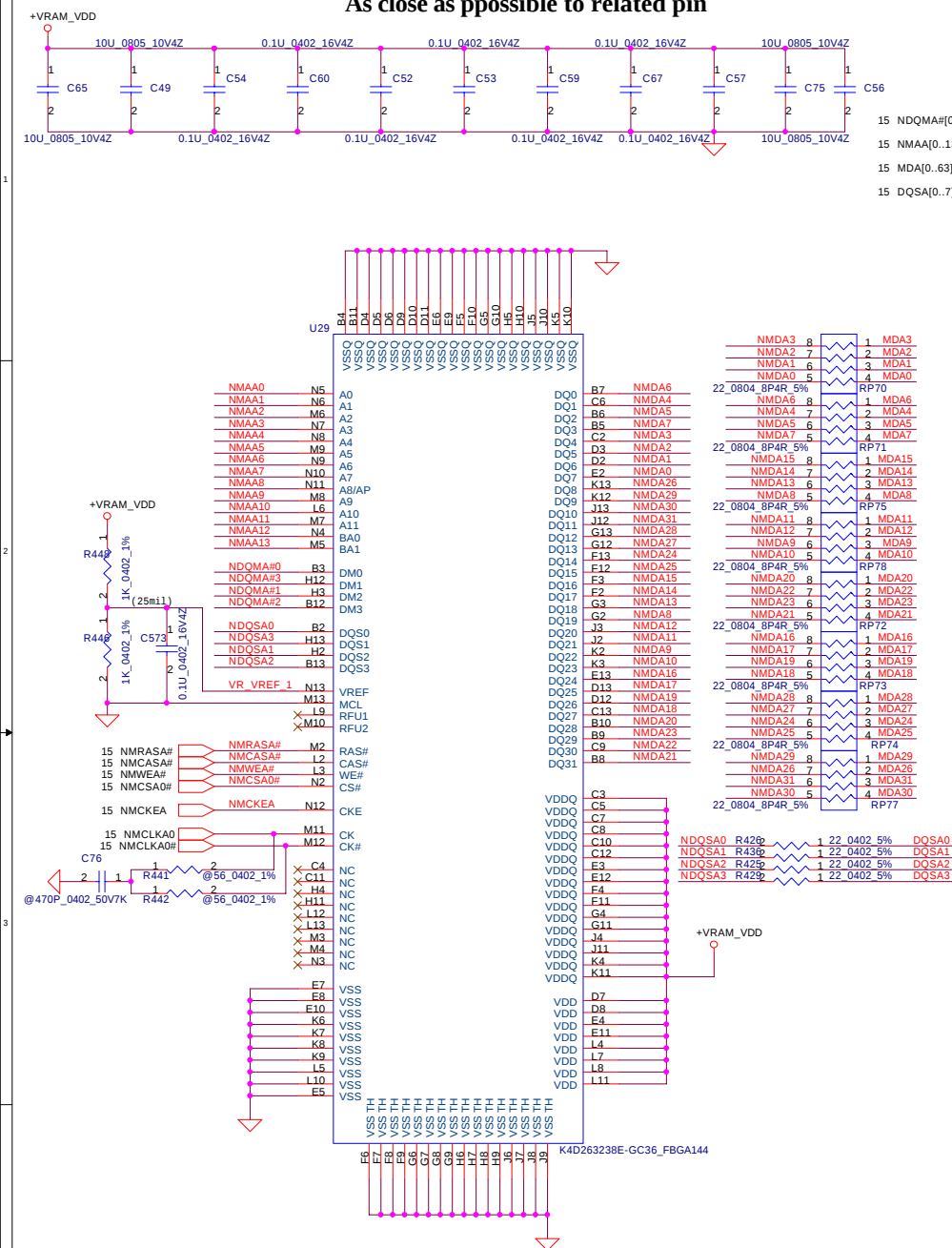
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLOCK GEN AS POSSIBLE
- 2- ROUTE ALL CPULCK/#, NBCLK/#, ITPCLK/# AND SCR/# ,AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



CLOCK OF IC

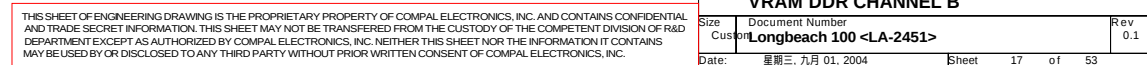
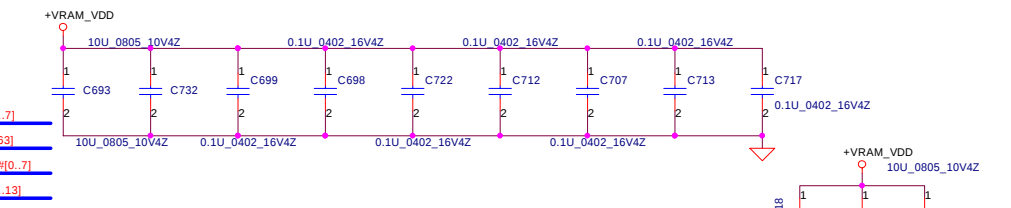


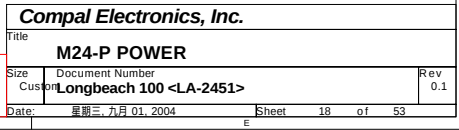
As close as possible to related pin



As close as possible to related pin

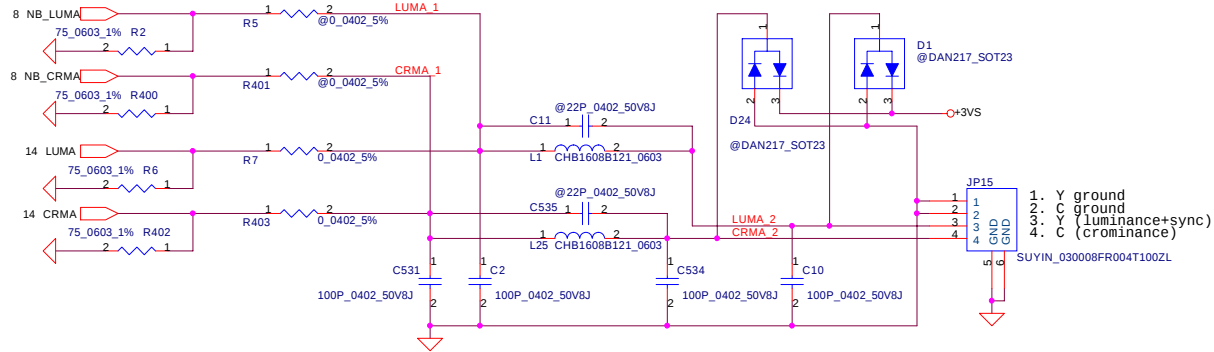
15 DQSB[0..7]
 15 MDB[0..63]
 15 NDQMB# [0..7]
 15 NMAB[0..13]



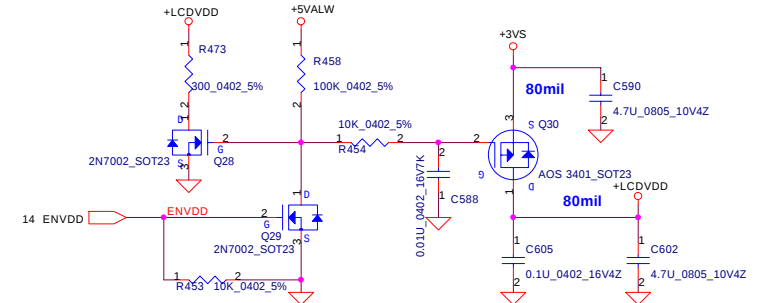


TV-OUT CONNECTOR

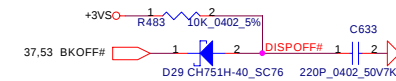
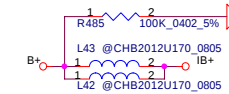
Reduce LUMA_1 and CRMA_1 length
As short as possible



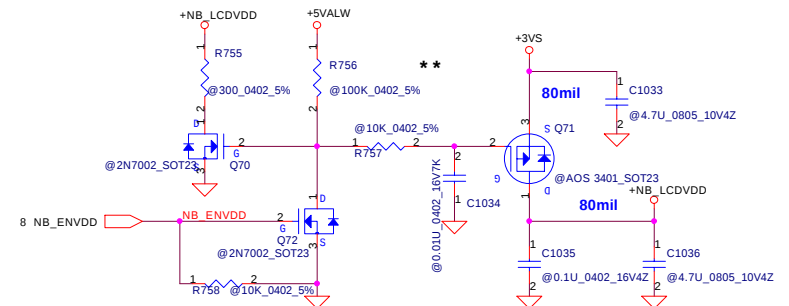
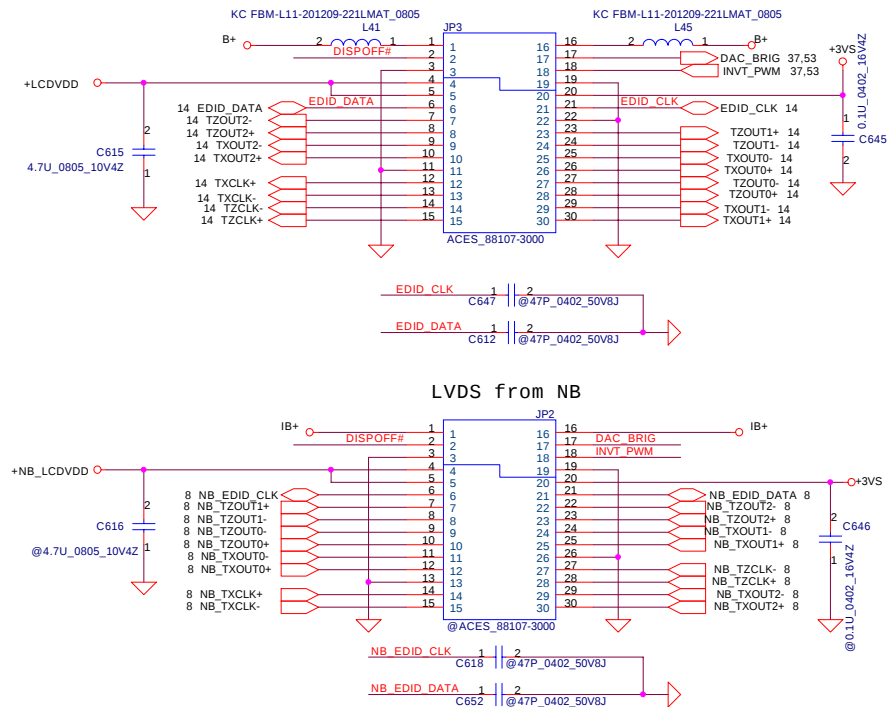
PANEL +LCDVDD CTRL CKT



+LCDVDD Width: 40mils
Place below parts between JP6 and JP7



LCD CONNECTOR



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CRT,TV-OUT,LVDS

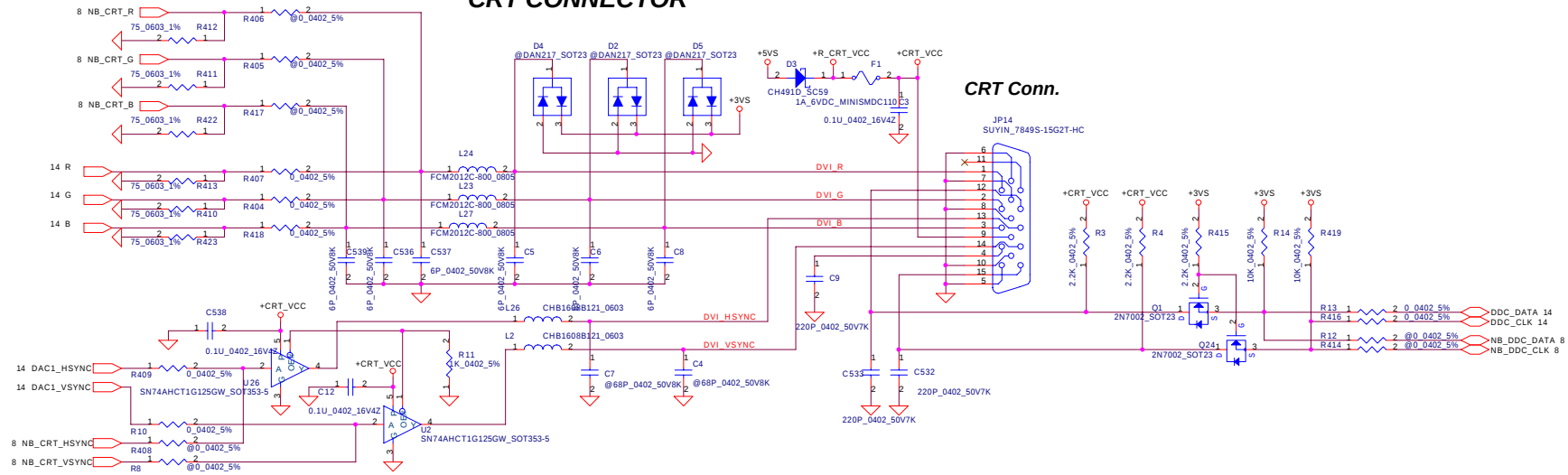
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Customer Longbeach 100 <LA-2451>

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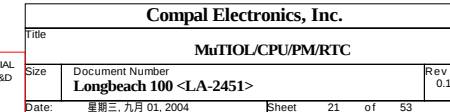
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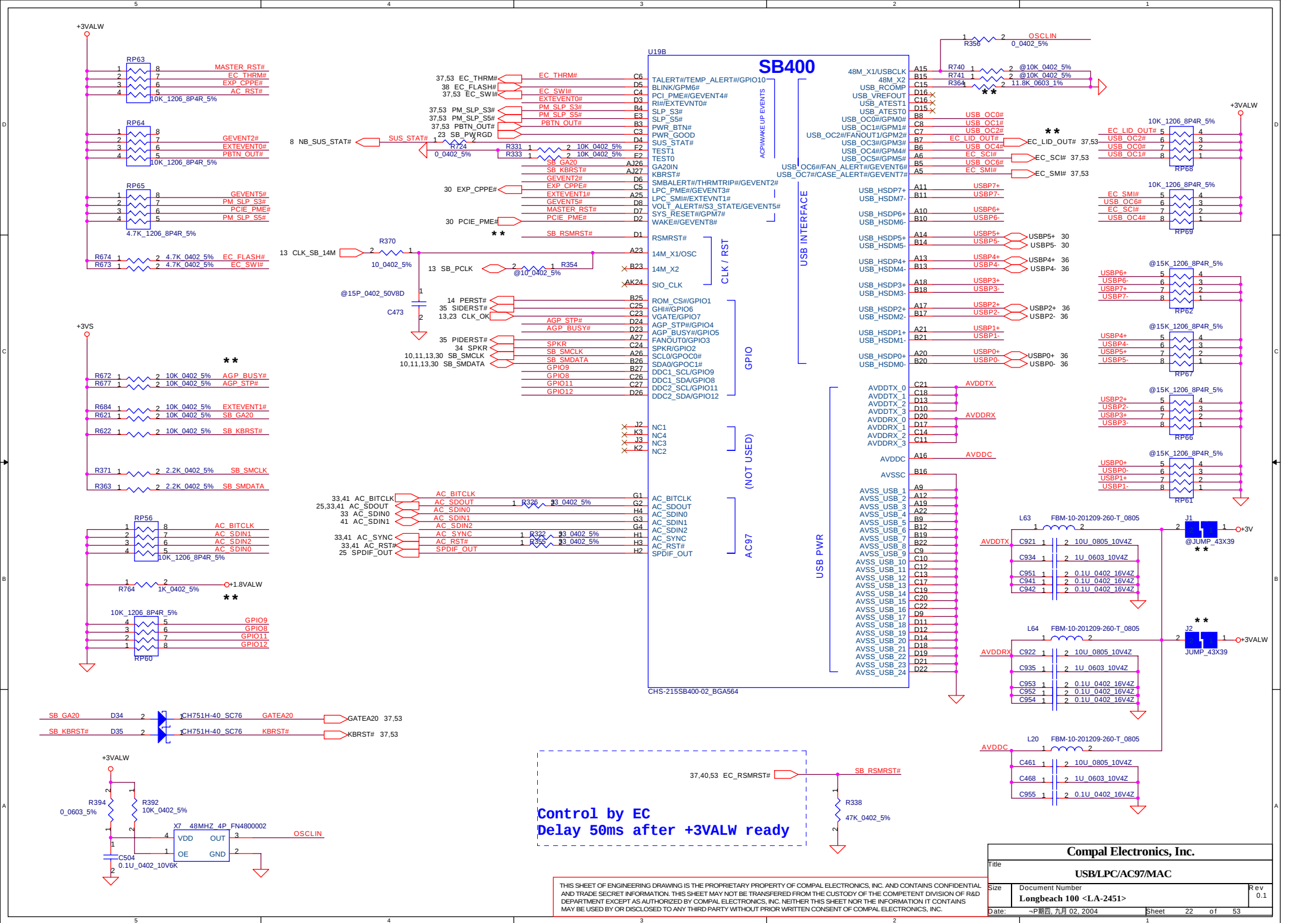
CRT CONNECTOR

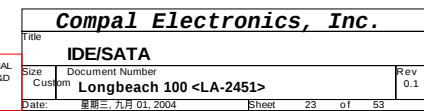
CRT Conn.



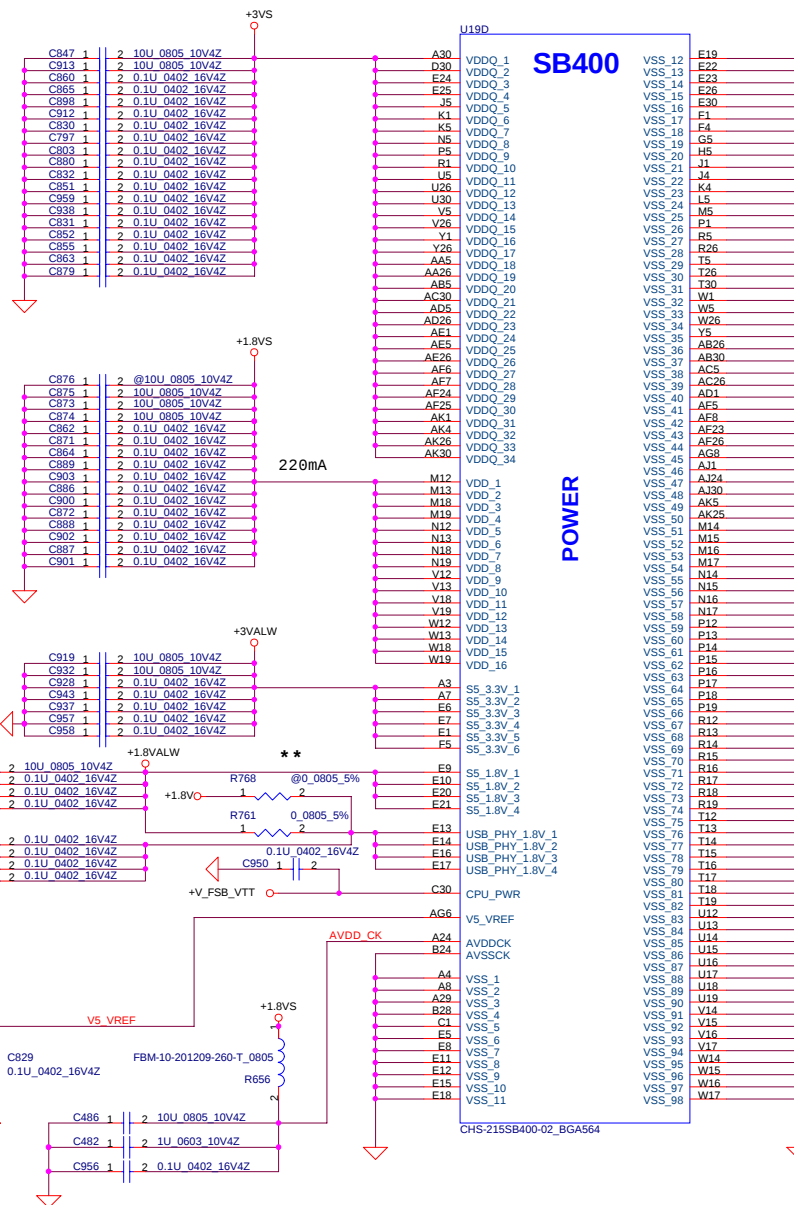
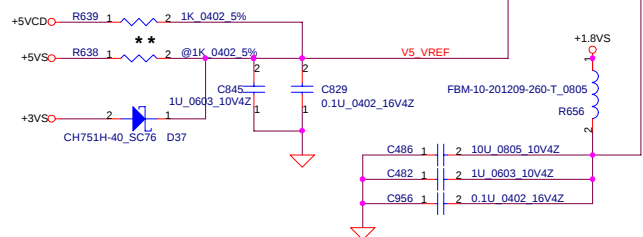
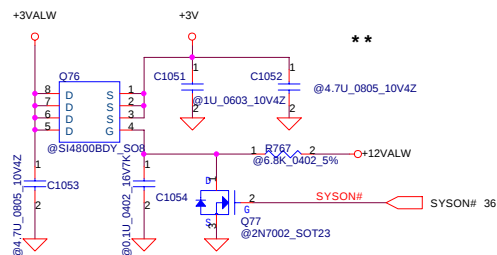
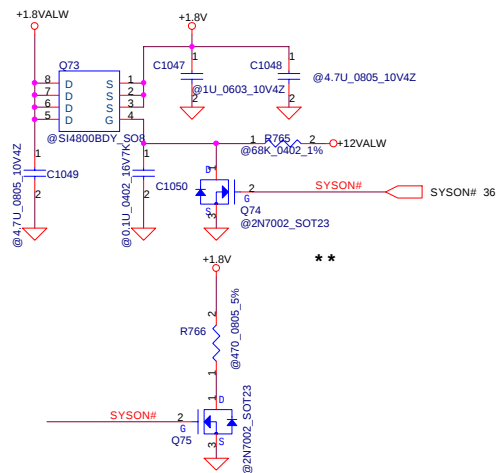
25,26,28,31,32,42 PCI_AD[0..31] PCI_AD[0..31]



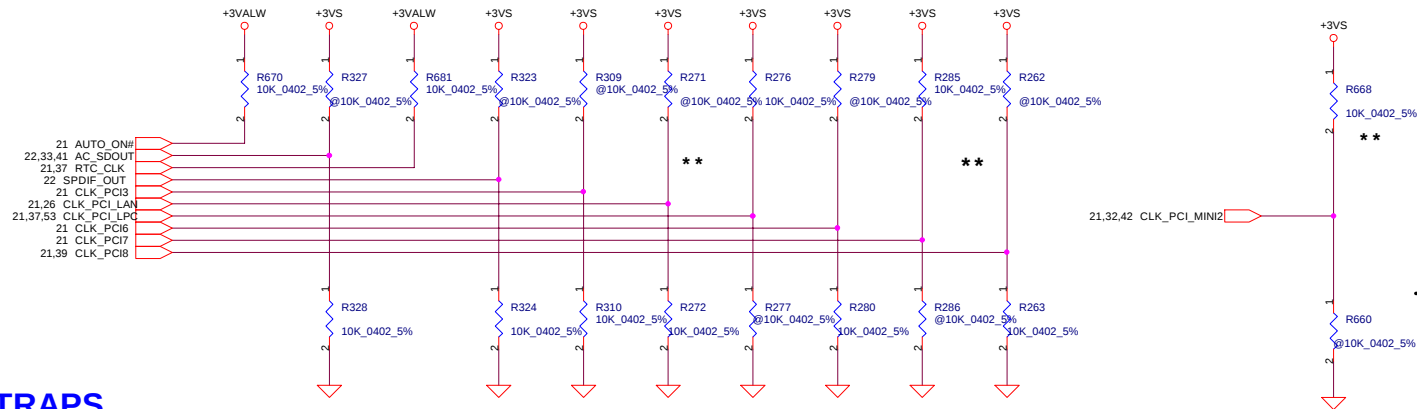




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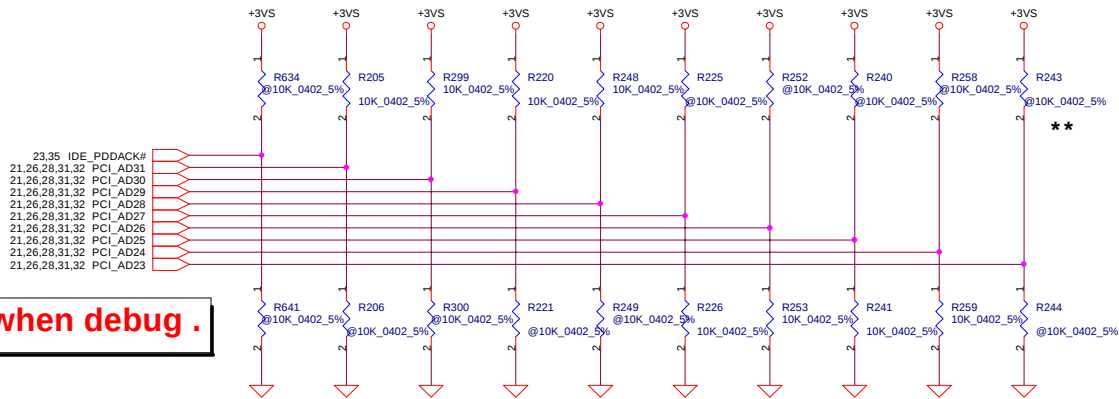


REQUIRED STRAPS



	AUTO_ON#	AC97_SDOOUT	RTC_CLK	SPDIF_OUT	CLK_PCI3	CLK_PCI_LAN	CLK_PCI_LPC	PCI_CLK6	PCI_CLK7	PCI_CLK8	CLK_PCI_MINI2
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	USB PHY PWRDOWN DISABLE	Internal PLL	14MHz OSC MODE DEFAULT	CPU I/F = K8	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM		Clock input buffer DEFAULT
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	USB PHY PWRDOWN ENABLE DEFAULT	External Clock DEFAULT	14MHz XTAL MODE	CPU I/F = P4 DEFAULT	L,H = NORMAL LPC ROM L,L = FWH ROM		Crystal Pad

Pop R634 when debug .

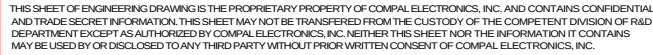


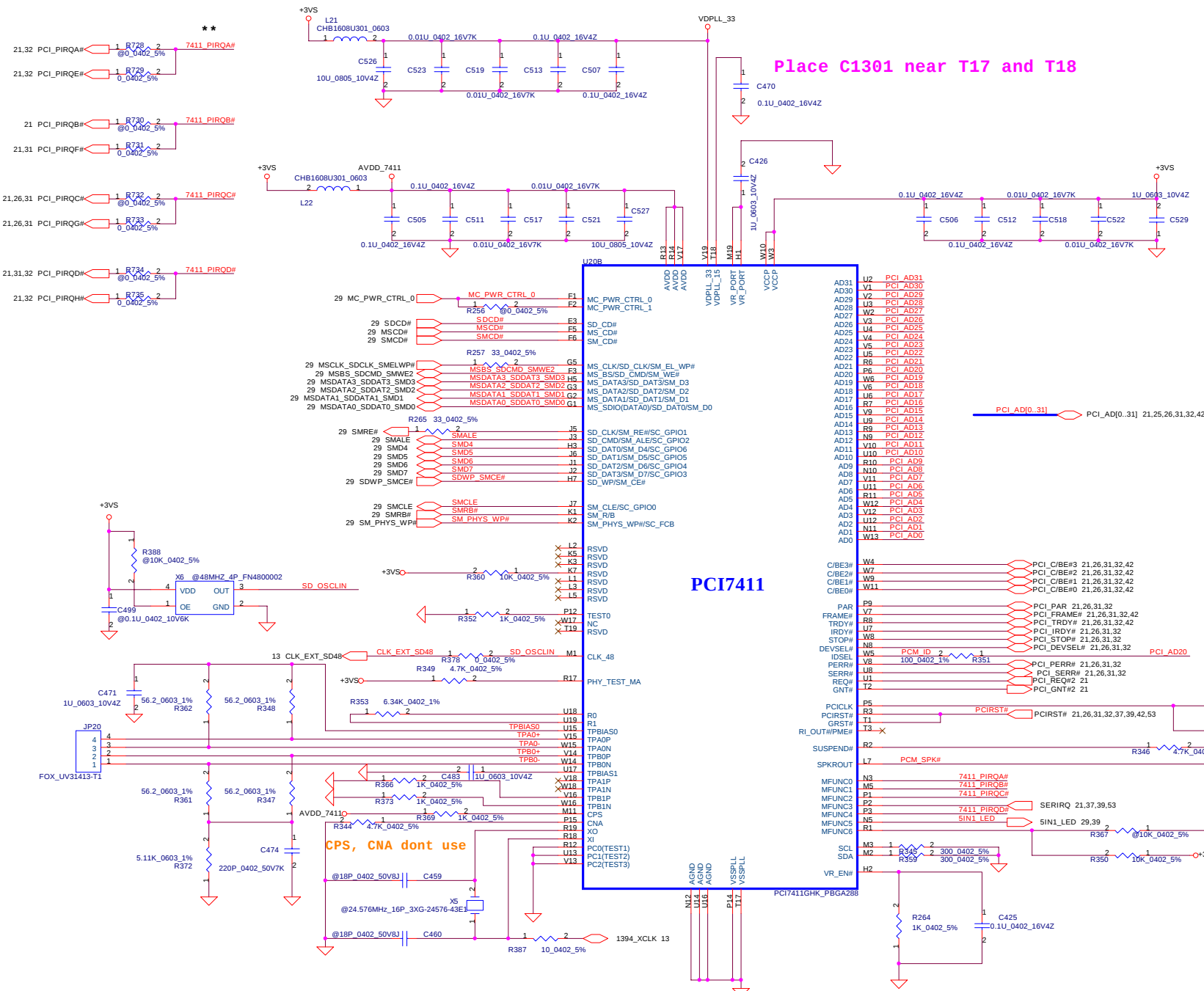
DEBUG STRAPS

	IDE_PDDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24
PULL HIGH	USE LONG RESET DEFAULT	PLL CHARGE PUMP CTRL BIT 1 HI DEFAULT	PLL CHARGE PUMP CTRL BIT 0 HI DEFAULT	PLL VCO CTRL BIT 1 HI DEFAULT	PLL VCO CTRL BIT 0 HI DEFAULT	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS
PULL LOW	USE SHORT RESET	PLL CHARGE PUMP CTRL BIT 1 LO	PLL CHARGE PUMP CTRL BIT 0 LO	PLL VCO CTRL BIT 1 LO	PLL VCO CTRL BIT 0 LO	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT

Compal Electronics, Inc.			
Title			
Hardware Trap			
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PCI7411

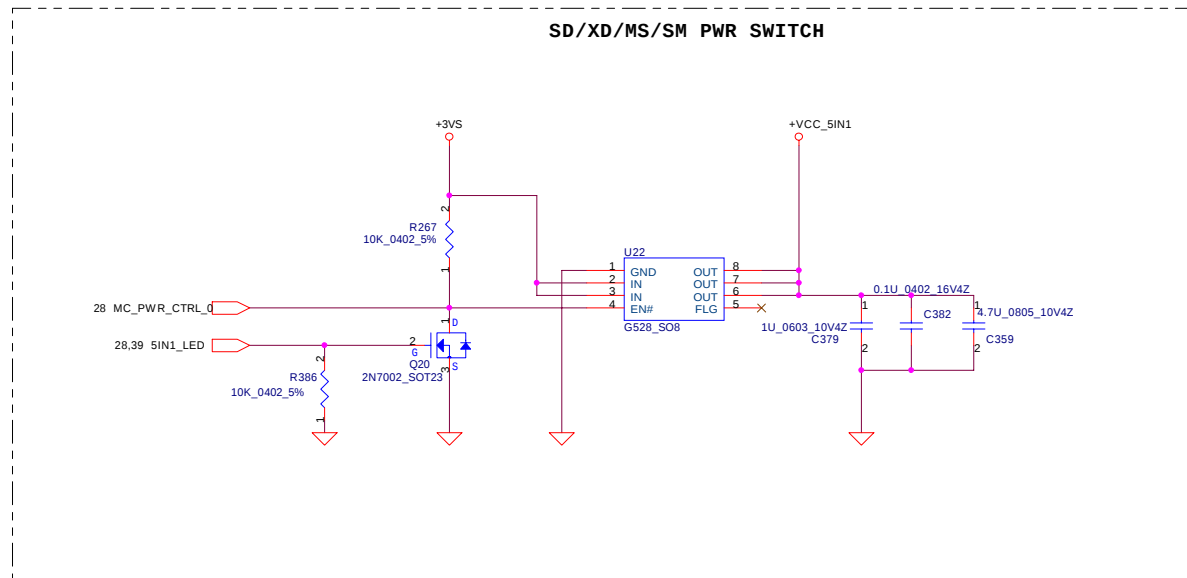
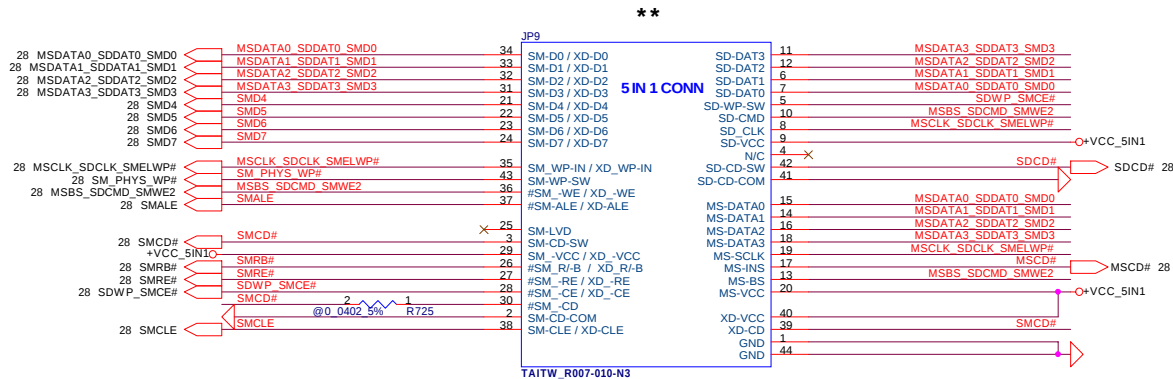
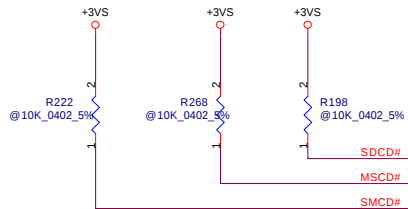
Place C1301 near T17 and T18

PCI_AD[0..31] PCI_AD[0..31] 21,25,26,31,32,42

CPS, CNA dont use

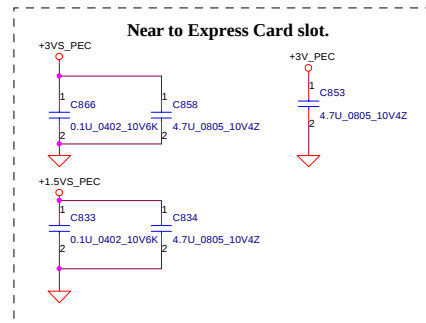
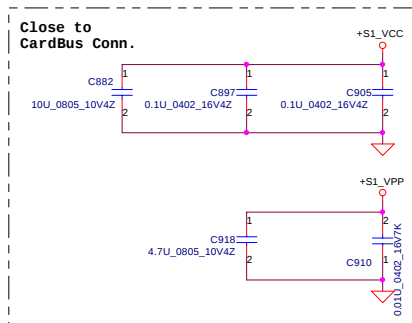
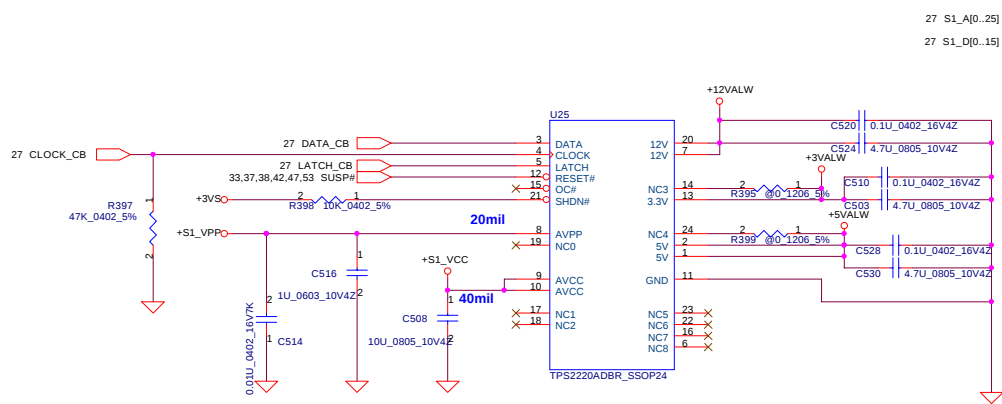
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Title		PCI7411-2	
Size	Document Number	Rev	0.1
Customer		Longbeach 100 <LA-2451>	
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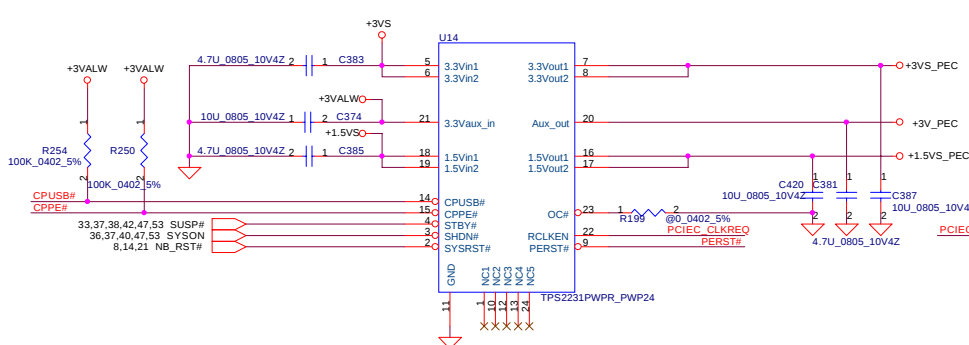


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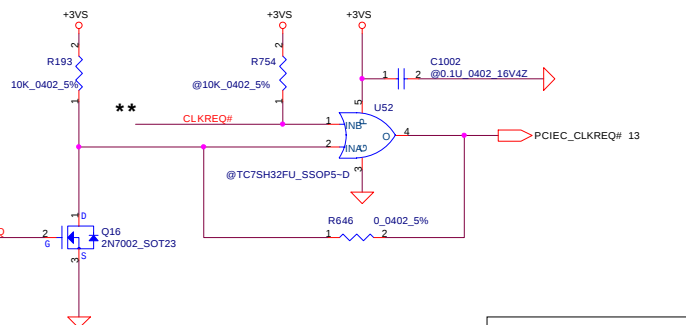
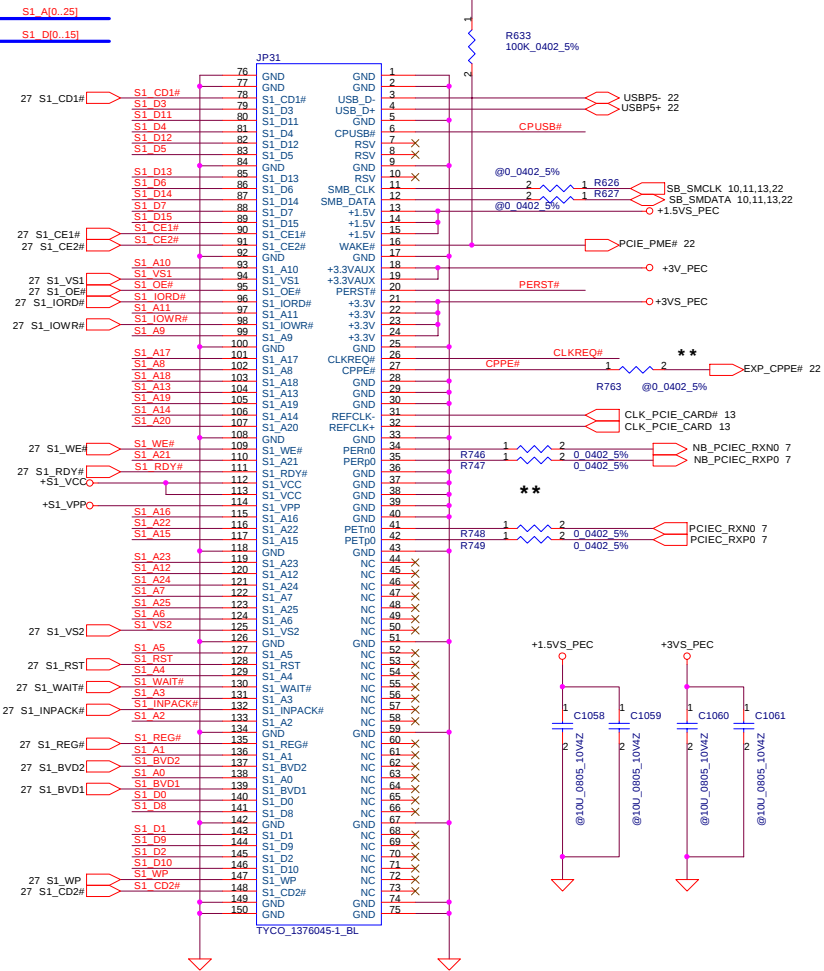
Power Switch for PCMCIA



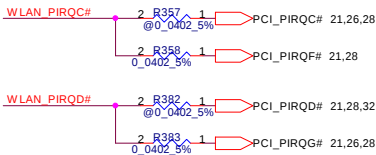
Power Switch for PCI-E



CardBus & PCI-E Socket

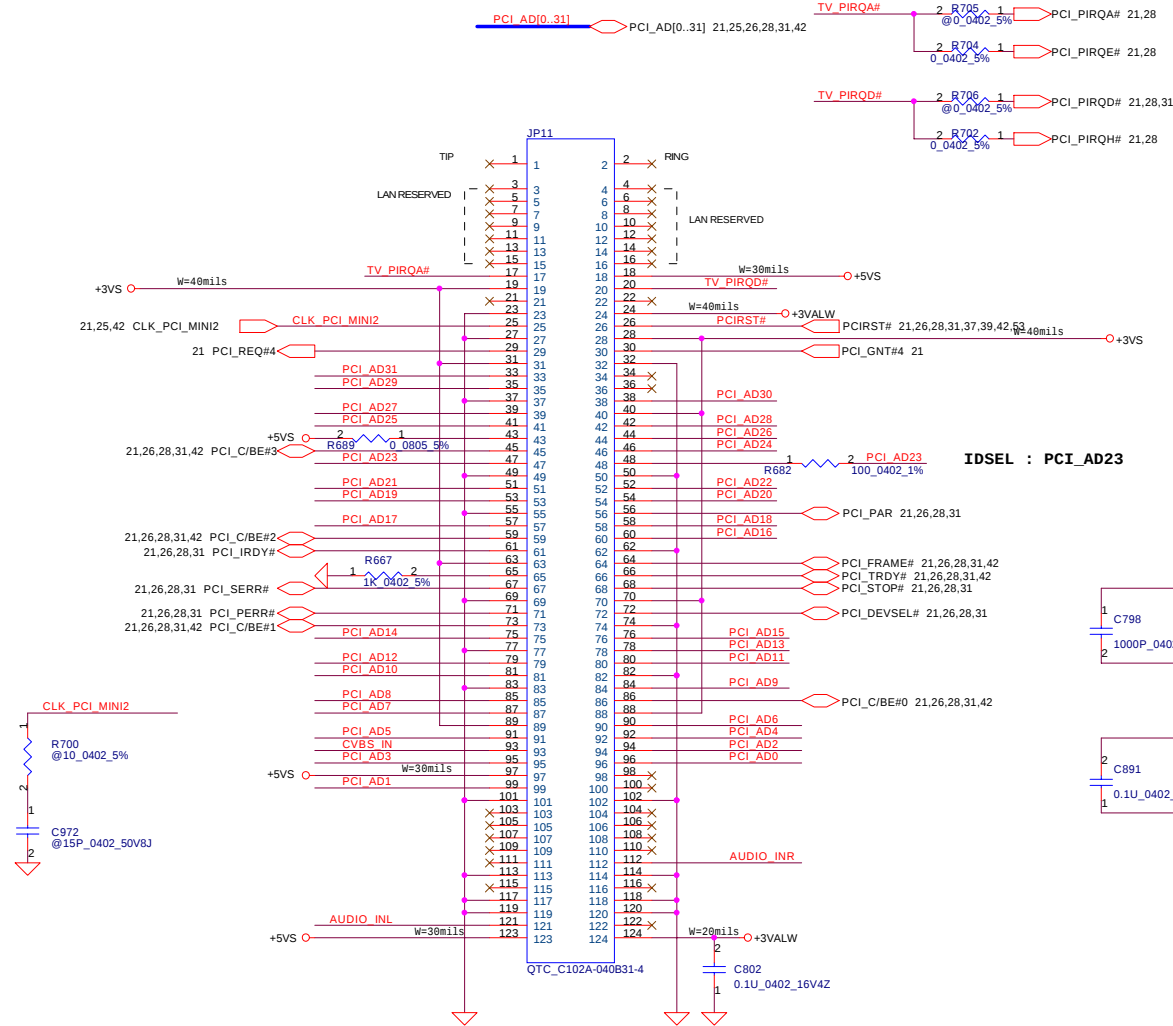


MINI PCI 1 SOCKET FOR WLAN (BOTTOM)



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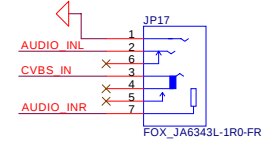
MINI_PCI 2 SOCKET FOR TV TURNER (TOP)



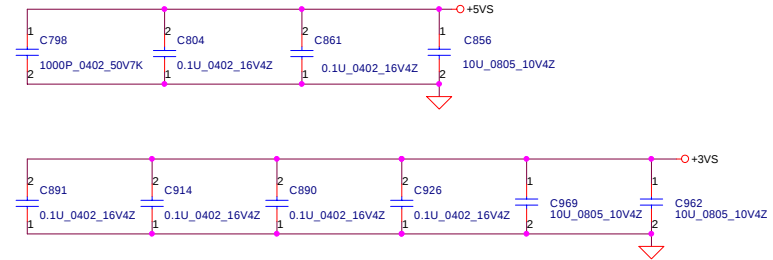
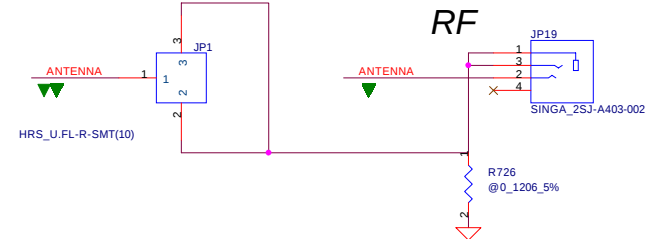
IDSEL : PCI_AD23

TV-Tuner

AV IN



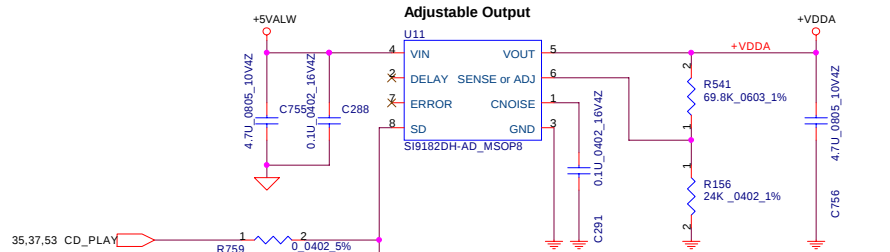
RF



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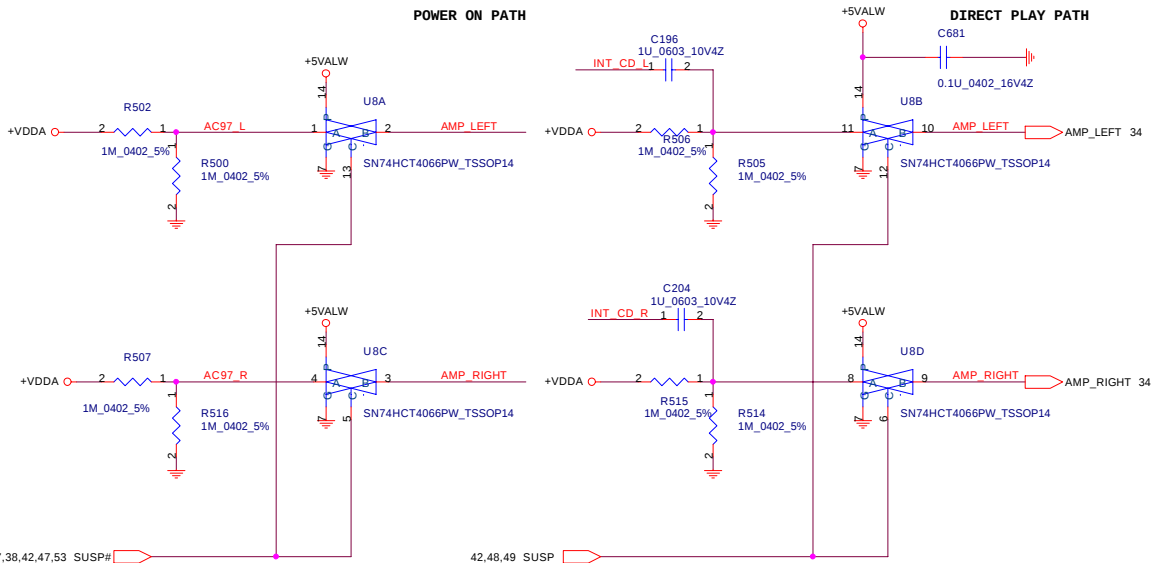
Title			MINI_PCI-TV Tuner
Size	Document Number	Rev	
Customer	Longbeach 100 <LA-2451>	0.1	
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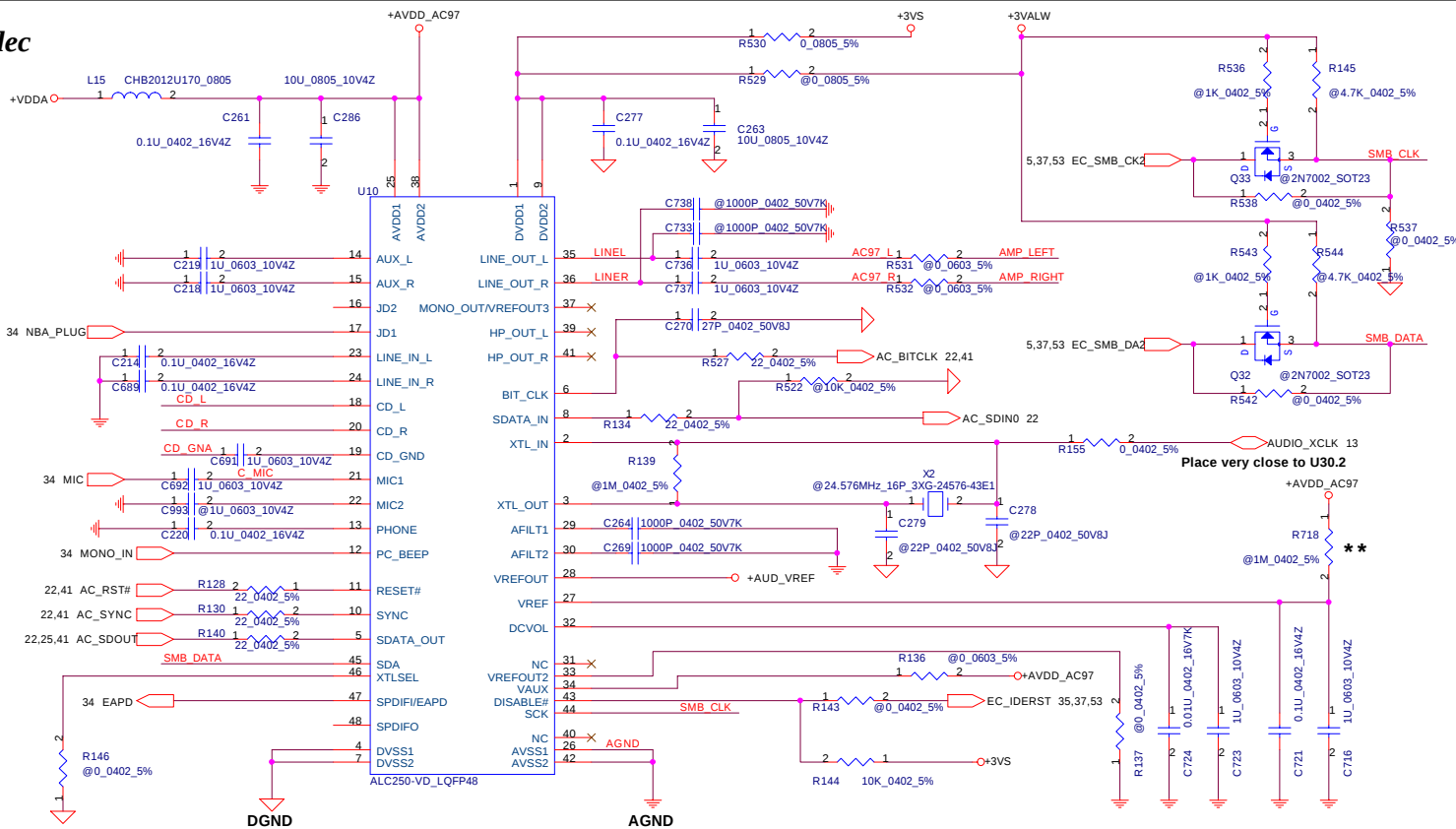


DEFAULT (WITH 4066)
U0 R0 R7 R8 R9 R10 R11 R12 R13 R14 C1 C2 C3 POP
Q1 Q2 R1 R2 R3 R4 R5 R6 DEPOP

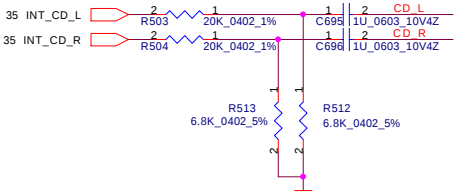
S3 (WITHOUT 4066)
Q1 Q2 R1 R2 R3 R4 R5 R6 POP
U1 R0 R7 R8 R9 R10 R11 R12 R13 R14 C1 C2 C3 DEPOP



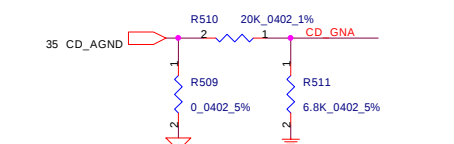
AC97 Codec



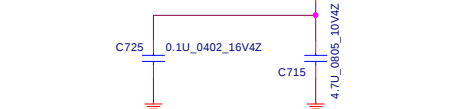
Audio Signal Bias Circuit



CD_AGND To CD_GNA Bypass



Analog Reference V



DGND To AGND Bypass



WITH 14.318MHz : Rxxx POP
WITH 24.576MHz : Rxxx DEPOP

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AC97 Codec			
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R161, R557	
2 AMP	-->1 Ohm
1 AMP	-->0 Ohm



JP13
1
2
ACES_85204-0200

JP12
1
2
ACES_85204-0200

BTL MODE
R522//R525=0.419K
Vmax=0.201V , GAINmax=18db
Vmin=5V, GAINmin=-80db

SE MODE
Vmax=1.53V , GAINmax=-6db
Vmin=5V, GAINmin=-80db

AMP & Audio Jack
 Document Number
 Longbeach 100 <LA-2451>
 Rev 0.1
 Date: 星期三, 九月 01, 2004 Sheet 34 of 53

EC Beep

37,53 BEEP#

C173
1U_0603_10V4Z

R104
560_0402_5%

CardBus Beep

28 PCM_SPK#

C184
1U_0603_10V4Z

R112
560_0402_5%

PCI Beep

22 SPKR#

C163
1U_0603_10V4Z

R99
560_0402_5%

R101
10K_0402_5%

D14
CH751H-40_SC76

System Beep To AC97' Codec

+AVDD_AC97

R131
10K_0402_5%

C253
10U_0805_10V4Z

R129
10K_0402_5%

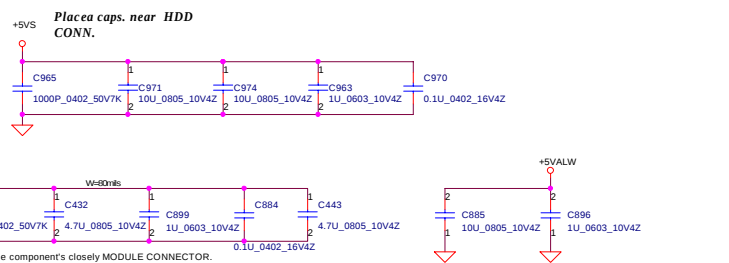
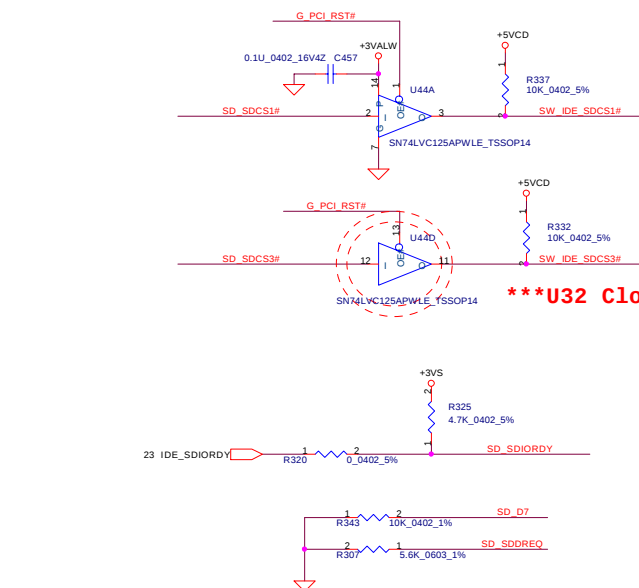
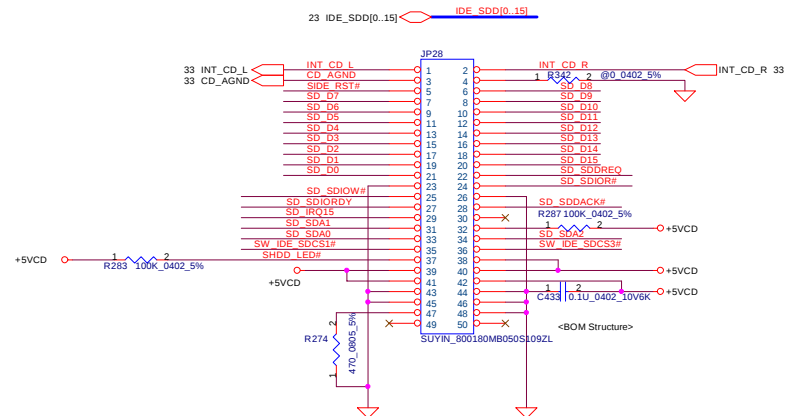
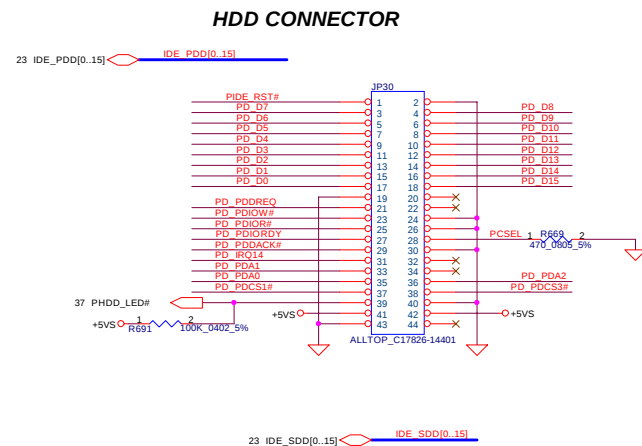
C223
1U_0603_10V4Z

R127
2.4K_0402_5%

MONO_IN 33

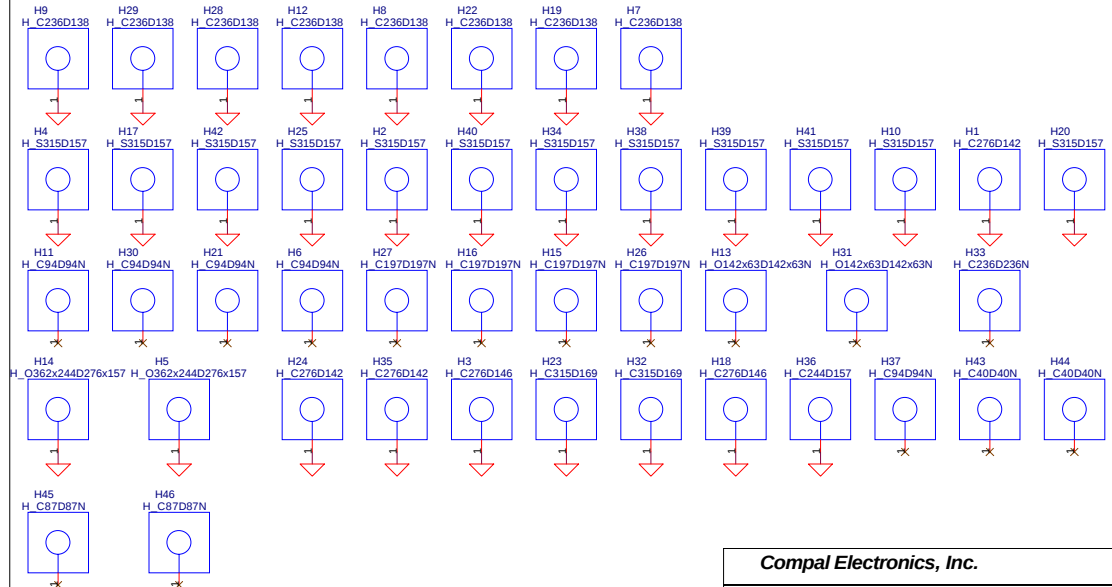
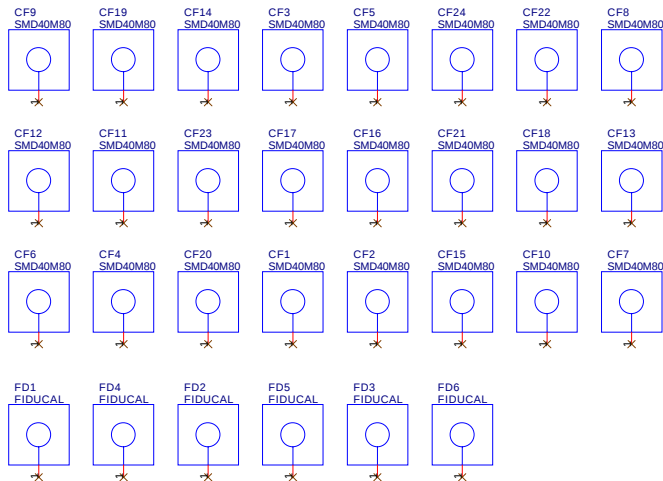
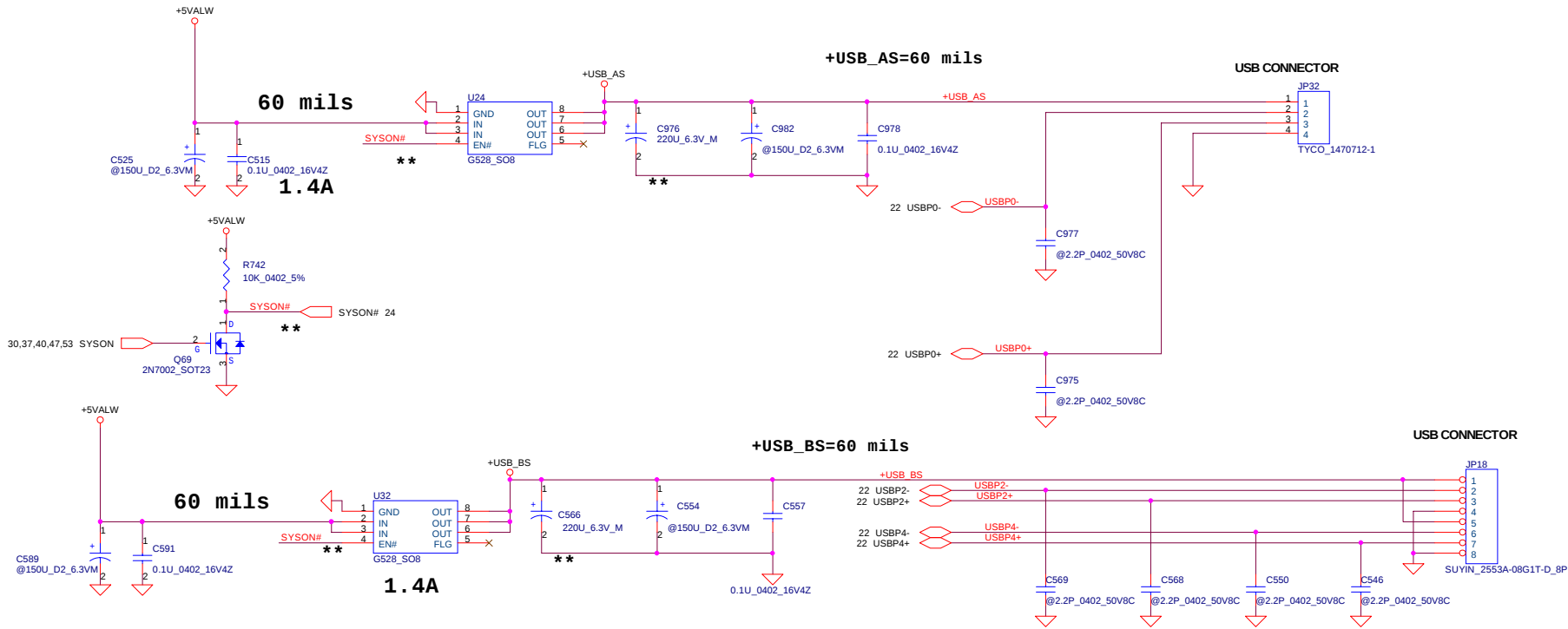
Q11
MMBT3904_SOT23

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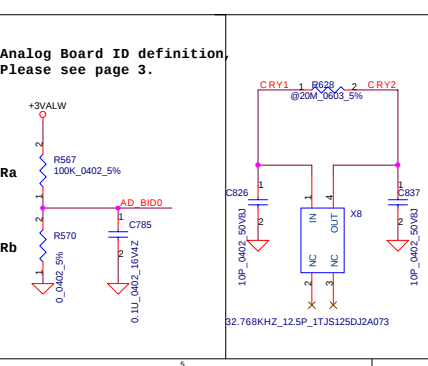
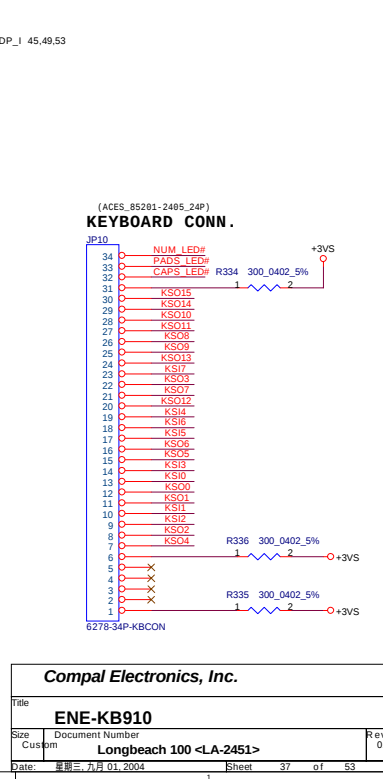
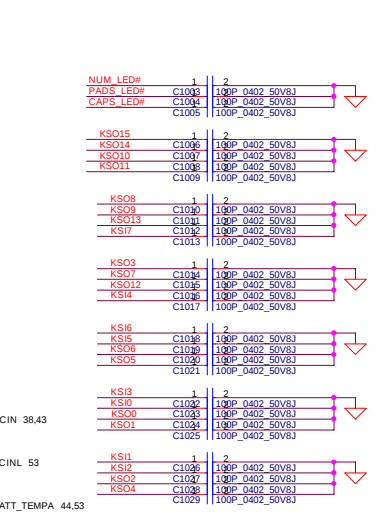
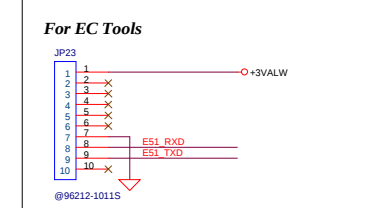
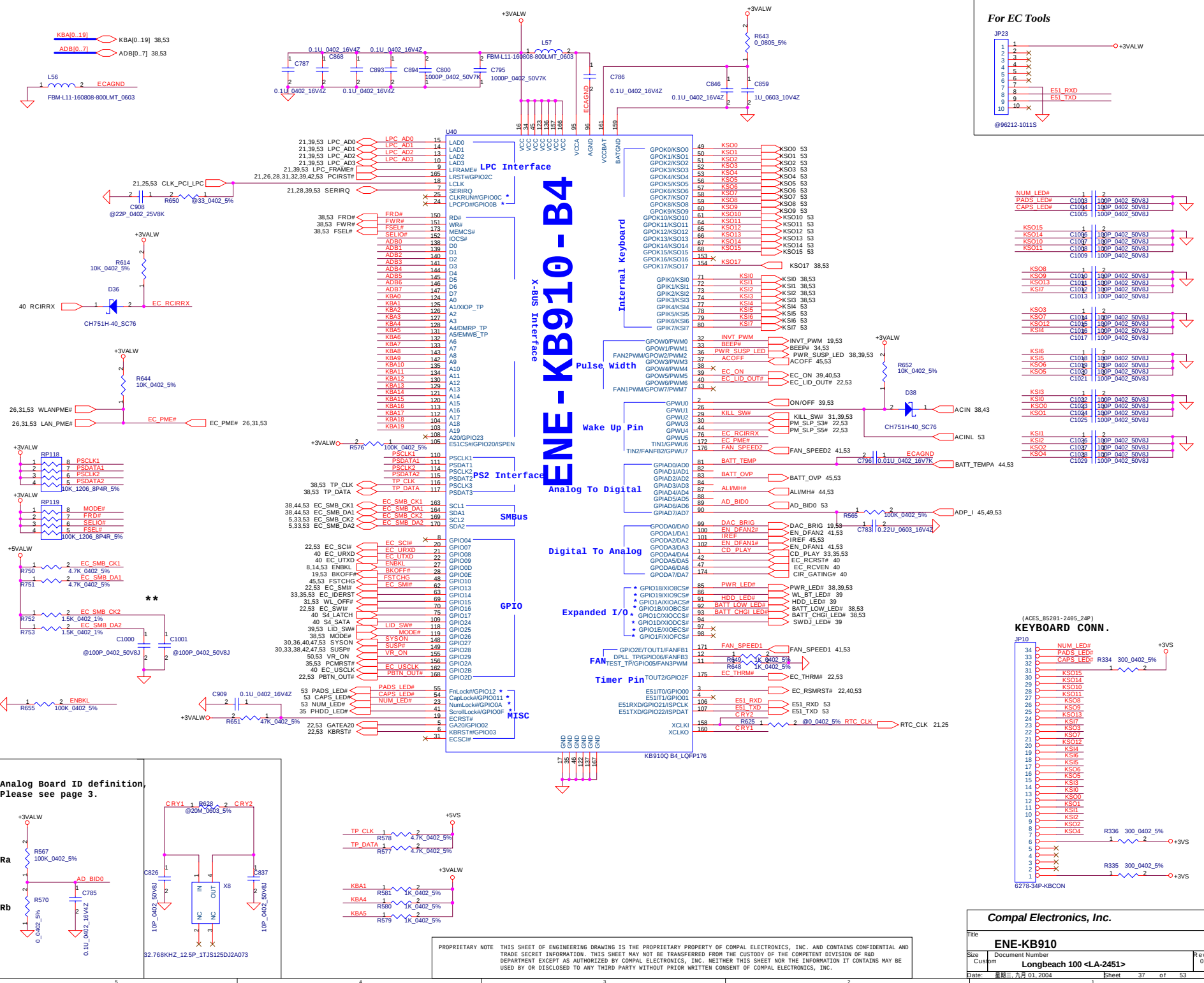
***U32 Close to CD-ROM Side

Keep 20 mils minimum spacing between
USB signals and others signals

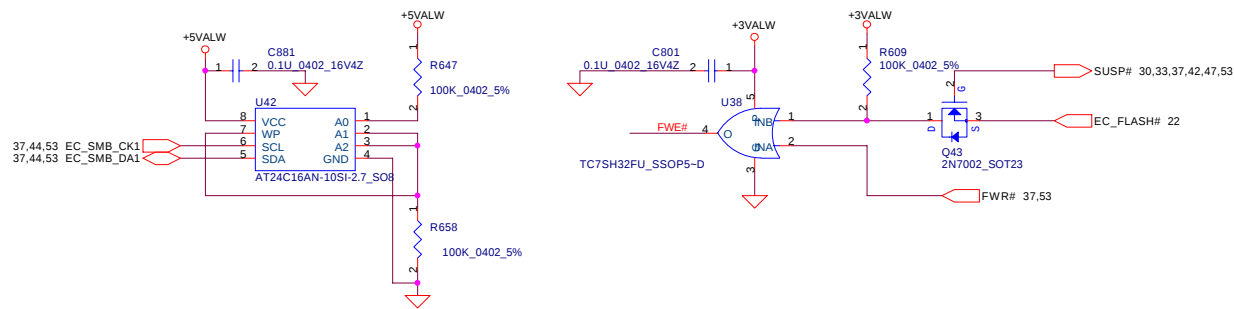


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Title			
USB Conn.			
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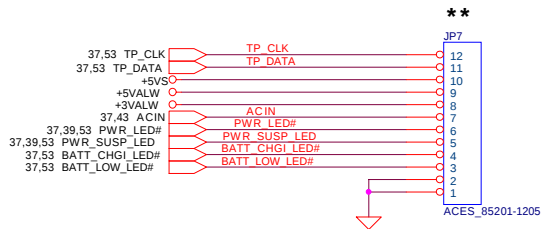
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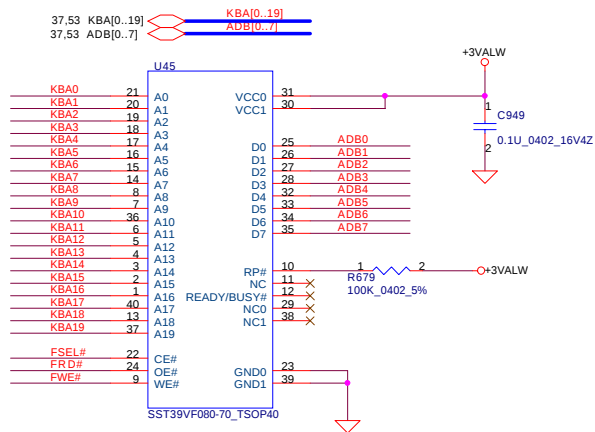
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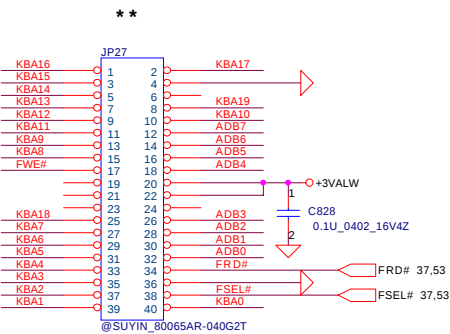
Touch Pad Connector



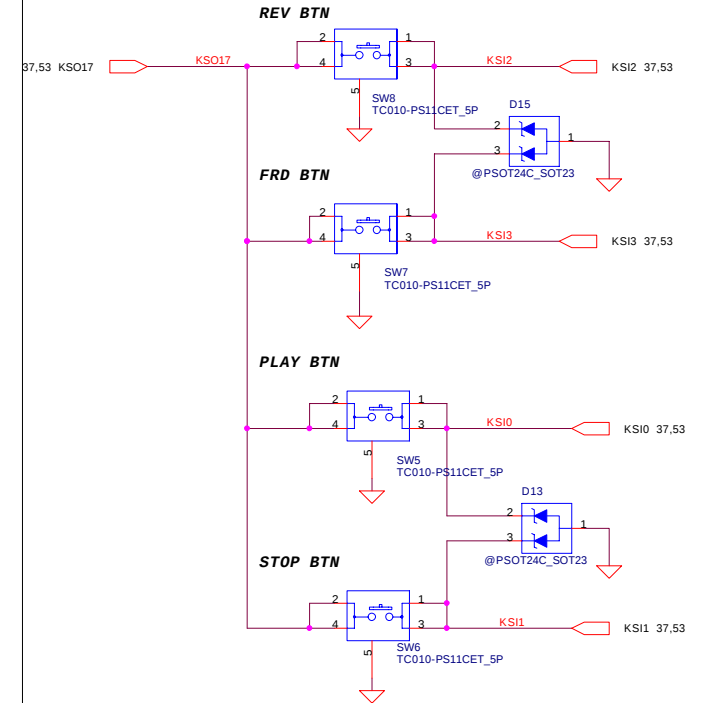
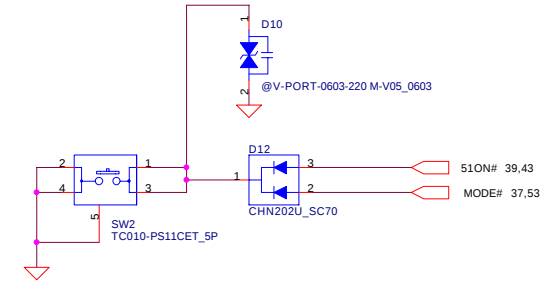
1MB Flash ROM



1MB BIOS Connector



Direct CD button

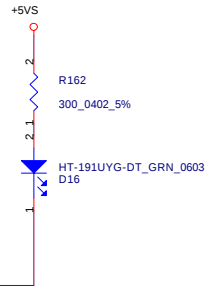


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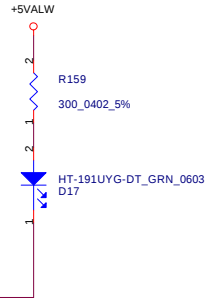
Title			
BIOS & EXT. I/O PORT			
Size	Document Number	Rev	
Custom	Longbeach 100 <LA-2451>	0.1	
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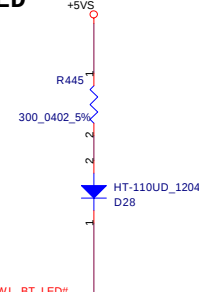
HDD LED



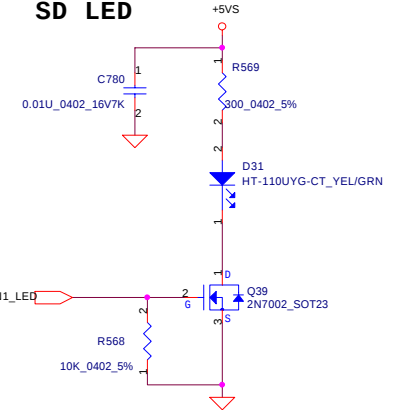
SWDJ LED



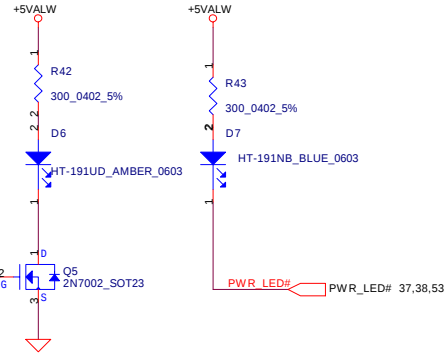
Wireless LED



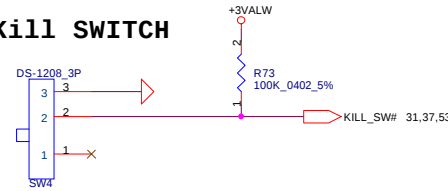
SD LED



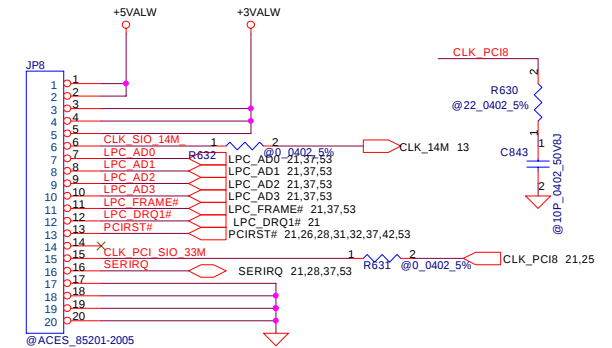
POWER LED



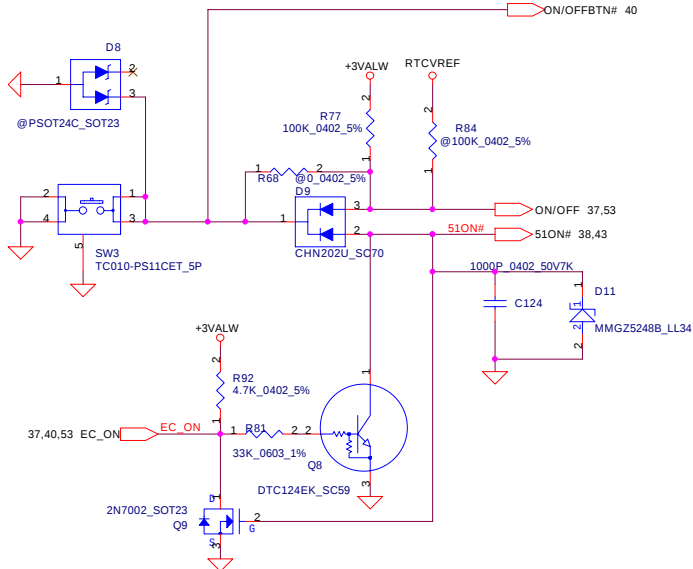
Kill SWITCH



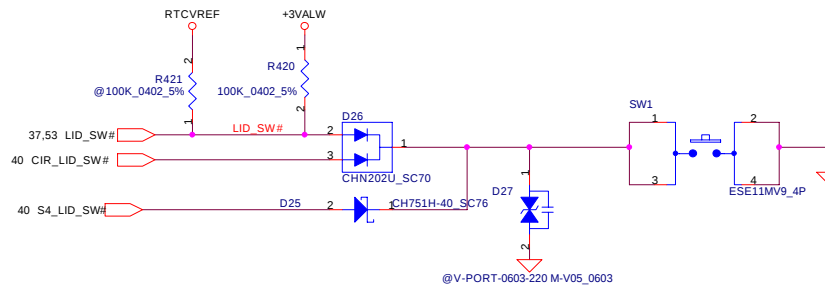
LPC Debug Port



Power Button



LID Switch

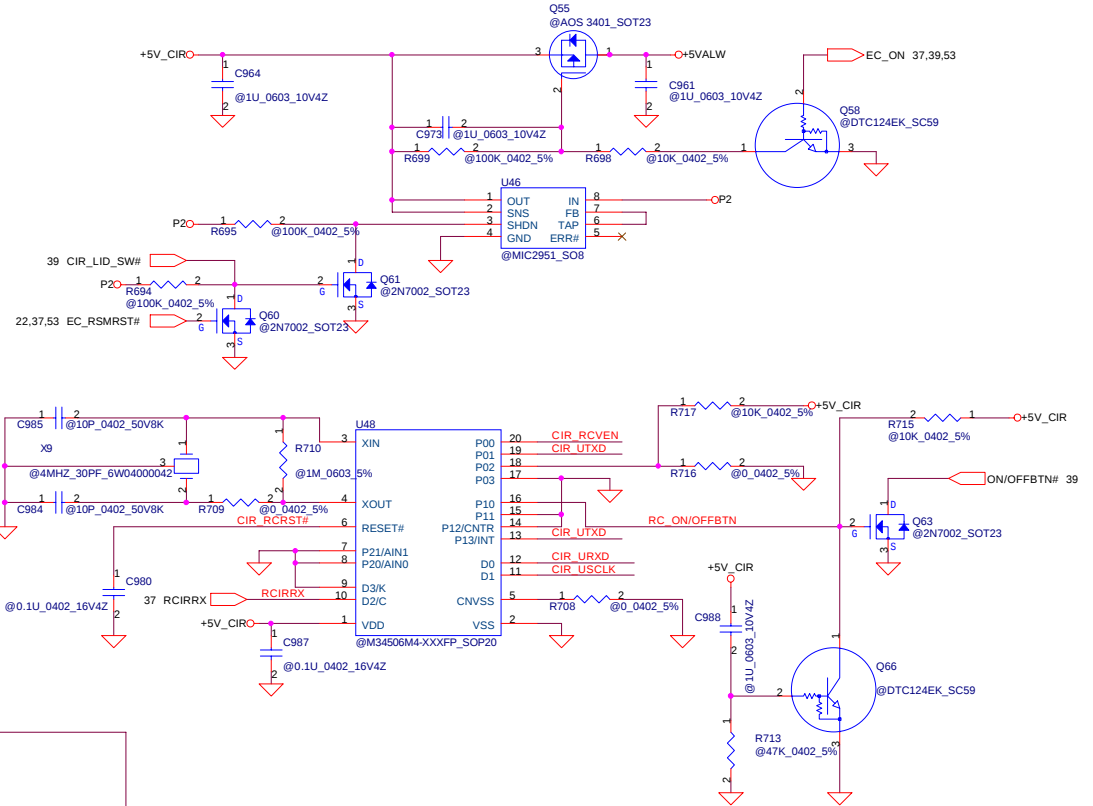
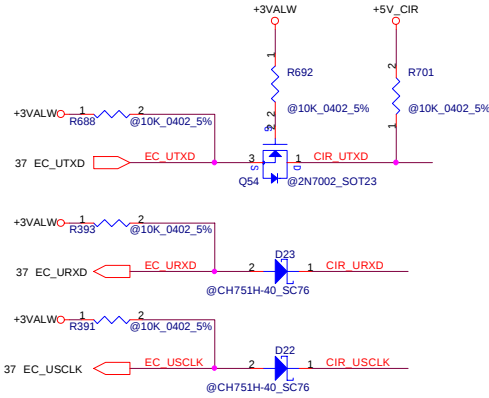


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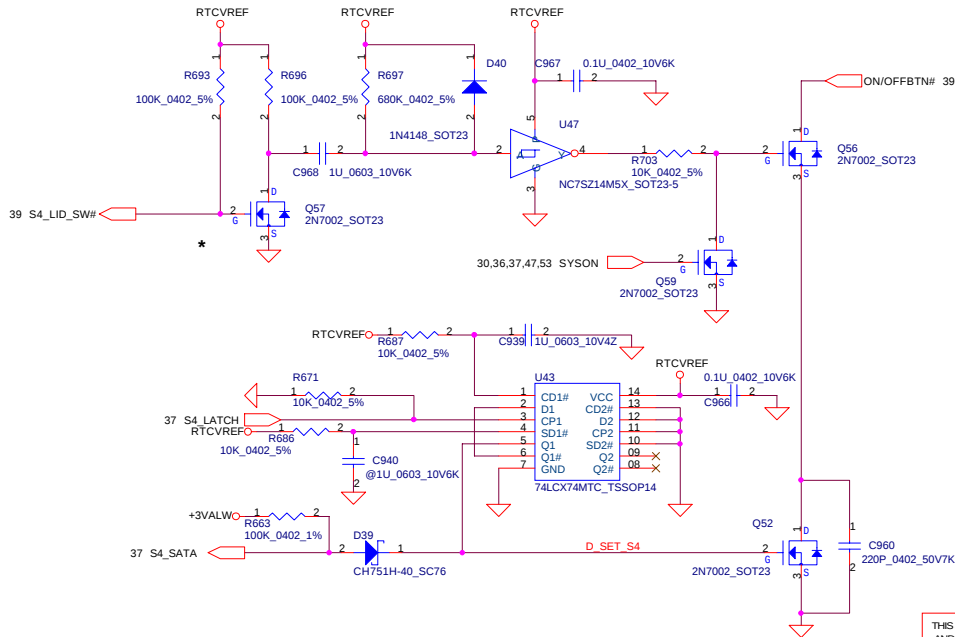
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Switches & Connectors

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Battery mode Hibernation

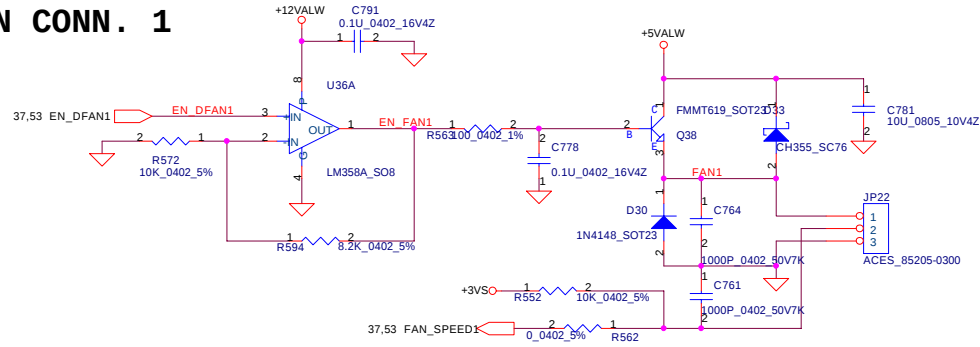


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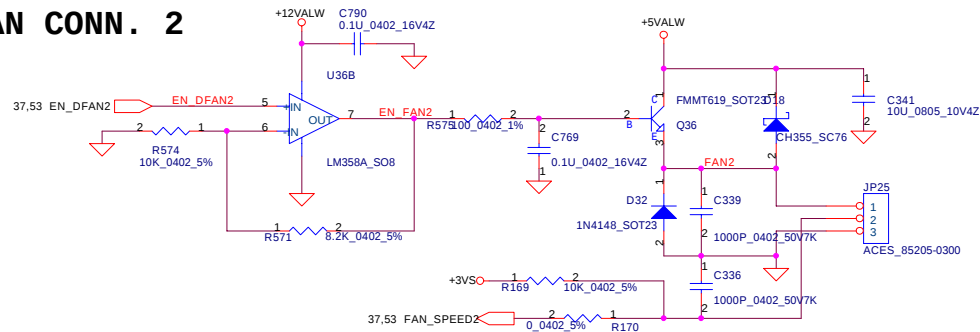
Compal Electronics, Inc.

Title			
CIR & MDC			
Size	Document Number	Rev	
Customer	Longbeach 100 <LA-2451>	0.1	
Date	星期三, 九月 01, 2004	Sheet	40 of 53

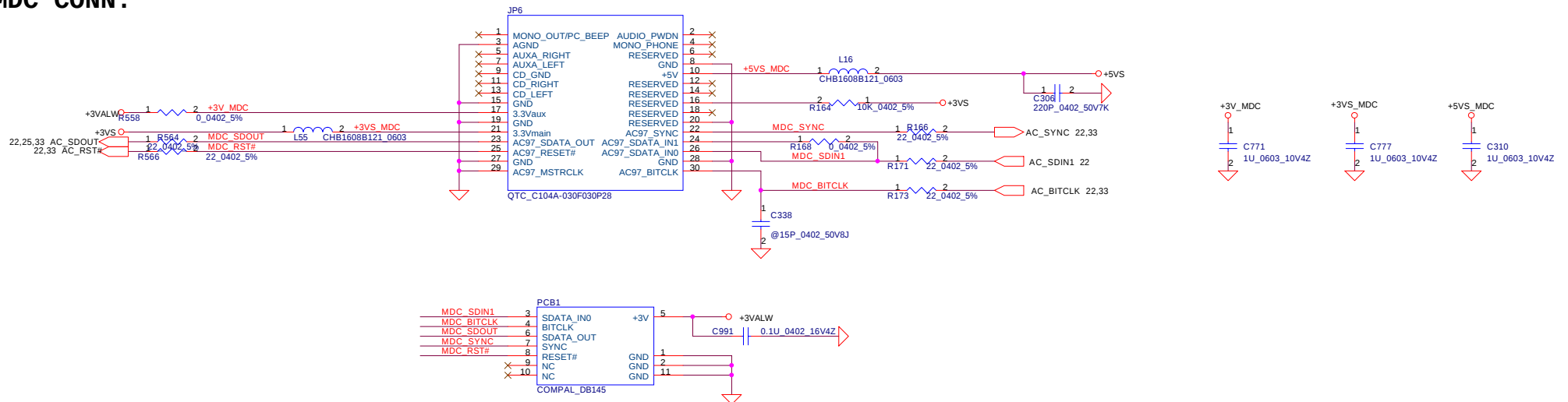
FAN CONN. 1



FAN CONN. 2

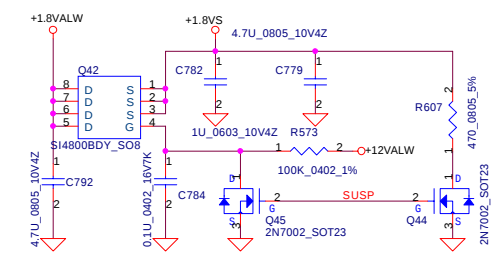


MDC CONN.

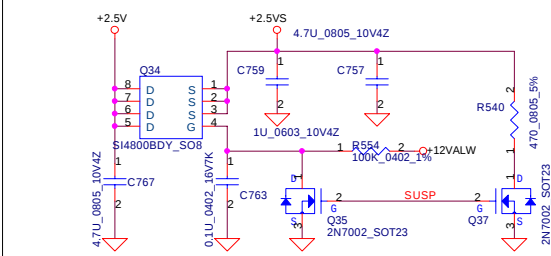


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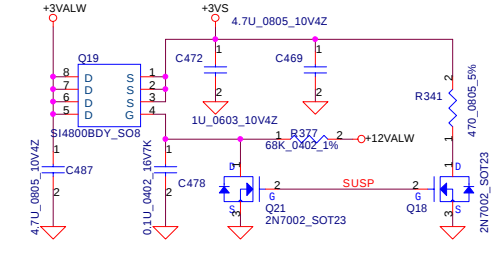
+1.8VALW TO +1.8VS



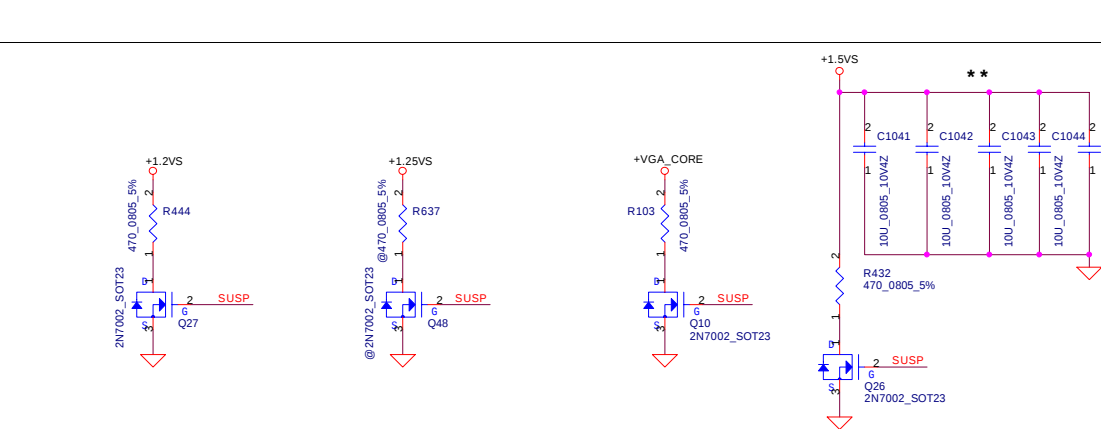
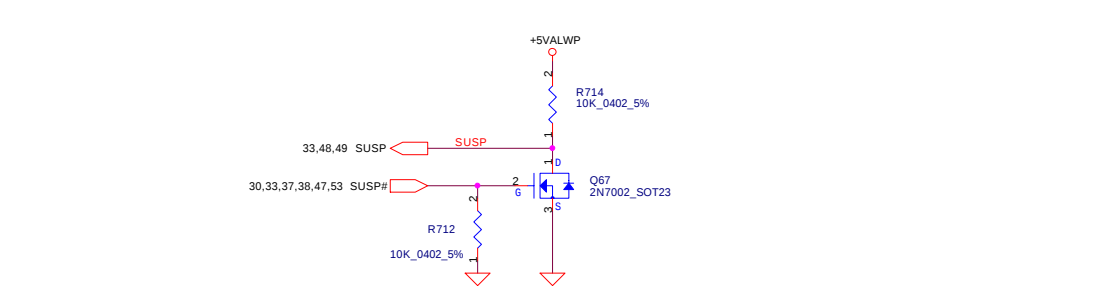
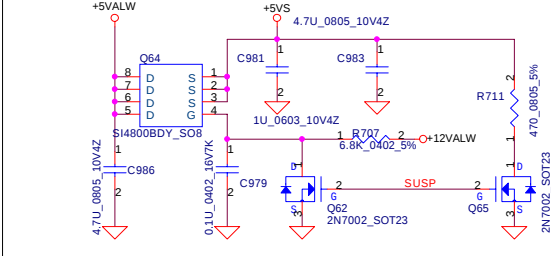
+2.5V TO +2.5VS



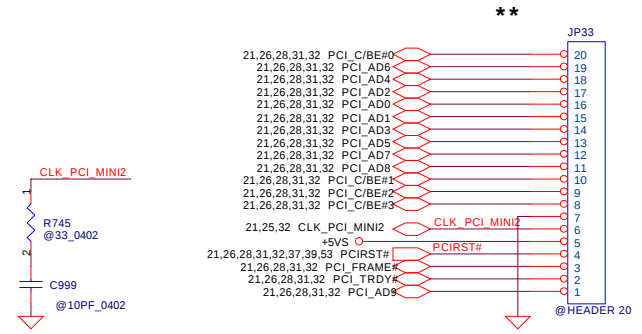
+3VALW TO +3VS



+5VALW TO +5VS

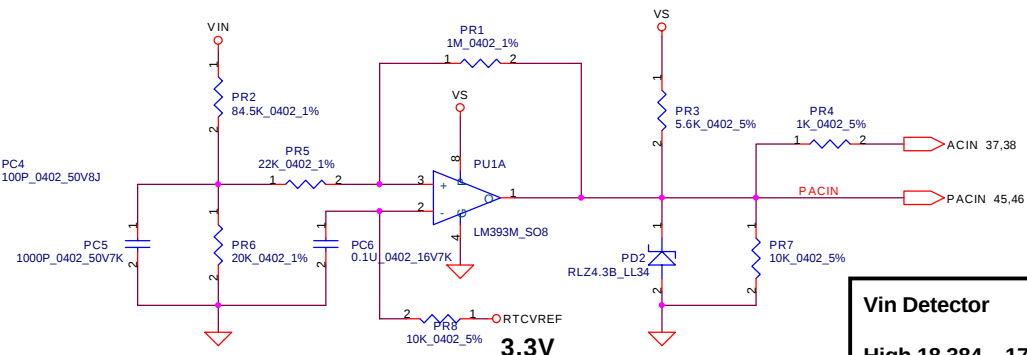


Port 80 Debug Card Connector

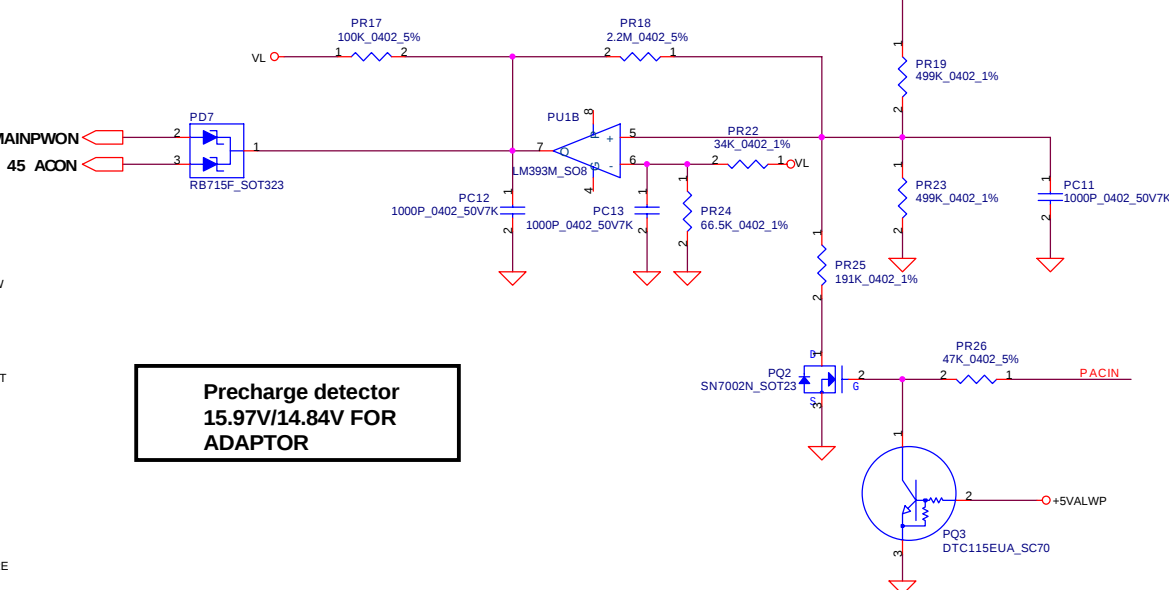
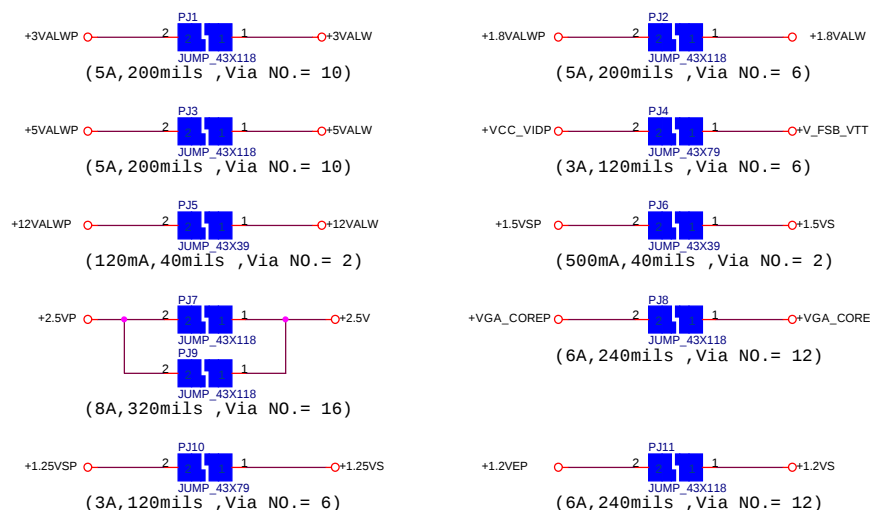
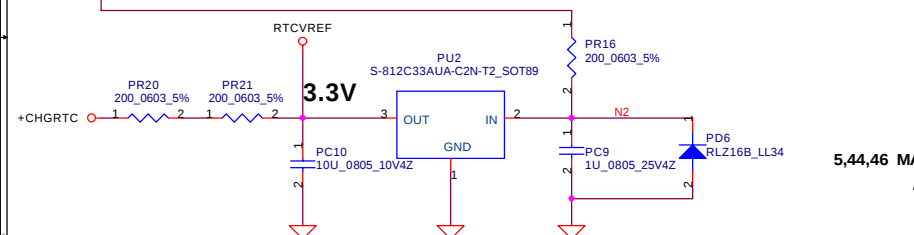
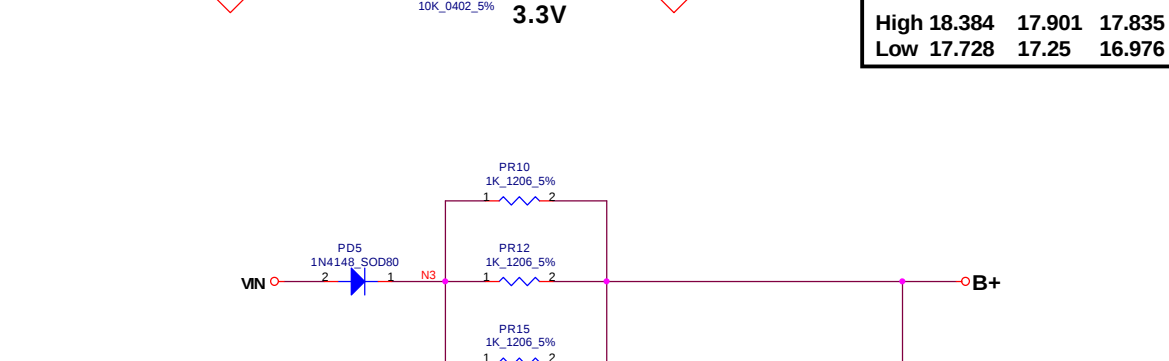


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Title POWER CONTROL CKT			
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Cus	Longbeach 100 <LA-2451>	0.1	
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High	18.384	17.901	17.835
Low	17.728	17.25	16.976



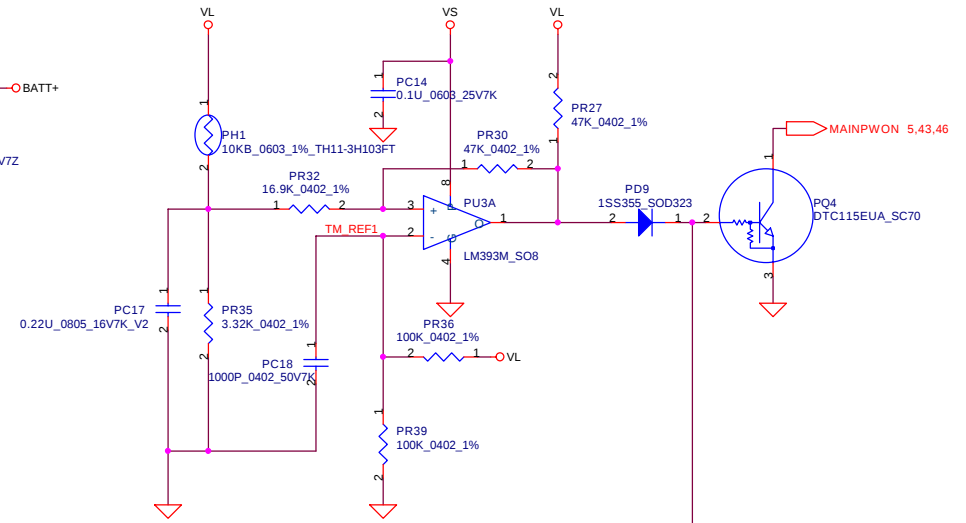
**Precharge detector
15.97V/14.84V FOR
ADAPTOR**

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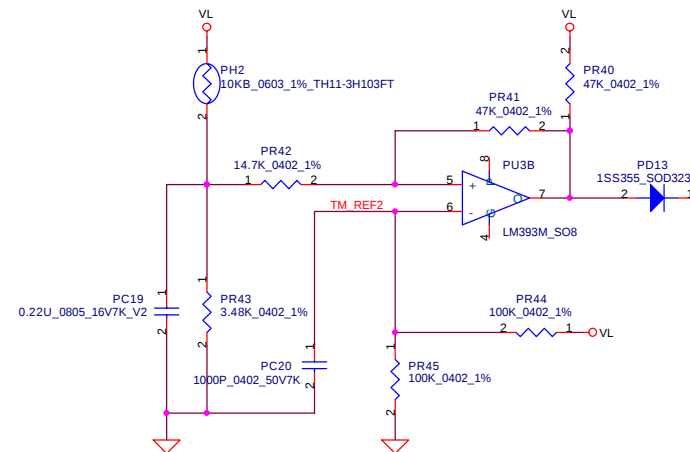
Compal Electronics, Inc.

Title			
DCIN & DETECTOR			
Size	Document Number		Rev
	Longbeach100		0.1
Date:	~P 陽三、九月 01, 2004		Sheet 43 of 53

PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C



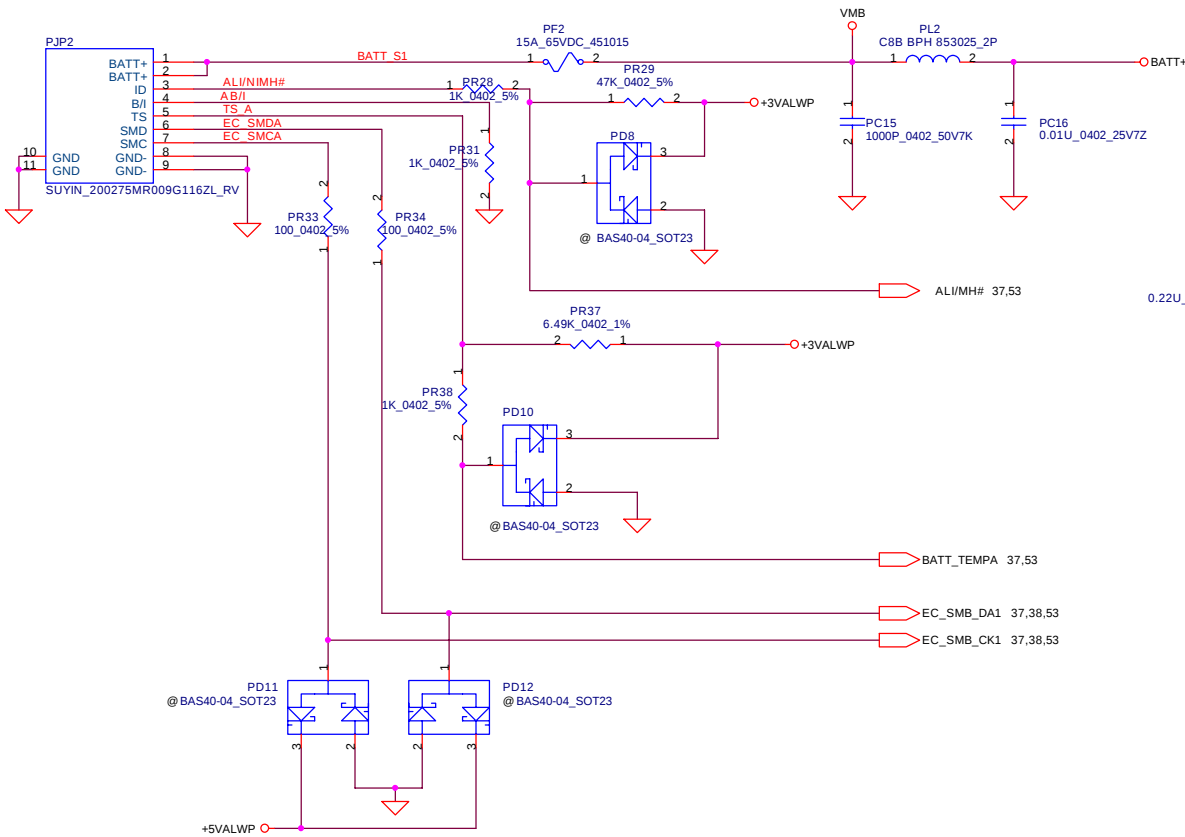
PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C

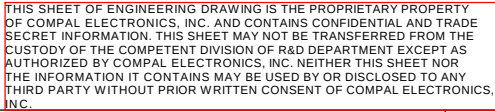


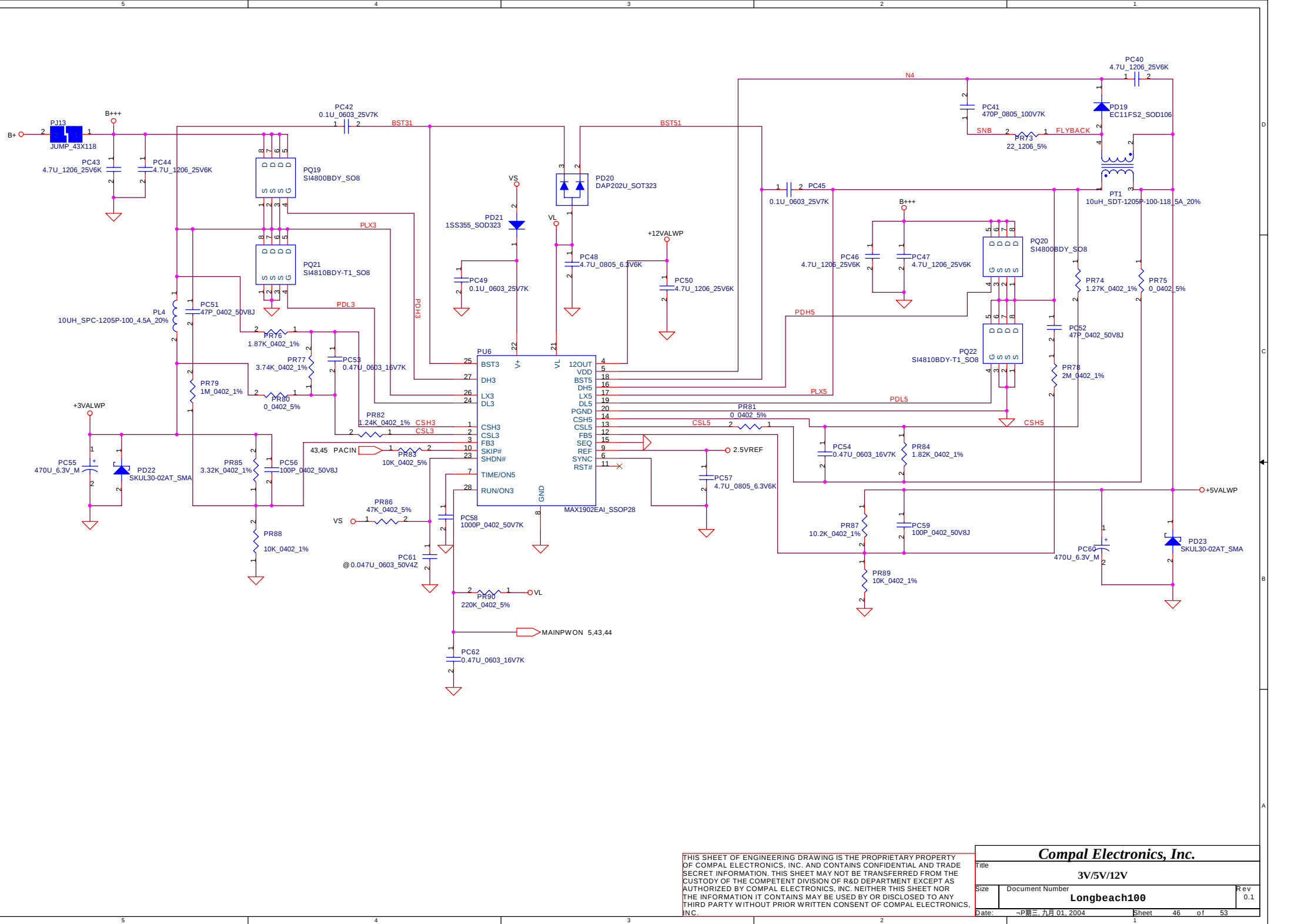
Compal Electronics, Inc.

Title				
BATTERY CONN /OTP				
Size	Document Number			Rev
	Longbeach100			0.1
Date:	~P版三, 九月 01, 2004		Sheet	44 of 53

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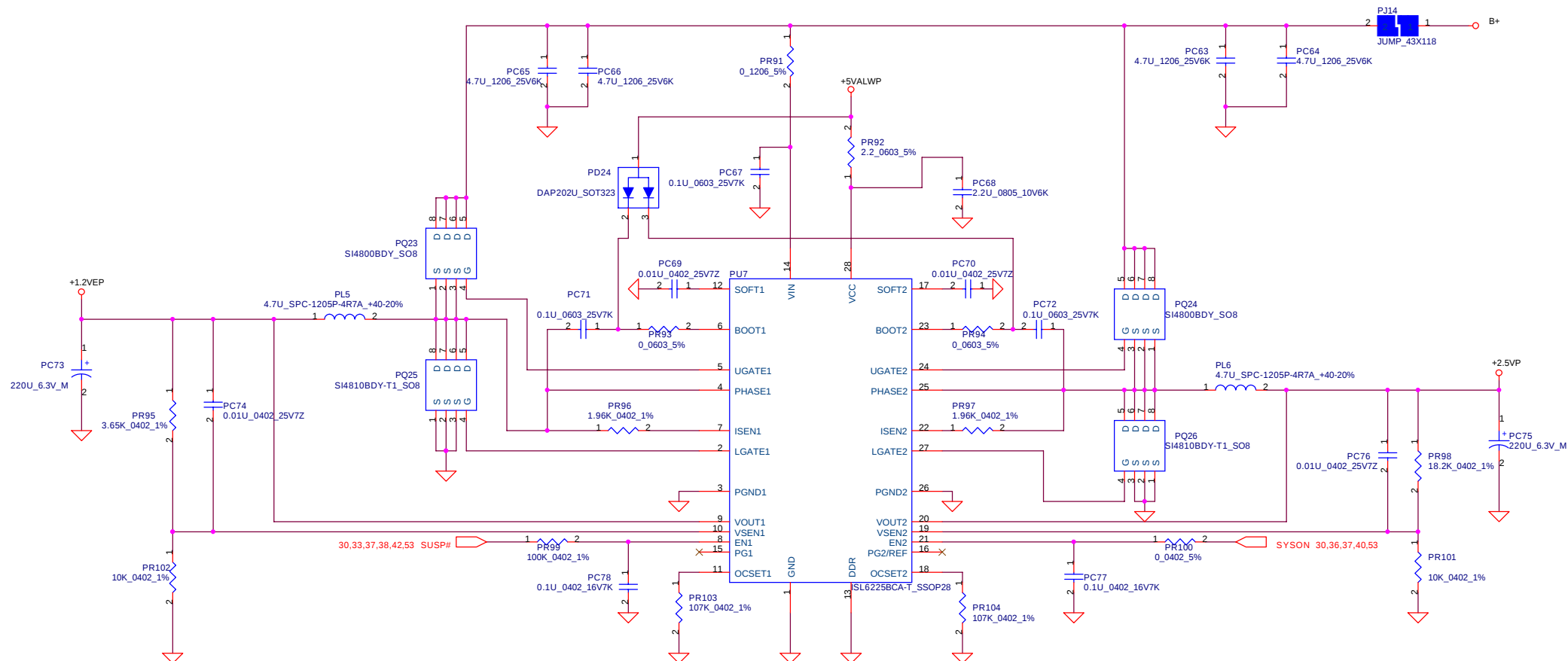




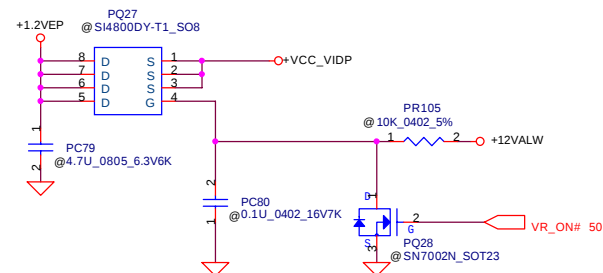


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Title			3V/5V/12V		
Size			Longbeach100		
Date:			~P期三, 九月 01, 2004		
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Rev			0.1		

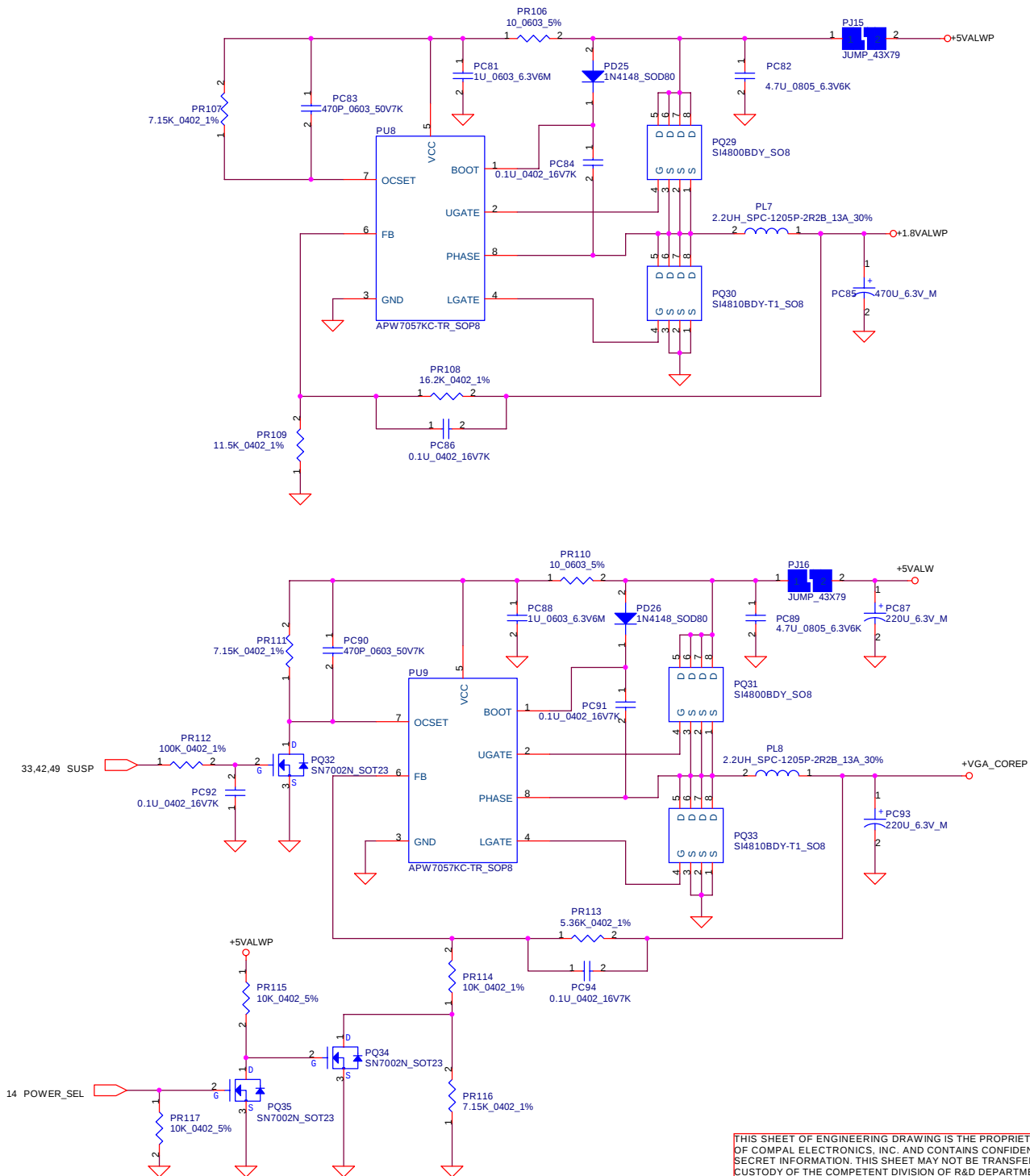


+1.2VEP TO +VCC_VIDP



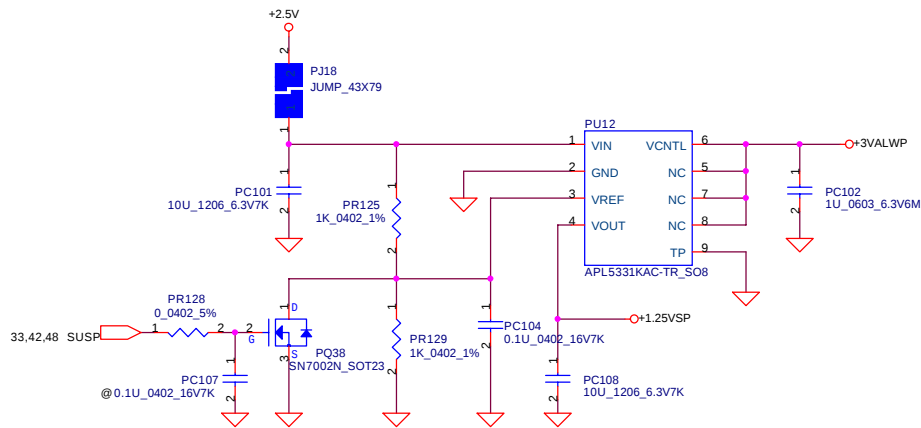
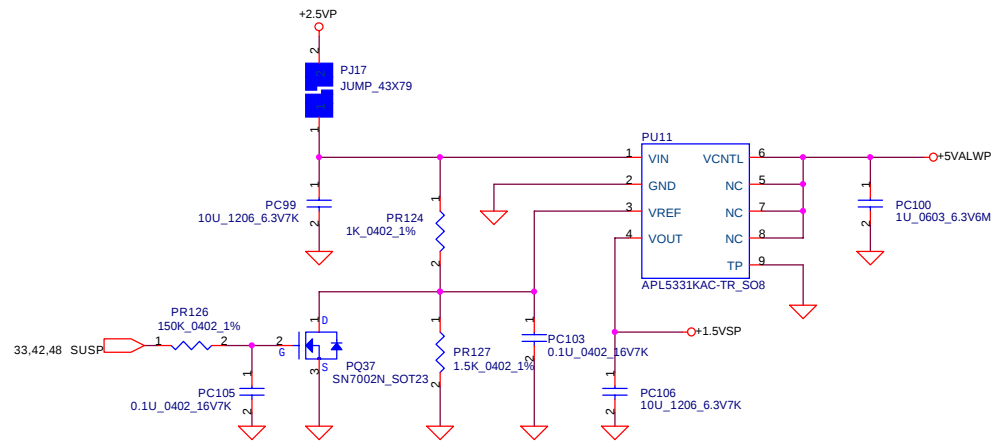
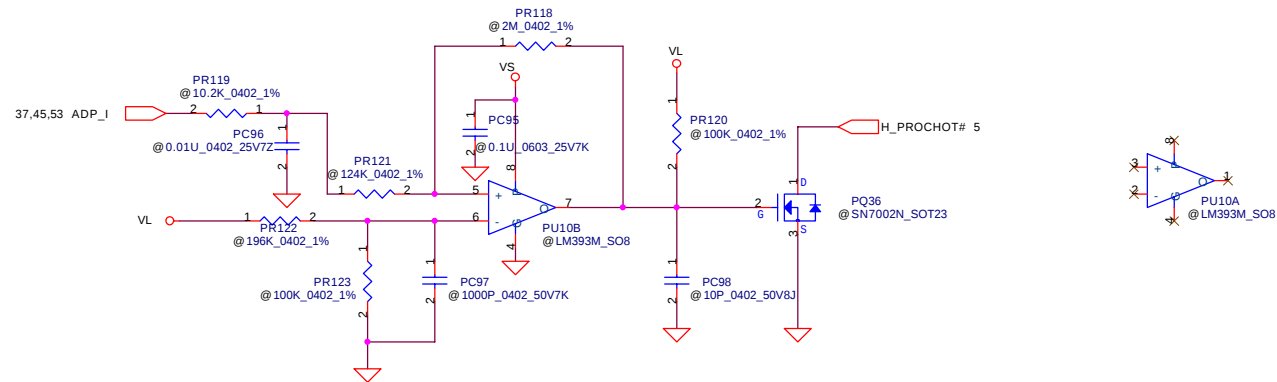
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Compal Electronics, Inc.			
Title		DDR_2.5V/1.2VEP	
Size	Document Number	Longbeach100	
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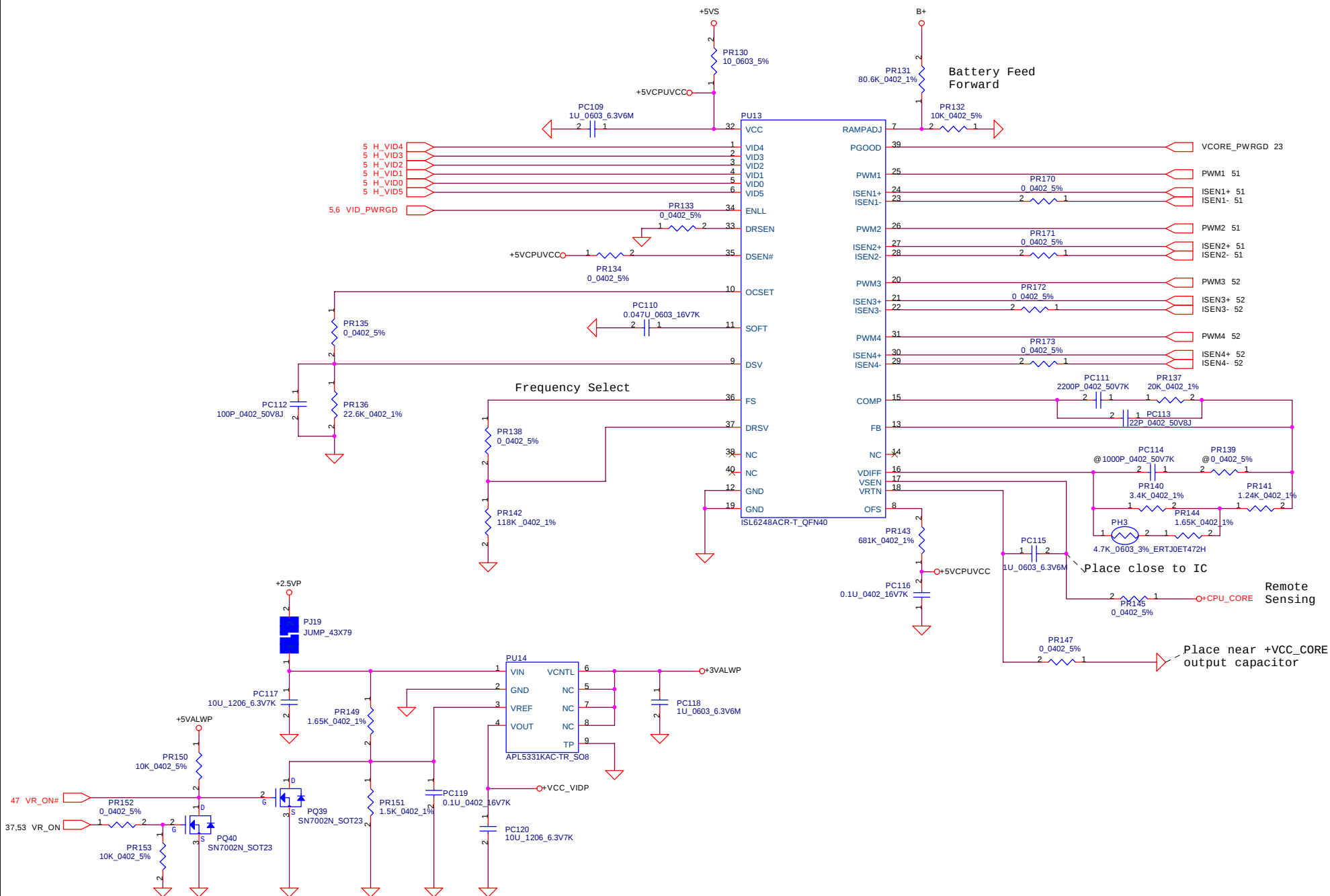
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Compal Electronics, Inc.			
Title		1.8V/VGA	
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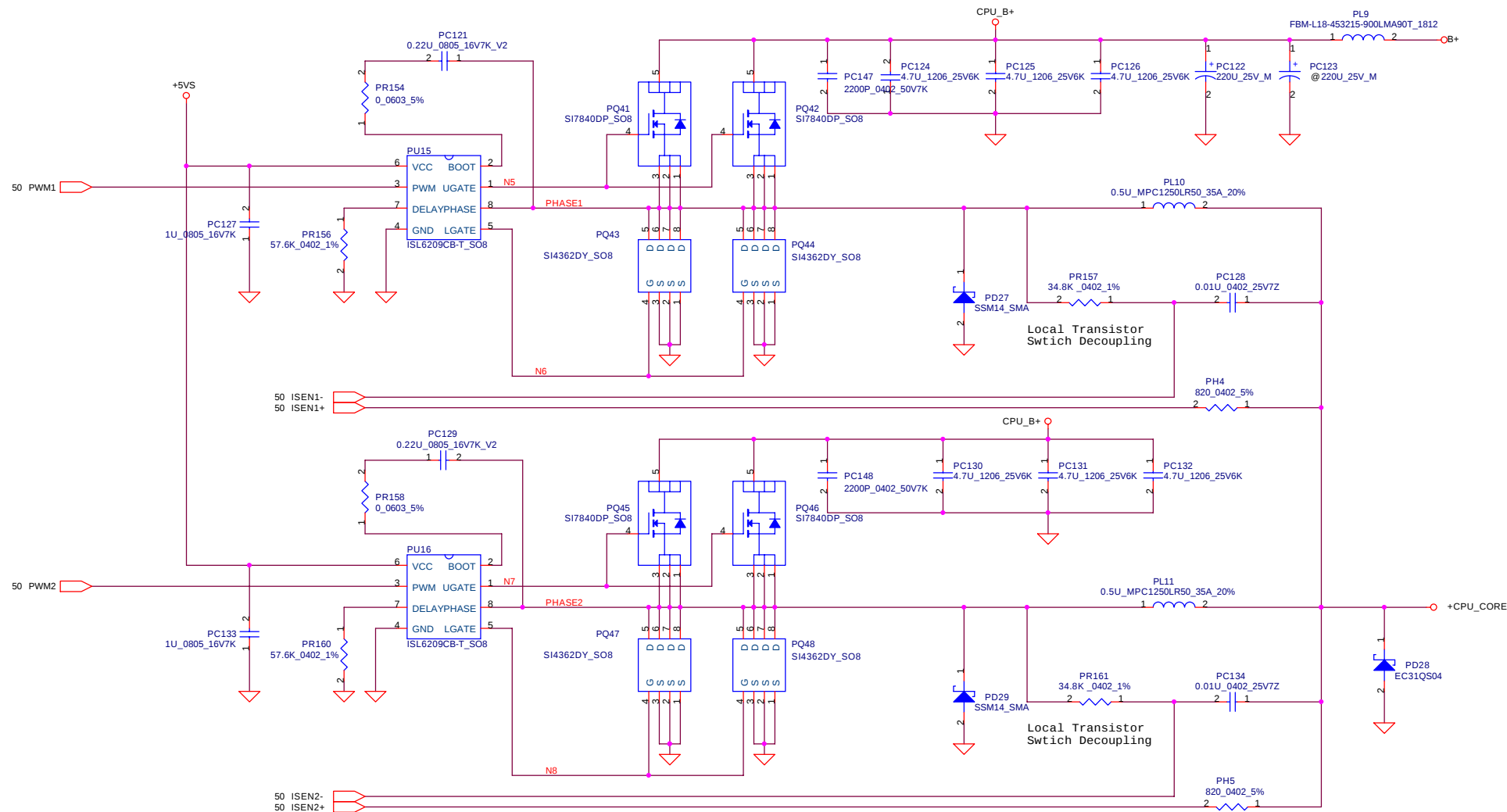
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Compal Electronics, Inc.			
Title		1.5V/1.25V/PROCHOT	
Size	Document Number	Longbeach100	
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Compal Electronics, Inc.			
Title			
CPU_CORE (1)			
Size	Document Number		Rev
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Compal Electronics, Inc.			
Title			
CPU_CORE (1)			
Size	Document Number		Rev
	Longbeach100		0.1
Date:	-P 星期三, 九月 01, 2004		Sheet 51 of 53

