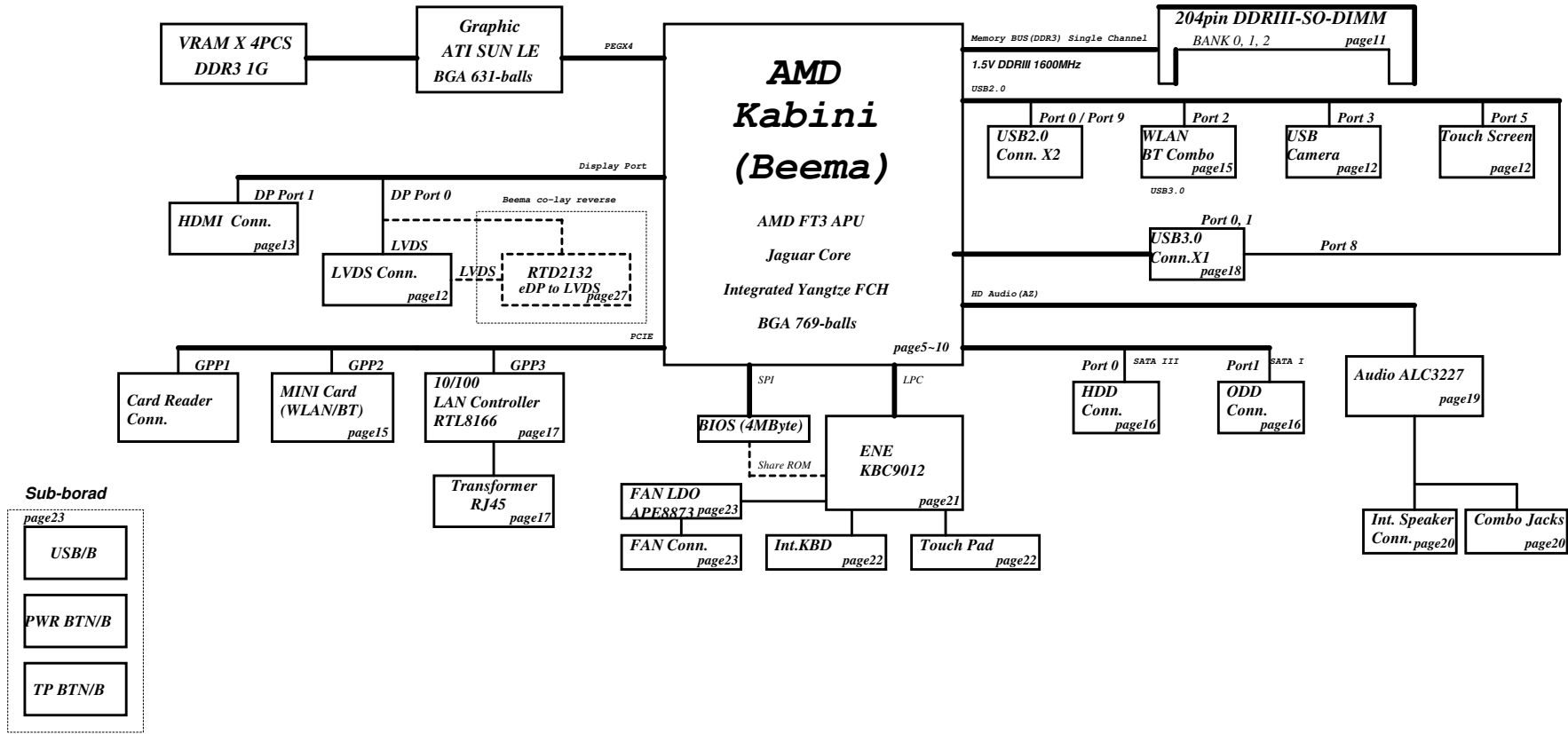
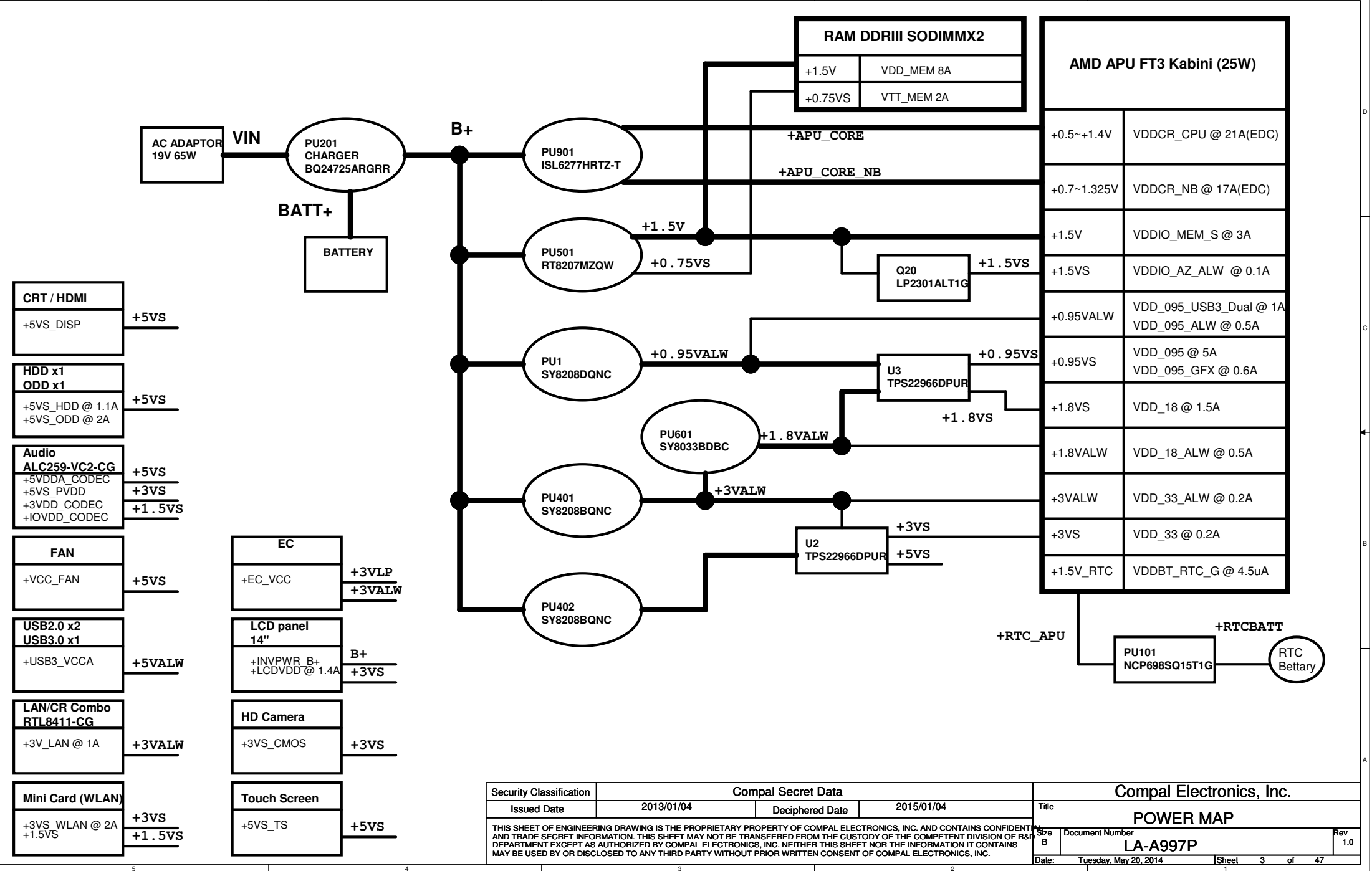






Voltage Rails

[illegible]

SIGNAL STATE	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD
0	0	0.000 V	0.000 V	0.300 V	0x00 - 0x0B
1	12K +/- 1%	0.347 V	0.354 V	0.360 V	0x0C - 0x1C
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3B
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3C - 0x46
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x47 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64

BOARD ID Table

Board ID	PCB Revision
0	EVT
1	
2	
3	
4	
5	
6	
7	

SMBus List

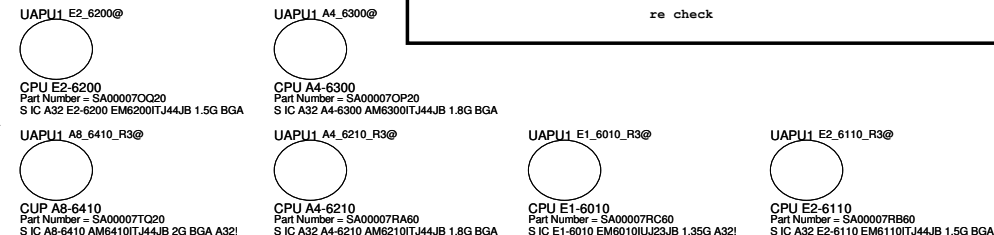
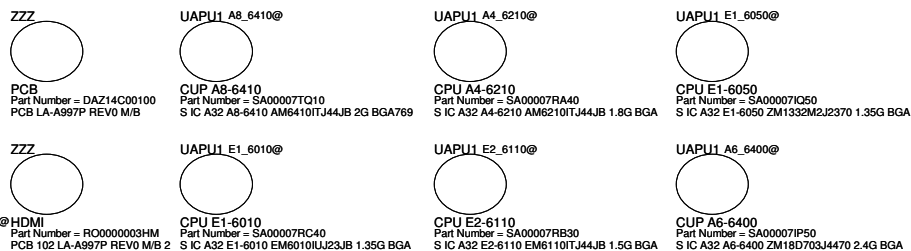
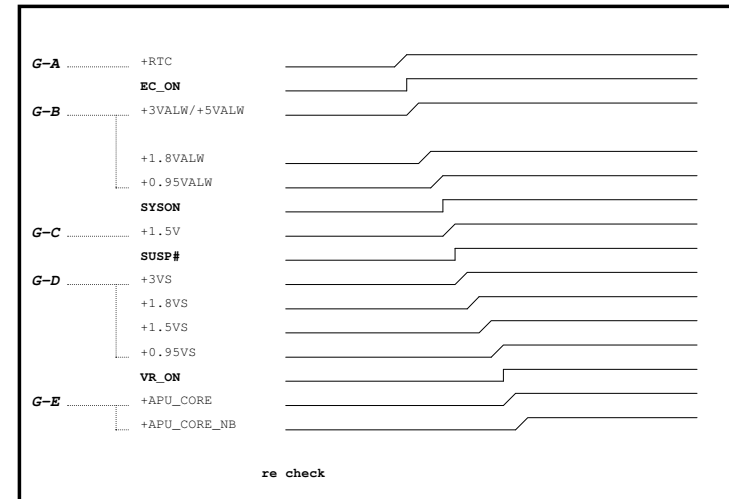
EC SMBus Port1 (+3VALW)			EC SMBus Port2 (+3VS)		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	SB-TSI (APU)	1001 100X b	98H

APU SMBus Port0 (+3VS)			APU SMBus Port1(+3VALW)		
Device	Address	HEX	Device	Address	HEX
DDR DIMM2	1010 000Xb	A0H			
DDR DIMM1	1010 001Xb	A2H			
Mini Card (DNI)					

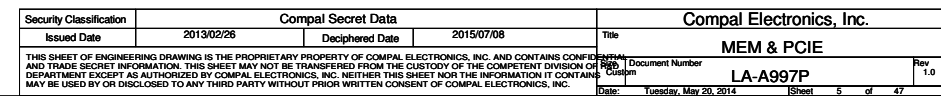
BOM Structure Table

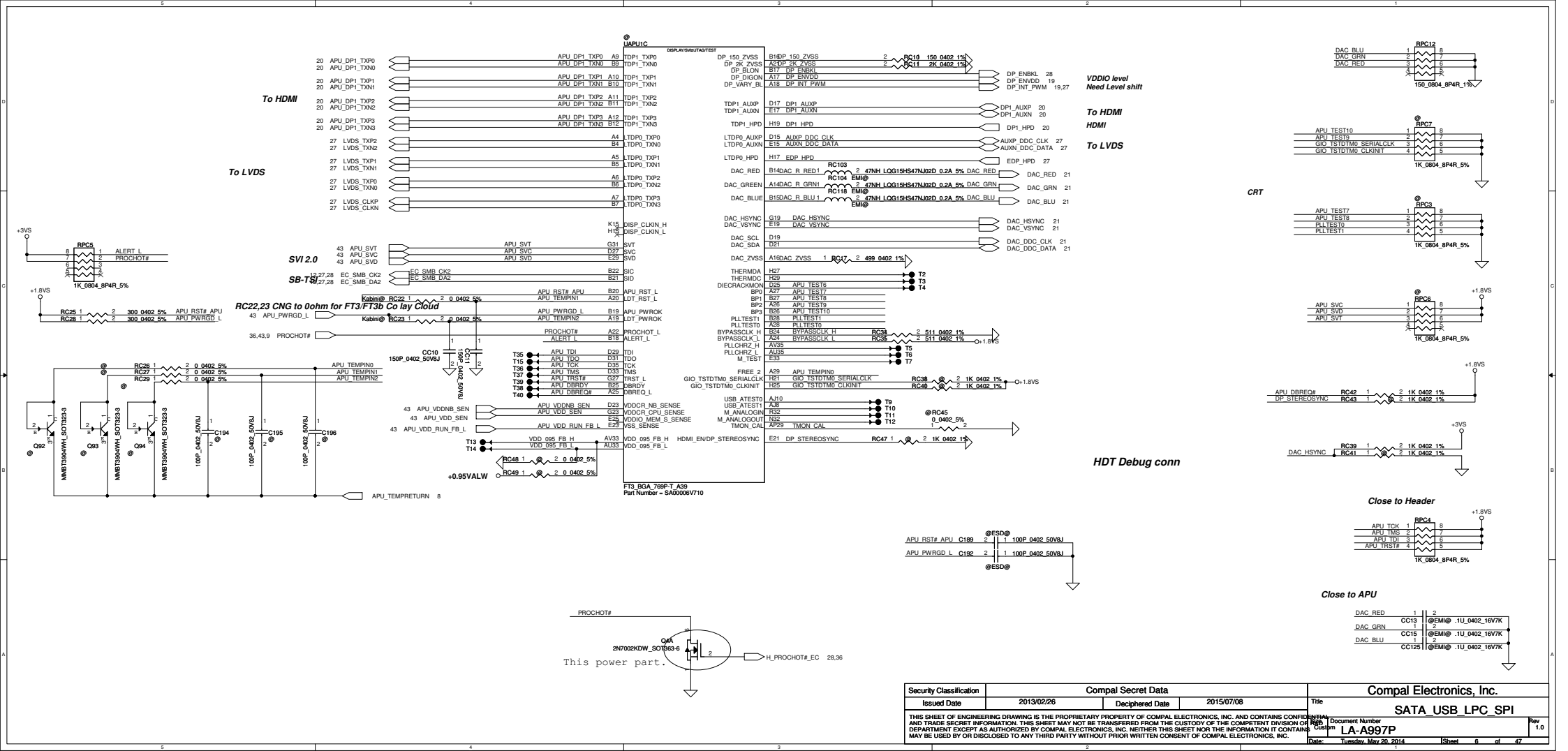
BOM Structure	BTO Item
@	Unpop
CONN@	Connector Part Control by ME
EMI@	EMI pop component
@EMI@	EMI unpop component
ESD@	ESD pop component
@ESD@	ESD Unpop component
eDP@	eDP Panel
LVDS@	LVDS Panel
AL@	Auto Load EC ROM
DB@	Debug only, remove at MP

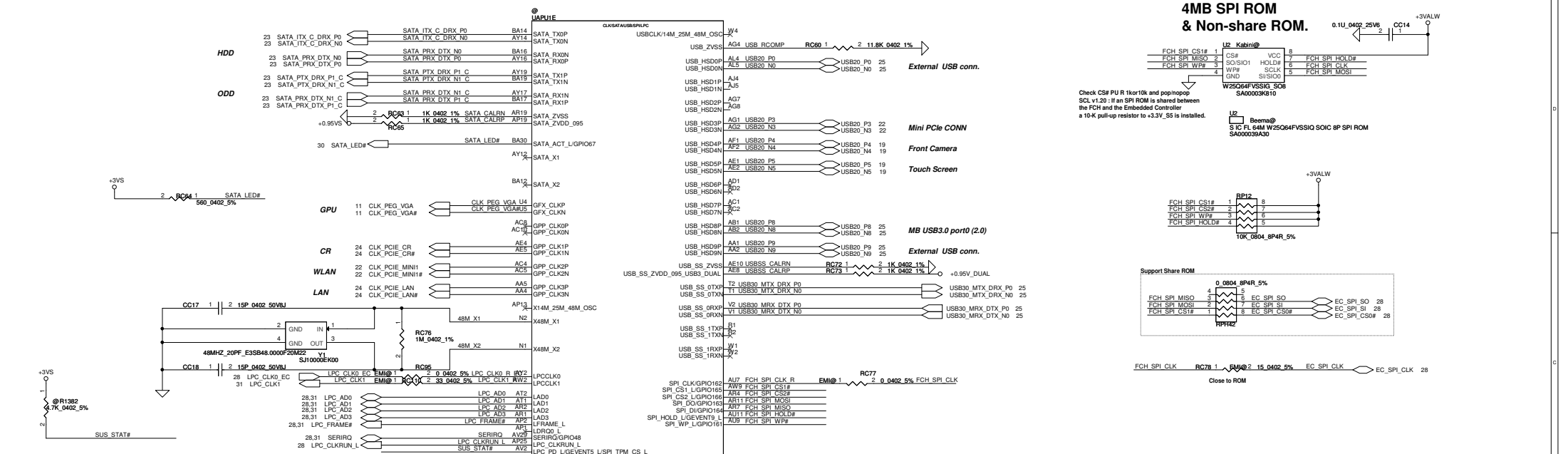
APU POWER SEQUENCE



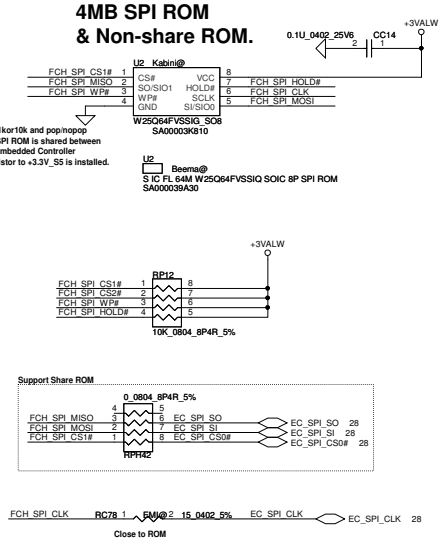
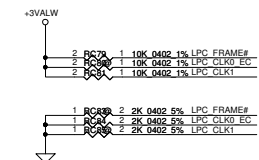
Security Classification		2013/02/26		Deciphered Date		2015/07/08		Title		Compal Electronics, Inc.	
Issued Date								NOTES LIST			
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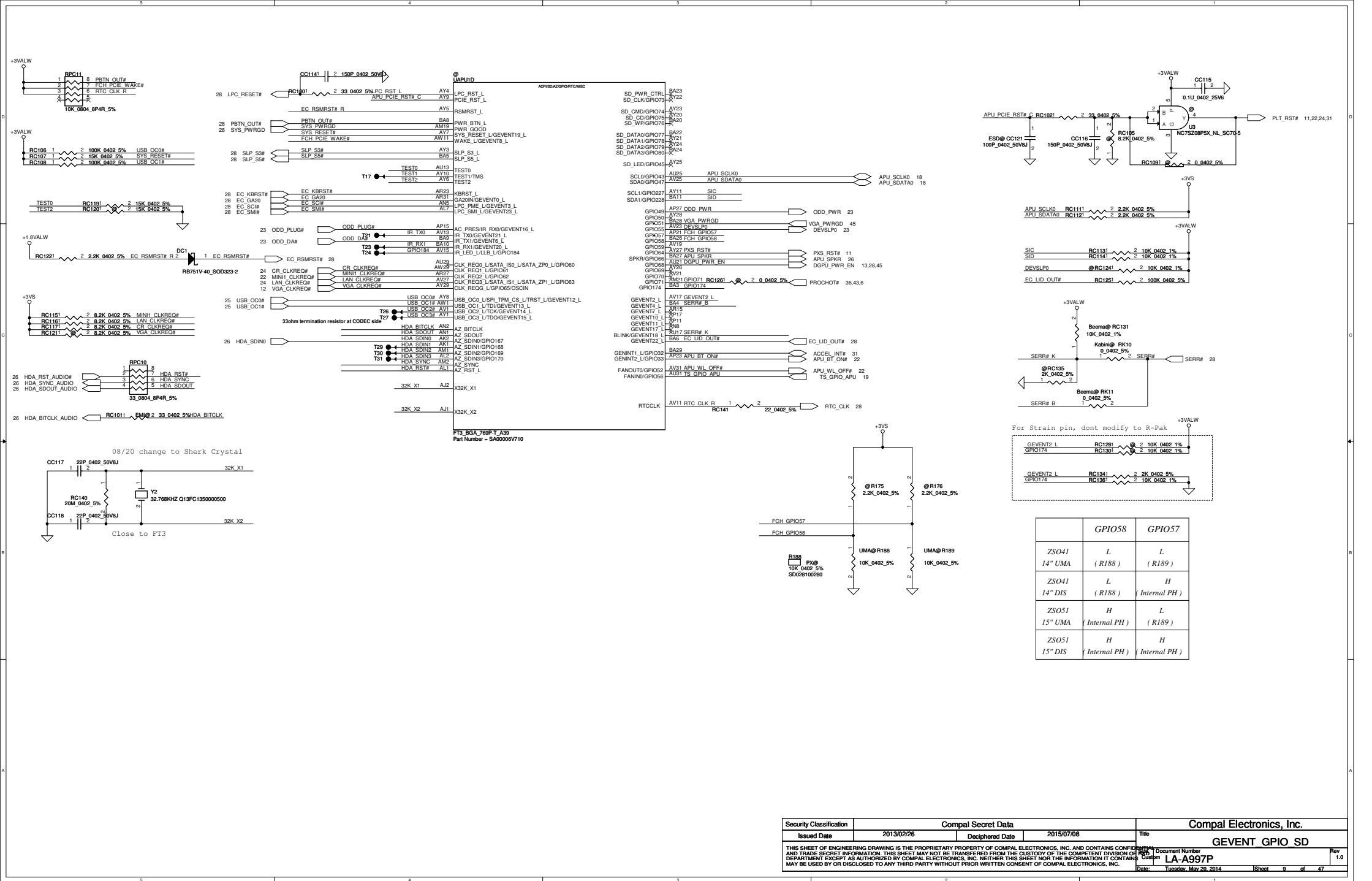


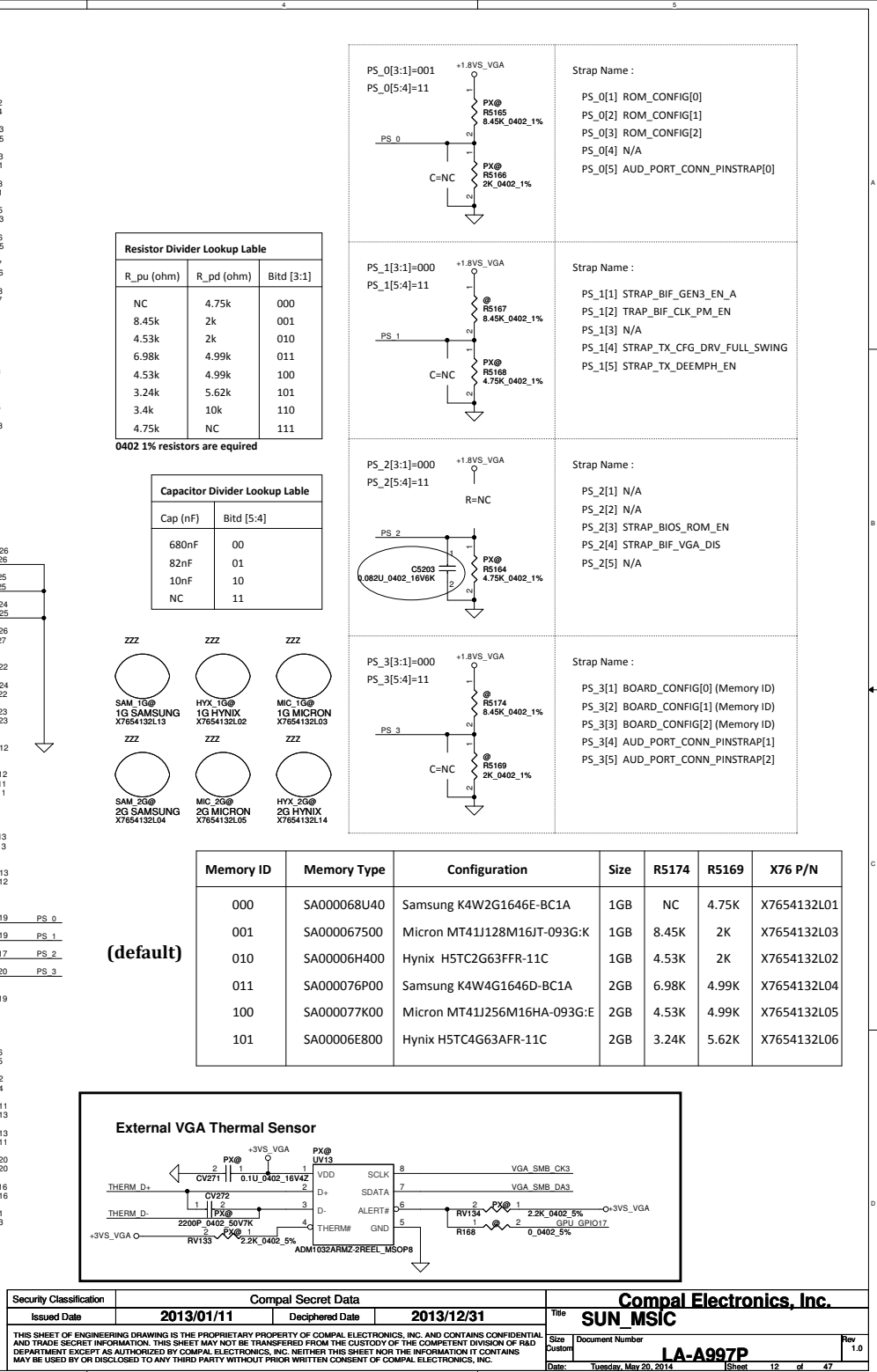


STRAPS OF APU					
	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWER UP/RESET TIMING (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	FAST POWER UP/RESET TIMING FOR SIMULATION

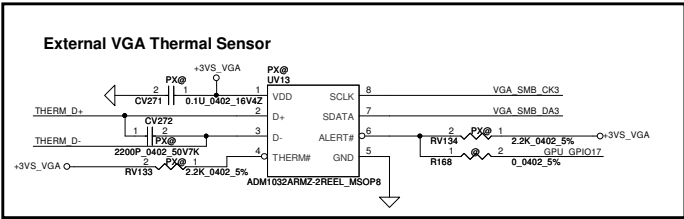


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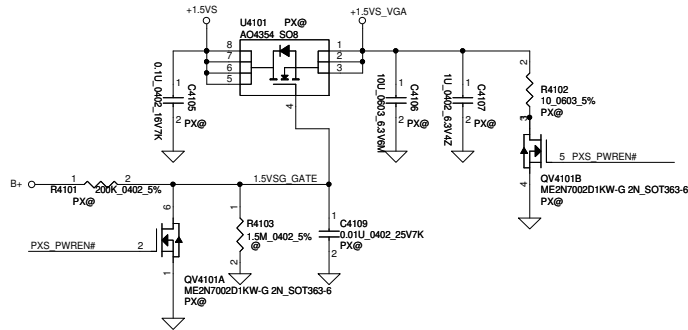


Memory ID	Memory Type	Configuration	Size	R5174	R5169	X76 P/N
000	SA000068U40	Samsung K4W2G1646E-BC1A	1GB	NC	4.75K	X7654132L01
001	SA000067500	Micron MT41J128M16JT-093G:K	1GB	8.45K	2K	X7654132L03
010	SA00006H400	Hynix H5TC2G63FFR-11C	1GB	4.53K	2K	X7654132L02
011	SA000076P00	Samsung K4W4G1646D-BC1A	2GB	6.98K	4.99K	X7654132L04
100	SA000077K00	Micron MT41J256M16HA-093G:E	2GB	4.53K	4.99K	X7654132L05
101	SA00006E800	Hynix H5TC4G63AFR-11C	2GB	3.24K	5.62K	X7654132L06



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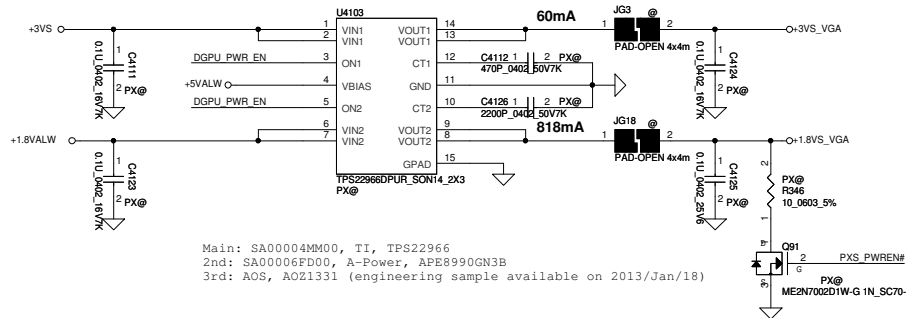
+1.5VS to +1.5VS_VGA (2.096A)



+3VS to +3VS_VGA (25mA)

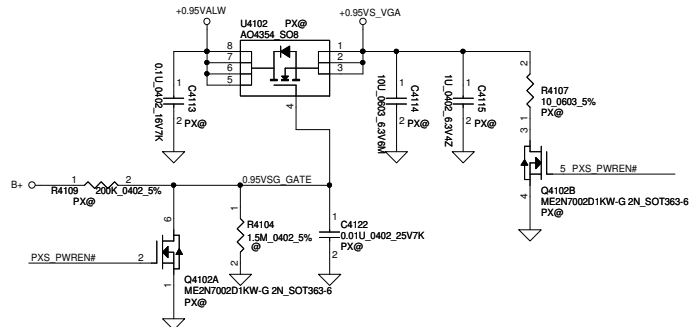
+1.8VALW to +1.8VS_VGA (311mA)

+1.8VS_VGA 必須比 +VGA_CORE晚起來



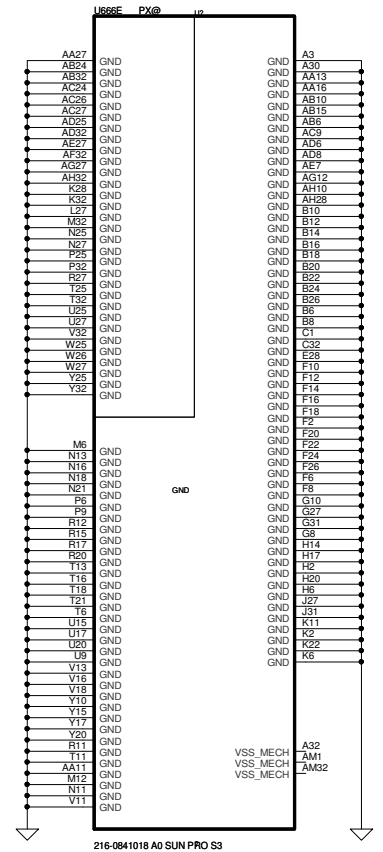
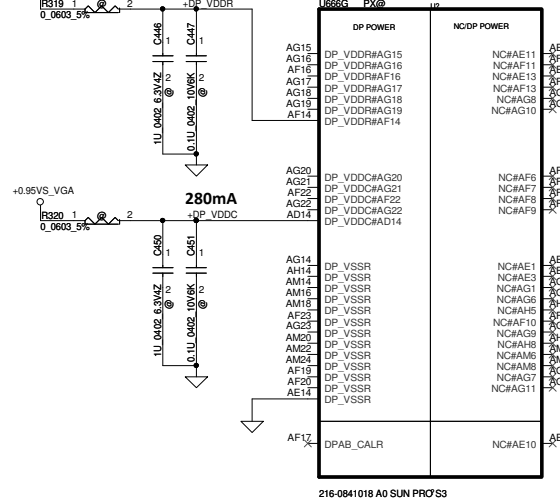
Main: SA00004MM00, TI, TPS22966
2nd: SA00006FD00, A-Power, APE8990GN3B
3rd: AOS, AOZ1331 (engineering sample available on 2013/Jan/18)

+0.95VALW to +0.95VSG (4.016A)

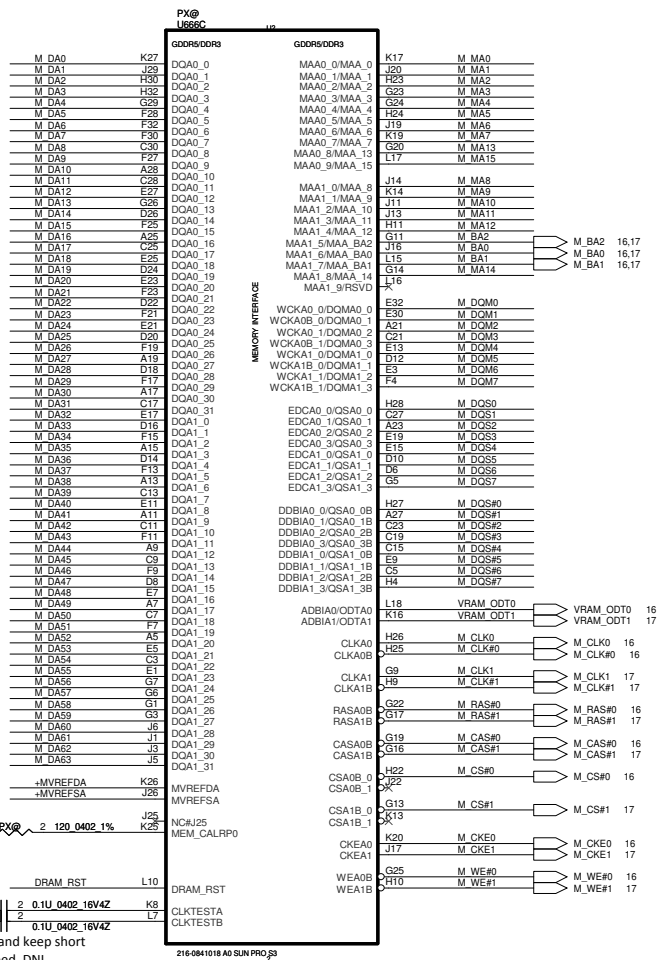


370mA (HDMI) 188mA (Display Port)

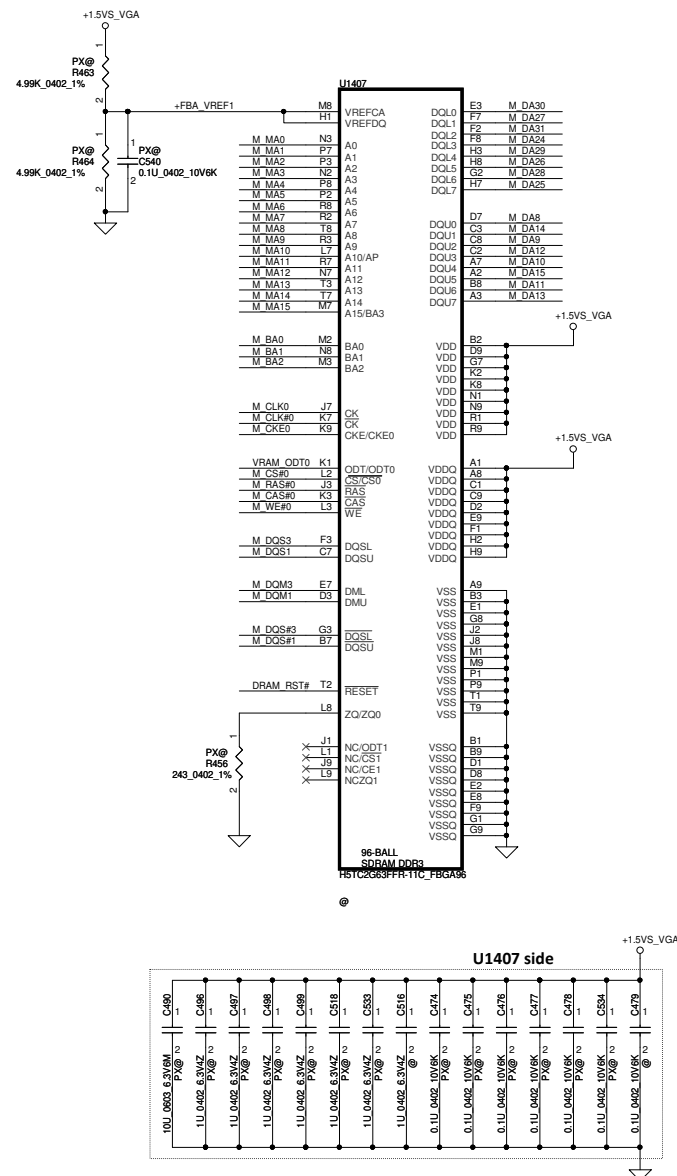
No Use GPU Display Port output



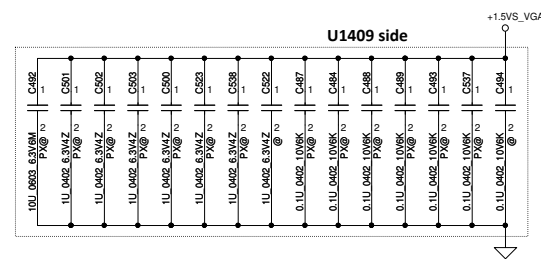
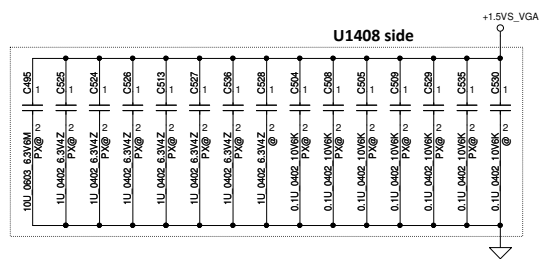
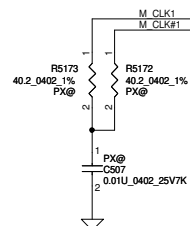
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								Custom			Document Number	
											LA-A997P	
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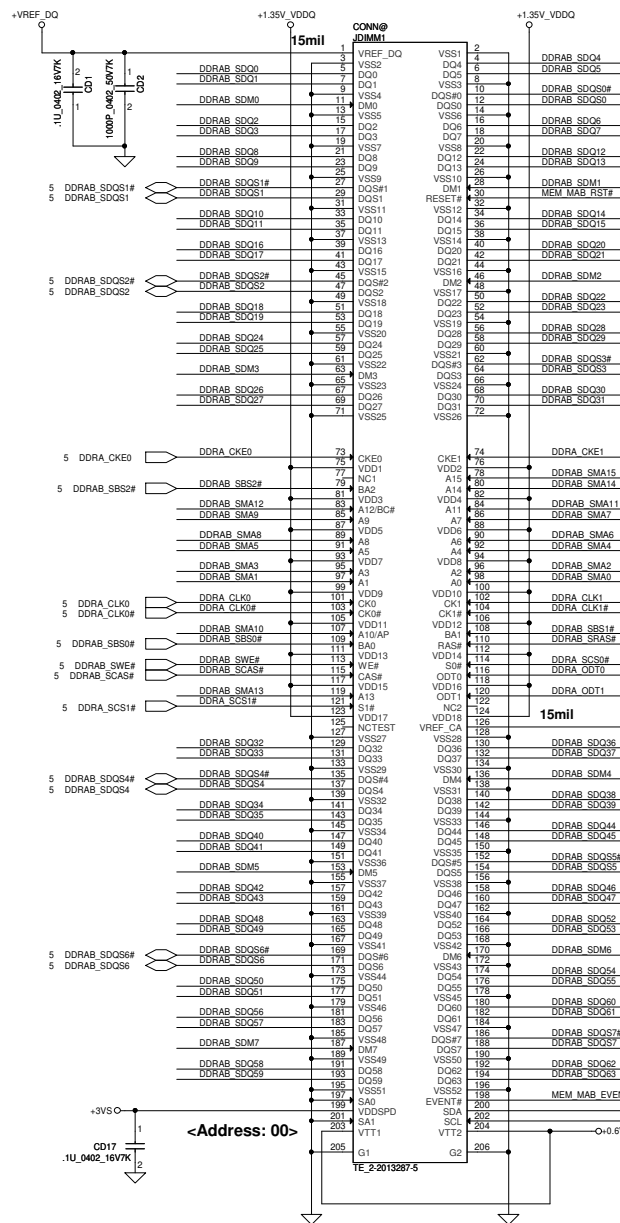
15,17	M_DA[63..0]		M_DA[63..0]
15,17	M_MA[15..0]		M_MA[15..0]
15,17	M_DQM[7..0]		M_DQM[7..0]
15,17	M_DQS[7..0]		M_DQS[7..0]
15,17	M_DQS#[7..0]		M_DQS#[7..0]



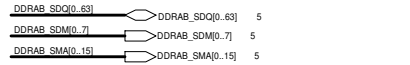
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Issued Date	2013/01/11	Deciphered Date	2013/12/31	Title	SUN VRAM A Lower	
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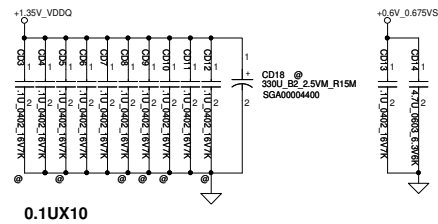
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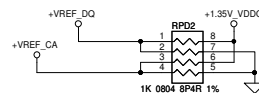
DIMM_1 H:4mm Reverse



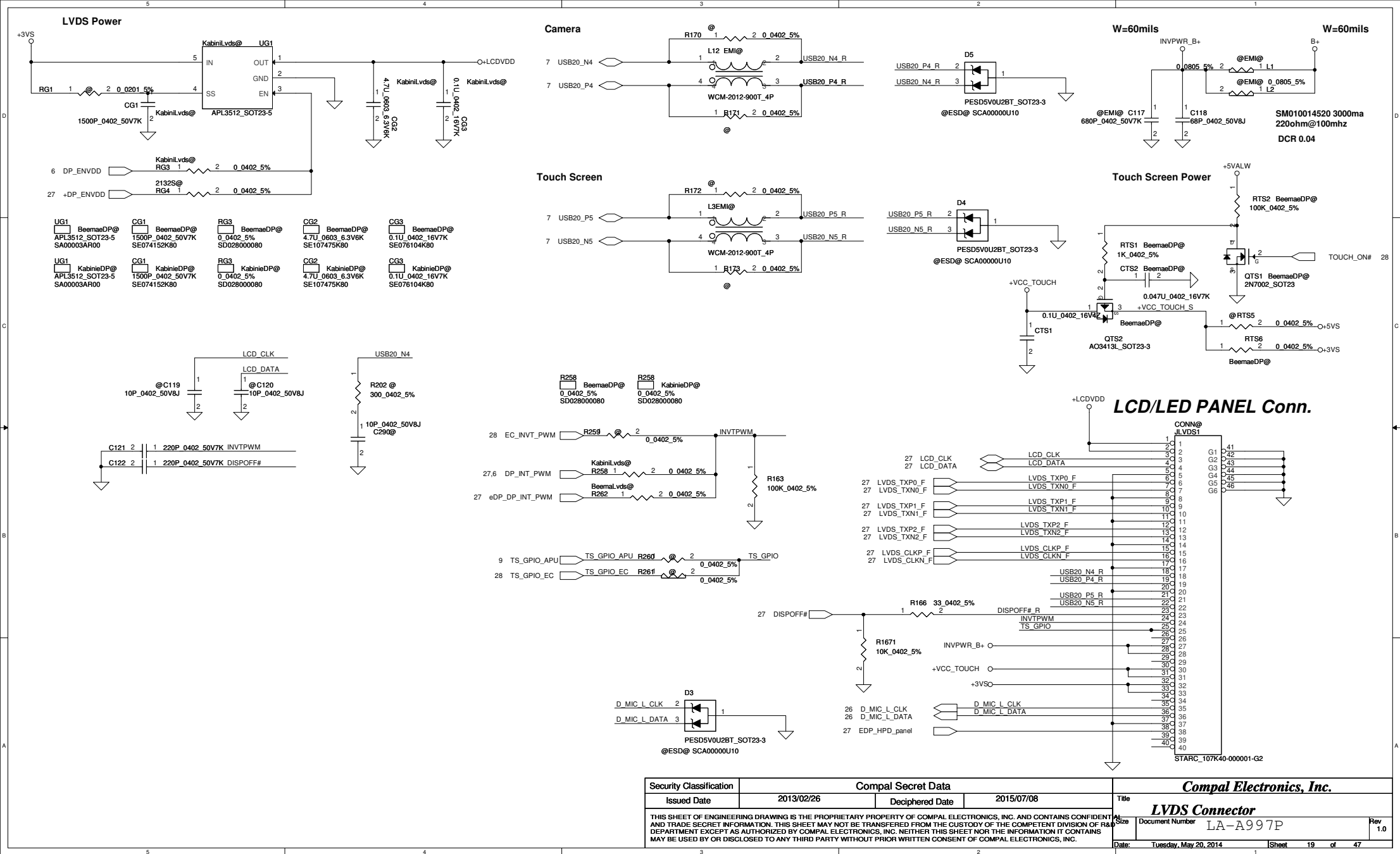
+1.35V_VDDQ/+0.675VS OF DIMM1

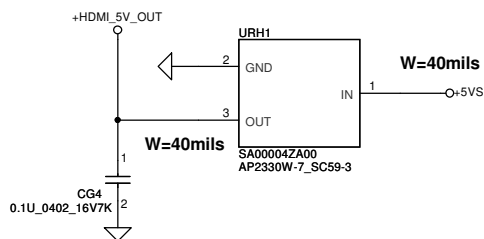
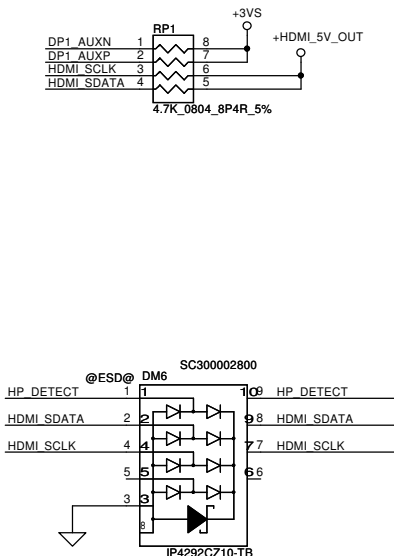
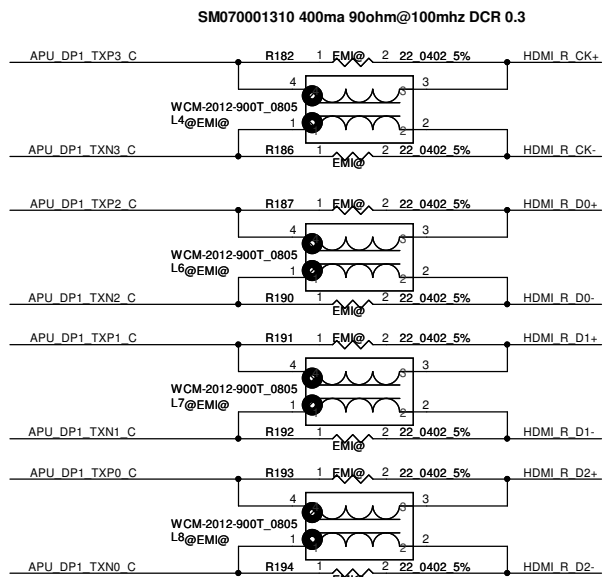
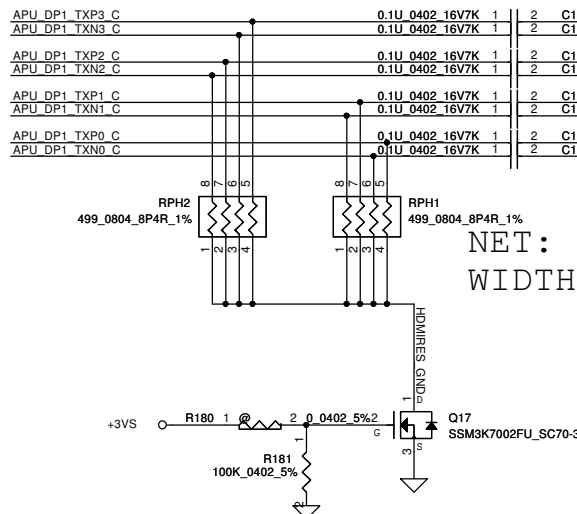
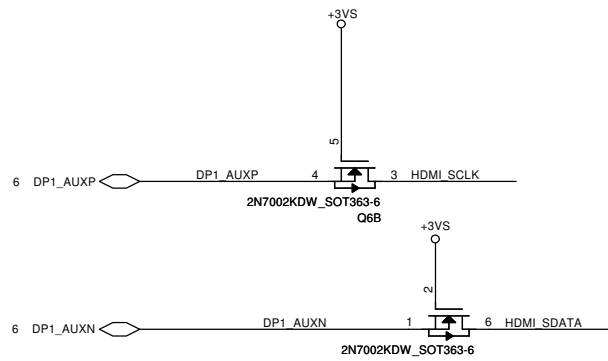


VREF for DIMM1

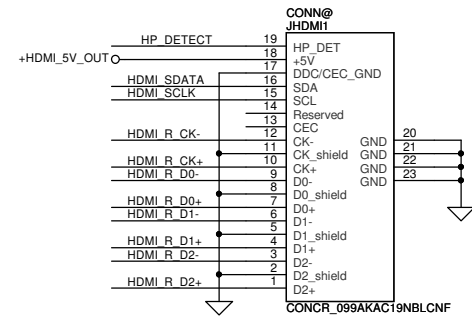


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				DDR3 SODIMM Socket		
				Size	Document Number	Rev
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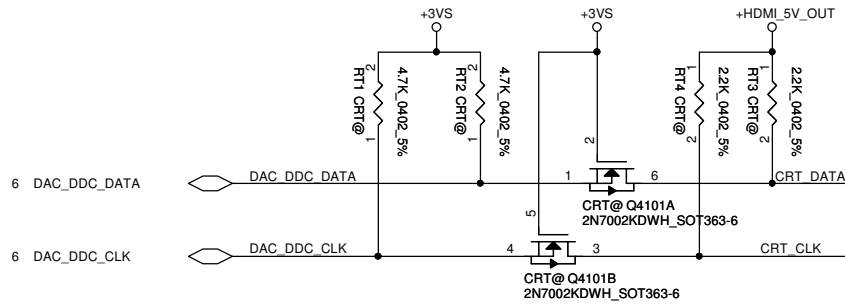
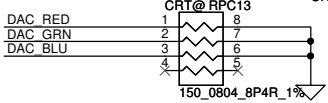
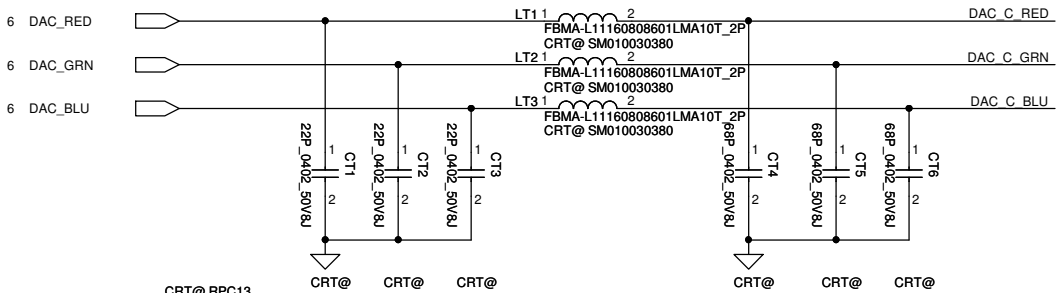
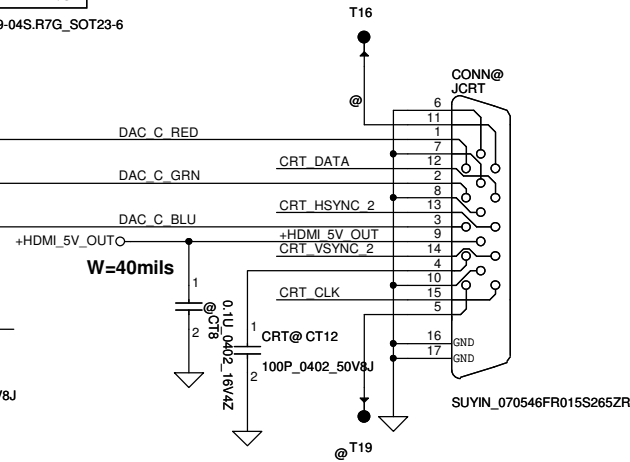
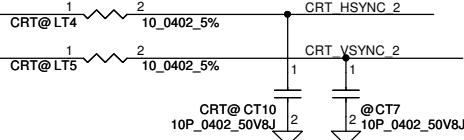
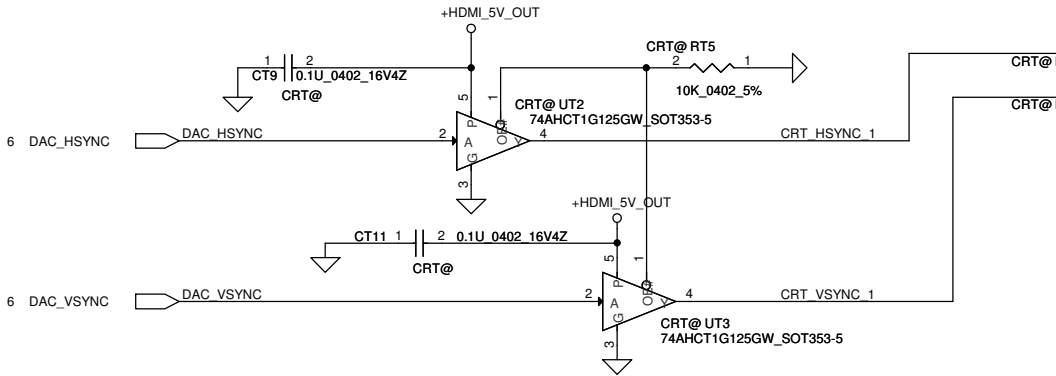
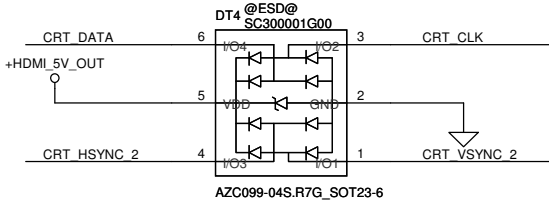
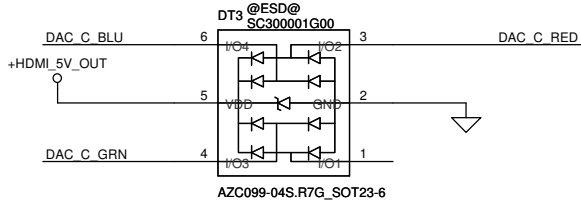


8/20 change HDMI Conn HDMI Conn.

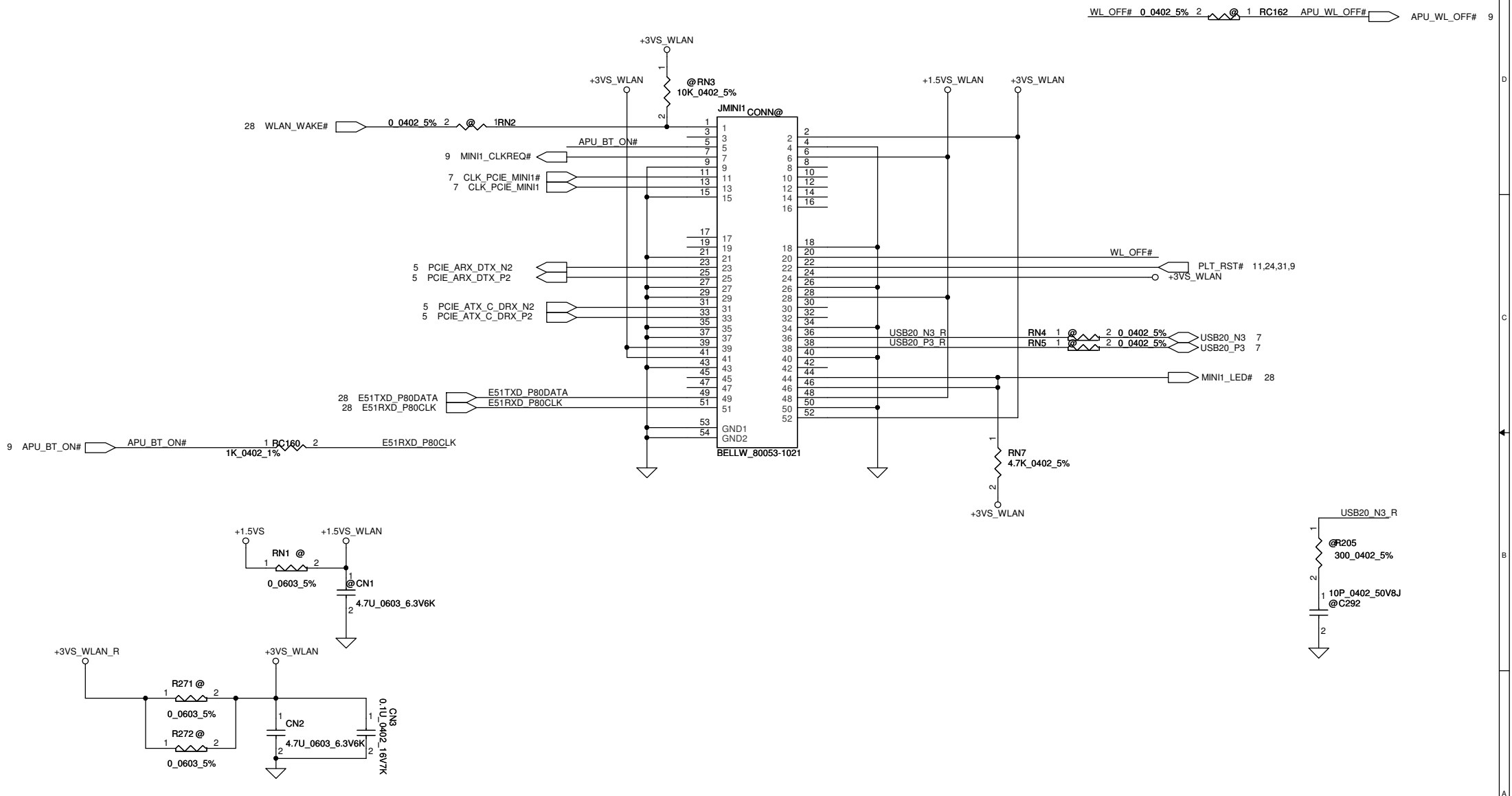


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CRT share HDMI Power

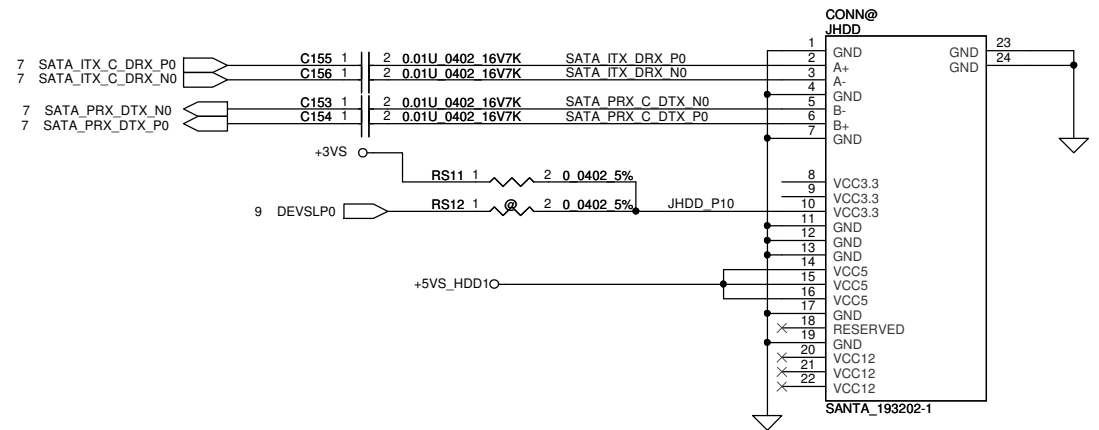
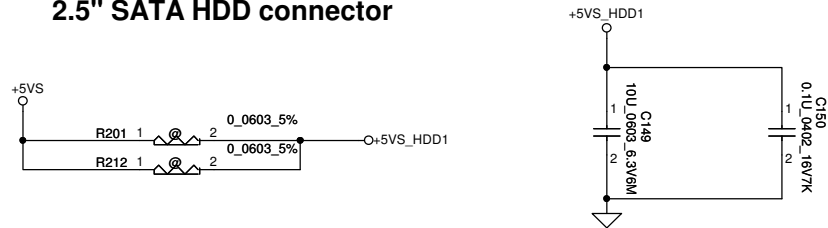


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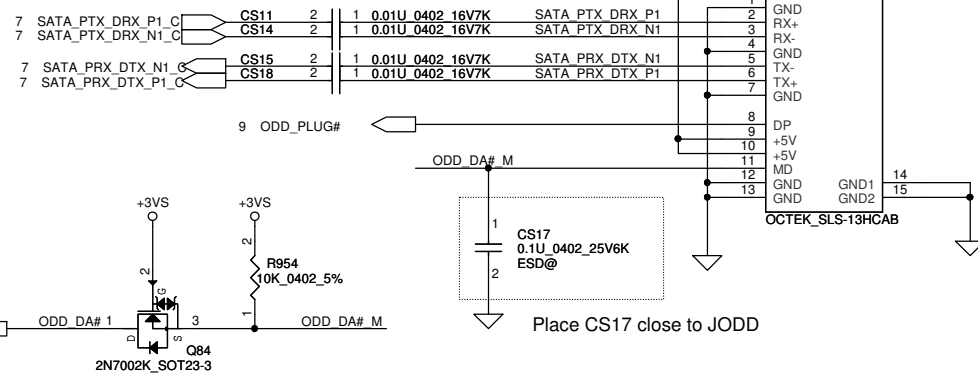
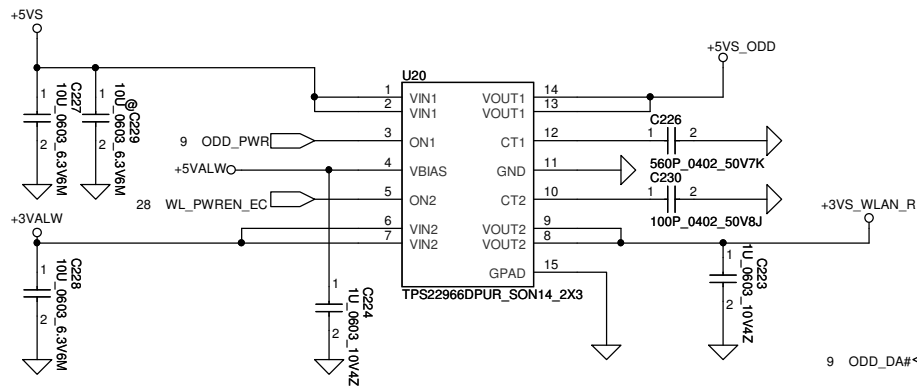
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2.5" SATA HDD connector

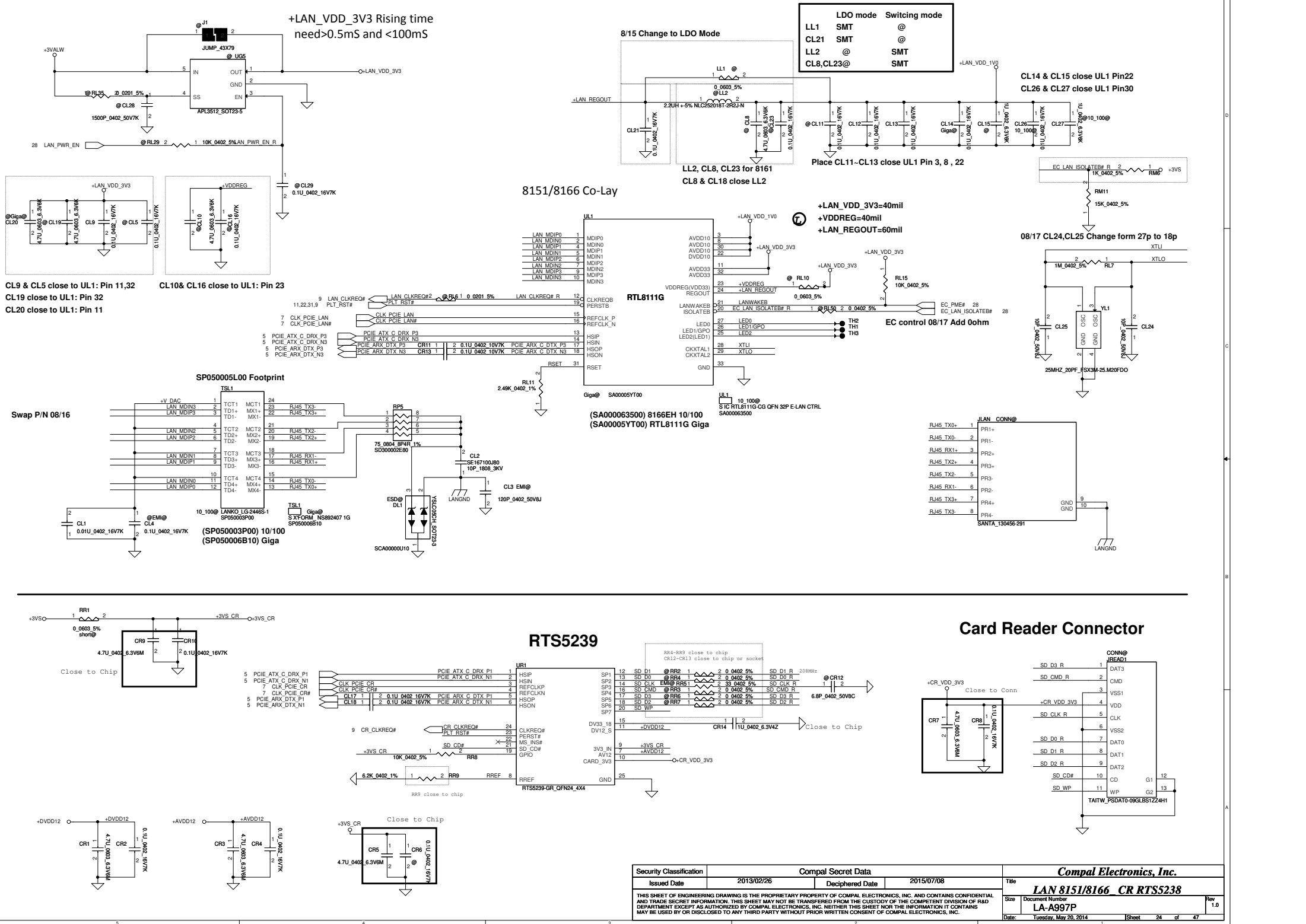


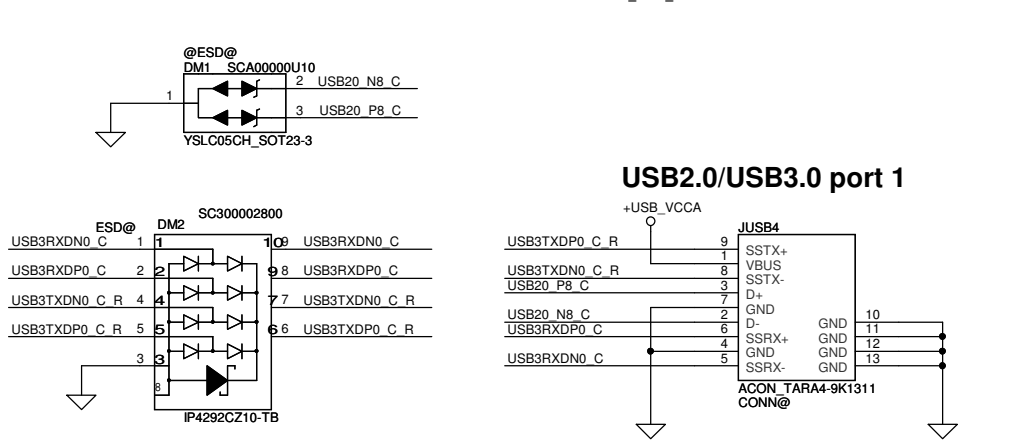
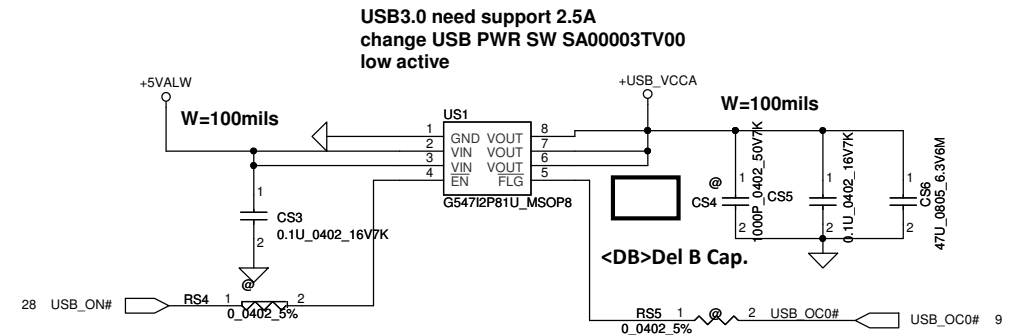
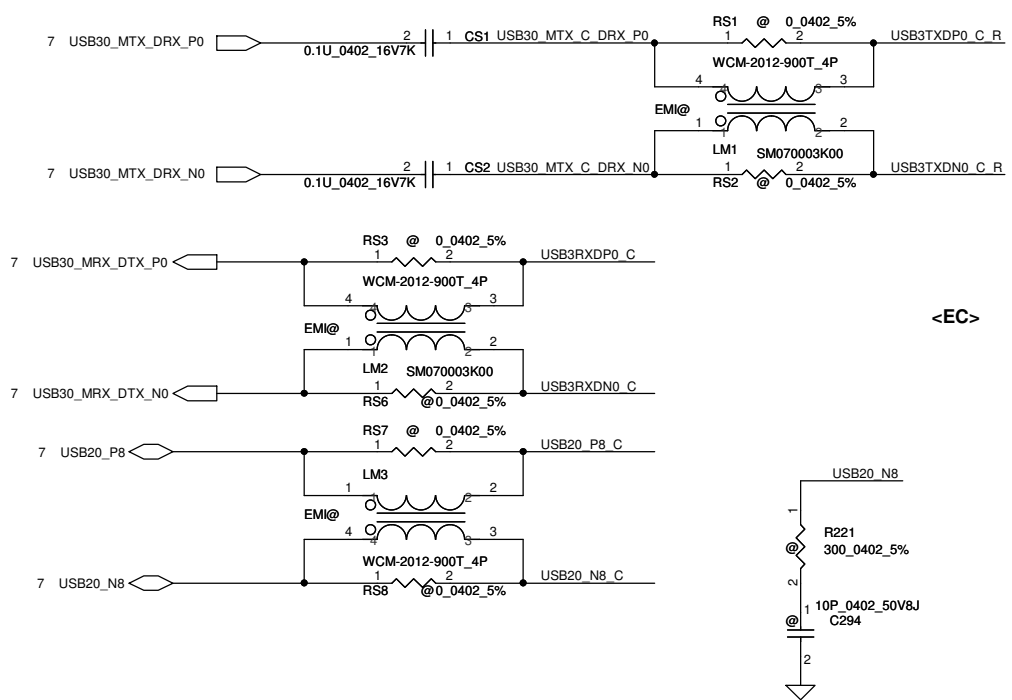
Change ODD Conn 08/22, check pin define

Place near ODD Connector

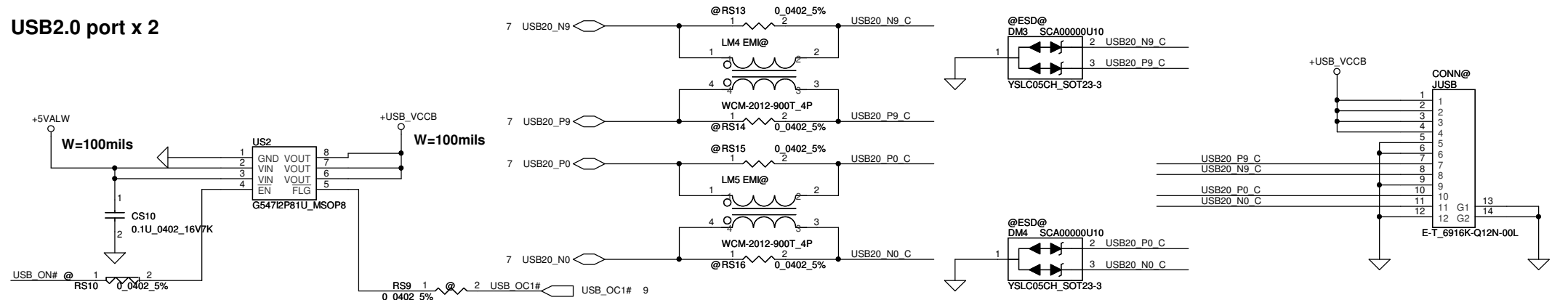


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				Date:	Tuesday, May 20, 2014
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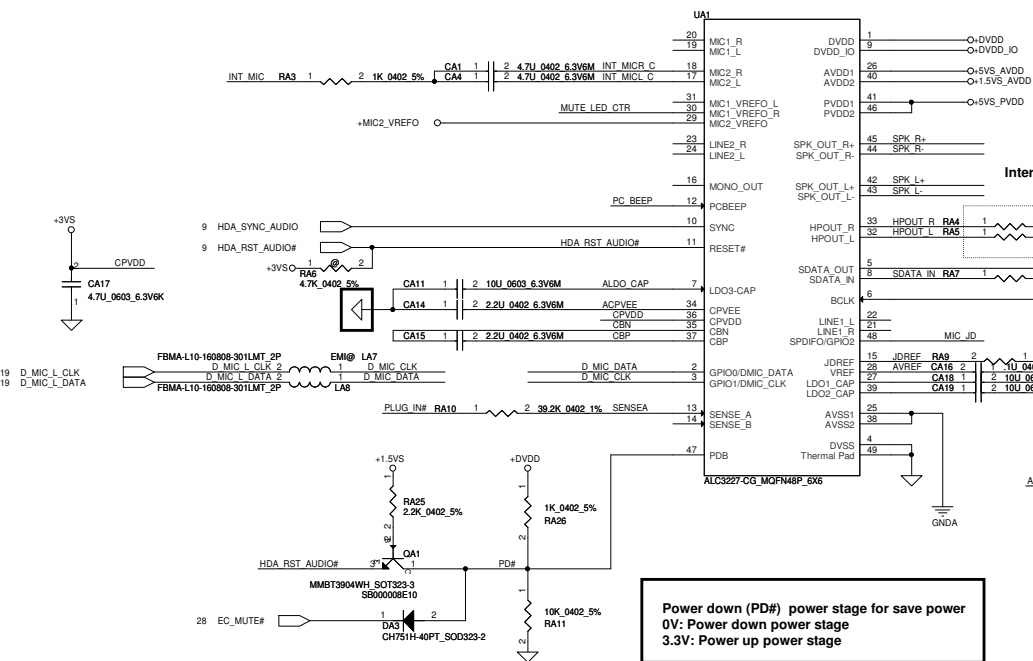




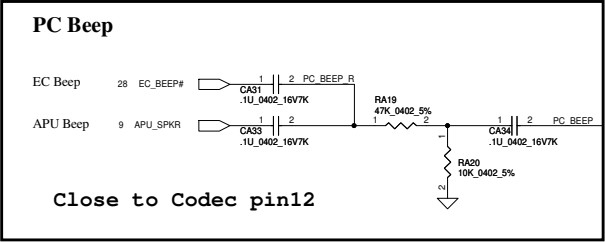
USB2.0 port x 2



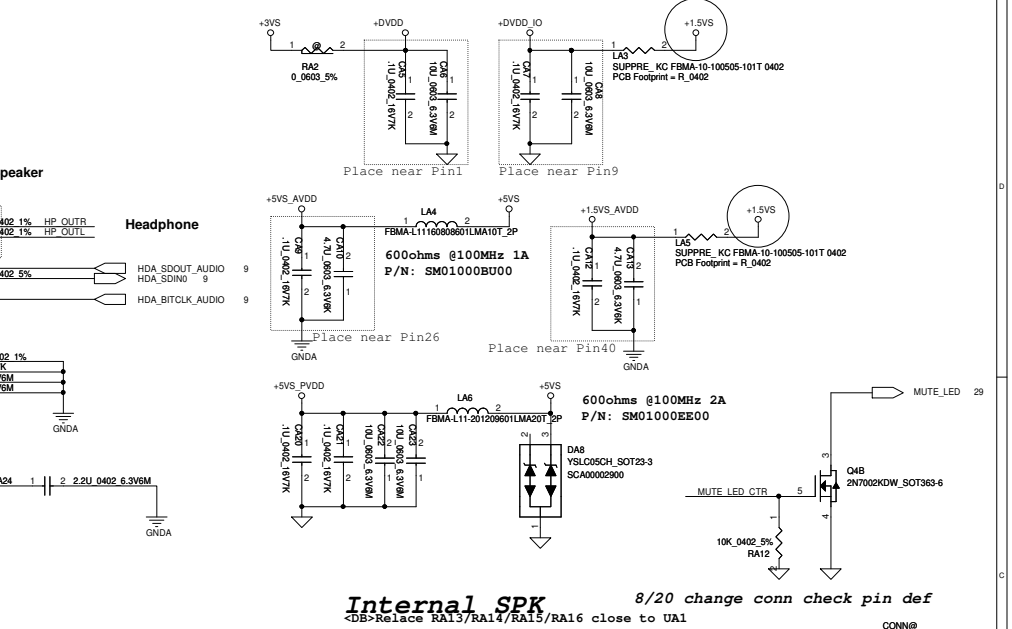
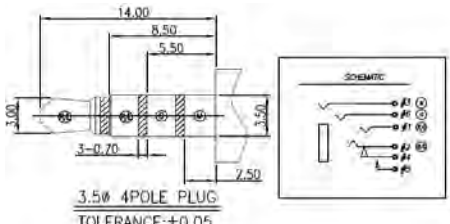
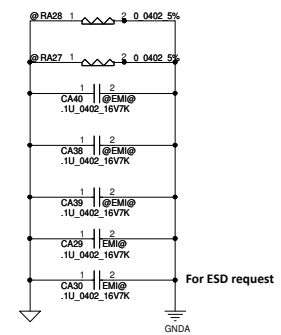
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	
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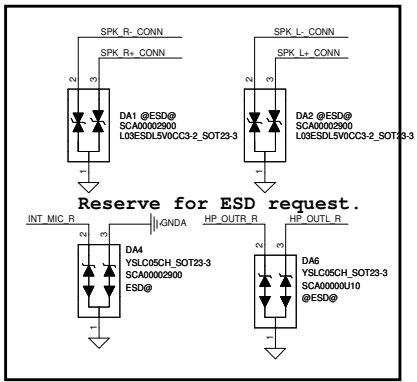
Power down (PD#) power stage for save power
0V: Power down power stage
3.3V: Power up power stage



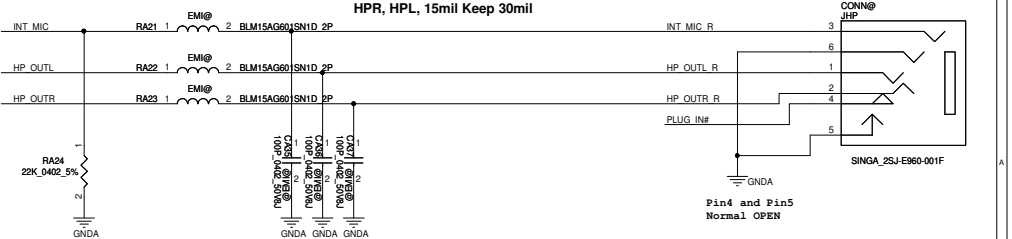
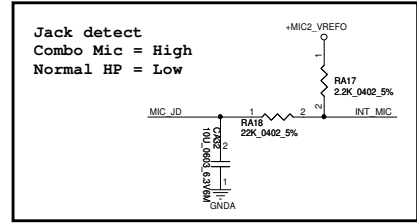
Close to Codec pin12



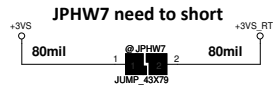
SM01000A00
SPK_R+ EM1@ RA13
SPK_L+ EM1@ RA14
SPK_R- EM1@ RA15
SPK_L- EM1@ RA16
SM01000A00



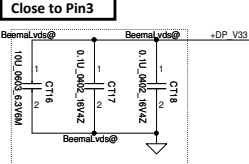
COMBO AUDIO JACK



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2015/01/04		
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Layout note

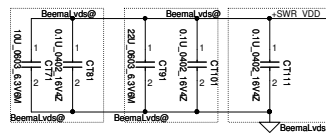


Layout note

Close to LT5

Close to Pin18

Close to Pin13

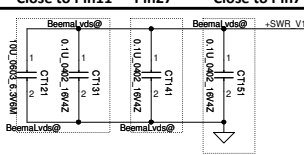


Layout note

Close to Pin11

Close to Pin27

Close to Pin7

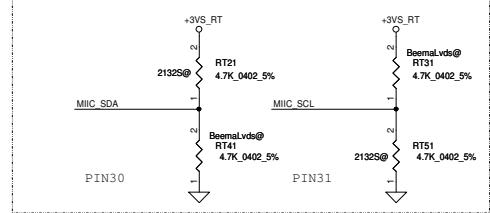


※ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.

EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.

EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.

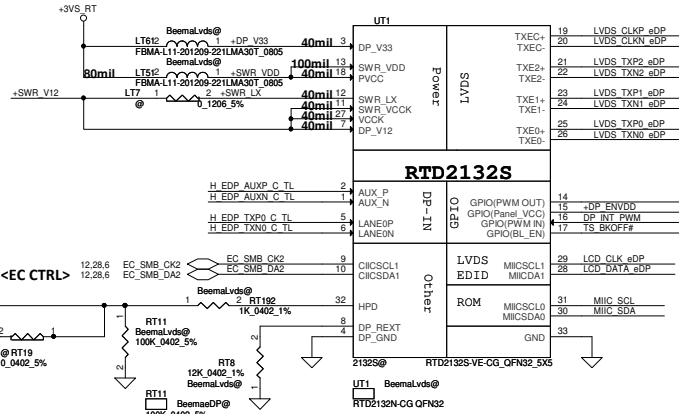
(※Default mode)



SWR / LDO Mode select

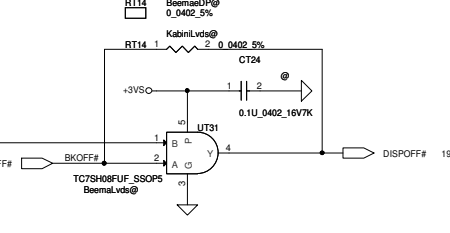
	LDO	SWR
2132S	Do not support	mount LT7
2132R	Use 0 ohm	mount LT7

※ If use 2132R, please select LDO mode as default.



Layout note

Close to Pin8



<RTS2132>
<EC CTRL>

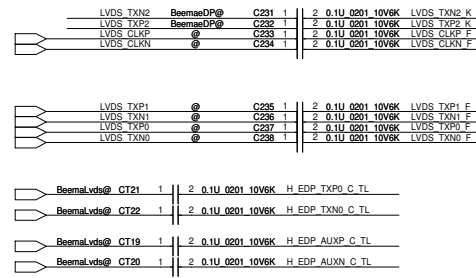
<CPU>

LTDP0_TXP3
LTDP0_TXN3

LTDP0_TXP1
LTDP0_TXN1
LTDP0_TXP0
LTDP0_TXN0

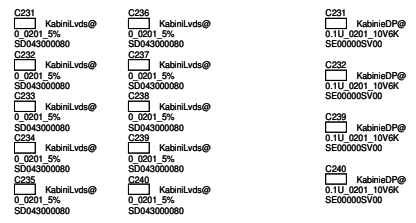
LTDP0_TXP2
LTDP0_TXN2

LTDP0_AUXP
LTDP0_AUXN



< Kabini LVDS>

< Kabini eDP>



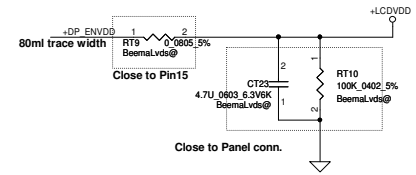
	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

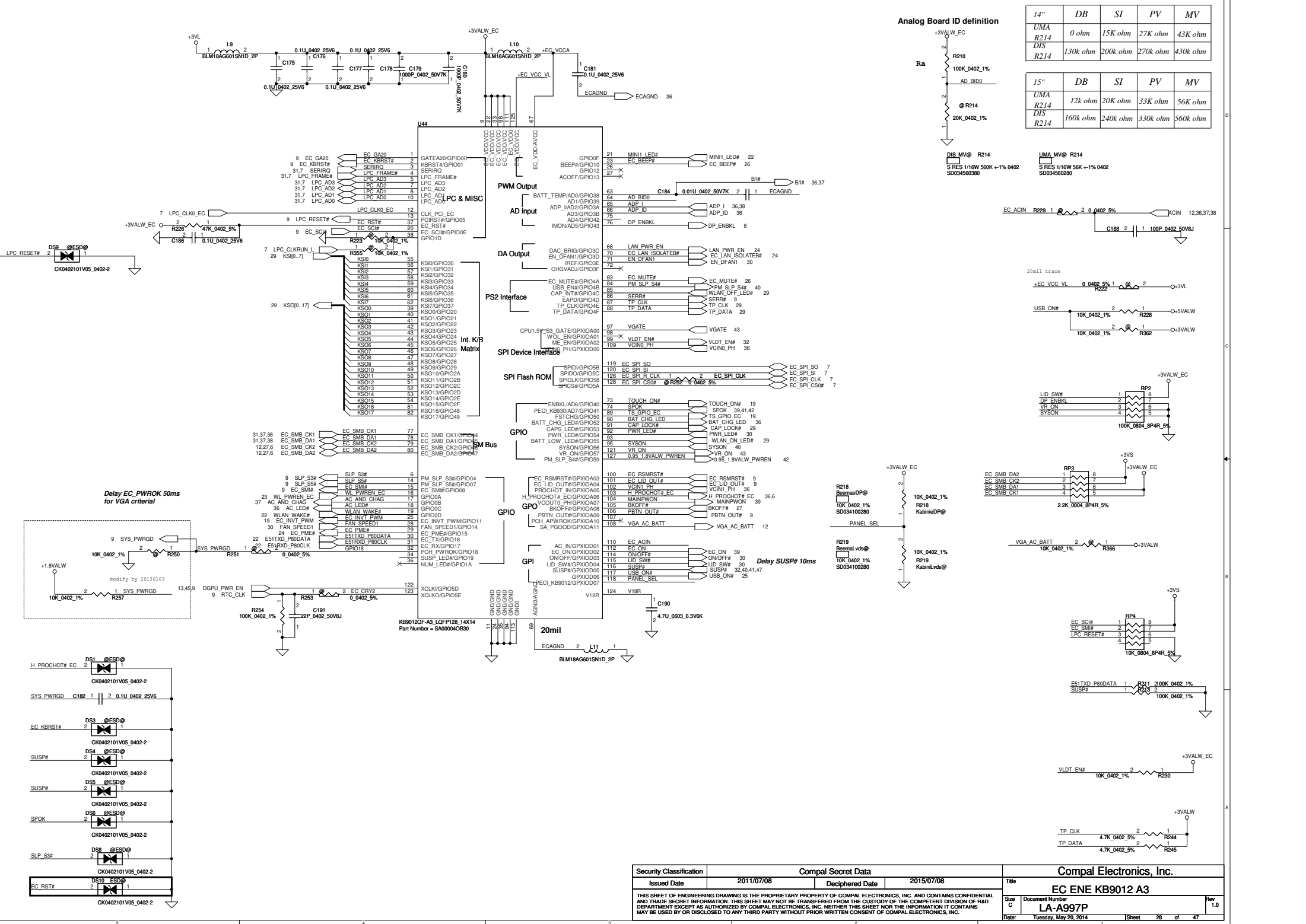
PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5~3.3V

* Version R has internal level shifter, remove level shifter circuit on AMD platform

Different between 2132S and 2132R	
2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter



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Analog Board ID definition

14"	DB	SI	PV	MV
UMA	0 ohm	15K ohm	27K ohm	43K ohm
R214				
DIS	130k ohm	200k ohm	270k ohm	430k ohm
R214				

15"	DB	SI	PV	MV
UMA	12k ohm	20K ohm	33K ohm	56K ohm
R214				
DIS	160k ohm	240k ohm	330k ohm	560k ohm
R214				

UMA MV@ R214
S RES 1/16W 560K +1% 0402
SD034560280

UMA MV@ R214
S RES 1/16W 56K +1% 0402
SD034560280

20mil trace

EC VCC VL 0.0402_1% 1 2

USB ON# 10K_0402_1% 2 1 R228

10K_0402_1% 2 1 R362

LID SW# 1 2 3 4 5 6 7 8
VR ON# 1 2 3 4 5 6 7 8
SYSON 1 2 3 4 5 6 7 8
100K_0804_8P4R 5%

EC SMB DA2 1 2 3 4 5 6 7 8
EC SMB CK2 1 2 3 4 5 6 7 8
EC SMB DA1 1 2 3 4 5 6 7 8
EC SMB CK1 1 2 3 4 5 6 7 8
2.2K_0804_8P4R 5%

VGA AC BATT 1 2 3 4 5 6 7 8
10K_0402_1% 2 1 R366

ESITXD_P80DATA 1 2 3 4 5 6 7 8
SUSP# 1 2 3 4 5 6 7 8
100K_0402_1%

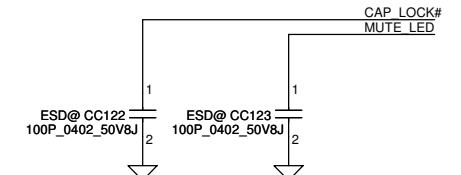
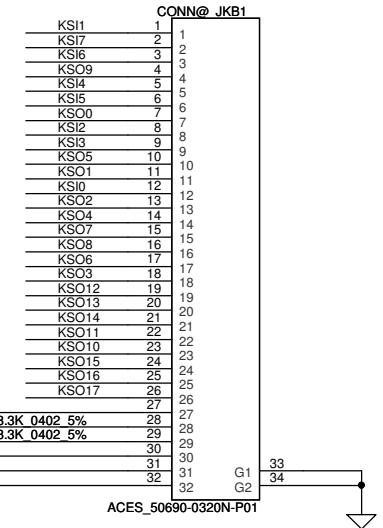
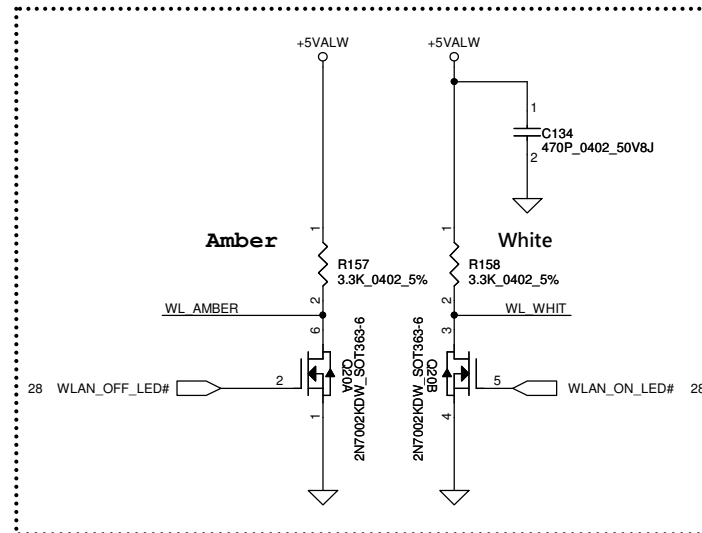
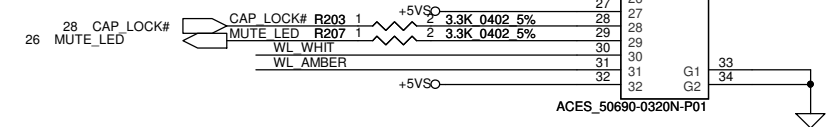
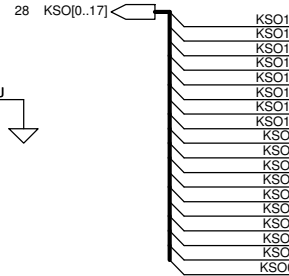
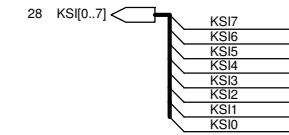
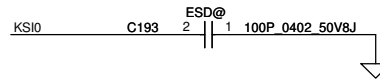
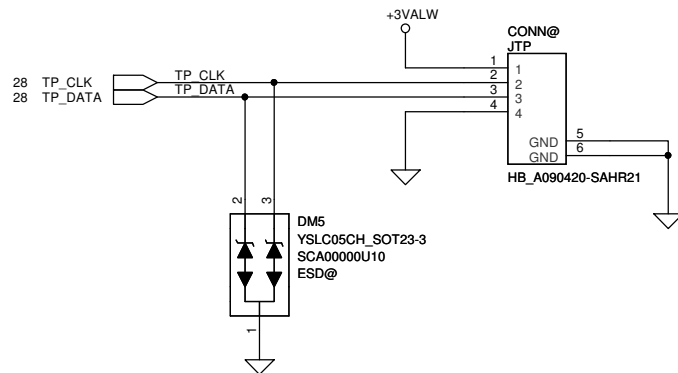
VLDT_EN# 10K_0402_1% 2 1 R230

TP_CLK 4.7K_0402_5% 2 1 R244

TP_DATA 4.7K_0402_5% 2 1 R245

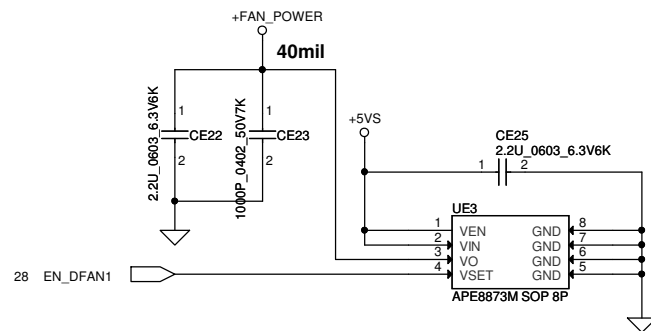
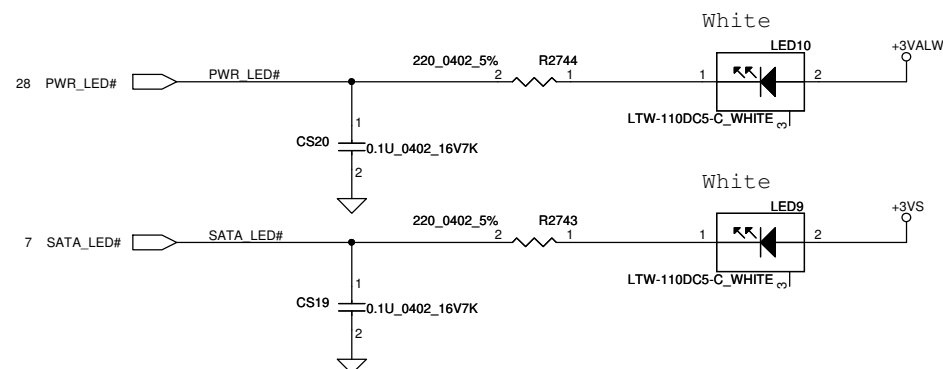
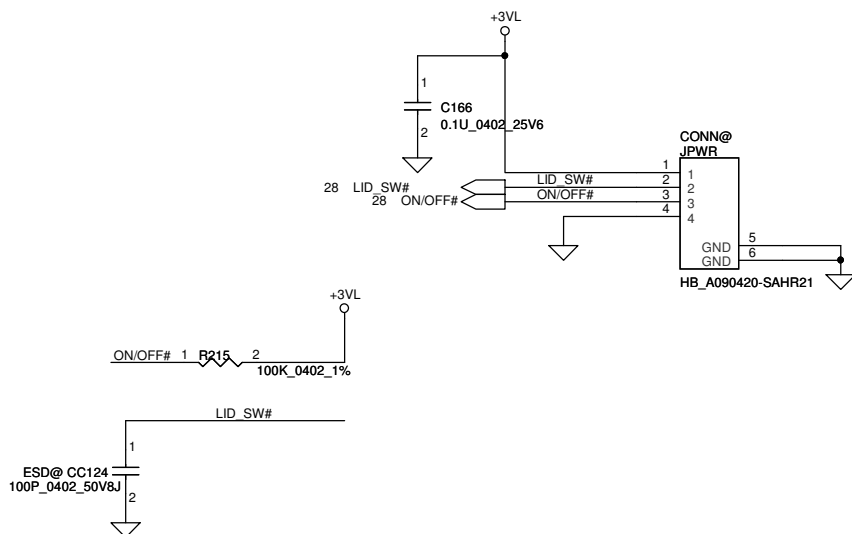
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Touch pad conn

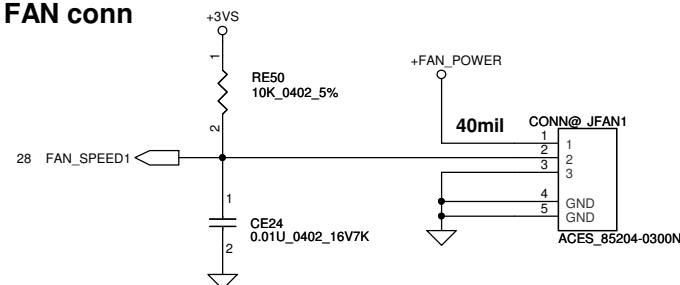


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Power Button Connector



FAN conn



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ACCELEROMETER

ACCELEROMETER

3V_GSEN

RH411 1 2 0.0402_5%

3V_GSEN

@RH503 0.0402_5%

3V_GSEN

ACCEL_INT#_R 1 2

@DH8

CH751H-40PT_S0D323-2

ACCEL_INT# 9

SI# 2012.04.10 Change ACCEL_INT# to INT1

3V_GSEN

@L125

INT2 9

INT1 11

VDD 14

SCL/SPC 4

SDA/SDVSDO 5

SDO/SAQ 6

CS 7

GND 8

RES 10

RES 11

RES 12

RES 13

RES 14

RES 15

RES 16

NC 2

NC 3

HP3DC2TR

+3V_GSEN

R208 1 2 0.0402_5%

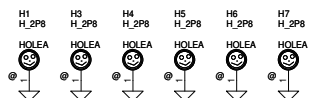
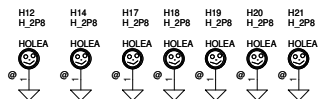
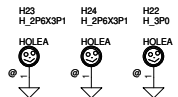
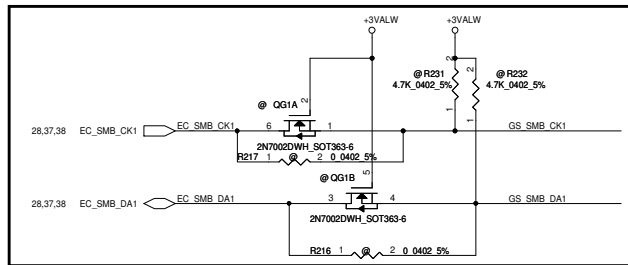
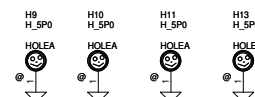
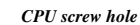
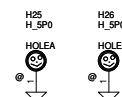
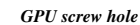
R227 0.0402_5%

R209 0.0402_5%

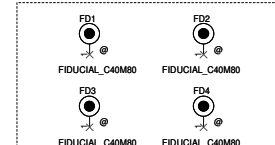
3V_GSEN

C241 1 2 0.1U_0402_16V7K

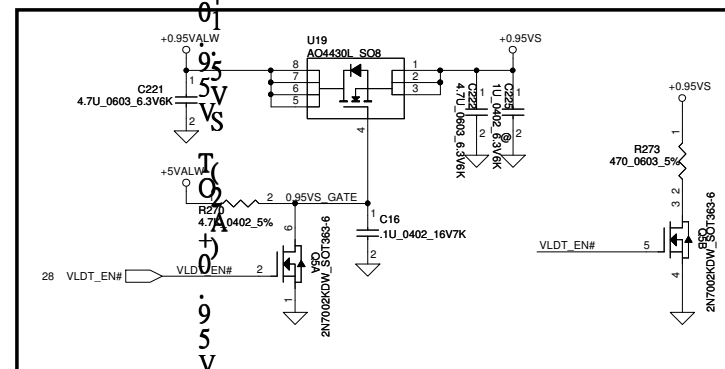
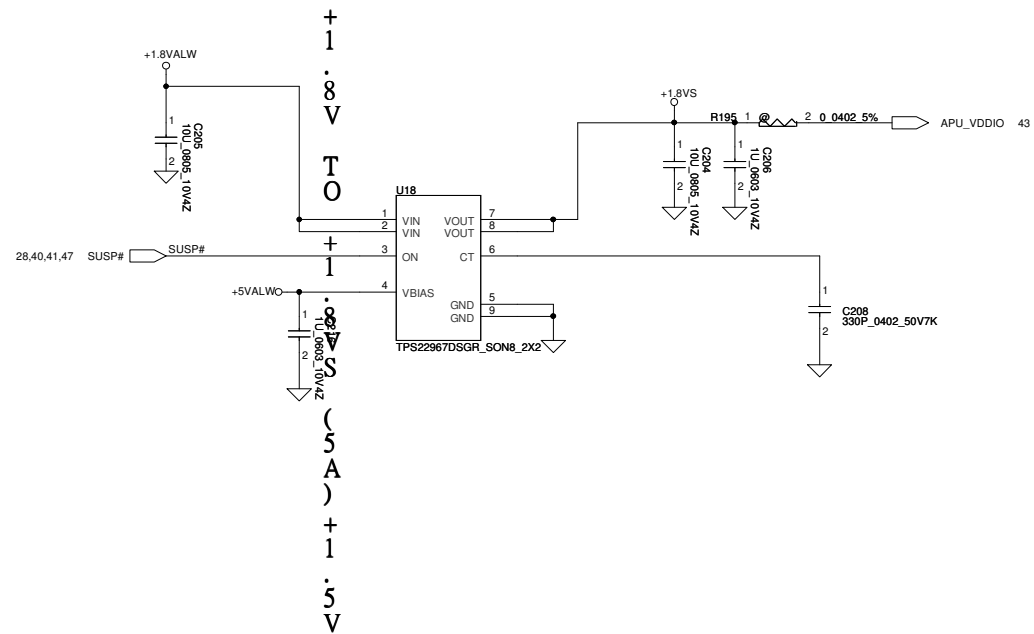
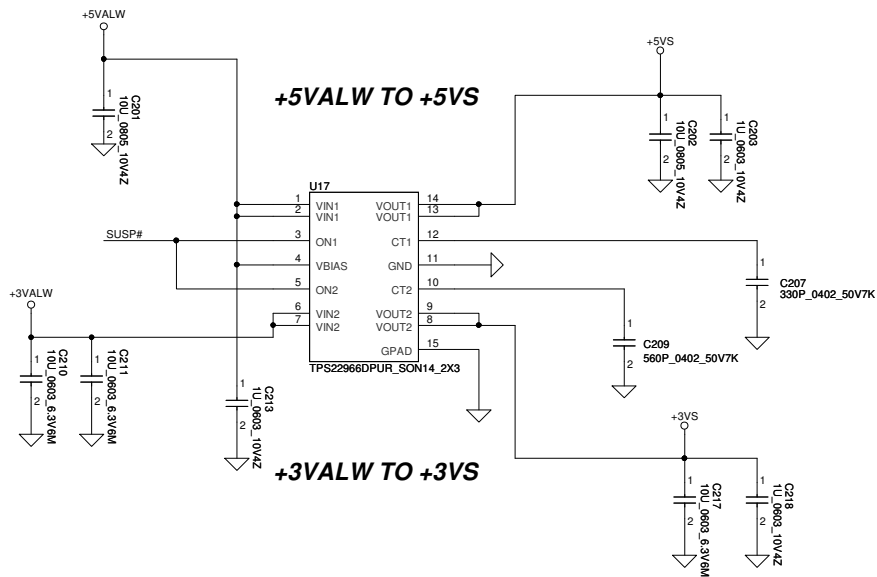
C242 1 2 10U_0603_5.3V5M

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FIDUCIAL

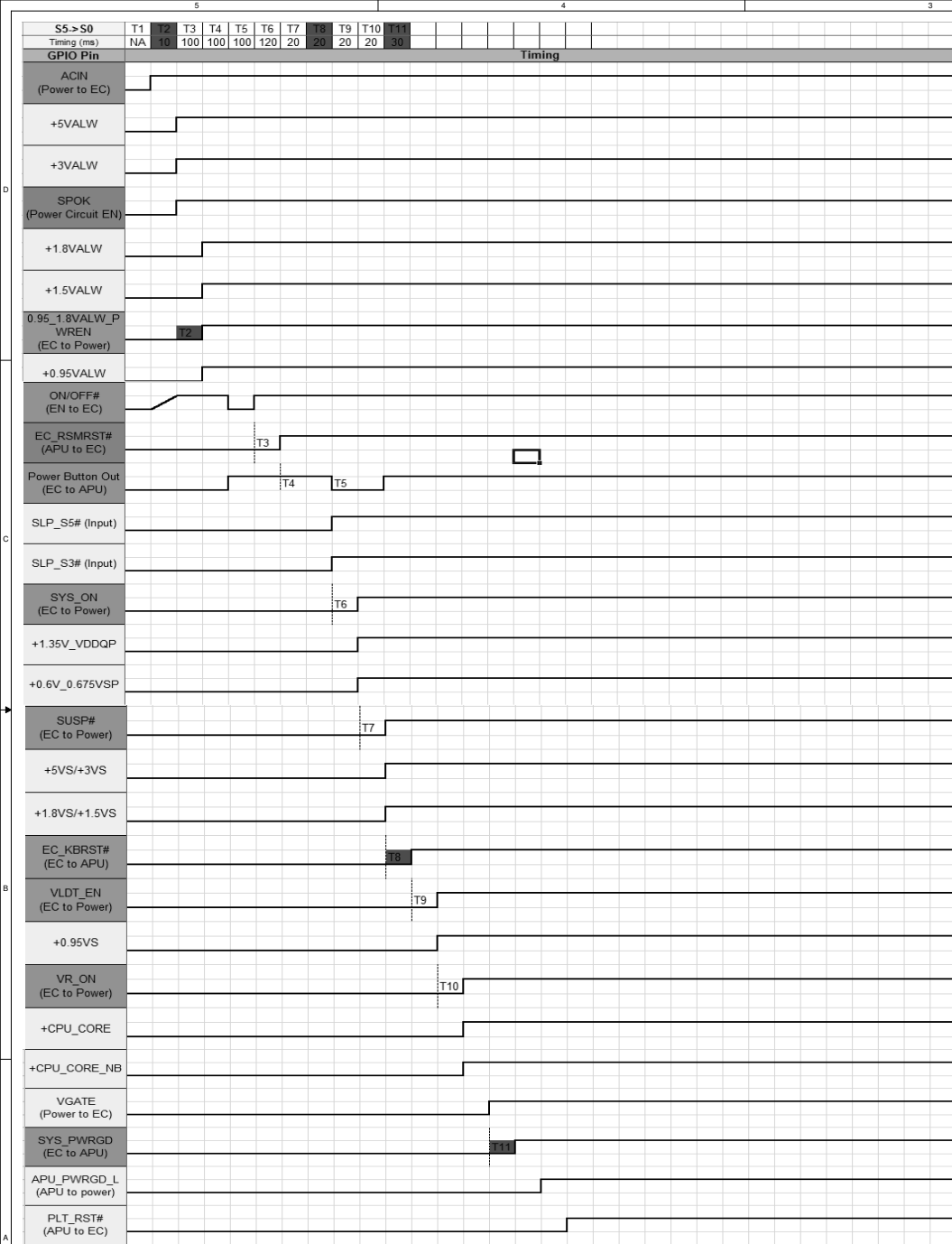


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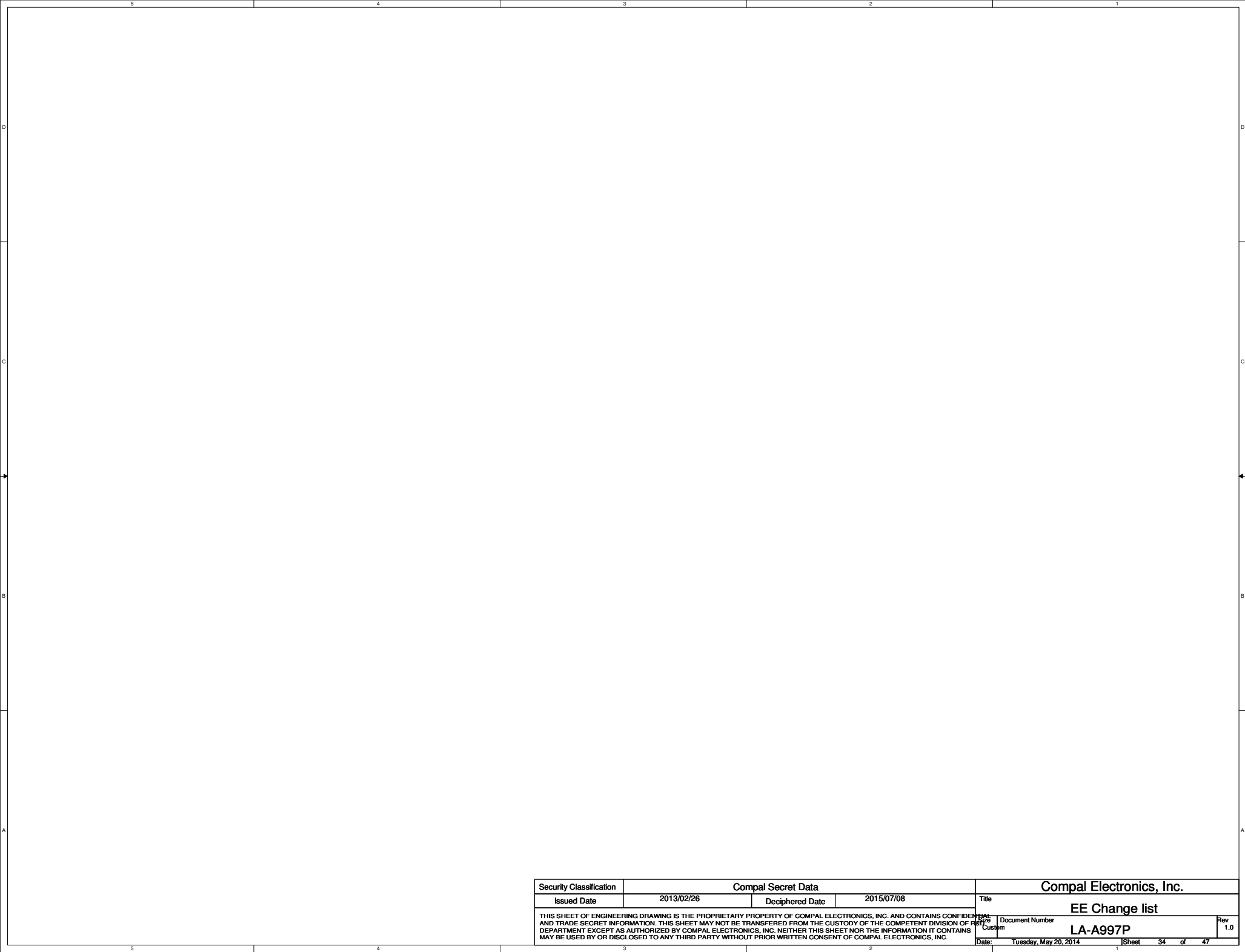


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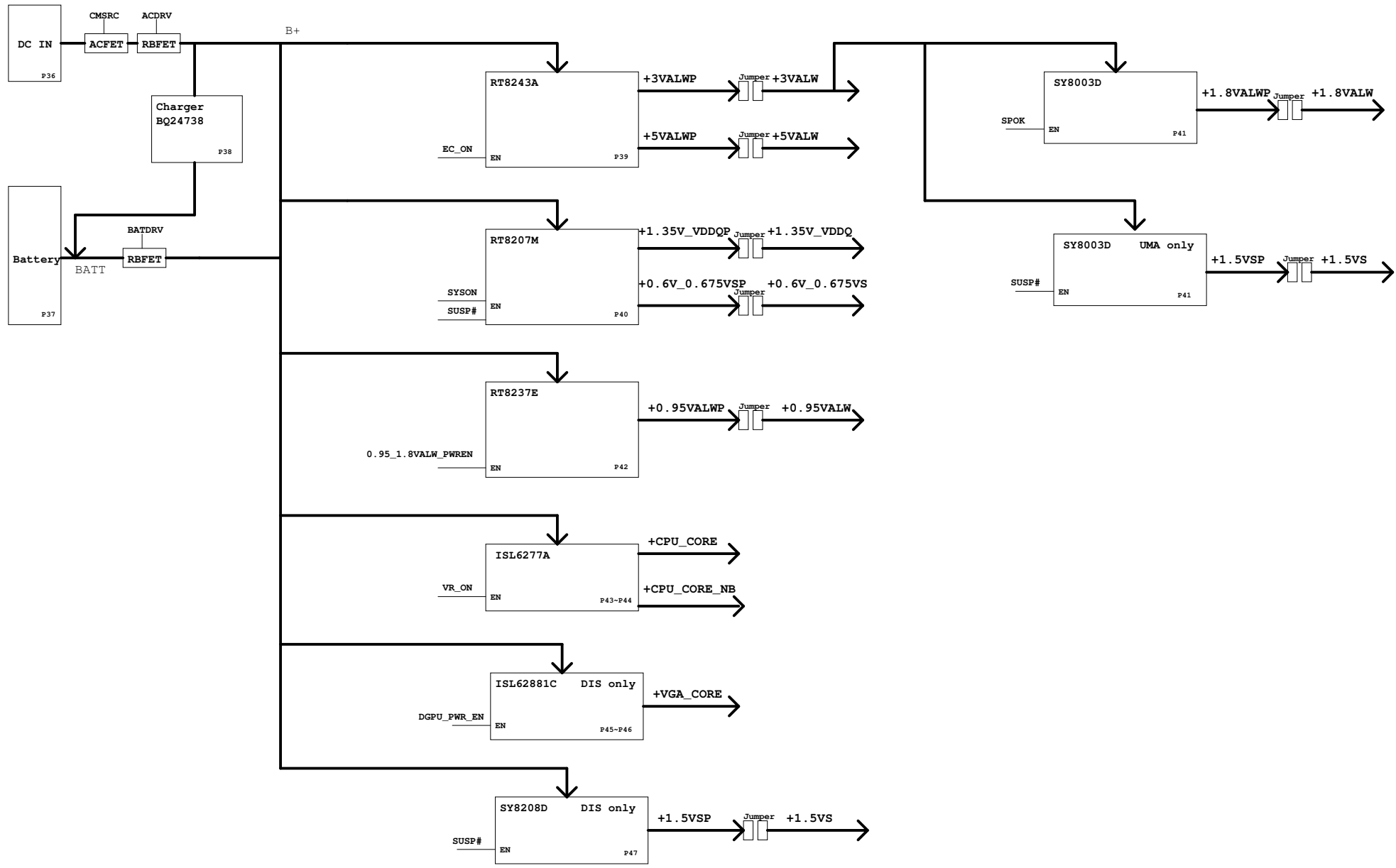
DC Interface			
Document Number		Rev	
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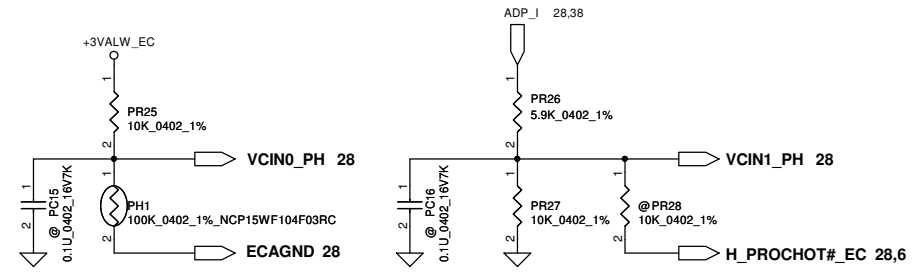
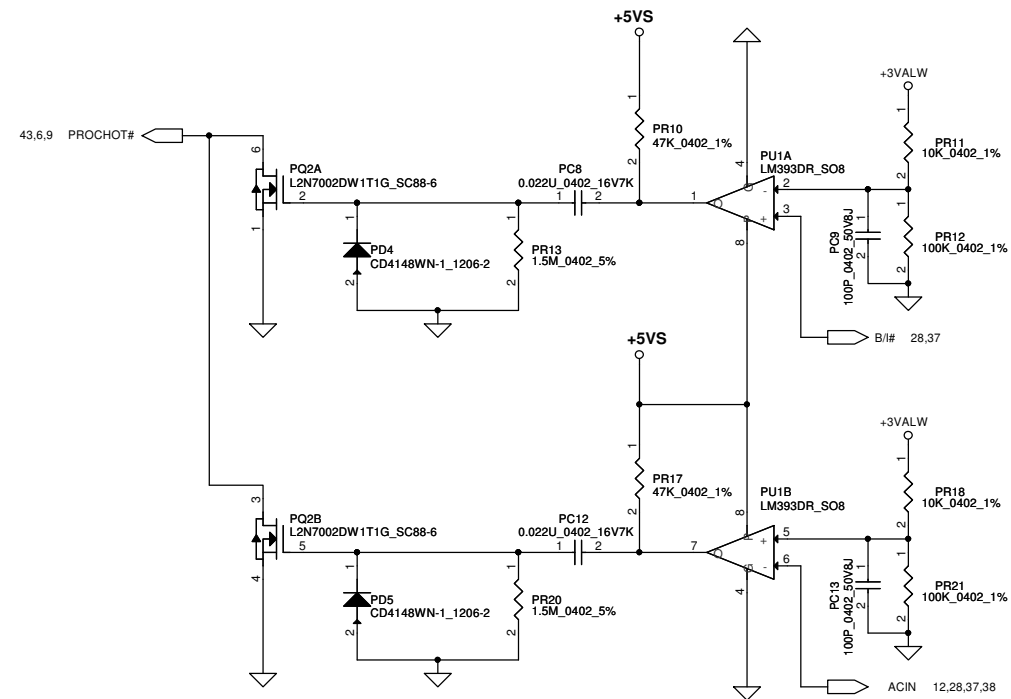
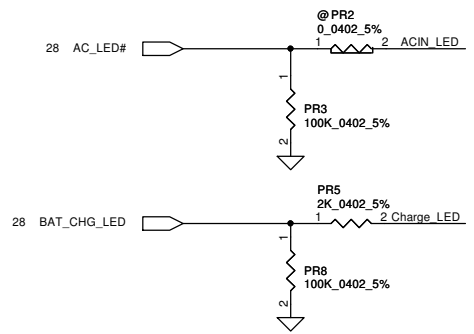
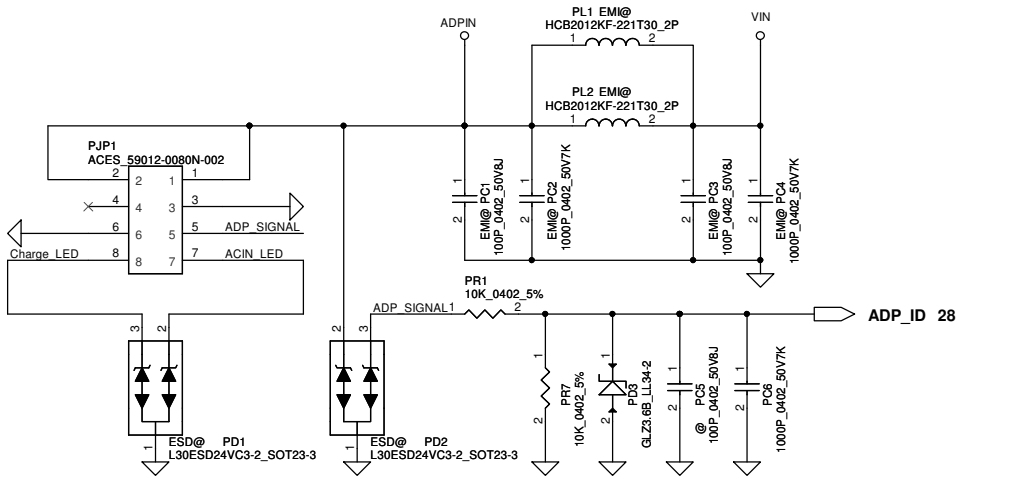
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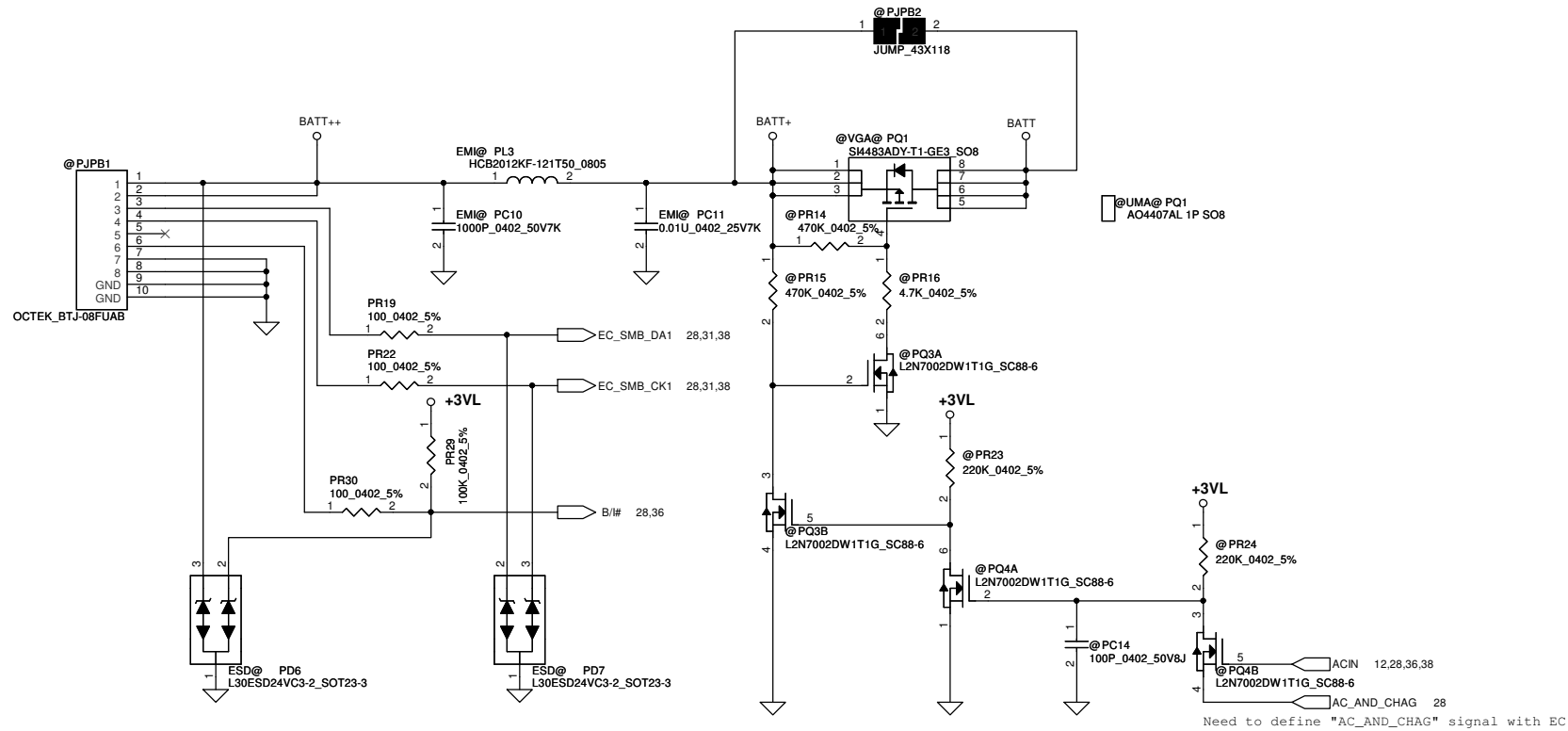
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Issued Date		2013/02/26		Deciphered Date		2015/07/08		Title			
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						Document Number		LA-A997P		Rev	
						Custom				1.0	
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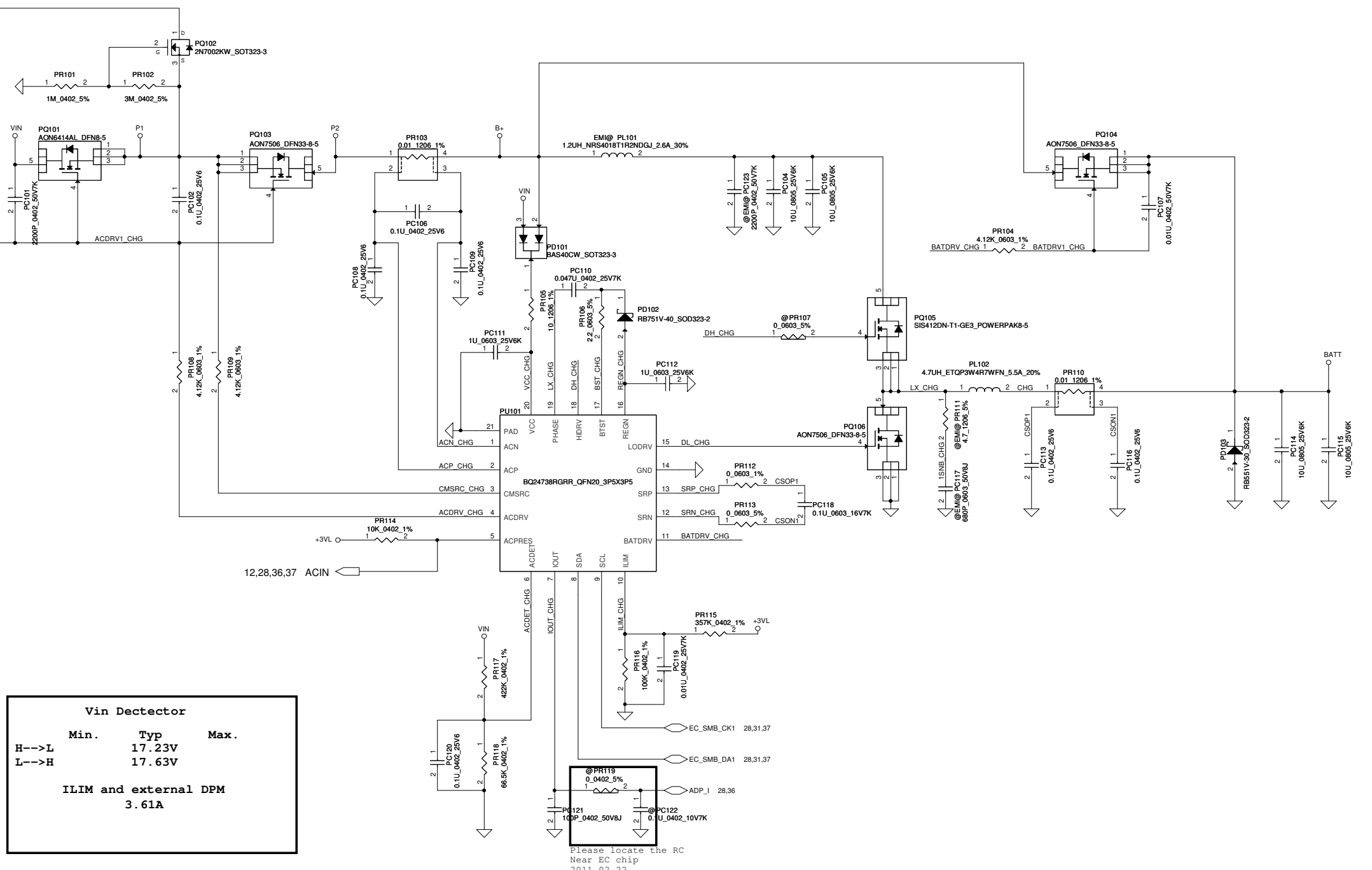
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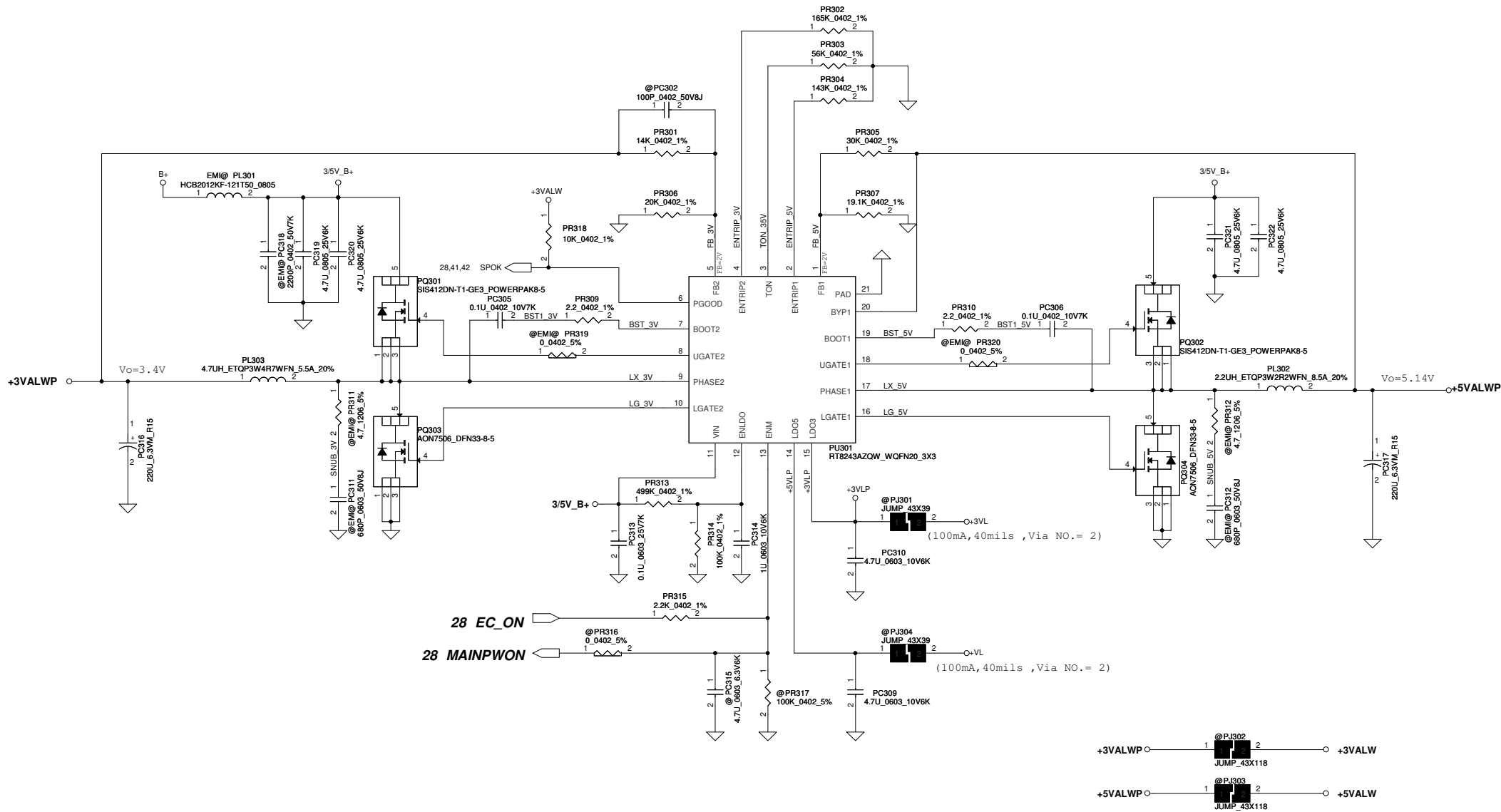
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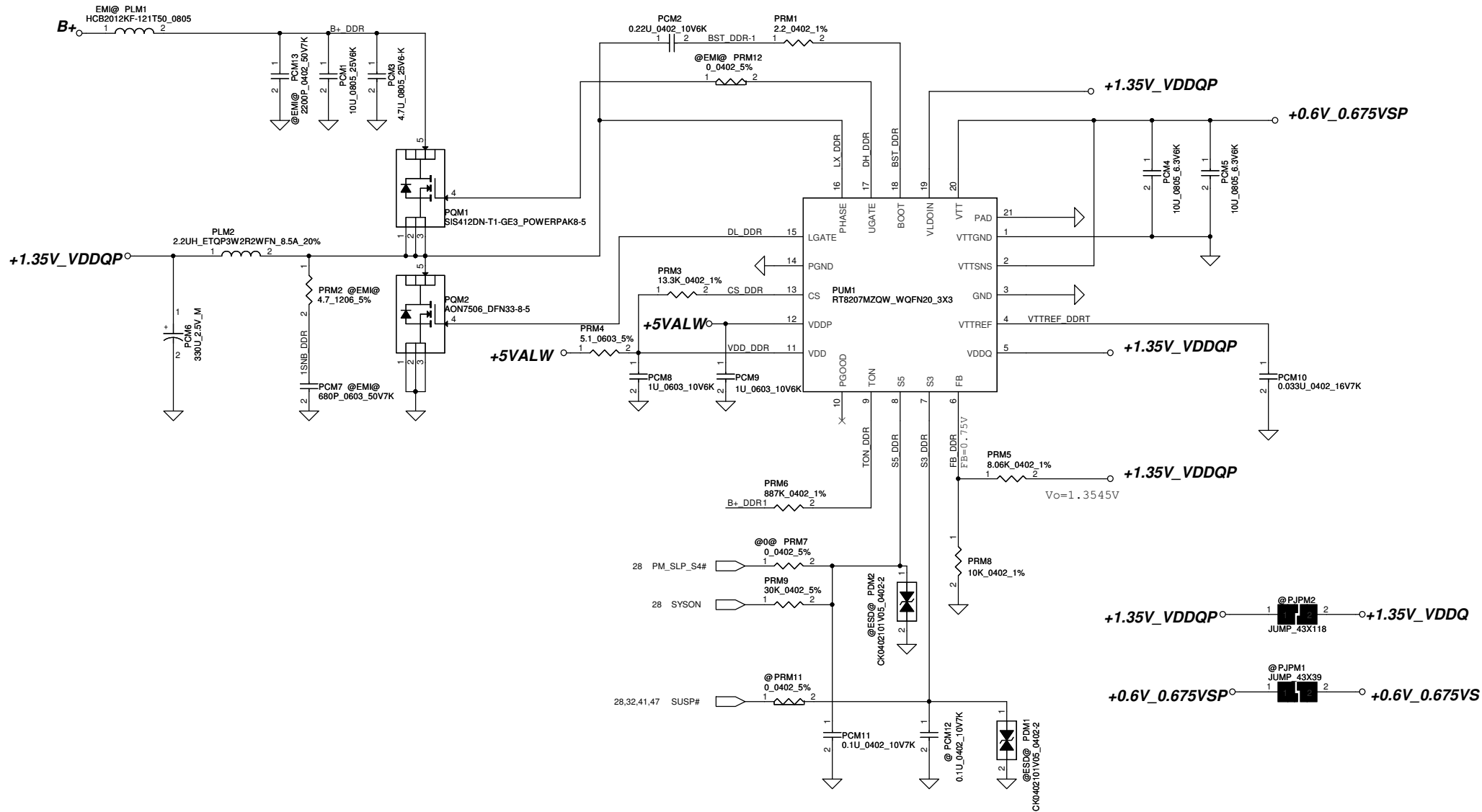
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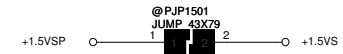
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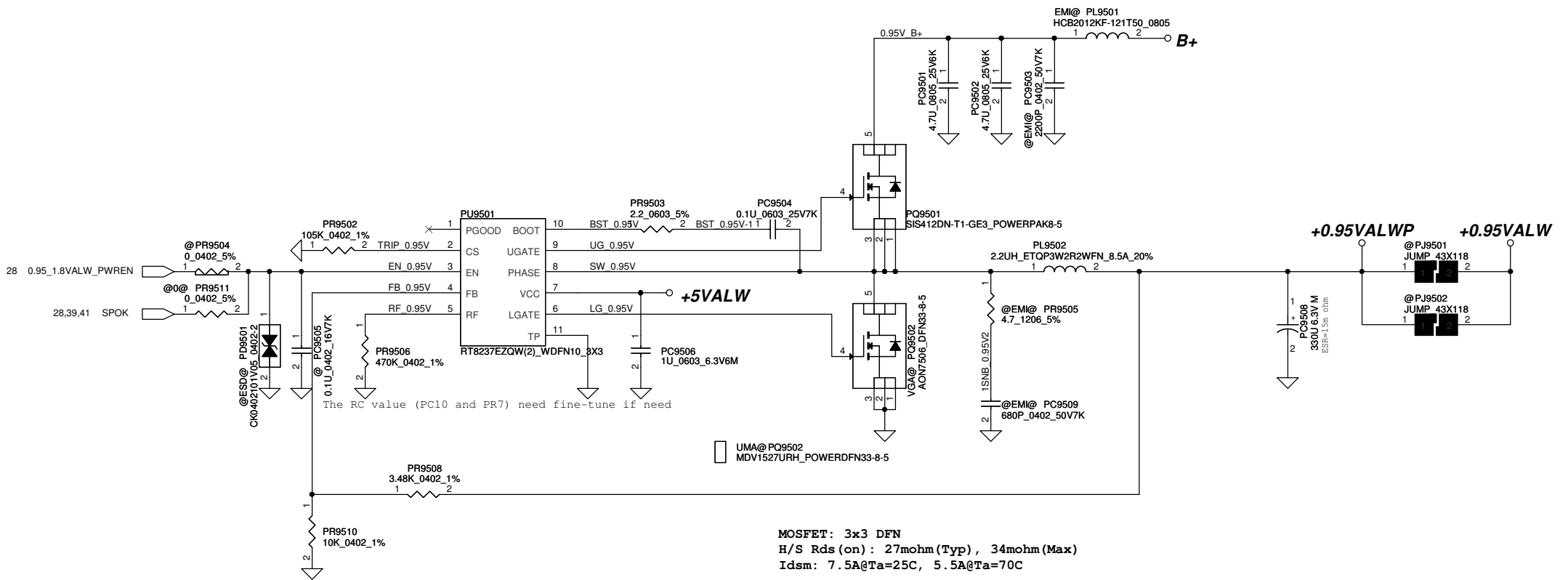
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				Cust	LA-A997P	1.0	
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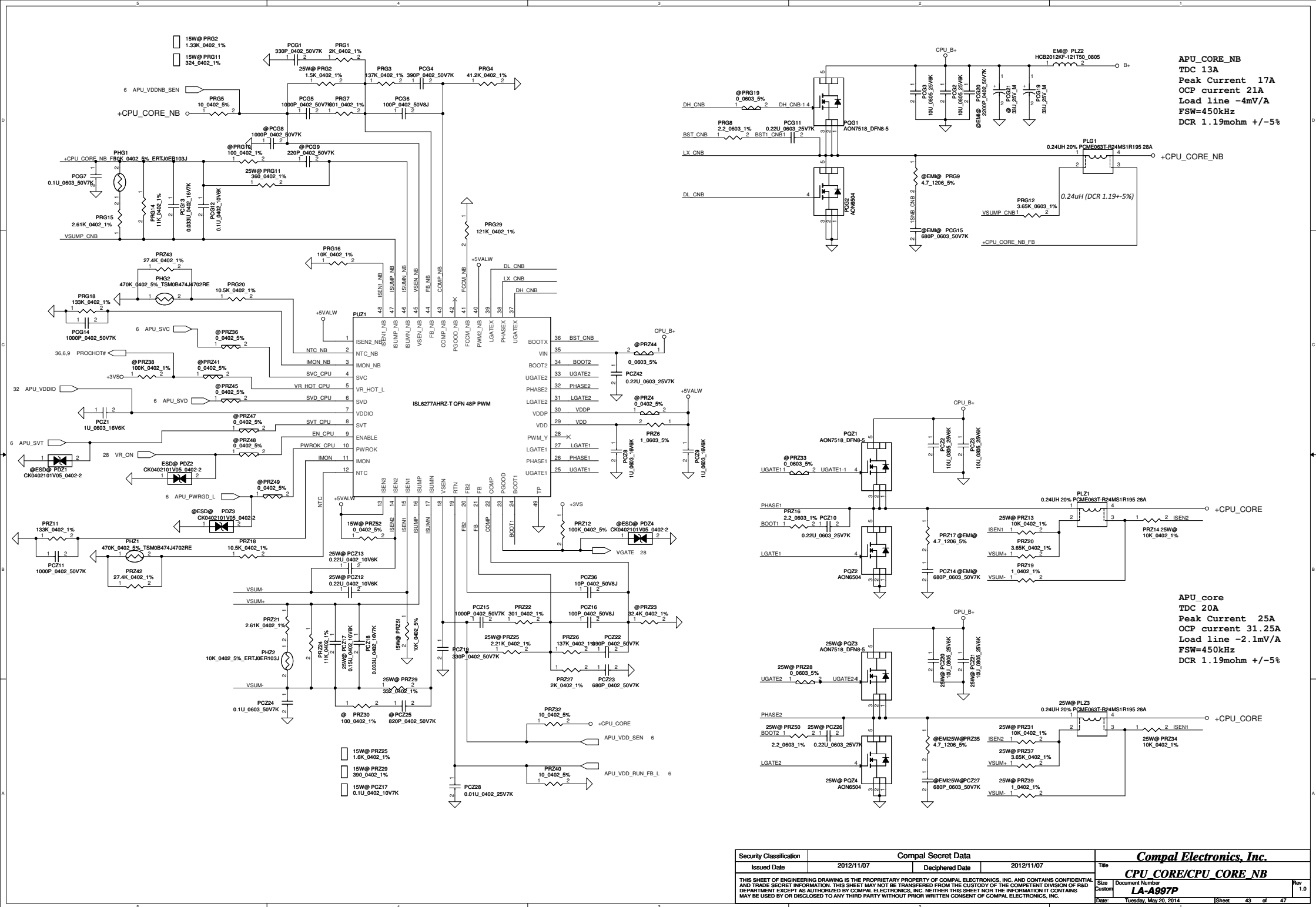
MOSFET: 3x3 DFN
H/S Rds (on): 27mohm (Typ), 34mohm (Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds (on): 9.9mohm (Typ), 13mohm (Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

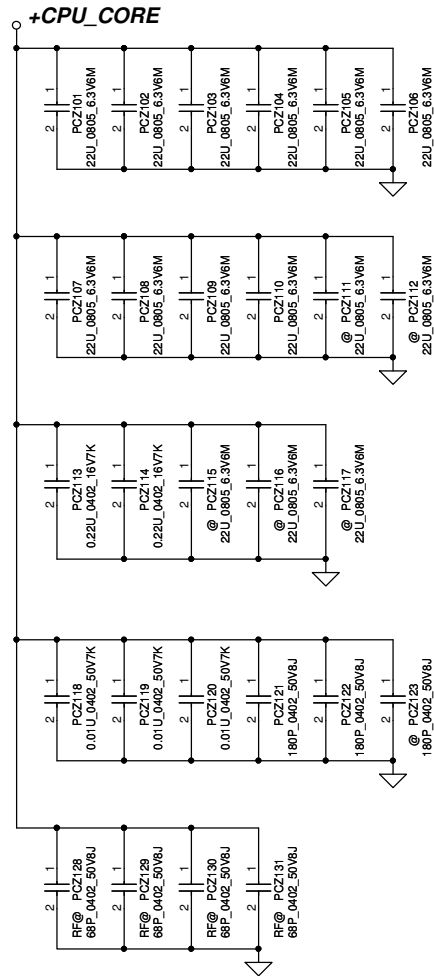
Choke: 7x7x3
Rdc=15.5mohm +/-15%

Switching Frequency: 290kHz
Imax=8A
OCP~10.977A
OVP: 120%~130%
VFB=0.704V, Vout=0.949V
MOSFET footprint: SIS412DN

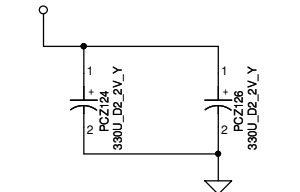
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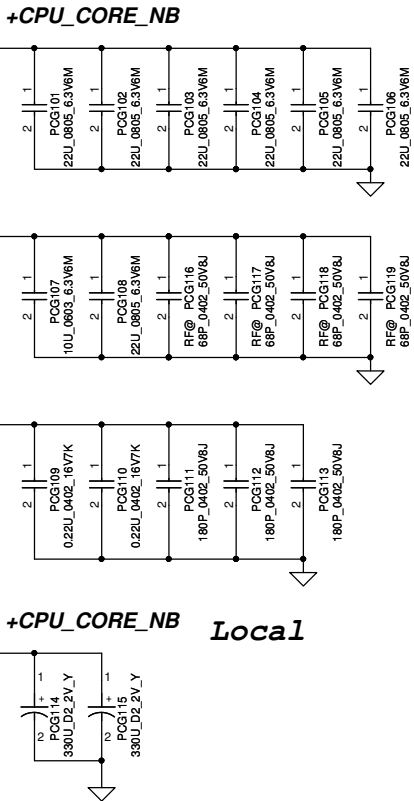
+CPU_CORE



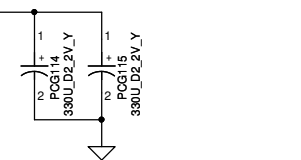
+CPU_CORE Local



+CPU_CORE_NB

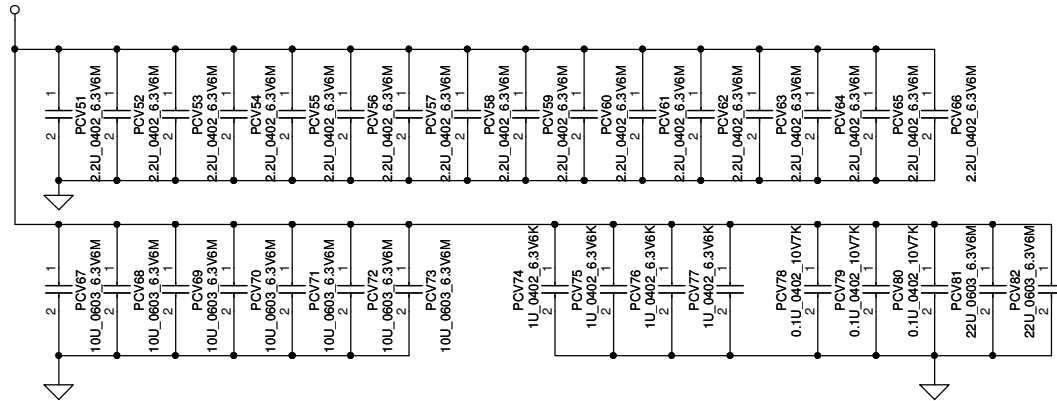


+CPU_CORE_NB Local

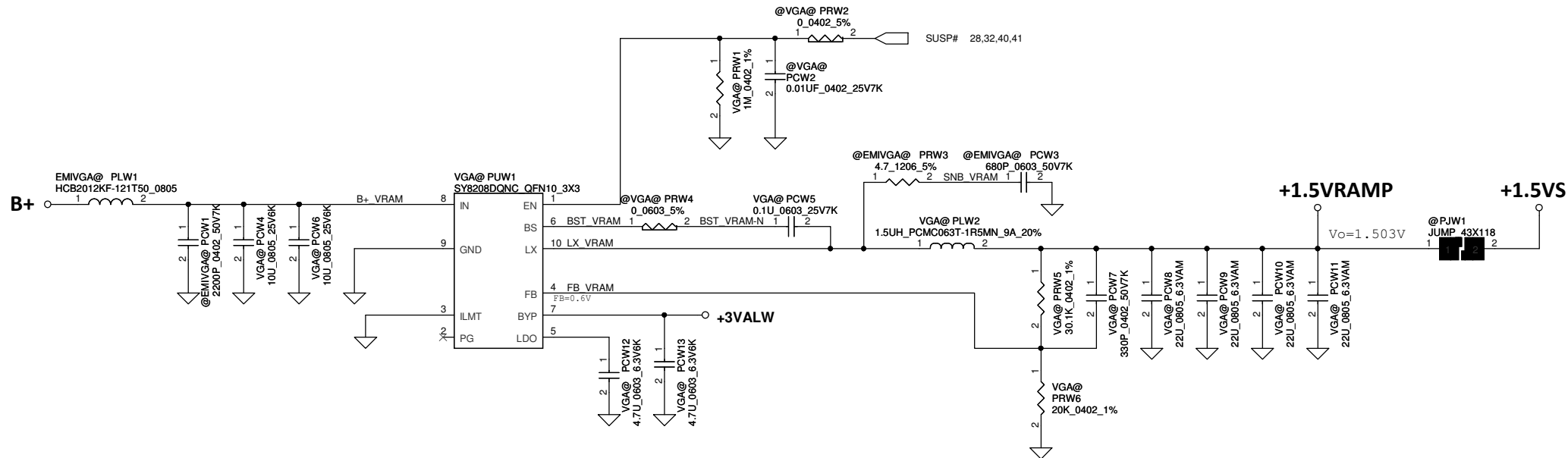


	330uF/9m	22uF/0805	0.22uF/0402	10uF/0603	0.01uF/0402	180pF/0402
+CPU_CORE	2	10	2		3	2
+CPU_CORE_NB	2	7	2	1		3

+VGA_CORE



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