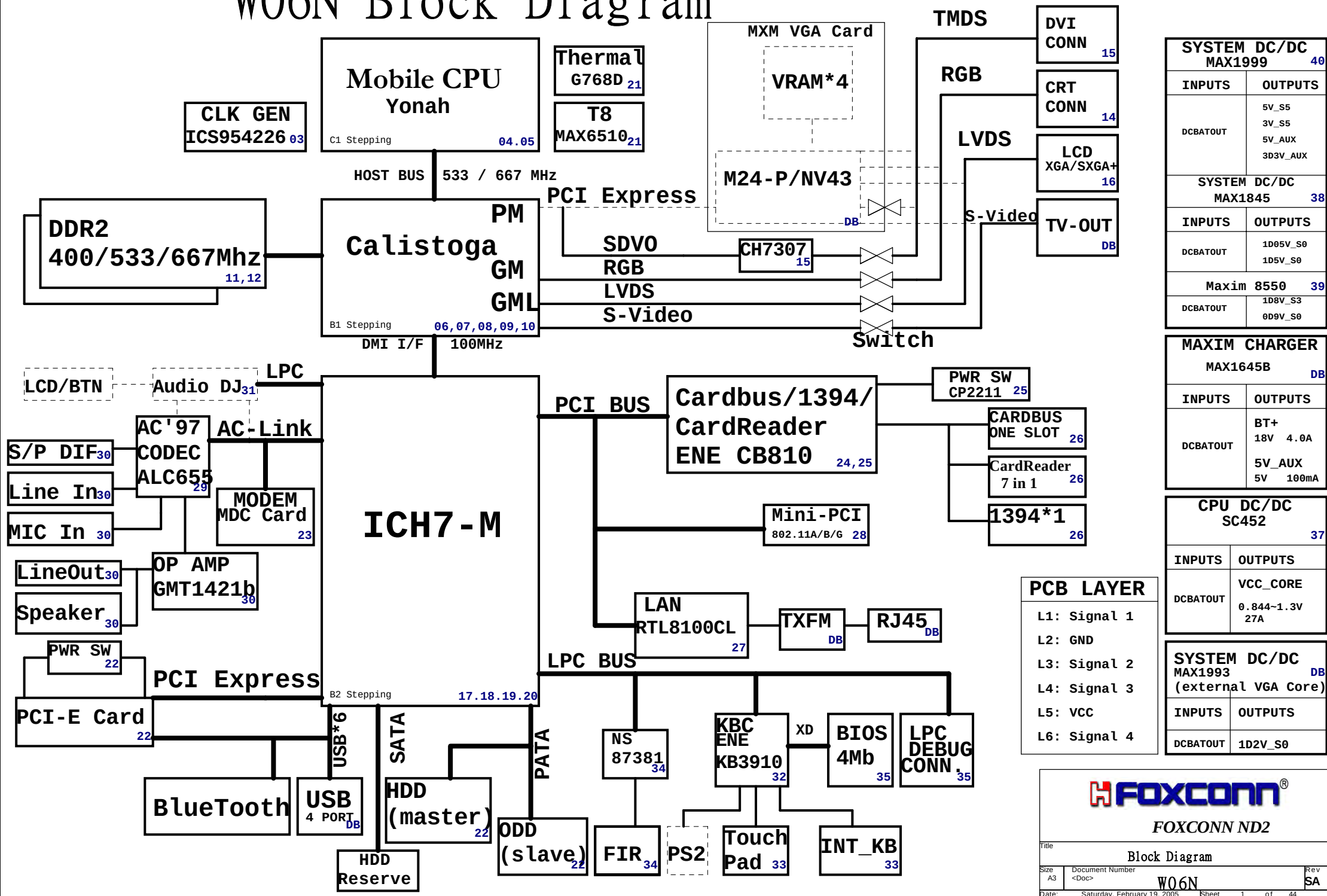


## W06N Block Diagram



# Calistoga Strapping Signals and Configuration

| Pin Name          | Strap Description                                                                                                      | Configuration                                                  |
|-------------------|------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------|
| CFG[2:0]          | FSB Frequency Select                                                                                                   | 001 = FSB533<br>011 = FSB667<br>Others = Reversed              |
| CFG[3:4]          | Reversed                                                                                                               |                                                                |
| CFG5              | DMI x2 Select                                                                                                          | 0 = DMI x2<br>1 = DMI x4 (Default)                             |
| CFG6              | NB strap                                                                                                               | 0 = Moby Dick<br>1 = Calistoga (Default)                       |
| CFG7              | CPU Strap                                                                                                              | 0= Reserved<br>1=Mobility (Default)                            |
| CFG8              | Reversed                                                                                                               |                                                                |
| CFG9              | PCI Express Graphics Lane reverse option for layout convenience                                                        | 0=Reverse Lanes<br>1=Normal Operation (Default)                |
| CFG10             | Reversed                                                                                                               |                                                                |
| CFG11             | Reversed                                                                                                               |                                                                |
| CFG[13:12]        | Reversed<br>Reversed                                                                                                   |                                                                |
| CFG[14:15]        | Reversed<br>Reversed                                                                                                   |                                                                |
| CFG16             | FSB Dynamic ODT                                                                                                        | 0 = Dynamic ODT Disabled<br>1 = Dynamic ODT Enabled (Default)  |
| CFG17             | Reversed                                                                                                               |                                                                |
| CFG18             | GMCH core VCC Select                                                                                                   | 0 = 1.05V (Default)<br>1 = 1.5V                                |
| CFG19             | DMI Lane Reversal                                                                                                      | 0 = Normal(Default)<br>1 = Lanes Reversal                      |
| CFG20             | 0= Only SDV0 or PCIe x1 is operational ( default)<br>1= SDV0 and PCIe x1 are operating simultaneously via the PEG port |                                                                |
| SDV0<br>CTRL_DATA | SDV0 Present                                                                                                           | 0 = No SDV0 device present<br>1= SDV0 device present (Default) |

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

## KBC Hardware Strap

| PinNumber | PinName | Function                                                                                                                                         |
|-----------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 125       | A1      | High:Enable the internal pull-up resistors on XIOCS [F:0] pins<br>Low:Disable the internal pull-up resistors on XIOCS [F:0]                      |
| 128       | A4      | High: Diasble DMPP(Recommended)<br>Low : Enable DMPP                                                                                             |
| 131       | A5      | High:Enable EMWB(Recommended for application using shared BIOS<br>Low:Disable EMWB                                                               |
| 11        | GPI005  | High:Test Mode<br>Low:32KHz c lock in normal running(Recommend)                                                                                  |
| 12        | GPI006  | High:Test Mode(KSOUT0~15 become DPLL internal data outputs,<br>KS016 becomes internal power-on reset output<br>Low:Normal operation(Recommended) |
| 105       | GPI020  | High:Normal operation(Recommended)<br>Low:Enable ISP mode during which the RD#,WR#,MEMSEL#,A[20:0] andD[7:0]will be controlled by ISP Contriller |

# ICS954226 Spread Spectrum Select

| Byte 6b7 | Byte 6b6 | byte 6b5 | Byte 6b4 | Spread Mode | Spread Amount% | Pin17/18 Mhz |
|----------|----------|----------|----------|-------------|----------------|--------------|
| 1        | 0        | 0        | 0        | Down        | 0.8            | 100          |
| 1        | 0        | 0        | 1        | Down        | 1.25           | 100          |
| 1        | 0        | 1        | 0        | Down        | 1.75           | 100          |
| 1        | 0        | 1        | 1        | Down        | 2.5            | 100          |
| 1        | 1        | 0        | 0        | Center      | +0.3           | 100          |
| 1        | 1        | 0        | 1        | Center      | +0.5           | 100          |
| 1        | 1        | 1        | 0        | Center      | +0.8           | 100          |
| 1        | 1        | 1        | 1        | Center      | +1.25          | 100          |

## PCI Routing

|         | IDSEL | IRQ | REQ/GNT |
|---------|-------|-----|---------|
| CB810   | 25    | E   | 0       |
| MiniPCI | 21    | G   | 1       |
| LAN     | 23    | F   | 2       |
| 1394    | 19    | E   | 3       |

## ICH7-M IDE Integrated Series Termination Resistors

|                                                                                  |                      |
|----------------------------------------------------------------------------------|----------------------|
| DD[15:0], DIOW#, DIOR#, DREQ,<br>DDACK#, IORDY, DA[2:0], DCS1#,<br>DCS3#, IDEIRQ | approximately 33 ohm |
|----------------------------------------------------------------------------------|----------------------|

# ICH7-M Integrated Pull-up and Pull-down Resistors

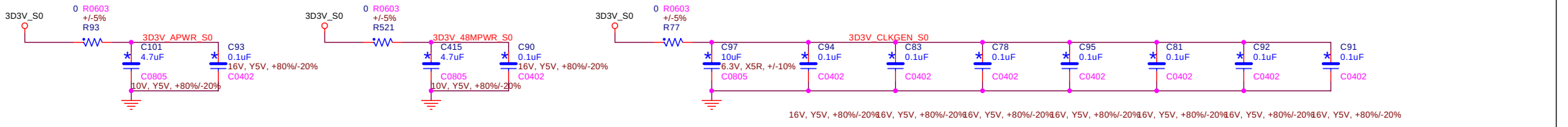
|                                                                                                                                                                                      |                                |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|
| EE_DIN, EE_DOUT, GNT[3:0]<br>GNT[4]#/GPO[48], GNT[5]#/GPO[17],<br>GNT[6]#/GPO[16], GPIO[25]<br>LAD[3:0]#/FB[3:0]#, LAN_RXD[2:0],<br>LDRQ[0], LDRQ[1]/GPI[41],PME#,<br>PWRBTN#, TP[3] | ICH7 internal 20K pull-ups     |
| SATALED#                                                                                                                                                                             | ICH7 internal 15K pull-ups     |
| ACZ_BITCLK, ACZ_RST#, ACZ_SDIN[2:0],<br>ACZ_SDOUT, ACZ_SYNC, DPRSTP#                                                                                                                 | ICH7 internal 20K pull-downs   |
| DPRSLPVR, EE_CS,SPKR,SPI_ARB, SPI_CLK,                                                                                                                                               |                                |
| USB[7:0][P,N]                                                                                                                                                                        | ICH7 internal 15K pull-downs   |
| DD[7], DDREQ                                                                                                                                                                         | ICH7 internal 11.5K pull-downs |
| LAN_CLK                                                                                                                                                                              | ICH7 internal 100K pull-downs  |

## ICH7-M Strapping Options

|          |                                                                                                                                                                                                                                                                                                                                                   |
|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| INTVRMEN | This signal enables the internal VccSus1_5V suspend regulator when connected to VccRTC. When connected to GND, the internal regulator is disabled.<br>To enable internla VccSus1_5V VRM pull signal to VccRTC via 330Kohm                                                                                                                         |
| SPKR     | The signal has a weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (ICH7M will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit. NOTE: Please refer to ICH7M EDS Rev0.5 (or latest) for all ICH7M Strap details. |

| Pin Name                                | Strap Description               | Configuration                                                            |
|-----------------------------------------|---------------------------------|--------------------------------------------------------------------------|
| GNT3#                                   | Top-Block Swap Override         | Internal Pull-up for top-block swap mode.                                |
| LINKALERT#                              | Reversed                        |                                                                          |
| SPKR                                    | No Reboot                       | Internal pull-down to indicate system is strapped to the no reboot more. |
| INTVRMEN                                | VccSus1_05 VRM Enable/Disable.  | 0 = Disable (Default)<br>1 = Enable                                      |
| GPIO25                                  | Reserved                        |                                                                          |
| EE_CS                                   | Reversed                        |                                                                          |
| GNT5#<br>/GPIO17#.<br>GNT4#<br>/GPIO48. | Boot BIOS Destination Selection | 01 = SPI<br>10 = PCI<br>11 = LPC (Default)                               |
| EE_DOUT                                 | Reversed                        |                                                                          |
| ACZ_SDOUT                               | XOR Chain Entrance              | 0 = Allow XOR Testing (Default)<br>1 = Not Allow                         |
| ACZ_SYNC                                | PCI-E Port CFG Bit 0            | Reversed                                                                 |
| GPIO16/<br>DPRSLPVR                     | Reversed                        |                                                                          |
| SATALED#                                | Reversed                        |                                                                          |
| REQ[4:1]#                               | XOR Chain Selection             | Not available in Datasheet Yet                                           |
| TP3                                     | XOR Chain Entrance              | Not available in Datasheet Yet                                           |

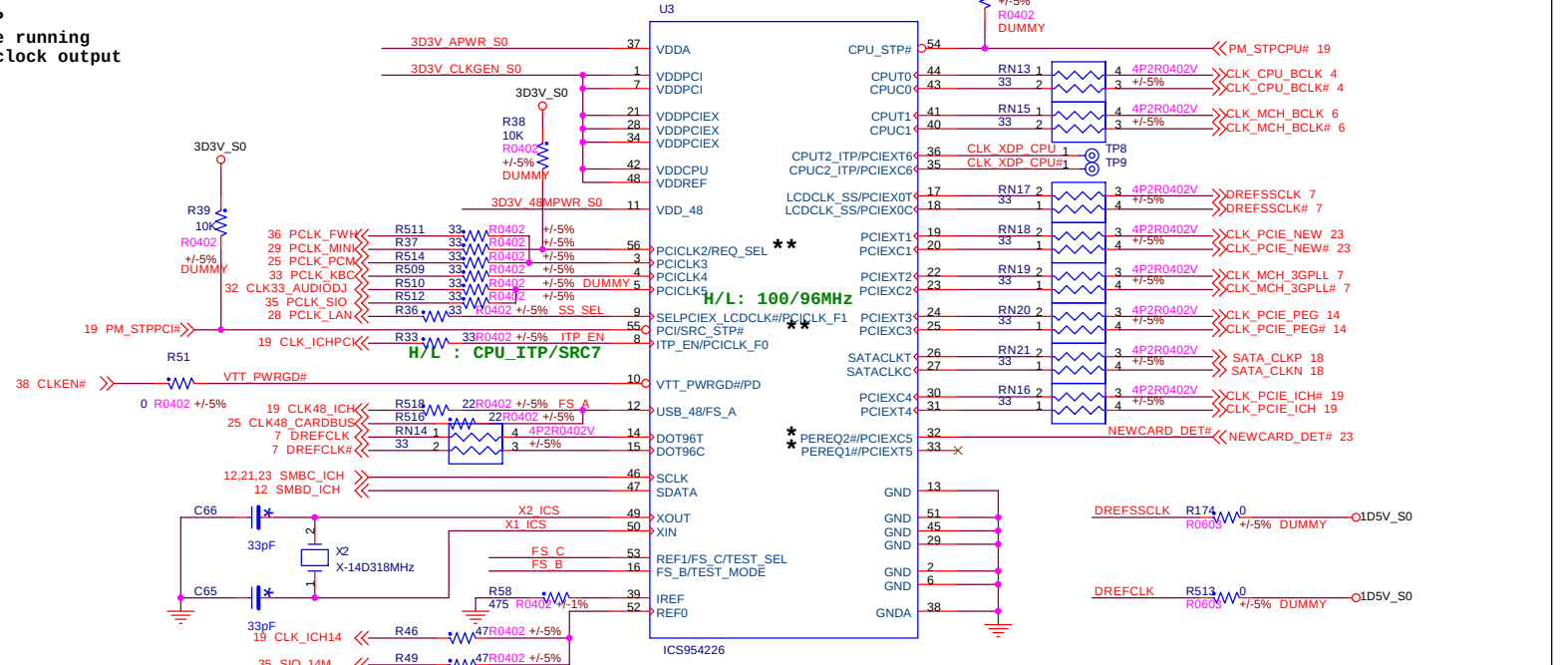
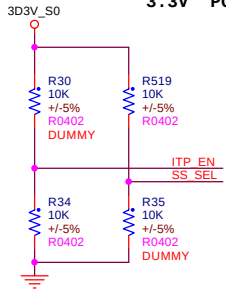
|                                                                                                      |                             |               |           |
|------------------------------------------------------------------------------------------------------|-----------------------------|---------------|-----------|
| <br>FOXCONN ND2 |                             |               |           |
| Title<br>Table of content                                                                            |                             |               |           |
| Size<br>A3                                                                                           | Document Number<br><Doc>    | W06N          | Rev<br>SA |
| Date:                                                                                                | Saturday, February 19, 2005 | Sheet 2 of 44 |           |



ITP\_EN  
SS\_SEL

0=PCIEX\_6  
0=LCDCLK

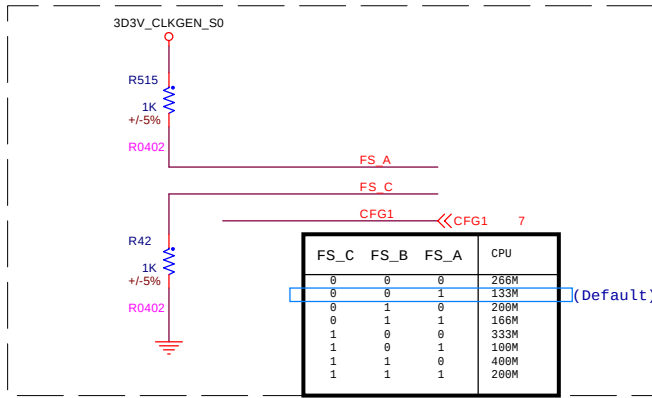
1=CPU\_2\_ITP  
1=PCIEX/free running  
3.3V PCI clock output



\*internal Pull-Up resistors  
\*\*internal Pull-Down resistor

EMI capacitor

|               |      |      |       |                 |       |
|---------------|------|------|-------|-----------------|-------|
| CLK_ICH14     | C80  | 10pF | C0402 | 50V, NPO, +/-5% | DUMMY |
| CLK33_AUDIODJ | C405 | 10pF | C0402 | 50V, NPO, +/-5% | DUMMY |
| PCLK_PCM      | C413 | 10pF | C0402 | 50V, NPO, +/-5% | DUMMY |
| PCLK_MINI     | C77  | 10pF | C0402 | 50V, NPO, +/-5% | DUMMY |
| PCLK_KBC      | C404 | 10pF | C0402 | 50V, NPO, +/-5% | DUMMY |
| CLK_ICHPCI    | C64  | 10pF | C0402 | 50V, NPO, +/-5% | DUMMY |
| CLK48_ICH     | C414 | 10pF | C0402 | 50V, NPO, +/-5% | DUMMY |
| PCLK_SIO      | C411 | 10pF | C0402 | 50V, NPO, +/-5% | DUMMY |
| SIO_14M       | C82  | 10pF | C0402 | 50V, NPO, +/-5% | DUMMY |



| FS_C | FS_B | FS_A | CPU  |
|------|------|------|------|
| 0    | 0    | 0    | 266M |
| 0    | 0    | 1    | 133M |
| 0    | 1    | 0    | 200M |
| 0    | 1    | 1    | 166M |
| 1    | 0    | 0    | 333M |
| 1    | 0    | 1    | 100M |
| 1    | 1    | 0    | 400M |
| 1    | 1    | 1    | 200M |

|               |     |                  |
|---------------|-----|------------------|
| CLK_PCIE_ICH  | R59 | 49.9 R0402 +/-1% |
| CLK_PCIE_ICH# | R60 | 49.9 R0402 +/-1% |
| DREFSSCLK#    | R62 | 49.9 R0402 +/-1% |
| DREFSSCLK     | R61 | 49.9 R0402 +/-1% |
| CLK_PCIE_NEW  | R63 | 49.9 R0402 +/-1% |
| CLK_PCIE_NEW# | R64 | 49.9 R0402 +/-1% |
| DREFCLK       | R53 | 49.9 R0402 +/-1% |
| DREFCLK#      | R55 | 49.9 R0402 +/-1% |
| SATA_CLKP     | R69 | 49.9 R0402 +/-1% |
| SATA_CLKN     | R70 | 49.9 R0402 +/-1% |

|                |     |                  |
|----------------|-----|------------------|
| CLK_CPU_BCLK   | R52 | 49.9 R0402 +/-1% |
| CLK_CPU_BCLK#  | R54 | 49.9 R0402 +/-1% |
| CLK_MCH_BCLK   | R56 | 49.9 R0402 +/-1% |
| CLK_MCH_BCLK#  | R57 | 49.9 R0402 +/-1% |
| CLK_PCIE_PEG   | R67 | 49.9 R0402 +/-1% |
| CLK_PCIE_PEG#  | R68 | 49.9 R0402 +/-1% |
| CLK_MCH_3GPLL  | R66 | 49.9 R0402 +/-1% |
| CLK_MCH_3GPLL# | R65 | 49.9 R0402 +/-1% |

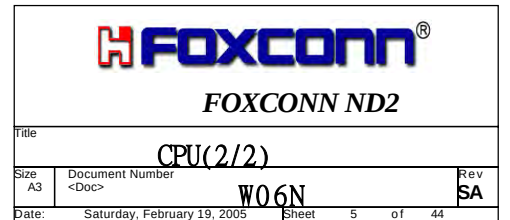
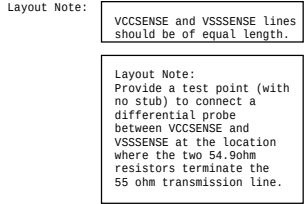


FOXCONN ND2

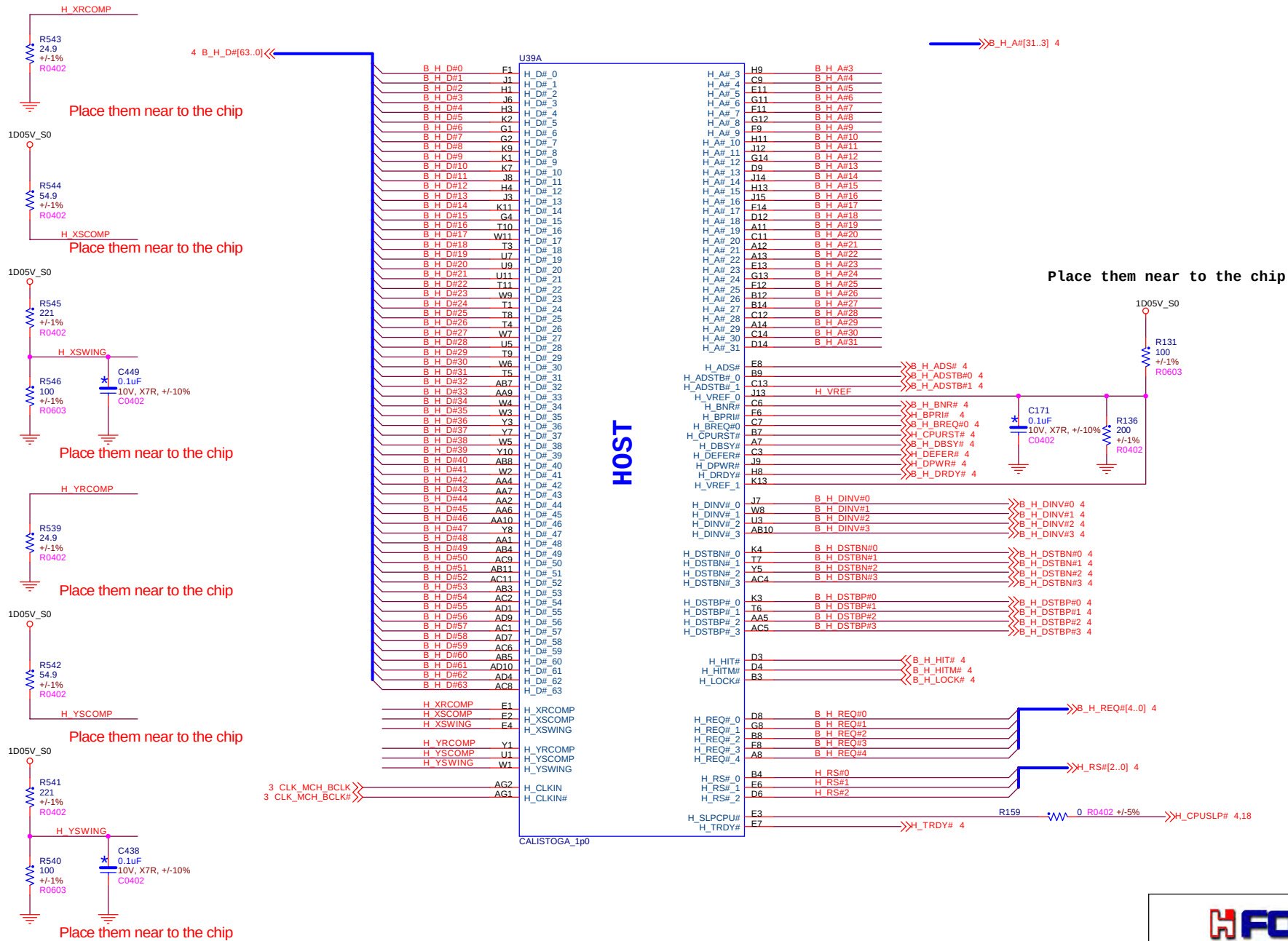
Clock Generator

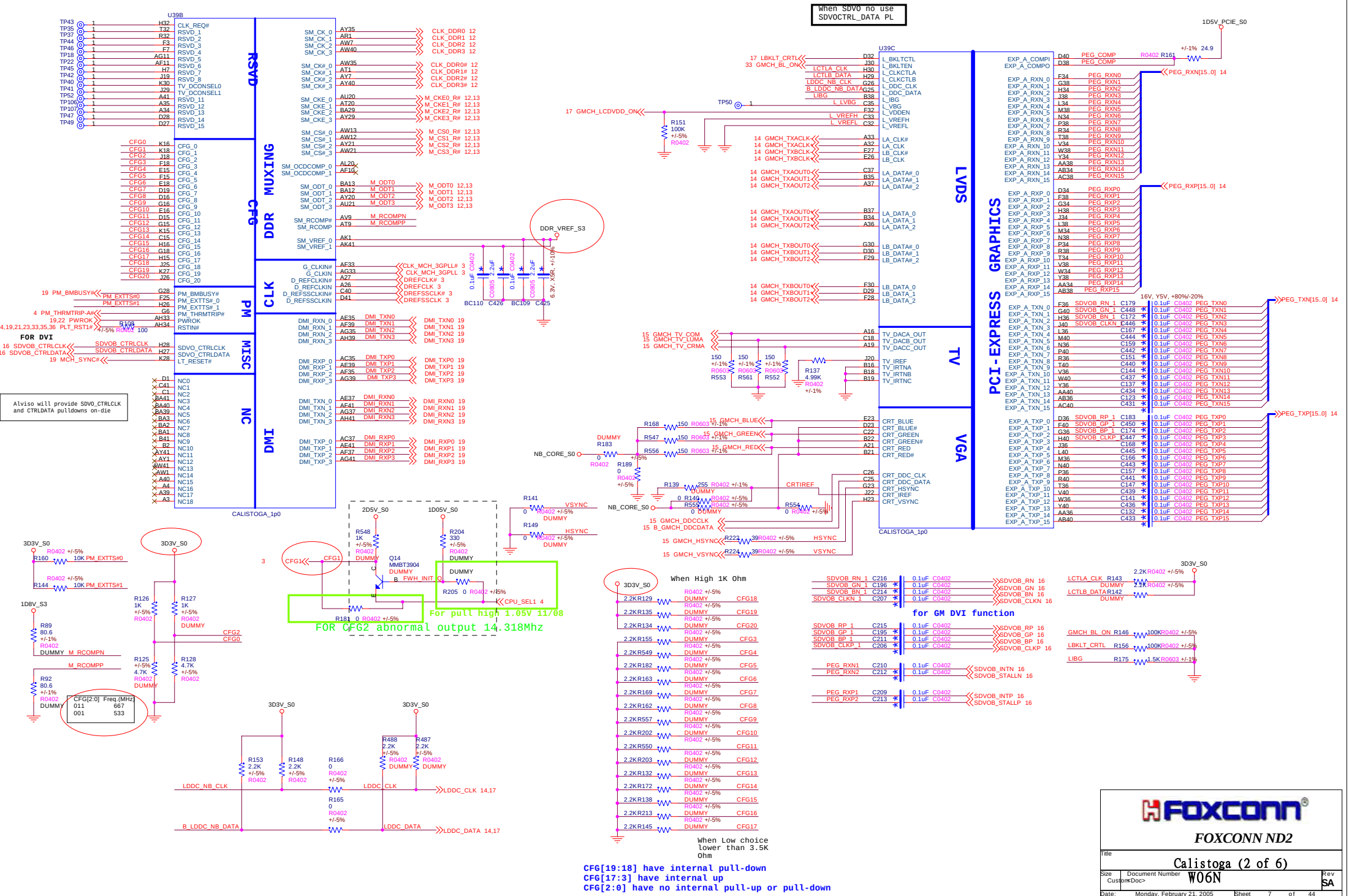
|       |                             |       |         |
|-------|-----------------------------|-------|---------|
| Title | Clock Generator             |       |         |
| Size  | Document Number             | W06N  | Rev     |
| A3    | <Doc>                       |       | SA      |
| Date: | Saturday, February 19, 2005 | Sheet | 3 of 44 |

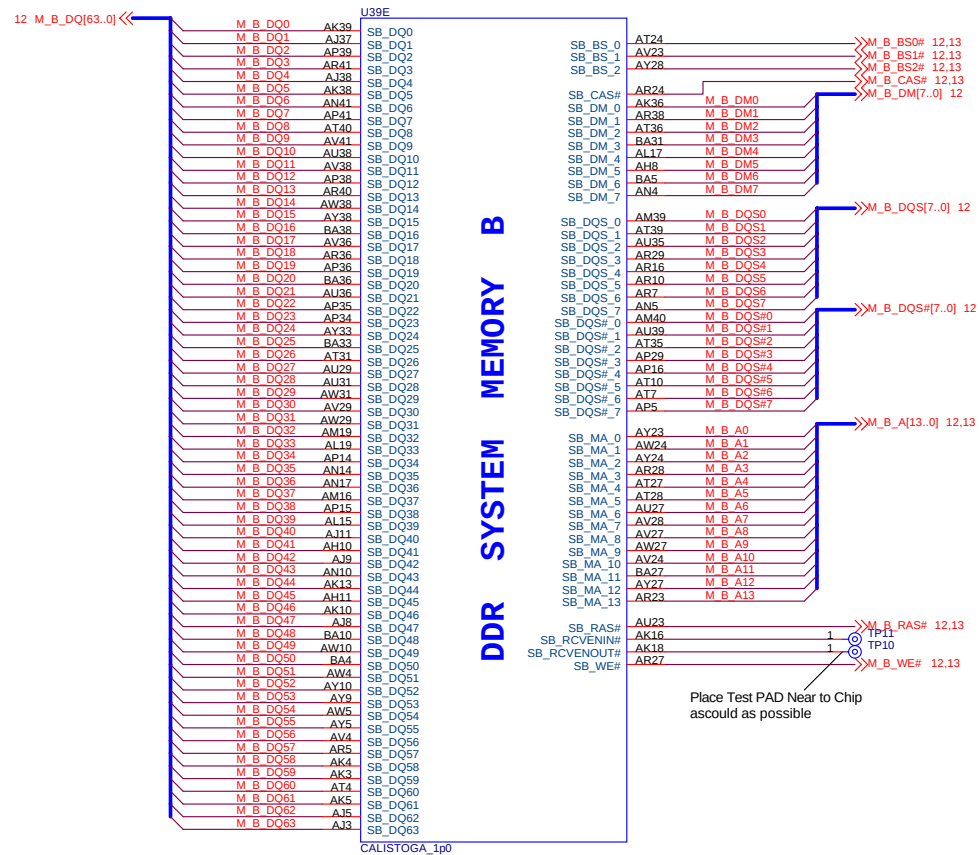
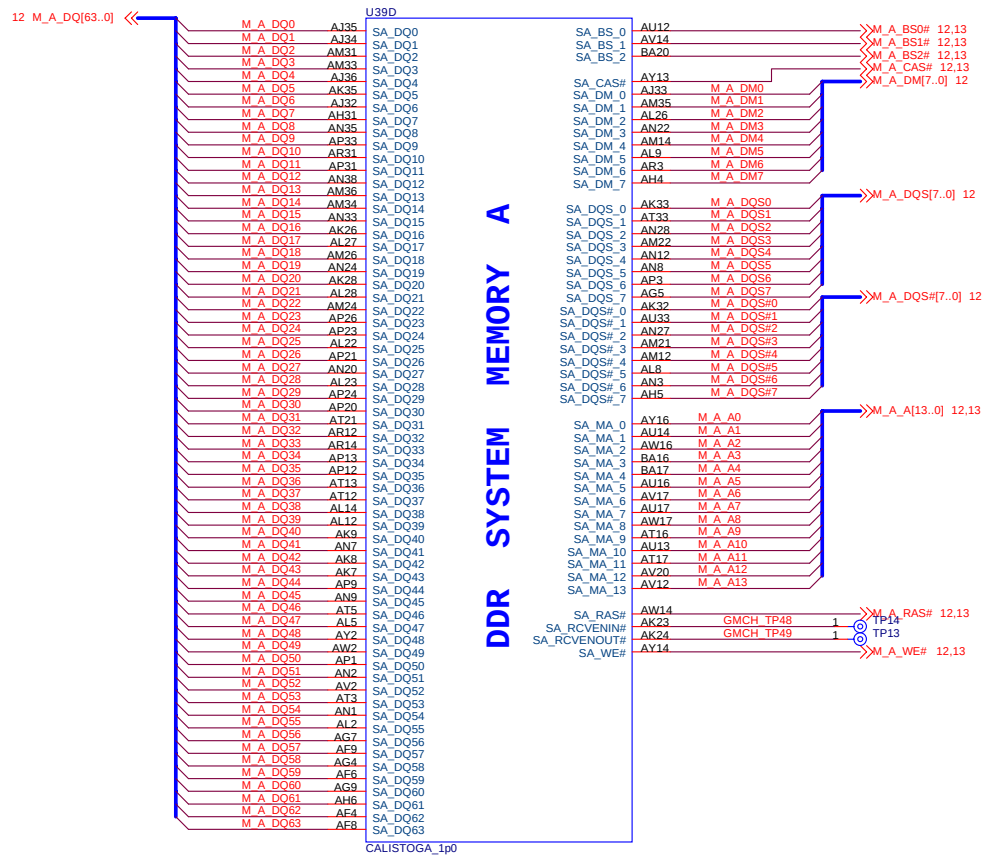
Date: Monday, February 21, 2005 Sheet 4 of 44







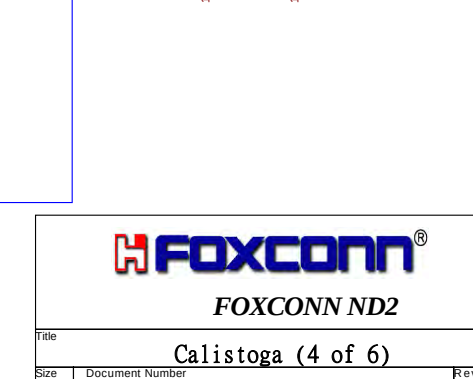
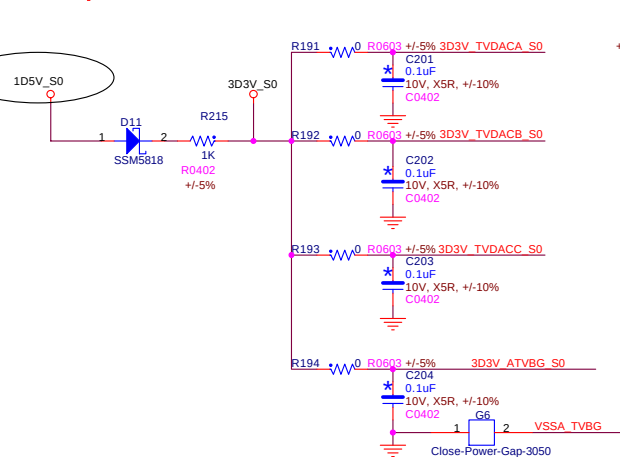




FOXCONN ND2

|               |                             |       |         |
|---------------|-----------------------------|-------|---------|
| Title         | Calistoga (3 of 6)          |       |         |
| Size          | Document Number             | Rev   | SA      |
| Customer Doc# | W06N                        |       |         |
| Date:         | Saturday, February 19, 2005 | Sheet | 8 of 44 |





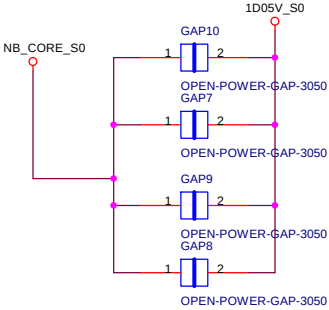
|                                                                                                      |                                                                                                        |
|------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|
| Layout Notes: VSSA_CRTDAC<br>Route caps within 250mil<br>of Alviso. Route FB<br>within 3" of Alviso. | Route VSSA_CRTDAC gnd from GMCH to<br>decoupling cap ground lead and then<br>connect to the gnd plane. |
|------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|

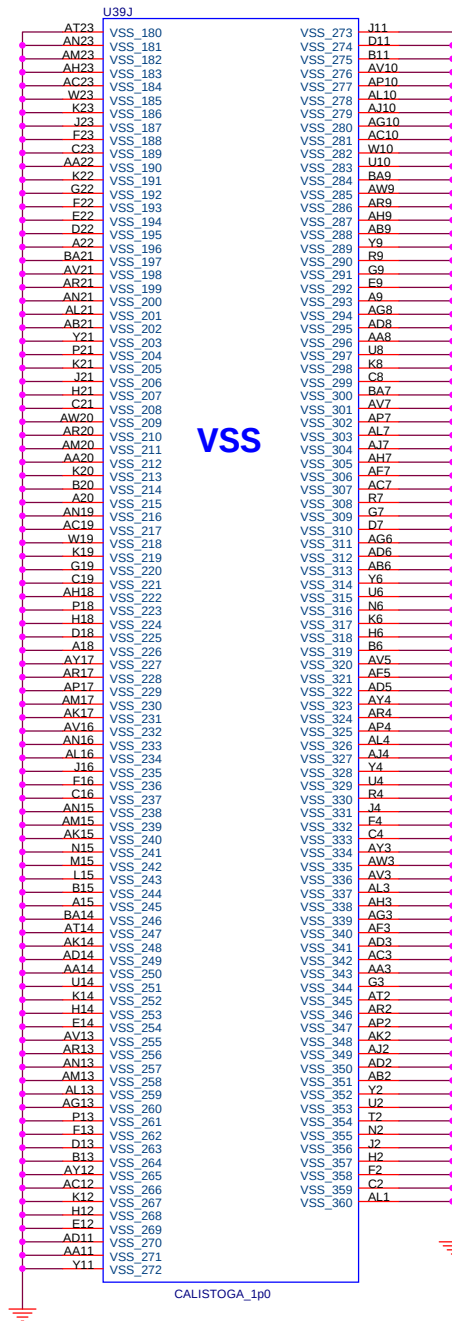
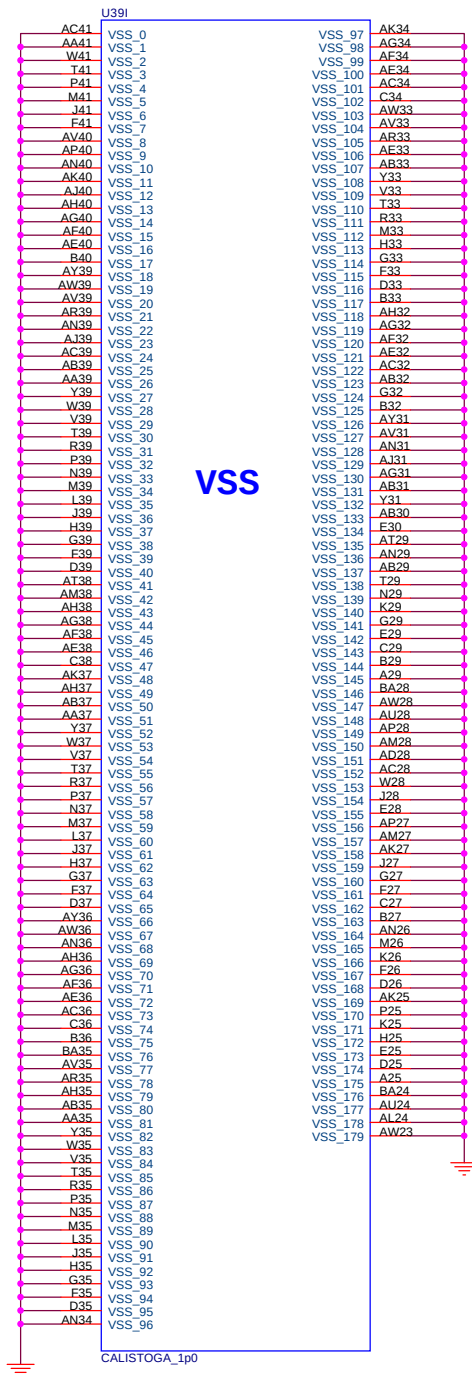
Route ASSATVBG gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane

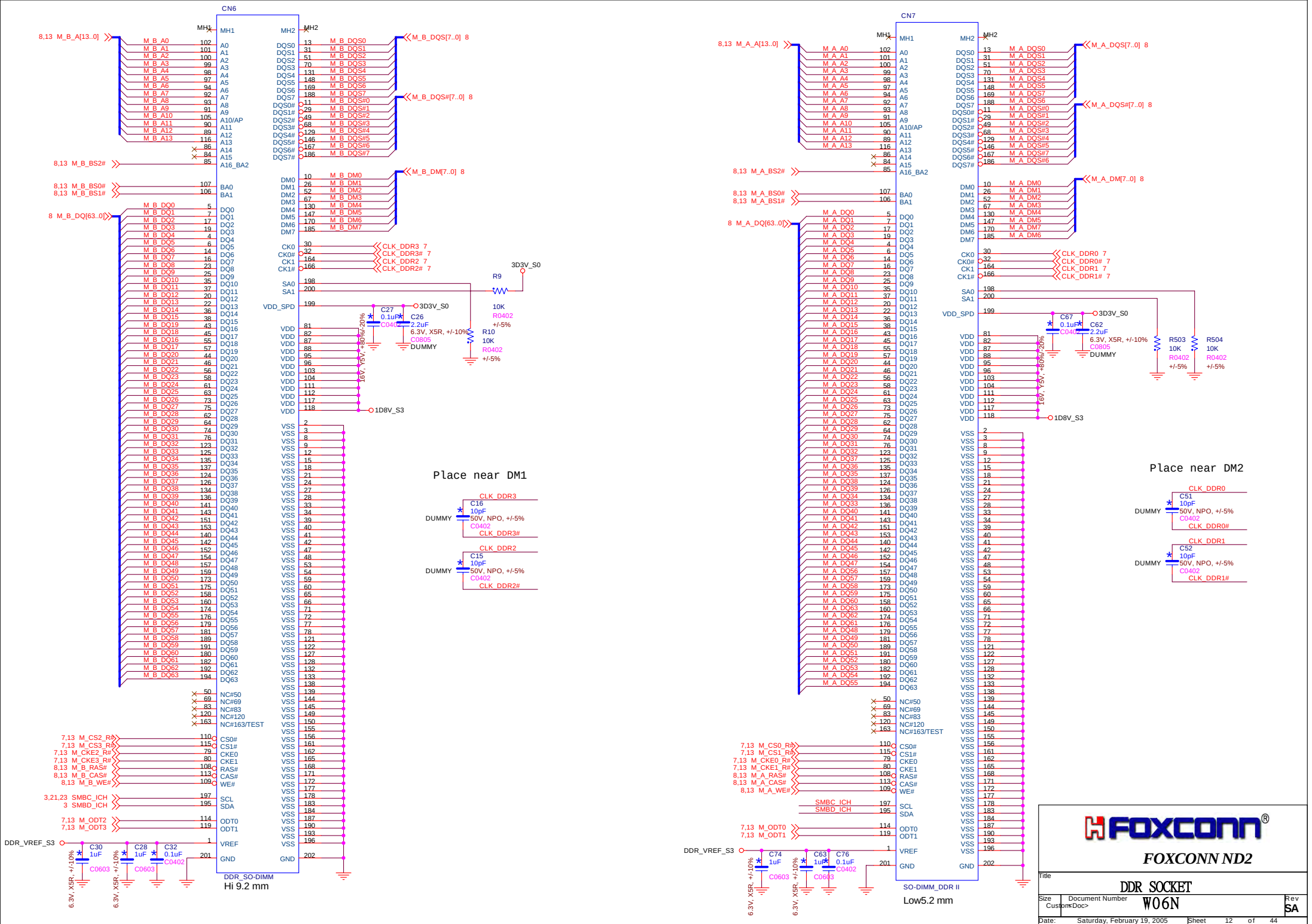


Calistoga (4 of 6)

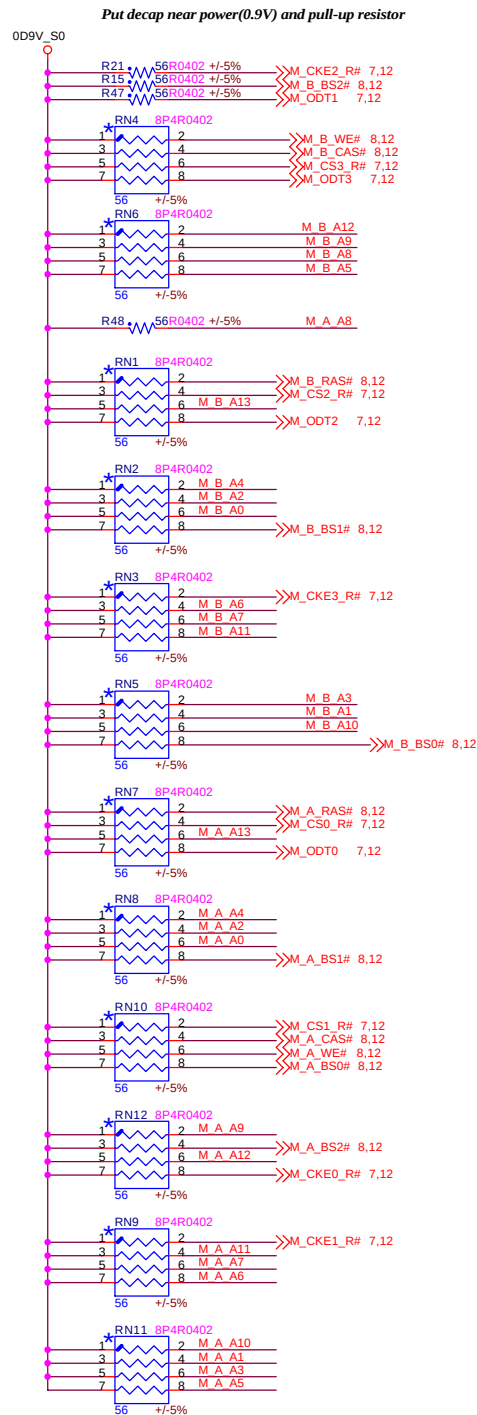
|             |                           |               |
|-------------|---------------------------|---------------|
| Size        | Document Number           | Rev           |
| Custom<Doc> | W06N                      | SA            |
| Date        | Monday, February 21, 2005 | Sheet 6 of 11 |



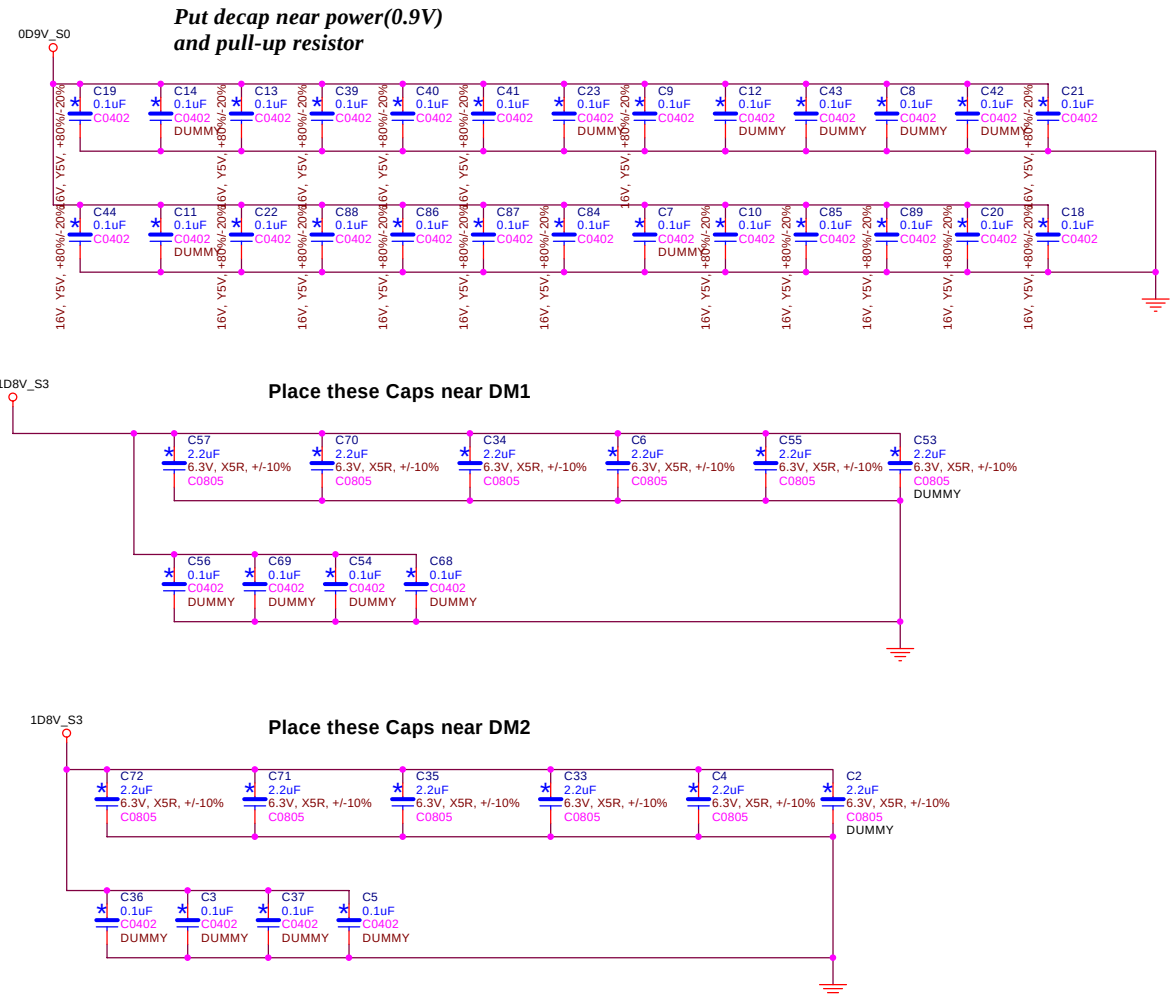




# PARALLEL TERMINATION



## Decoupling Capacitor



**FOXCONN®**

**FOXCONN ND2**

Title  
**DDR Termination Resistor**

Size  
A3 Document Number

**W06N**

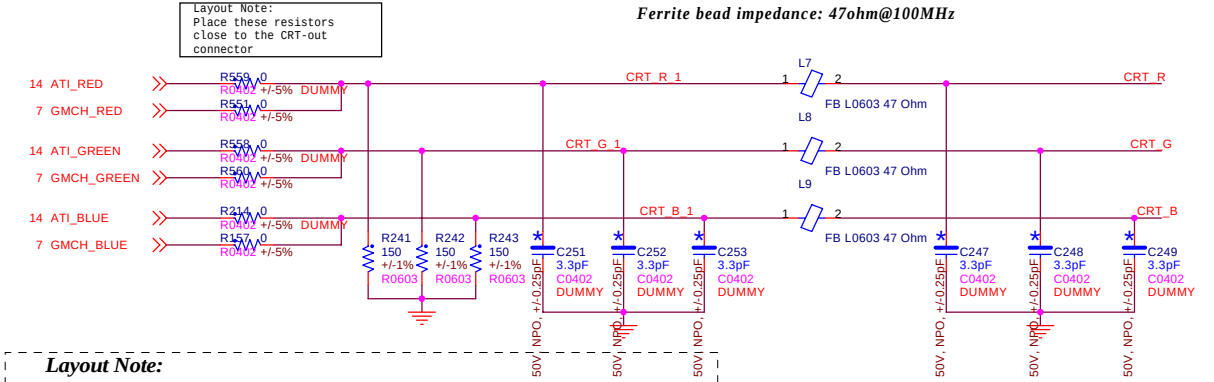
Rev  
SA

Date: Saturday, February 19, 2005 Sheet 13 of 44

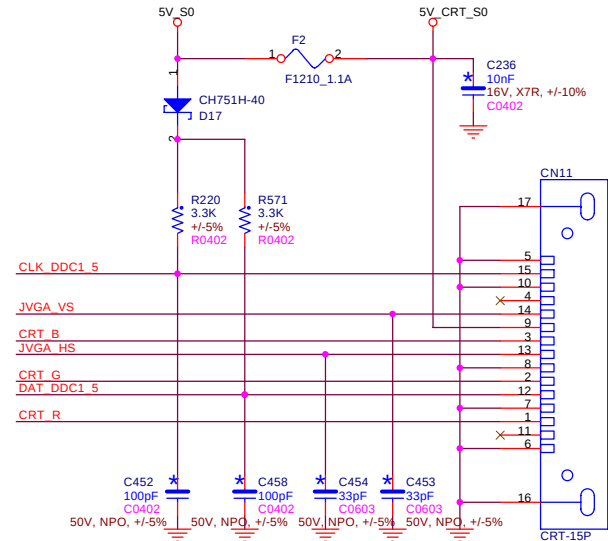
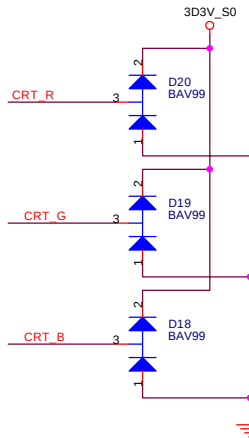
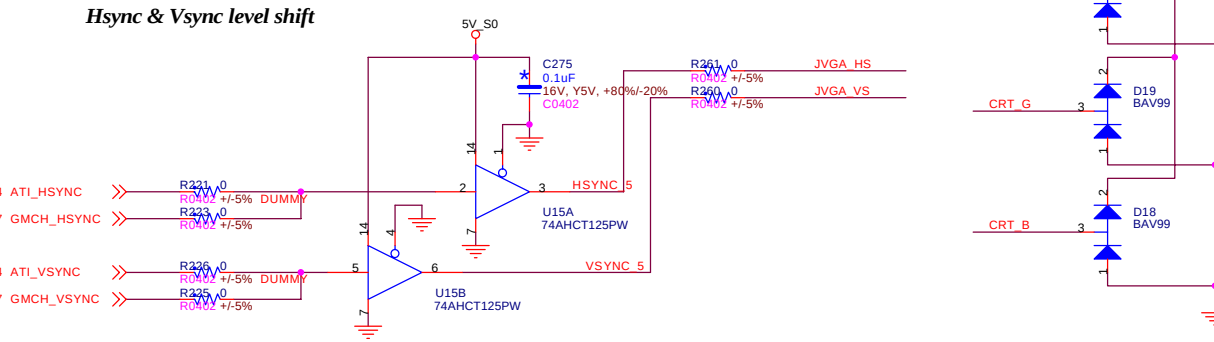




# CRT I/F & CONNECTOR

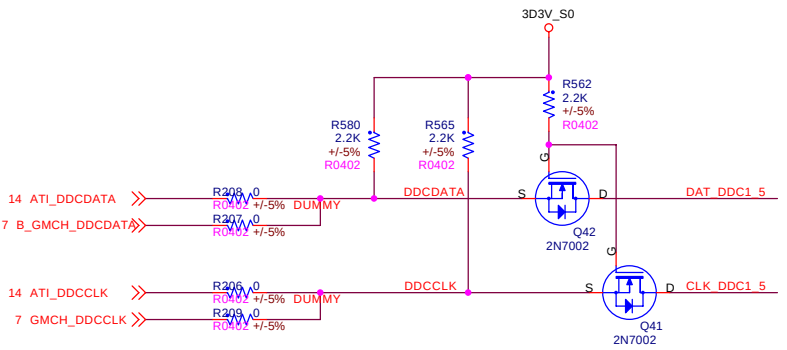


**Layout Note:**  
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



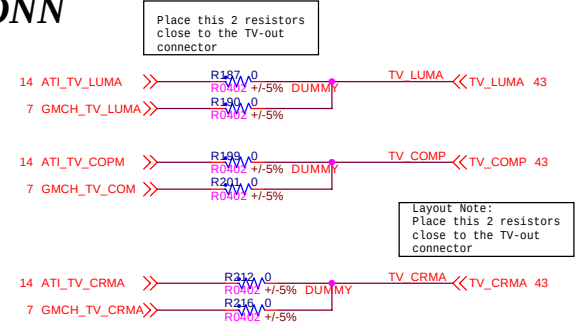
Change VCC from 3.3V to 2.5V 10/27 03'

**DDC\_CLK & DATA level shift**



5V @ ext. CRT side

## TV OUT CONN

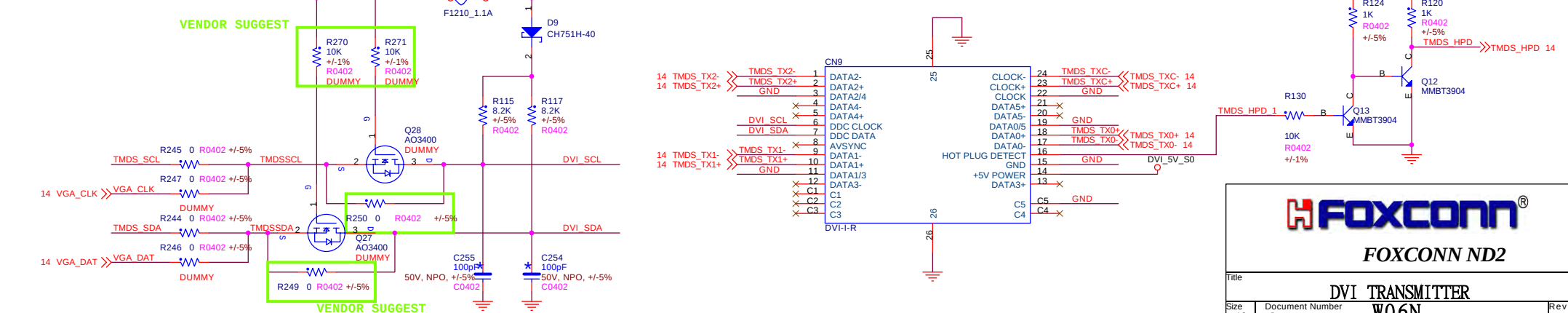
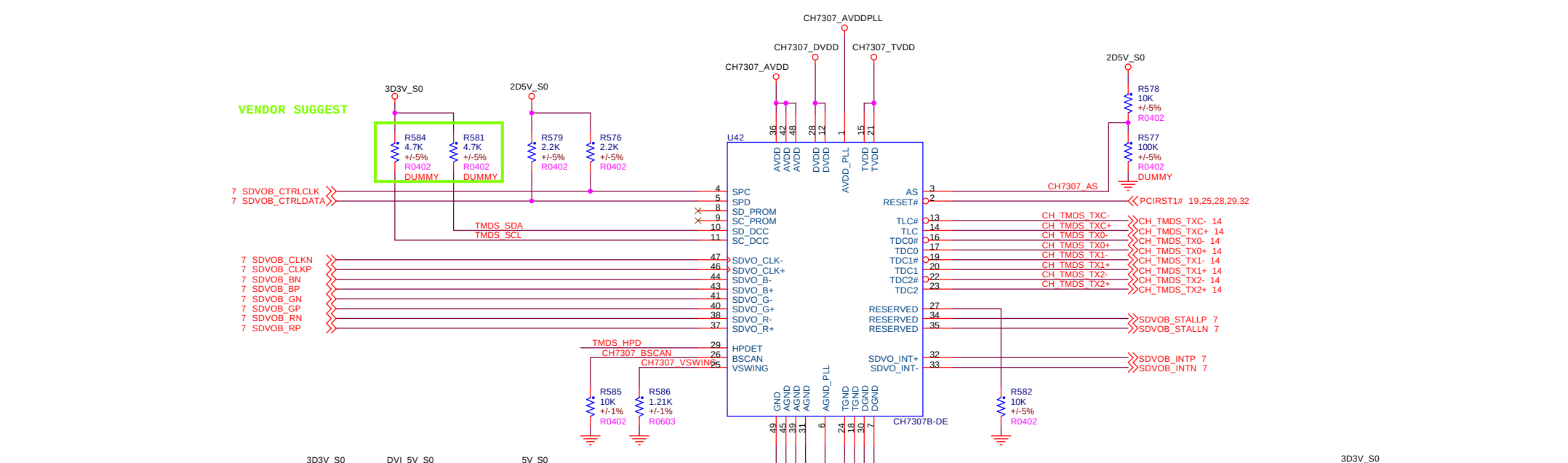
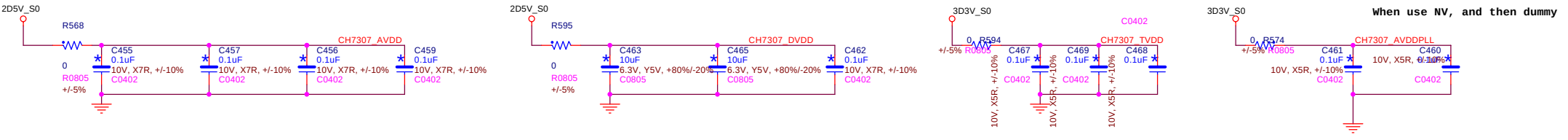


Layout Note:  
Place this 2 resistors close to the TV-out connector



FOXCONN ND2

|                                      |                          |           |
|--------------------------------------|--------------------------|-----------|
| Title<br>CRT/TV                      |                          |           |
| Size<br>A3                           | Document Number<br><Doc> | Rev<br>SA |
| Date:<br>Saturday, February 19, 2005 | Sheet<br>15              | of<br>44  |





FOXCONN ND2

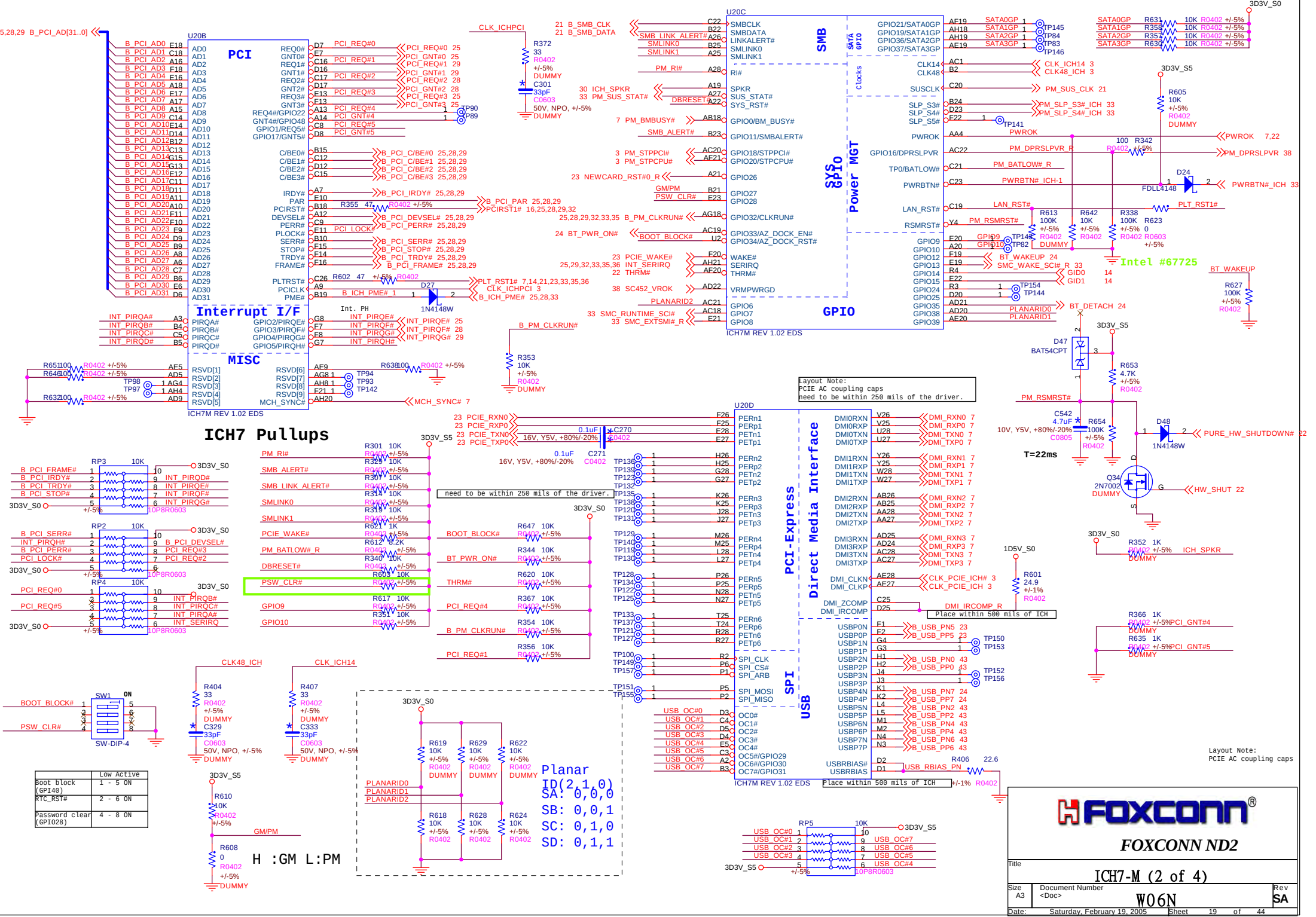
|       |                             |       |                 |     |    |
|-------|-----------------------------|-------|-----------------|-----|----|
| Title |                             |       | DVI TRANSMITTER |     |    |
| Size  | Document Number             | W06N  |                 | Rev | SA |
| A3    | <Doc>                       |       |                 |     |    |
| Date: | Saturday, February 19, 2005 | Sheet | 16              | of  | 44 |



**FOXCONN ND2**

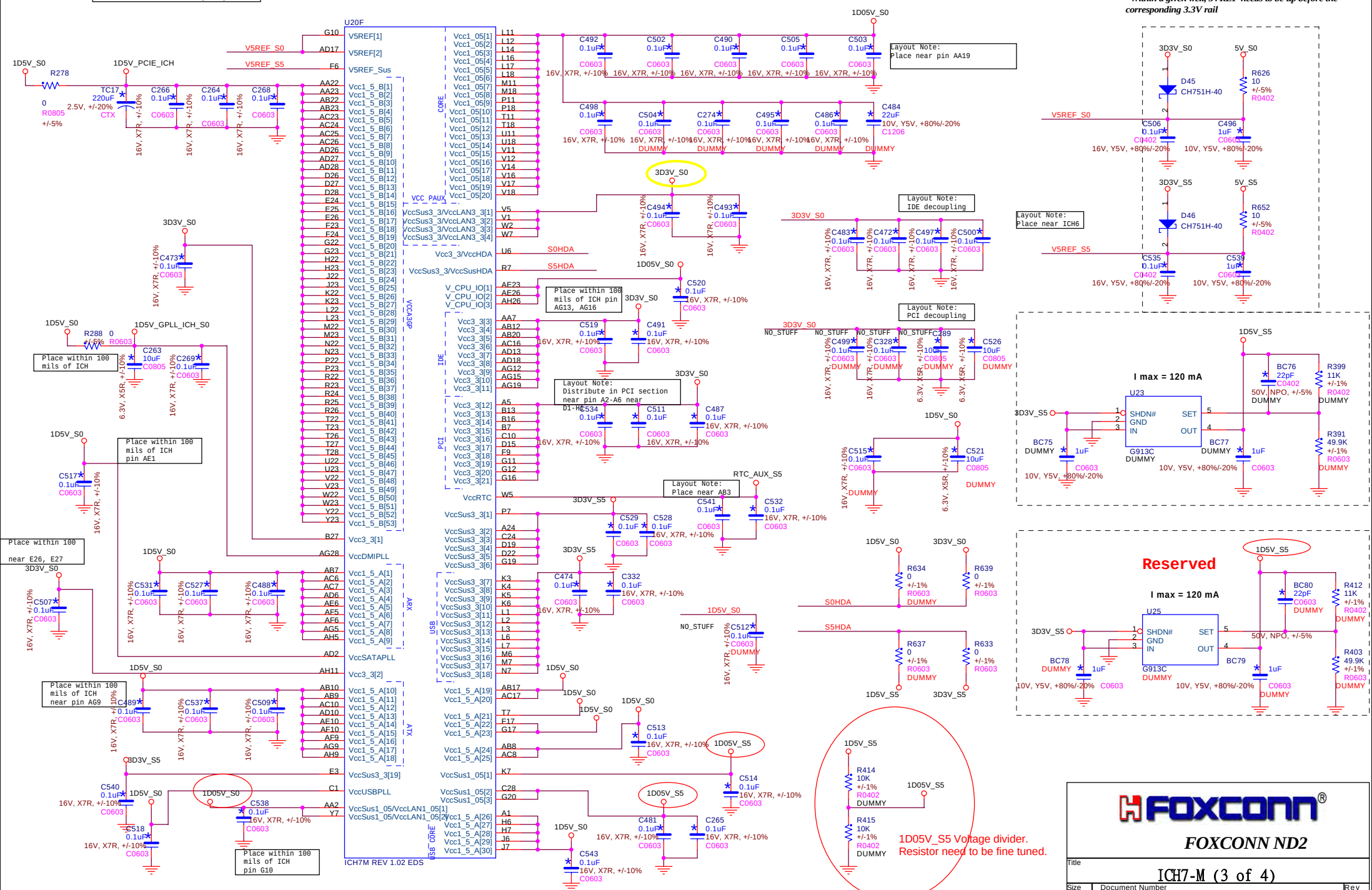
|                 |                             |       |           |
|-----------------|-----------------------------|-------|-----------|
| Title           |                             |       |           |
| LVDS / Inverter |                             |       |           |
| Size<br>A3      | Document Number<br><Doc>    | W06N  | Rev<br>SA |
| Date:           | Saturday, February 19, 2005 | Sheet | 17 of 44  |







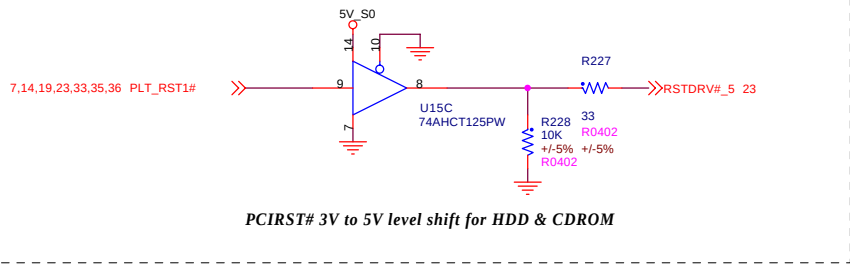
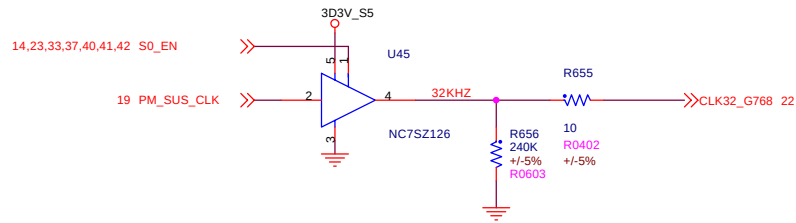
Layout Note:  
Place above caps within  
100 mils of ICH near F27, P27, AB27



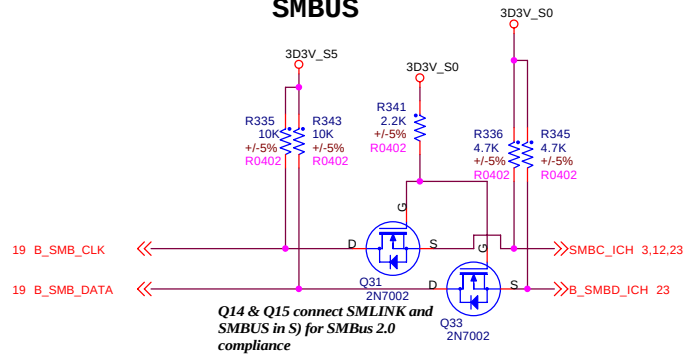
**FOXCONN®**  
*FOXCONN ND2*

|                 |                             |       |           |
|-----------------|-----------------------------|-------|-----------|
| Title           |                             |       |           |
| ICH7-M (3 of 4) |                             |       |           |
| Size<br>A3      | Document Number<br><Doc>    | W06N  | Rev<br>SA |
| Date:           | Saturday, February 19, 2005 | Sheet | 20 of 44  |

### 32K suspend clock output



### SMBUS



| U20E |         |          |      |
|------|---------|----------|------|
| A4   | VSS[1]  | VSS[98]  | P28  |
| A23  | VSS[2]  | VSS[99]  | R1   |
| B1   | VSS[3]  | VSS[100] | R11  |
| B8   | VSS[4]  | VSS[101] | R12  |
| B11  | VSS[5]  | VSS[102] | R13  |
| B14  | VSS[6]  | VSS[103] | R14  |
| B17  | VSS[7]  | VSS[104] | R15  |
| B20  | VSS[8]  | VSS[105] | R16  |
| B26  | VSS[9]  | VSS[106] | R17  |
| B28  | VSS[10] | VSS[107] | R18  |
| C2   | VSS[11] | VSS[108] | T6   |
| C6   | VSS[12] | VSS[109] | T12  |
| C27  | VSS[13] | VSS[110] | T13  |
| D10  | VSS[14] | VSS[111] | T14  |
| D13  | VSS[15] | VSS[112] | T15  |
| D18  | VSS[16] | VSS[113] | T16  |
| D21  | VSS[17] | VSS[114] | T17  |
| D24  | VSS[18] | VSS[115] | U4   |
| E1   | VSS[19] | VSS[116] | U12  |
| E2   | VSS[20] | VSS[117] | U13  |
| E4   | VSS[21] | VSS[118] | U14  |
| E8   | VSS[22] | VSS[119] | U15  |
| F15  | VSS[23] | VSS[120] | U16  |
| F3   | VSS[24] | VSS[121] | U17  |
| F4   | VSS[25] | VSS[122] | U24  |
| F5   | VSS[26] | VSS[123] | U25  |
| F12  | VSS[27] | VSS[124] | U26  |
| F27  | VSS[28] | VSS[125] | V2   |
| F28  | VSS[29] | VSS[126] | V13  |
| G1   | VSS[30] | VSS[127] | V15  |
| G2   | VSS[31] | VSS[128] | V24  |
| G5   | VSS[32] | VSS[129] | V27  |
| G6   | VSS[33] | VSS[130] | V28  |
| G9   | VSS[34] | VSS[131] | W6   |
| G14  | VSS[35] | VSS[132] | W24  |
| G18  | VSS[36] | VSS[133] | W25  |
| G21  | VSS[37] | VSS[134] | W26  |
| G24  | VSS[38] | VSS[135] | Y3   |
| G25  | VSS[39] | VSS[136] | Y24  |
| G26  | VSS[40] | VSS[137] | Y27  |
| H3   | VSS[41] | VSS[138] | Y28  |
| H4   | VSS[42] | VSS[139] | AA1  |
| H5   | VSS[43] | VSS[140] | AA24 |
| H24  | VSS[44] | VSS[141] | AA25 |
| H27  | VSS[45] | VSS[142] | AA26 |
| H28  | VSS[46] | VSS[143] | AB4  |
| J1   | VSS[47] | VSS[144] | AB6  |
| J2   | VSS[48] | VSS[145] | AB11 |
| J5   | VSS[49] | VSS[146] | AB14 |
| J24  | VSS[50] | VSS[147] | AB16 |
| J25  | VSS[51] | VSS[148] | AB19 |
| J26  | VSS[52] | VSS[149] | AB21 |
| K24  | VSS[53] | VSS[150] | AB24 |
| K27  | VSS[54] | VSS[151] | AB27 |
| K28  | VSS[55] | VSS[152] | AB28 |
| L13  | VSS[56] | VSS[153] | AC2  |
| L15  | VSS[57] | VSS[154] | AC5  |
| L24  | VSS[58] | VSS[155] | AC9  |
| L25  | VSS[59] | VSS[156] | AC11 |
| L26  | VSS[60] | VSS[157] | AD1  |
| M3   | VSS[61] | VSS[158] | AD3  |
| M4   | VSS[62] | VSS[159] | AD4  |
| M5   | VSS[63] | VSS[160] | AD7  |
| M12  | VSS[64] | VSS[161] | AD8  |
| M13  | VSS[65] | VSS[162] | AD11 |
| M14  | VSS[66] | VSS[163] | AD15 |
| M15  | VSS[67] | VSS[164] | AD19 |
| M16  | VSS[68] | VSS[165] | AD23 |
| M17  | VSS[69] | VSS[166] | AE2  |
| M24  | VSS[70] | VSS[167] | AE4  |
| M27  | VSS[71] | VSS[168] | AE8  |
| M28  | VSS[72] | VSS[169] | AE11 |
| N1   | VSS[73] | VSS[170] | AE13 |
| N2   | VSS[74] | VSS[171] | AE18 |
| N5   | VSS[75] | VSS[172] | AE21 |
| N6   | VSS[76] | VSS[173] | AE24 |
| N11  | VSS[77] | VSS[174] | AE25 |
| N12  | VSS[78] | VSS[175] | AE2  |
| N13  | VSS[79] | VSS[176] | AE4  |
| N14  | VSS[80] | VSS[177] | AE8  |
| N15  | VSS[81] | VSS[178] | AE11 |
| N16  | VSS[82] | VSS[179] | AE27 |
| N17  | VSS[83] | VSS[180] | AE28 |
| N18  | VSS[84] | VSS[181] | AG1  |
| N24  | VSS[85] | VSS[182] | AG3  |
| N25  | VSS[86] | VSS[183] | AG7  |
| N26  | VSS[87] | VSS[184] | AG11 |
| P3   | VSS[88] | VSS[185] | AG14 |
| P4   | VSS[89] | VSS[186] | AG17 |
| P12  | VSS[90] | VSS[187] | AG20 |
| P13  | VSS[91] | VSS[188] | AG25 |
| P14  | VSS[92] | VSS[189] | AH1  |
| P15  | VSS[93] | VSS[190] | AH3  |
| P16  | VSS[94] | VSS[191] | AH7  |
| P17  | VSS[95] | VSS[192] | AH12 |
| P24  | VSS[96] | VSS[193] | AH23 |
| P27  | VSS[97] | VSS[194] | AH27 |

ICH7M REV 1.02 EDS

**FOXCONN**

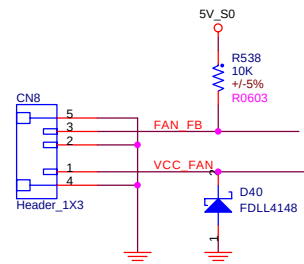
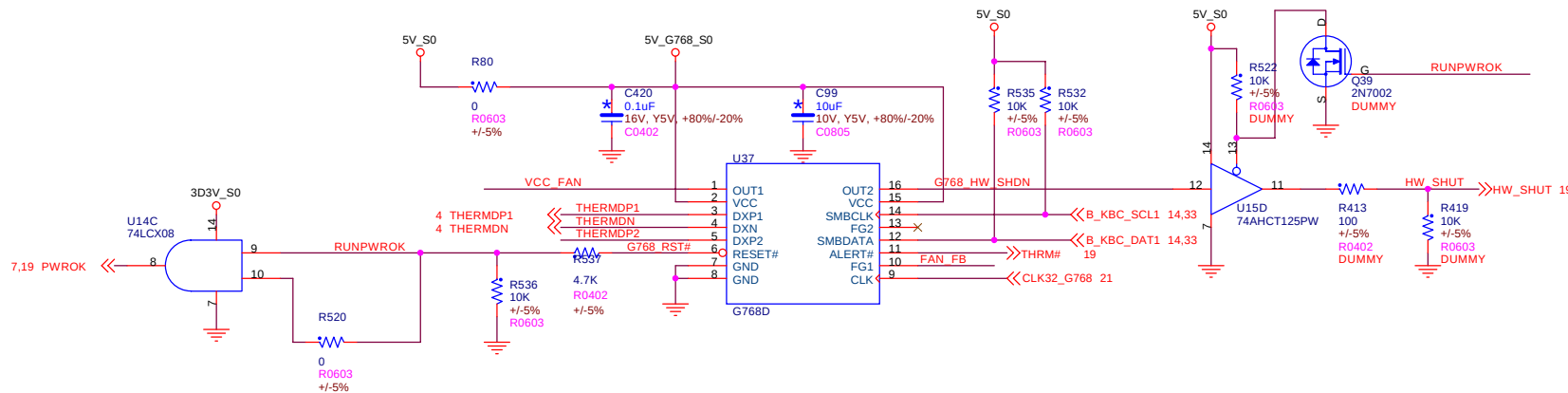
FOXCONN ND2

|                 |                             |       |          |
|-----------------|-----------------------------|-------|----------|
| Title           |                             |       |          |
| ICH7-M (4 of 4) |                             |       |          |
| Size            | Document Number             | Rev   |          |
| A3              | <Doc>                       | SA    |          |
| Date:           | Saturday, February 19, 2005 | Sheet | 21 of 44 |

## Reserve for G768B works at High Speed



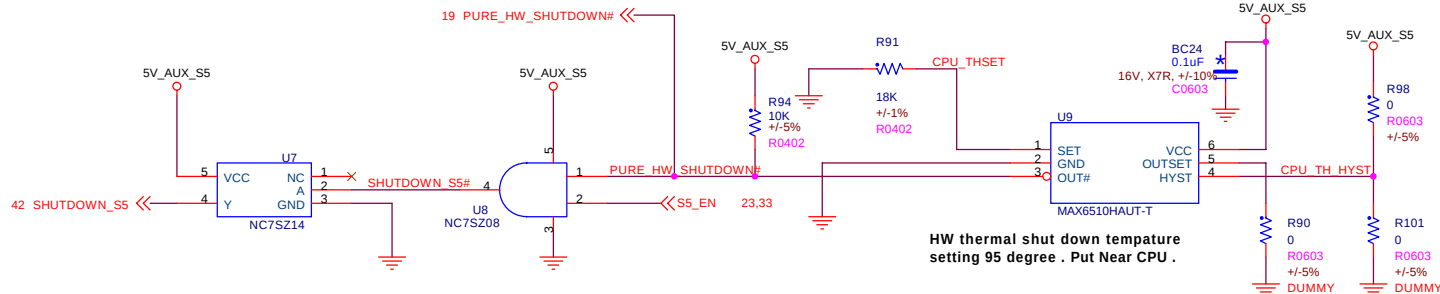
HW thermal shut down tempature setting 95 degree . Put Near CPU .



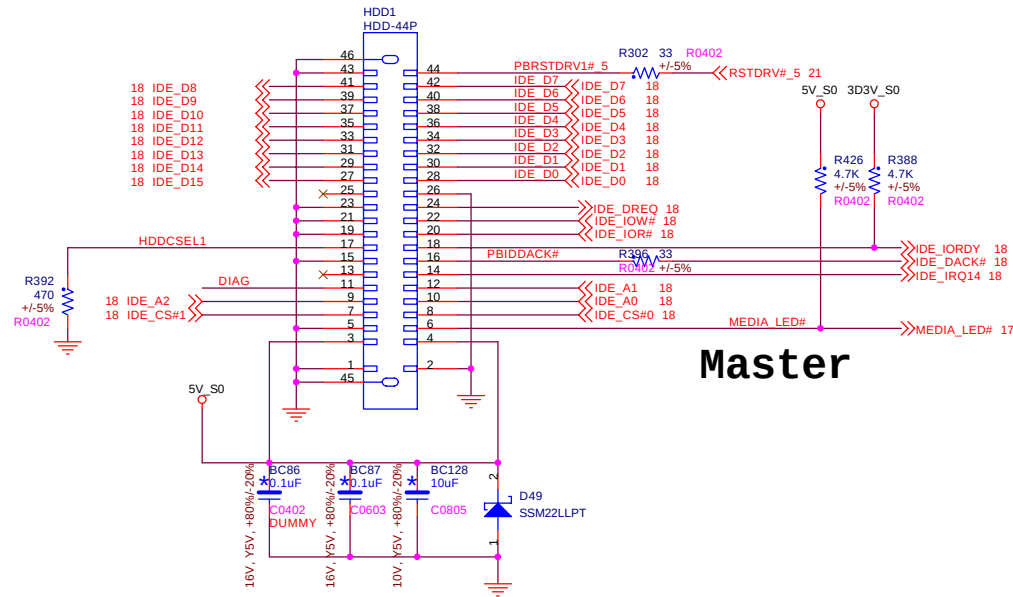
C419 0.1uF \*  
16V, Y5V, +80%/-20%  
C0402

C417 10uF \*  
10V, Y5V, +80%/-20%  
C0805

C421 2.2nF \*  
50V, X7R, +/-10%  
C0402

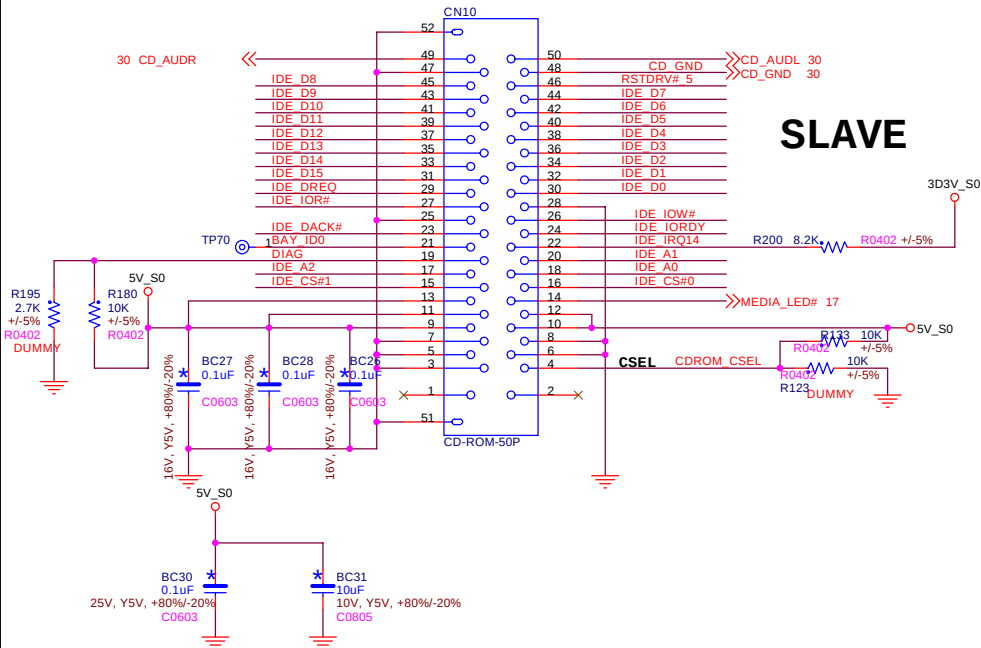


# HDD Connector

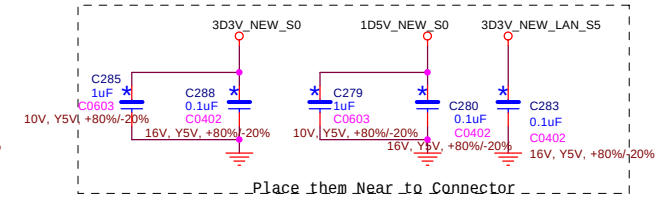
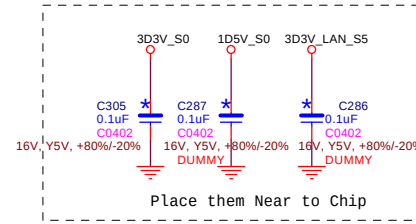


## Master

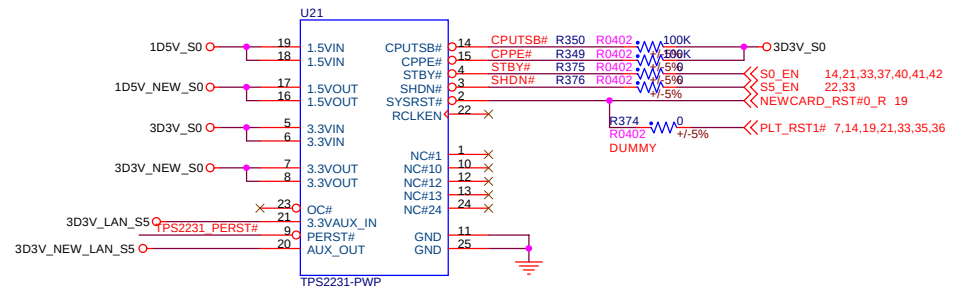
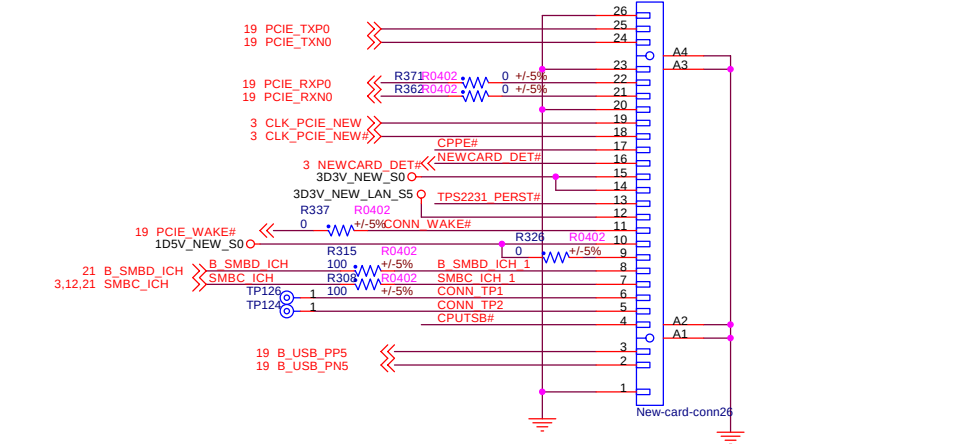
# CDROM



## SLAVE



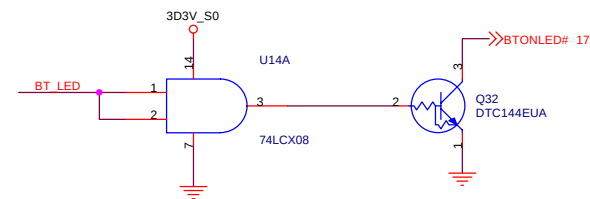
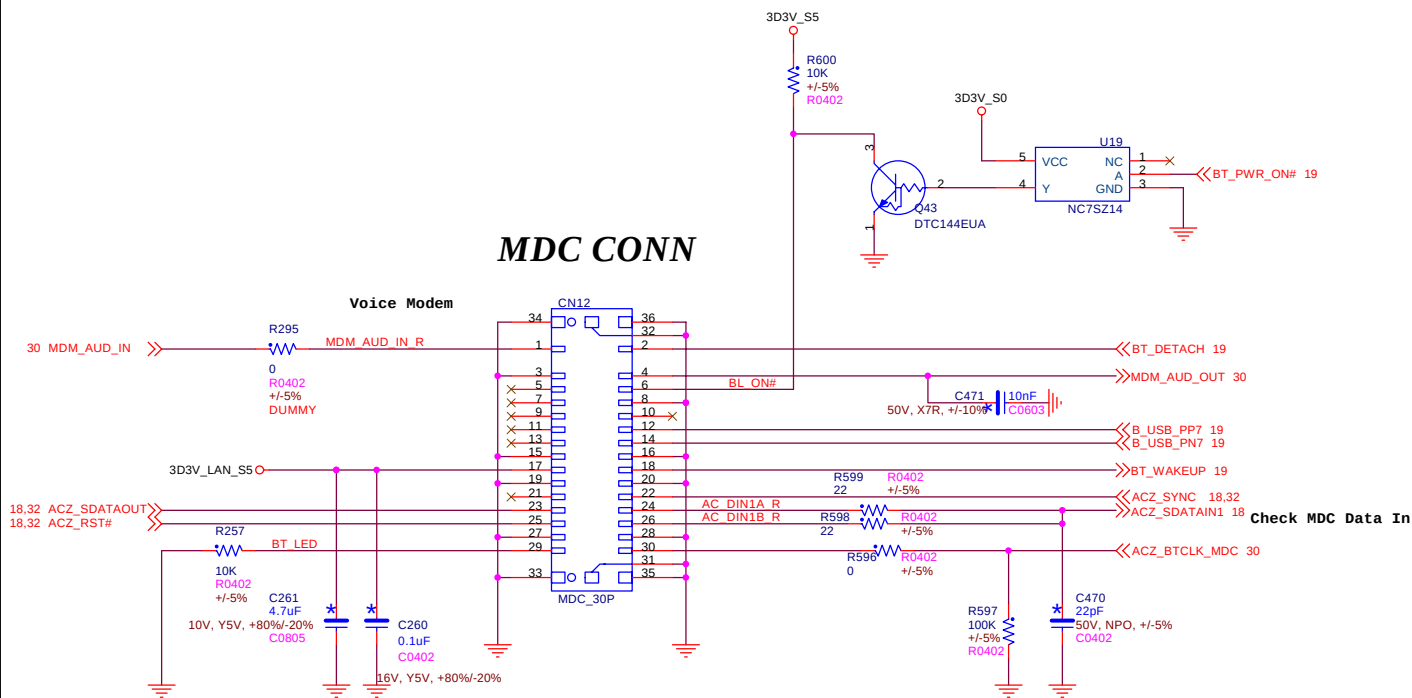
## Check new card pin define



**FOXCONN®**

**FOXCONN ND2**

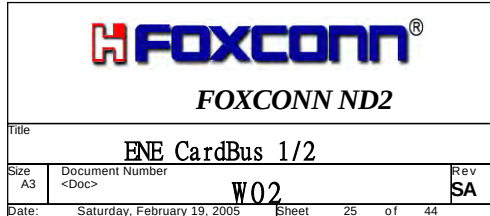
|       |                             |       |                    |    |     |
|-------|-----------------------------|-------|--------------------|----|-----|
| Title |                             |       | SATA/CDROM/NEWCARD |    | Rev |
| Size  | Document Number             | <Doc> |                    |    |     |
| A3    |                             |       | W02                |    | SA  |
| Date: | Saturday, February 19, 2005 | Sheet | 23                 | of | 44  |



**FOXCONN®**

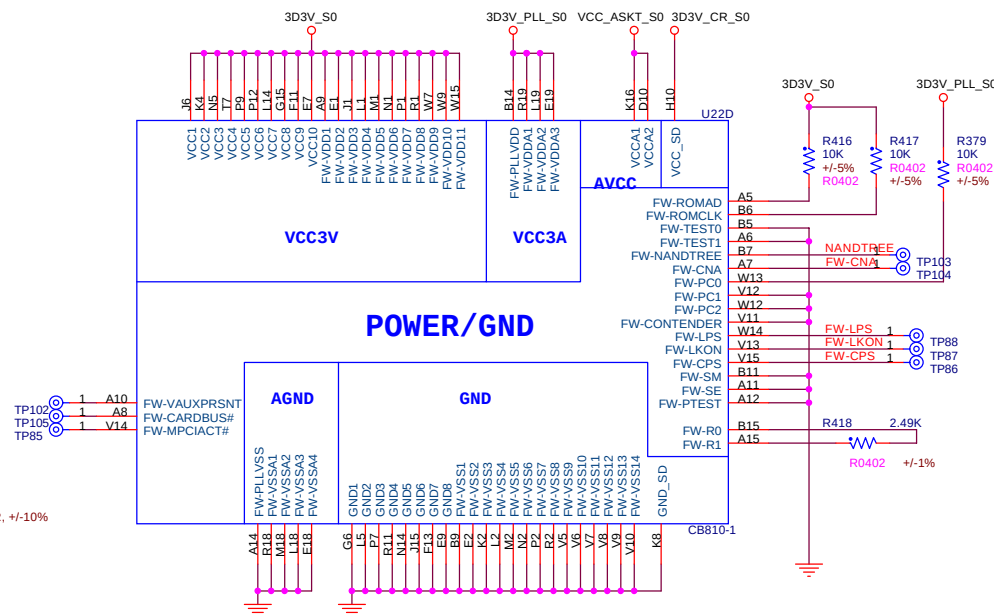
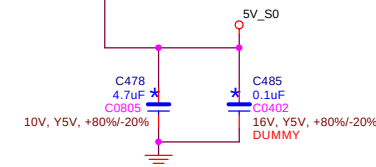
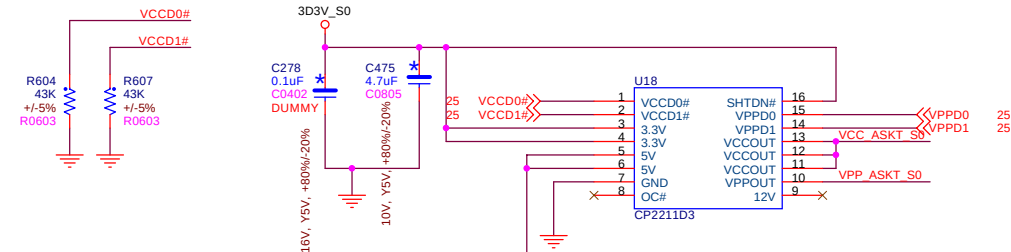
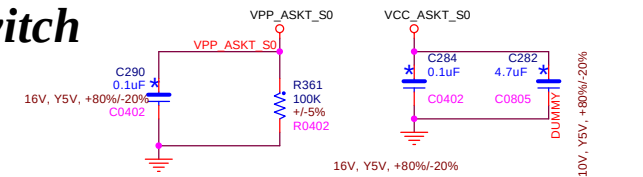
**FOXCONN ND2**

|       |                             |       |          |
|-------|-----------------------------|-------|----------|
| Title |                             |       | MDC      |
| Size  | Document Number             | Rev   | SA       |
| A3    | <Doc>                       | W02   |          |
| Date: | Saturday, February 19, 2005 | Sheet | 24 of 44 |

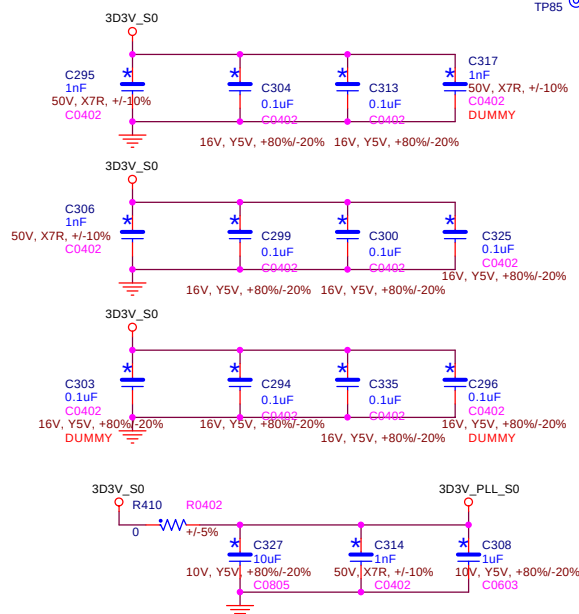




## Power switch



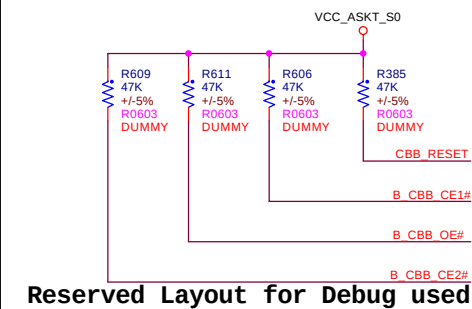
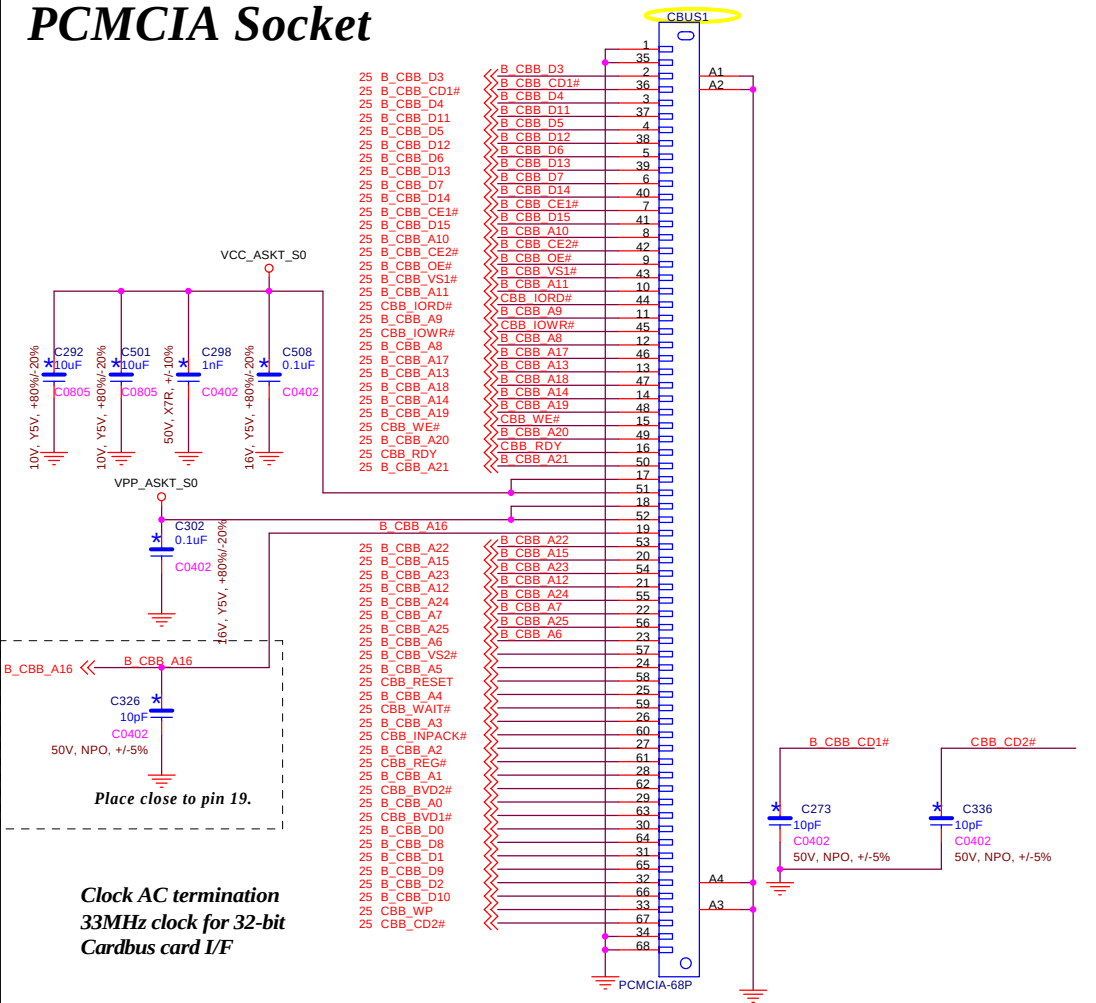
Bypass/Decoupling Capacitors  
Should be places as close to  
PCI7421 as possible



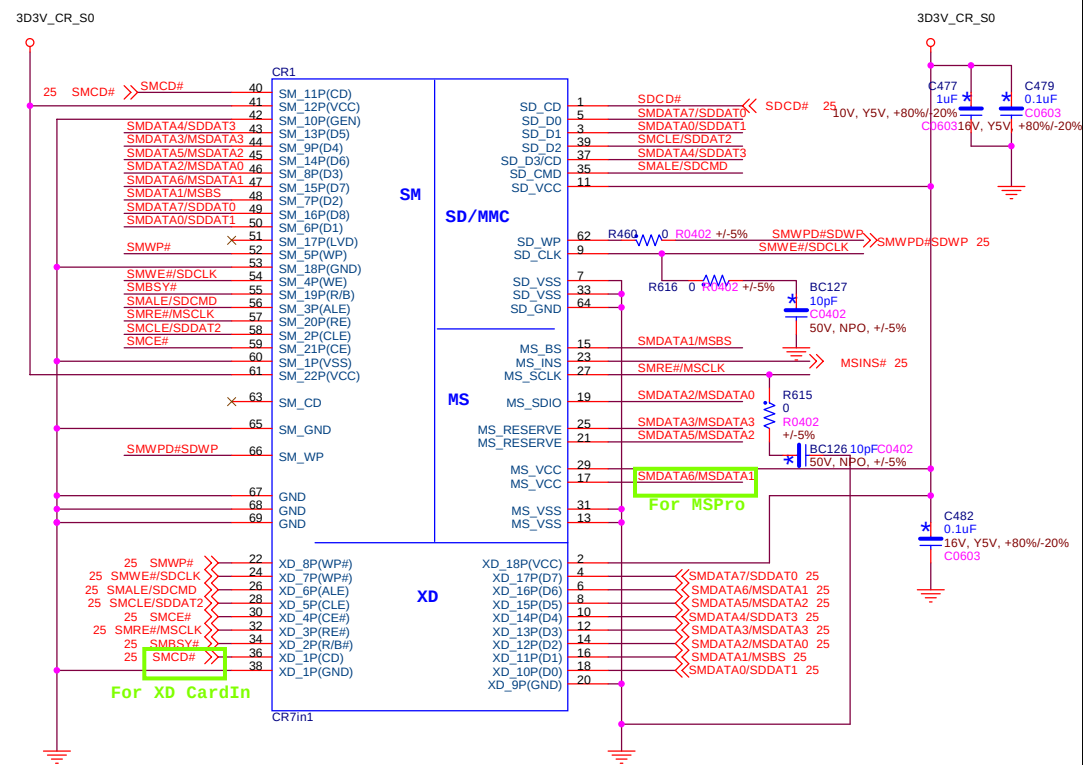
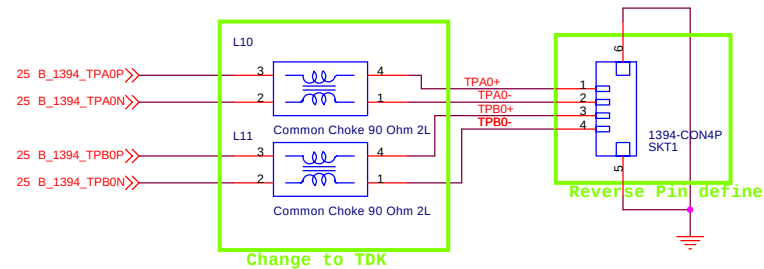
**FOXCONN ND2**

|                 |                             |                |           |
|-----------------|-----------------------------|----------------|-----------|
| Title           |                             |                |           |
| ENE CardBus 2/2 |                             |                |           |
| Size<br>A3      | Document Number<br><Doc>    | W02            | Rev<br>SA |
| Date:           | Saturday, February 19, 2005 | Sheet 26 of 44 |           |

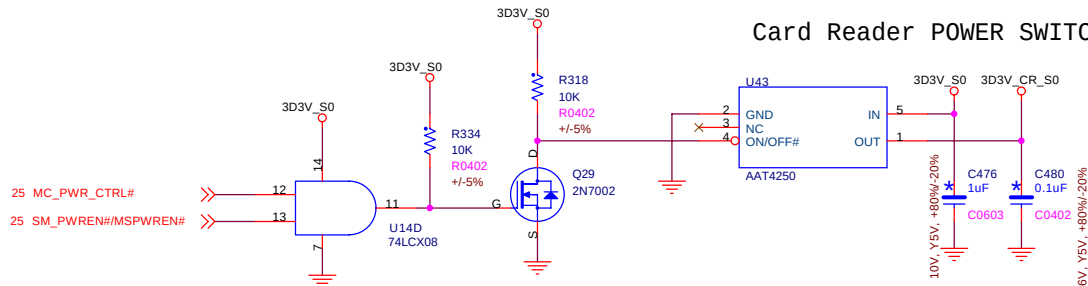
## PCMCIA Socket



## 1394 Connector



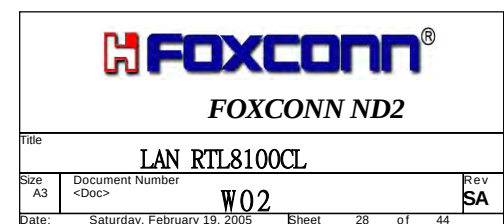
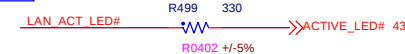
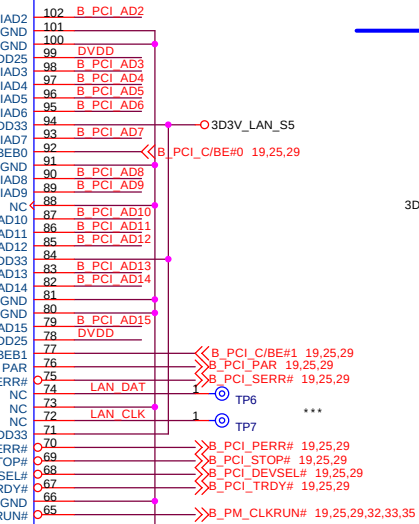
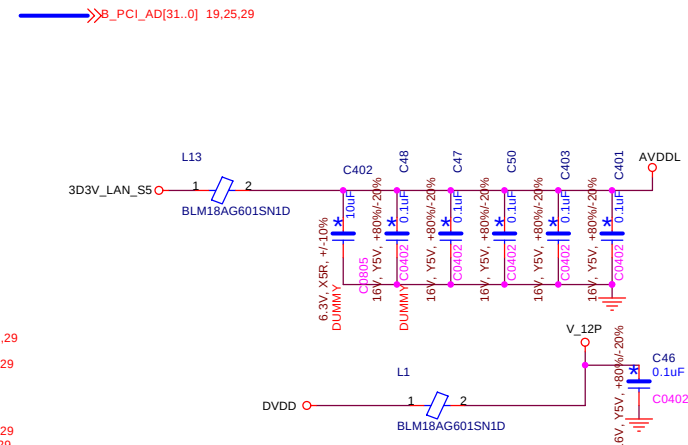
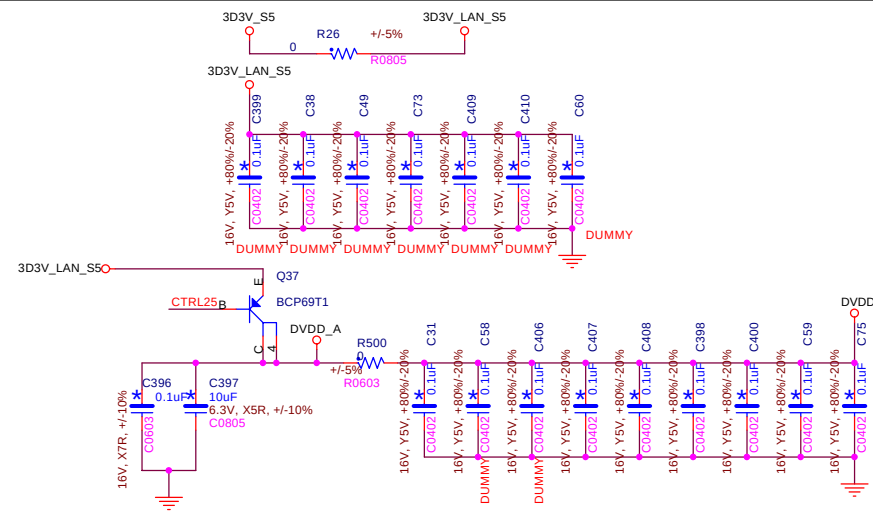
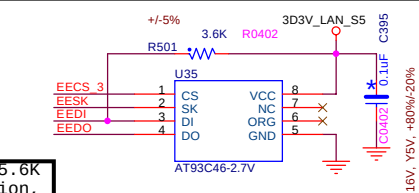
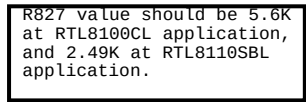
Card Reader POWER SWITCH



**FOXCONN ND2**

PCMCIA SLOT / 1394 CONN.

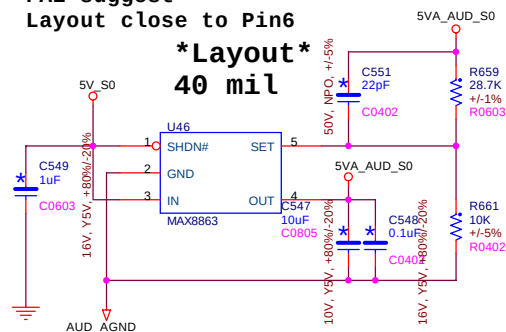
|                                   |                          |           |
|-----------------------------------|--------------------------|-----------|
| Size<br>A3                        | Document Number<br><Doc> | Rev<br>SA |
| Date: Saturday, February 19, 2005 | Sheet 27 of 44           |           |



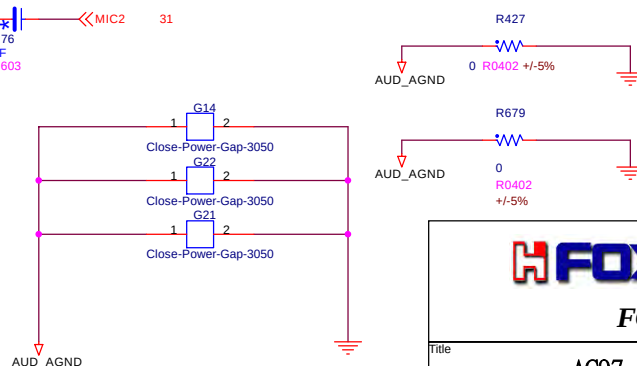
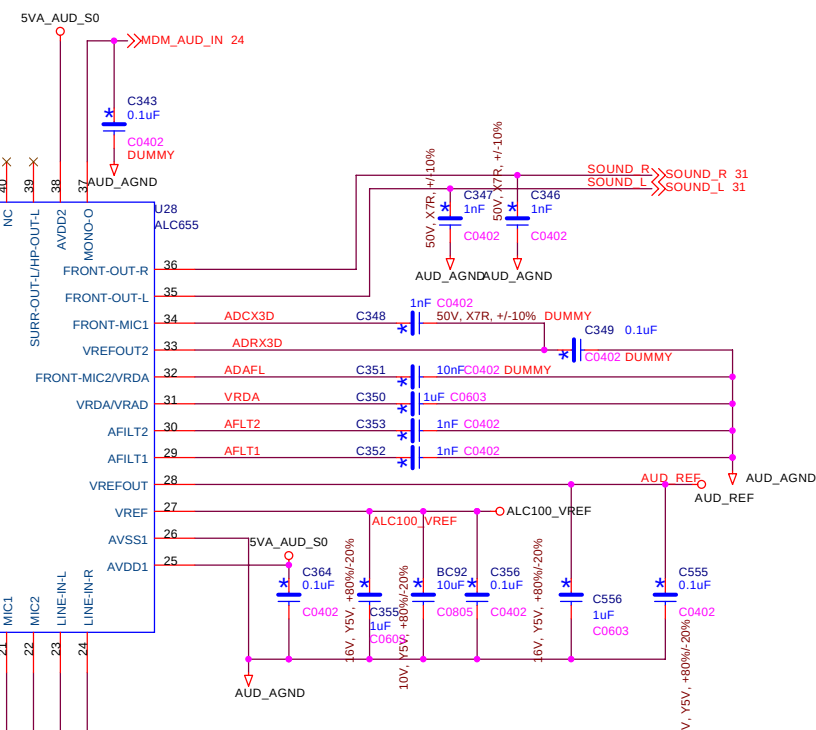
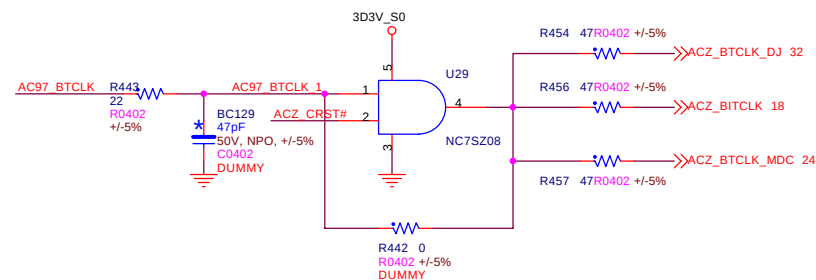
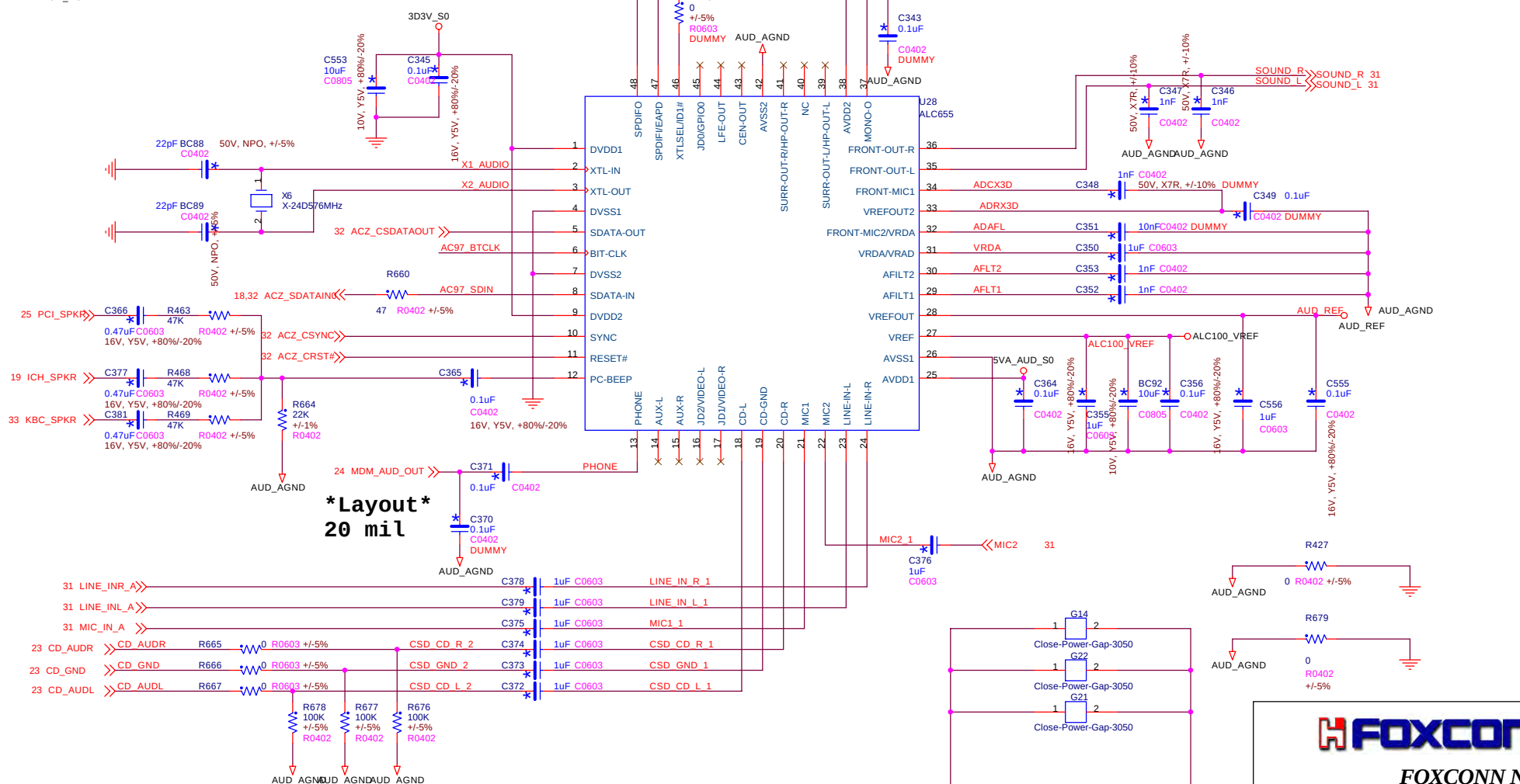


FAB suggest  
Layout close to Pin6

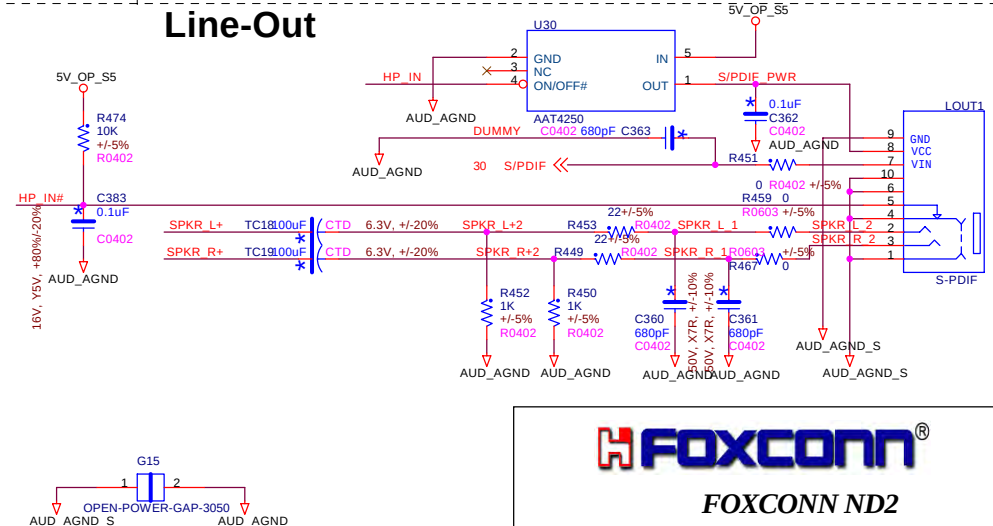
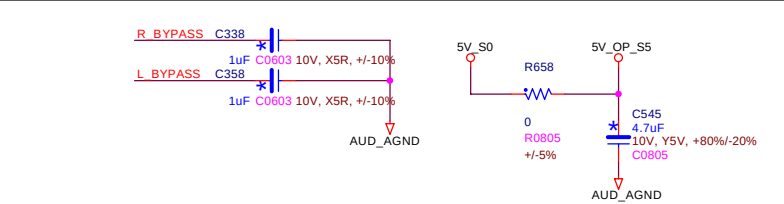
**\*Layout\***  
**40 mil**



Low for internal CLK

**FOXCONN ND2**

|            |                             |       |           |
|------------|-----------------------------|-------|-----------|
| Title      |                             |       |           |
| AC97 code  |                             |       |           |
| Size<br>A3 | Document Number<br><Doc>    | W02   | Rev<br>SA |
| Date:      | Saturday, February 19, 2005 | Sheet | 30 of 44  |







19,25,29,32,35,36 INT\_SERIRQ  
18,32,35,36 B\_LPC\_LFRAME#  
18,32,35,36 B\_LPC\_LAD0  
18,32,35,36 B\_LPC\_LAD1  
18,32,35,36 B\_LPC\_LAD2  
18,32,35,36 B\_LPC\_LAD3  
3 PCLK\_KBC

19,25,28,29,32,35,36  
15

PCLK\_KBC

7,14,19,21,23,35,36 PLT\_RST1#

Pull-Down resistor required to avoid leakage current

3D3V\_AUX\_S5

R259 10K +/-5%  
R0402

19 SMC

R282 47K  
R0402 +/-5%

ECRST#

BC63 10K +/-5%  
0.1uF  
25V, Y5V, +80%/-20%  
C0603

POWER-ON RESET  
Example Only

3D3V\_S5

R217 10K +/-5%  
R0402

COVERUP

3D3V\_AUX\_S5

R283 10K +/-5%  
R0402

19,25,28 B\_ICH\_PME#

R280

5V\_S0

R231 10K +/-5%  
R0402

R230 10K +/-5%  
R0402

R229 10K +/-5%  
R0402

R232 10K +/-5%  
R0402

TP110  
TP71  
TP72  
TP73

PSCLK2  
PSDAT2  
PSCLK3  
PSDAT3

43 BT+SENSE

R17 10K +/-5%  
R0603  
DUMMY

R13 39K +/-1%  
R0603

BT+ BAT

BT+SENSE KBC

R11 10K +/-5%  
R0603  
DUMMY

R12 10K +/-5%  
R0603

C17 0.1uF  
C0402  
16V, Y5V, +80%/-20%

14,21,23,37,40,41,42  
41  
19  
18  
22,23  
29  
17

0 ohm

R240 0 R0402  
+/-5%  
DUMMY

R238 10K +/-5%  
R0402  
DUMMY

14 AT1\_BL\_ON

7 GMCH\_BL\_ON

BAT\_TH

R22 15K +/-1%  
R0603

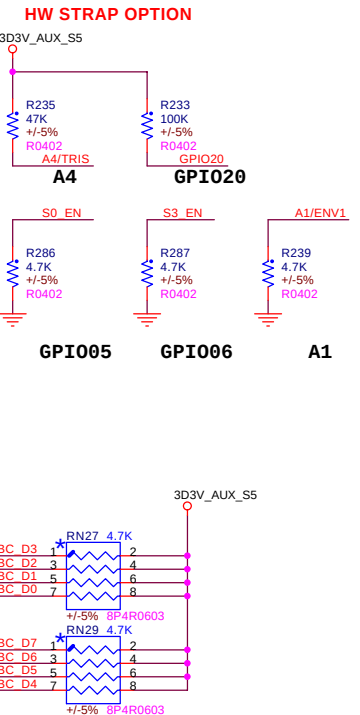
C45 0.1uF  
C0402  
16V, Y5V, +80%/-20%

BAT\_TYPE

AD OFF

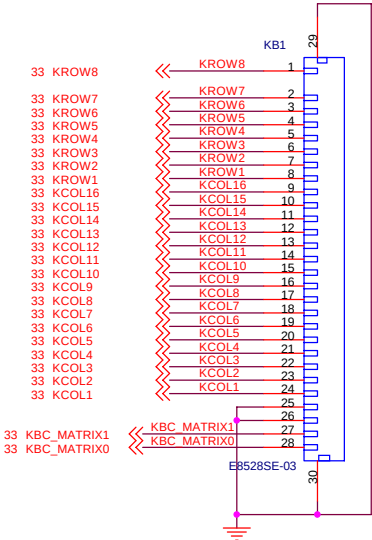
R24 10K +/-5%  
R0402

19 SMC  
19 SI  
THERM\_ALERT#\_GP

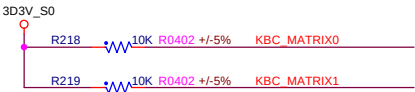
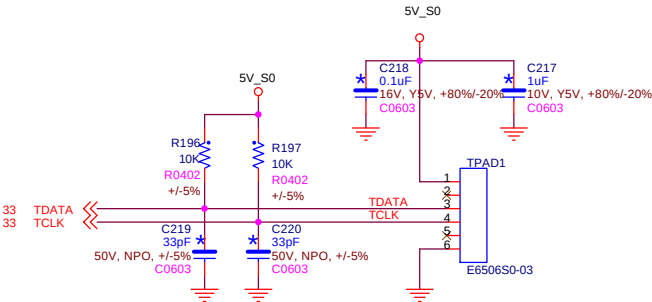


|                                                                                       |                                        |                                  |                          |
|---------------------------------------------------------------------------------------|----------------------------------------|----------------------------------|--------------------------|
|  |                                        |                                  |                          |
| <p align="center"><b>FOXCONN ND2</b></p>                                              |                                        |                                  |                          |
| <p>Title</p> <p align="center"><b>KBC ENE3910</b></p>                                 |                                        |                                  |                          |
| <p>Size<br/>A3</p>                                                                    | <p>Document Number<br/>&lt;Doc&gt;</p> | <p align="center"><b>W02</b></p> | <p>Rev<br/><b>SA</b></p> |
| Date:                                                                                 | Saturday, February 19, 2005            | Sheet                            | 33 of 44                 |

Internal KeyBoard Connector

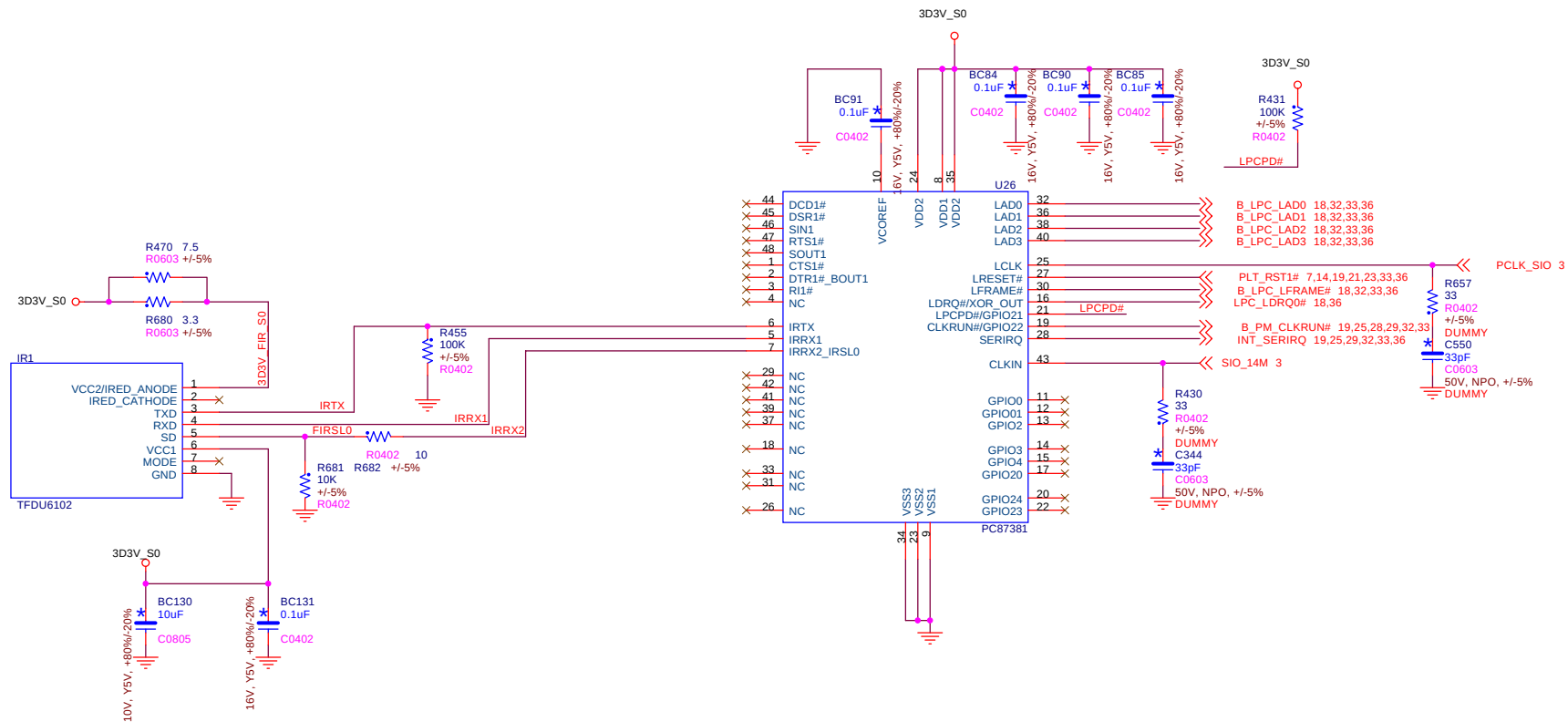


TouchPad Connector



Keyboard matrix ( from vendor )

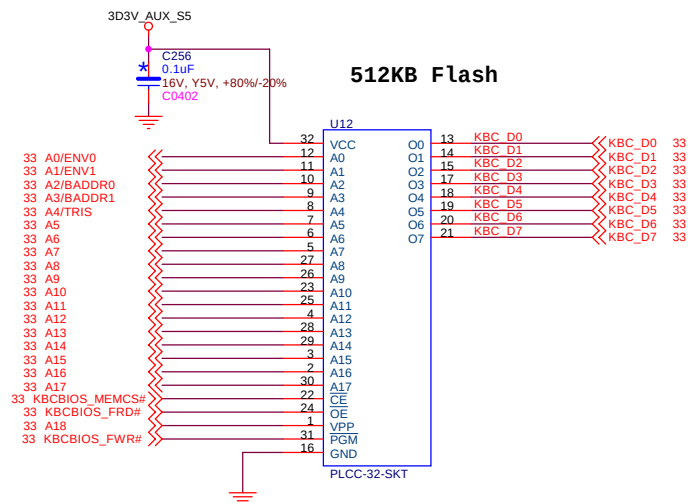
|            | US | Eur | Jap | Ohter |
|------------|----|-----|-----|-------|
| MATRIXID1# | 1  | 0   | 1   | 0     |
| MATRIXID2# | 1  | 1   | 0   | 0     |



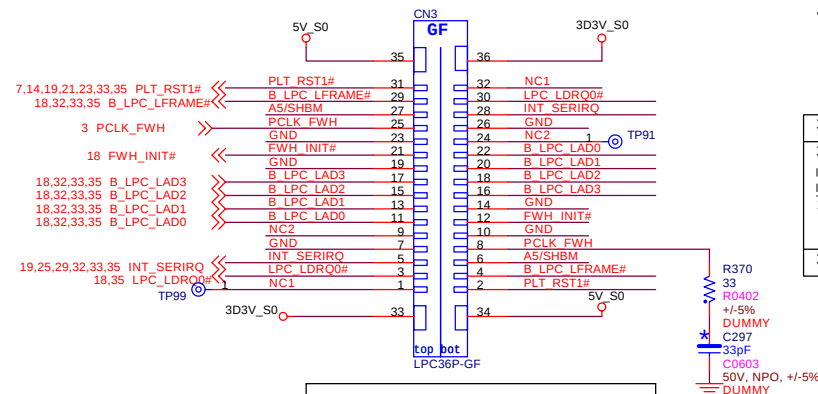
**FOXCONN®**

**FOXCONN ND2**

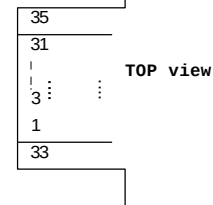
|             |                             |       |    |       |
|-------------|-----------------------------|-------|----|-------|
| Title       |                             |       |    |       |
| SIO NS87381 |                             |       |    |       |
| Size        | Document Number             |       |    | Rev   |
| A3          | <Doc>                       | W06N  |    | SA    |
| Date:       | Saturday, February 19, 2005 | Sheet | 35 | of 44 |



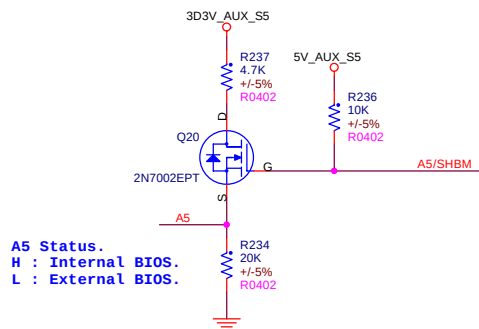
## DEBUG GOLDEN FINGER GOLDEN FINGER FOR DEBUG BOARD



TOP VIEW(1.3...35)  
BOTTOM VIEW(2.4..36)



Boot Device must have ID[3:0] = 0000  
Has internal pull-down resistors  
All may be left floated  
FPET7 Elec. P3-46

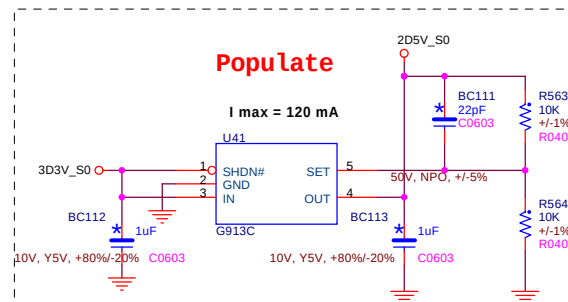
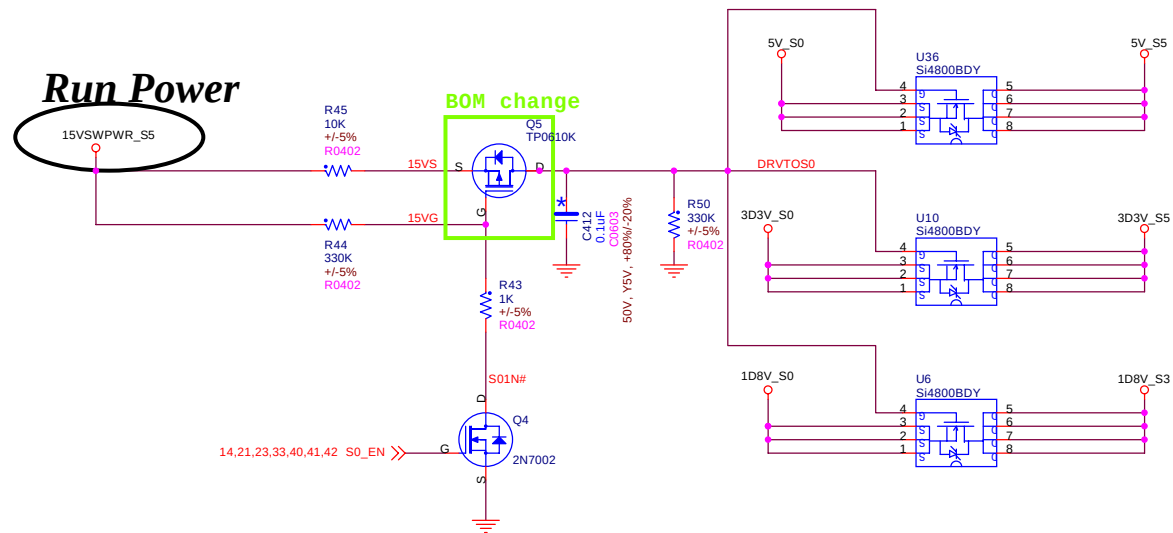


A5 Status.  
H : Internal BIOS.  
L : External BIOS.

**FOXCONN**

FOXCONN ND2

|       |                             |             |          |
|-------|-----------------------------|-------------|----------|
| Title |                             | BIOS /Debug |          |
| Size  | Document Number             | W02         | Rev SA   |
| A3    | <Doc>                       |             |          |
| Date: | Saturday, February 19, 2005 | Sheet       | 36 of 44 |

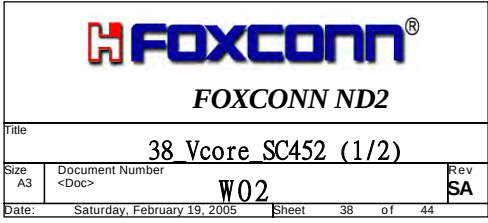


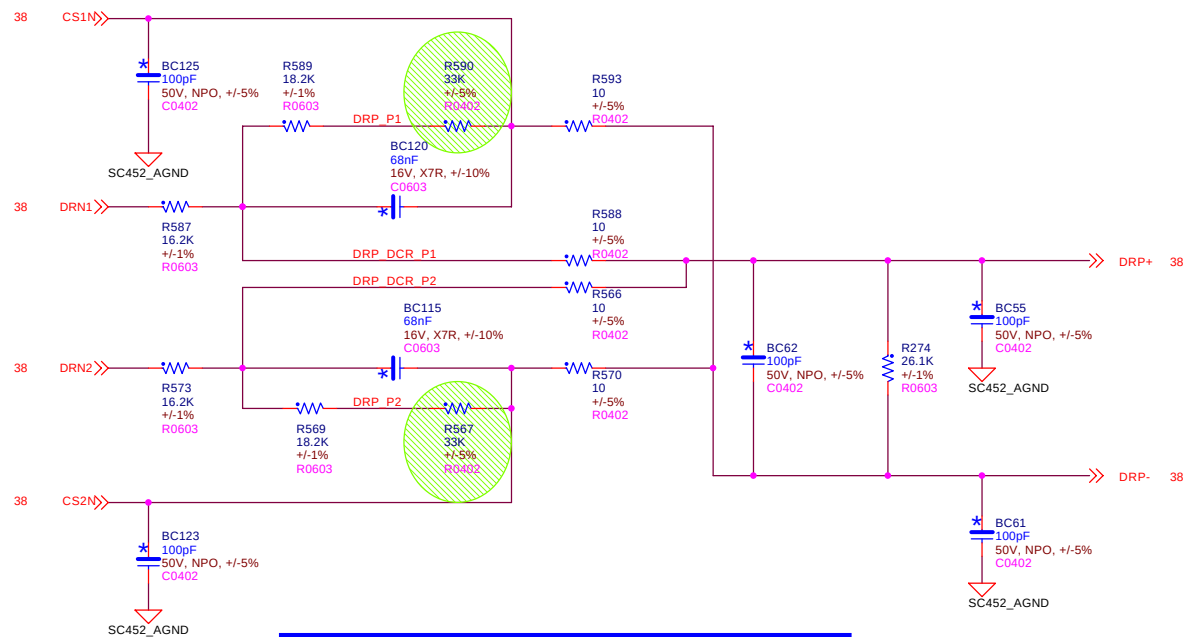
**FOXCONN®**

**FOXCONN ND2**

|                                   |                          |  |                |     |           |
|-----------------------------------|--------------------------|--|----------------|-----|-----------|
| Title                             |                          |  |                |     | Rev<br>SA |
| PWRPLANE&RESETLOGIC               |                          |  |                |     |           |
| Size<br>A3                        | Document Number<br><Doc> |  |                | W02 |           |
| Date: Saturday, February 19, 2005 |                          |  | Sheet 37 of 44 |     |           |







Note:  
 DRN1/ CS1N are the terminal of the L16  
 DRN2/ CS2N are the terminal of the L20

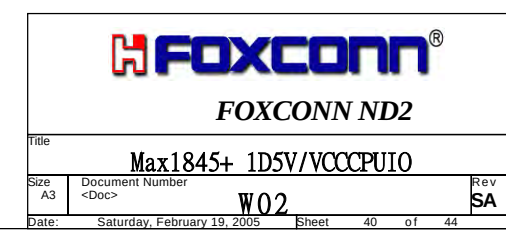
### INDUCTOR DROOP

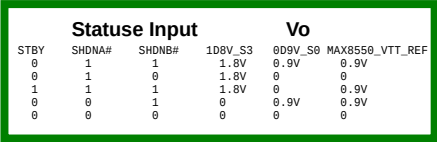
DRNx is the "+" end of the inductor . CSxN is the "-" end .

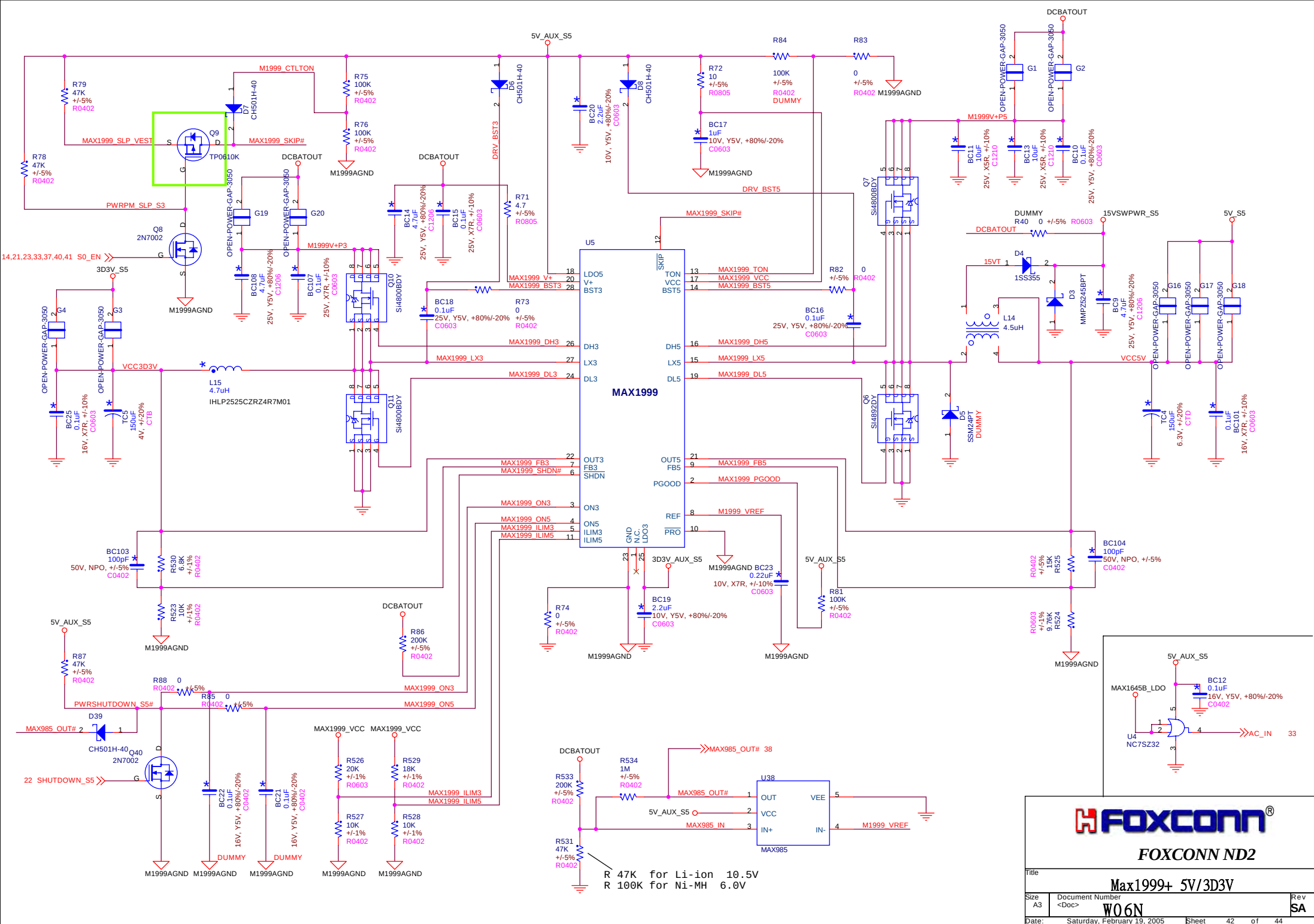


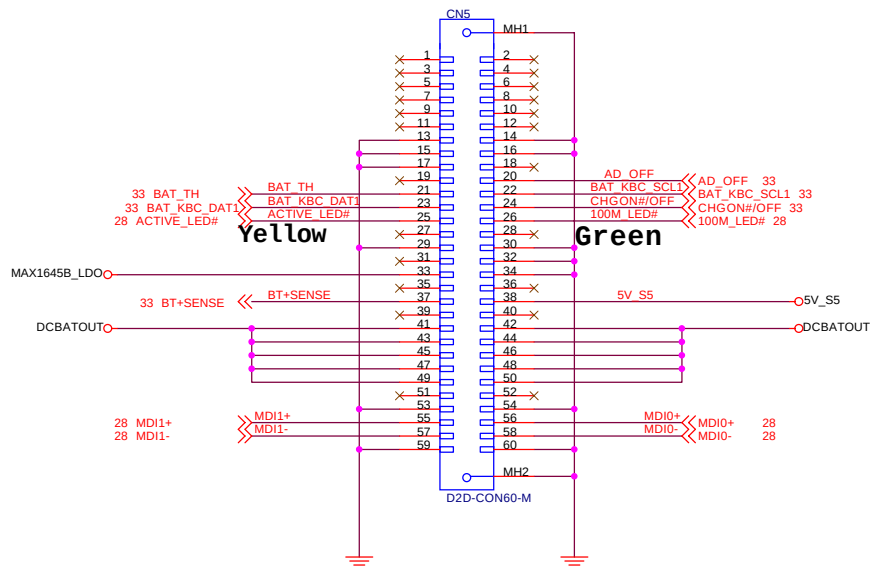
FOXCONN ND2

|       |                             |       |                      |
|-------|-----------------------------|-------|----------------------|
| Title |                             |       | 39_Vcore_SC452 (2/2) |
| Size  | Document Number             | Rev   |                      |
| A3    | <Doc>                       | SA    |                      |
| Date: | Saturday, February 19, 2005 | Sheet | 39 of 44             |

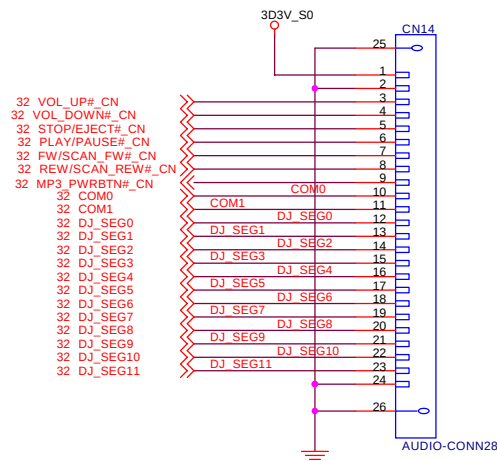




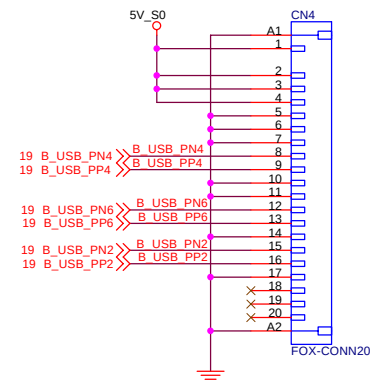




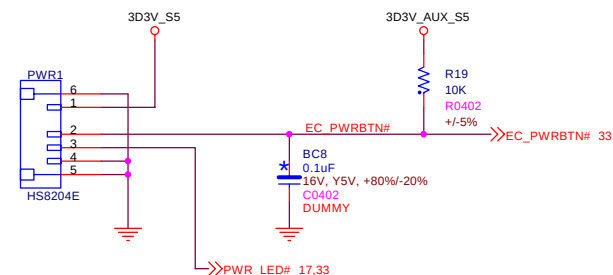
**Power /LAN Connector**



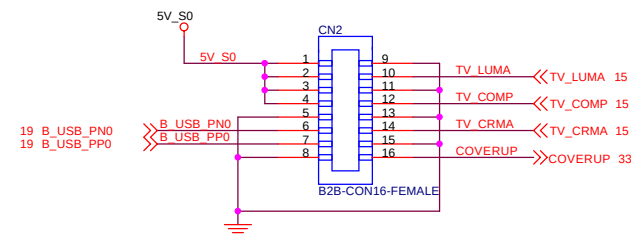
**AudioDJ Connector**



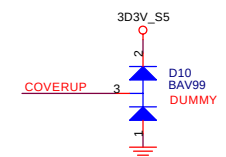
**3 PORT USB Connector**



**Power Switch Connector**



**USB / TV Connector**



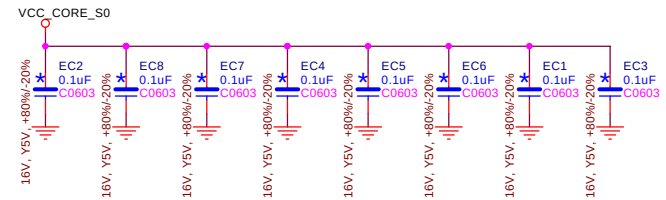
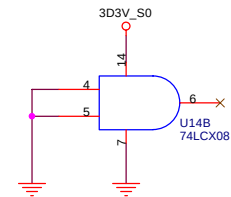
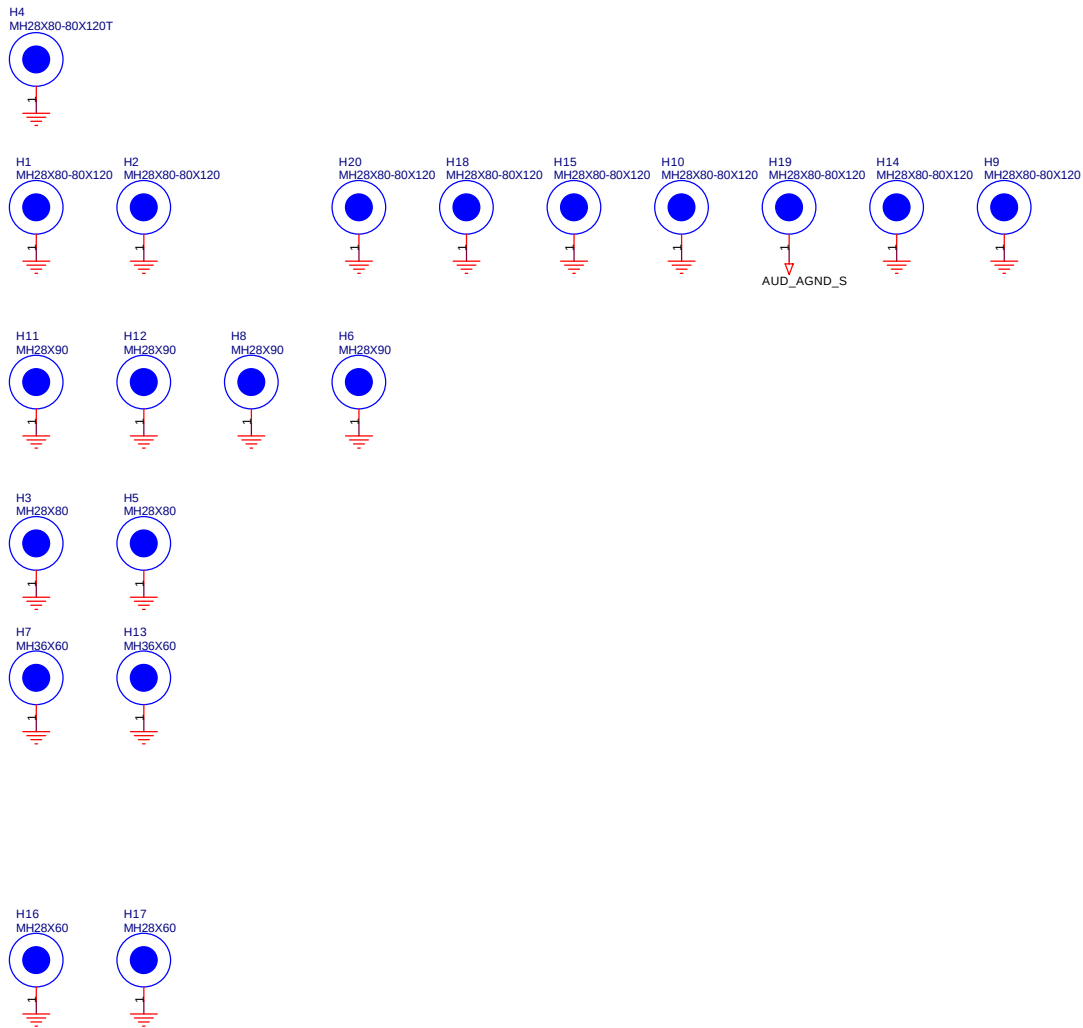
**FOXCONN®**

**FOXCONN ND2**

|       |                             |                 |                           |       |
|-------|-----------------------------|-----------------|---------------------------|-------|
| Title |                             |                 | Daughter Board Connectors |       |
| Size  | A3                          | Document Number | <Doc>                     |       |
| Date: | Saturday, February 19, 2005 | Sheet           | 43                        | of 44 |

**W02**

Rev  
**SA**



FOXCONN ND2

|              |                             |  |       |          |
|--------------|-----------------------------|--|-------|----------|
| Title        |                             |  |       |          |
| UNUSED PARTS |                             |  |       |          |
| Size         | Document Number             |  |       | Rev      |
| A3           | <Doc>                       |  |       | SA       |
| W02          |                             |  |       |          |
| Date:        | Saturday, February 19, 2005 |  | Sheet | 44 of 44 |