LCFC Confidential

YOGA3-BDW M/B Schematics Document

INTEL Broadwell Mobile ULT Platform
INTEL BDW U-series CPU + DDR3L DIMM+ NV N16S-GT

2014-04-28

REV:1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2014/01/11	Deciphered Date	2013/11/08

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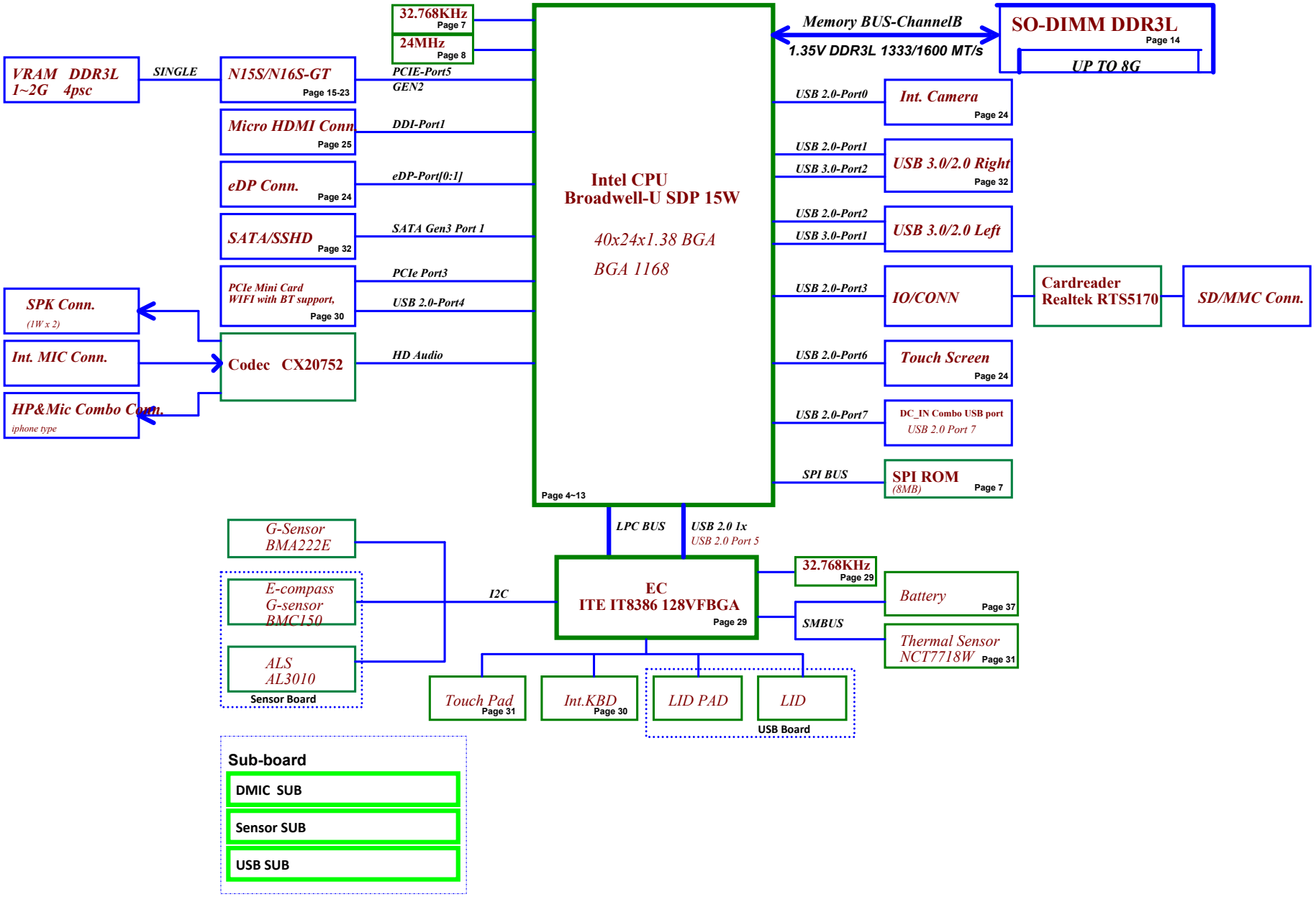
Yoga3 BDW Refresh Block diagram



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Title: Block Diagram

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+ +3VL +5VLP	+3VALW +5VALW	+3VALW_PCH	+1.35V	+5VS +3VS +1.5VS +1.05VS +0.68VS +CPU_CORE	+1.35V_CPU
S0	O	O	O	O	O	O
S3	O	O	O	O	X	O
DS3	O	O	X	O	X	X
S5 S4/AC Only	O	O	O	X	X	X
S5 S4 Battery only	O	X	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	+VALW	+VALW_PCH	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	ON	OFF	OFF
DS3 (Suspend to RAM)	LOW	LOW	HIGH	ON	LOW	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	Sensor	ALS	BATT	touch sensor	SODIMM	GPU	Thermal Sensor	PCH	charger
EC_SMB_CLK1 EC_SMB_DAT1	IT8386 +3VALW_EC	X	X	V +3VLP	X	X	X	X	X	V
EC_SMB_CLK3 EC_SMB_DAT3	IT8386 +3VS	V +3VS	V +3VS	X	X	X	X	X	X	X
EC_SMB_CLK0 EC_SMB_DAT0	IT8386 +3VS	X	X	X	X	X	V	V +3VS	V +3VALW_PCH	X
SMB_CLK SMB_DATA	PCH +3VALW_PCH	X	X	X	X	V +3VS	X	X	X	X

SM Bus address

	Device	address
EC1	Battery	0001 011X b
	Charger	
EC3	Sensor	
	ALS	
	Thermal Sensor	1001_100xb
EC0	PCH THM	
PCH	TP	

PCIE PORT LIST

Port	Device
1	X
2	X
3	WLAN
4	X
5	GPU

USB Port Table

		USB20		USB30
EXCI1/XHCI	0	CAMERA	1	Left USB
	1	Right USB	2	Right USB
	2	Left USB	3	X
	3	CARD READER	4	X
	4	BT		
	5	Sensor		
	6	TOUCH PANEL		
	7	DC_IN combo USB2.0		

BOM Structure Table

BOM Structure		BOM Structure	
DA8@	PCB	MIRROR@	EC Mirror-code enable
UMA@	UMA SKU part	UNMIRROR@	EC Mirror-code disableable
DEBUG@	DEBUG CARD Part	OPT@	Discrete GPU SKU part
ME@	ME part(connector, hole)	N15SGT@	For N15S-GT GPU part
RF@	RF request	GC6@	GC62.0 support part
EMC@	EMC request	RANKA@	For VRAM RankA part
CD@	COST DOWN Part		
REV@	RESERVER Part		

Board ID Table

Board ID	Description	PCB Revision

BOM Configuration Table

SKU	Description	BOM Config	
SKU1			
SKU2			

X76&VGA Configuration Table

SKU	Description	BOM Config	

PCB And LOGO Config

PCB	ZZZ3 DA8@ PCB 0YC NM-A381 REV0 M/B	LOGO
CPU	ZZZ1 I7@ BDW U2+2 Ci7 ZZZ2 I5@ BDW U2+2 Ci5 ZZZ9 I3@ BDW 2+2U 1.6G 1333 ES2	ZZZ4 HDMI@ HDMI LOGO ZZZ5 USB30@ USB30 LOGO
VRAM	ZZZ6 HY2G@ HYNIX 2G ZZZ7 MIC2G@ MICRON 2G ZZZ8 SAM2G@ SAMSUNG 2G	

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Title: **Notes List**

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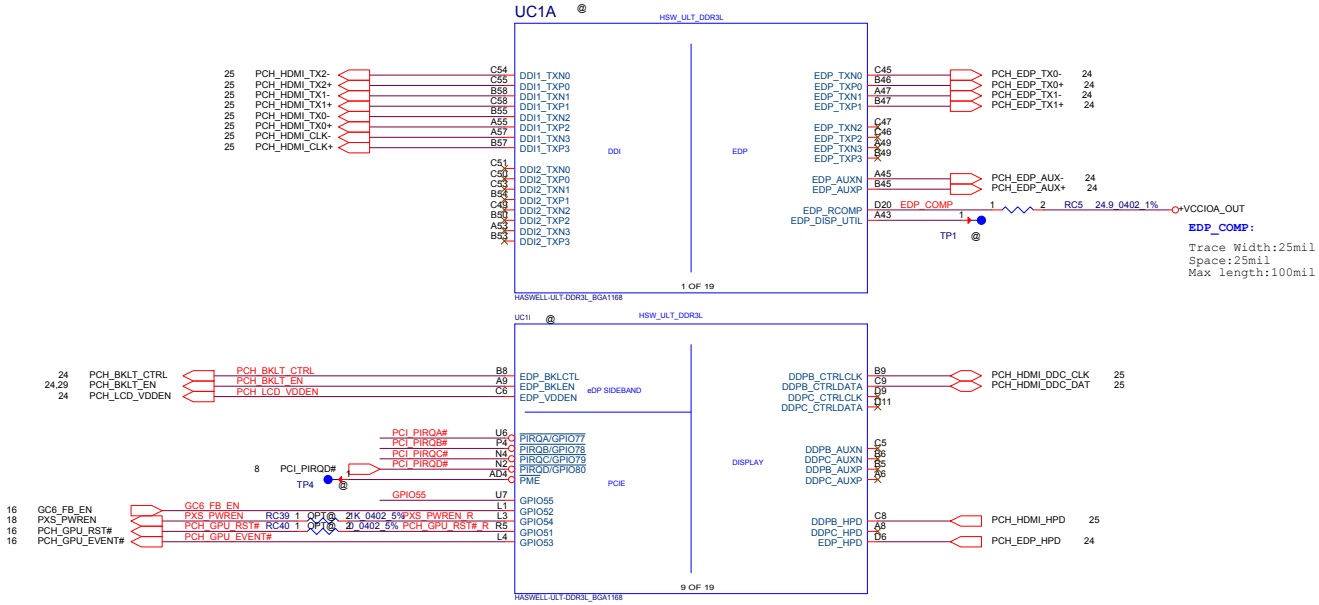
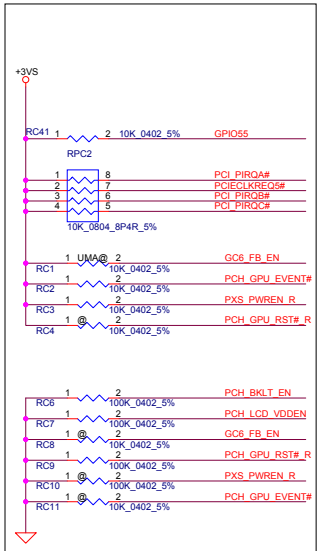
Haswell MCP (DDI,EDP)



Connect to GPU signal :
GC6_FB_EN
PCH_GPU_EVENT#
PCH_GPU_RST#
PCH_PLT_RST#
PXS_PWREN

PCIECLKREQ5# — PCIECLKREQ5# 8



Port	DDI PROCESSOR Pin Names	HDMI* Mapping
Port 1	DDI1_TXN[0]	HDMIxC_TX2_DN
	DDI1_TXP[0]	HDMIxC_TX2_DP
	DDI1_TXN[1]	HDMIxC_TX1_DN
	DDI1_TXP[1]	HDMIxC_TX1_DP
	DDI1_TXN[2]	HDMIxC_TX0_DN
	DDI1_TXP[2]	HDMIxC_TX0_DP
	DDI1_TXN[3]	HDMIxC_CLK_DN
	DDI1_TXP[3]	HDMIxC_CLK_DP
	DDPB_HPD	DDI1_HPD_Q
	DDPB_CTRLCLK	DDI1_CTRL_CK
	DDPB_CTRLDATA	DDI1_CTRL_DATA

DisplayPort* Disabling and Termination

Pin Name	Recommendation
DDPC_AUXP	No Connect
DDPC_AUXN	No Connect
DDPC_HPD	No Connect
DDI2_TXP[3:0]	No Connect
DDI2_TXN[3:0]	No Connect
DDPC_CTRLCLK	No Connect
DDPC_CTRLDATA	No Connect

Title: MCP (DDI,EDP)
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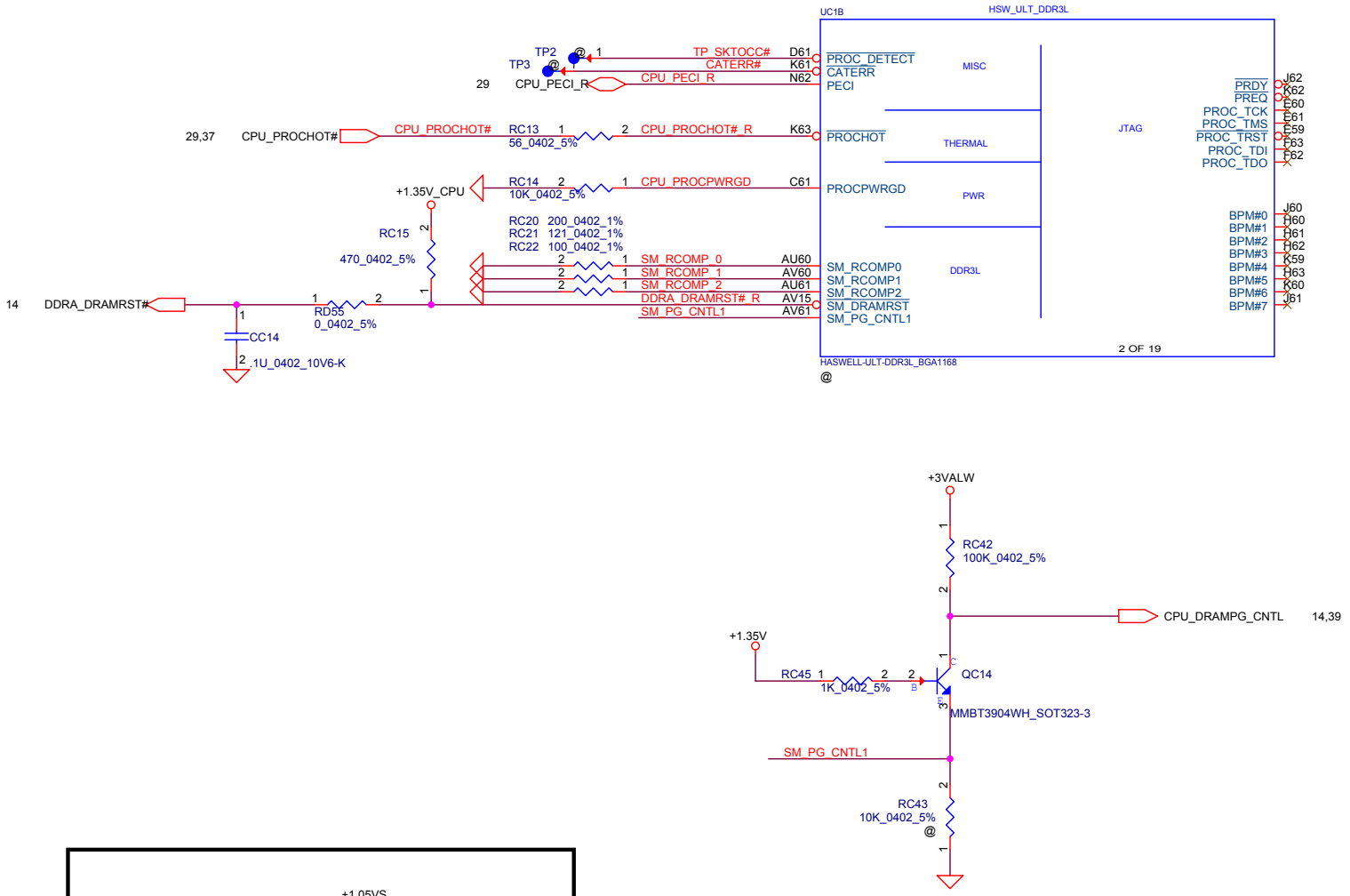
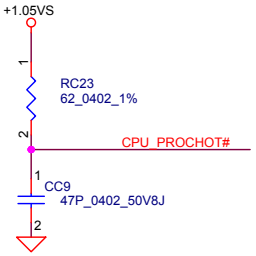


VR OD Output
Place CC9 Close to EC Side
RC23 Close to MCP
for Defensive Design
CPU_PROCHOT#



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Title: MCP (MISC,THERMAL,JATG

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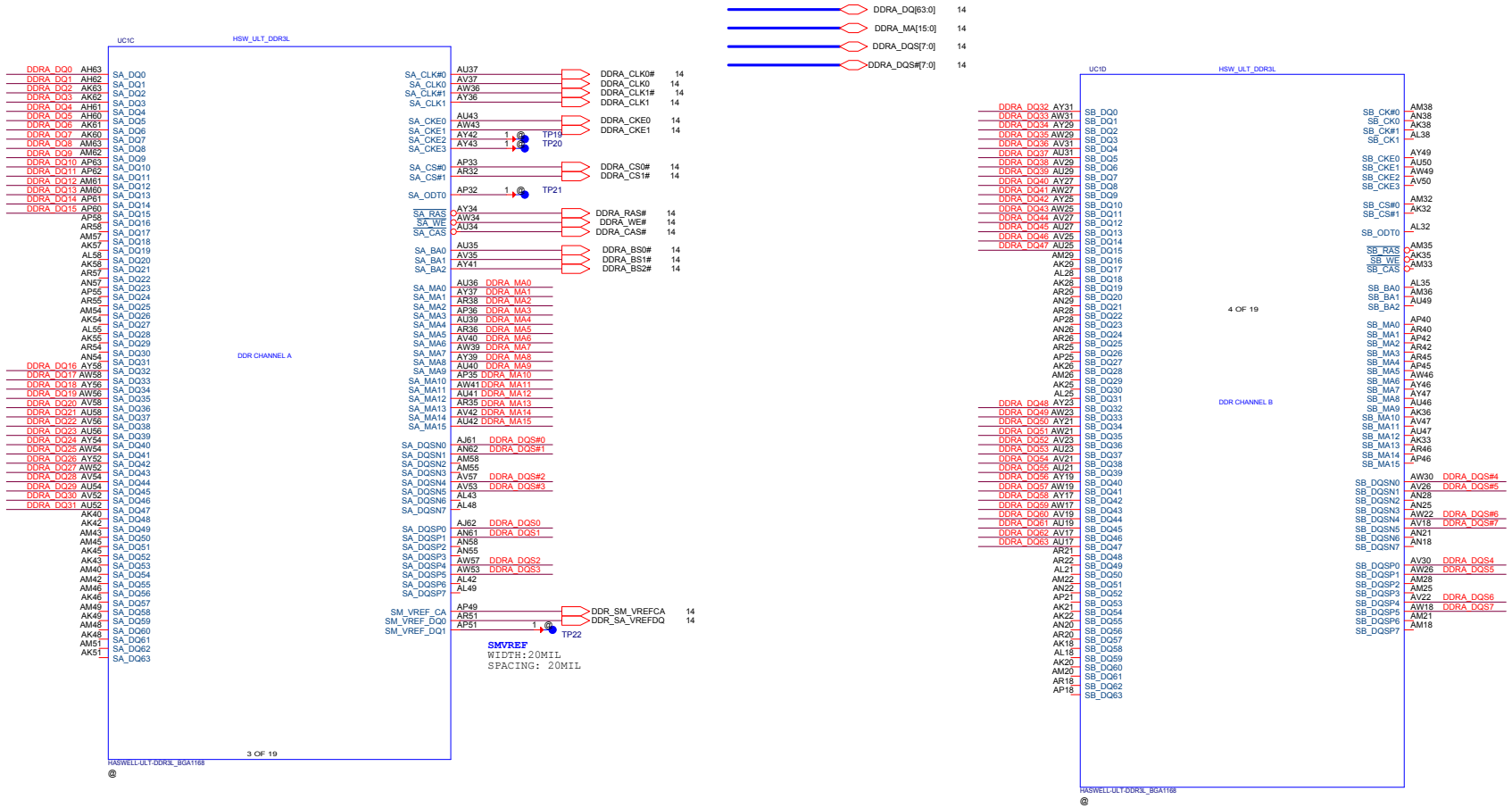
BDW-U 使用so-dimm时,白皮书给出的参照依据是interleaved,



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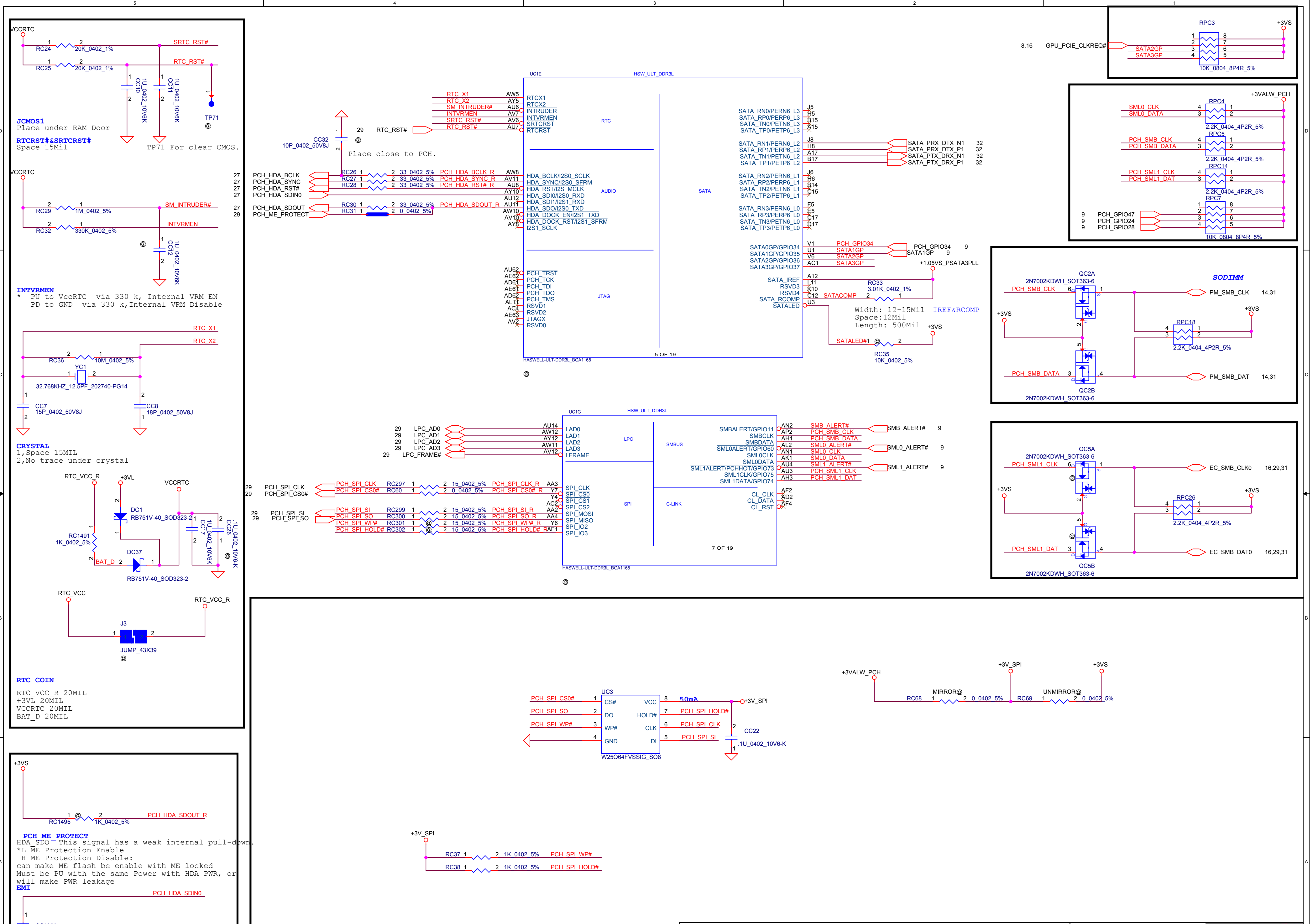

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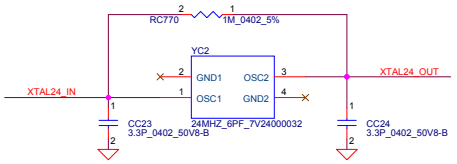
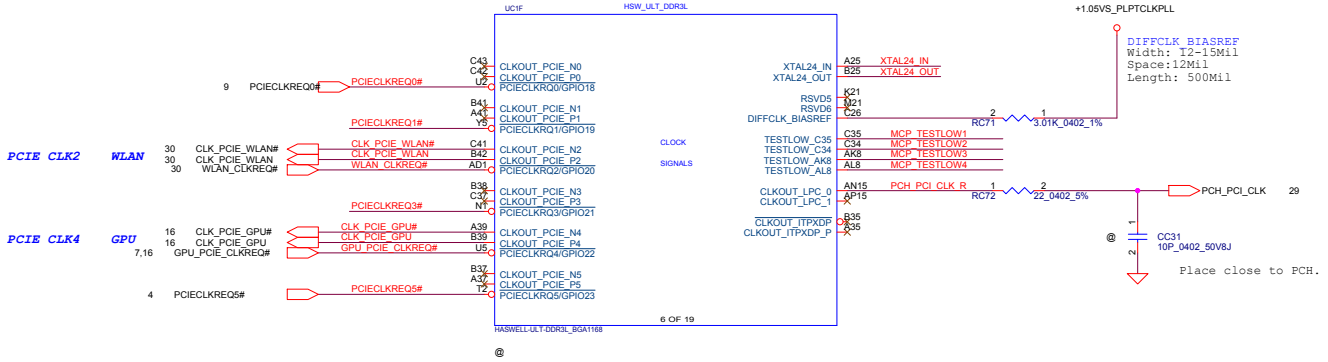
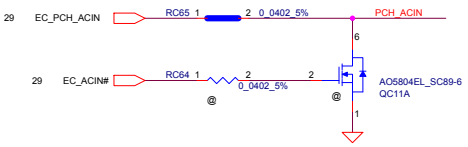
Haswell MCP (Clock,PM)

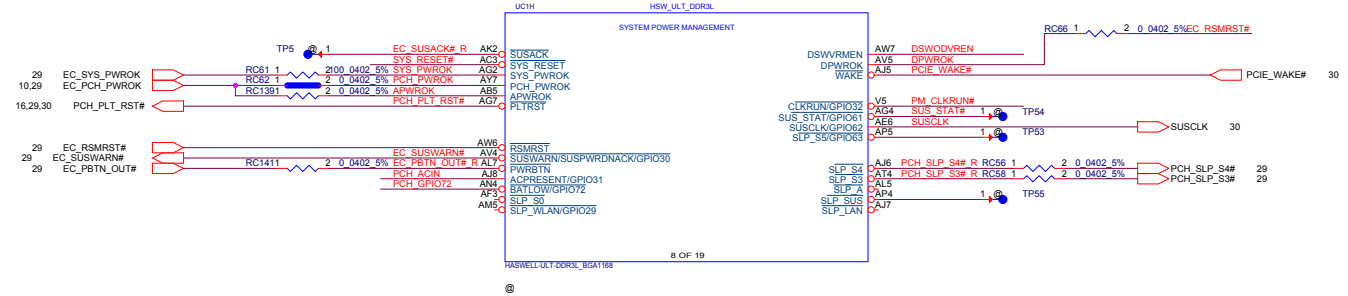


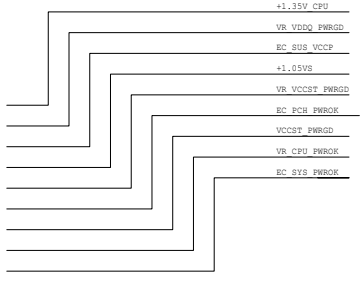


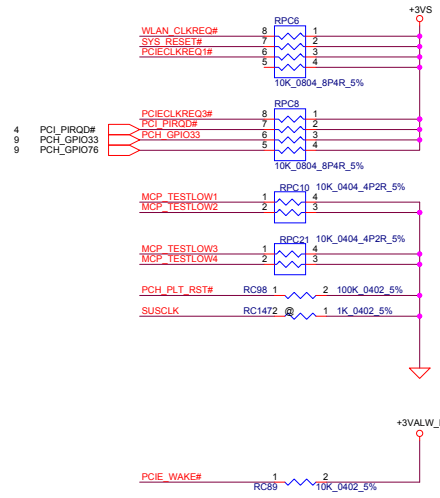
+1.05VS_PLPTCLKPLL

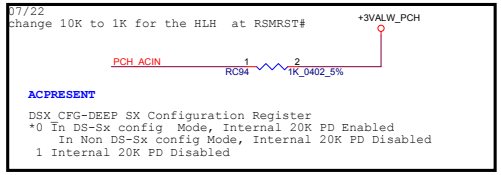
DIFFCLK_BIASREF
Width: T2-15Mil
Space:12Mil
Length: 500Mil

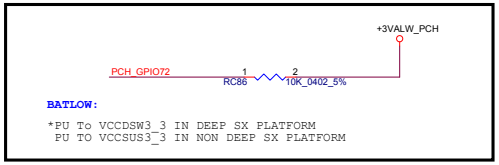


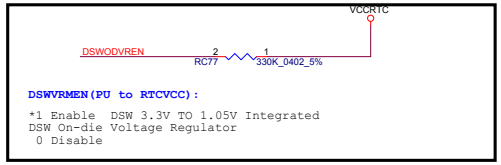


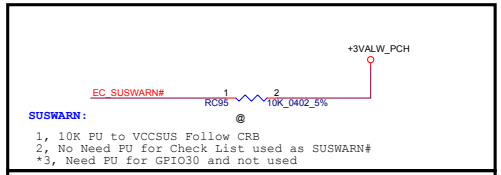


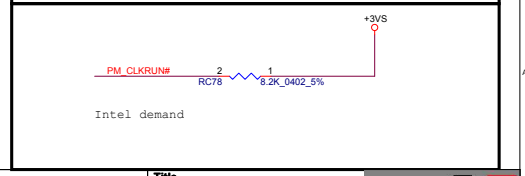












Title			
MCP (Clock,PM)			
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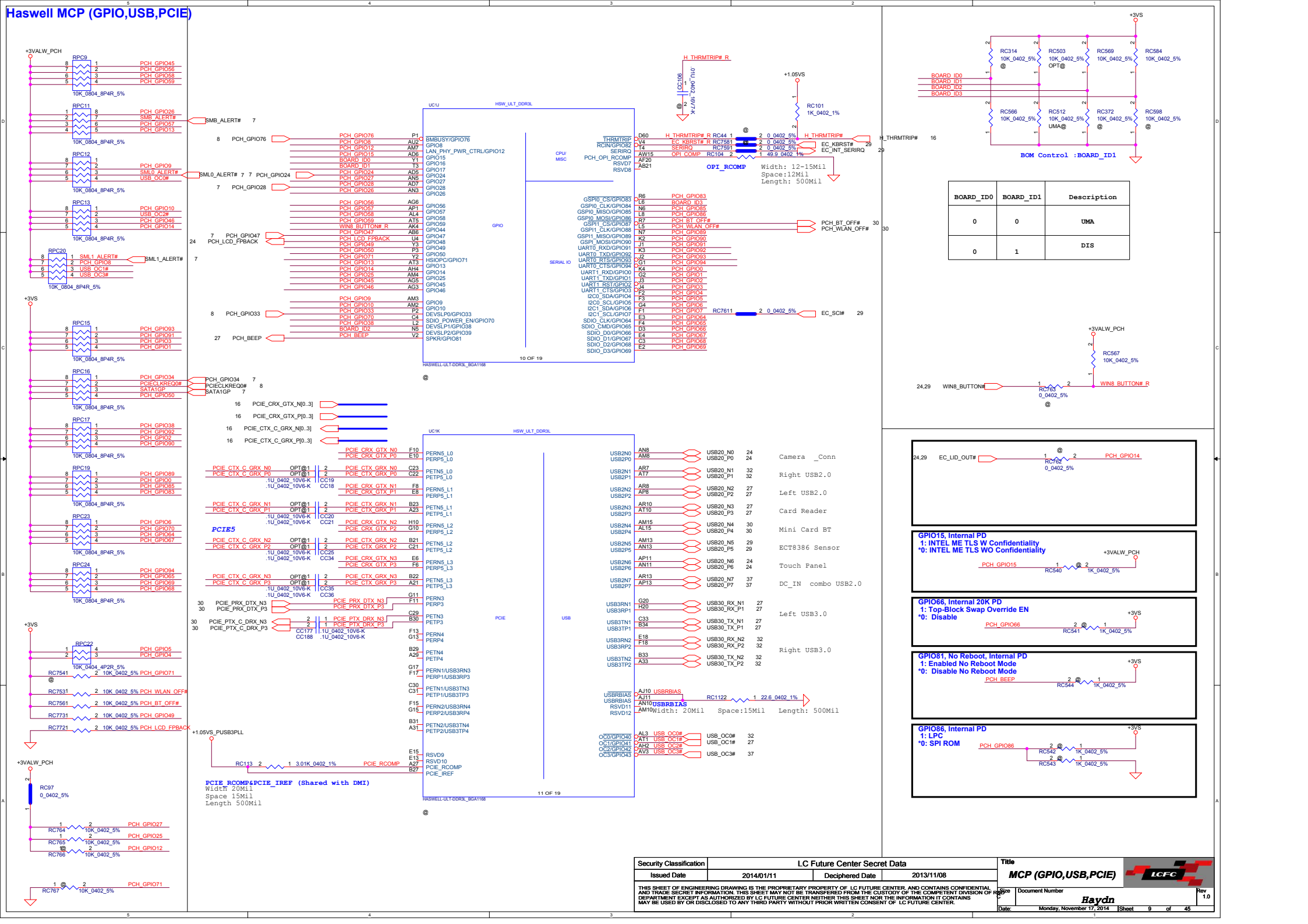
Haswell MCP (GPIO,USB,PCIE)



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Title	MCP (GPIO,USB,PCIE)		
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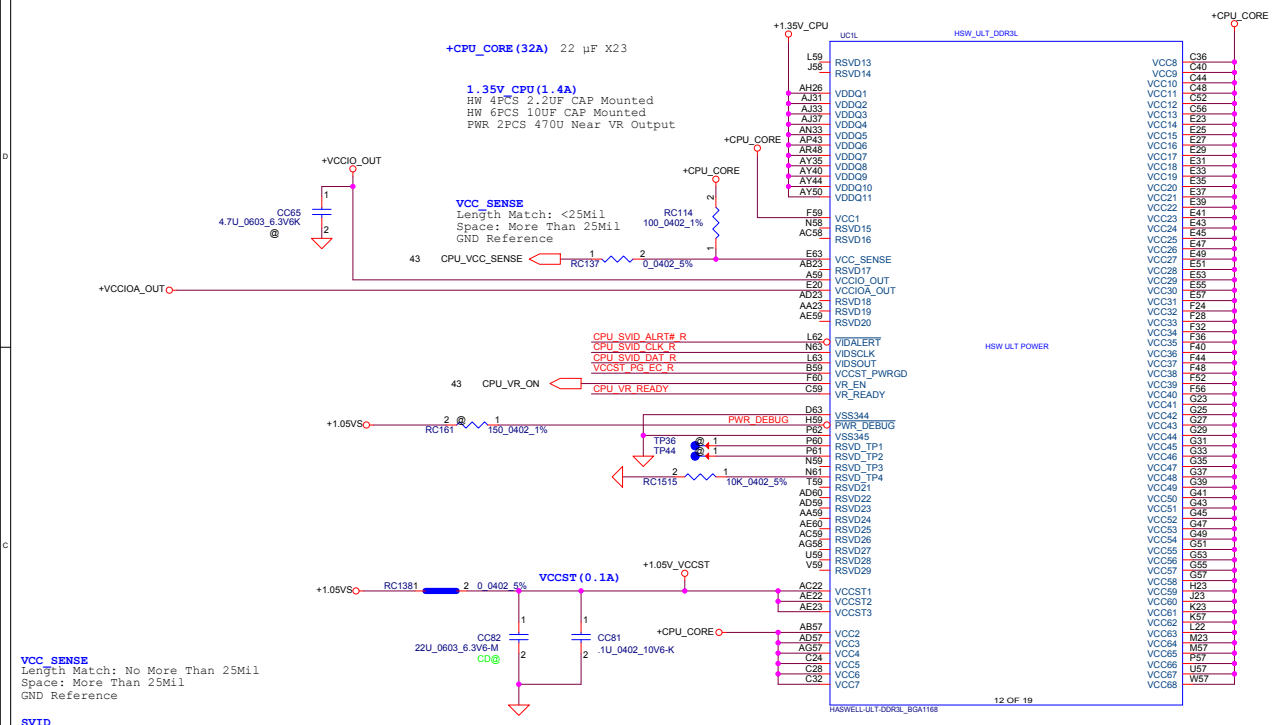
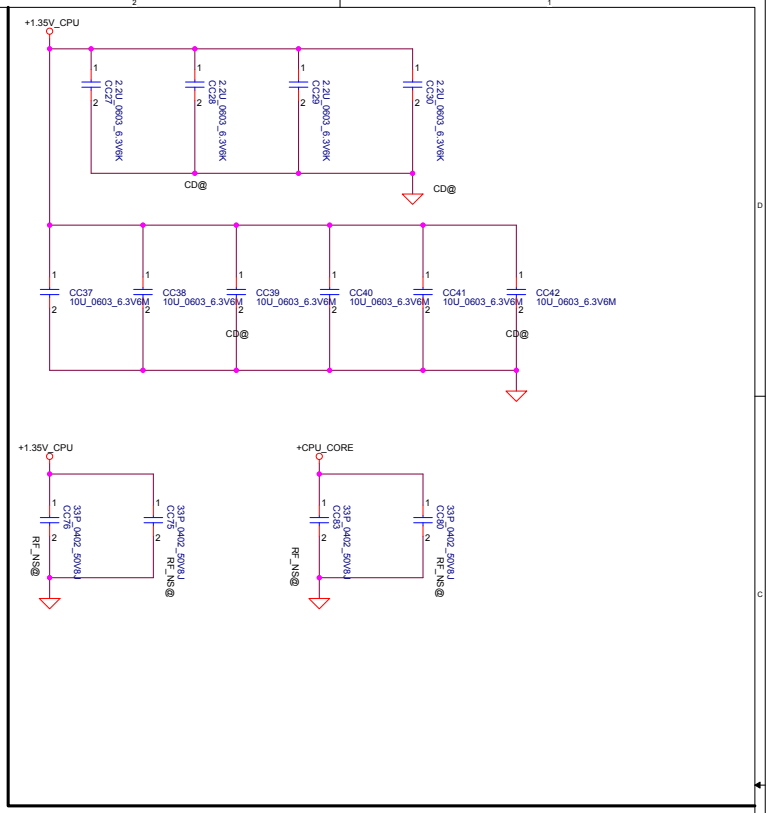
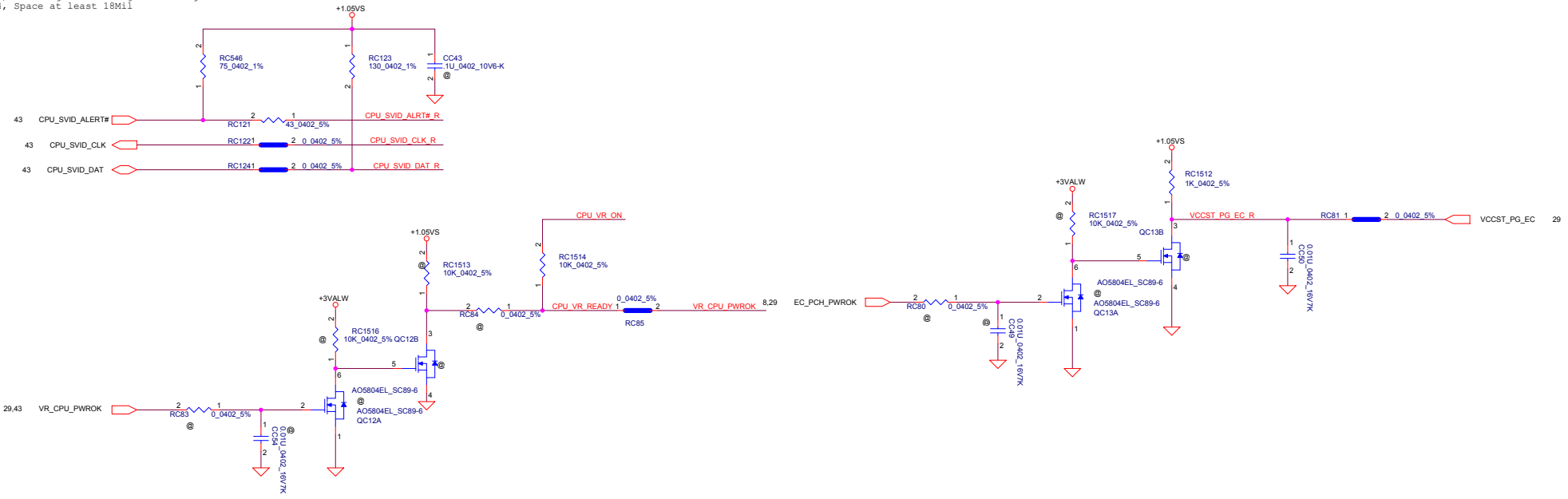
Haswell MCP (Power)





VCC_SENSE
Length Match: No More Than 25Mil
Space: More Than 25Mil
GND Reference

SVID
1, Stripline Line, No More Than 6000Mil
2, Alert# Route Between CLK and Data
3, CLK Length<Data Length<CLK Length + 2000Mil
4, Space at least 18Mil



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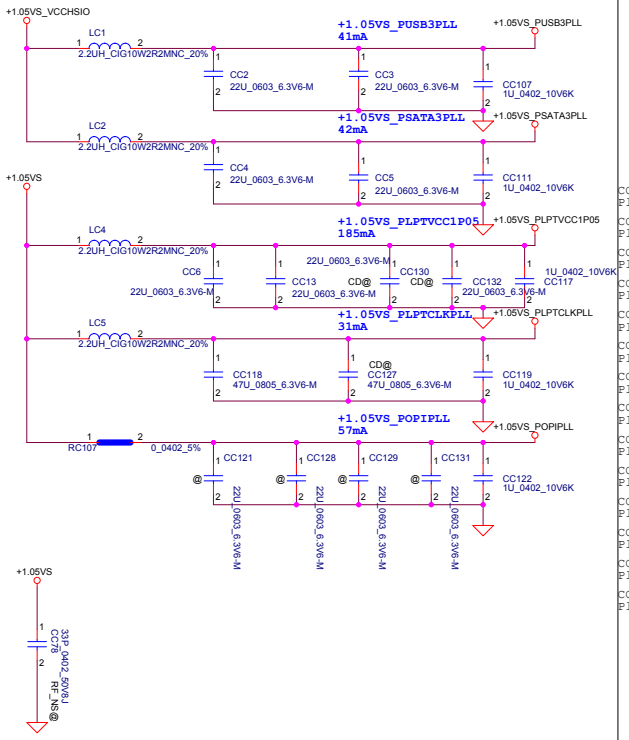
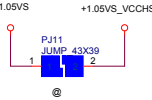
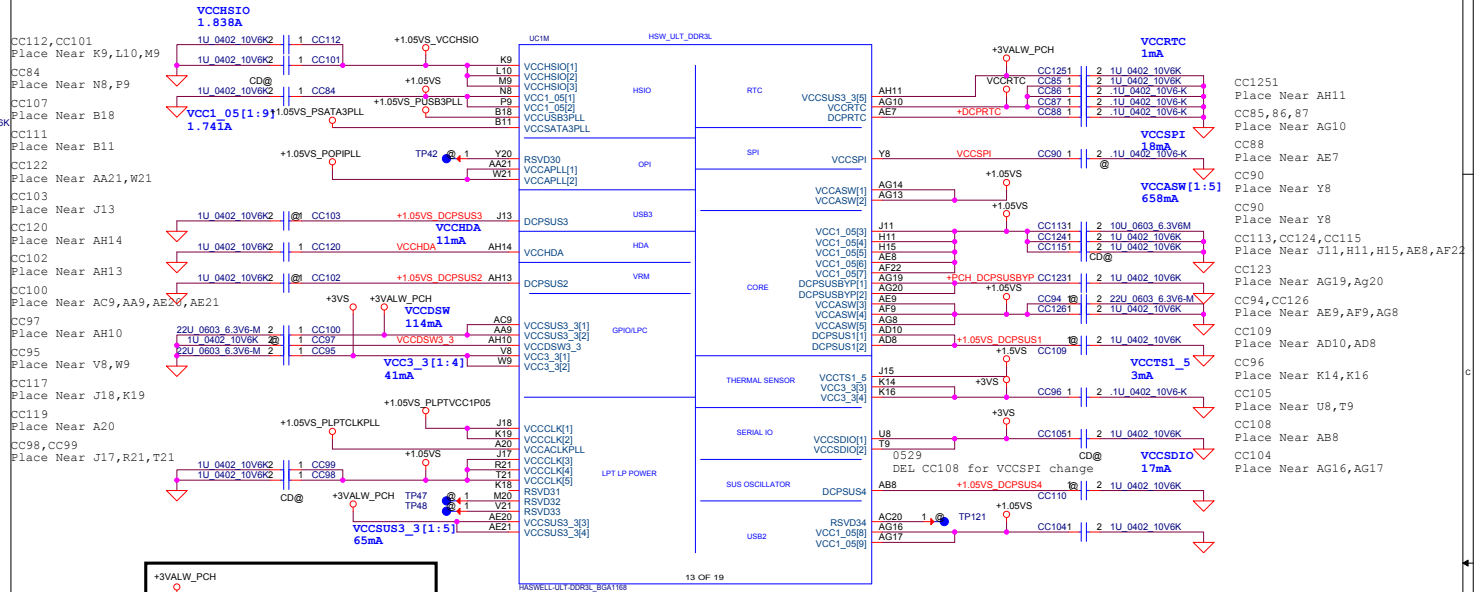
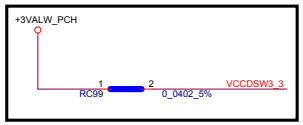
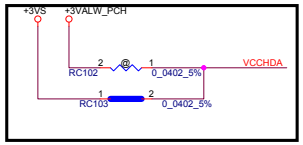
Haswell MCP (Power2)

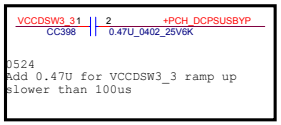


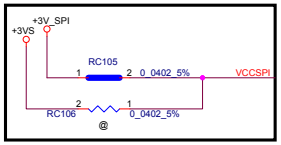












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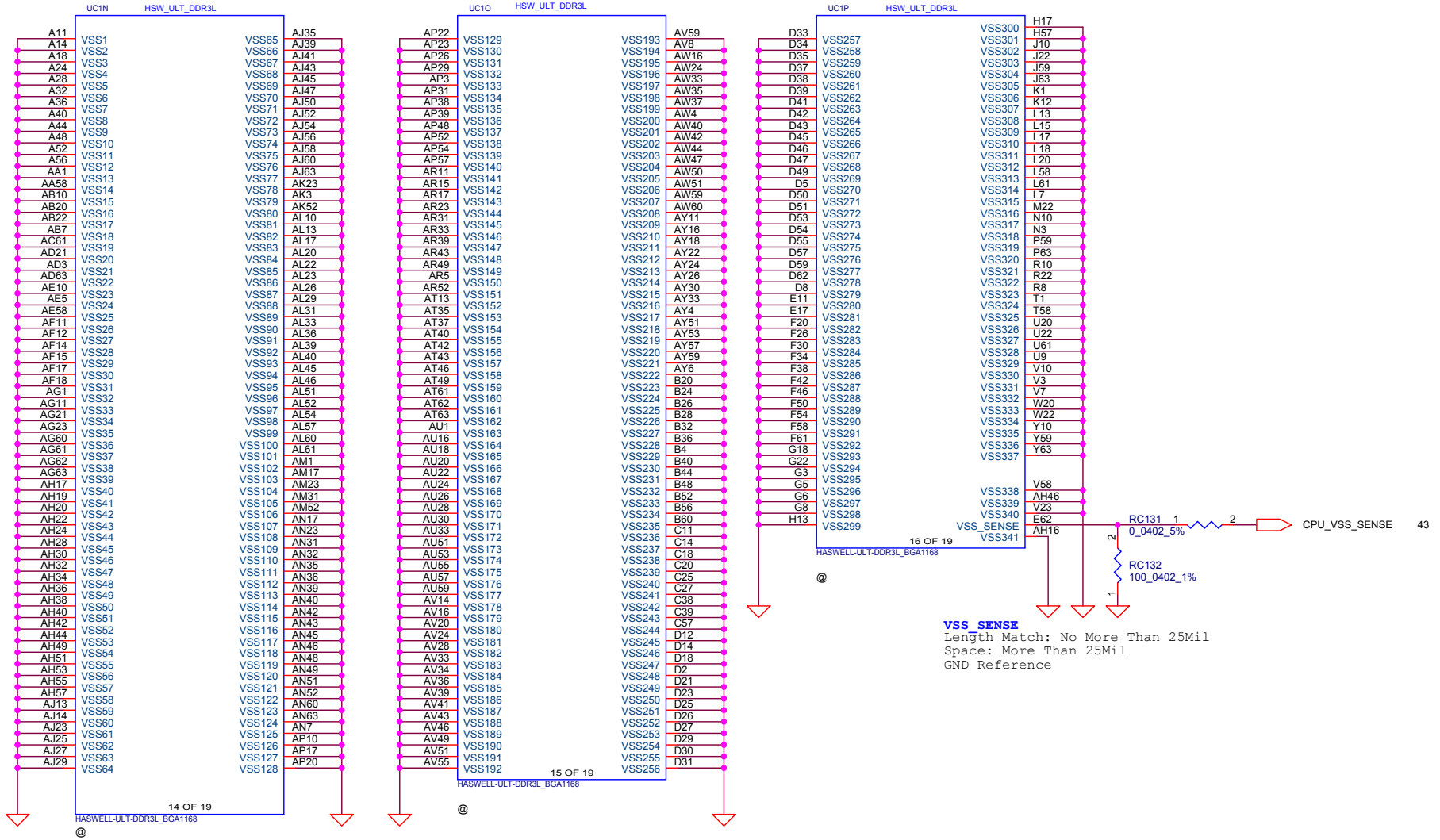
Haswell MCP (VSS)



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Title: MCP (VSS)

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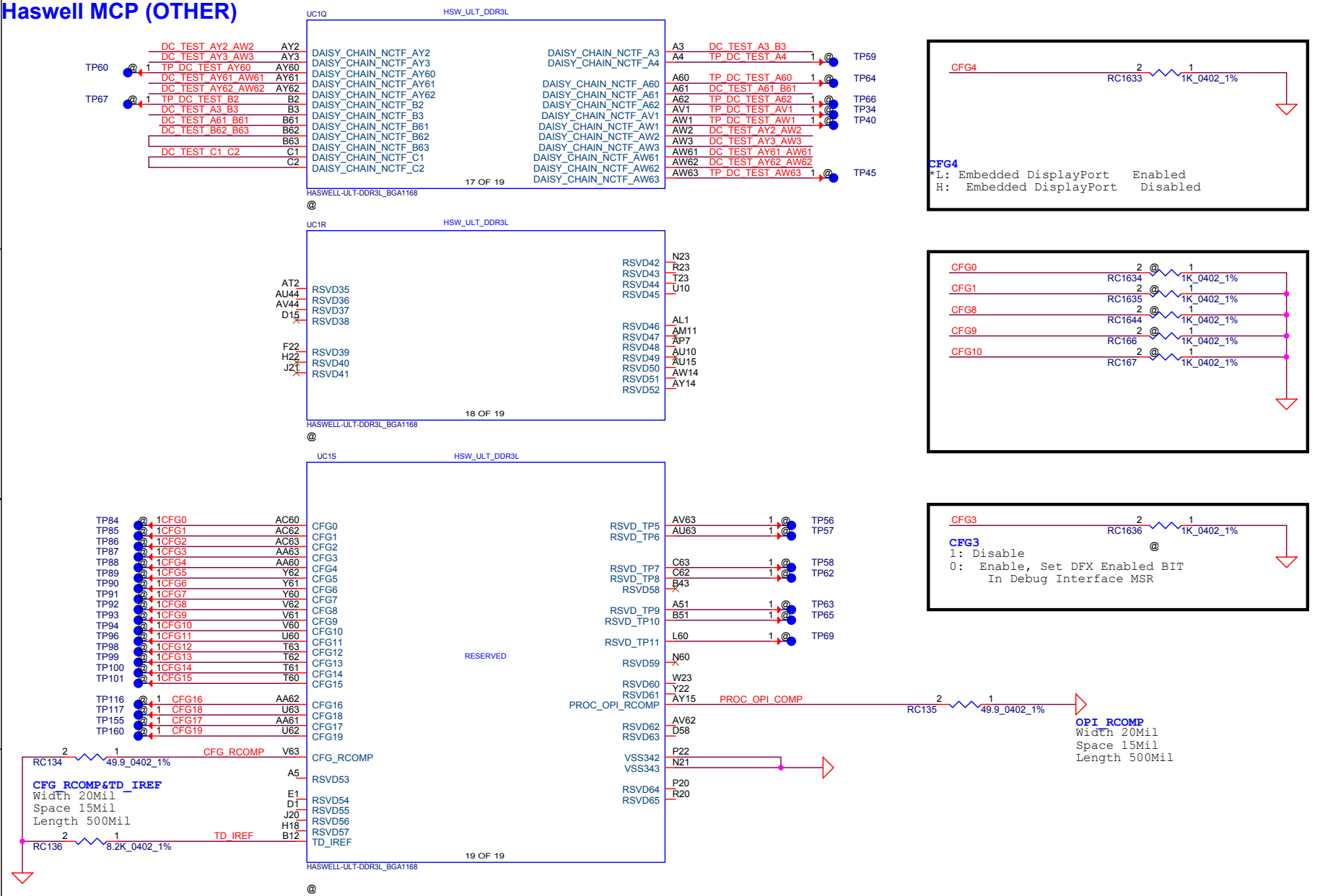
Haswell MCP (OTHER)



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Title: MCP (OTHER)

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DDR SO-DIMM

Trace width:20 mils
Space:20mils

DDR Swap Table

New Net Name	Pin Number	Old Net Name

VDDQ(2A)
Decoupling CAP

4 PCS 1UF CAP Near Each Side Of DIMM VDD Pin
4PCS 10UF CAP Near Each Side Of DIMM VDD Pin

VTT(700mA)
Decoupling CAP

4PCS 0.1UF CAP Near The DIMM
2PCS 10UF CAP On the VTT Island

For RF request

JDDRL

LCN_DAN06-K4408-0103

ME@ DIMM ADRESS: SA1:SA0 00

Trace width:20 mils
Space:20mils

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Title	DDR3L		
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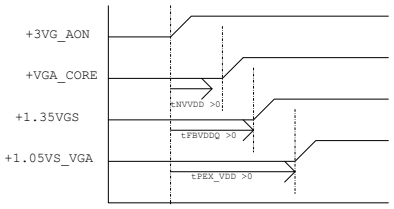
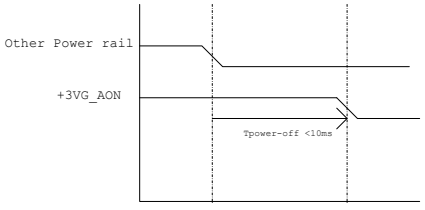
N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

N15V-GM Power Sequence

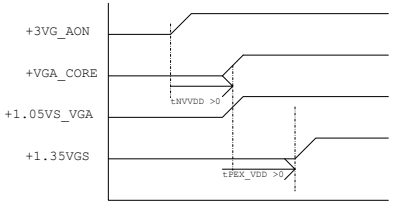


1. all power rail ramp up time should be larger than 40us



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

N15S-GT Power Sequence



1. all power rail ramp up time should be larger than 40us and less than 2ms .

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

Products	GPU (4) (W)	Mem (1,5) (MHz)	NVCLK /MCLK	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)		I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD		TBD	TBD	TBD	TBD

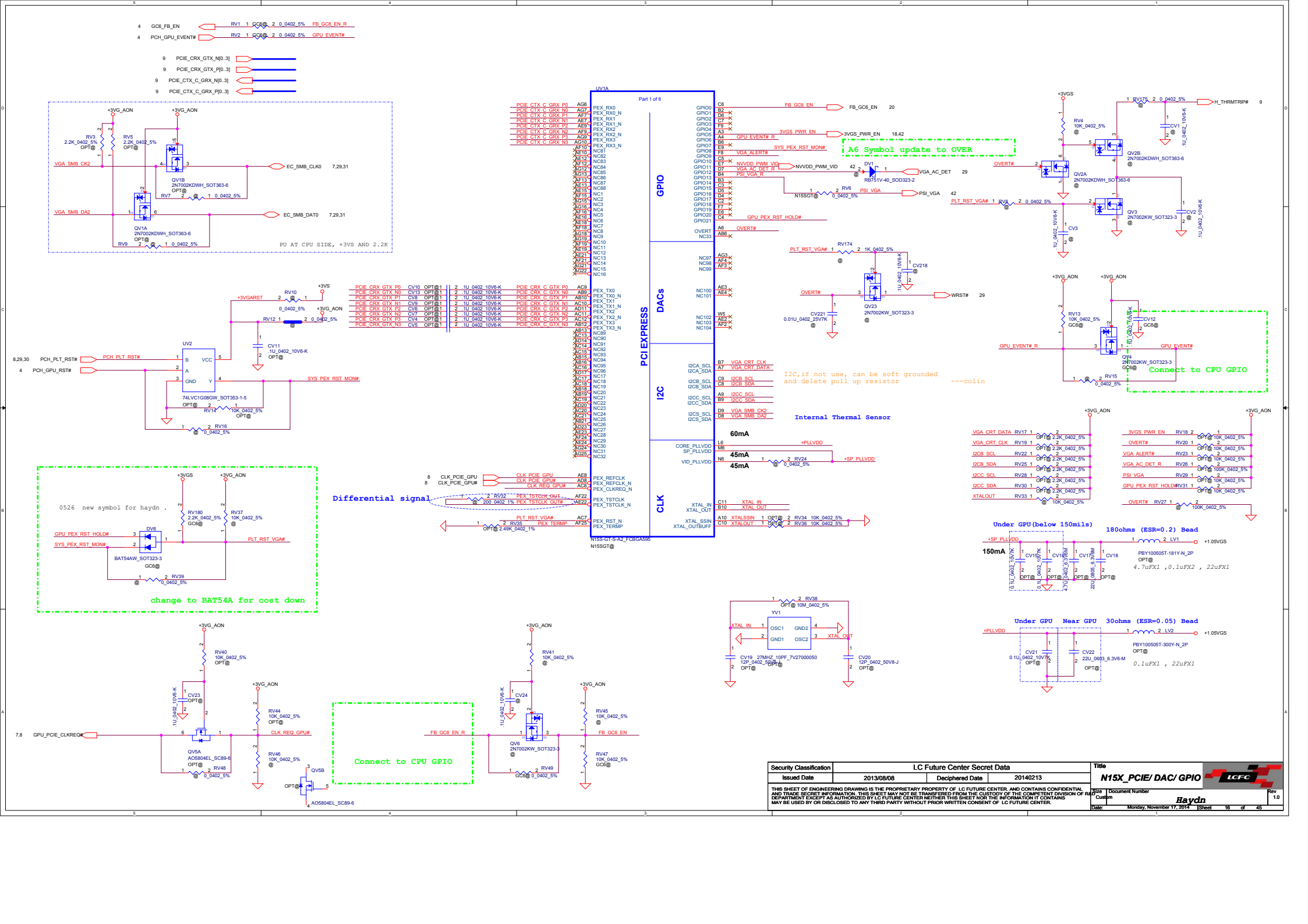
N15x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

N15x Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED


GC6_FB_EN
PCH_GPU_EVENT#
RV1 GC6@ FB_GC6_EN_R
RV2 GC6@ GPU_EVENT#
PCIE_CRX_GTX_N[0..3]
PCIE_CRX_GTX_P[0..3]
PCIE_CTX_C_GRX_N[0..3]
PCIE_CTX_C_GRX_P[0..3]
+3VG_AON
VGA_SMB_CK2
VGA_SMB_DA2
QV1B 2N7002KDWH_SOT363-6
QV1A 2N7002KDWH_SOT363-6
EC_SMB_CLK0 7,29,31
EC_SMB_DAT0 7,29,31
PU AT CPU SIDE, +3VS AND 2.2K
UV1A
Part 1 of 6
PCI EXPRESS
GPIO
DACs
I2C
CLK
FB_GC6_EN
3VGS_PWR_EN
SYS_PEX_RST_MON#
NVVDD_PWM_VID
VGA_AC_DET
PSI_VGA
GPU_PEX_RST_HOLD#
OVERT#
VGA_ALERT#
A6 Symbol update to OVER
H_THRMTRIP# 9
WRST# 29
GPU_EVENT#
Connect to CPU GPIO
I2C,if not use, can be soft grounded and delete pull up resistor ---colin
Internal Thermal Sensor
60mA
45mA
45mA
+PLLVDD
+SP_PLLVDD
Differential signal
CLK_PCIE_GPU
CLK_PCIE_GPU#
CLK_REQ_GPU#
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
PLT_RST_VGA#
PEX_TERMP
XTAL_IN
XTAL_OUT
XTALSSIN
XTALOUT
N15S-GT-S-A2_FCBGA595
N15SGT@
+3VGS
+3VGARST
PCH_PLT_RST#
PCH_GPU_RST#
74LVC1G08GW_SOT353-1-5
0526 new symbol for haydn .
BAT54AW_SOT323-3
change to BAT54A for cost down
Under GPU(below 150mils)
180ohms (ESR=0.2) Bead
150mA
PBY100505T-181Y-N_2P
4.7uFX1 ,0.1uFX2 , 22uFX1
Under GPU Near GPU 30ohms (ESR=0.05) Bead
PBY100505T-300Y-N_2P
0.1uFX1 , 22uFX1
YV1
CV19 27MHZ_10PF_7V27000050
CV20 12P_0402_50V8-J
QV5A AO5804EL_SC89-6
QV5B AO5804EL_SC89-6
QV6 2N7002KW_SOT323-3
QV23 2N7002KW_SOT323-3
QV4 2N7002KW_SOT323-3
QV2A 2N7002KDWH_SOT363-6
QV2B 2N7002KDWH_SOT363-6
QV3 2N7002KW_SOT323-3
RB751V-40_SOD323-2
Connect to CPU GPIO
Security Classification
LC Future Center Secret Data
Issued Date
2013/08/08
Deciphered Date
20140213
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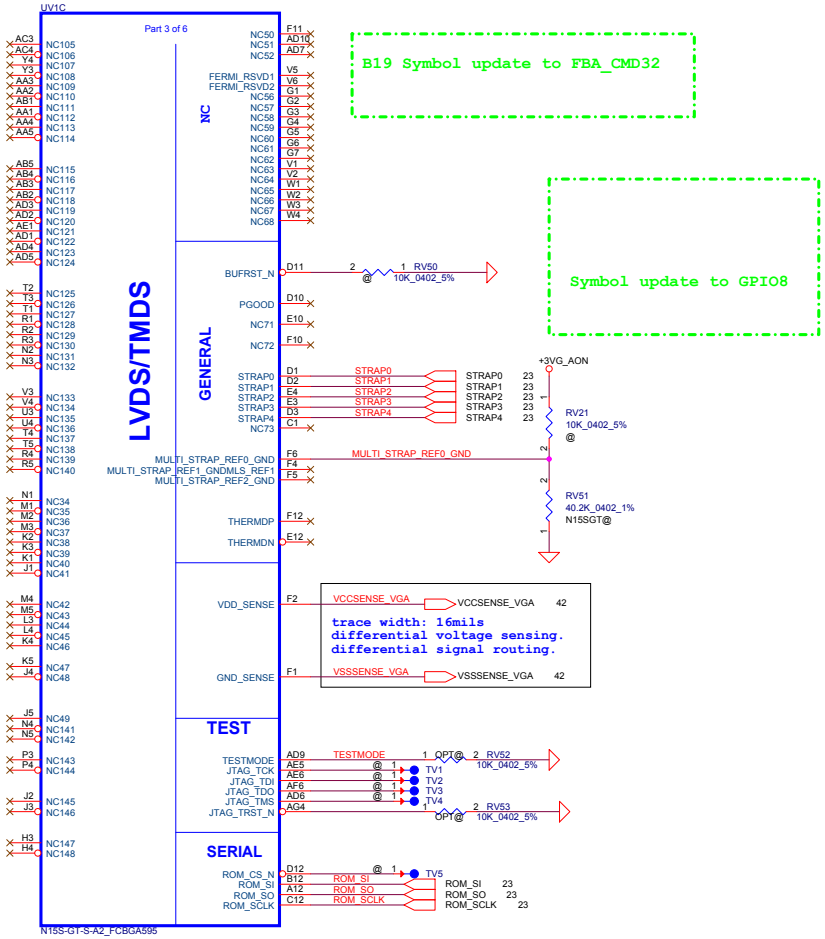
Title
N15X_PCIE/ DAC/ GPIO
Size Custom
Document Number
Haydn
Rev 1.0
Date: Monday, November 17, 2014
Sheet 16 of 45

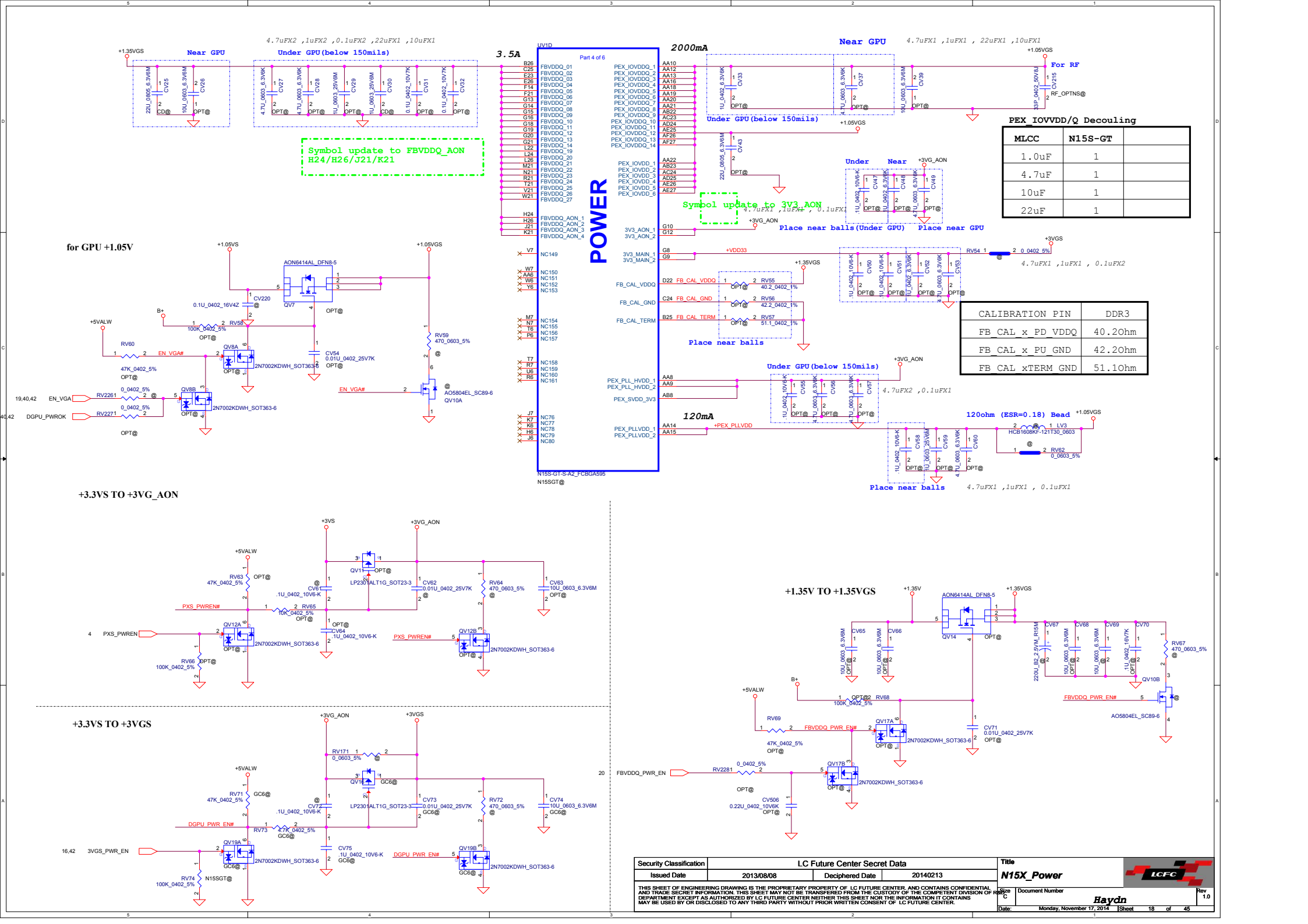


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	20140213

Title: N15X_LVDS/ HDMI/ THERM

Size	Document Number	Rev
C	Haydn	1.0

Date: Monday, November 17, 2014 Sheet 17 of 45


Near GPU
Under GPU(below 150mils)
3.5A
2000mA
120mA
Symbol update to FBVDDQ_AON
H24/H26/J21/K21
Symbol update to 3V3_AON
POWER
Part 4 of 6
N15S-GT-S-A2_FCBGA595
N15SGT@
Place near balls(Under GPU)
Place near GPU
Place near balls
PEX_IOVDDQ/Q Decoupling
MLCC | N15S-GT
1.0uF | 1
4.7uF | 1
10uF | 1
22uF | 1
CALIBRATION PIN | DDR3
FB_CAL_x_PD_VDDQ | 40.2Ohm
FB_CAL_x_PU_GND | 42.2Ohm
FB_CAL_xTERM_GND | 51.1Ohm
120ohm (ESR=0.18) Bead
for GPU +1.05V
+3.3VS TO +3VG_AON
+3.3VS TO +3VGS
+1.35V TO +1.35VGS
Security Classification
LC Future Center Secret Data
Issued Date
2013/08/08
Deciphered Date
20140213
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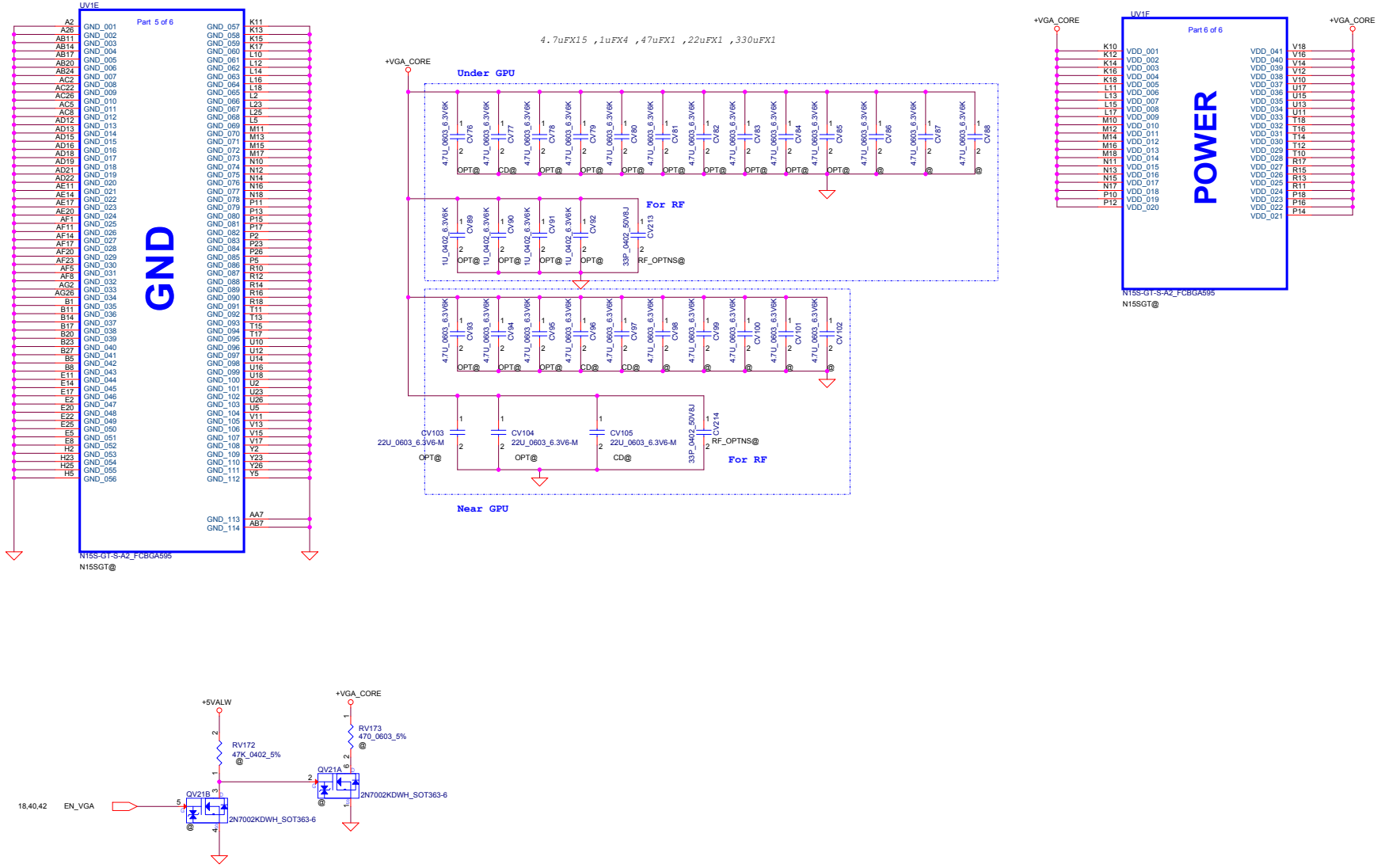
Title
N15X_Power
Size C
Document Number
Haydn
Rev 1.0
Date: Monday, November 17, 2014
Sheet 18 of 45



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	20140213

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Title: N15X_+VGA CORE, GND

Size: C | Document Number: Haydn | Rev: 1.0

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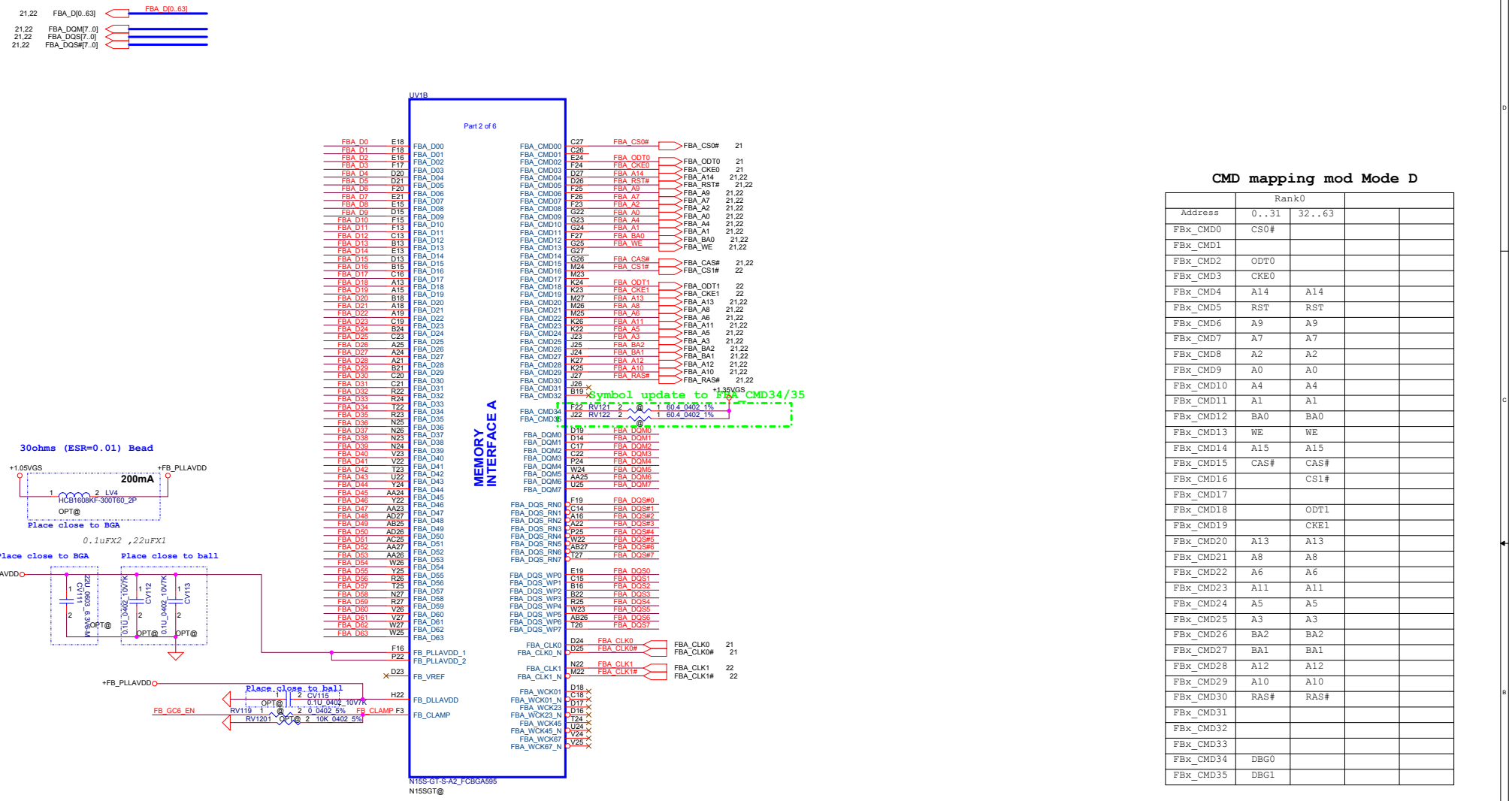

CMD mapping mod Mode D

	Rank0			
Address	0..31	32..63		
FBx_CMD0	CS0#			
FBx_CMD1				
FBx_CMD2	ODT0			
FBx_CMD3	CKE0			
FBx_CMD4	A14	A14		
FBx_CMD5	RST	RST		
FBx_CMD6	A9	A9		
FBx_CMD7	A7	A7		
FBx_CMD8	A2	A2		
FBx_CMD9	A0	A0		
FBx_CMD10	A4	A4		
FBx_CMD11	A1	A1		
FBx_CMD12	BA0	BA0		
FBx_CMD13	WE	WE		
FBx_CMD14	A15	A15		
FBx_CMD15	CAS#	CAS#		
FBx_CMD16		CS1#		
FBx_CMD17				
FBx_CMD18		ODT1		
FBx_CMD19		CKE1		
FBx_CMD20	A13	A13		
FBx_CMD21	A8	A8		
FBx_CMD22	A6	A6		
FBx_CMD23	A11	A11		
FBx_CMD24	A5	A5		
FBx_CMD25	A3	A3		
FBx_CMD26	BA2	BA2		
FBx_CMD27	BA1	BA1		
FBx_CMD28	A12	A12		
FBx_CMD29	A10	A10		
FBx_CMD30	RAS#	RAS#		
FBx_CMD31				
FBx_CMD32				
FBx_CMD33				
FBx_CMD34	DBG0			
FBx_CMD35	DBG1			

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Issued Date	2013/08/08	Deciphered Date	20140213

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Title: N15X_MEM Interface

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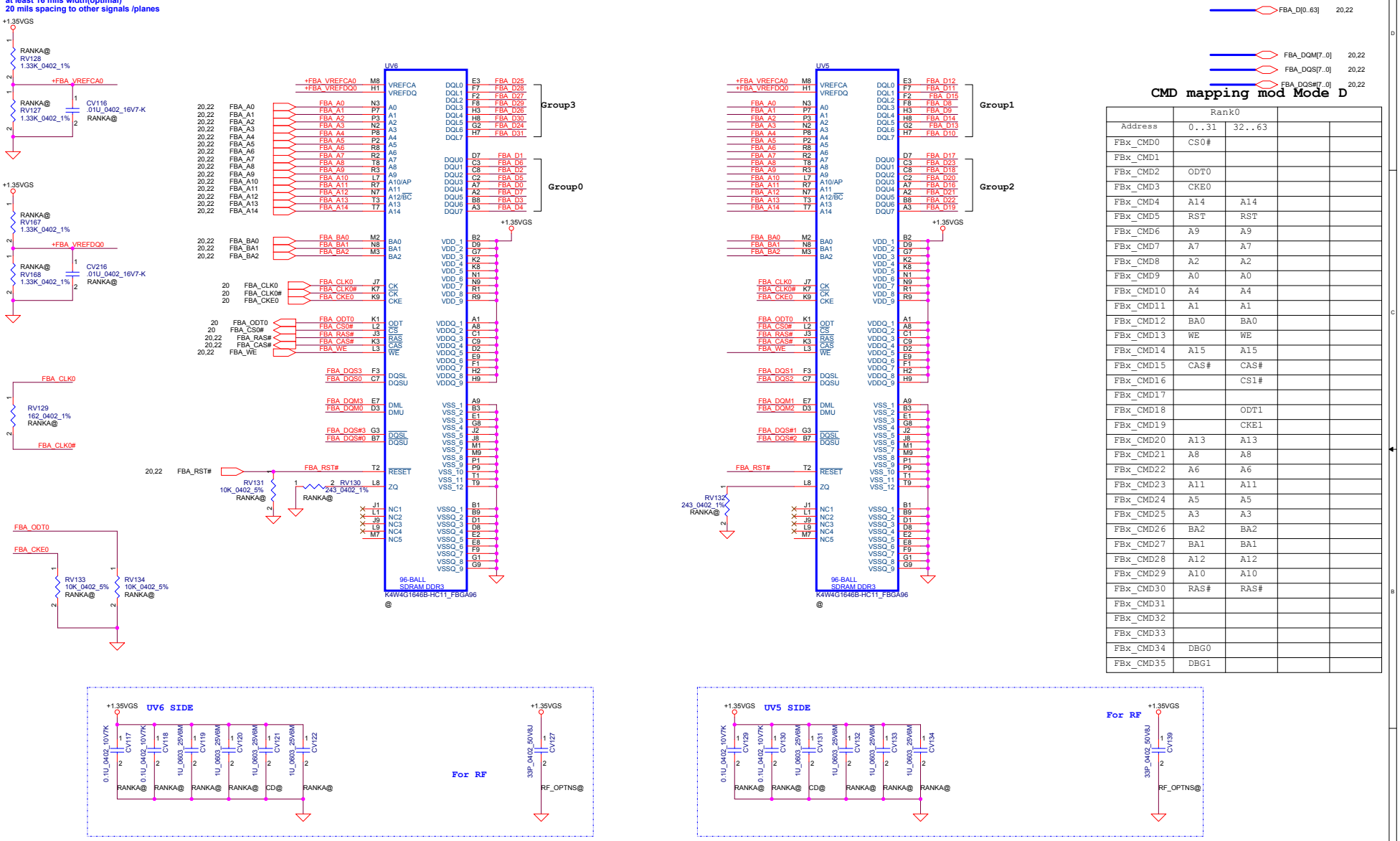
at least 16 mils width(optimal)
20 mils spacing to other signals /planes



CMD mapping mod Mode D

	Rank0			
Address	0..31	32..63		
FBx_CMD0	CS0#			
FBx_CMD1				
FBx_CMD2	ODT0			
FBx_CMD3	CKE0			
FBx_CMD4	A14	A14		
FBx_CMD5	RST	RST		
FBx_CMD6	A9	A9		
FBx_CMD7	A7	A7		
FBx_CMD8	A2	A2		
FBx_CMD9	A0	A0		
FBx_CMD10	A4	A4		
FBx_CMD11	A1	A1		
FBx_CMD12	BA0	BA0		
FBx_CMD13	WE	WE		
FBx_CMD14	A15	A15		
FBx_CMD15	CAS#	CAS#		
FBx_CMD16		CS1#		
FBx_CMD17				
FBx_CMD18		ODT1		
FBx_CMD19		CKE1		
FBx_CMD20	A13	A13		
FBx_CMD21	A8	A8		
FBx_CMD22	A6	A6		
FBx_CMD23	A11	A11		
FBx_CMD24	A5	A5		
FBx_CMD25	A3	A3		
FBx_CMD26	BA2	BA2		
FBx_CMD27	BA1	BA1		
FBx_CMD28	A12	A12		
FBx_CMD29	A10	A10		
FBx_CMD30	RAS#	RAS#		
FBx_CMD31				
FBx_CMD32				
FBx_CMD33				
FBx_CMD34	DBG0			
FBx_CMD35	DBG1			

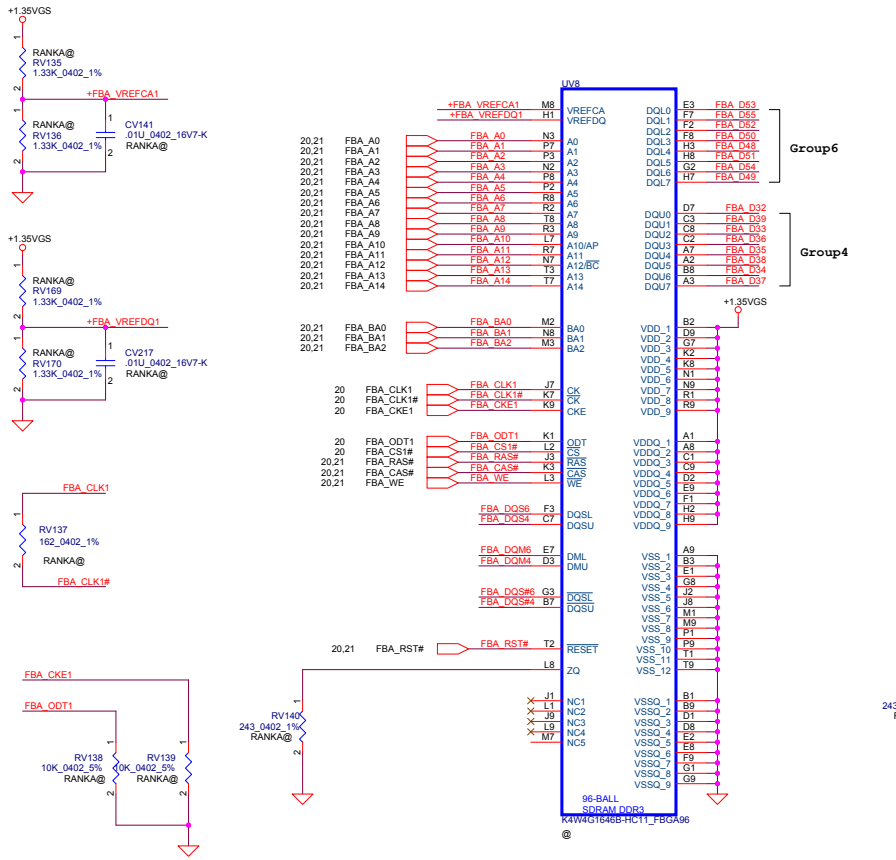
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	20140213

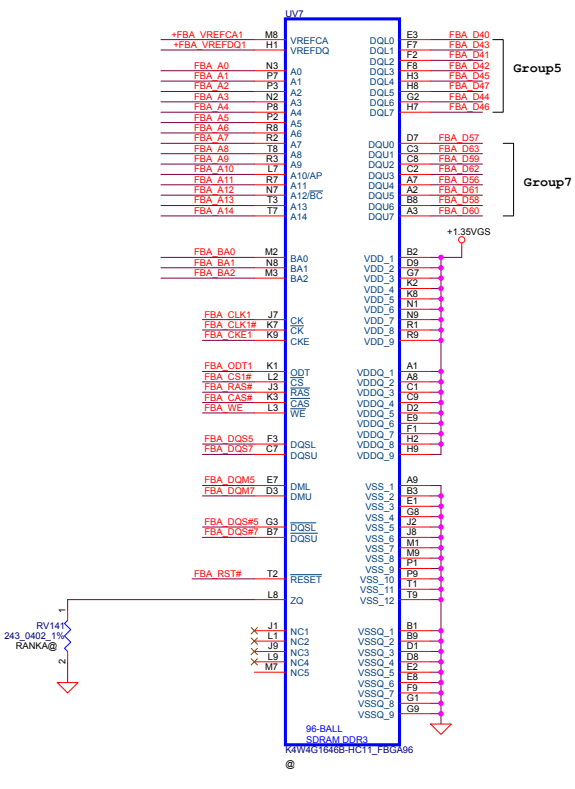
Title: DDR3 VRAM Rank0_L

Size: C | Document Number: Haydn | Rev: 1.0

Date: Monday, November 17, 2014 | Sheet 21 of 45

at least 16 mils width(optimal)
20 mils spacing to other signals /planes

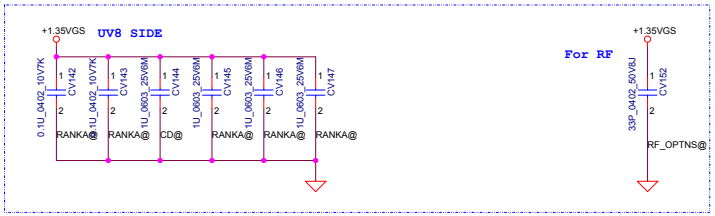


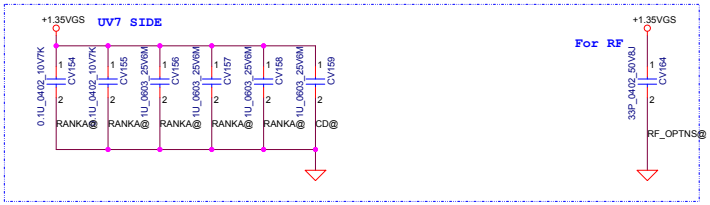


FBA_D[0..63] 20,21
FBA_DQM[7..0] 20,21
FBA_DQS[7..0] 20,21
FBA_DQS#[7..0] 20,21

CMD mapping mod Mode D

	Rank0			
Address	0..31	32..63		
FBx_CMD0	CS0#			
FBx_CMD1				
FBx_CMD2	ODT0			
FBx_CMD3	CKE0			
FBx_CMD4	A14	A14		
FBx_CMD5	RST	RST		
FBx_CMD6	A9	A9		
FBx_CMD7	A7	A7		
FBx_CMD8	A2	A2		
FBx_CMD9	A0	A0		
FBx_CMD10	A4	A4		
FBx_CMD11	A1	A1		
FBx_CMD12	BA0	BA0		
FBx_CMD13	WE	WE		
FBx_CMD14	A15	A15		
FBx_CMD15	CAS#	CAS#		
FBx_CMD16		CS1#		
FBx_CMD17				
FBx_CMD18		ODT1		
FBx_CMD19		CKE1		
FBx_CMD20	A13	A13		
FBx_CMD21	A8	A8		
FBx_CMD22	A6	A6		
FBx_CMD23	A11	A11		
FBx_CMD24	A5	A5		
FBx_CMD25	A3	A3		
FBx_CMD26	BA2	BA2		
FBx_CMD27	BA1	BA1		
FBx_CMD28	A12	A12		
FBx_CMD29	A10	A10		
FBx_CMD30	RAS#	RAS#		
FBx_CMD31				
FBx_CMD32				
FBx_CMD33				
FBx_CMD34	DBG0			
FBx_CMD35	DBG1			





Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	20140213

Title: DDR3 VRAM Rank0_H

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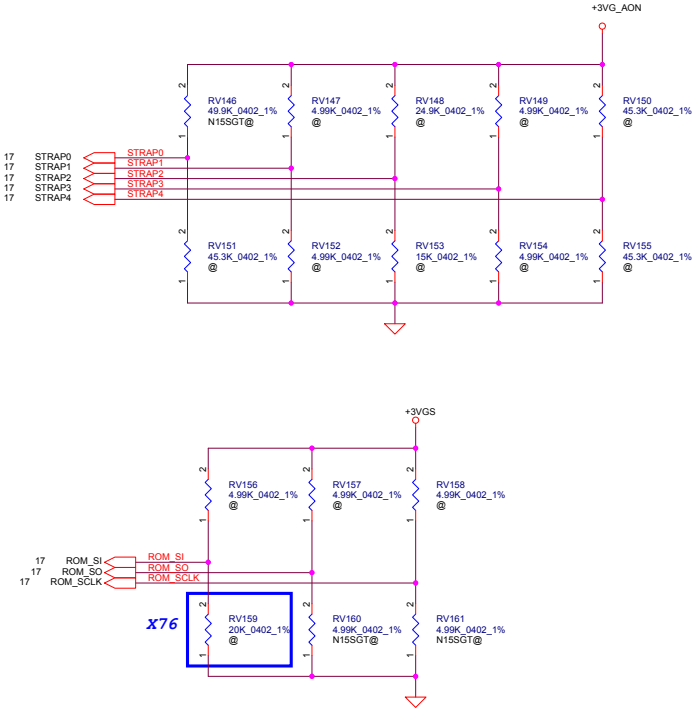

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

N15x Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

X76

GPU	FB Memory (DDR3)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N15S-GT	Hynix 900MHz	H5TC4G63AFR-11C 256M x 16	0x3 PD 20K	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff	Un-stuff
	Micron 900MHz	MT41J256M16HA-093G:E 256M x 16	0x4 PD 24.9K							
	Samsung 900MHz	K4W4G1646D-BC1A 256M x 16	0x5 PD 30.1K							
	Hynix 900MHz	H5TC2G63FFR-11C 128M x 16	0x9 PU 10K							
	Micron 900MHz	MT41J128M16JT-093G:K 128M x 16	0xA PU 15K							
	Samsung 900MHz	K4W2G1646Q-BC1A 128M x 16	0xB PU 20K							

VRAM	X76	VRAM P/N
Samsung	X76409JVL01	SA00005SH10
	X76409JVL51 (1G 32Mx16)	
Micron	X76409JVL02	SA00005M100
	X76409JVL02 (2G 64Mx32)	
Hynix		

Title		
N15X_MISC		
Size C	Document Number Haydn	Rev 1.0
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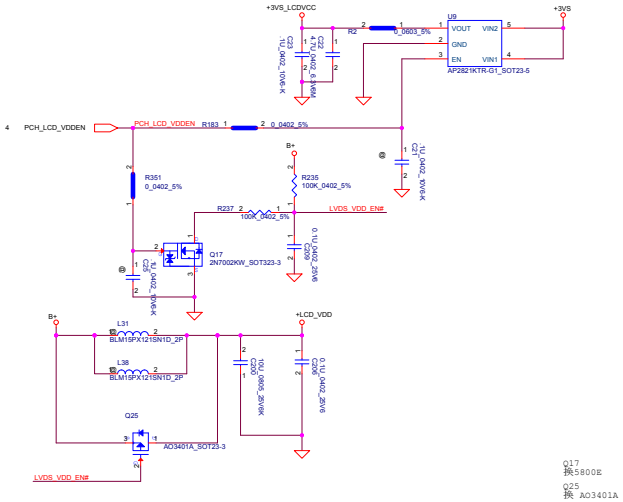
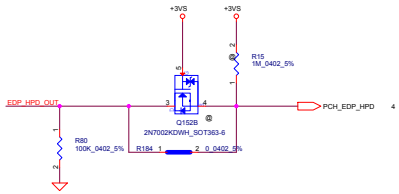
LCD PWR



Q17 換5800E

Q25 換 AO3401A

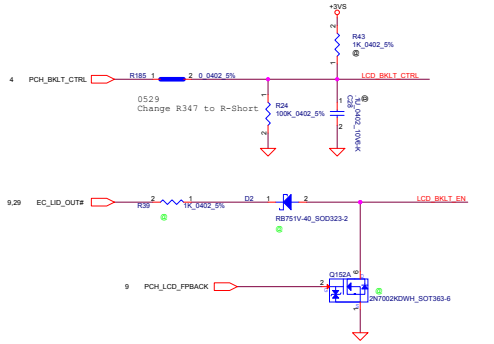
Hot-Plug



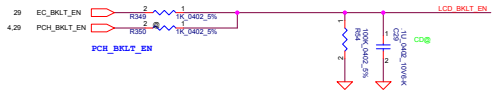
EDP_HPD

*EDP EN,EDP-HPD EN
EDP EN, EDP-HPD Disabled, 10K PU Via VCCIO
EDP Disabled, NC

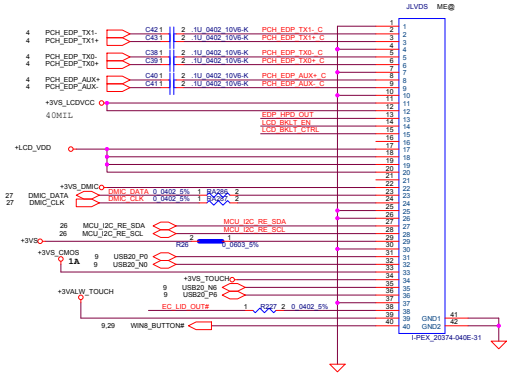
BKLT CNTL



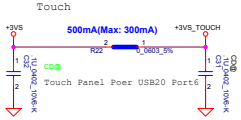
LCD背光控制，LID控制以及PCH的热键控制都NC，直接由EC来做背光控制.

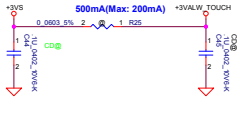


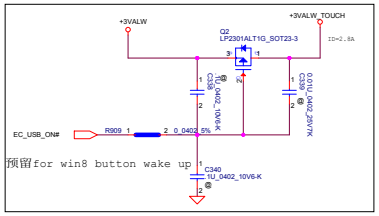
For LCD CONN YOGA3_11"

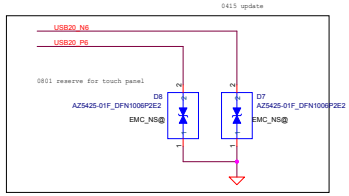


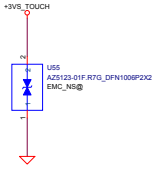
Touch

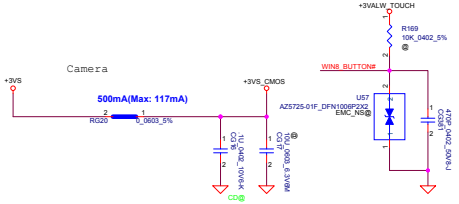


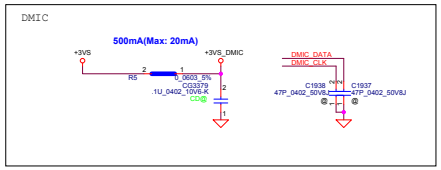












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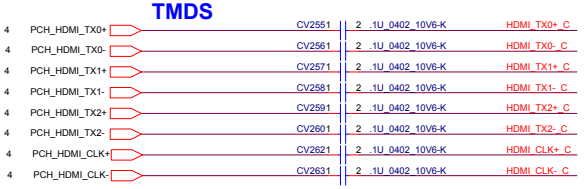
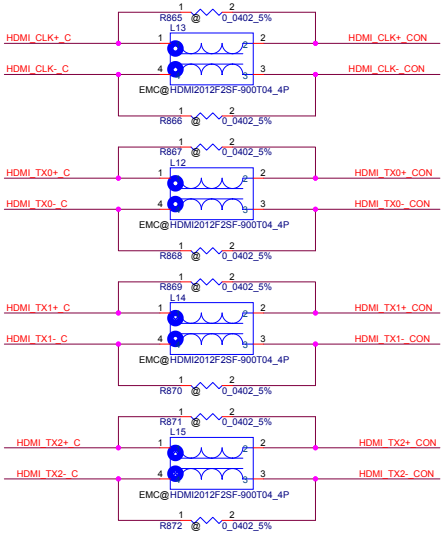
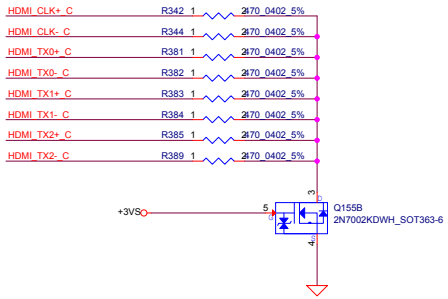
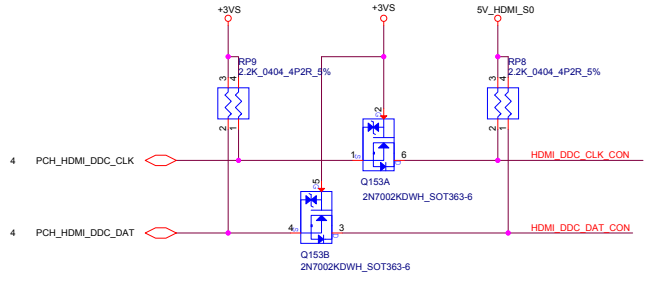
TMDS



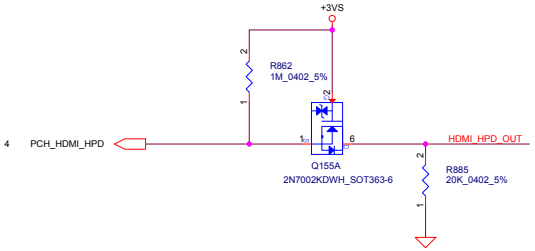




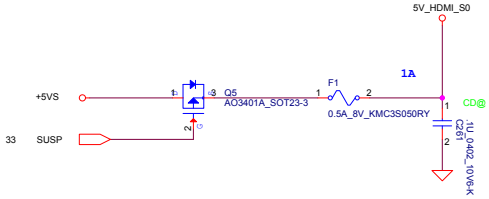
DDC



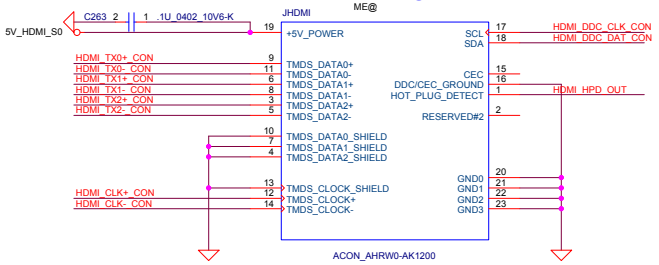
H-PLUG



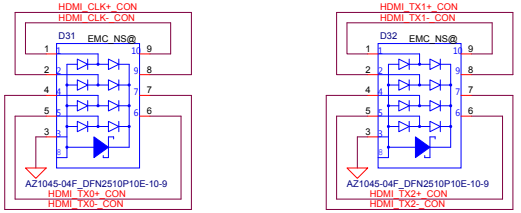
CONN

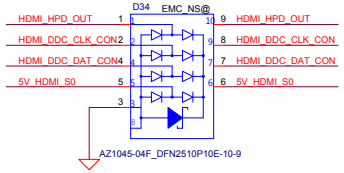


MINI HDMI CONN



ESD





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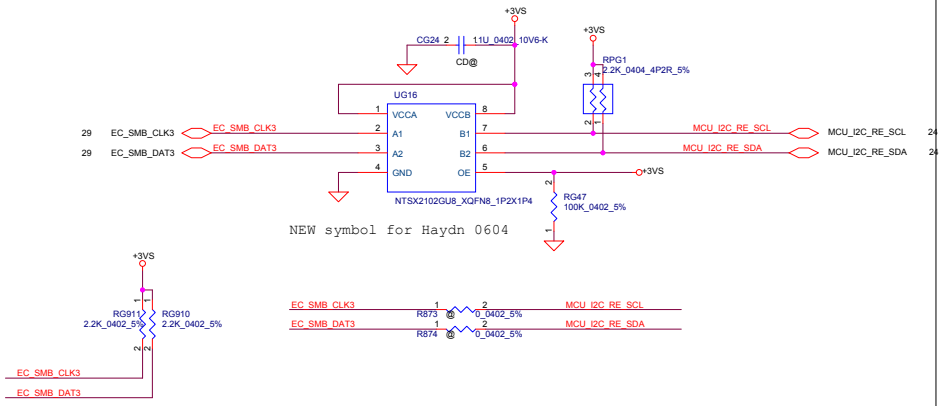
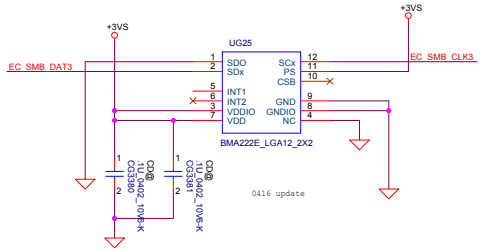


G-SENSOR



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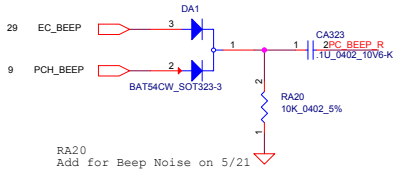
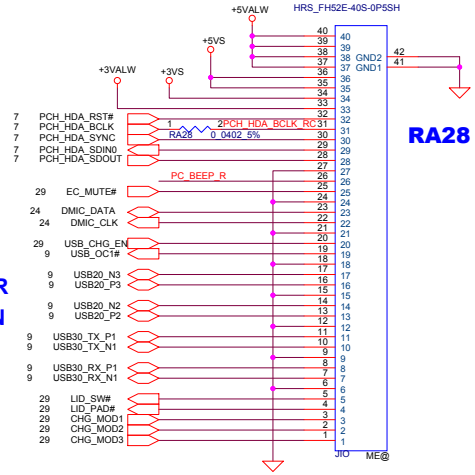
JIO HDA CARDREADER USB CONN

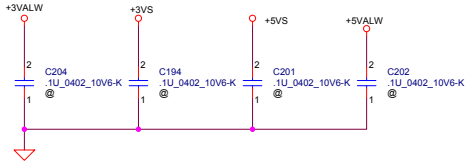


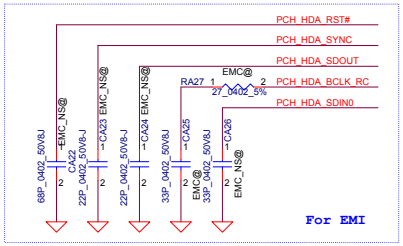
RA20
Add for Beep Noise on 5/21

CARD READER
Left USB_CONN



RA28 Close to JIO





NEW symbol for Haydn 0609

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Title

Cardreader

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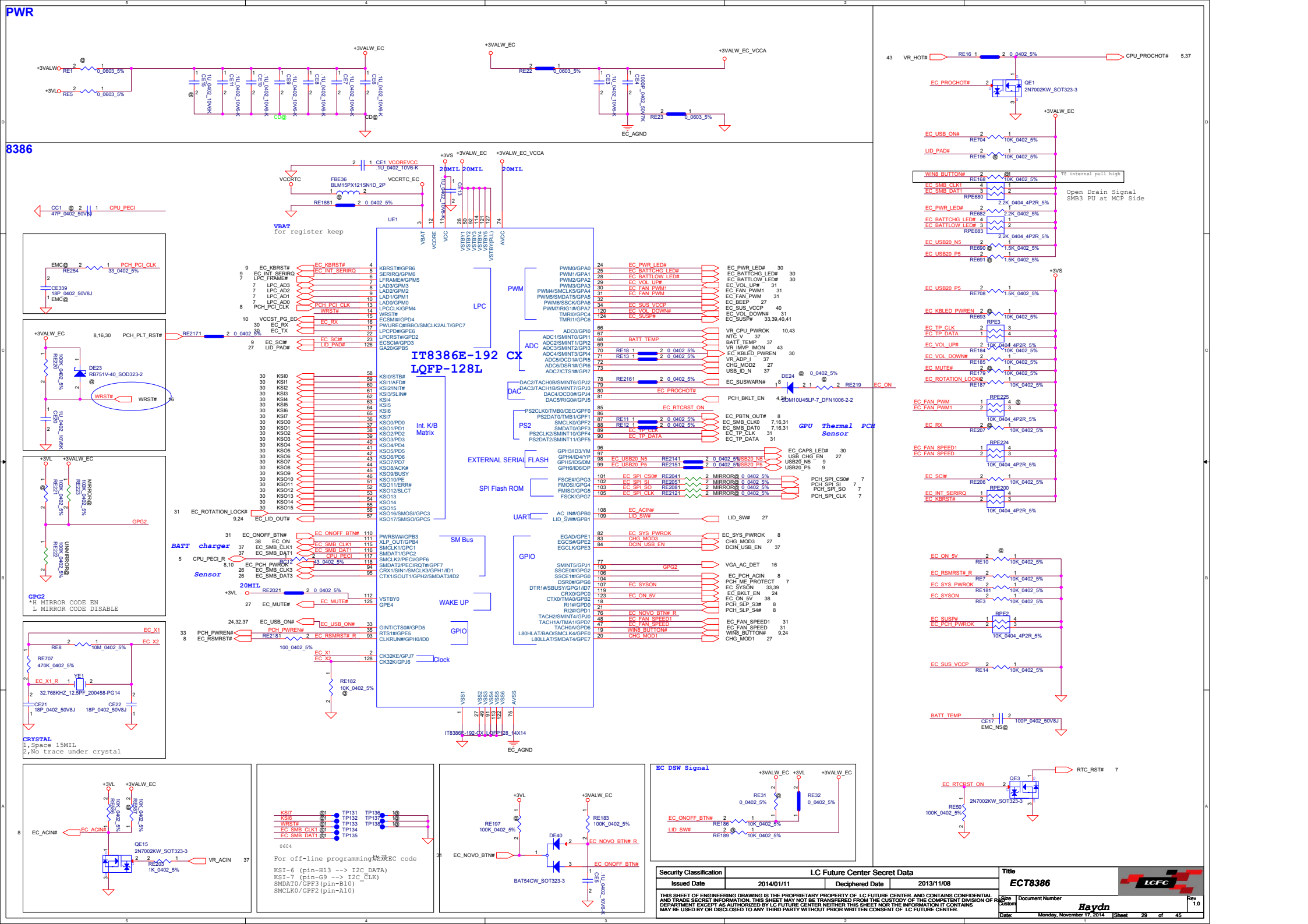
PWR
8386
IT8386E-192 CX
LQFP-128L
LPC
PWM
ADC
DAC
PS2
Int. K/B Matrix
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
GPIO
SM Bus
WAKE UP
Clock
GPU Thermal PCH Sensor
BATT charger
Sensor
CRYSTAL
1,Space 15MIL
2,No trace under crystal
GPG2
*H MIRROR CODE EN
L MIRROR CODE DISABLE
EC DSW Signal
Open Drain Signal
SMB3 PU at MCP Side
For off-line programming烧录EC code
KSI-6 (pin-H13 --> I2C_DATA)
KSI-7 (pin-G9 --> I2C_CLK)
SMDAT0/GPF3(pin-B10)
SMCLK0/GPF2(pin-A10)
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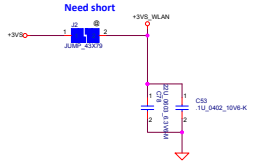
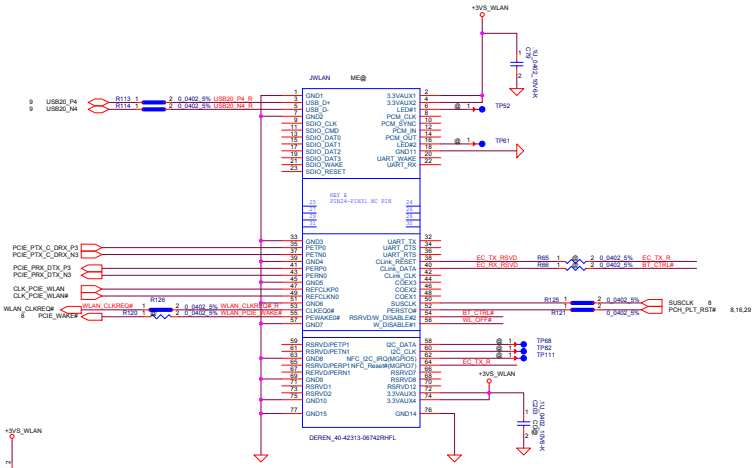
WIFI&BT Board Connector

Mini Card(WLAN/WiMAX)

Need short



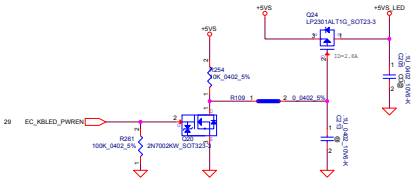


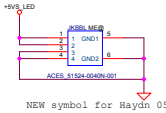
NEW symbol for Haydn 0609

WLAN&BT Combo module circuits

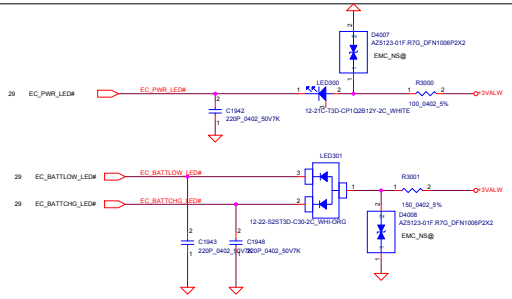
	BT on module Enable	BT on module Disable
* BT_CRTL	H	L
PCH_BT_ON#	L	H

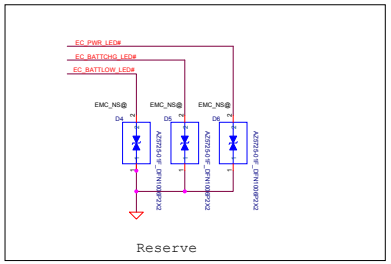
KB BL





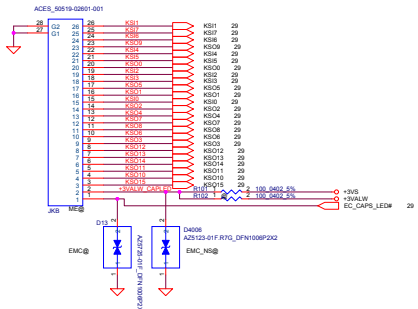
NEW symbol for Haydn 0530





Reserve

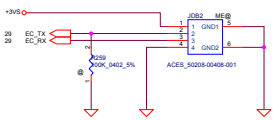
Keyboard Connector



+3VALW_CAPLED	C117	1	2 EMC_NS@ 100P_0402_50V8J	EC_CAPS_LED#	C133	1	2 EMC_NS@ 100P_0402_50V8J				
KSO2	C89	1	2 EMC_NS@ 100P_0402_50V8J	KSO1	C90	1	2 EMC_NS@ 100P_0402_50V8J				
KSO15	C92	1	2 EMC_NS@ 100P_0402_50V8J	KSO7	C93	1	2 EMC_NS@ 100P_0402_50V8J				
KSO6	C94	1	2 EMC_NS@ 100P_0402_50V8J	KSI2	C95	1	2 EMC_NS@ 100P_0402_50V8J				
KSO8	C96	1	2 EMC_NS@ 100P_0402_50V8J	KSO5	C97	1	2 EMC_NS@ 100P_0402_50V8J				
KSO13	C98	1	2 EMC_NS@ 100P_0402_50V8J	KSI3	C99	1	2 EMC_NS@ 100P_0402_50V8J				
KSO12	C100	1	2 EMC_NS@ 100P_0402_50V8J	KSO14	C109	1	2 EMC_NS@ 100P_0402_50V8J				
KSO11	C119	1	2 EMC_NS@ 100P_0402_50V8J	KSI7	C110	1	2 EMC_NS@ 100P_0402_50V8J				
KSO10	C107	1	2 EMC_NS@ 100P_0402_50V8J	KSI6	C122	1	2 EMC_NS@ 100P_0402_50V8J				
KSO3	C116	1	2 EMC_NS@ 100P_0402_50V8J	KSI5	C108	1	2 EMC_NS@ 100P_0402_50V8J				
KSO4	C115	1	2 EMC_NS@ 100P_0402_50V8J	KSI4	C123	1	2 EMC_NS@ 100P_0402_50V8J				
KSI0	C121	1	2 EMC_NS@ 100P_0402_50V8J	KSO9	C111	1	2 EMC_NS@ 100P_0402_50V8J				
KSO0	C124	1	2 EMC_NS@ 100P_0402_50V8J	KSI1	C120	1	2 EMC_NS@ 100P_0402_50V8J				

For EMC

UART Debug Connector



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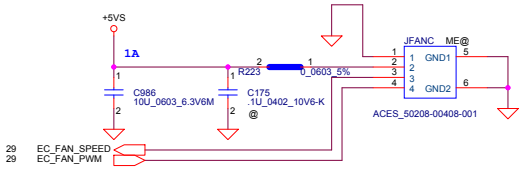
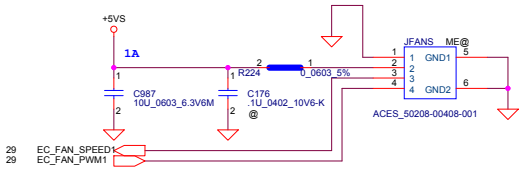
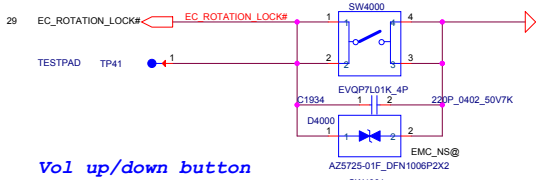
THERMAL SENSOR AND FAN

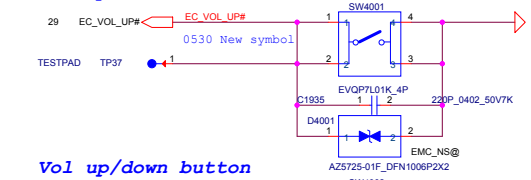




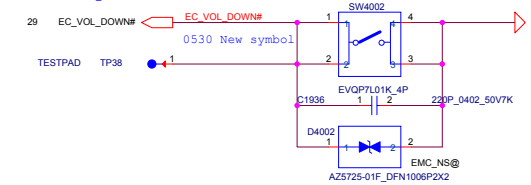
Rotation button



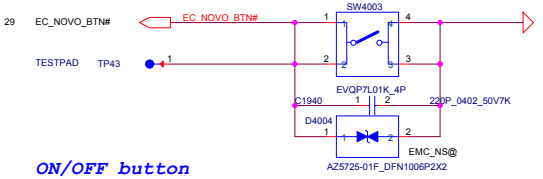
Vol up/down button



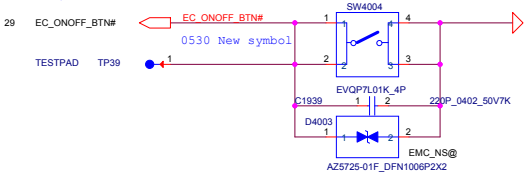
Vol up/down button



NOVO button

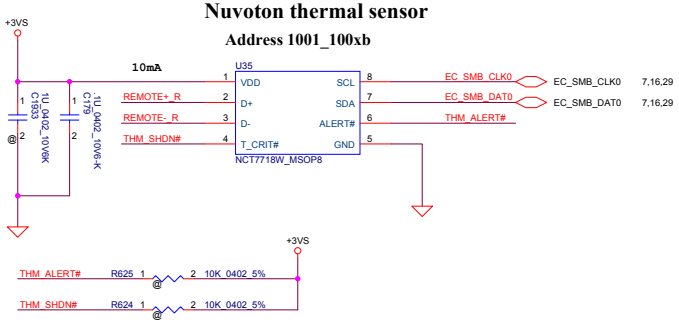


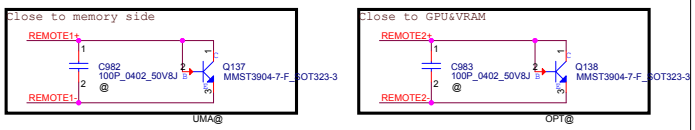
ON/OFF button



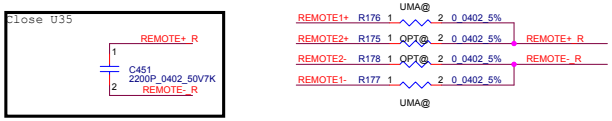
Nuvoton thermal sensor

Address 1001_100xb

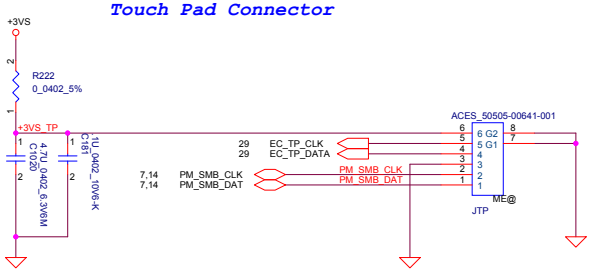


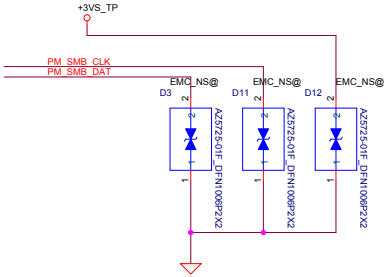


REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"



Touch Pad Connector





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Title	CONN(THM&FAN&RTN&SPI)		
Size C	Document Number Haydn		Rev 1.0
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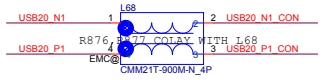
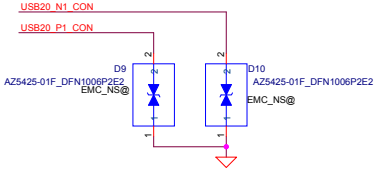
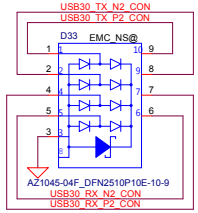
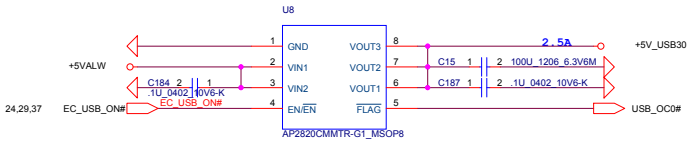
USB30

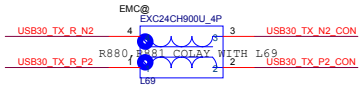


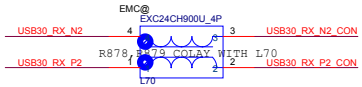




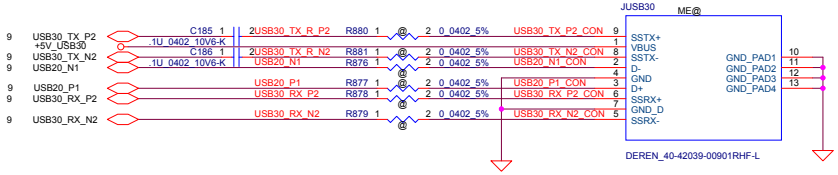


Low Active 2A

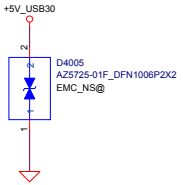




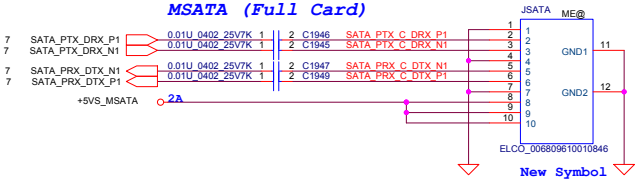
Left USB3.0/2.0



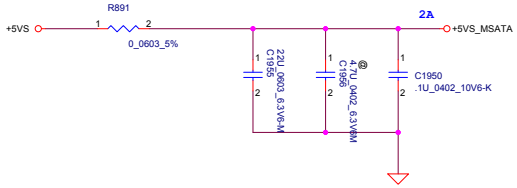
NEW symbol for Haydn 0604



MSATA (Full Card)



New Symbol



Security Classification	LC Future Center Secret Data		
Issued Date	2014/01/11	Deciphered Date	2013/11/08

Title	CONN(MSATA&USB30&USB		
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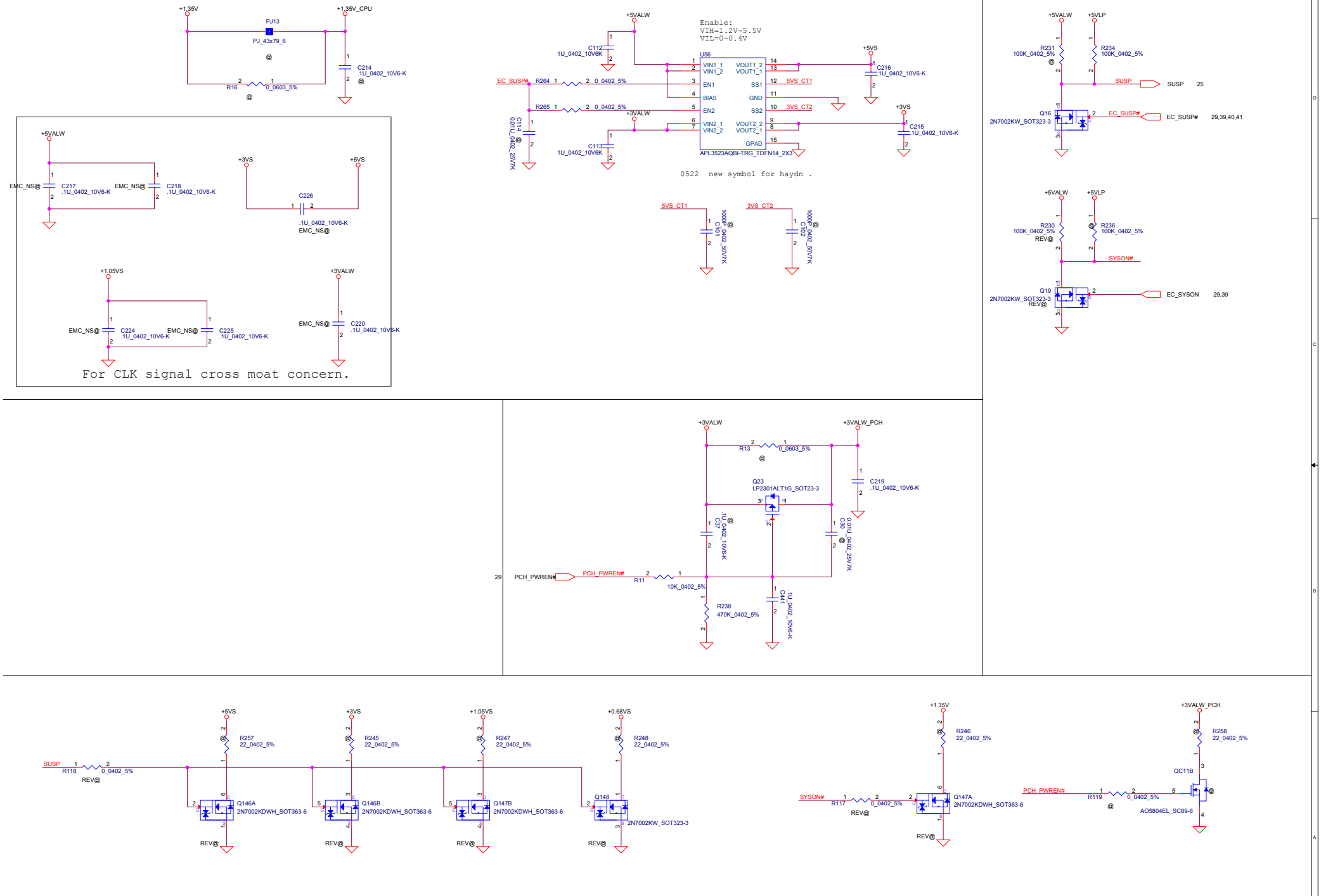

Security Classification	LC Future Center Secret Data		
Issued Date	2014/01/11	Deciphered Date	2013/11/08

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Title: **POWER SWITCH**

Size	Document Number	Rev
C	Haydn	1.0

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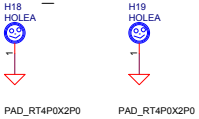
PAD_CT6P0B7P0D3P6

PAD_CT6P0

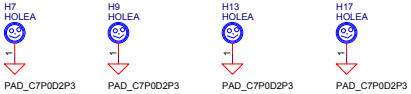
PAD_C7P0D4P3

PAD_RT4P0X2P0

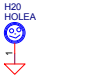


PAD_C7P0D5P6

PAD_C7P0D2P3



PAD_ShapeT6P0X5P5



PAD_O2P7X2P2D2P7X2P2N

PAD_C2P2D2P2N

Security Classification	LC Future Center Secret Data		
Issued Date	2014/01/11	Deciphered Date	2013/11/08

Title: **Screw and Hole**

Size	Document Number	Rev
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4/16:
1.EDP connector change to 40 pin , touch connector change to 10pin .
2.G sensor change to BMA222E
3.Modify DIMM connector pin define

4/24:
1.CV112 change to 0.1uF follow DG.

4/28:
1.unstuff pull up pull down resistor for GPU CMD signal (Single rank no need)
2. Reserve pull down resistor for signal OVERT#
3.reserve pull up resistor for signal MULTI_STRAP_REF0_GND

4/29:
1.use buffer for signal CPU_DRAMPG_CNTL

5/4:
1.Delete N15VGM@ part for Haydn only support N16S-GT.

5/6:
1.VR_ADP_ID change to USB_ID_N
2.EC_ADP_ID_ON# change to DCIN_USB_EN
3.Delete GPU CMD signal pull up/pull down resistor
4.update EC to LQFP package
.

5/8:
1. Change YC1,YE1 to 32.768KHZ_12.5PF_200458-PG14
2. Stuff QV7 for GPU +1.05V power
3.Add one BJT on thermal sensor for GPU&VRAM
4. Change YC1 to 32.768KHZ_12.5PF_202740-PG14

5/9:
1. modify HDMI DATA signal connection .
2. renaming GPU command signal
3.mount RC762, unmount DC27 for cost down .

5/11:
1.Change UE1 to IT8386E-192-CX_LQFP128 for cost down
2.Change YC2 to 24MHZ_6PF_7V24000032 for cost down
3.Change D4,D5,D6,D13 to ESD9N5BL-2-TR_DFN1006-2 for cost down

5/12:
1.Change JWLAN to LCN_DAN05-67146-0102
2.Delete JRTC.
3.Change CC130 to SE00000PL0J for cost down
4.Change D31,D32,D33 to AZ1045-04F for cost down

5/14:
1.Change R105 to 1K ohm.
2.Change CC44 to SGA00009900 for layout placement concern .
3.Change QV8,QV17,QV21 to 2N7002KDWH for layout placement concern .

5/15:
1.Change JFANC ,JFANS to 88231-04001 follow ME connector list .

5/19:
1.Touch Pad change to I2C interface.
2.Haydn support two FAN ,connect the two FAN signal to EC .
3.Delete one debug connector JDB3.
4.delete deep S3 schematic part .
5.Modify KB pin define .

5/20:
1.Move lid_pad# part schematic to USB DB .

5/21:
1.Change D34 to AZ1045-04F_DFN2510P10E-10-9 follow EMC suggestion .
2.Change D7,D8,D9,D10 to AZ5425-01F follow EMC suggestion .
3.Delete SPI rom power control part schematic since not support DS3 now .
4.Touch screen part function use the same connector with EDP .

5/22:
1.Use cost down solution for signal CPU_DRAMPG_CNTL follow G .
2.Change U56 to APL3523AQBI-TRG for cost down.
3.Change JKB to ACES_50506-0260M-001 follow ME connector list .

5/26:
1.Change DV5,DV6 to BAT54AW_SOT323-3 for cost down.
2. Reserve JRTC
3. modify JLVDS pin define .
4.Delete reserved components QV24,QV25 ,DV5 for signal VGA_PWRGD

5/27:
1.Reserve CC110 for signal +1.05VS_DCPSUS4
2.Change JKB to ACES_50519-02601-001 follow ME connector list .
3. Change JTP to ACES_50509-0060N-001 follow ME connector list .
4. Delete WLAN AOAC part schematic .
5. Swap VRAM data group 2 ,group3 and Swap VRAM data group 6 ,group7 for layout routing concern .

5/28:
1.Reserve USB3.0 signal that connected to JIO.
2.Reserve R873,R874 for the possibility to cost down I2C redriver.
3.Change QV10,QV13 to 2N7002KDWH for layout placement concern .
4.Swap VRAM data group 4 ,group6 for layout routing concern .
5.Change RPC10 to RPC10 and RPC21 for layout concern.

5/29:
1.Reserve RV39 ,RV171 follow NVIDIA suggestion.
2.Modify JIO pin define ,add USB charger mode control signal .

0603:
1.Change JFANC ,JFANS to ACES_50208-00408-001 follow ME connector list .
2.Delete PCIE_WAKE#,PCH_ACIN...reserved pull up signal +3VL for layout concern.
3.Delete QV13 ,Change QV12,QV19 to 2N7002KDWH_SOT363-6 for layout concern.

0604:
1.Change JUSB30 to C-K_26211-8B19-02 follow ME connector list .
2.Change UG16 to NTSX2T02GU8_XQFN8 for cost down.
3.Delete reserved component CC44 for layout concern.
4.update hole symbol.

0606:
1.Change HDMI part 0.1uF cap to 0402 size Follow DG.
2.Add reserved Caps for keyboard signal follow EMC suggestion.
3.Add reserved Caps for HDA signal follow EMC suggestion

0607:
1.Combine EC part resistor for bom quantity concern.

6/9:
1.Change JHDMI to AHRW0-AK1200 follow ME connector list .
2. Change JTP to 50505-00641-001 follow ME connector list .
3.Change JIO to ACES_51540-04041-001 follow ME connector list .
4. Change JWLAN to LOTES_APCI0062-P007A follow ME connector list .

6/10:
1.Modify JLVDS pin define.
2. Add signal ILIM_SEL for USB charger.

6/12:
1.Change LV2 to PBY100505T-300Y-N ,LV1 to PBY100505T-181Y-N For smaller size.
2.Reserve RTC_RST# schematic controlled by EC.
3.Modify EC pin define(Four signals.)

6/16:
1.Change button switch SW4000,SW4001,SW4002,SW4003,SW4004 to EVQP7L01K_4P.

6/17:
1.Change QV5, QC13, QC12, QV10 to AO5804EL SC89-6 for layout concern.
2.Change CV22,CC121,CC130,CC131, CV103, CV104, CV105 to SE00000M00J for layout concern.

6/18:
1.Modify GPU power on sequence .
2.Change CV111 to SE00000M00J ,CV60 to SE107475K0J for layout concern.
3.Add thermal protection schematic .
4.Change QC11,Q149 to SB00000XP0J for layout concern.

6/19:
1.Delete thermal protection schematic dummy components since no space to placement .

6/20:
1.Add C217,C218,C220,C224,C225,C226 For CLK signal cross moat concern .
2.Delete JCMOS1 ,add test point for signal RTC_RST#

SIV

7/21:
1.Delete CG380 For CG380/CG381 function repetition
2.Delete RV70,RV61 +1.35VGS/+1.05VGS Mosfet control signals power level change
3.Change CV54 from 0.1uf to 0.01uf, RV228 from 560ohm to 0ohm, CV506 from 0.1uf to 0.22uf for GPU power sequence change
4.Change touch pad to SMBUS solution.

7/29:
1.Delete QC5 (not connect to PCH)
2.Change RE218 from 0ohm to 100ohm for EC_RSMRST# overshot/undershot fail
3.Add CC50 0.01uf for VCCST_PG_EC_R undershot fail
4.Change RC61 from 0ohm to 100ohm for SYS_PWROK overshot/undershot fail
5.Change CC23,CC24 to 2.7pF ,CV19,CV20 to 12pF follow crystal vendor suggestion.
6.Change RE707 to 470K ,CC7 to 15pF follow crystal vendor suggestion.

08/05:
1.modfiy EC GPIO (EC_ON)

08/07:
1.JLVDS rotate 180 degree

08/11:
1.Change 0 ohm resistor(RC65,R184,RE188,R351,RC761,RD16,RD22, RE32, RC97, R110, R125,R121,R126
RC138,RE202,RE217,RC31,R109,R113,R114,RC758,RC759,RC105, RC103,RC99) to jump
2. NO stuff CE6 ,CD88

08/11:
1.Mount RA27 ,CA25 Follow EMC suggestion.
2. Change JIO to HRS_FH52E-40S-0P5SH follow ME suggestion.
3.Change JSATA to ELCO_006809610010846 follow ME suggestion.

SIT

9/23:
1.Change JLVDS to I-PEX_20374-040E-31 follow ME suggestion.
2.Change some power plane from +3VALW to +3VALW_PCH.
3.Mount D13 follow emc suggestion.

9/24:
1.Reserve CC31 and CC32 For EMC.

9/25:
1.Mount RE254 ,CE339 For EMC.
2.Change RE22 , RE23 ,RC62 ,RC81 ,RC85 ,R909 ,R223,R224 to R short.
3.Change L69,L70 to EXC24CH900U for cost down

10/13:
1.Change CC23,CC24 to 3.3pF for RTC Time test fail in windows.

11/11:
1.Change CE339 to 18pF for HSW platform LPC CLK fall slew rate test fail issue.

11/13:
1.Change R2,R22,R5,R13,RG20,R26,RC107,RC122,RC124,RE214,RE215,RE216 to R short for cost down.
2. Mount RE50,QE3,Q23,R11,R238,C441 for clear CMOS.
3.Change JWLAN to DEREN_40-42313-06742RHFL follow ME request.
4.Change JUSB30 to DEREN_40-42039-00901RHF-L Follow ME request.

Title			
HW_Change_List			
Size: C	Document Number: Yoga3-BDW		Rev: 1.0
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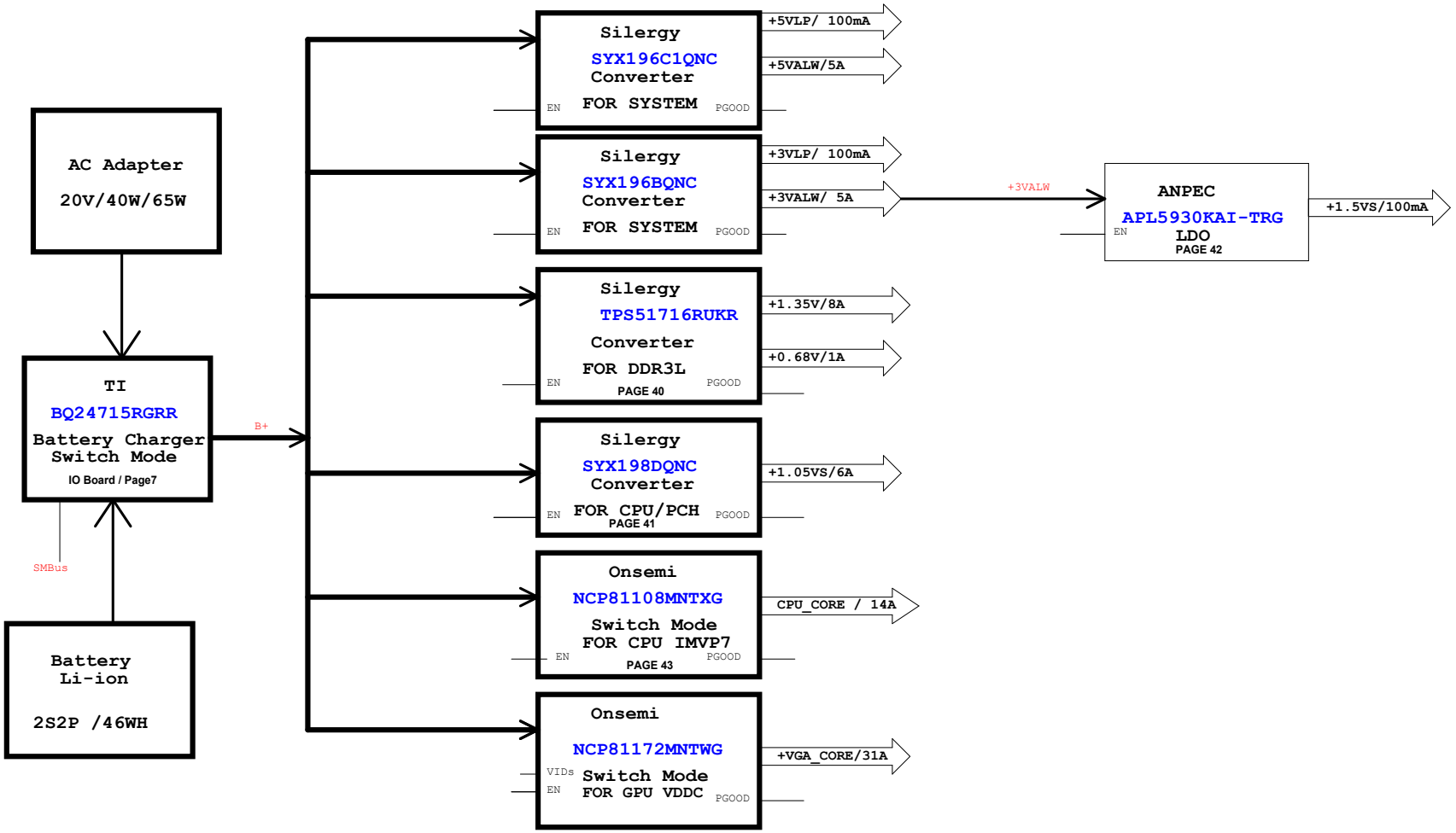

Security Classification	LC Future Center Secret Data		
Issued Date	2014/01/11	Deciphered Date	2013/11/08

Title: PWR_BLOCK DIAGRAM

Size: C	Document Number: Yoga3-BDW	Rev: 1.0
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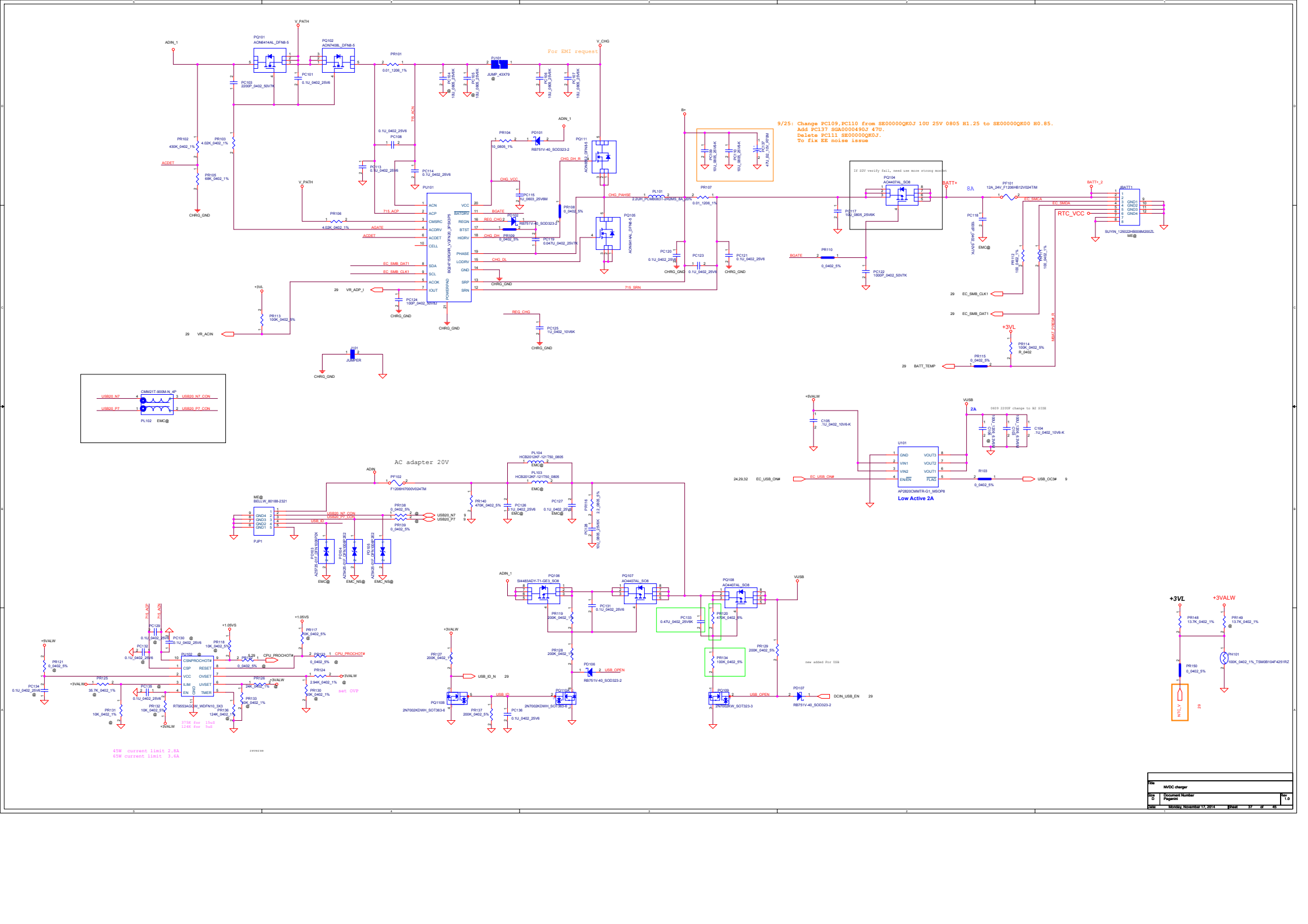
V_PATH
ADIN_1
PQ101
AON6414AL_DFN8-5
PQ102
AON7408L_DFN8-5
PR101
0.01_1206_1%
V_CHG
For EMI request
PJ101
JUMP_43X79
PC103
2200P_0402_50V7K
PC101
0.1U_0402_25V6
PC104
10U_0805_25V6K
PC105
10U_0805_25V6K
PC106
10U_0805_25V6K
PC107
10U_0805_25V6K
PR102
430K_0402_1%
PR103
4.02K_0402_1%
ACDET
PR105
68K_0402_1%
CHRG_GND
PC108
0.1U_0402_25V6
715_ACN
PC113
0.1U_0402_25V6
PC114
0.1U_0402_25V6
PR104
10_0805_1%
PD101
RB751V-40_SOD323-2
PQ111
AON6411_DFN8-5
CHG_DH_R
CHG_VCC
PC115
1U_0603_25V6M
PR106
4.02K_0402_1%
AGATE
PU101
BQ24779RGRR_VQFN28_3P5X3P5
ACN
ACP
CMSRC
ACDRV
ACDET
CELL
PHASE
LODRV
GND
SRP
SRN
VCC
BATDRV
REGN
BTST
HIDRV
BGATE
REG_CHG2
CHG_DH_PR109
CHG_DL
EC_SMB_DAT1
EC_SMB_CLK1
ACOK
IOUT
PCWB5FAD
PD102
RB751V-40_SOD323-2
PR109
0_0402_5%
PC119
0.047U_0402_25V7K
PR108
0_0402_5%
PQ105
AON6414AL_DFN8-5
PL101
2.2UH_PCMB063T-2R2MS_8A_20%
PR107
0.01_1206_1%
PC120
0.1U_0402_25V6
PC123
0.1U_0402_25V6
PC121
0.1U_0402_25V6
CHRG_GND
715_ACP
715_SRN
PC124
100P_0402_50V8J
PC125
1U_0402_10V6K
REG_CHG
J101
JUMPER
+3VL
PR113
100K_0402_5%
29 VR_ADP_I
29 VR_ACIN
B+
9/25: Change PC109,PC110 from SE00000QK0J 10U 25V 0805 H1.25 to SE00000QK00 H0.85.
Add PC137 SGA0000490J 47U.
Delete PC111 SE00000QK0J.
To fix EE noise issue
PC109
10U_0805_25V6K
PC110
10U_0805_25V6K
PC137
47U_6X_10V_M
If SDV verify fail, need use more strong mosfet
PQ104
AO4407AL_SO8
BATT+
8A
PF101
12A_24V_F1206HB12V024T/M
BATT+_2
JBATT1
SUYIN_125023HB008M200ZL
ME@
EC_SMCA
EC_SMDA
RTC_VCC
PC117
10U_0805_25V6K
PC118
1000P_0402_50V7K
EMC@
PR110
0_0402_5%
PC122
1000P_0402_50V7K
PR113
100K_0402_1%
PR114
100K_0402_5%
R_0402
PR115
0_0402_5%
29 BATT_TEMP
29 EC_SMB_CLK1
29 EC_SMB_DAT1
+3VL
AGATE_PR108_R
CMM21T-900M-N_4P
USB20_N7
USB20_P7
USB20_N7_CON
USB20_P7_CON
PL102
EMC@
AC adapter 20V
ADIN
PF102
F1206H07000V024TM
PL104
HCB2012KF-121T50_0805
PL103
HCB2012KF-121T50_0805
EMC@
PR140
470K_0402_5%
PC126
0.1U_0402_25V6
EMC@
PC127
0.1U_0402_25V6
EMC@
PR116
2.2_0805_5%
PC128
10U_0805_25V6K
ME@
BELLW_80188-2321
PJP1
USB_ID
PR138
0_0402_5%
PR139
0_0402_5%
USB20_N7
USB20_P7
PD103
AZ5125-01F_DFN1006F-2
PD104
AZ5125-01F_DFN1006F-2
PD105
AZ5125-01F_DFN1006F-2
EMC@
EMC_NS@
EMC_NS@
+5VALW
C105
1U_0402_10V6-K
VUSB
2A
0609 2200F change to R2 SIZE
PR142
0.05_1206_1%
PR143
0.05_1206_1%
C104
1U_0402_10V6-K
U101
AP2820CMMTR-G1_MSOP8
GND
VIN1
VIN2
EN
VOUT3
VOUT2
VOUT1
FLAG
24,29,32 EC_USB_ON#
EC_USB_ON#
R103
0_0402_5%
USB_OC3#
9
Low Active 2A
PQ106
SI4463ADY-T1-GE3_SO8
PQ107
AO4407AL_SO8
PQ108
AO4407AL_SO8
PC131
0.1U_0402_25V6
PC133
0.47U_0402_25V6K
PR119
200K_0402_1%
PR120
470K_0402_5%
PR128
200K_0402_1%
PR129
200K_0402_5%
PR134
100K_0402_5%
new added For USB
PD106
RB751V-40_SOD323-2
USB_OPEN
PD107
RB751V-40_SOD323-2
DCIN_USB_EN
29
PQ109
2N7002KDW_SOT323-3
PQ110A
2N7002KDWH_SOT363-6
PQ110B
2N7002KDWH_SOT363-6
PR127
200K_0402_1%
PR137
200K_0402_5%
PC136
0.1U_0402_25V6
USB_ID_N
29
+3VALW
+1.05VS
PC129
0.1U_0402_25V6
715_ACP
715_ACN
PC132
0.1U_0402_25V6
PC130
0.1U_0402_25V6
PU102
RT9553AGQW_WDFN10_3X3
CSNPROCHOT#
CSP
VCC
ILIM
EN
RESET#
OVSET
UVSET
TIMER
GND
PR118
10K_0402_5%
PR117
10K_0402_5%
PR122
0_0402_5%
CPU_PROCHOT#
PR121
0_0402_5%
PR125
35.7K_0402_1%
PR126
24K_0402_1%
PR131
10K_0402_1%
PR132
10K_0402_1%
PR133
10K_0402_1%
PR135
0.1U_0402_25V6
PR136
124K_0402_1%
PR124
2.94K_0402_1%
PR130
10K_0402_1%
set OVP
PC134
0.1U_0402_25V6
975K for 15uS
124K for 5uS
45W current limit 2.8A
65W current limit 3.6A
reverse
+3VL
+3VALW
PR148
13.7K_0402_1%
PR149
13.7K_0402_1%
PH101
100K_0402_1%_TSM0B104F4251R2
PR150
0_0402_5%
NTC_V
29
Title
NVDC charger
Size
D
Document Number
Pegamx
Rev
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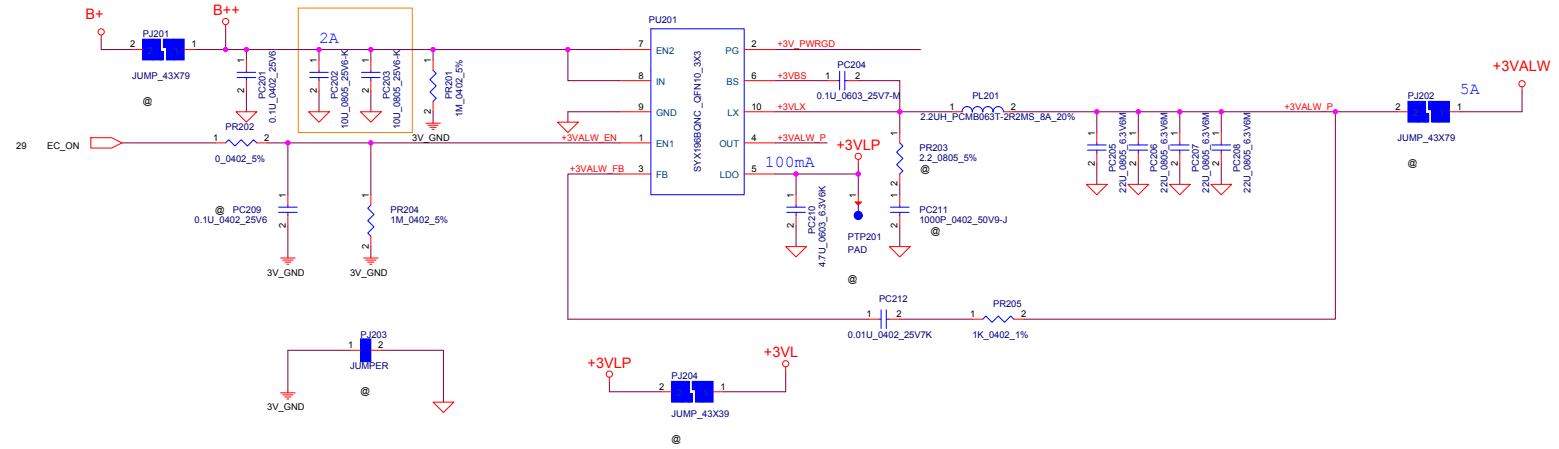
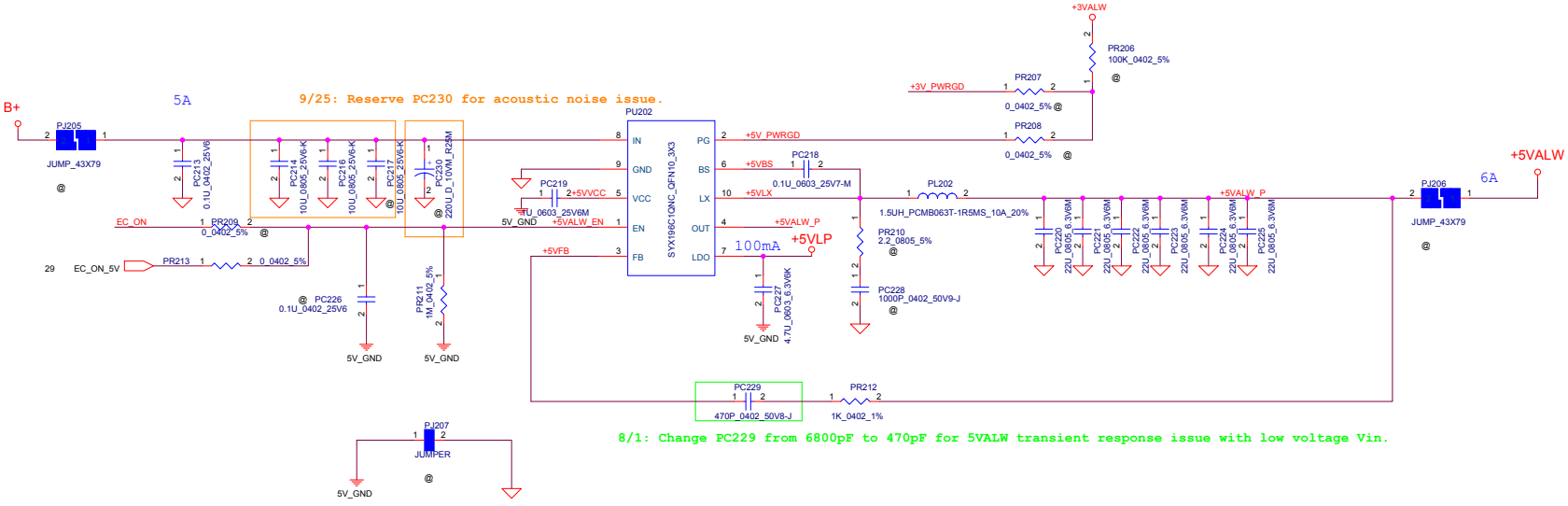
9/25: Change PC202,PC203,PC214,PC216 from SE00000QK0J 10U 25V 0805 H1.25 to SE00000QK00 H0.85.
Reserve PC230 SGA00007I00 220U.
To fix EE noise issue.



9/25: Reserve PC230 for acoustic noise issue.



8/1: Change PC229 from 6800pF to 470pF for 5VALW transient response issue with low voltage Vin.

3VALWP	5VALWP
VFB=2V TDC 5A Fsw=350KHZ OCP:7.8A~9.5A	TDC 5A Fsw=300KHZ OCP:7.8A~9.5A

Security Classification	LC Future Center Secret Data		
Issued Date	2014/02/20	Deciphered Date	2014/02/20

Title	3VALWP/5VALWP	
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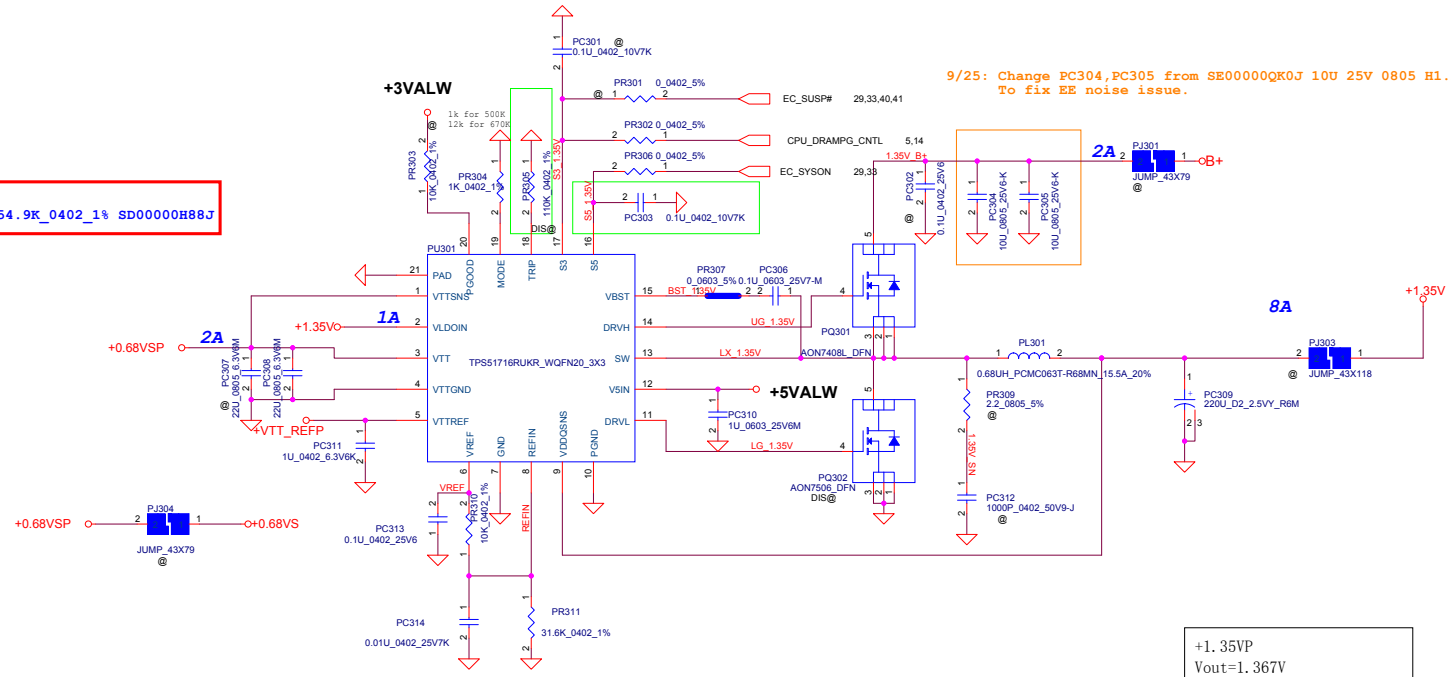
8/1: Follow EE request to stuff PC303 0.1u_0402_10v7k for EC_SYSON overshot/undershot fail

9/25: Change PC304,PC305 from SE00000QK0J 10U 25V 0805 H1.25 to SE00000QK00 H0.85
To fix EE noise issue.

UMA SKU OCP
PR305 change to 54.9K_0402_1% SD00000H88J



+1.35VP
Vout=1.367V
Iocp min=13A fro DIS SKU
Iocp min=6A fro UMA SKU

UMA SKU
PQ302 change to AON7408L for 4A output current

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Issued Date	2014/01/11	Deciphered Date	2013/11/08

Title: PWR_1.35V/0.68VS

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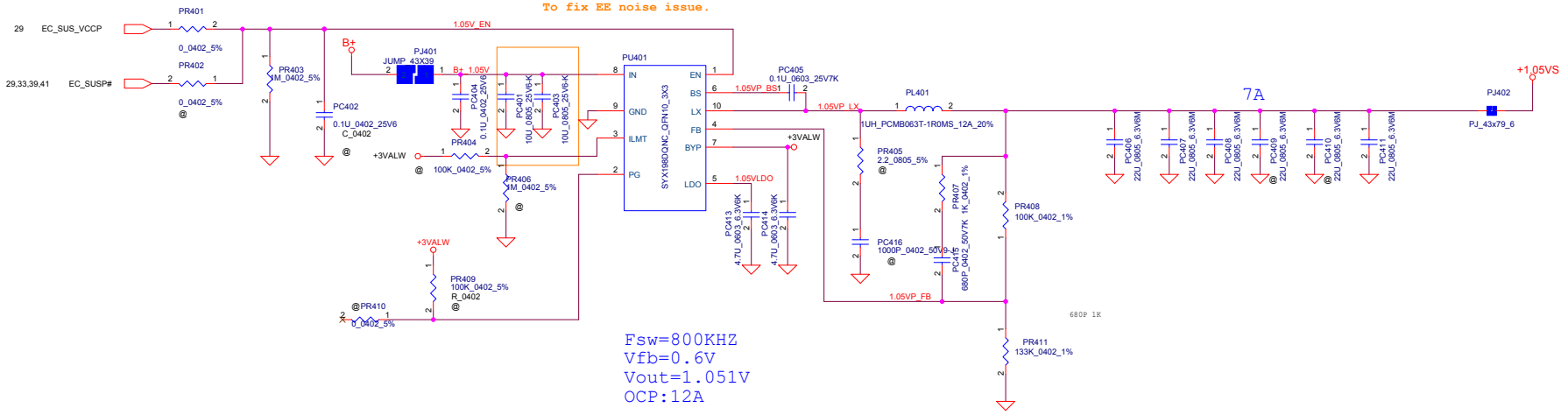
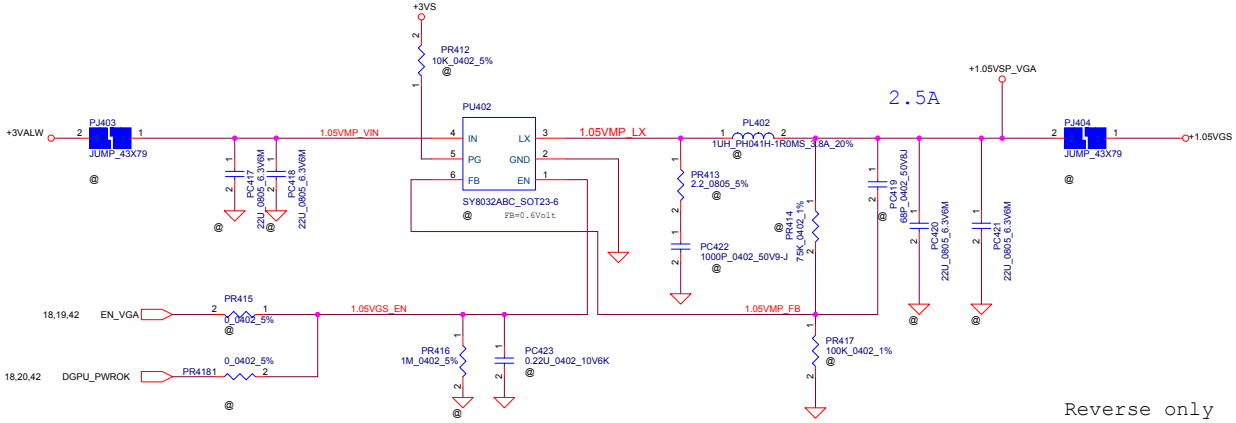
9/25: Change PC401,PC403 from SE00000QK0J 10U 25V 0805 H1.25 to SE00000QK00 H0.85.
Stuff PC401.
To fix EE noise issue.



Fsw=800KHZ
Vfb=0.6V
Vout=1.051V
OCP:12A



Reverse only

Security Classification	LC Future Center Secret Data		
Issued Date	2014/01/11	Deciphered Date	2013/11/08

Title	PWR_1.35V/0.68VS		
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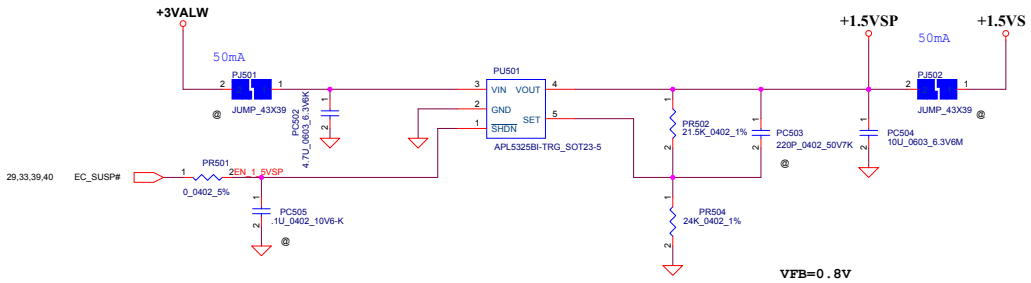

Security Classification	LC Future Center Secret Data		
Issued Date	2014/01/11	Deciphered Date	2013/11/08

Title: PWR_VCCSA

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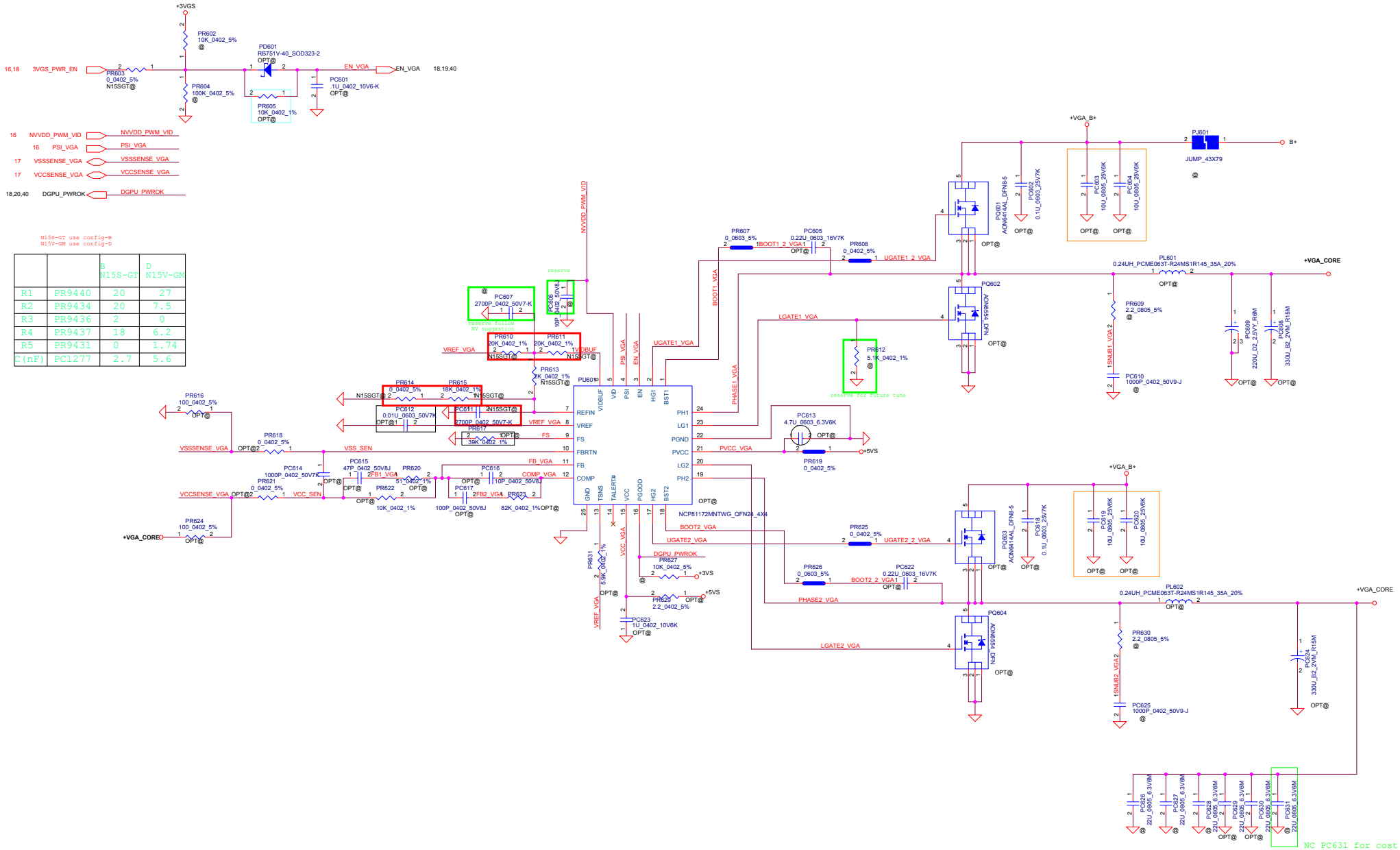

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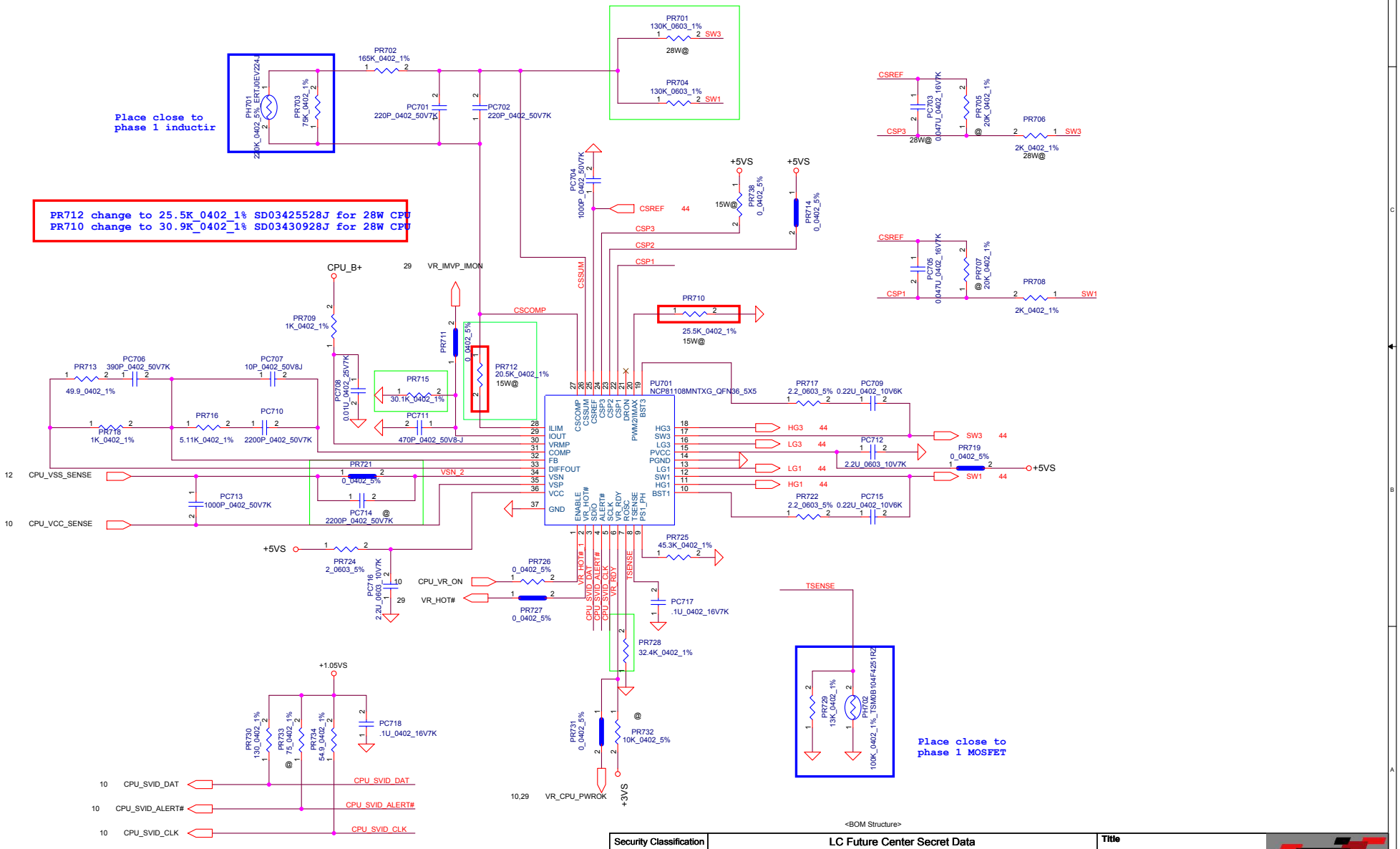

<BOM Structure>

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Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: **CPU_CORE**

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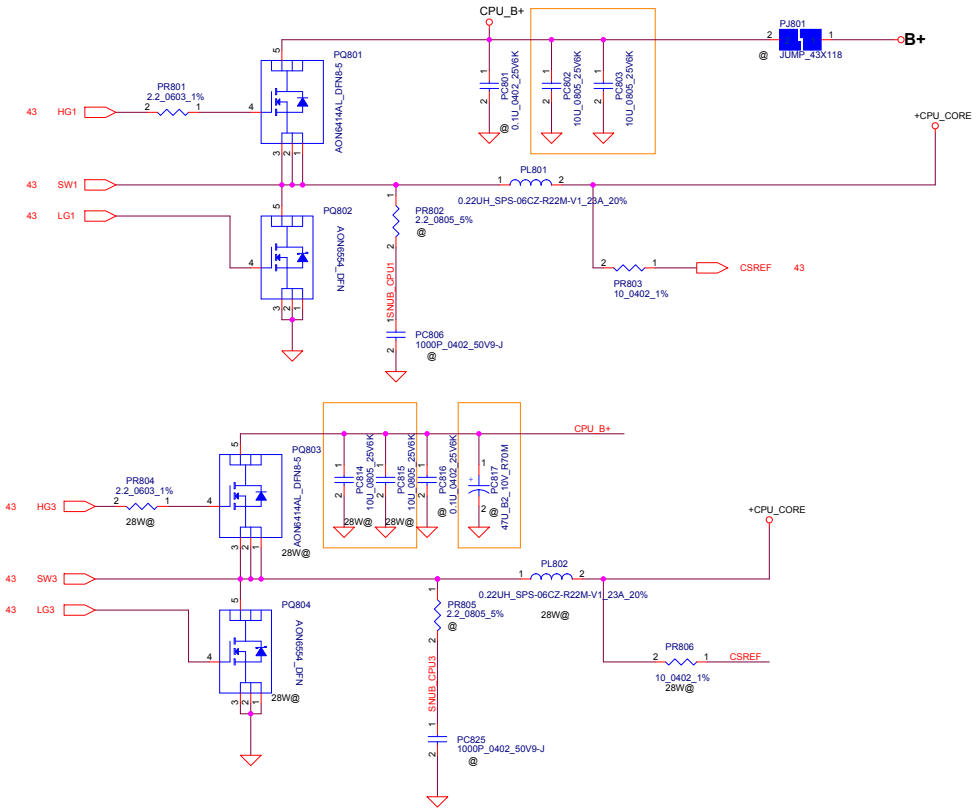

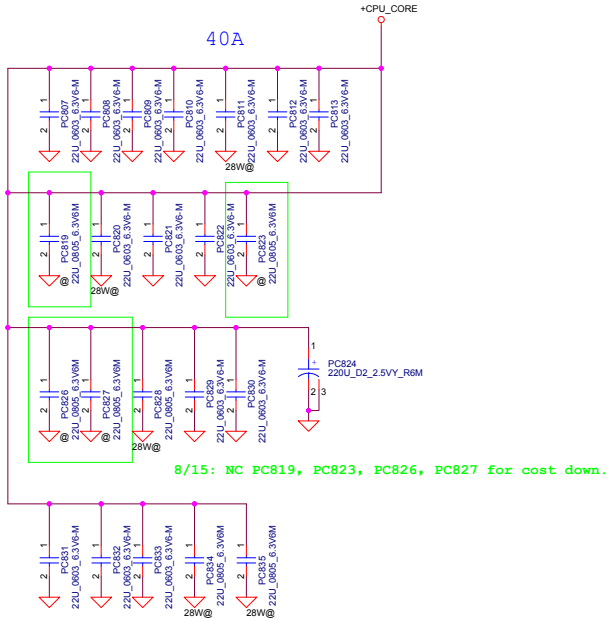

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title

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