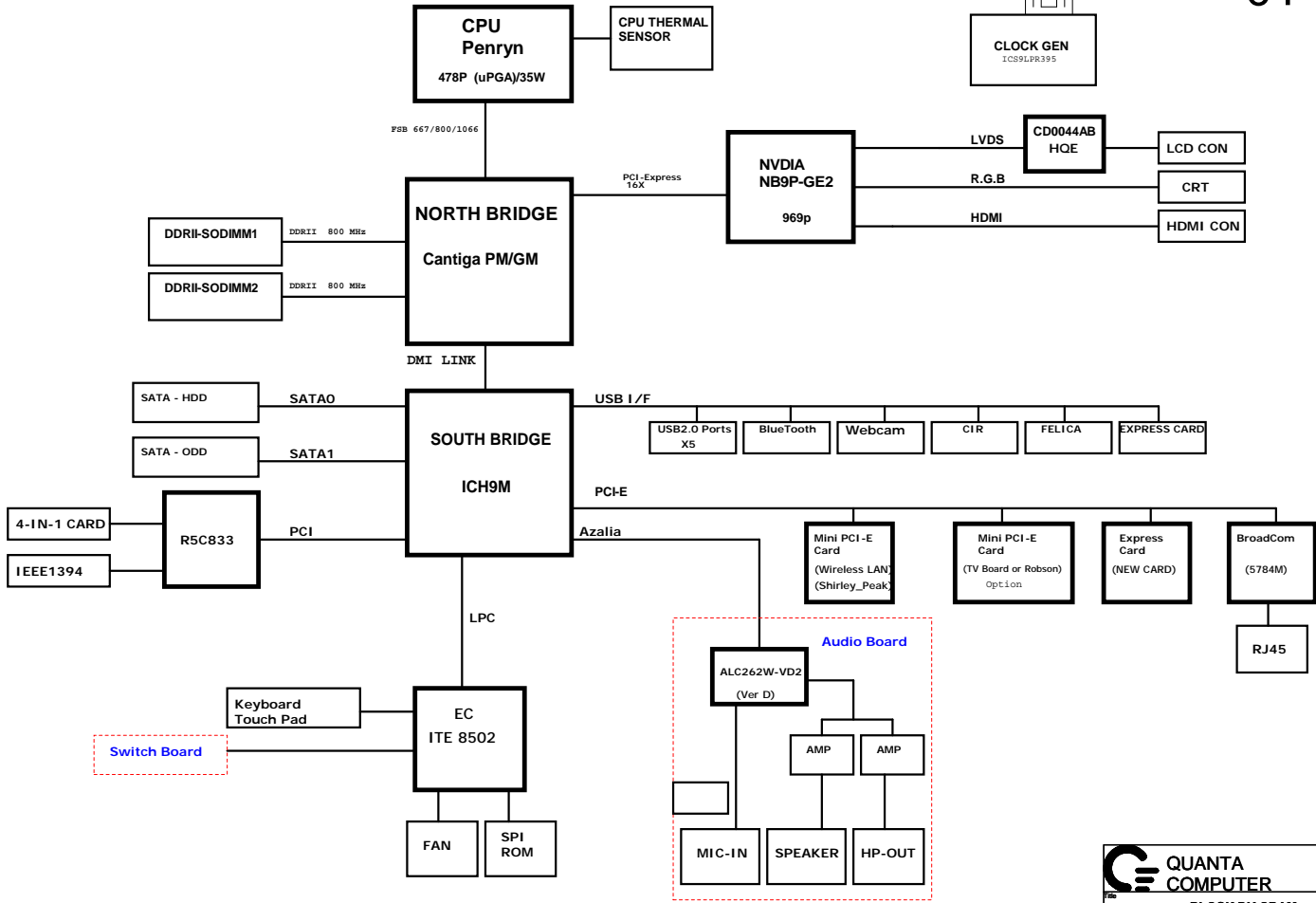


AQ1 BLOCK DIAGRAM

01



QUANTA COMPUTER

BLOCK DIAGRAM

File	Document Number	Rev
	AQ1 MAIN BOARD	1A
Date	Thursday, June 08, 2006	Sheet 1 of 47

AQ1 Power Rails

Power	Voltage	S0	S3	S4	S5	Ctl Signal
15VPCU	15V	V	V	V	V	
5VPCU	5V	V	V	V	V	
3VPCU	3.3V	V	V	V	V	
RVCC3	3.3V	V	V	Note1	Note1	RVCC_ON
VGCS_LAN	3.3V	V	V	Note1	Note1	WOL_EN
5VSUS	5V	V	V			SUSON
3VSUS	3.3V	V	V			SUSON
1.8VSUS	1.8V	V	V			SUSON
VTT_MEM	0.9V	V				MAINON
VCES	5V	V				MAINON
VC33	3.3V	V				MAINON
VC1.8	1.8V	V				MAINON
VC1.5	1.5V	V				MAINON
VC1.2	1.2V	V				MAINON
VC1.1	1.1V	V				MAINON
VGA_CORE	1.009V	V				MAINON
VCCP	1.05V	V				MAINON
VC1.8_DTV	1.8V	V				MAINON
VCC6.0_DTV	6V	V				MAINON
CPU_CORE	By VID	V				VRON

Note1: ON at support WOL function

AQ1 PCI DEVICES IRQ ROUTING

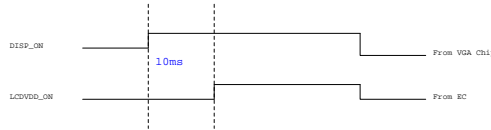
PCI DEVICE	IDSEL#	REQ# / CNT#	Interrupts
R5C833	PCI_AD18	0	A/B

PCB STACK UP
8L

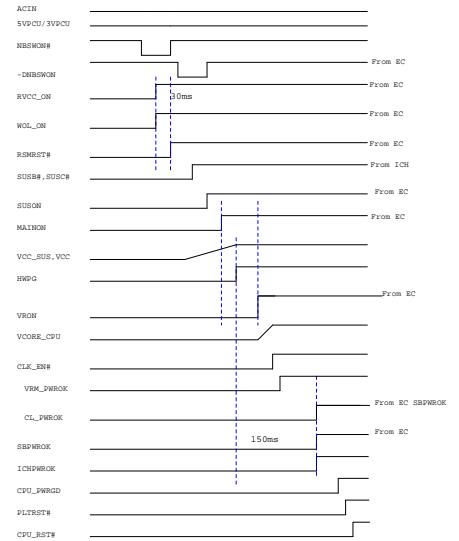
- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : IN3
- LAYER 7 : SGND1
- LAYER 8 : BOT

PAGE LIST

- 01--Block Diagram
- 02--SYSTEM INFORMATION
- 03--CLOCK GENERATOR-IC59LPR395
- 04--CPU HOST BUS (1 of 2)
- 05--CPU POWER (2 of 2)
- 06--GMCH HOST (1 of 5)
- 07--GMCH DDR (2 of 5)
- 08--GMCH DMI VIDEO (3 of 5)
- 09--GMCH Power (4 of 5)
- 10--GMCH Power 2 (5 of 5)
- 11--DDRII SODIMMX2
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- 13--ICH9-M PCI E /SPI(2 of 4)
- 14--ICH9-M GPIO (3 of 4)
- 15--ICH9-M Power (4 of 4)
- 16--ODD/HDD/EXPRESS CARD
- 17--R5C833
- 18--SD_MS_XD SLOT
- 19--CRT/HDMI/LCD
- 20--AUDIO BOARD CONN
- 21-- Mini PCI-E
- 22--Drill HOLE
- 23--INT.KB &TP CONN&LED
- 24--CIR
- 25--USB&FELICA&CAMERA
- 26-- EC ITE8502
- 27--BCM5784M/RJ45
- 28--NV9X (PCIE I/F) 1/5
- 29--NV9X (MEMORY I/F) 2/5
- 30--NV9X (DISPLAY) 3/5
- 31--NV9X (GPIO & STRAPS) 4/5
- 32--NV9X (POWER & GND) 5/5
- 33--NB9X VRAM I
- 34--NB9X VRAM II
- 35--CD0044AB(HQE)
- 36--BLANKING PAGE
- 37--POWER CPU CORE (ISL6266A)
- 38--POWER 3V & 5V & VC1.8_DTV
- 39--POWER 1.8VSUS/VTT_MEM
- 40--POWER VCCP
- 41--POWER VC1.8 (OZ8118LN)
- 42--POWER VGACORE(MAX8792)
- 43--CHARGER(ISL6251)
- 44--Battery connector
- 45--Discharge



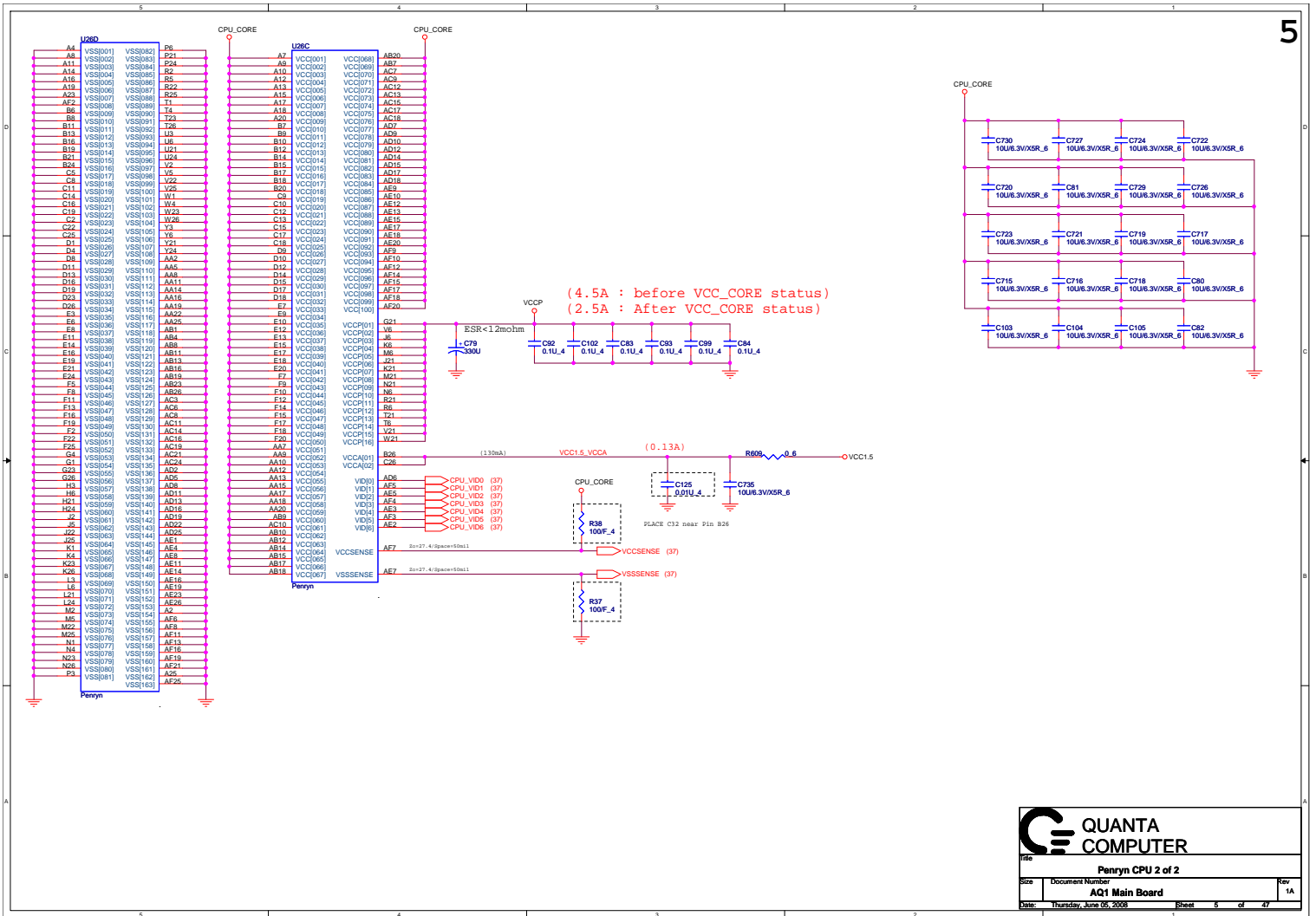
AQ1 Power On Sequence



QUANTA COMPUTER

SYSTEM INFORMATION

Doc. Number	Doc. Name	Rev.
1000000000	AQ1 MAIN BOARD	1.0
Doc. Number: Nov 04, 2008	Doc. Name: Nov 04, 2008	Doc. Rev: 1.0



QUANTA COMPUTER

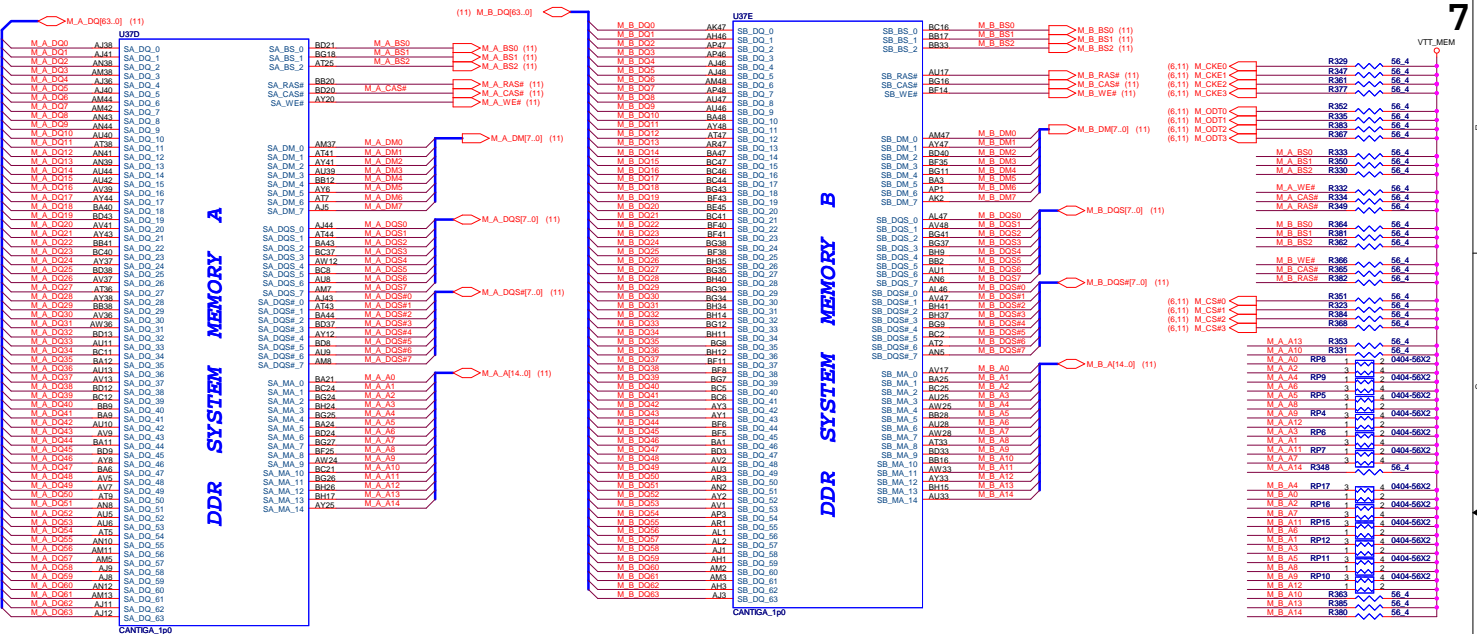
Penryn CPU 2 of 2

Document Number: AQ1 Main Board

Date: Thursday, June 05, 2008

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Rev 1A

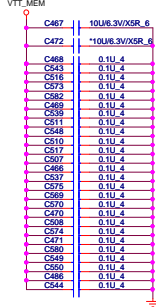
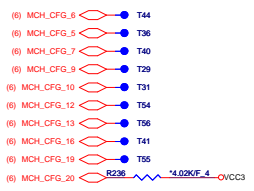


GMCH Strap pin description

CFG#	Low	High
CFG6	ITPM HOST interface enable	ITPM HOST interface disable
CFG7	AMT Firmware will use TLS cipher suite with no confidentiality	AMT Firmware will use TLS cipher suite with confidentiality
CFG9	PCIe Graphics lan: Reverse Lane	PCIe Graphics lan: Normal operation
CFG10	PCIe Loopback enable	PCIe Loopback disable
CFG16	FSS Dynamic ODT Disabled	FSS Dynamic ODT Enabled
CFG19	DMI LANE Normal	DMI LANE Reversed
CFG20	only SDVO/DP/HDMI or PCIe is operational	SDVO/DP/HDMI and PCIe are operation simultaneously via the PEG port

CFG12[11]:XOR / All 7 Clock Un-gating
 00 = Reserve
 01 = XOR mode enabled
 10 = All 7 mode enabled
 * 11 = Normal Operation(Default)

Int.Pull-down : CFG 18,19,20
 Int.Pull-high : CFG 3-17

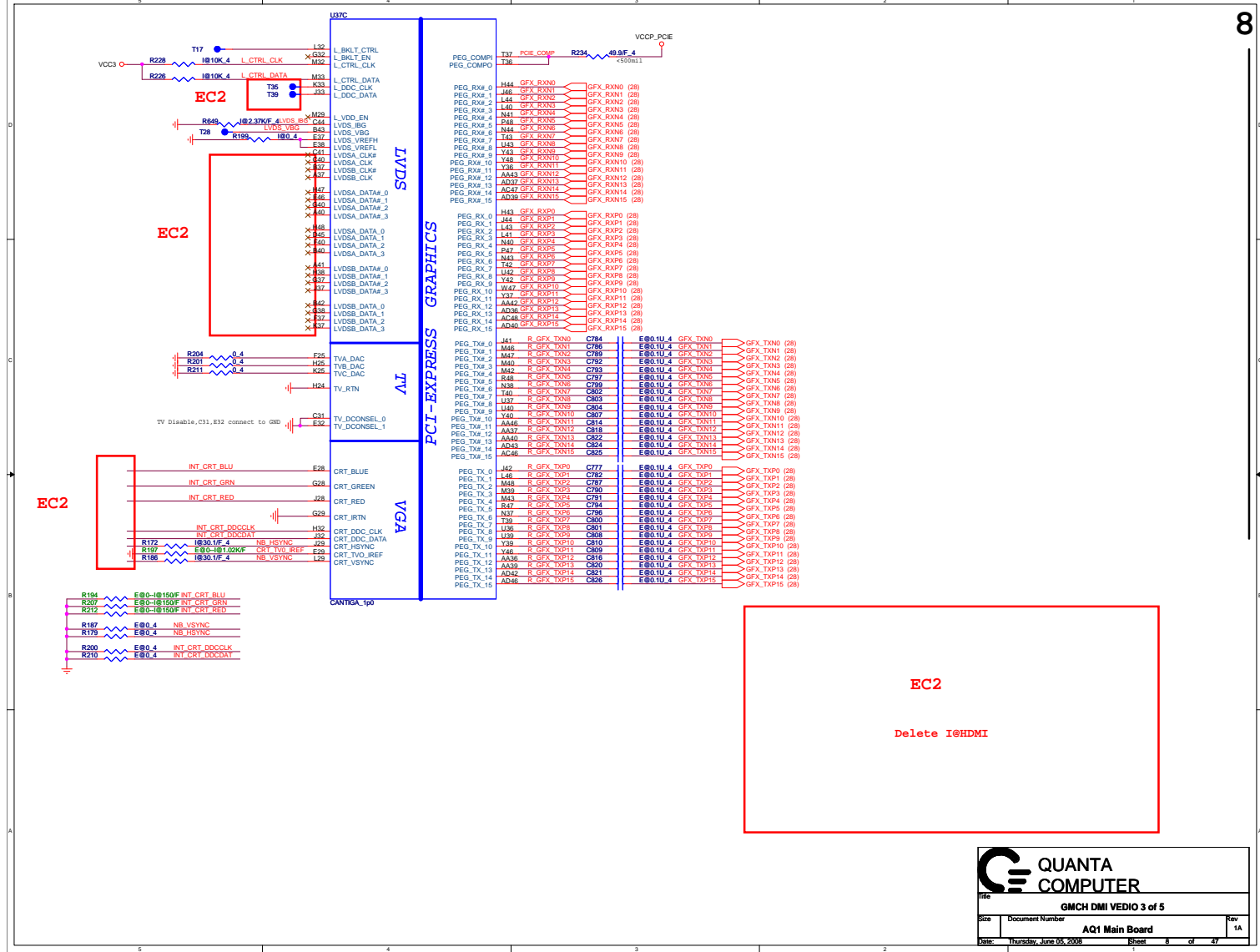


QUANTA COMPUTER

GMCH DDR II 2 of 5

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Date: Thursday, June 05, 2008
 Sheet: 7 of 47



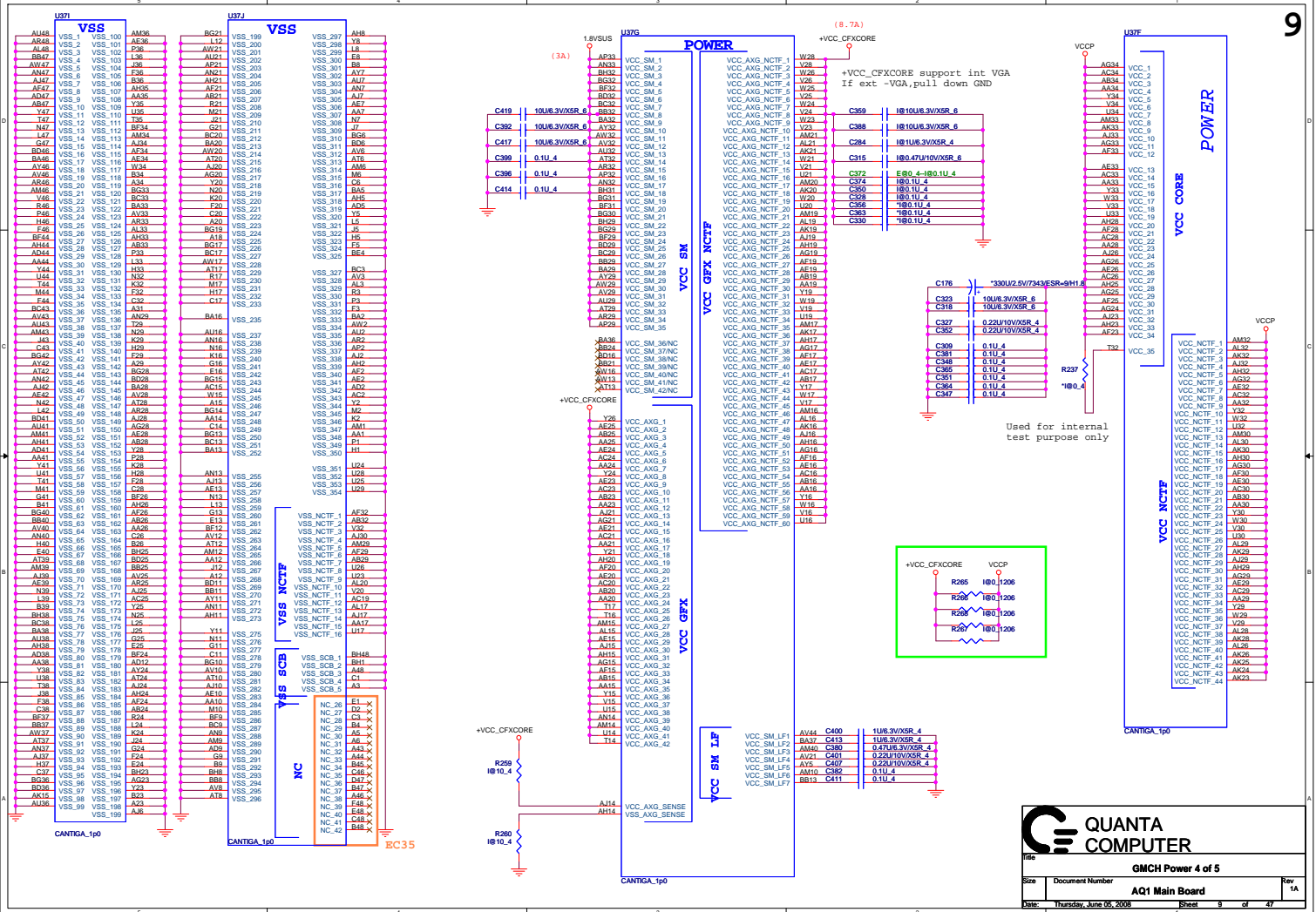
QUANTA COMPUTER

File: **GMCH DMI VEDIO 3 of 5**

Size: Document Number

Part: **AQ1 Main Board** Rev: 1A

Date: Thursday, June 05, 2008 Sheet: 8 of 47

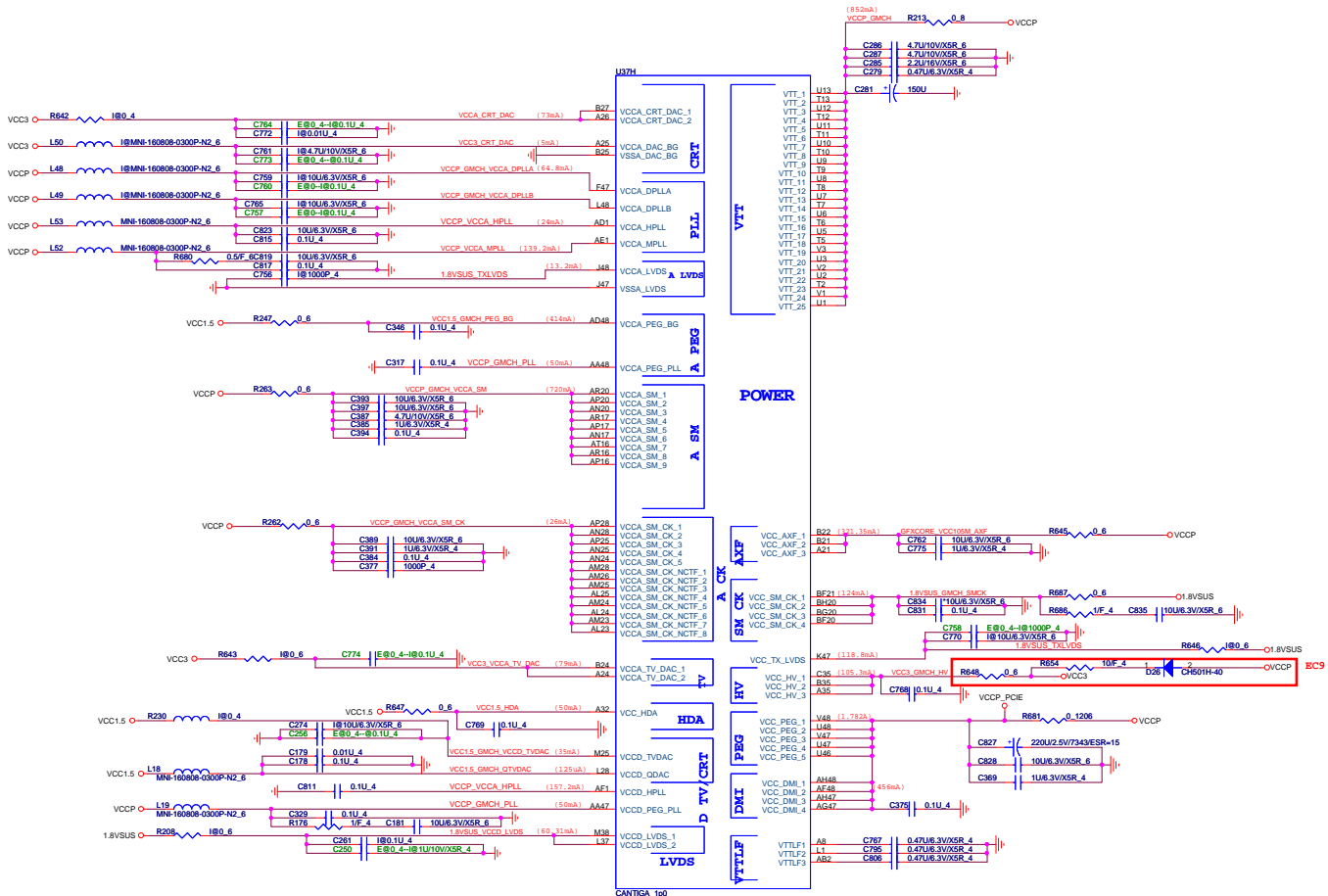


QUANTA COMPUTER

Doc: **GMCH Power 4 of 5**

Site: Document Number **AQ1 Main Board** Rev: 1A

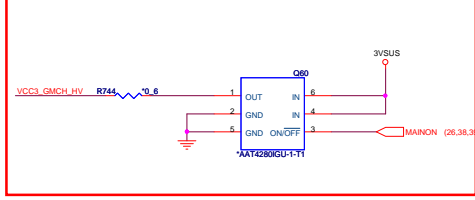
Date: Thursday, June 05, 2008 Sheet: 9 of 47



DG1.5: EXT&INT VGA Power Plane Option table

POWER PLANE	EXT VGA	INT VGA	MARK
VCCA_CRT_DAC	GND	VCC3	
VCCD_LVDS	GND	1.8VSUS	
VCC_TX_LVDS	GND	1.8VSUS	
VCCA_LVDS	GND	1.8VSUS	
VCCD_QDAC	VCC1.5	VCC1.5	Pos GMCH Thermal sensor
VCCA_TV_DAC	GND	VCC3	
VCCD_TV_DAC	GND	VCC1.5	
VCCA_DAC_BG	GND	VCC3	
VCC_AXG	GND	+VCC_CFXCORE	
VCC_AXG_NCTF	GND	+VCC_CFXCORE	
VCCA_DPLLA	GND	+VCC_CFXCORE	
VCCA_DPLLB	GND	+VCC_CFXCORE	

@:Install for Integrated Graphic UMA
 E@:Install for External Graphic Discrete

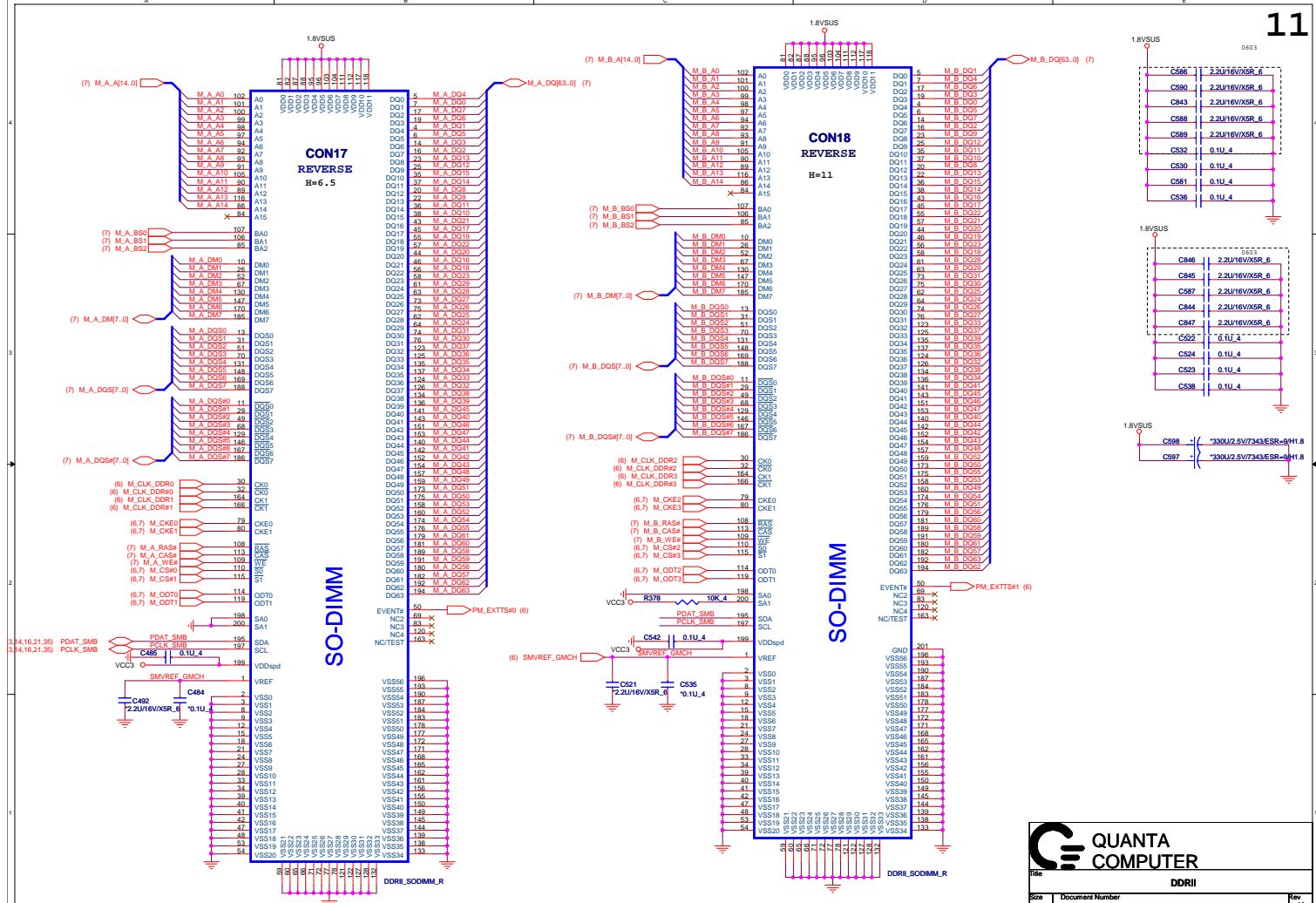


QUANTA COMPUTER

File: **GMCH Power 5 of 5**

Doc: Document Number **AQ1 Main Board** Rev: 1A

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QUANTA COMPUTER

DDR4

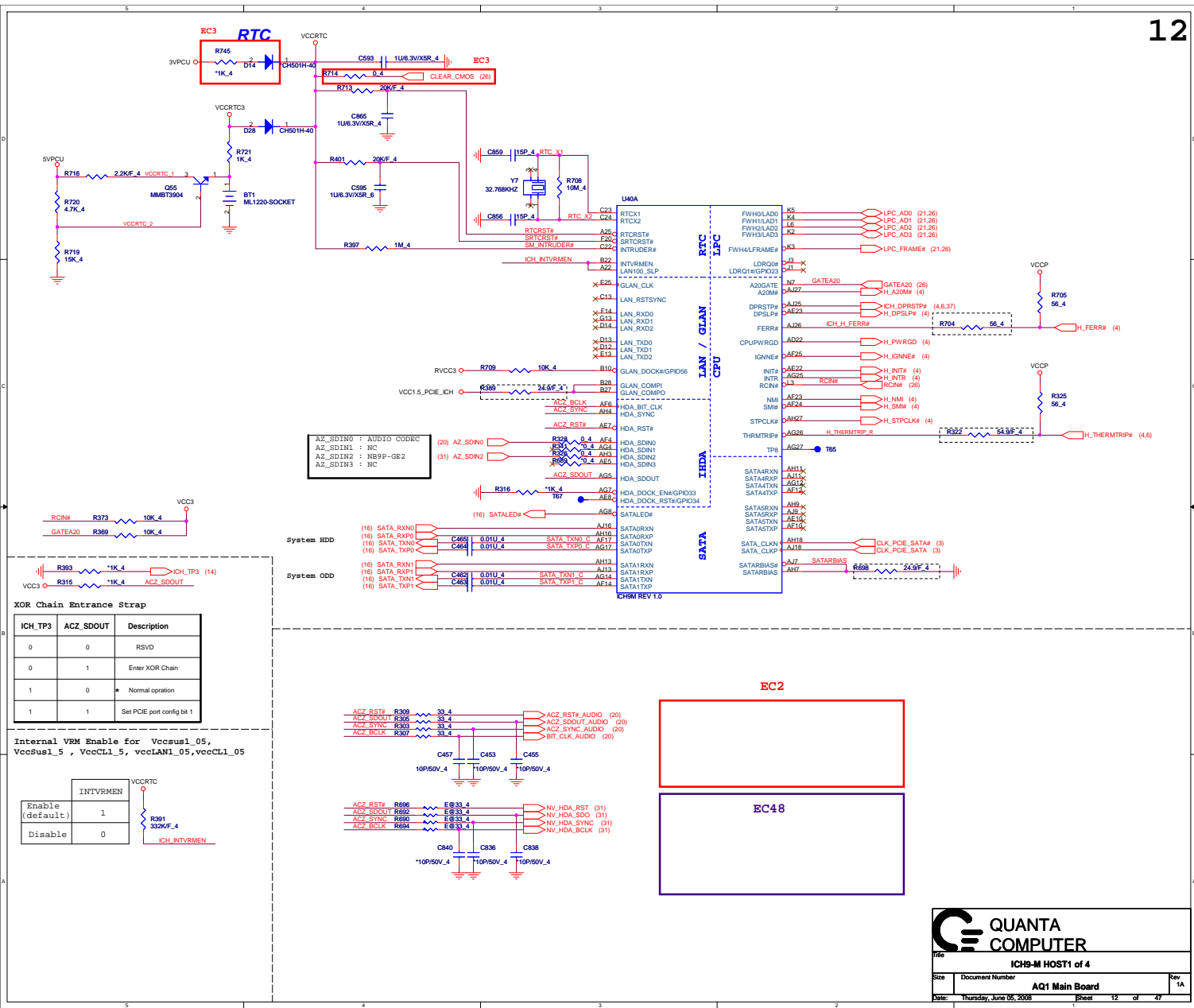
Doc: Document Number

Date: Thursday, June 05, 2008

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<AQ1 Main Board>



AZ_SDIN0 : AUDIO CODEC
 AZ_SDIN1 : IC
 AZ_SDIN2 : NB9P-GB2
 AZ_SDIN3 : IC

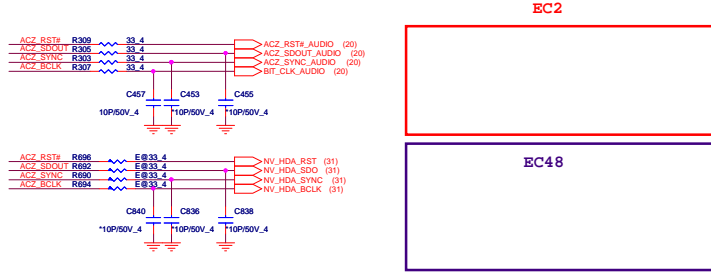
System HDD
 System ODD

XOR Chain Entrance Strap

ICH_TP3	ACZ_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation
1	1	Set PCIe port config bit 1

Internal VRM Enable for VccsUs1_05, VccSUs1_5, VccCL1_5, vccLAN1_05, vccCL1_05

Enable (default)	INTVRMEN
Enable	1
Disable	0



QUANTA COMPUTER

ICH9-M HOST1 of 4

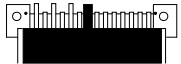
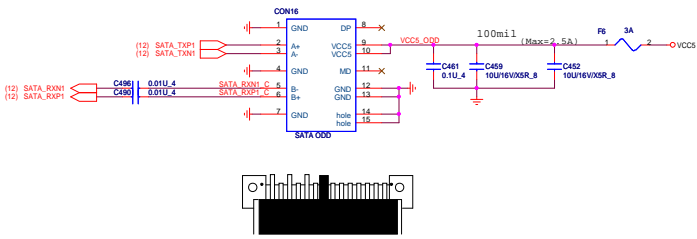
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Sheet 12 of 47

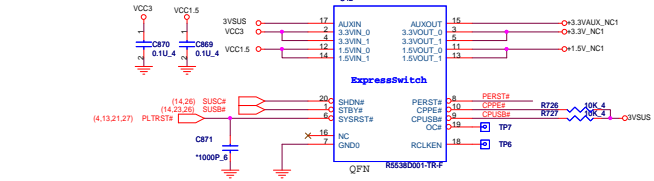
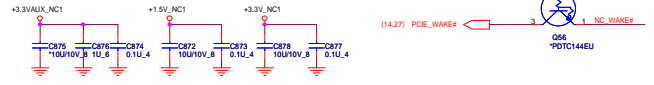
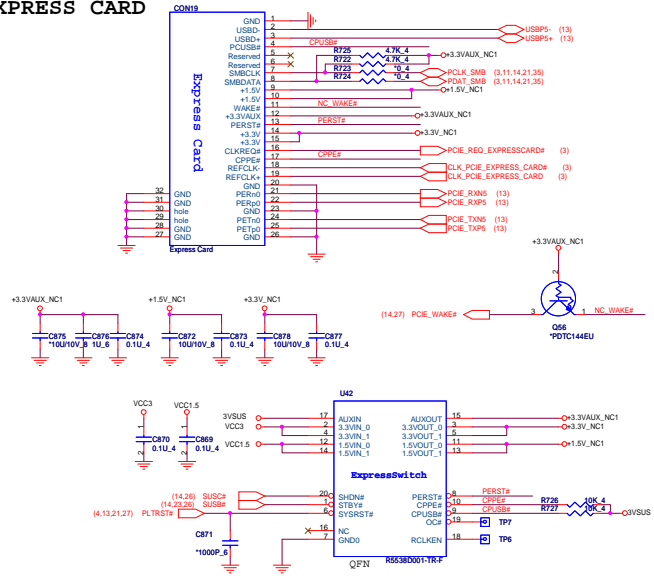
Rev 1A

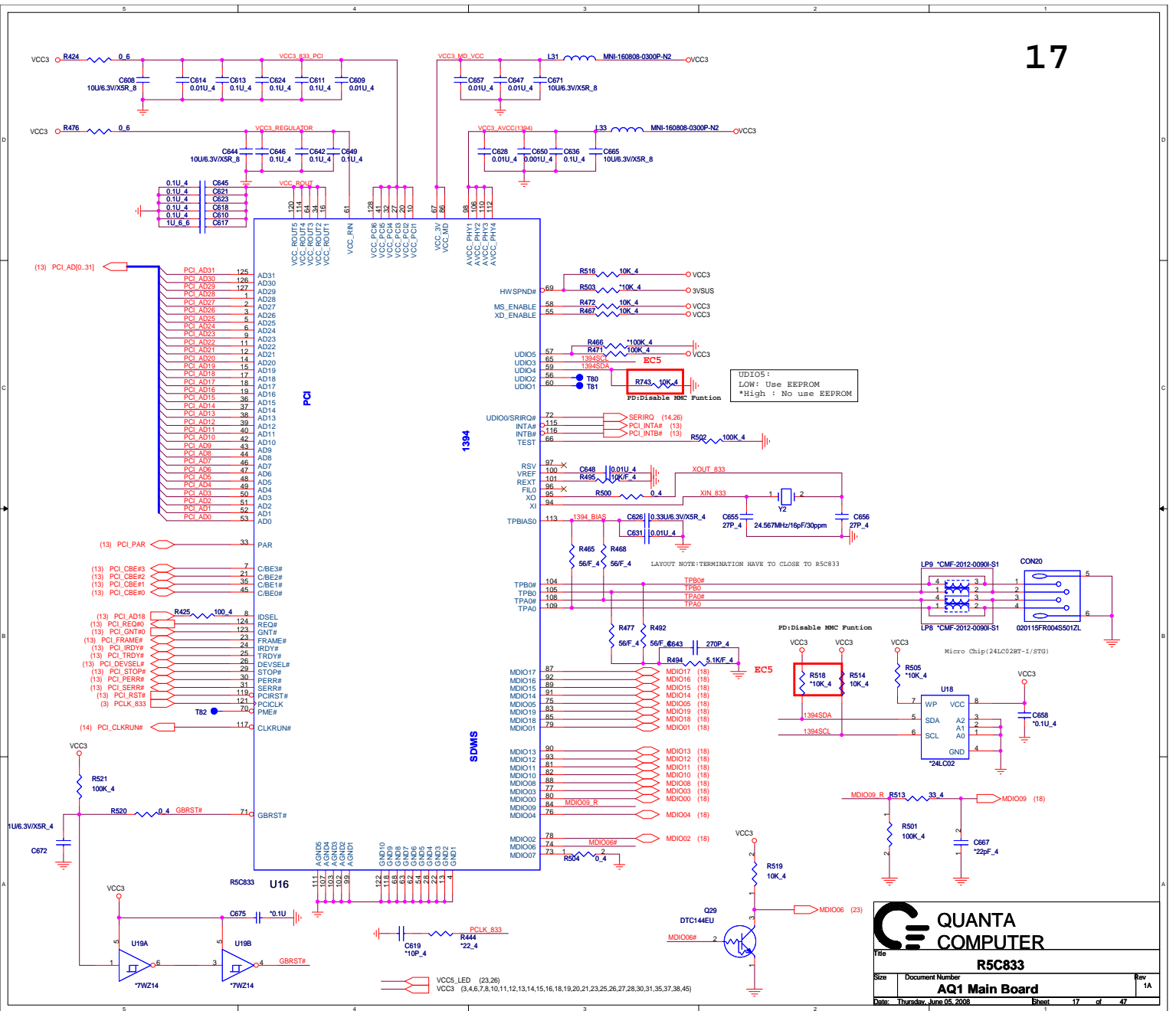
AQ1 Main Board

ODD CONNECTOR



EXPRESS CARD

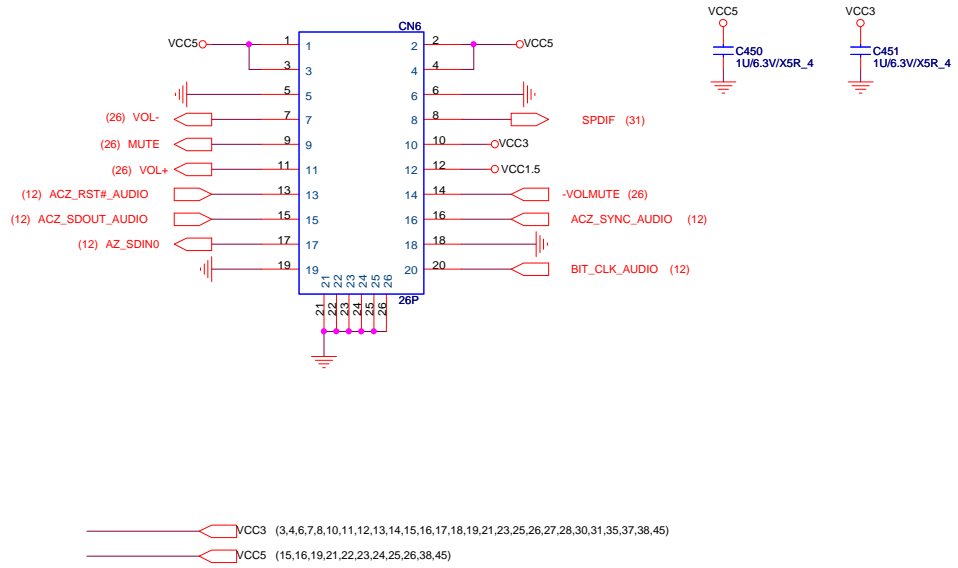





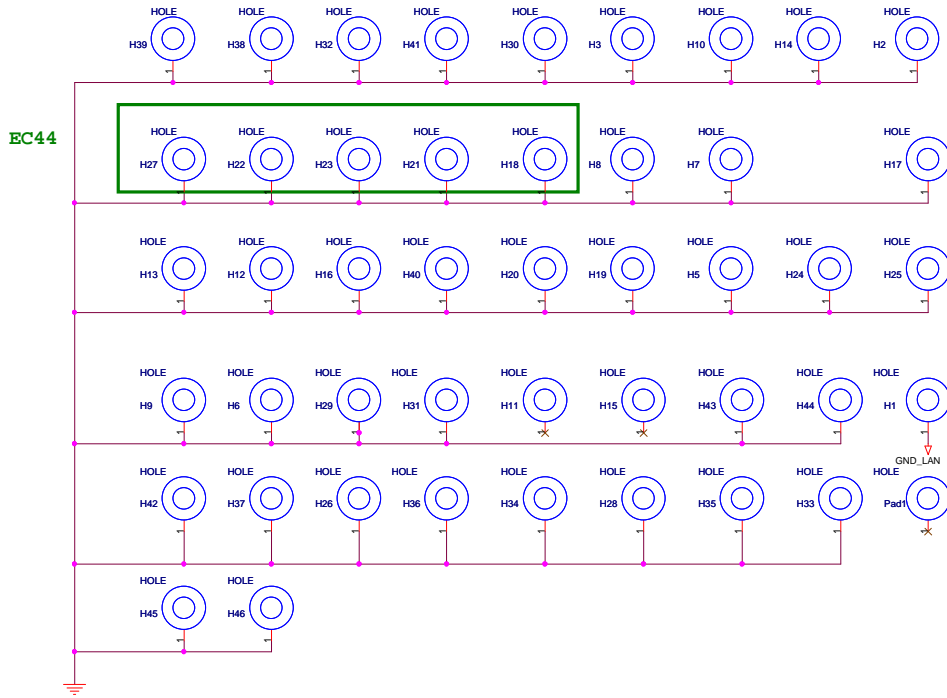
QUANTA COMPUTER

R5C833

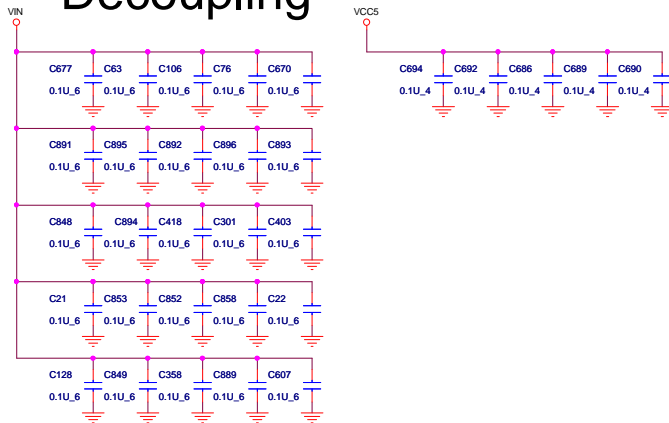
Size	Document Number	Rev
	AQ1 Main Board	1A
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 QUANTA COMPUTER		
Title Audio Board		
Size Custom	Document Number AQ1 MAIN BOARD	Rev 1A
Date: Thursday, June 05, 2008	Sheet 20 of 47	

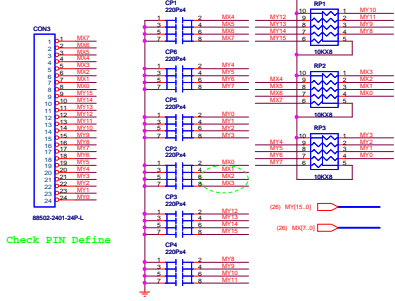


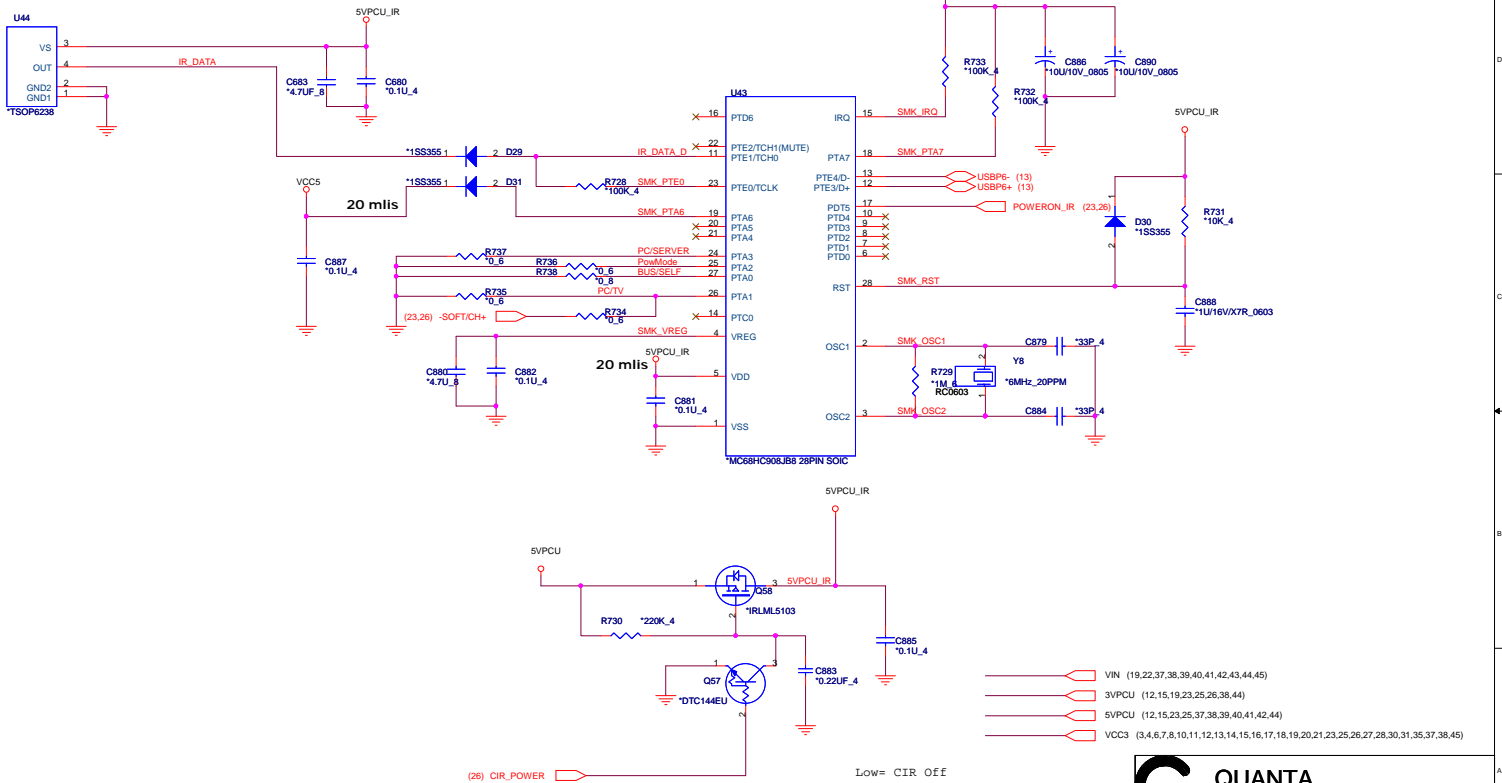
Decoupling



			QUANTA COMPUTER	
			HOLE	
Title	Document Number	AQ1 MAIN BOARD		Rev 1A
Size Custom	Date: Thursday, June 05, 2008			Sheet 22 of 47

INT. KEYBOARD





- VIN (19,22,37,38,39,40,41,42,43,44,45)
- 3VPCU (12,15,19,23,25,26,38,44)
- 5VPCU (12,15,23,25,37,38,39,40,41,42,44)
- VCC3 (3,4,6,7,8,10,11,12,13,14,15,16,17,18,19,20,21,23,25,26,27,28,30,31,35,37,38,45)

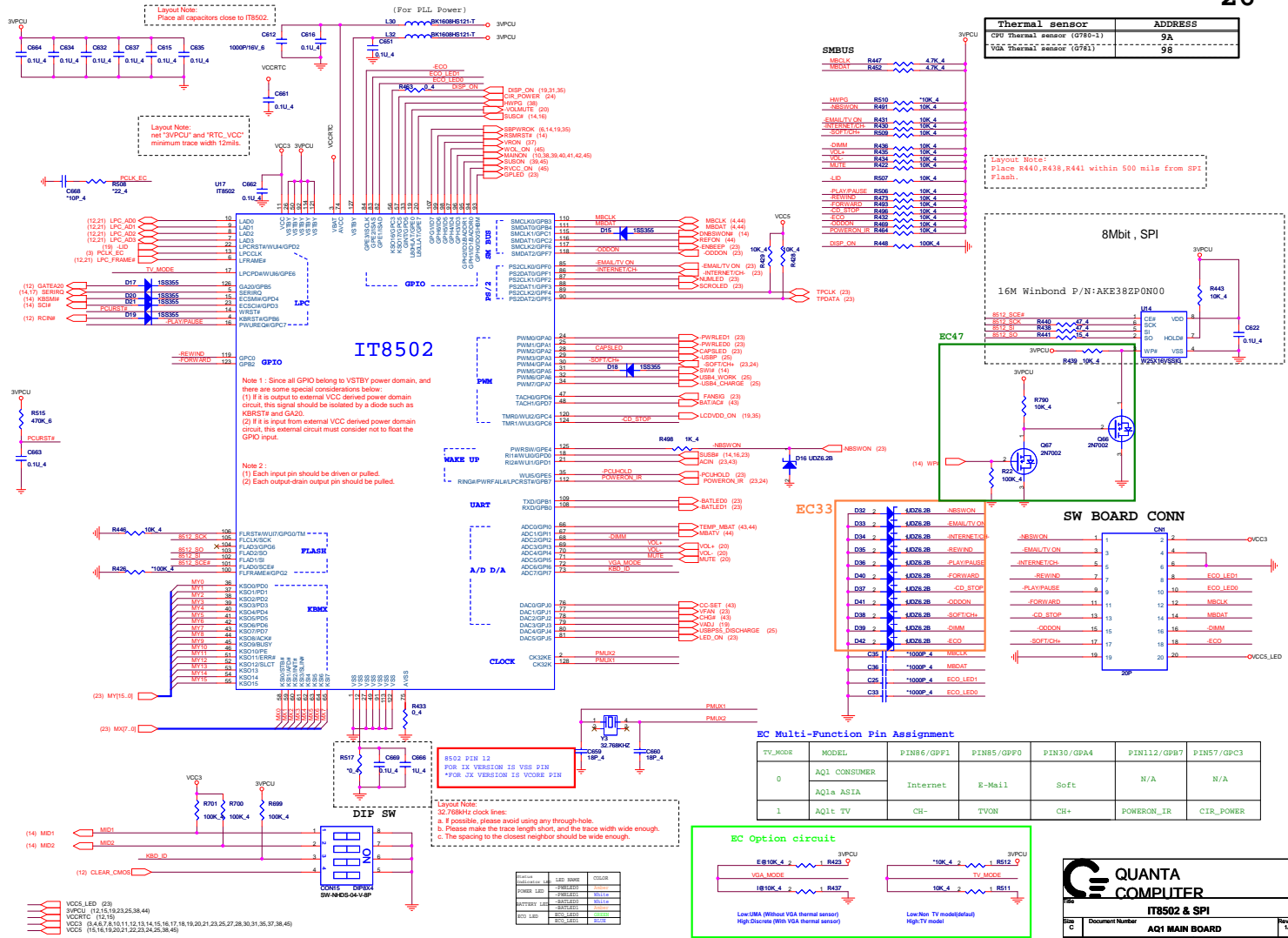
Low= CIR OFF
 Hi= CIR ON

QUANTA COMPUTER

Title: **CIR&BLUETOOTH**

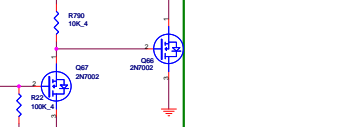
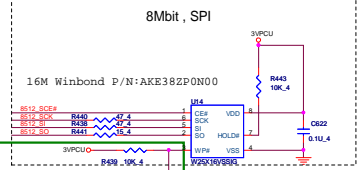
Size B	Document Number	Rev 1A
	AQ1 MAIN BOARD	

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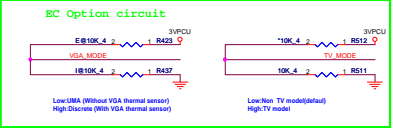
Thermal sensor	ADDRESS
CPU Thermal sensor (G780-1)	9A
VGA Thermal sensor (G781)	9B

Layout Note:
Place R440, R438, R441 within 500 mils from SPI Flash.



EC Multi-Function Pin Assignment

TV_MODE	MODEL	PIN8/GPP1	PIN5/GPP0	PIN30/GPA4	PIN112/GPB7	PIN57/GPC3
0	AQ1 CONSUMER	Internet	E-Mail	Soft	N/A	N/A
1	AQ1a ASIA	CH-	TVON	CH+	POWERON_IR	CIR_POWER



QUANTA COMPUTER

IT8502 & SPI

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Layout Note:
Place all capacitors close to IT8502.

Layout Note:
net '3VPCU' and 'RTC_VCC' minimum trace width 12mils.

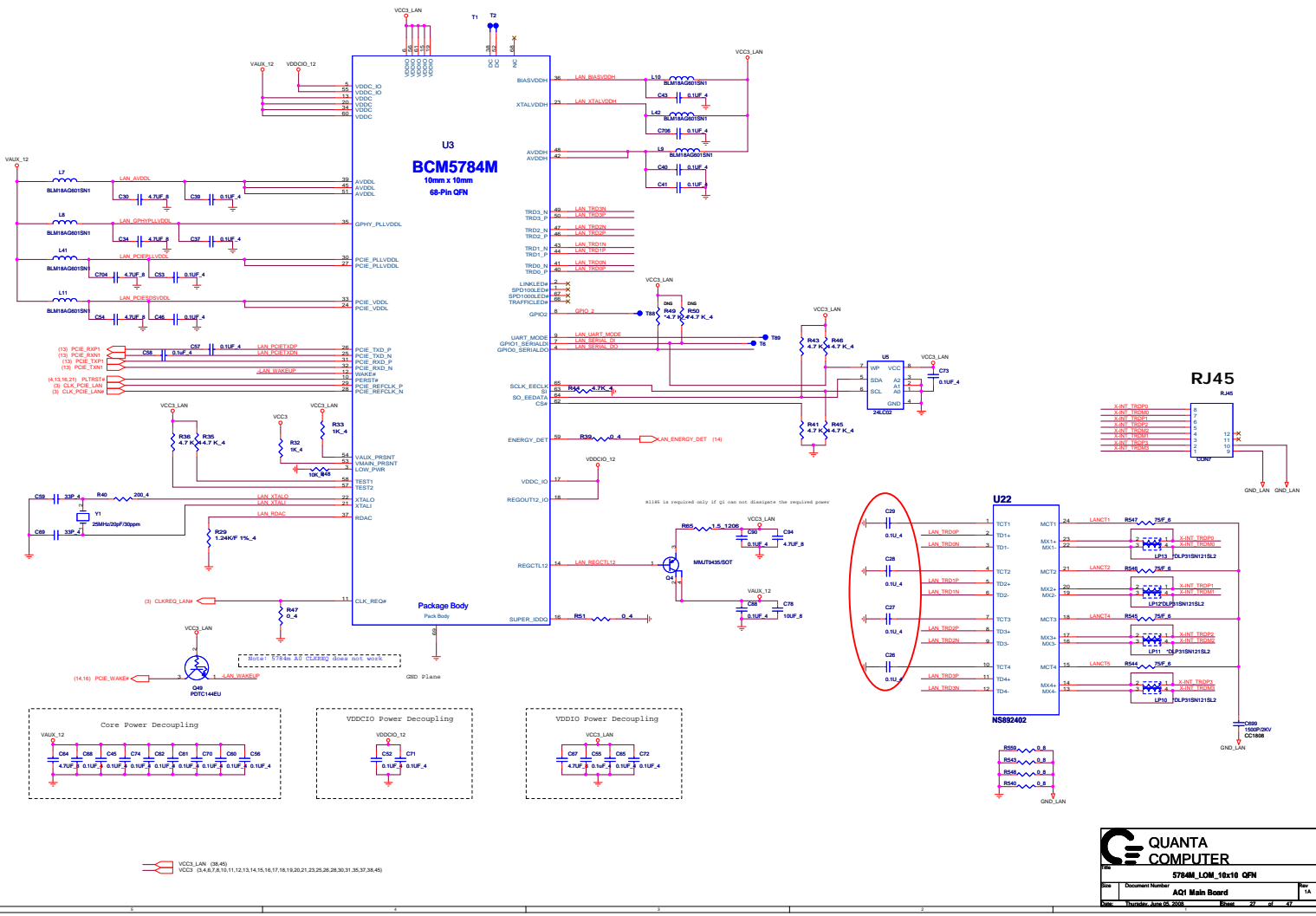
Note 1: Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRSTW and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2:
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

Layout Note:
#502 PIN 12 FOR 'X' VERSION IS VSS PIN *FOR 'X' VERSION IS VOORE PIN

Layout Note:
32.768MHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

Pin	LED NAME	COLOR
POWER_LED	POWER_LED	GREEN
BATTERY_LED	BATTERY_LED	RED
WFO_LED	WFO_LED	GREEN
WFO_LED	WFO_LED	RED

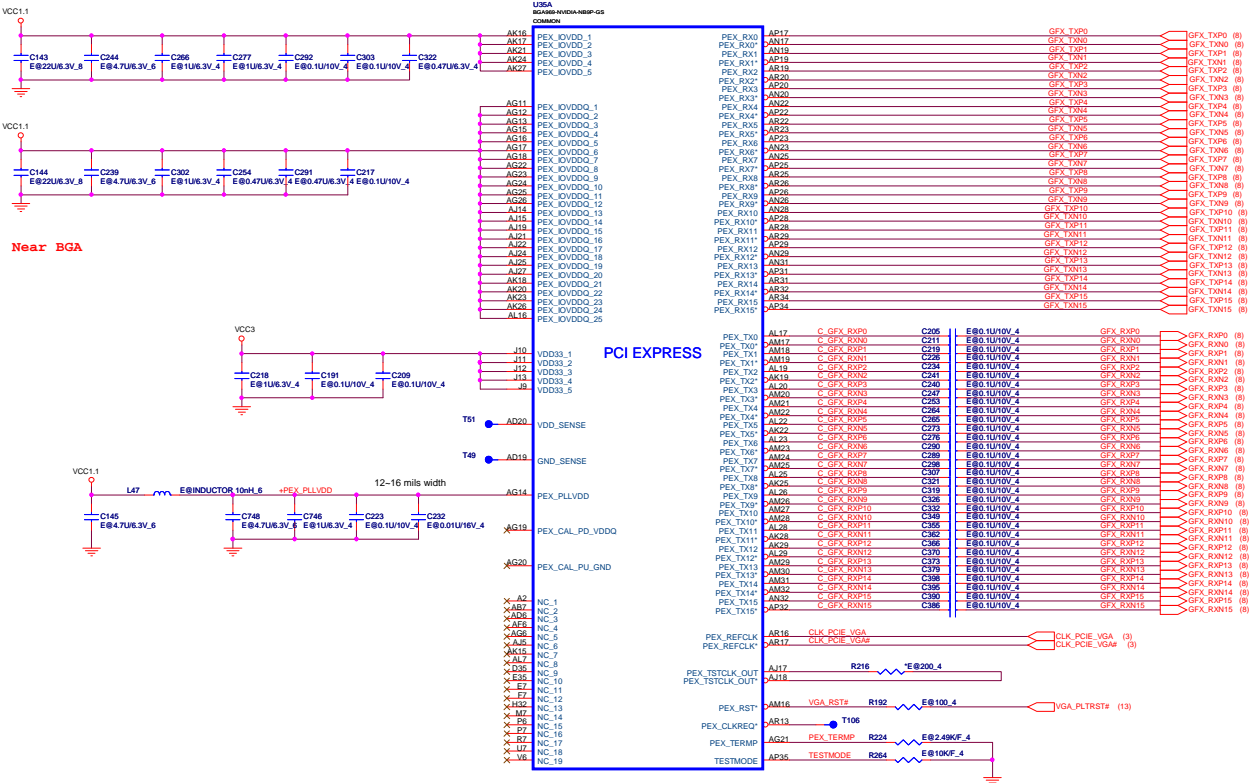


QUANTA COMPUTER

5784M_L0M_10x10 QFN

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Foundry: Avago (G. 2021) Page: 27 of 47



Component	Value	Reference	Value	Reference	Value	Reference
PEX_RX00	AP17	GFX_TXP0	GFX_TXP0	(8)	GFX_TXP0	(8)
PEX_RX01	AM12	GFX_TXP1	GFX_TXP1	(8)	GFX_TXP1	(8)
PEX_RX02	AM13	GFX_TXP2	GFX_TXP2	(8)	GFX_TXP2	(8)
PEX_RX03	AM14	GFX_TXP3	GFX_TXP3	(8)	GFX_TXP3	(8)
PEX_RX04	AM15	GFX_TXP4	GFX_TXP4	(8)	GFX_TXP4	(8)
PEX_RX05	AM16	GFX_TXP5	GFX_TXP5	(8)	GFX_TXP5	(8)
PEX_RX06	AM17	GFX_TXP6	GFX_TXP6	(8)	GFX_TXP6	(8)
PEX_RX07	AM18	GFX_TXP7	GFX_TXP7	(8)	GFX_TXP7	(8)
PEX_RX08	AM19	GFX_TXP8	GFX_TXP8	(8)	GFX_TXP8	(8)
PEX_RX09	AM20	GFX_TXP9	GFX_TXP9	(8)	GFX_TXP9	(8)
PEX_RX10	AM21	GFX_TXP10	GFX_TXP10	(8)	GFX_TXP10	(8)
PEX_RX11	AM22	GFX_TXP11	GFX_TXP11	(8)	GFX_TXP11	(8)
PEX_RX12	AM23	GFX_TXP12	GFX_TXP12	(8)	GFX_TXP12	(8)
PEX_RX13	AM24	GFX_TXP13	GFX_TXP13	(8)	GFX_TXP13	(8)
PEX_RX14	AM25	GFX_TXP14	GFX_TXP14	(8)	GFX_TXP14	(8)
PEX_RX15	AM26	GFX_TXP15	GFX_TXP15	(8)	GFX_TXP15	(8)
PEX_TX00	AL17	C GFX_RXP0	C205	E@0.1U10V_4	GFX_RXP0	(8)
PEX_TX01	AM12	C GFX_RXP1	C211	E@0.1U10V_4	GFX_RXP1	(8)
PEX_TX02	AM13	C GFX_RXP2	C234	E@0.1U10V_4	GFX_RXP2	(8)
PEX_TX03	AM14	C GFX_RXP3	C240	E@0.1U10V_4	GFX_RXP3	(8)
PEX_TX04	AM15	C GFX_RXP4	C283	E@0.1U10V_4	GFX_RXP4	(8)
PEX_TX05	AM16	C GFX_RXP5	C284	E@0.1U10V_4	GFX_RXP5	(8)
PEX_TX06	AM17	C GFX_RXP6	C273	E@0.1U10V_4	GFX_RXP6	(8)
PEX_TX07	AM18	C GFX_RXP7	C280	E@0.1U10V_4	GFX_RXP7	(8)
PEX_TX08	AM19	C GFX_RXP8	C307	E@0.1U10V_4	GFX_RXP8	(8)
PEX_TX09	AM20	C GFX_RXP9	C321	E@0.1U10V_4	GFX_RXP9	(8)
PEX_TX10	AM21	C GFX_RXP10	C319	E@0.1U10V_4	GFX_RXP10	(8)
PEX_TX11	AM22	C GFX_RXP11	C332	E@0.1U10V_4	GFX_RXP11	(8)
PEX_TX12	AM23	C GFX_RXP12	C340	E@0.1U10V_4	GFX_RXP12	(8)
PEX_TX13	AM24	C GFX_RXP13	C373	E@0.1U10V_4	GFX_RXP13	(8)
PEX_TX14	AM25	C GFX_RXP14	C380	E@0.1U10V_4	GFX_RXP14	(8)
PEX_TX15	AM26	C GFX_RXP15	C386	E@0.1U10V_4	GFX_RXP15	(8)
PEX_REFCLK	AR16	CLK_PCIE_VGA		CLK_PCIE_VGA	(9)	
PEX_REFCLK	AR17	CLK_PCIE_VGA#		CLK_PCIE_VGA#	(9)	
PEX_RST#	AM16	VGA_RST#	R192	E@100_4	VGA_FLTRST#	(13)
PEX_TERM	AP21	PEX_TERM	R224	E@2.49K_F_4		
TESTMODE	AP35	TESTMODE	R264	E@10K_F_4		

VCC1.1 (29.30,39.45)
 VCC3 (1.4,6.7,8.10,11.12,13.14,15.16,17.18,19.20,21.23,25.26,27.30,31.35,37.38,45)

QUANTA COMPUTER

File: NV9X (PCIE IF) 1/5

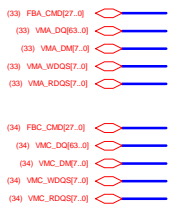
Size: Document Number: AQ1 MAIN BOARD

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U35B
80485-NVDA-NBSP-GE
COMMOD

MEMORY I/F A

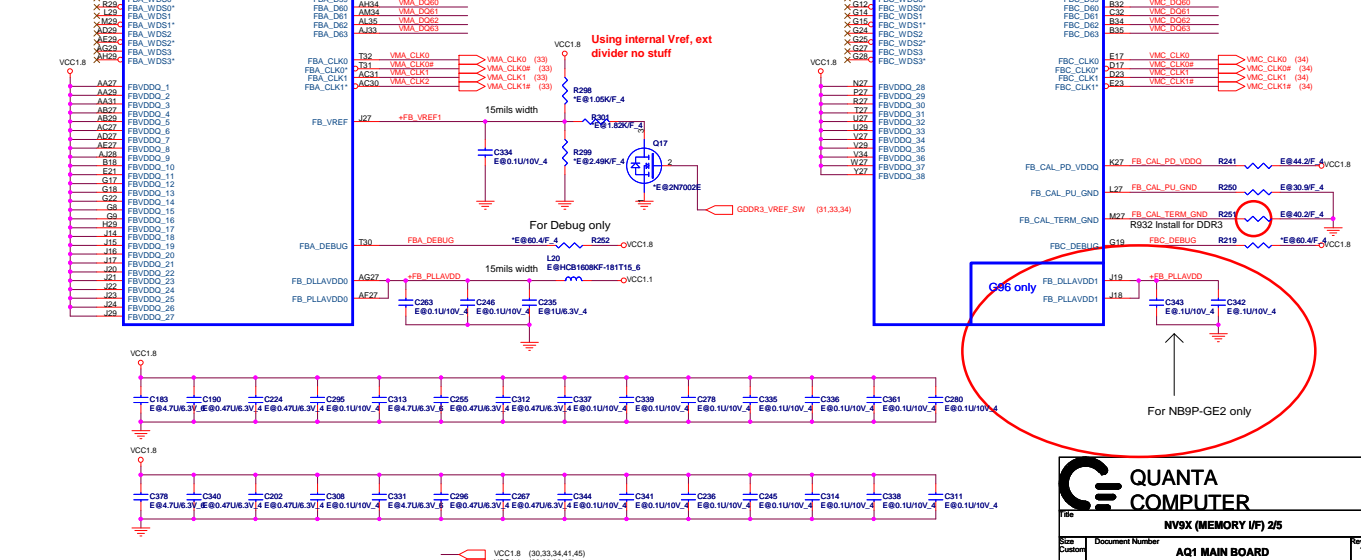
FBA_CMD0_V12	FBA_CMD0	FBA_D0	VMA_D00
FBA_CMD1_W31	FBA_CMD1	FBA_D1	VMA_D01
FBA_CMD2_V30	FBA_CMD2	FBA_D2	VMA_D02
FBA_CMD3_V32	FBA_CMD3	FBA_D3	VMA_D03
FBA_CMD4_V34	FBA_CMD4	FBA_D4	VMA_D04
FBA_CMD5_V34	FBA_CMD5	FBA_D5	VMA_D05
FBA_CMD6_V34	FBA_CMD6	FBA_D6	VMA_D06
FBA_CMD7_W33	FBA_CMD7	FBA_D7	VMA_D07
FBA_CMD8_V30	FBA_CMD8	FBA_D8	VMA_D08
FBA_CMD9_V34	FBA_CMD9	FBA_D9	VMA_D09
FBA_CMD10_V34	FBA_CMD10	FBA_D10	VMA_D10
FBA_CMD11_V34	FBA_CMD11	FBA_D11	VMA_D11
FBA_CMD12_V30	FBA_CMD12	FBA_D12	VMA_D12
FBA_CMD13_V34	FBA_CMD13	FBA_D13	VMA_D13
FBA_CMD14_V32	FBA_CMD14	FBA_D14	VMA_D14
FBA_CMD15_V34	FBA_CMD15	FBA_D15	VMA_D15
FBA_CMD16_V34	FBA_CMD16	FBA_D16	VMA_D16
FBA_CMD17_V34	FBA_CMD17	FBA_D17	VMA_D17
FBA_CMD18_V34	FBA_CMD18	FBA_D18	VMA_D18
FBA_CMD19_V34	FBA_CMD19	FBA_D19	VMA_D19
FBA_CMD20_V34	FBA_CMD20	FBA_D20	VMA_D20
FBA_CMD21_V34	FBA_CMD21	FBA_D21	VMA_D21
FBA_CMD22_V34	FBA_CMD22	FBA_D22	VMA_D22
FBA_CMD23_V30	FBA_CMD23	FBA_D23	VMA_D23
FBA_CMD24_V34	FBA_CMD24	FBA_D24	VMA_D24
FBA_CMD25_V34	FBA_CMD25	FBA_D25	VMA_D25
FBA_CMD26_V34	FBA_CMD26	FBA_D26	VMA_D26
FBA_CMD27_V34	FBA_CMD27	FBA_D27	VMA_D27
FBA_CMD28_V34	FBA_CMD28	FBA_D28	VMA_D28
FBA_CMD29_V34	FBA_CMD29	FBA_D29	VMA_D29
FBA_CMD30_V34	FBA_CMD30	FBA_D30	VMA_D30
FBA_CMD31_V34	FBA_CMD31	FBA_D31	VMA_D31
FBA_CMD32_V34	FBA_CMD32	FBA_D32	VMA_D32
FBA_CMD33_V34	FBA_CMD33	FBA_D33	VMA_D33
FBA_CMD34_V34	FBA_CMD34	FBA_D34	VMA_D34
FBA_CMD35_V34	FBA_CMD35	FBA_D35	VMA_D35
FBA_CMD36_V34	FBA_CMD36	FBA_D36	VMA_D36
FBA_CMD37_V34	FBA_CMD37	FBA_D37	VMA_D37
FBA_CMD38_V34	FBA_CMD38	FBA_D38	VMA_D38
FBA_CMD39_V34	FBA_CMD39	FBA_D39	VMA_D39
FBA_CMD40_V34	FBA_CMD40	FBA_D40	VMA_D40
FBA_CMD41_V34	FBA_CMD41	FBA_D41	VMA_D41
FBA_CMD42_V34	FBA_CMD42	FBA_D42	VMA_D42
FBA_CMD43_V34	FBA_CMD43	FBA_D43	VMA_D43
FBA_CMD44_V34	FBA_CMD44	FBA_D44	VMA_D44
FBA_CMD45_V34	FBA_CMD45	FBA_D45	VMA_D45
FBA_CMD46_V34	FBA_CMD46	FBA_D46	VMA_D46
FBA_CMD47_V34	FBA_CMD47	FBA_D47	VMA_D47
FBA_CMD48_V34	FBA_CMD48	FBA_D48	VMA_D48
FBA_CMD49_V34	FBA_CMD49	FBA_D49	VMA_D49
FBA_CMD50_V34	FBA_CMD50	FBA_D50	VMA_D50
FBA_CMD51_V34	FBA_CMD51	FBA_D51	VMA_D51
FBA_CMD52_V34	FBA_CMD52	FBA_D52	VMA_D52
FBA_CMD53_V34	FBA_CMD53	FBA_D53	VMA_D53
FBA_CMD54_V34	FBA_CMD54	FBA_D54	VMA_D54
FBA_CMD55_V34	FBA_CMD55	FBA_D55	VMA_D55
FBA_CMD56_V34	FBA_CMD56	FBA_D56	VMA_D56
FBA_CMD57_V34	FBA_CMD57	FBA_D57	VMA_D57
FBA_CMD58_V34	FBA_CMD58	FBA_D58	VMA_D58
FBA_CMD59_V34	FBA_CMD59	FBA_D59	VMA_D59
FBA_CMD60_V34	FBA_CMD60	FBA_D60	VMA_D60
FBA_CMD61_V34	FBA_CMD61	FBA_D61	VMA_D61
FBA_CMD62_V34	FBA_CMD62	FBA_D62	VMA_D62
FBA_CMD63_V34	FBA_CMD63	FBA_D63	VMA_D63
FBA_CMD64_V34	FBA_CMD64	FBA_D64	VMA_D64
FBA_CMD65_V34	FBA_CMD65	FBA_D65	VMA_D65
FBA_CMD66_V34	FBA_CMD66	FBA_D66	VMA_D66
FBA_CMD67_V34	FBA_CMD67	FBA_D67	VMA_D67
FBA_CMD68_V34	FBA_CMD68	FBA_D68	VMA_D68
FBA_CMD69_V34	FBA_CMD69	FBA_D69	VMA_D69
FBA_CMD70_V34	FBA_CMD70	FBA_D70	VMA_D70
FBA_CMD71_V34	FBA_CMD71	FBA_D71	VMA_D71
FBA_CMD72_V34	FBA_CMD72	FBA_D72	VMA_D72
FBA_CMD73_V34	FBA_CMD73	FBA_D73	VMA_D73
FBA_CMD74_V34	FBA_CMD74	FBA_D74	VMA_D74
FBA_CMD75_V34	FBA_CMD75	FBA_D75	VMA_D75
FBA_CMD76_V34	FBA_CMD76	FBA_D76	VMA_D76
FBA_CMD77_V34	FBA_CMD77	FBA_D77	VMA_D77
FBA_CMD78_V34	FBA_CMD78	FBA_D78	VMA_D78
FBA_CMD79_V34	FBA_CMD79	FBA_D79	VMA_D79
FBA_CMD80_V34	FBA_CMD80	FBA_D80	VMA_D80
FBA_CMD81_V34	FBA_CMD81	FBA_D81	VMA_D81
FBA_CMD82_V34	FBA_CMD82	FBA_D82	VMA_D82
FBA_CMD83_V34	FBA_CMD83	FBA_D83	VMA_D83
FBA_CMD84_V34	FBA_CMD84	FBA_D84	VMA_D84
FBA_CMD85_V34	FBA_CMD85	FBA_D85	VMA_D85
FBA_CMD86_V34	FBA_CMD86	FBA_D86	VMA_D86
FBA_CMD87_V34	FBA_CMD87	FBA_D87	VMA_D87
FBA_CMD88_V34	FBA_CMD88	FBA_D88	VMA_D88
FBA_CMD89_V34	FBA_CMD89	FBA_D89	VMA_D89
FBA_CMD90_V34	FBA_CMD90	FBA_D90	VMA_D90
FBA_CMD91_V34	FBA_CMD91	FBA_D91	VMA_D91
FBA_CMD92_V34	FBA_CMD92	FBA_D92	VMA_D92
FBA_CMD93_V34	FBA_CMD93	FBA_D93	VMA_D93
FBA_CMD94_V34	FBA_CMD94	FBA_D94	VMA_D94
FBA_CMD95_V34	FBA_CMD95	FBA_D95	VMA_D95
FBA_CMD96_V34	FBA_CMD96	FBA_D96	VMA_D96
FBA_CMD97_V34	FBA_CMD97	FBA_D97	VMA_D97
FBA_CMD98_V34	FBA_CMD98	FBA_D98	VMA_D98
FBA_CMD99_V34	FBA_CMD99	FBA_D99	VMA_D99
FBA_CMD100_V34	FBA_CMD100	FBA_D100	VMA_D100



U35C
80485-NVDA-NBSP-GE
COMMOD

MEMORY I/F B

FBC_CMD0_C17	FBC_CMD0	FBC_D0	VMC_D00
FBC_CMD1_B18	FBC_CMD1	FBC_D1	VMC_D01
FBC_CMD2_F21	FBC_CMD2	FBC_D2	VMC_D02
FBC_CMD3_A23	FBC_CMD3	FBC_D3	VMC_D03
FBC_CMD4_D21	FBC_CMD4	FBC_D4	VMC_D04
FBC_CMD5_B21	FBC_CMD5	FBC_D5	VMC_D05
FBC_CMD6_E20	FBC_CMD6	FBC_D6	VMC_D06
FBC_CMD7_F20	FBC_CMD7	FBC_D7	VMC_D07
FBC_CMD8_F20	FBC_CMD8	FBC_D8	VMC_D08
FBC_CMD9_F20	FBC_CMD9	FBC_D9	VMC_D09
FBC_CMD10_F19	FBC_CMD10	FBC_D10	VMC_D10
FBC_CMD11_A22	FBC_CMD11	FBC_D11	VMC_D11
FBC_CMD12_A22	FBC_CMD12	FBC_D12	VMC_D12
FBC_CMD13_C22	FBC_CMD13	FBC_D13	VMC_D13
FBC_CMD14_B17	FBC_CMD14	FBC_D14	VMC_D14
FBC_CMD15_C21	FBC_CMD15	FBC_D15	VMC_D15
FBC_CMD16_C26	FBC_CMD16	FBC_D16	VMC_D16
FBC_CMD17_D24	FBC_CMD17	FBC_D17	VMC_D17
FBC_CMD18_C20	FBC_CMD18	FBC_D18	VMC_D18
FBC_CMD19_A19	FBC_CMD19	FBC_D19	VMC_D19
FBC_CMD20_D22	FBC_CMD20	FBC_D20	VMC_D20
FBC_CMD21_D22	FBC_CMD21	FBC_D21	VMC_D21
FBC_CMD22_D22	FBC_CMD22	FBC_D22	VMC_D22
FBC_CMD23_D22	FBC_CMD23	FBC_D23	VMC_D23
FBC_CMD24_D18	FBC_CMD24	FBC_D24	VMC_D24
FBC_CMD25_F18	FBC_CMD25	FBC_D25	VMC_D25
FBC_CMD26_F18	FBC_CMD26	FBC_D26	VMC_D26
FBC_CMD27_F22	FBC_CMD27	FBC_D27	VMC_D27
FBC_CMD28_C21	FBC_CMD28	FBC_D28	VMC_D28
FBC_CMD29_C21	FBC_CMD29	FBC_D29	VMC_D29
FBC_CMD30_C21	FBC_CMD30	FBC_D30	VMC_D30
FBC_CMD31_C21	FBC_CMD31	FBC_D31	VMC_D31
FBC_CMD32_C21	FBC_CMD32	FBC_D32	VMC_D32
FBC_CMD33_C21	FBC_CMD33	FBC_D33	VMC_D33
FBC_CMD34_C21	FBC_CMD34	FBC_D34	VMC_D34
FBC_CMD35_C21	FBC_CMD35	FBC_D35	VMC_D35
FBC_CMD36_C21	FBC_CMD36	FBC_D36	VMC_D36
FBC_CMD37_C21	FBC_CMD37	FBC_D37	VMC_D37
FBC_CMD38_C21	FBC_CMD38	FBC_D38	VMC_D38
FBC_CMD39_C21	FBC_CMD39	FBC_D39	VMC_D39
FBC_CMD40_C21	FBC_CMD40	FBC_D40	VMC_D40
FBC_CMD41_C21	FBC_CMD41	FBC_D41	VMC_D41
FBC_CMD42_C21	FBC_CMD42	FBC_D42	VMC_D42
FBC_CMD43_C21	FBC_CMD43	FBC_D43	VMC_D43
FBC_CMD44_C21	FBC_CMD44	FBC_D44	VMC_D44
FBC_CMD45_C21	FBC_CMD45	FBC_D45	VMC_D45
FBC_CMD46_C21	FBC_CMD46	FBC_D46	VMC_D46
FBC_CMD47_C21	FBC_CMD47	FBC_D47	VMC_D47
FBC_CMD48_C21	FBC_CMD48	FBC_D48	VMC_D48
FBC_CMD49_C21	FBC_CMD49	FBC_D49	VMC_D49
FBC_CMD50_C21	FBC_CMD50	FBC_D50	VMC_D50
FBC_CMD51_C21	FBC_CMD51	FBC_D51	VMC_D51
FBC_CMD52_C21	FBC_CMD52	FBC_D52	VMC_D52
FBC_CMD53_C21	FBC_CMD53	FBC_D53	VMC_D53
FBC_CMD54_C21	FBC_CMD54	FBC_D54	VMC_D54
FBC_CMD55_C21	FBC_CMD55	FBC_D55	VMC_D55
FBC_CMD56_C21	FBC_CMD56	FBC_D56	VMC_D56
FBC_CMD57_C21	FBC_CMD57	FBC_D57	VMC_D57
FBC_CMD58_C21	FBC_CMD58	FBC_D58	VMC_D58
FBC_CMD59_C21	FBC_CMD59	FBC_D59	VMC_D59
FBC_CMD60_C21	FBC_CMD60	FBC_D60	VMC_D60
FBC_CMD61_C21	FBC_CMD61	FBC_D61	VMC_D61
FBC_CMD62_C21	FBC_CMD62	FBC_D62	VMC_D62
FBC_CMD63_C21	FBC_CMD63	FBC_D63	VMC_D63
FBC_CMD64_C21	FBC_CMD64	FBC_D64	VMC_D64
FBC_CMD65_C21	FBC_CMD65	FBC_D65	VMC_D65
FBC_CMD66_C21	FBC_CMD66	FBC_D66	VMC_D66
FBC_CMD67_C21	FBC_CMD67	FBC_D67	VMC_D67
FBC_CMD68_C21	FBC_CMD68	FBC_D68	VMC_D68
FBC_CMD69_C21	FBC_CMD69	FBC_D69	VMC_D69
FBC_CMD70_C21	FBC_CMD70	FBC_D70	VMC_D70
FBC_CMD71_C21	FBC_CMD71	FBC_D71	VMC_D71
FBC_CMD72_C21	FBC_CMD72	FBC_D72	VMC_D72
FBC_CMD73_C21	FBC_CMD73	FBC_D73	VMC_D73
FBC_CMD74_C21	FBC_CMD74	FBC_D74	VMC_D74
FBC_CMD75_C21	FBC_CMD75	FBC_D75	VMC_D75
FBC_CMD76_C21	FBC_CMD76	FBC_D76	VMC_D76
FBC_CMD77_C21	FBC_CMD77	FBC_D77	VMC_D77
FBC_CMD78_C21	FBC_CMD78	FBC_D78	VMC_D78
FBC_CMD79_C21	FBC_CMD79	FBC_D79	VMC_D79
FBC_CMD80_C21	FBC_CMD80	FBC_D80	VMC_D80
FBC_CMD81_C21	FBC_CMD81	FBC_D81	VMC_D81
FBC_CMD82_C21	FBC_CMD82	FBC_D82	VMC_D82
FBC_CMD83_C21	FBC_CMD83	FBC_D83	VMC_D83
FBC_CMD84_C21	FBC_CMD84	FBC_D84	VMC_D84
FBC_CMD85_C21	FBC_CMD85	FBC_D85	VMC_D85
FBC_CMD86_C21	FBC_CMD86	FBC_D86	VMC_D86
FBC_CMD87_C21	FBC_CMD87	FBC_D87	VMC_D87
FBC_CMD88_C21	FBC_CMD88	FBC_D88	VMC_D88
FBC_CMD89_C21	FBC_CMD89	FBC_D89	VMC_D89
FBC_CMD90_C21	FBC_CMD90	FBC_D90	VMC_D90
FBC_CMD91_C21	FBC_CMD91	FBC_D91	VMC_D91
FBC_CMD92_C21	FBC_CMD92	FBC_D92	VMC_D92
FBC_CMD93_C21	FBC_CMD93	FBC_D93	VMC_D93
FBC_CMD94_C21	FBC_CMD94	FBC_D94	VMC_D94
FBC_CMD95_C21	FBC_CMD95	FBC_D95	VMC_D95
FBC_CMD96_C21	FBC_CMD96	FBC_D96	VMC_D96
FBC_CMD97_C21	FBC_CMD97	FBC_D97	VMC_D97
FBC_CMD98_C21	FBC_CMD98	FBC_D98	VMC_D98
FBC_CMD99_C21	FBC_CMD99	FBC_D99	VMC_D99
FBC_CMD100_C21	FBC_CMD100	FBC_D100	VMC_D100



QUANTA COMPUTER

NV9X (MEMORY I/F) 2/5

Doc: AQ1 MAIN BOARD

Rev: 1A

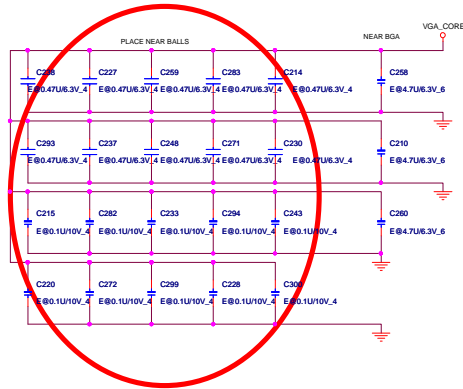
Date: Thursday, June 05, 2008

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NVVDD Decoupling

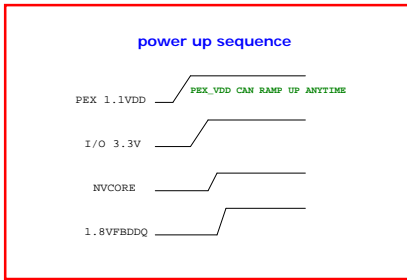
U360
80408AVDDA-NVSP-GS
COMMON

VGA_CORE	LS6F	LS6F	VGA_CORE
	AB11	VDD_001	P21
	AB13	VDD_002	P22
	AB15	VDD_003	P23
	AB17	VDD_004	R11
	AB19	VDD_005	R12
	AB21	VDD_006	R13
	AB23	VDD_007	R14
	AB25	VDD_008	R15
	AC11	VDD_009	R16
	AC12	VDD_010	R17
	AC13	VDD_011	R18
	AC14	VDD_012	R19
	AC15	VDD_013	R20
	AC16	VDD_014	R21
	AC17	VDD_015	R22
	AC18	VDD_016	R23
	AC19	VDD_017	R24
	AC20	VDD_018	R25
	AC21	VDD_019	R26
	AC22	VDD_020	T14
	AC23	VDD_021	T15
	AC24	VDD_022	T16
	AC25	VDD_023	T17
	AD12	VDD_024	T22
	AD14	VDD_024	T24
	AD16	VDD_025	V11
	AD18	VDD_026	V12
	AD22	VDD_027	V13
	AD24	VDD_028	V17
	L11	VDD_030	W18
	L12	VDD_031	W21
	L13	VDD_032	W22
	L14	VDD_033	W25
	L15	VDD_034	W11
	L16	VDD_035	W12
	L17	VDD_036	W13
	L18	VDD_037	W14
	L19	VDD_038	W15
	L20	VDD_039	W16
	L21	VDD_040	W17
	L22	VDD_041	W18
	L23	VDD_042	W19
	L24	VDD_043	W20
	L25	VDD_044	W21
	M12	VDD_045	W22
	M14	VDD_046	W23
	M16	VDD_047	W24
	M18	VDD_048	W25
	M20	VDD_049	Y12
	M22	VDD_050	Y13
	M24	VDD_051	Y16
	P11	VDD_052	Y18
	P13	VDD_053	Y20
	P15	VDD_054	Y22
	P17	VDD_055	Y24
	P19	VDD_056	Y24



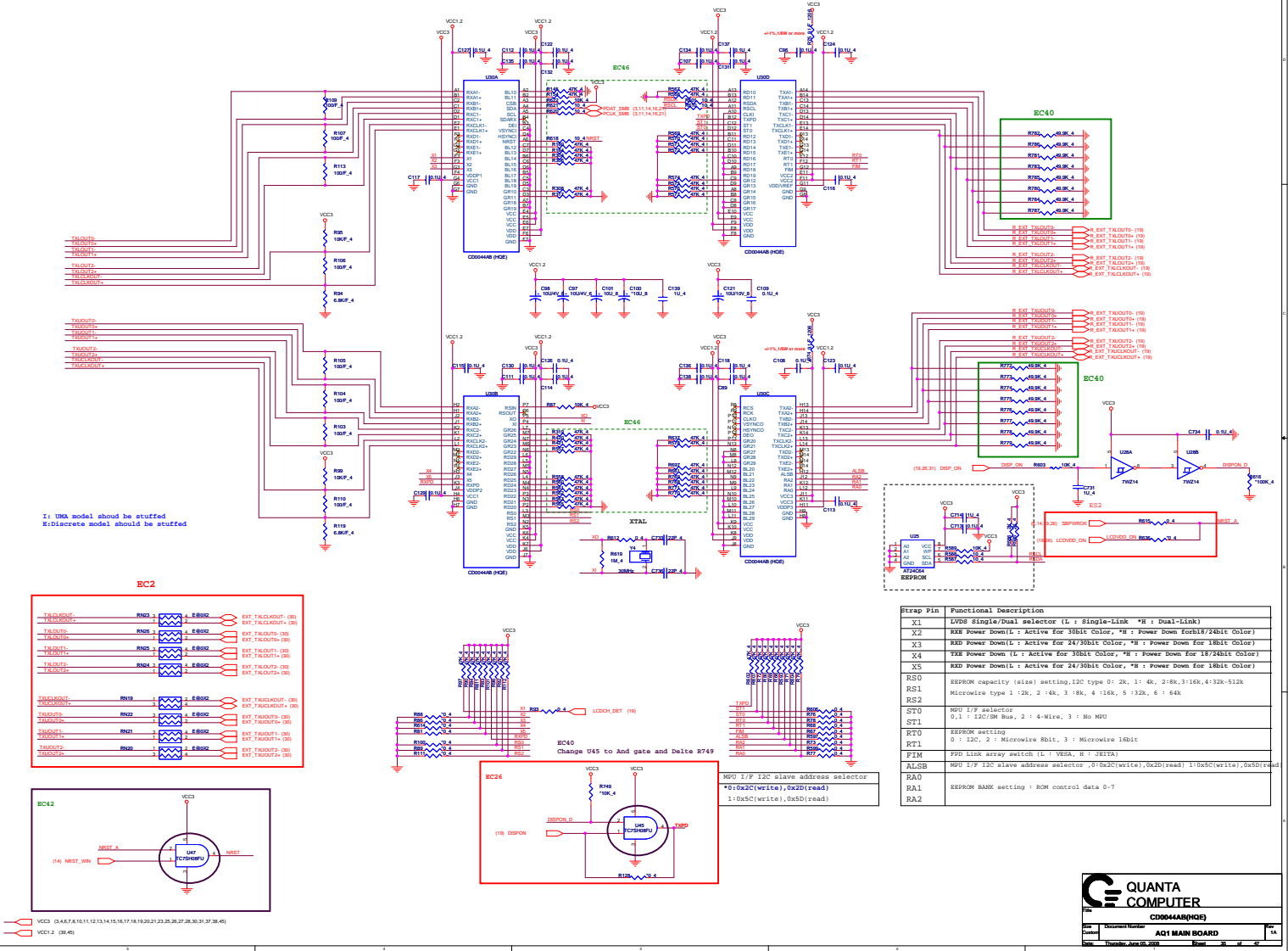
Follow Design Guide DG-03276-001 4.7uFx3 and 0.47x10 uF instead of 0.1uF x10

NB9M: VGACORE +0.90V (Normal) , +1.09V

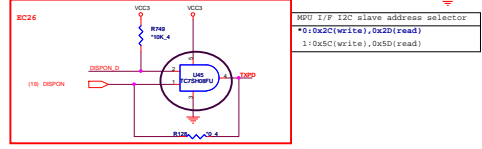
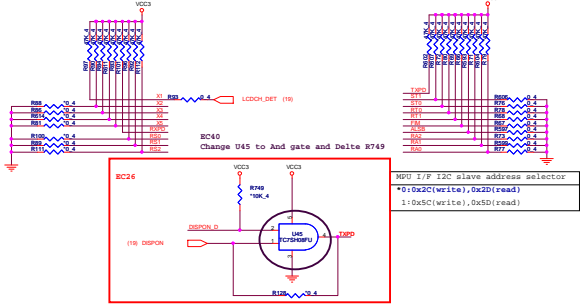
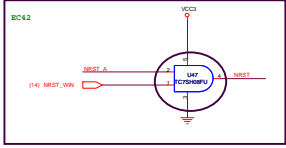
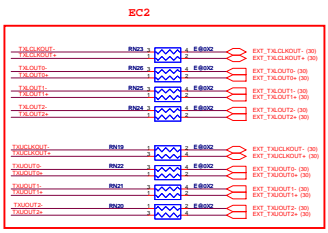


VGA_CORE (42,45)

AA11	GND_1	E15
AA12	GND_2	E18
AA13	GND_3	E24
AA14	GND_4	E27
AA15	GND_5	E30
AA16	GND_6	E6
AA17	GND_7	E101
AA18	GND_8	E2
AA19	GND_9	GND_104
AA20	GND_10	F34
AA21	GND_11	F2
AA22	GND_12	GND_106
AA23	GND_13	J31
AA24	GND_14	GND_108
AA25	GND_15	J5
AA26	GND_16	GND_109
AA27	GND_17	GND_110
AA28	GND_18	L1
AA29	GND_19	L11
AA30	GND_20	L12
AA31	GND_21	M11
AA32	GND_22	M12
AA33	GND_23	M13
AA34	GND_24	M14
AA35	GND_25	M15
AA36	GND_26	M16
AA37	GND_27	M17
AA38	GND_28	M18
AA39	GND_29	M19
AA40	GND_30	M2
AA41	GND_31	M21
AA42	GND_32	M22
AA43	GND_33	M23
AA44	GND_34	M24
AA45	GND_35	M25
AA46	GND_36	M26
AA47	GND_37	M27
AA48	GND_38	M28
AA49	GND_39	M29
AA50	GND_40	M30
AA51	GND_41	M31
AA52	GND_42	M32
AA53	GND_43	M33
AA54	GND_44	M34
AA55	GND_45	M35
AA56	GND_46	M36
AA57	GND_47	M37
AA58	GND_48	M38
AA59	GND_49	M39
AA60	GND_50	M40
AA61	GND_51	M41
AA62	GND_52	M42
AA63	GND_53	M43
AA64	GND_54	M44
AA65	GND_55	M45
AA66	GND_56	M46
AA67	GND_57	M47
AA68	GND_58	M48
AA69	GND_59	M49
AA70	GND_60	M50
AA71	GND_61	N14
AA72	GND_62	N15
AA73	GND_63	N16
AA74	GND_64	N17
AA75	GND_65	N18
AA76	GND_66	N19
AA77	GND_67	N20
AA78	GND_68	N21
AA79	GND_69	N22
AA80	GND_70	N23
AA81	GND_71	N24
AA82	GND_72	N25
AA83	GND_73	N26
AA84	GND_74	N27
AA85	GND_75	N28
AA86	GND_76	N29
AA87	GND_77	N30
AA88	GND_78	N31
AA89	GND_79	N32
AA90	GND_80	N33
AA91	GND_81	N34
AA92	GND_82	N35
AA93	GND_83	N36
AA94	GND_84	N37
AA95	GND_85	N38
AA96	GND_86	N39
AA97	GND_87	N40
AA98	GND_88	N41
AA99	GND_89	N42
AA100	GND_90	N43
AA101	GND_91	N44
AA102	GND_92	N45
AA103	GND_93	N46
AA104	GND_94	N47
AA105	GND_95	N48
AA106	GND_96	N49
AA107	GND_97	N50
AA108	GND_98	N51
AA109	GND_99	N52
AA110	GND_100	N53
AA111	GND_101	N54
AA112	GND_102	N55
AA113	GND_103	N56
AA114	GND_104	N57
AA115	GND_105	N58
AA116	GND_106	N59
AA117	GND_107	N60
AA118	GND_108	N61
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AA155	GND_145	N98
AA156	GND_146	N99
AA157	GND_147	N100
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AA161	GND_151	N104
AA162	GND_152	N105
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AA317	GND_307	N260
AA318	GND_308	N261
AA319	GND_309	N262
AA320	GND_310	N263
AA321	GND_311	N264
AA322		



I: U9A model should be stuffed
 S: Discrete model should be stuffed




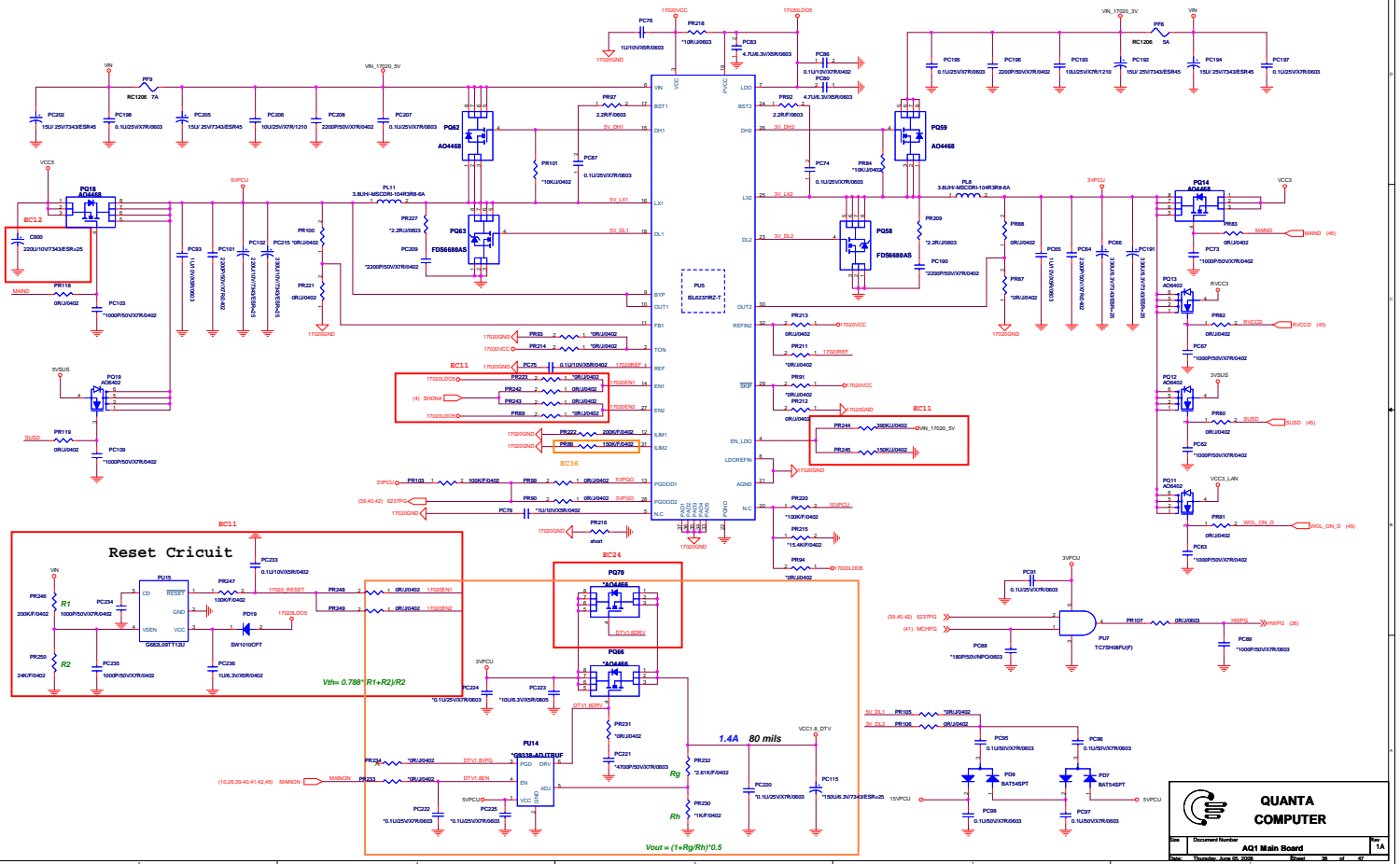
Strap Pin	Functional Description
X1	I2S Single/Dual selector (L: Single-Link "H": Dual-Link)
X2	RAM Power Down(L: Active for 38Bit Color, "H": Power Down for 18/19/38Bit Color)
X3	RAM Power Down(L: Active for 24/38Bit Color, "H": Power Down for 18/19/38Bit Color)
X4	RAM Power Down(L: Active for 38Bit Color, "H": Power Down for 18/19/38Bit Color)
X5	RAM Power Down(L: Active for 24/38Bit Color, "H": Power Down for 18/19/38Bit Color)
RS0	EEPROM capacity (eisel setting, I2C type 0: 2k, 1: 4k, 2: 8k, 3: 16k, 4: 32k-512k)
RS1	Microwire type 1: 2k, 2: 4k, 3: 8k, 4: 16k, 5: 32k, 6: 64k
ST0	MPU I/F selector
ST1	0: 1: I2C/SPI Bus, 2: 4-Wire, 3: No MPU
RT0	EEPROM setting
RT1	0: 1: I2C, 2: Microwire Sbit, 3: Microwire 16bit
FRM	FDI Link array switch (L: YES, "H": YES)
ALCSB	MPU I/F I2C slave address selector -S1:0x5C(write), 0x5D(read)
BA0	EEPROM BANK setting: ROM control data 0-7
RA1	
RA2	

QUANTA COMPUTER

CD0044AB(HQE)

AG1 MAIN BOARD

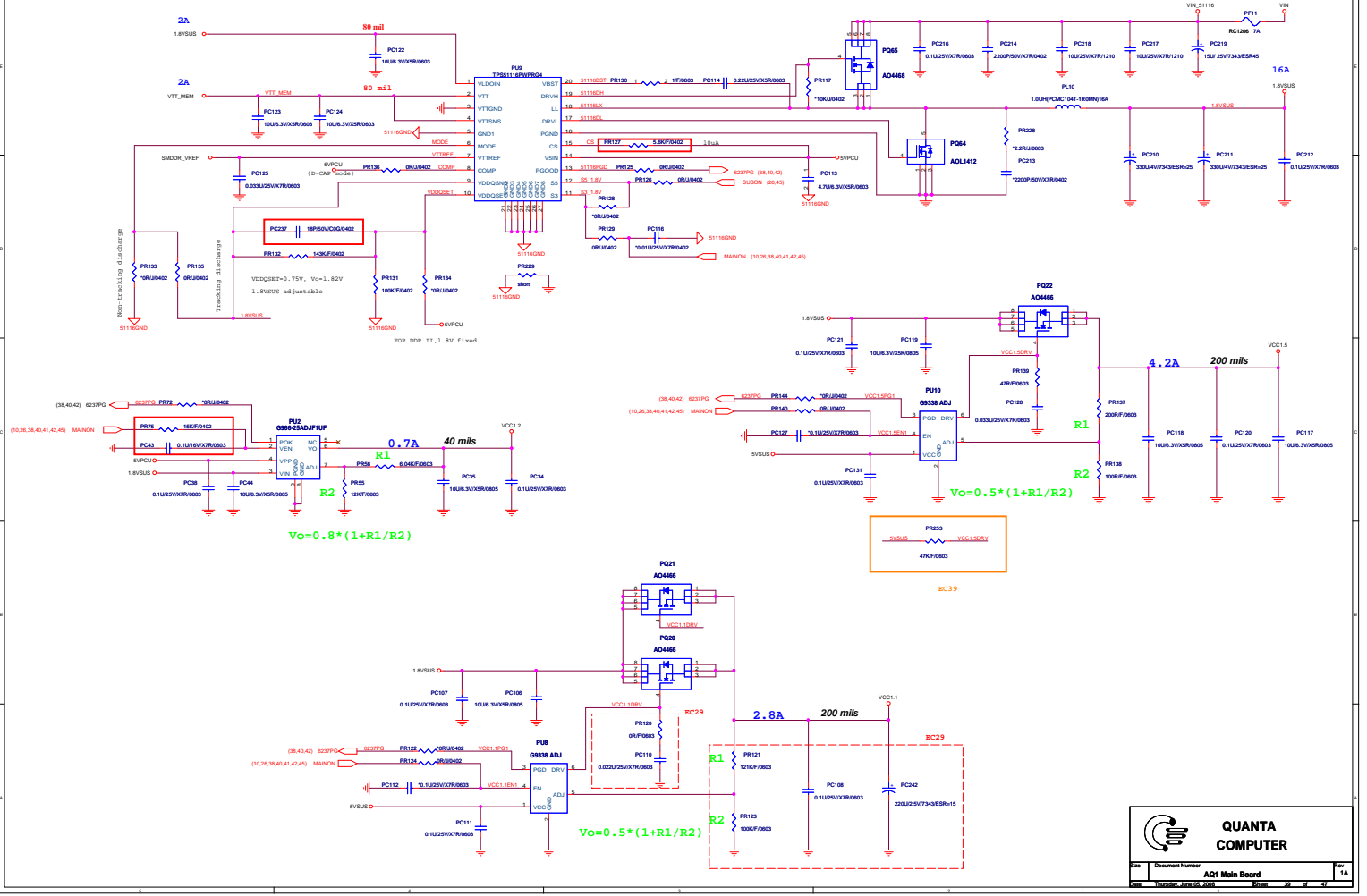
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Doc	Document Number	Rev	LA
	AQ1 MAIN BOARD		
Date	Thursday, June 05, 2008	Sheet	18 of 47

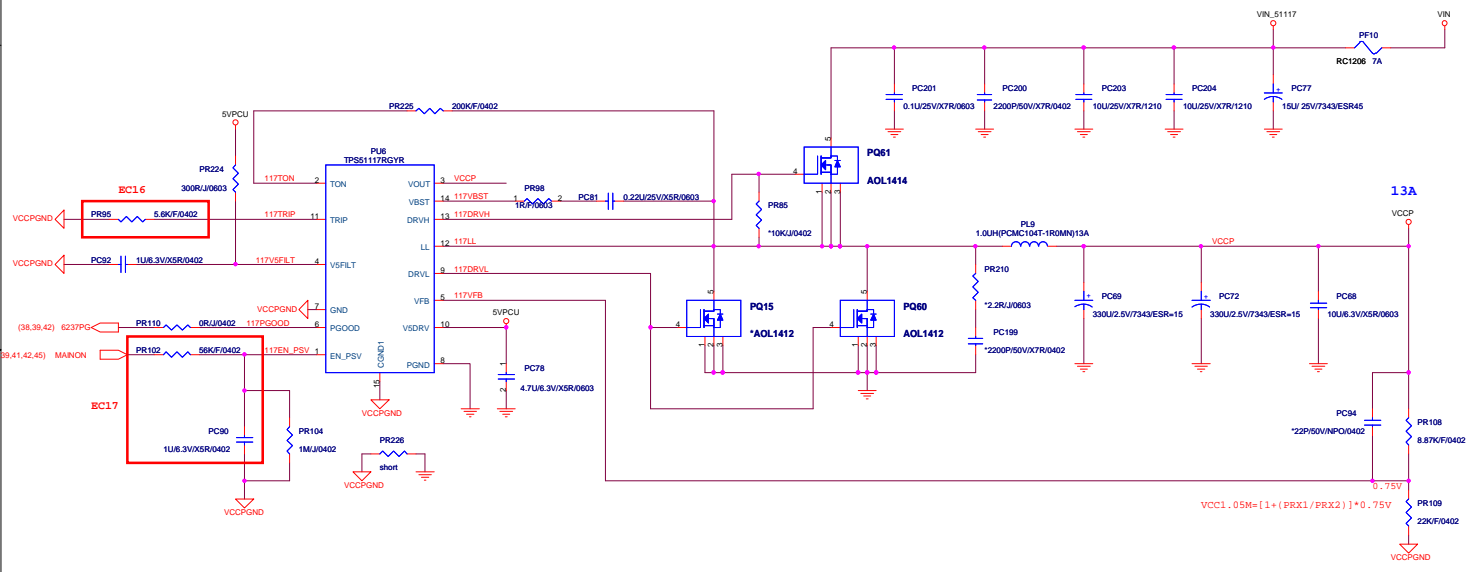


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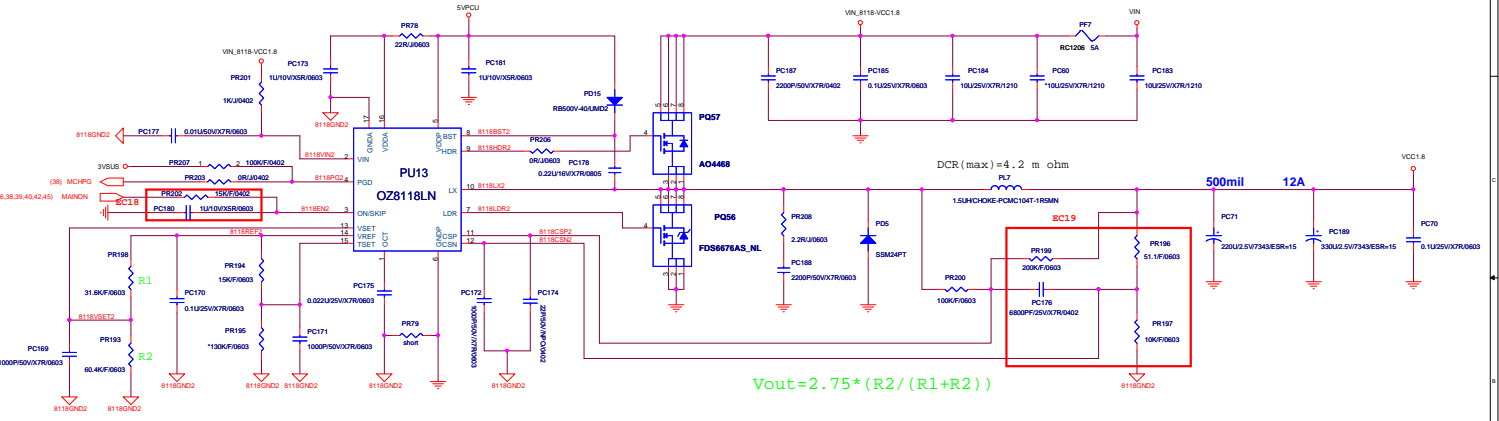
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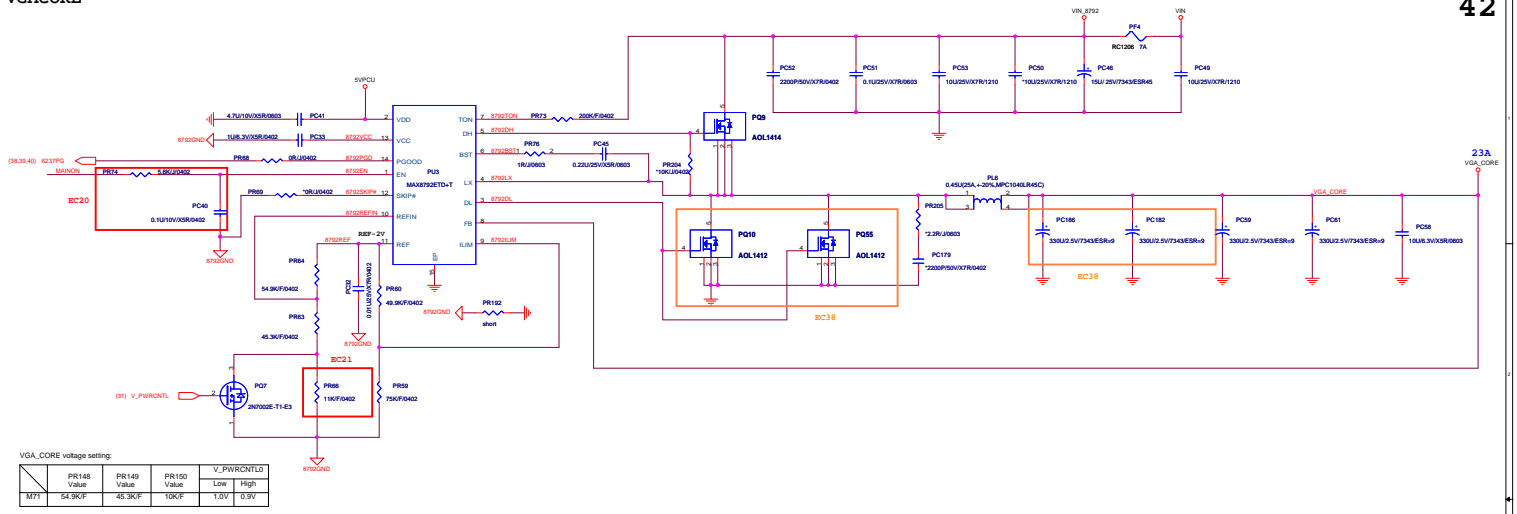
$$V_{out} = 2.75 * (R2 / (R1 + R2))$$

QUANTA COMPUTER

Document Number: **AQ1 Main Board**

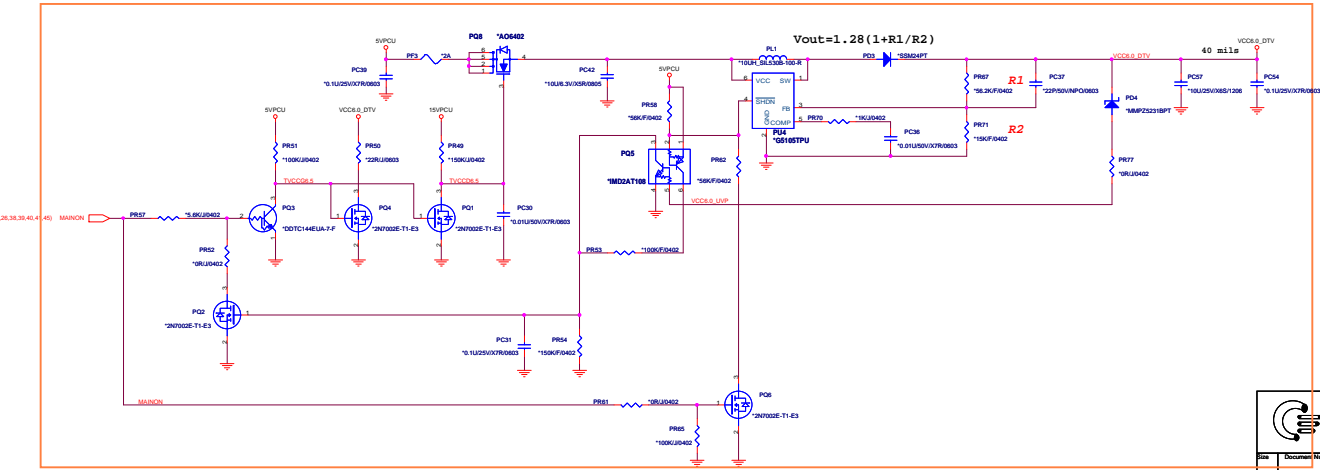
Date: **Thursday, June 05, 2008**

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VGA_CORE voltage setting:

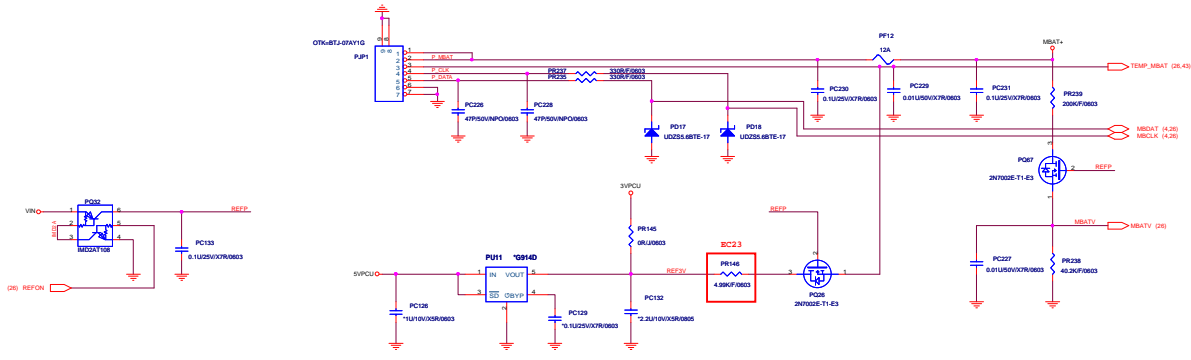
	PR140 Value	PR142 Value	PR150 Value	V_PWRCONTLO	
MPT	54.3KΩ	45.3KΩ	10KΩ	Low	High
				1.0V	0.5V



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Doc: _____ Date: _____ Title: _____



TEMP_MBAT voltage :

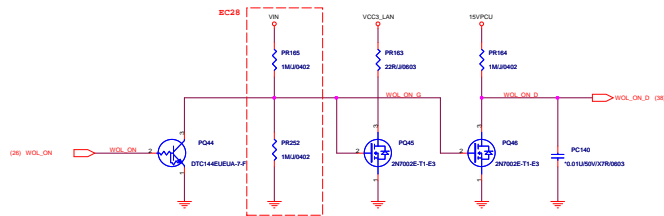
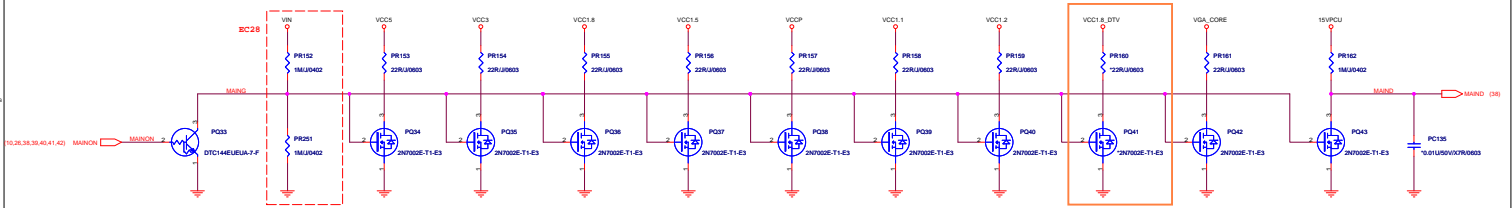
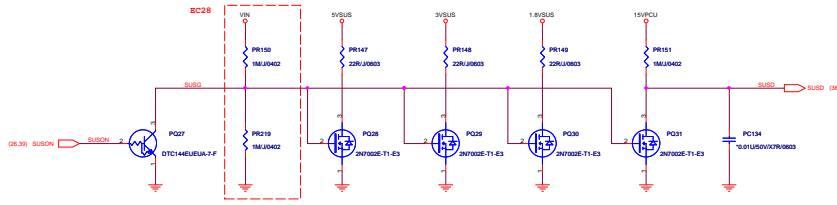
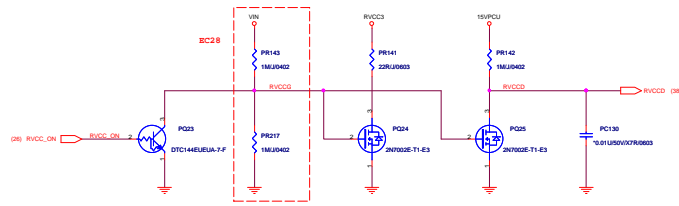
	System Off	System On
Battery	0V	1.6V
Adapter	3.3V	3.3V
Battery+Adapter	1.6V	1.6V

MBATV voltage :

Li-Ion 48*P	$16.8V * 40.2 / (200 + 40.2) = 2.812V$
NI-MH 8S1P	$12.0V * 40.2 / (200 + 40.2) = 2.008V$
NI-MH 8S1P	$8.0V * 40.2 / (200 + 40.2) = 1.34V$

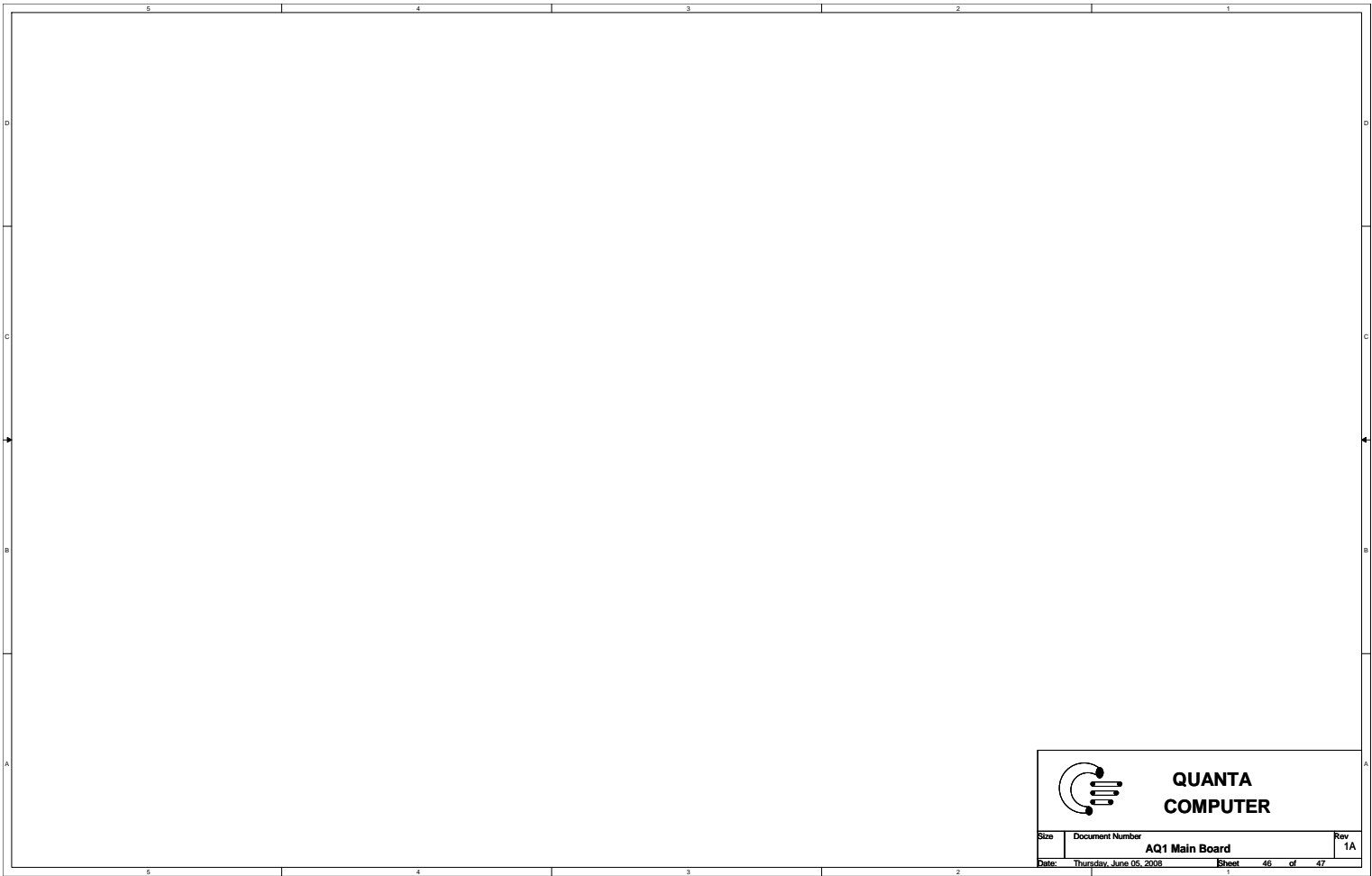
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