

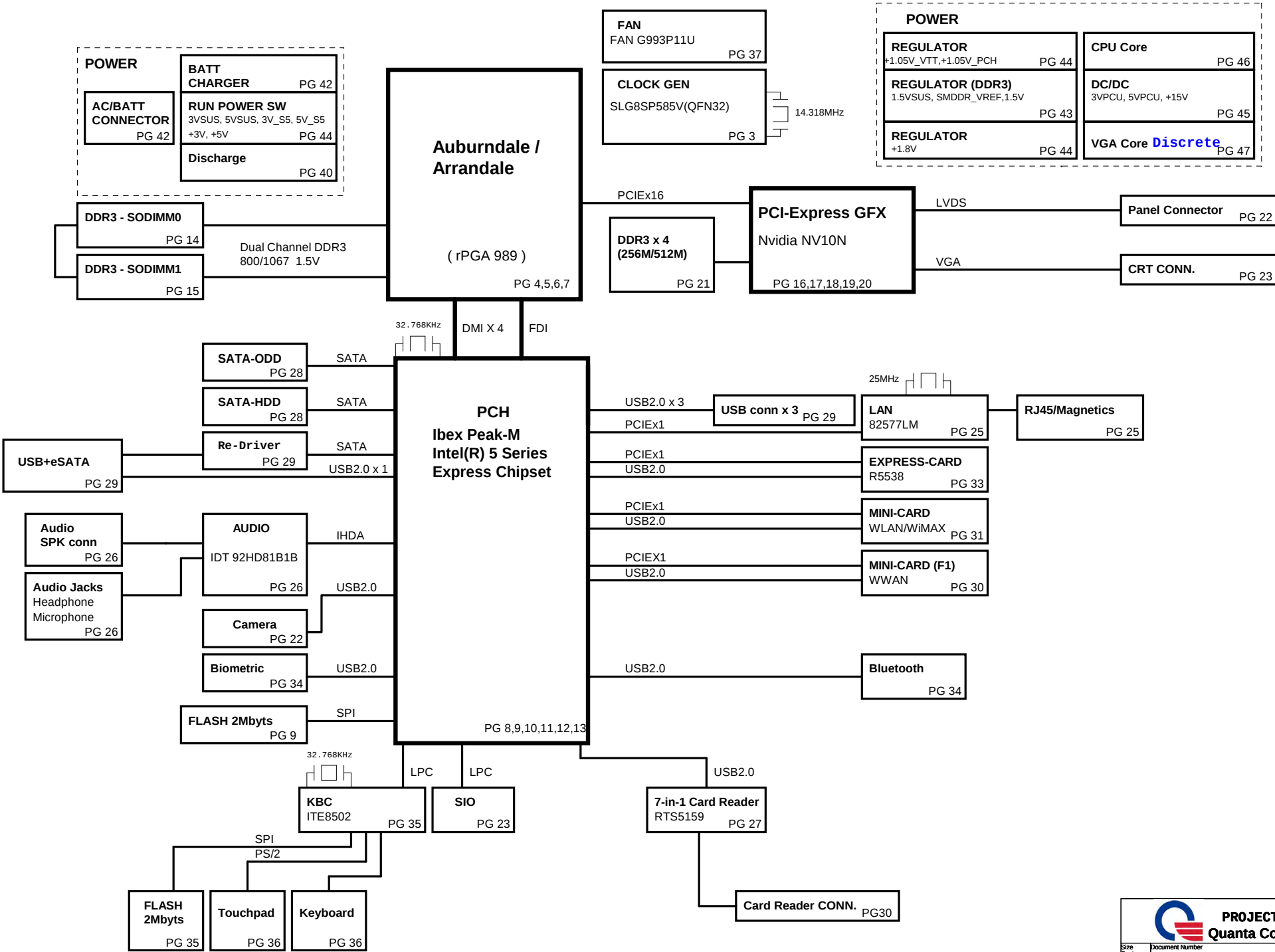


Table of Contents

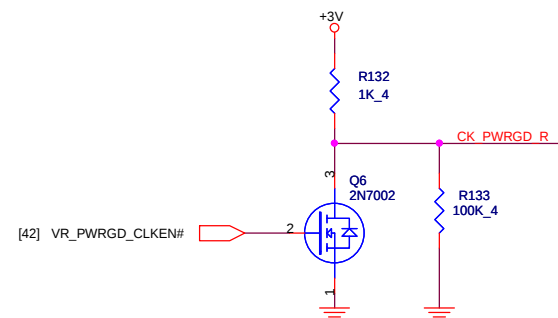
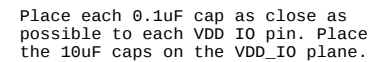
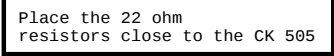
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3	CLOCK GENERATOR
4-7	Auburndale CPU
8-13	Ibex Peak-M
14-15	DDRIII SO-DIMM
16-22	Discreate VGA (M92-XT)
23	LCD + Camera Conn.
24	HDMI Conn.
25	CRT Conn.
26	Audio Codec ALC269
27	RTL8111DL
28	SATA HDD & ODD
29	USB x 2 & ESATA
30	USB X2/SIM_CARD/LEDs/RF
31	MINI-Card (UWB & WWAN)
32	MINI-Card (WLAN)
33	ONFI
34	Express Card
35	K/B & T/P
36	BLUETOOTH
37	FAN & Thermal
38	G-Sensor
39	B To B Conn.
40	iTPM & RFID EEPROM
41	KBC IT8502E
42	HOLD & SKEW
43	Discharge
44	Charger
45	DDR3 (TPS5116REGR)
46	1.05V_VTT & 1.05_PCH (RT8204)
47	3V/5V (MAX17101)
48	CPU (MAX17082)
49	DIS_GFX_VCC (MAX8792)
50	DIS_1.8V_RUN (OZ8116LN)
51	Power Block Dianram
52	XDP
53	Revision & Schematic Value Description
54	BOM Matrix Table

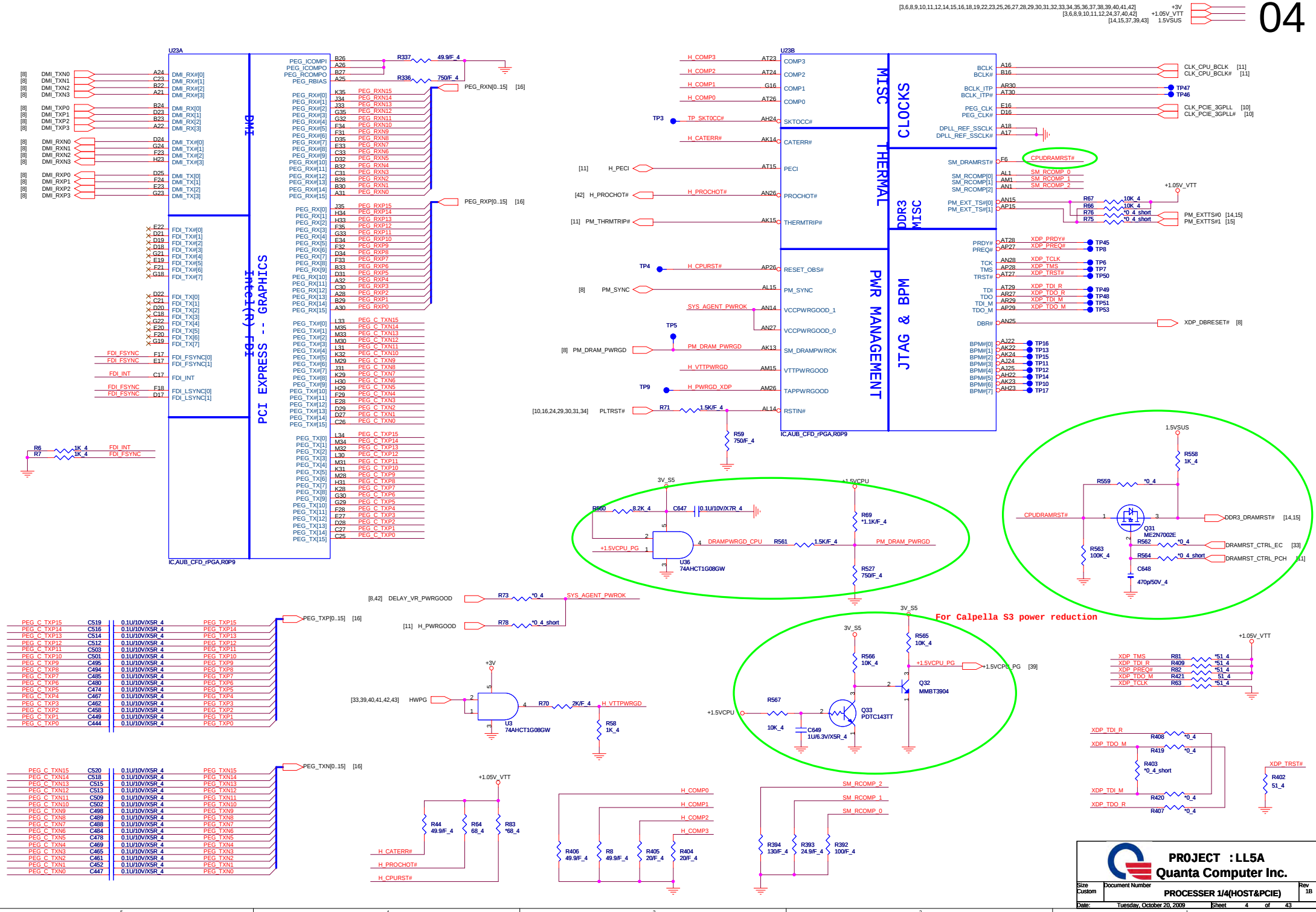
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	23,32,43,44,45,46,47,48,49,50	MAIN POWER		S0-S5
+3VRTC	+3.0V~+3.3V	9,12,41	RTC		S0-S5
3VPCU	+3.3V	9,23,27,30,32,35,39,41,43,44,47	ITE8052 POWER	3V5V_EN	S0-S5
5VPCU	+5V	14,43,44,45,46,47,49,50	DC/DC POWER IC SOURCE	3V5V_EN	S0-S5
+15V	+15V	23,38,43,45,46,47	LARGE POWER	3V5V_EN	S0-S5
LANVCC	+3.3V	27,43	LAN POWER	LAN_ON	
5V_S5	+5V	12,29,30,43	PCH SUS POWER	S5_ON	S0-S3
3V_S5	+3.3V	8,9,10,11,12,43,52	Sys Management,PCH Resume Well, Intel HD Audio,USB,WLAN WiMAX POWER	S5_ON	S0-S3
5VSUS	+5V	23,39,43,48	SLP_S4# CTRLD POWER	SUSON	S0-S3
3VSUS	+3.3V	14,15,30,34,41,43,49	SLP_S4# CTRLD POWER	SUSON	S0-S3
1.5VSUS	+1.5V	4,6,14,15,43,45,46,49,50	SODIMM POWER	SUSON	S0-S3
0.75VSMDDR_VTERM	+0.75V	14,15,43,45	DDR3 SODIMM REFERENCE POWER	MAIN_ON	S0
+5V	+5V	12,18,23,24,25,26,28,35,37,41,43,44	SLP_S3# CTRLD POWER	MAIN_ON	S0
+3V	+3.3V	3,4,8,9,10,11,12,14,15,17,23,25,26,27,28,29,30,31,32,33,34,36,37,38,39,40,41,43,44,45,46,47,48,50,52	SLP_S3# CTRLD POWER	MAIN_ON	S0
+1.8V	+1.8V	6,12,17,18,21,22,33,43,50	LVDS,NVM POWER	MAIN_ON	S0
+1.5V	+1.5V	12,18,19,20,31,32,34,45,46	Mini PCIe,Express Card POWER	MAIN_ON	S0
+1.05V_VTT	+1.05V	4,6,11,12,43,46,48,52	AuBurndale VTT POWER	MAIN_ON	S0
+1.05V_PCH	+1.05V	3,10,12,43,46,52	PCH CORE POWER	1.05V_RUN_ON	S0
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,43,49	VGA CORE POWER	GFXVR_EN	S0
VCC_CORE		6,43,48	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	23	LCD Power	ENVDD	S0
+5V_ODD	+5V	28	ODD Power	MAIN_ON	S0
+5V_HDD	+5V	28	HDD Power	MAIN_ON	S0
BAT-V	+10V~+17V	44	MAIN BATTERY	CHG_PBATT	S0-S5



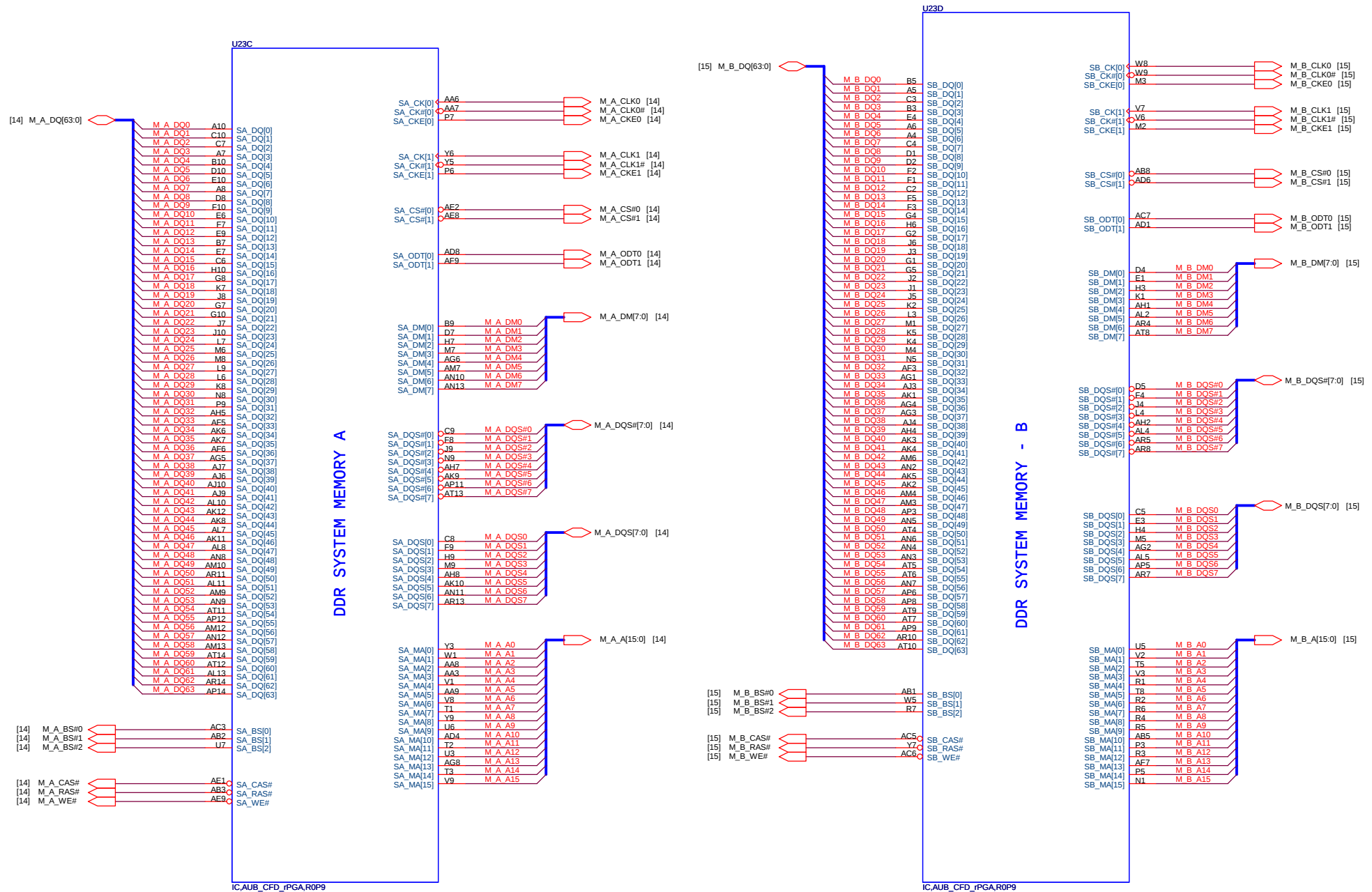
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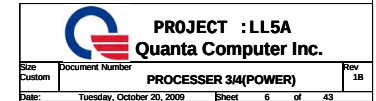
AUBURNDALE PROCESSOR (DDR3)

05



PROJECT : LL5A
Quanta Computer Inc.

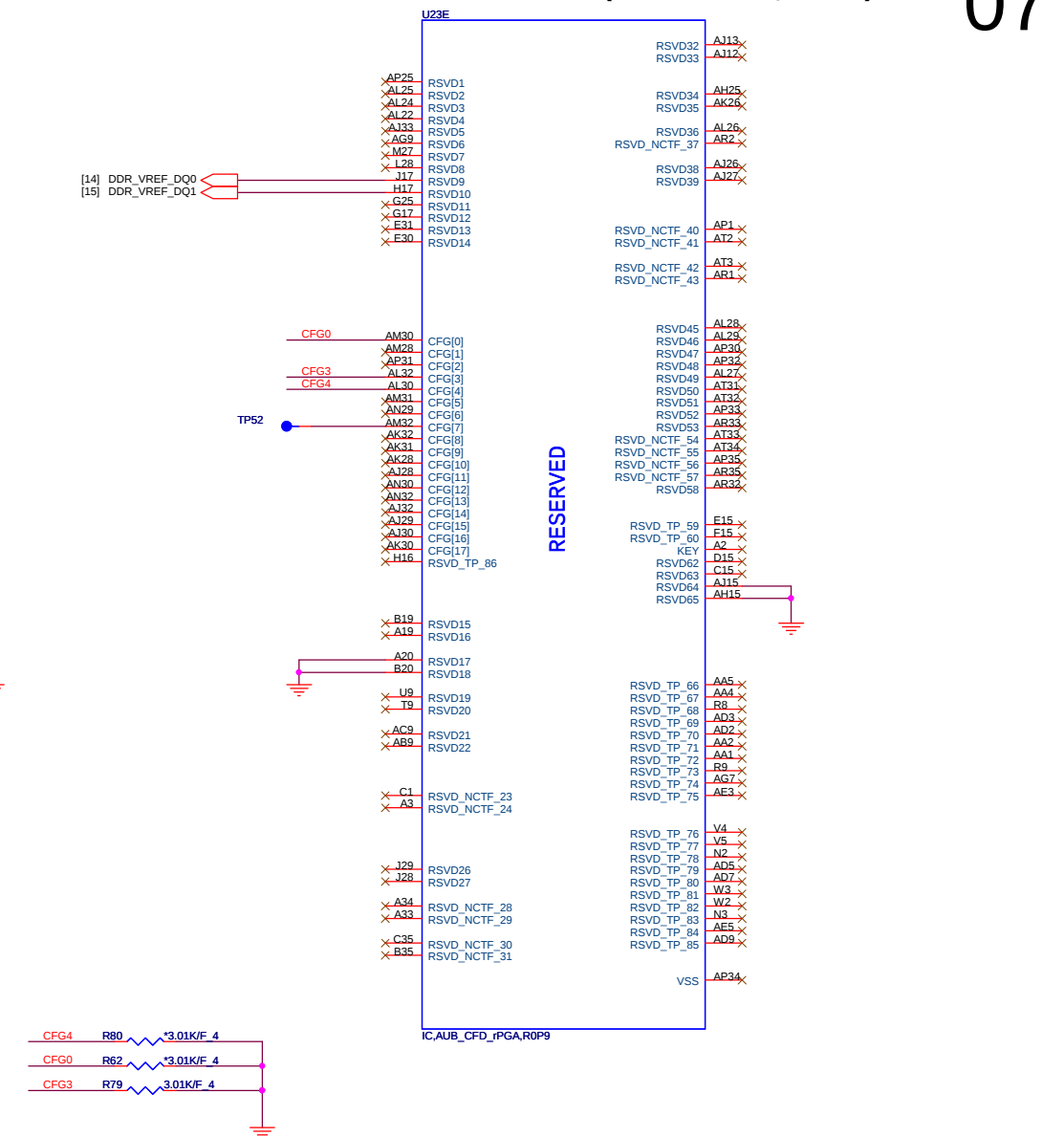
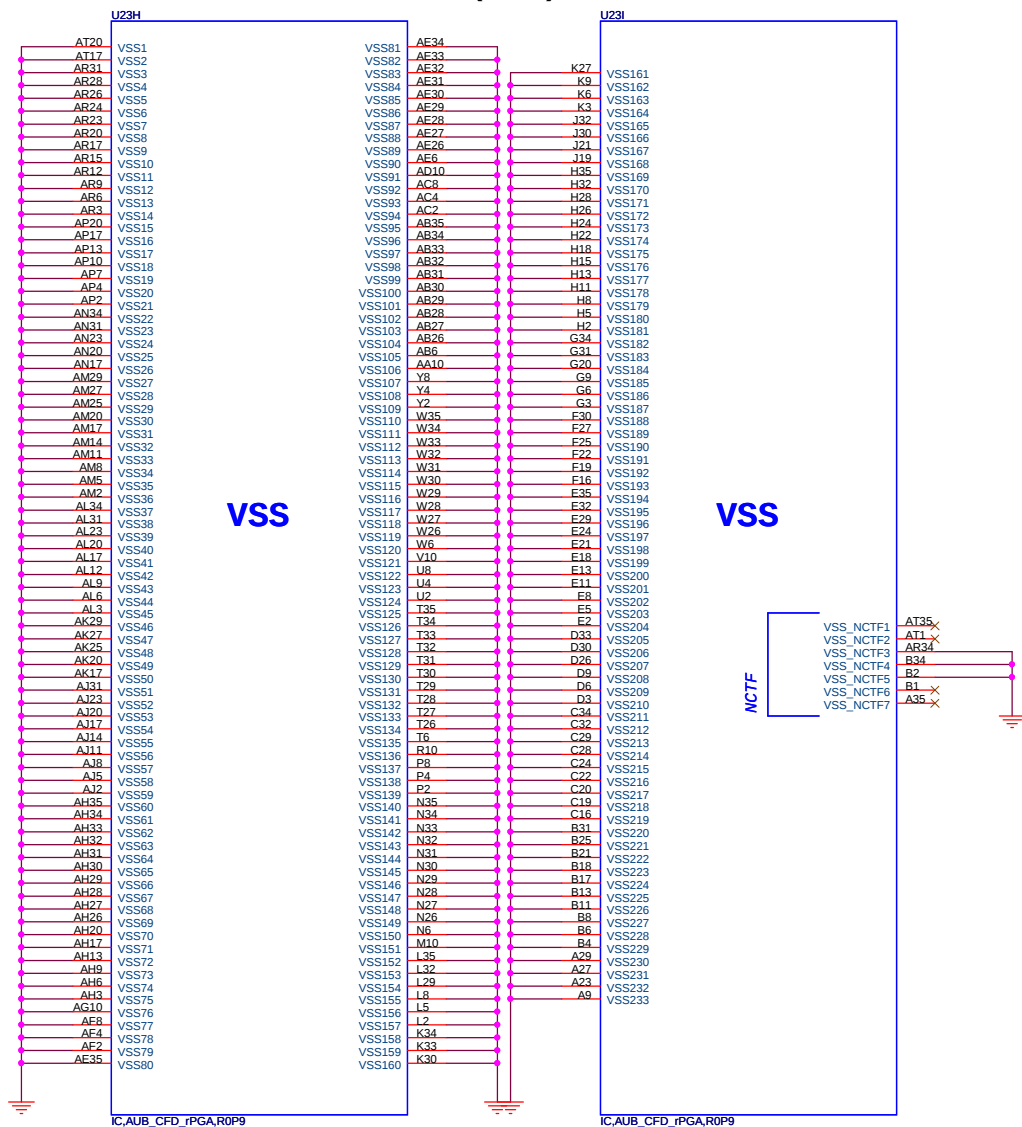
Size	Document Number	Rev
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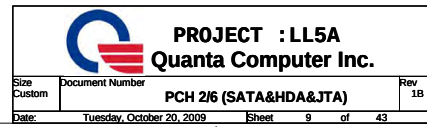
AUBURNDALE PROCESSOR (GND)

AUBURNDALE PROCESSOR(RESERVED, CFG)

07



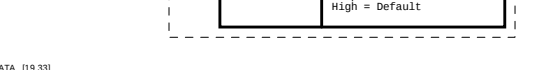
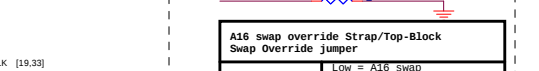
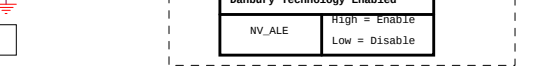
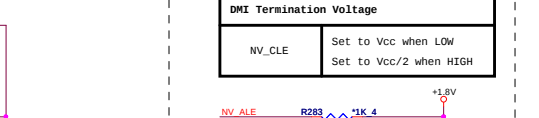
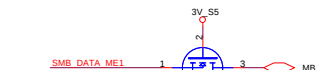
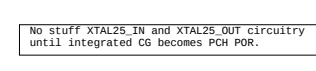
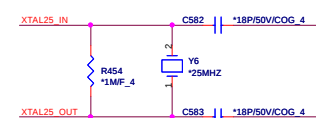
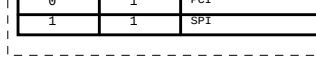
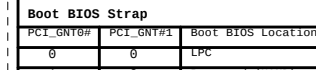
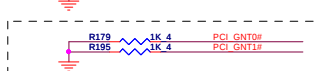
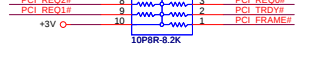
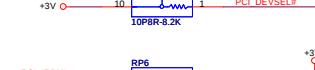
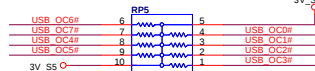
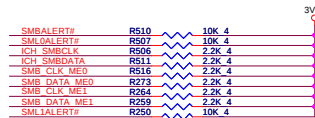
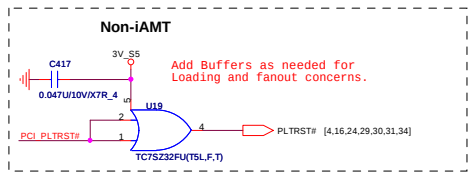
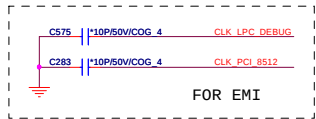
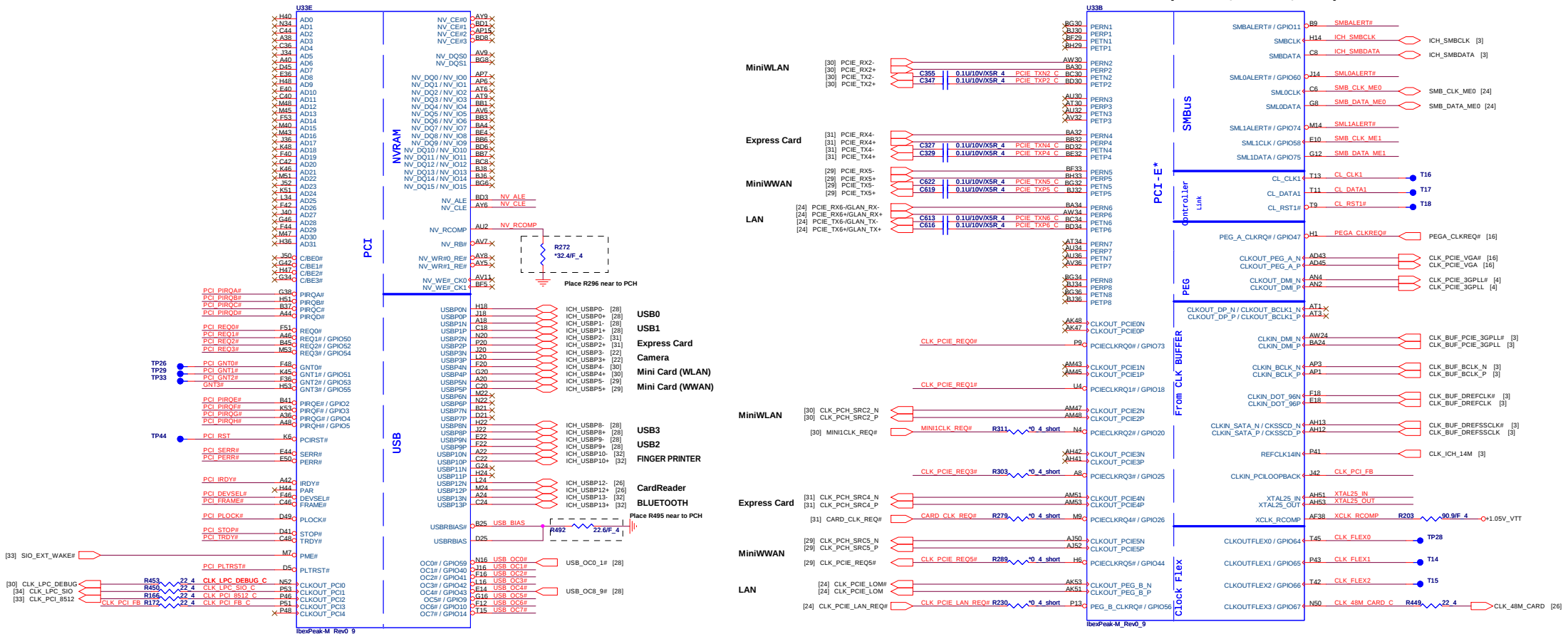
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed



IBEX PEAK-M (PCI, USB, NVRAM)

IBEX PEAK-M (PCI-E, SMBUS, CLK)

10



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

[3,4,6,8,9,10,12,14,15,16,18,19,22,23,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42]

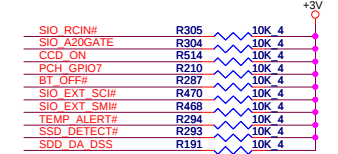
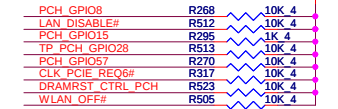
+3V

[4,8,9,10,12,24,30,37]

3V_S5

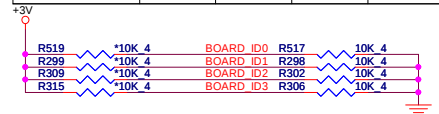
[3,4,6,8,9,10,12,24,37,40,42]

11



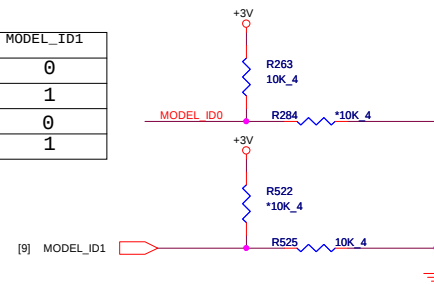
Board ID

Board ID For Function	ID3 GPIO39	ID2 GPIO38	ID1 GPIO37	ID0 GPIO36
SDV	0	0	0	0
SIV	0	0	0	1
SIT	0	0	1	0
SVT	0	0	1	1
SOVP	0	1	0	0



Model ID

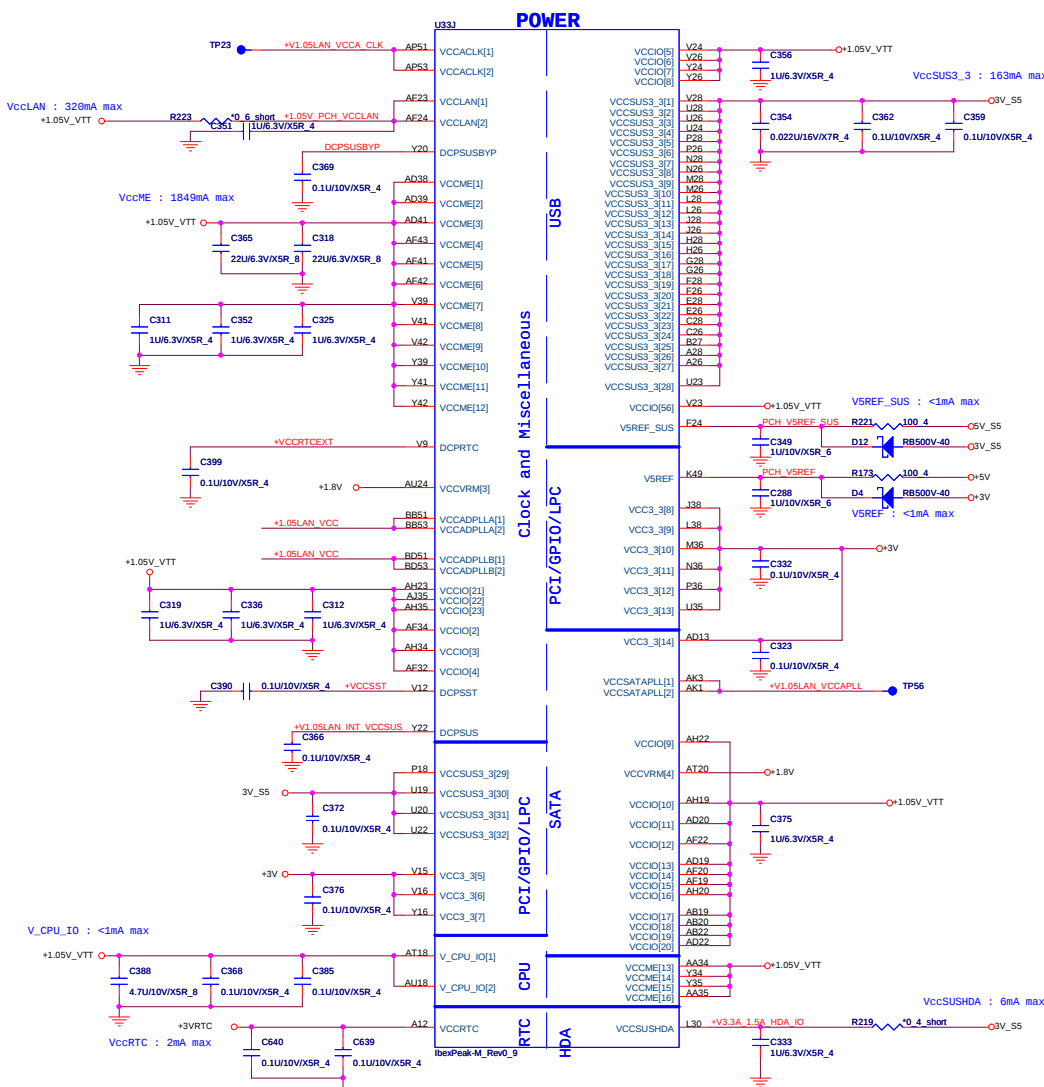
Model ID	MODEL_ID0	MODEL_ID1
Default	0	0
LL3/LL3A	0	1
LL5/LL5A	1	0
	1	1

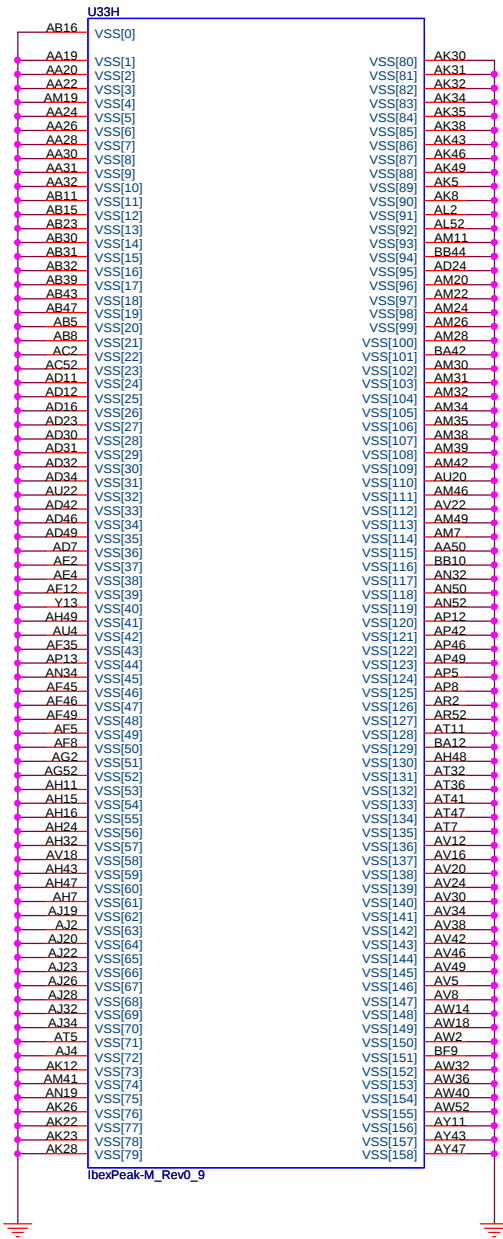


SV_SET_UP 1-X High = Strong (Default)

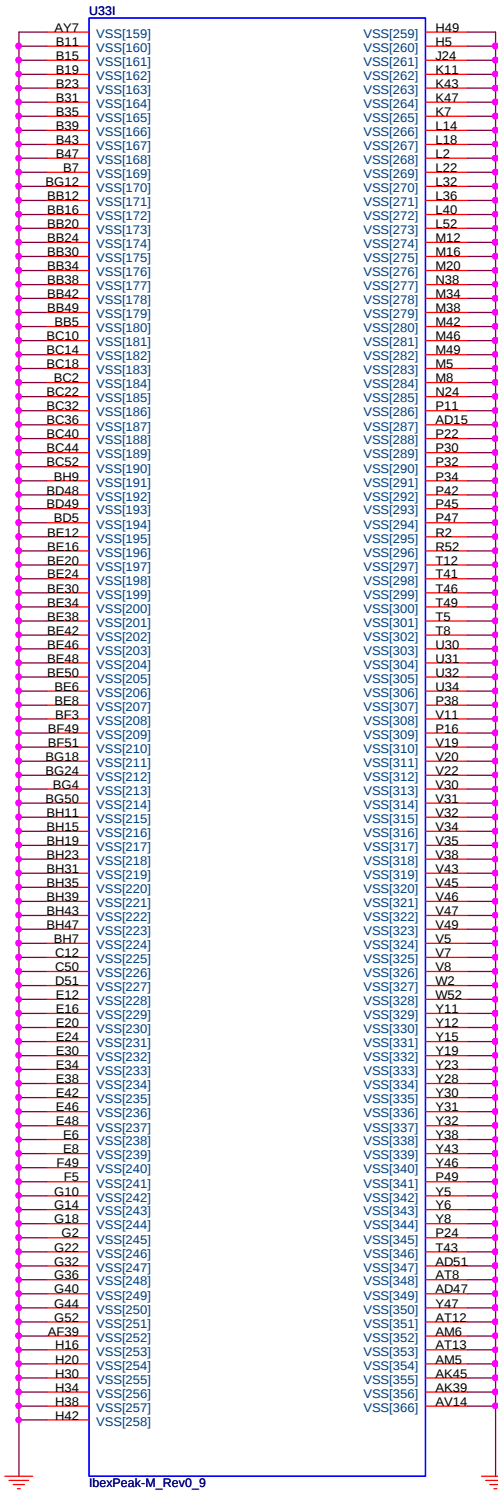
PROJECT : LL5A
Quanta Computer Inc.

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IbexPeak-M_Rev0_9

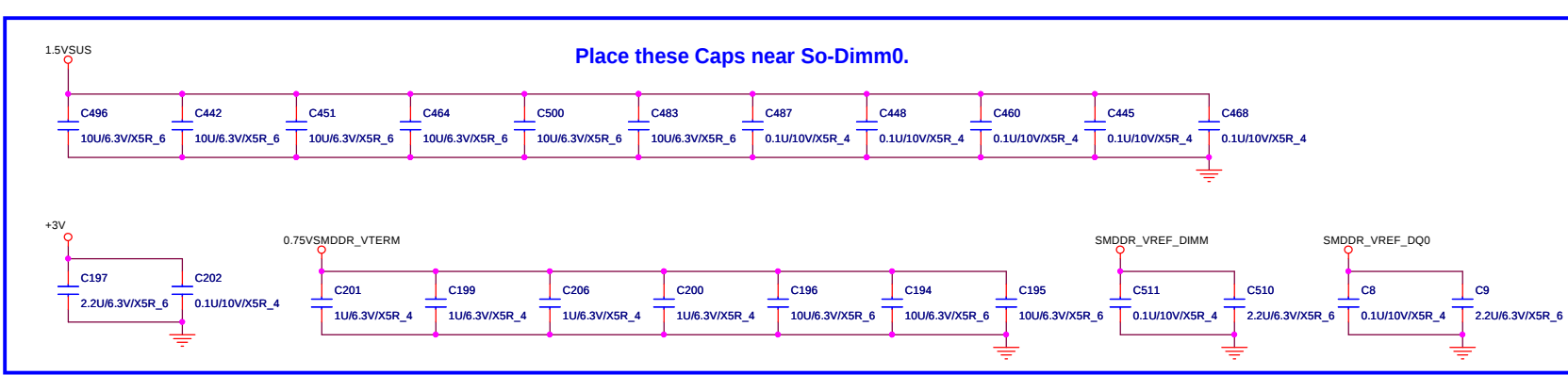
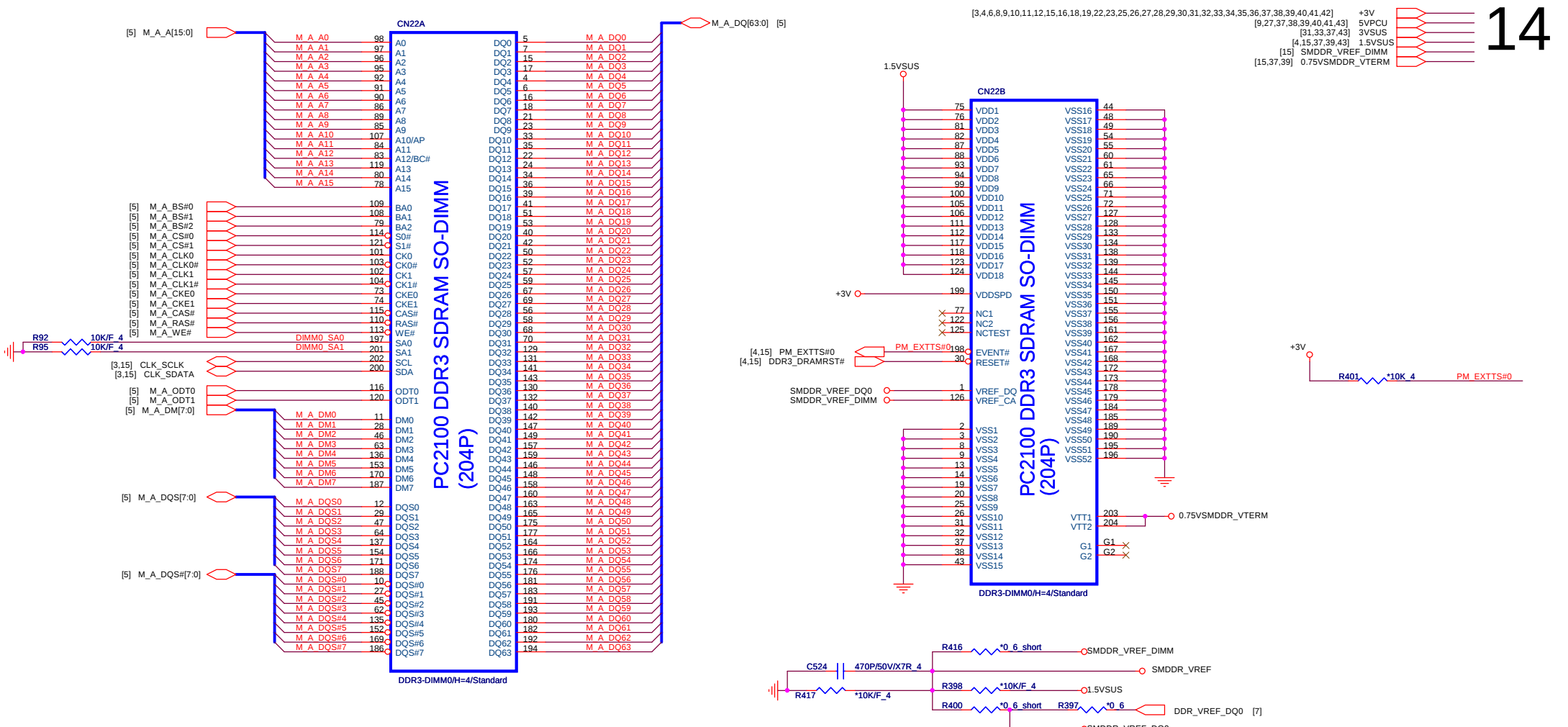


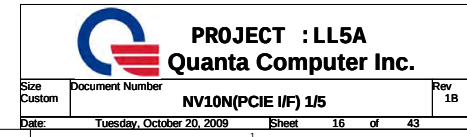
IbexPeak-M_Rev0_9

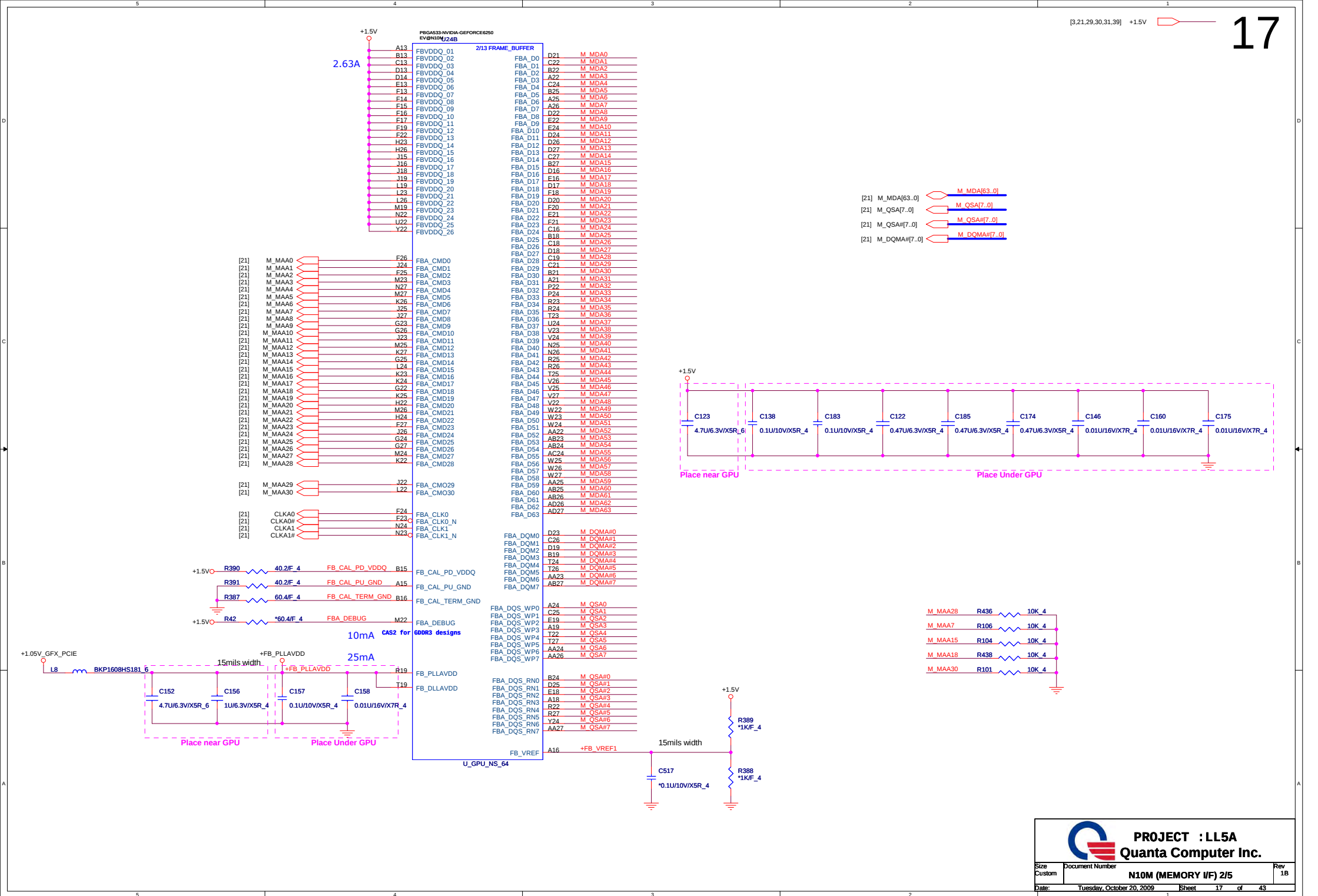


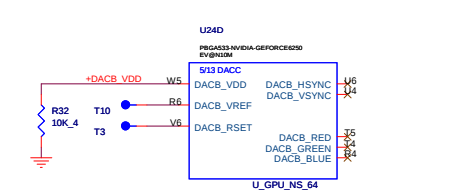
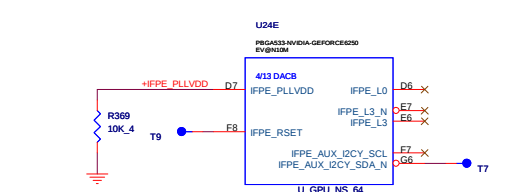
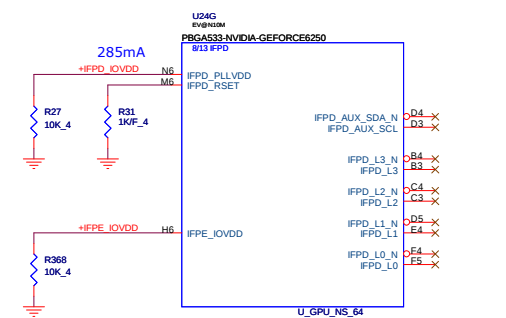
PROJECT : LL5A
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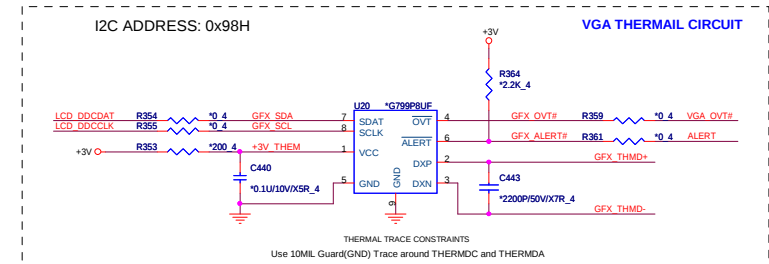
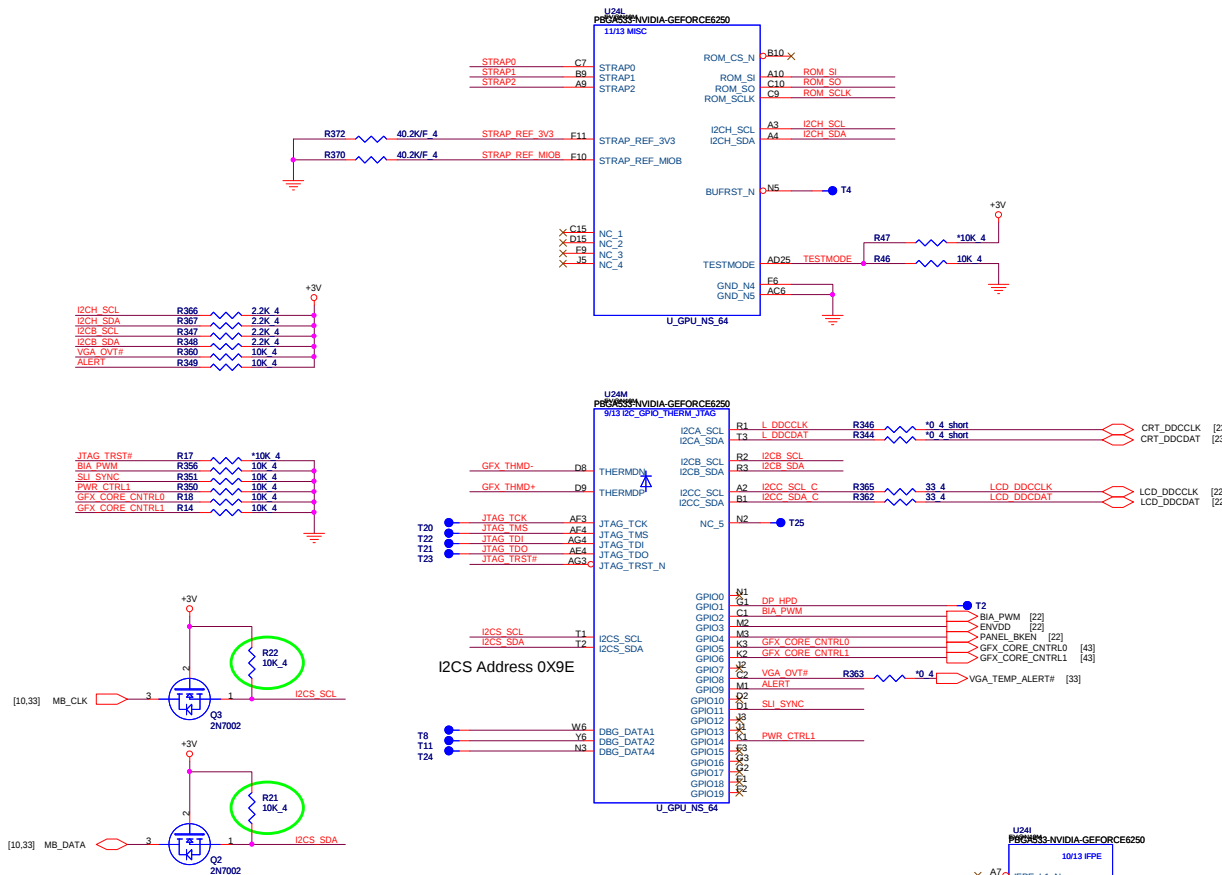
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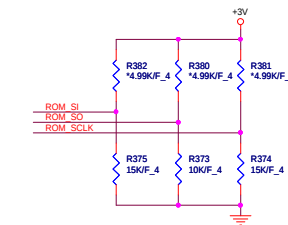


LL5A STRAP FUNCTION MAPPING

USER[3:0]: 1111	EDID is used
3GIO_PADCFG[3:0]: 0001	NoteBook
PCI_DEVID[3:0]: 0001	
SUB_VENDOR: 0	No Vedio BIOS ROM
SLOT_CLK_CLG: 1	GPU AND MCH USE COMMON REF CLOCK
PEX_PLL_EN_TERM: 0	DISABLE PEX_PLL TERMINATION
RAMCFG[3:0]: 0010 AND 0011	
XCLK_417: 0	277MHz(Default)
FB_0_BAR_SIZE: 0	256MB(Default)
SMB_ALT_ADDR: 0	0x9E(Default)
VGA_DEVICE: 1	VGA device(Default)

ROM_SI	RAMCFG LSIT:
PD R9064:20K/F	0011 SAMSUNG K4W1G1646E-HC12 64M16b * 4PCS
PD R9064:15K/F	0010 HYNIX H5TQ1G63BFR-12C 64M16b * 4PCS

PCI_DEVID[4] / SUBVENDOR



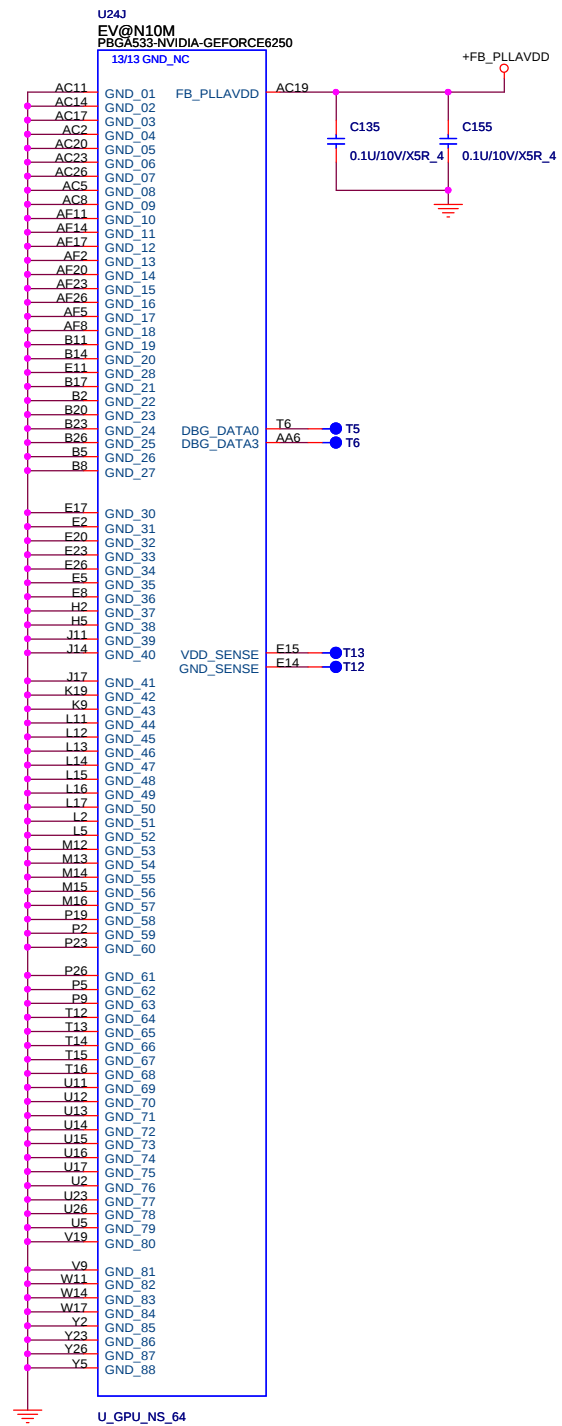
Logical Strap Bit Mapping

Straps	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

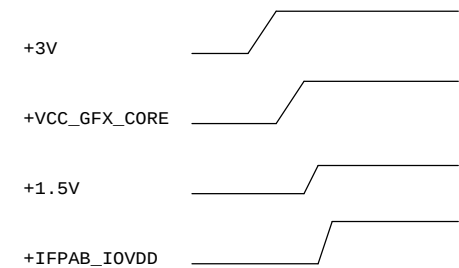
GPIO ASSIGNMENTS

GPIO	NB9X	N10X	I/O	ACTIVE	Function Description
0	General Purpose	General Purpose	I/O	N/A	Hot Plug Detect for IFP Link C
1	HPD-C	HPD-C	I	N/A	Panel Backlight Brightness Control (PWM Capable)
2	LCD0_BL_PWM	LCD0_BL_PWM	O	H	Panel Power Enable
3	LCD0_VDD	LCD0_VDD	O	H	Panel Backlight ON/OFF
4	LCD0_BL_PWM	LCD0_BL_PWM	O	H	Panel Backlight ON/OFF
5	GPU_VID0	GPU_VID0	O	N/A	GPU_VID0
6	GPU_VID1	GPU_VID1	O	N/A	GPU_VID1
7	GPU_VID2/MEM_VID	GPU_VID2	O	N/A	GPU_VID2
8	OVERT	OVERT	I/O	L	Thermal Over Temperature
9	FAN_PWM/ALERT	ALERT	I/O	L	Thermal Alert (PWM Capable)
10	MEM_VREF	MEM_VREF	O	N/A	Memory VREF Switch
11	SLI_SYNC	SLI_SYNC	I/O	L	SLI SYNC
12	AC_DET	PWR_LEVEL (in)	I	N/A	Power Level Detect
13	PWR_CTRL0	MEM_VID (out)	O	L	MEM_VID0
14	PWR_CTRL1	PWR_CTRL1	O	N/A	Power Supply Control
15	HPD-E	HPD-E	I	N/A	Hot Plug Detect for IFP Link E
16	DVL_MODE1	FAN_PWM(out)	O	N/A	Fan PWM Control
17	HDMI_DETECT0	Reserved	N/A	N/A	
18	DVL_MODE1	Reserved	N/A	N/A	
19	HDMI_DETECT1	HPD-D	I	N/A	Hot Plug Detect for IFP Link D

Stamps	NB9X	N10X	Function Description
ROM_SO	XCLK_277 TVMODE(2) TVMODE(1) TVMODE(0)	XCLK_277 TVMODE(2) TVMODE(1) TVMODE(0)	55nm PU 5K/F ohm 40nm PU 10K/F ohm
ROM_SCLK	PCI_DEVID_EXT SUB_VENDOR SLOT_CLK_CFG PEX_PLL_EN_TERM	PCI_DEVID_EXT SUB_VENDOR SLOT_CLK_CFG PEX_PLL_EN_TERM	55nm/40nm PD 15K/F ohm
ROM_SI	RAMCFG(3) RAMCFG(2) RAMCFG(1) RAMCFG(0)	RAMCFG(3) RAMCFG(2) RAMCFG(1) RAMCFG(0)	Hynix PD 15K/F ohm Samsung PD 20K/F ohm
Strap 2	PCI_DEVID(3) PCI_DEVID(2) PCI_DEVID(1) PCI_DEVID(0)	PCI_DEVID(3) PCI_DEVID(2) PCI_DEVID(1) PCI_DEVID(0)	55nm PU 25K/F ohm 40nm/GS PU 10K/F ohm 40nm/GS PU 5K/F ohm 40nm/NS PU 25K/F ohm
Strap 1	3GIO_PADCFG(3) 3GIO_PADCFG(2) 3GIO_PADCFG(1) 3GIO_PADCFG(0)	3GIO_PADCFG(3) 3GIO_PADCFG(2) 3GIO_PADCFG(1) 3GIO_PADCFG(0)	40nm/NS PU 34.9K/F ohm
Strap 0	USER(3) USER(2) USER(1) USER(0)	USER(3) USER(2) USER(1) USER(0)	



power up sequence



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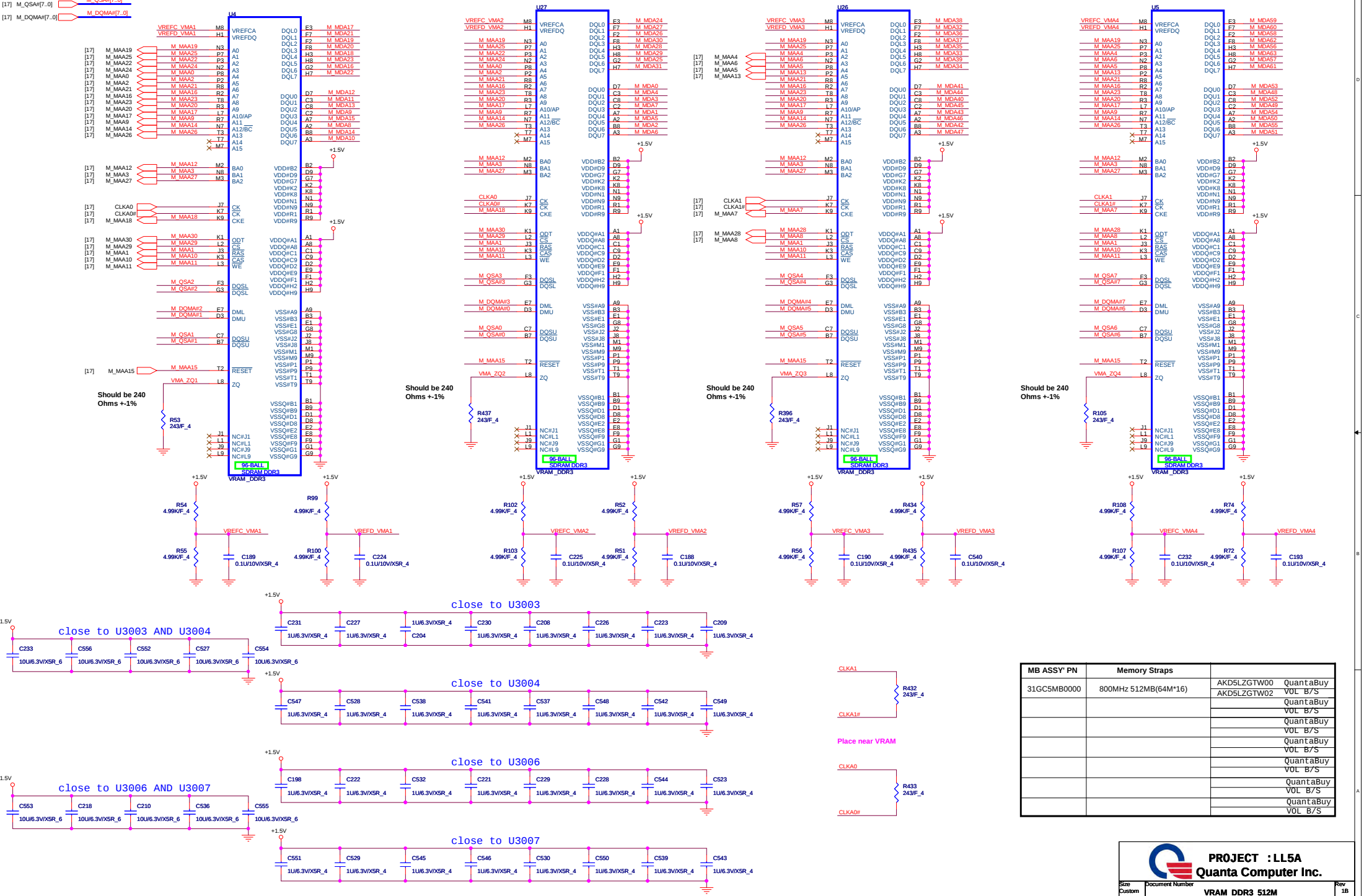
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256MB/ 512MB DDR3

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[3.17,29,30,31,39] +1.5V

- [17] M_MDA[63..0] M_MDA[63..0]
- [17] M_QSA[7..0] M_QSA[7..0]
- [17] M_QSA[7..0] M_QSA[7..0]
- [17] M_QMA[7..0] M_QMA[7..0]



MB ASSY PN	Memory Straps		
31G55MB0000	800MHz 512MB(64M*16)	AKD5LZGTW00	QuantaBuy
		AKD5LZGTW02	VOL B/S
			QuantaBuy
			VOL B/S
			QuantaBuy
			VOL B/S
			QuantaBuy
			VOL B/S
			QuantaBuy
			VOL B/S
			QuantaBuy
			VOL B/S

PROJECT : LL5A
Quanta Computer Inc.

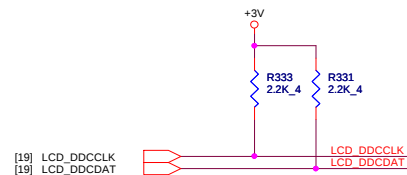
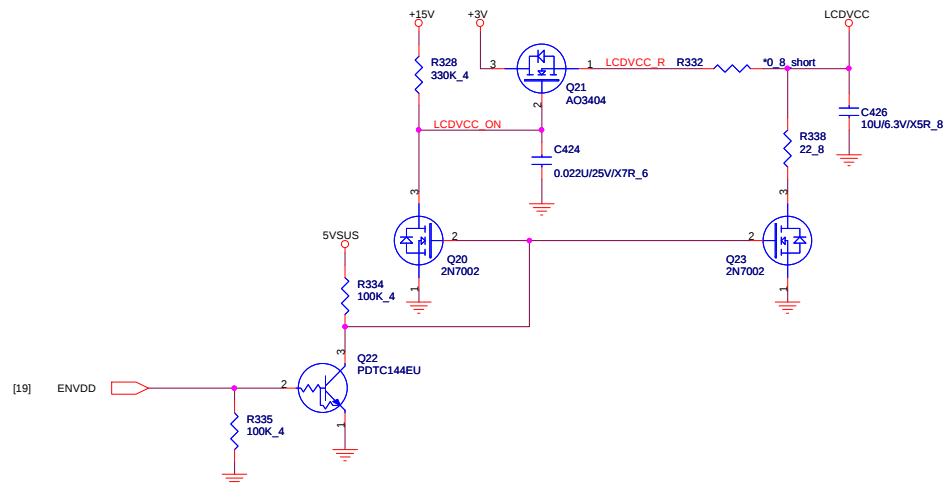
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Document Number: VRAM_DDR3_512M

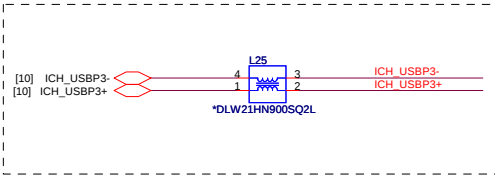
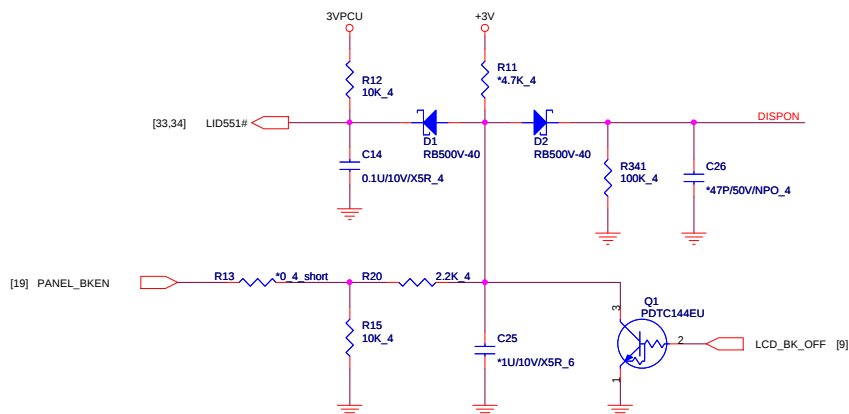
Date: Tuesday, October 20, 2009

Sheet: 21 of 43

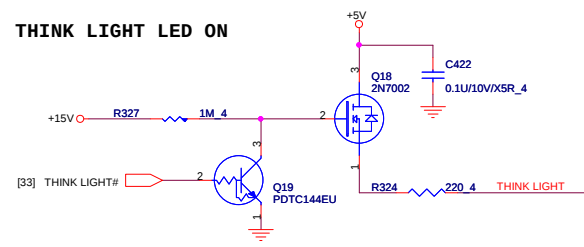
LCDVCC



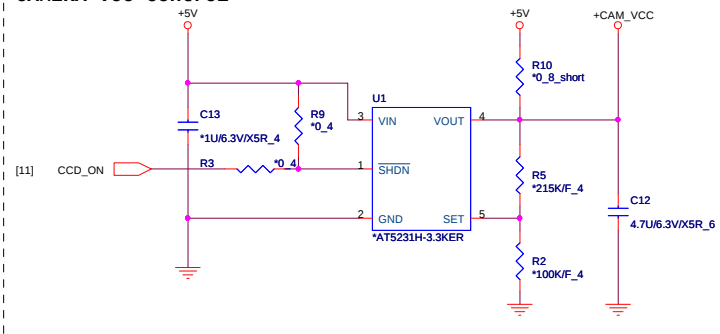
back light

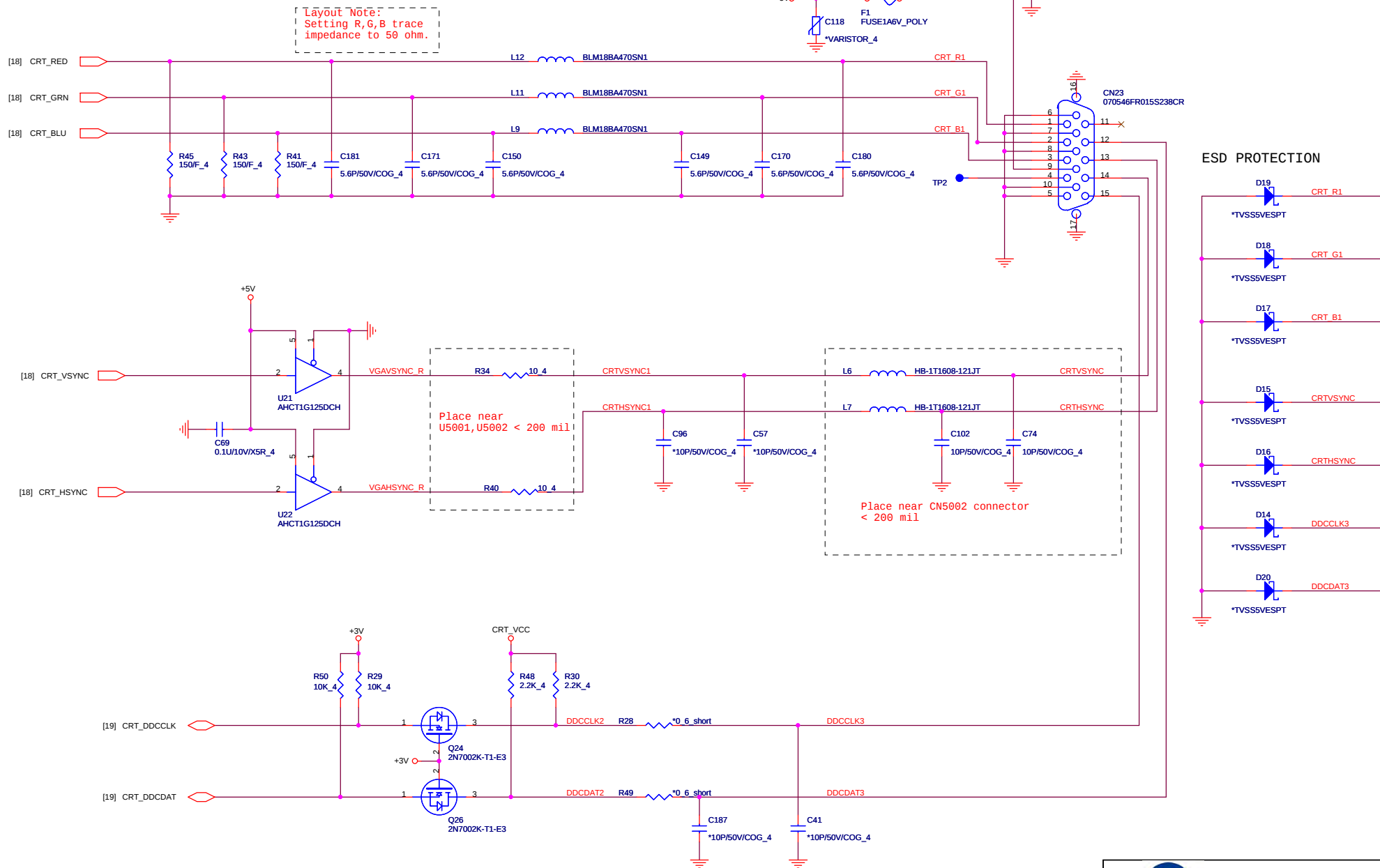


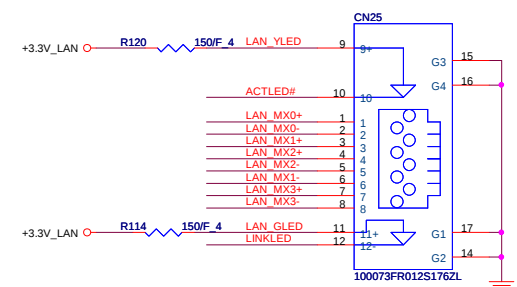
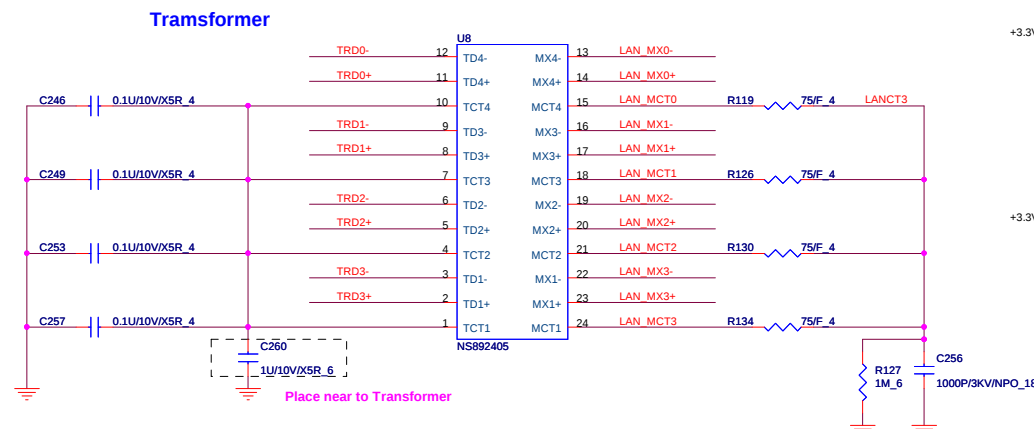
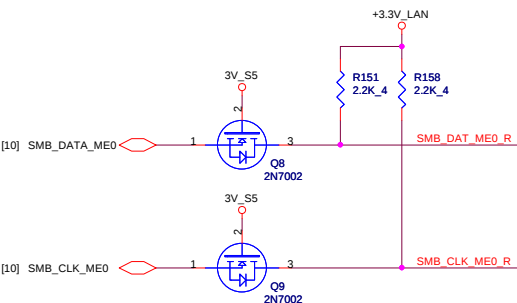
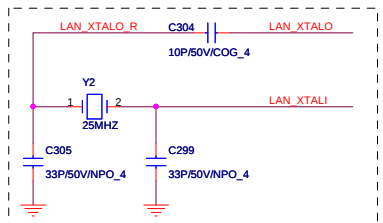
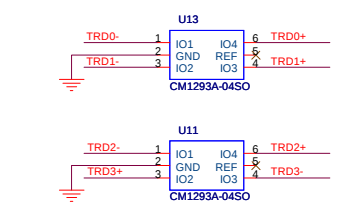
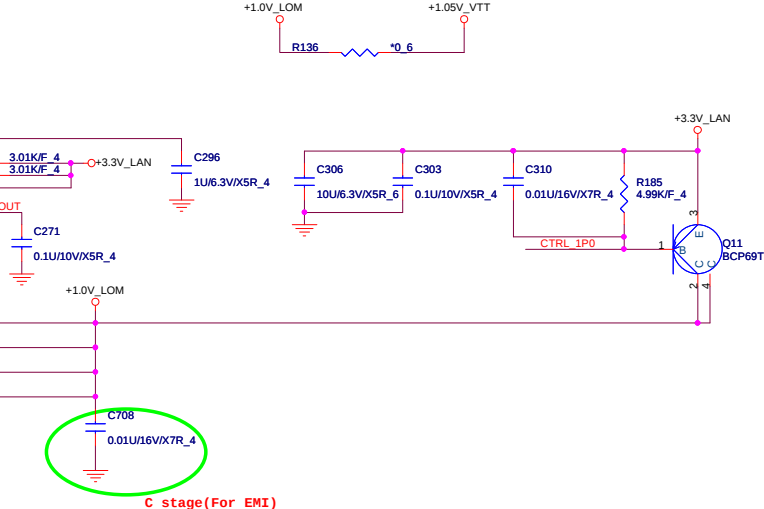
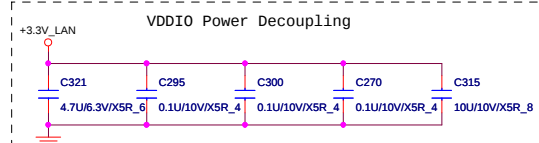
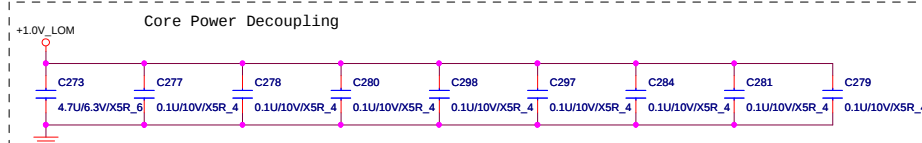
THINK LIGHT LED ON

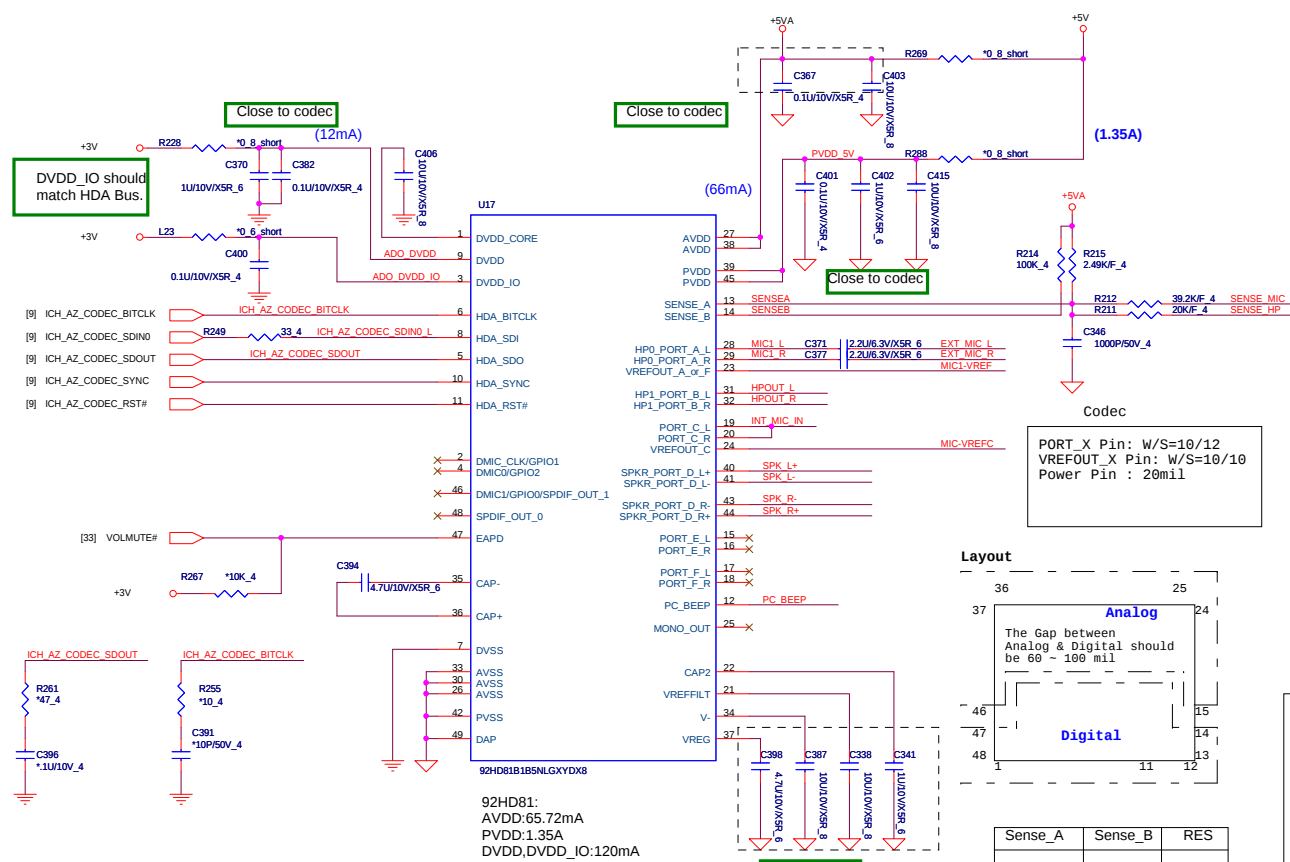


CAMERA VCC Control

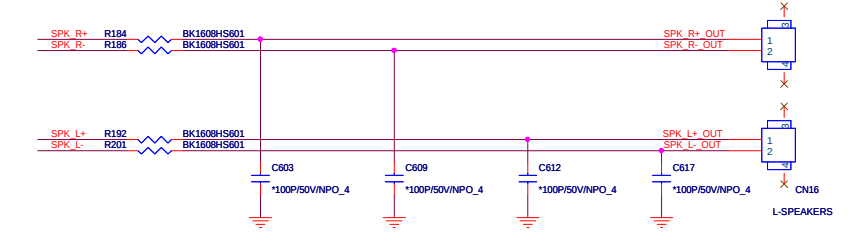




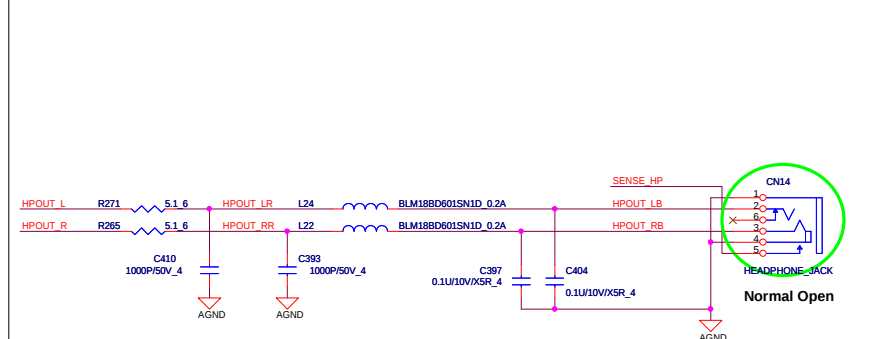




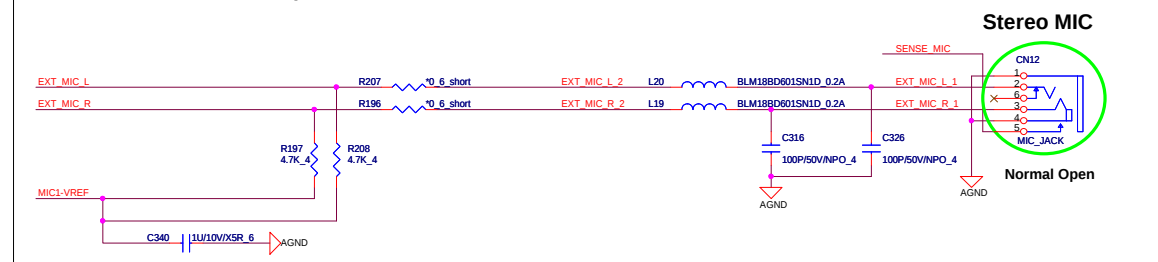
INT Speaker



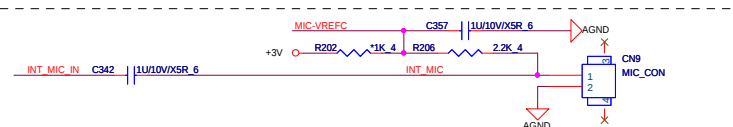
Headphone out



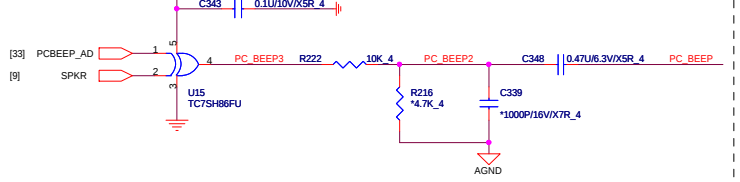
External Microphone Jack



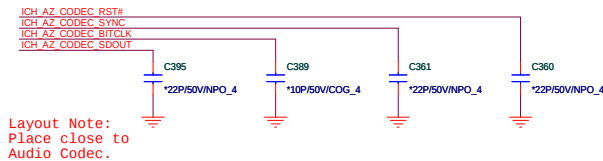
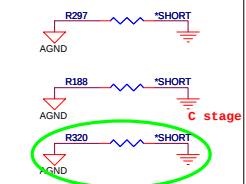
INT MIC

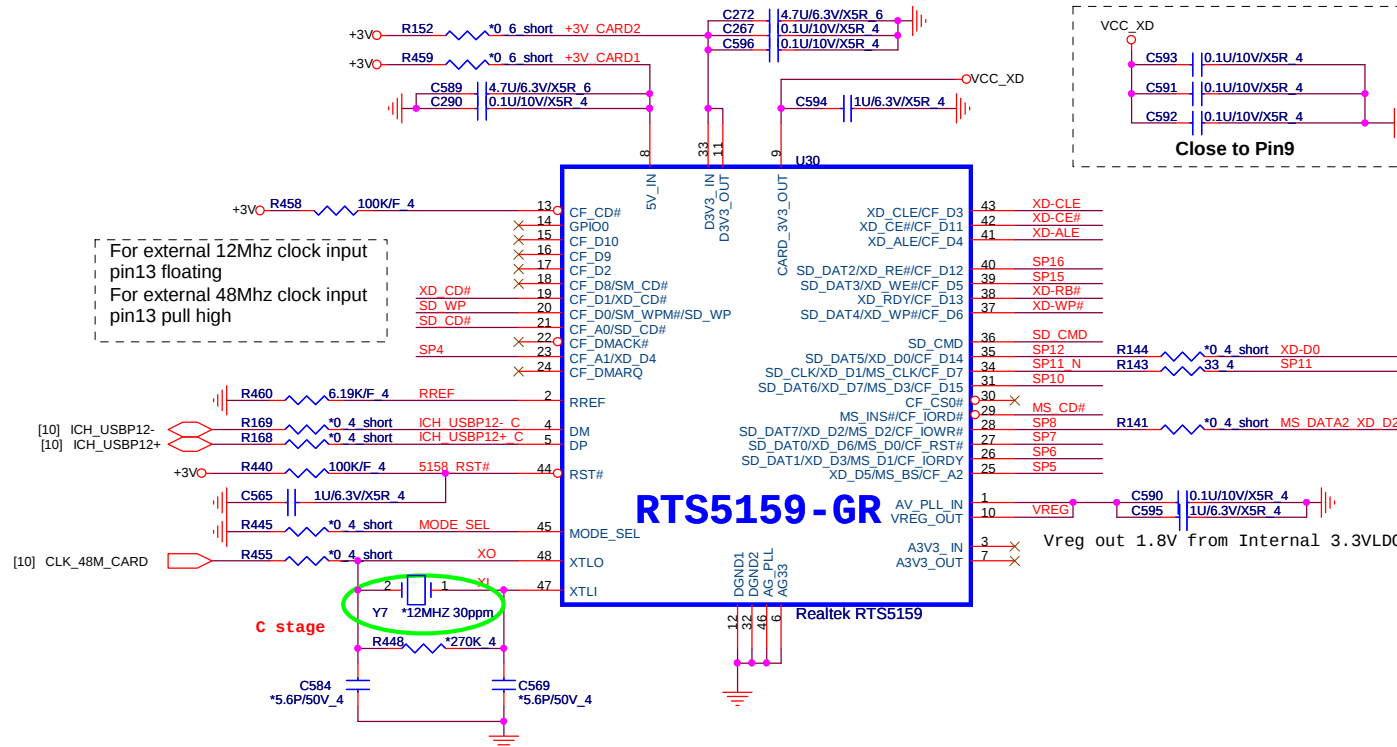


PC BEEP



EMI Reserved

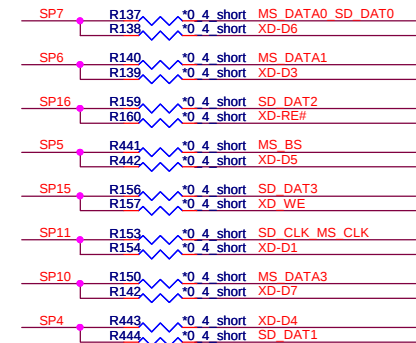
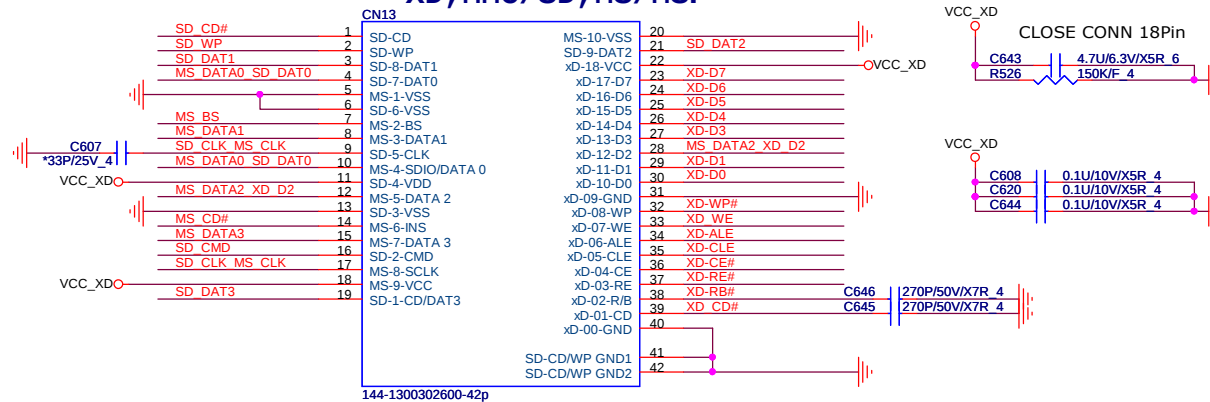




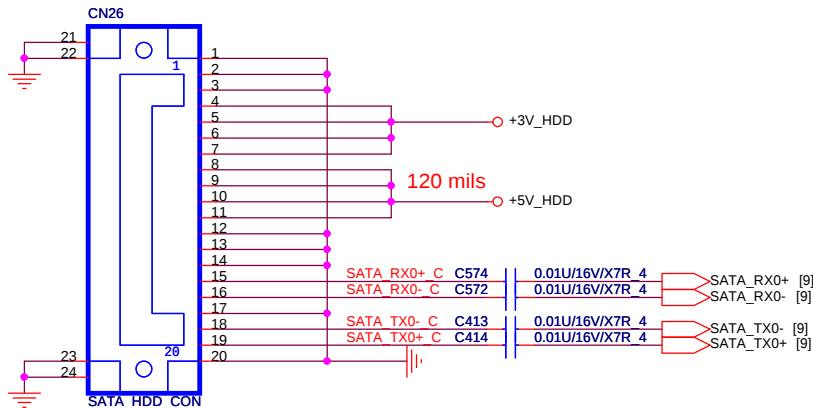
Note:

SD/MMC	MS	XD
SP0		
SP1	SD WP	XD_CD#
SP2	SD CD#	
SP3	SD DAT1	XD D4
SP4		XD D5
SP5	MS BS	XD D3
SP6	MS D1	XD D6
SP7	SD DAT0	XD D2
SP8	MS D2	
SP9	MS INS#	
SP10	SD DAT6	XD D7
SP11	SD CLK	XD D1
SP12	SD DAT5	XD D0
SP13	SD DAT4	XD WP#
SP14		XD R/B#
SP15	SD DAT3	XD WE#
SP16	SD DAT2	XD RE#
SP17		XD ALE
SP18		XD CE#
SP19		XD CLE

For RTS5159

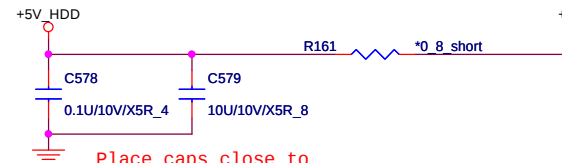
5 IN1 CARD READER
XD, MMC/SD, MS/MSP

SATA-HDD CONNECTOR

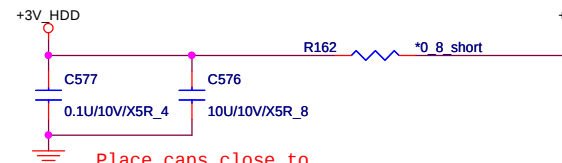


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 [12,22,23,25,32,33,34,35,37,38] +3V
 [22,37,39,41] +5V
 [9,37,38,39,40,41,43] 5VPCU
 [9,22,24,33,34,35,37,38,40,41,43] 3VPCU

27

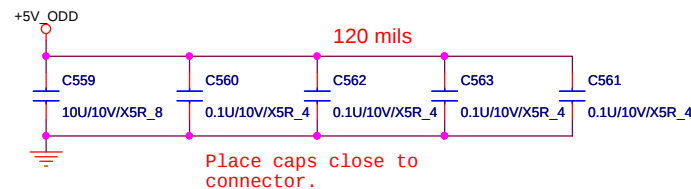
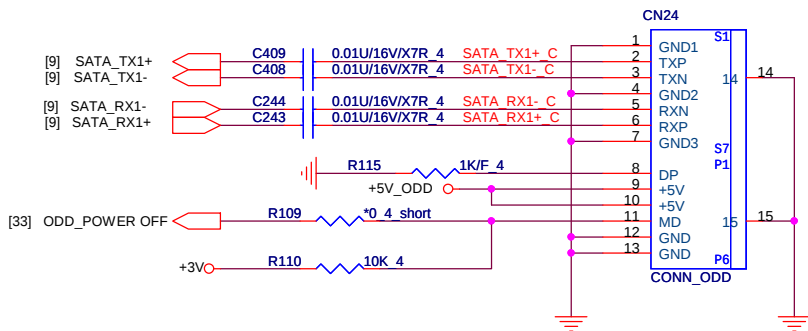


Place caps close to connector.

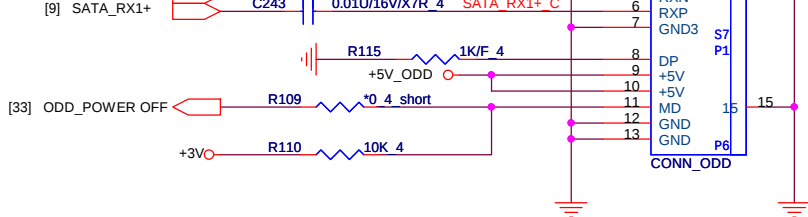


Place caps close to connector.

SATA CD-ROM

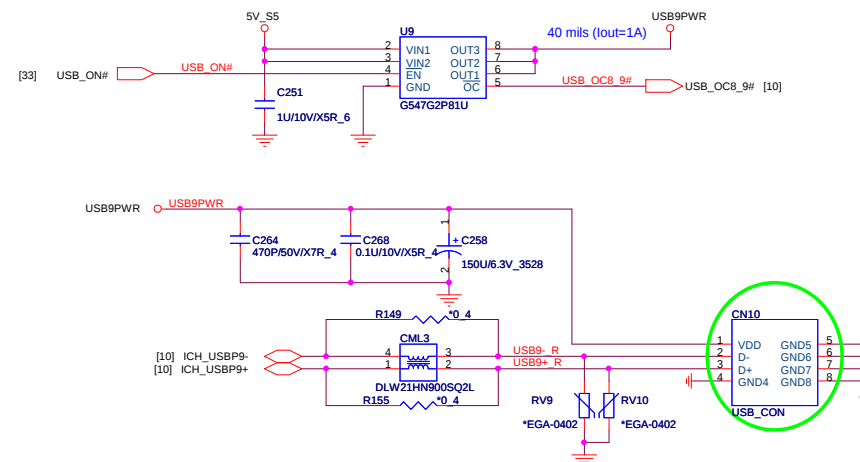


Place caps close to connector.



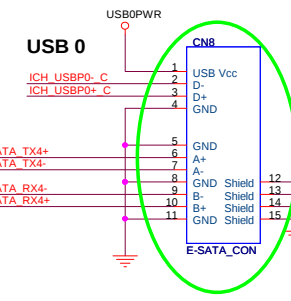
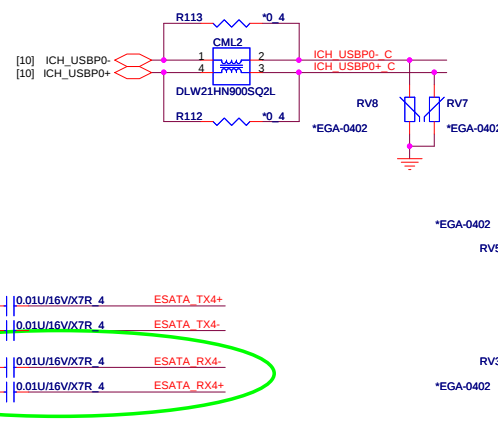
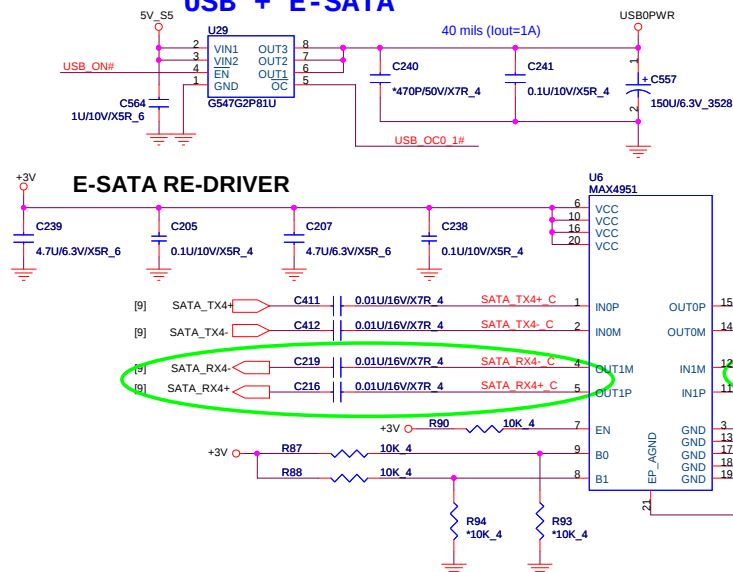
[33] ODD_EN

USB 4



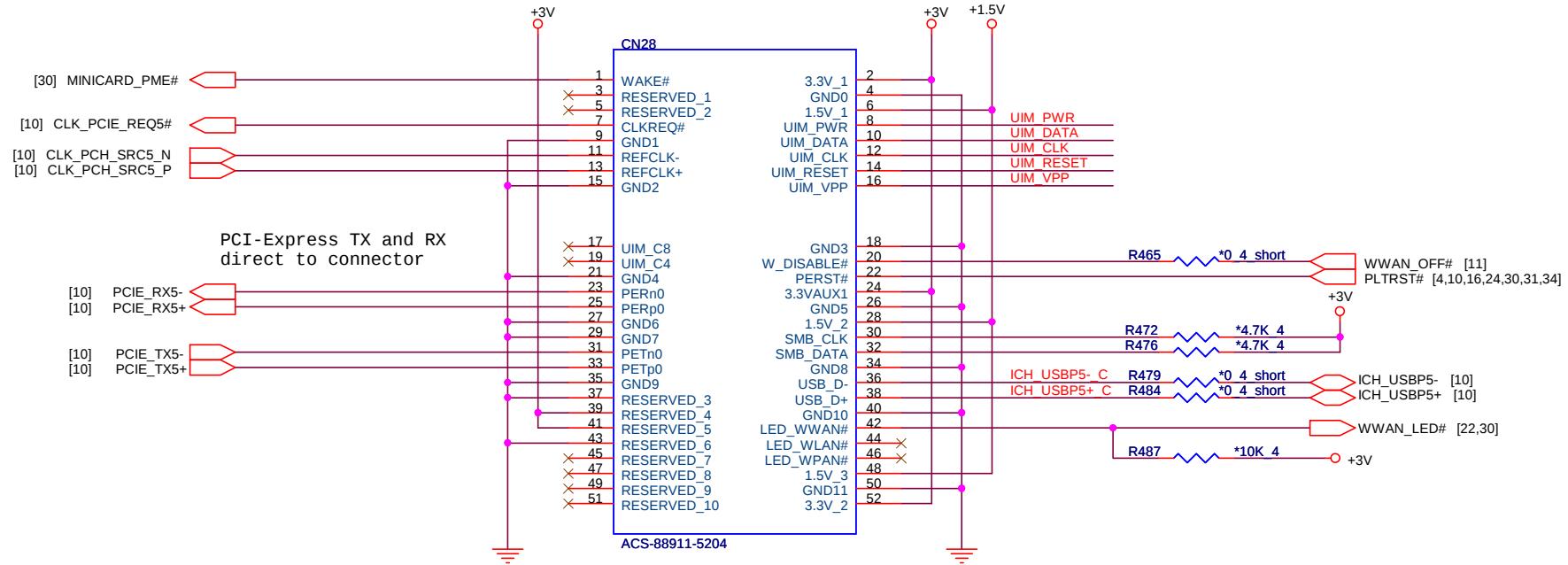
USB 1

USB + E-SATA

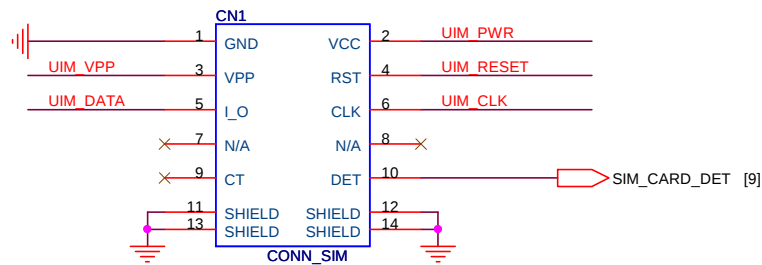


EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0.1 Boost Output

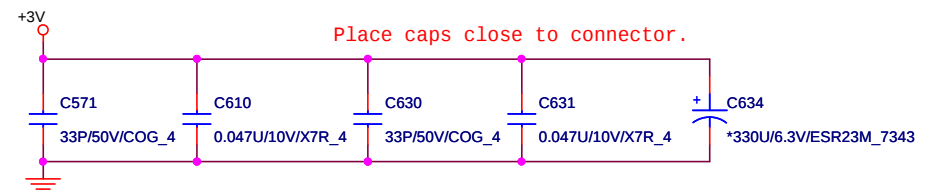
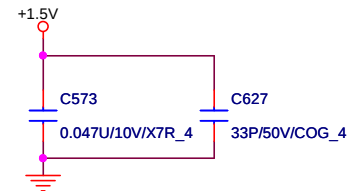
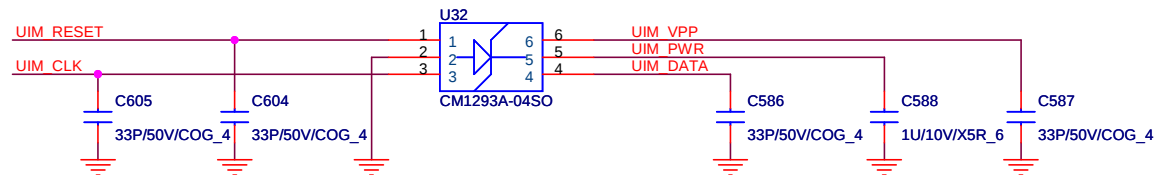
MiniCard WWAN connector



SIM Card CONN



Layout Note:
UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible



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Quanta Computer Inc.

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MINI-Card (WWAN)		
Date:	Tuesday, October 20, 2009	Sheet 29 of 43

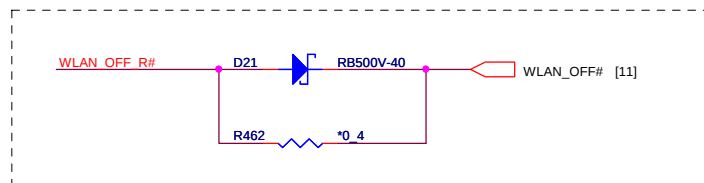
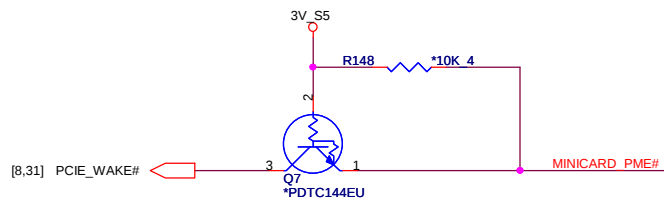
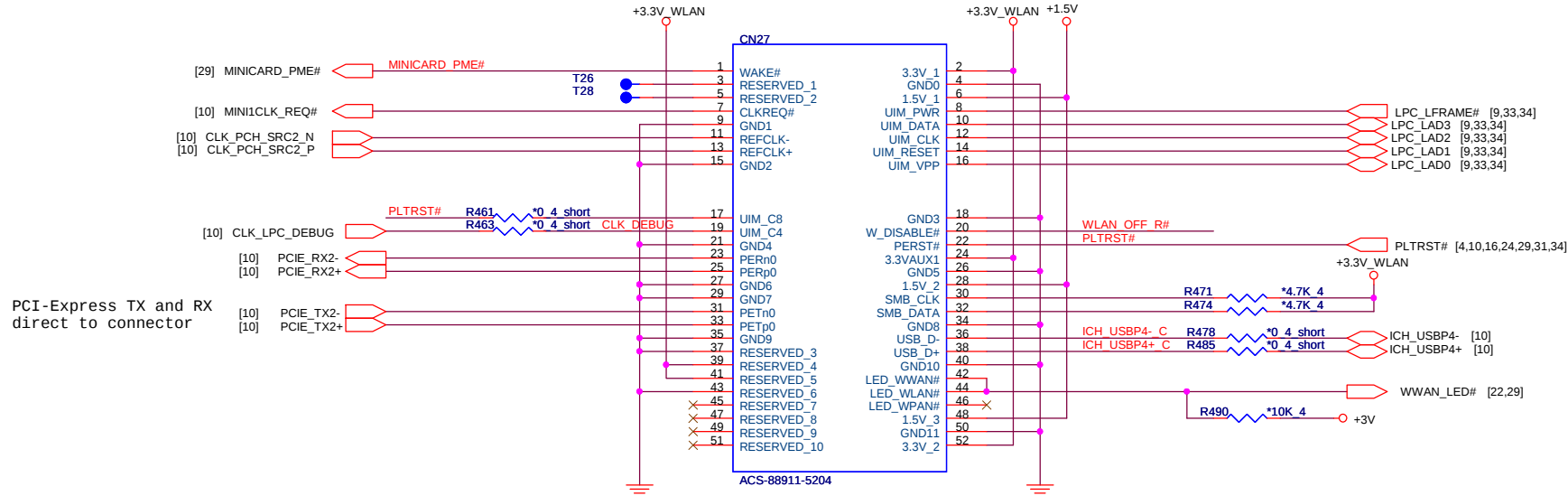
MiniCard WLAN/WiMAX connector

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[3,17,21,29,31,39]
[4,8,9,10,11,12,24,37]

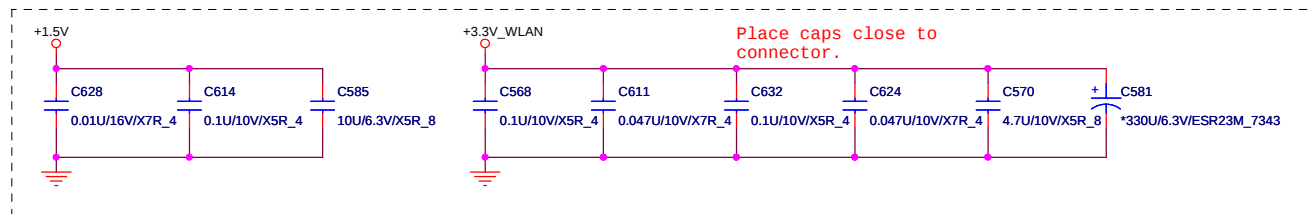
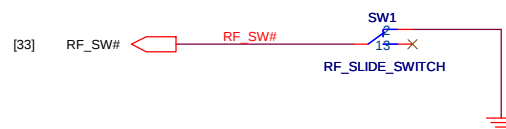
+3V
+1.5V
3V_S5



30



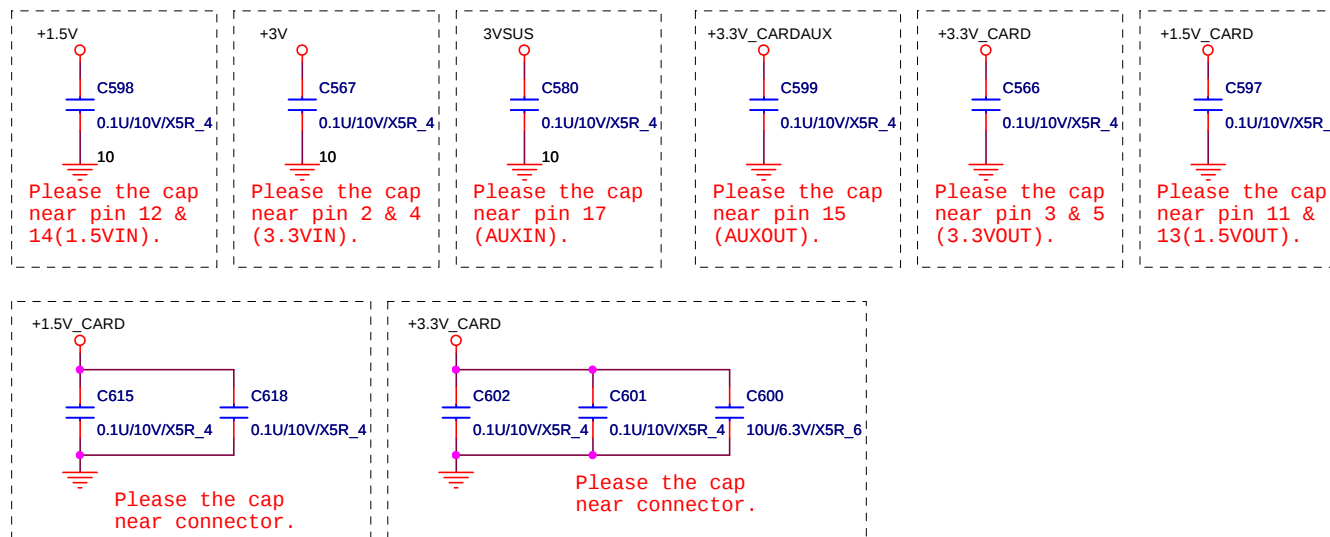
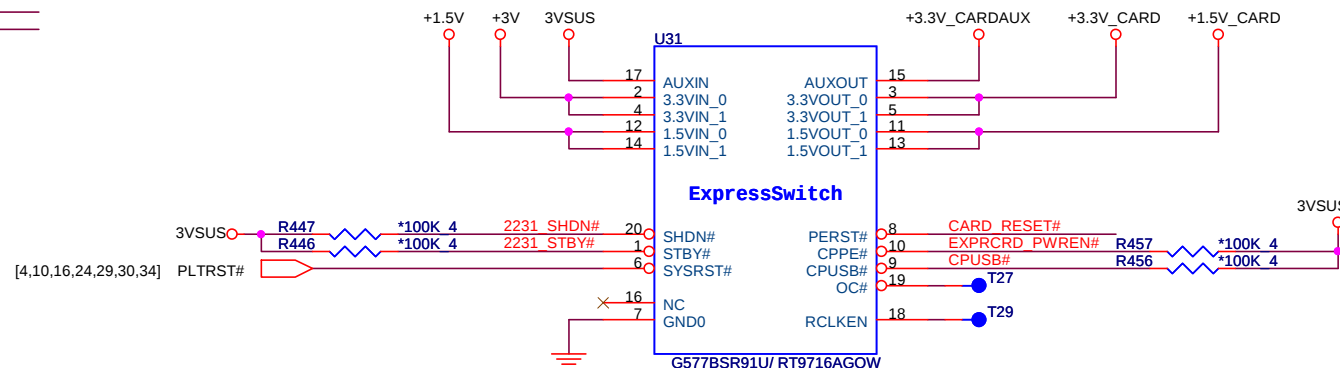
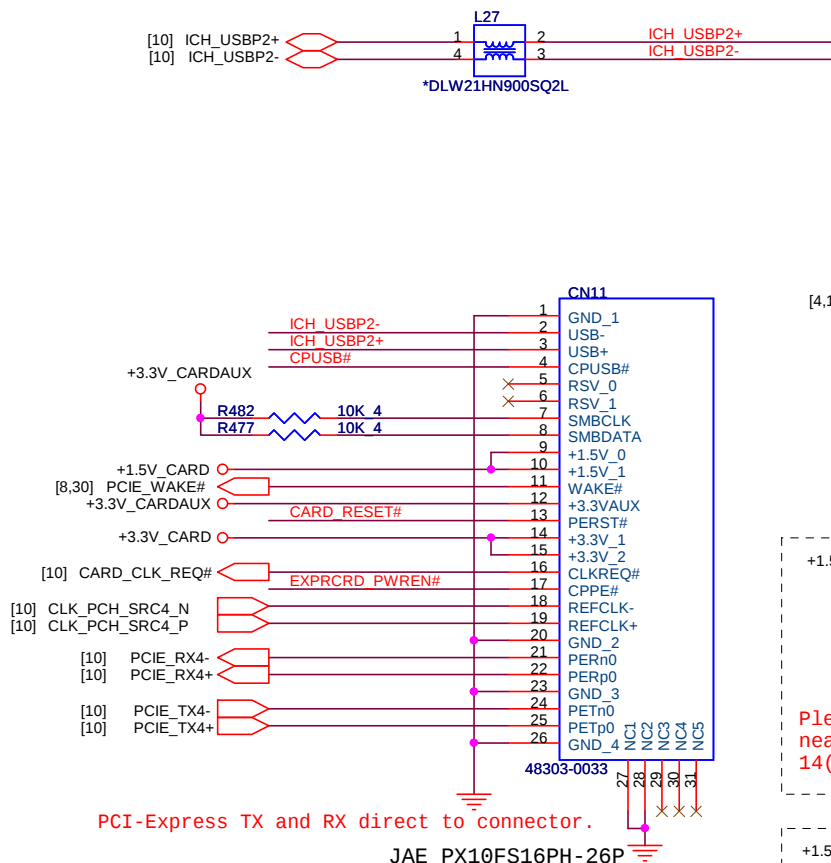
RF ON/OFF SWITCH



Express Card

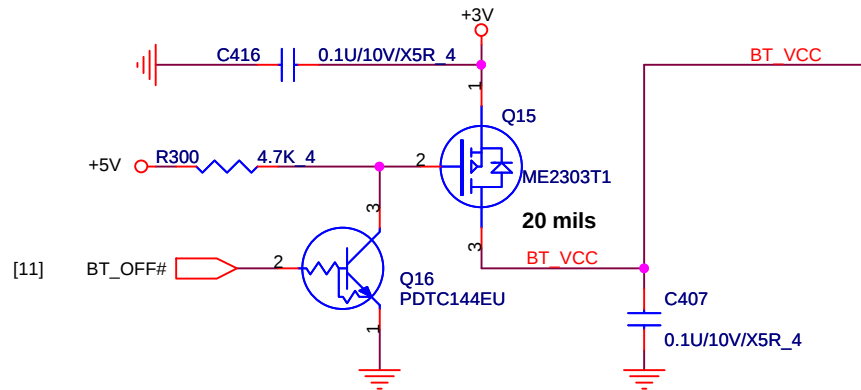
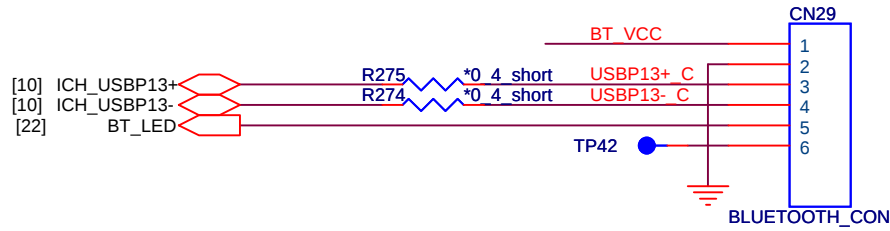
31

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA.

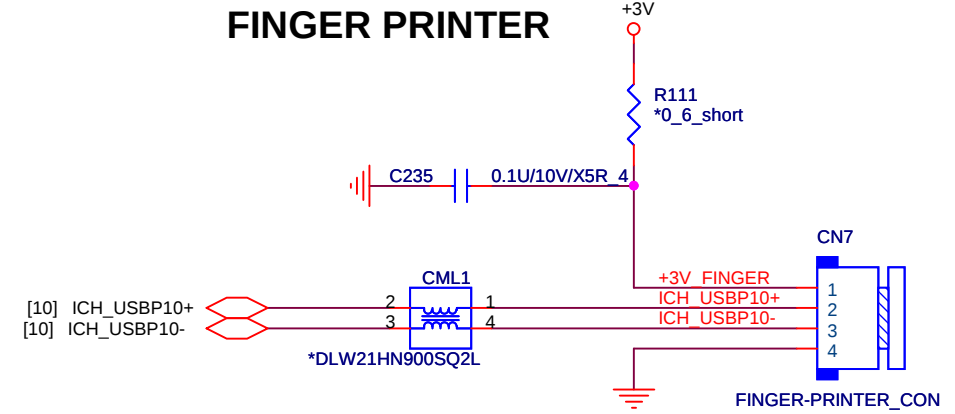




BLUETOOTH



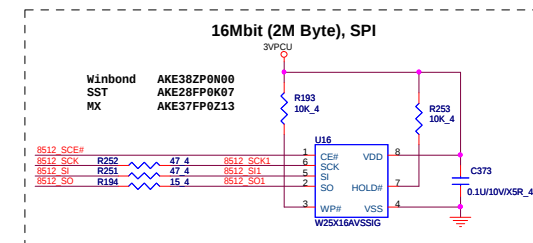
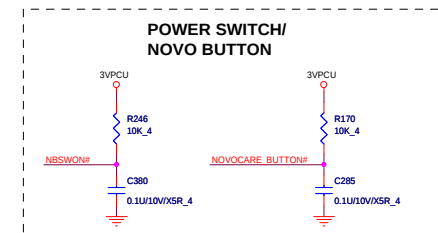
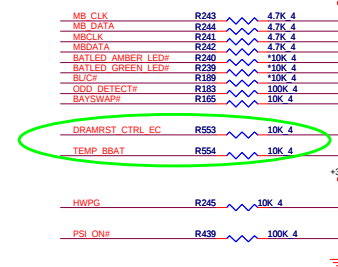
FINGER PRINTER



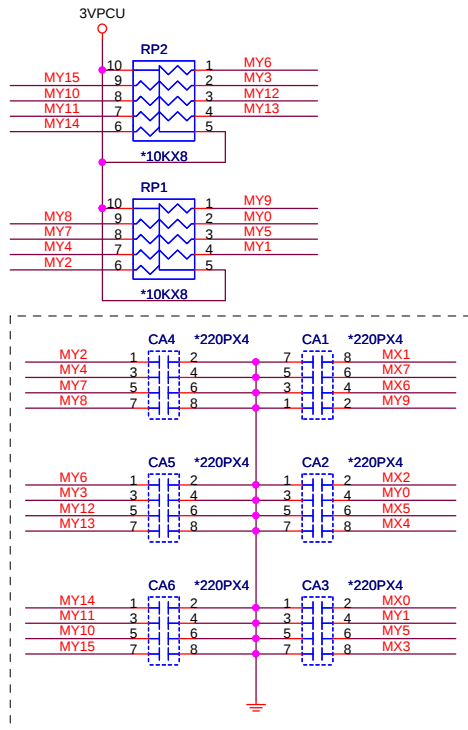
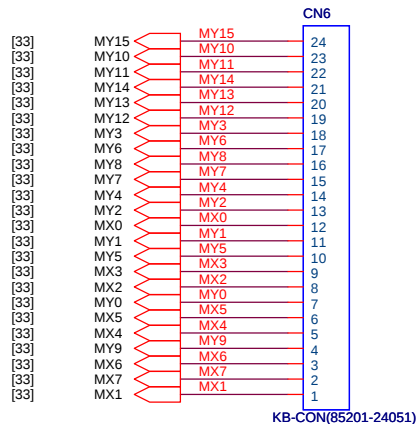
PROJECT : LL5A
Quanta Computer Inc.

Size Custom	Document Number	Rev 1B
Date:	Tuesday, October 20, 2009	Sheet 32 of 43

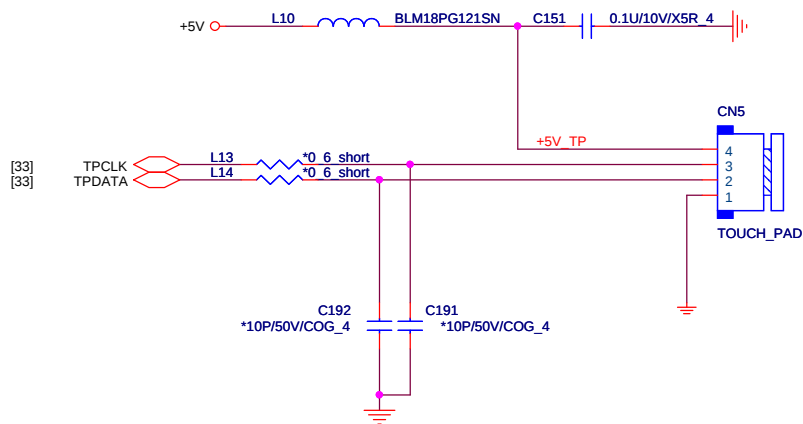
BT/FP



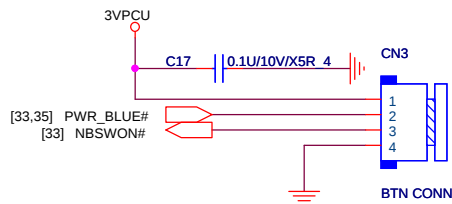
KEYBOARD



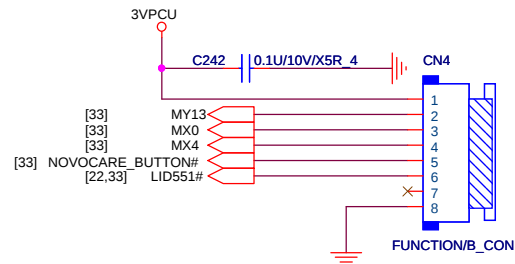
TOUCH PAD



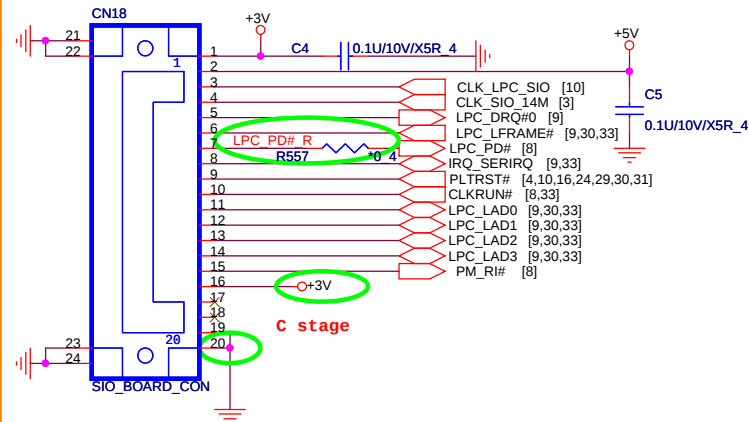
POWER BUTTON BOARD



FUNCTION BUTTON BOARD



SIO BOARD

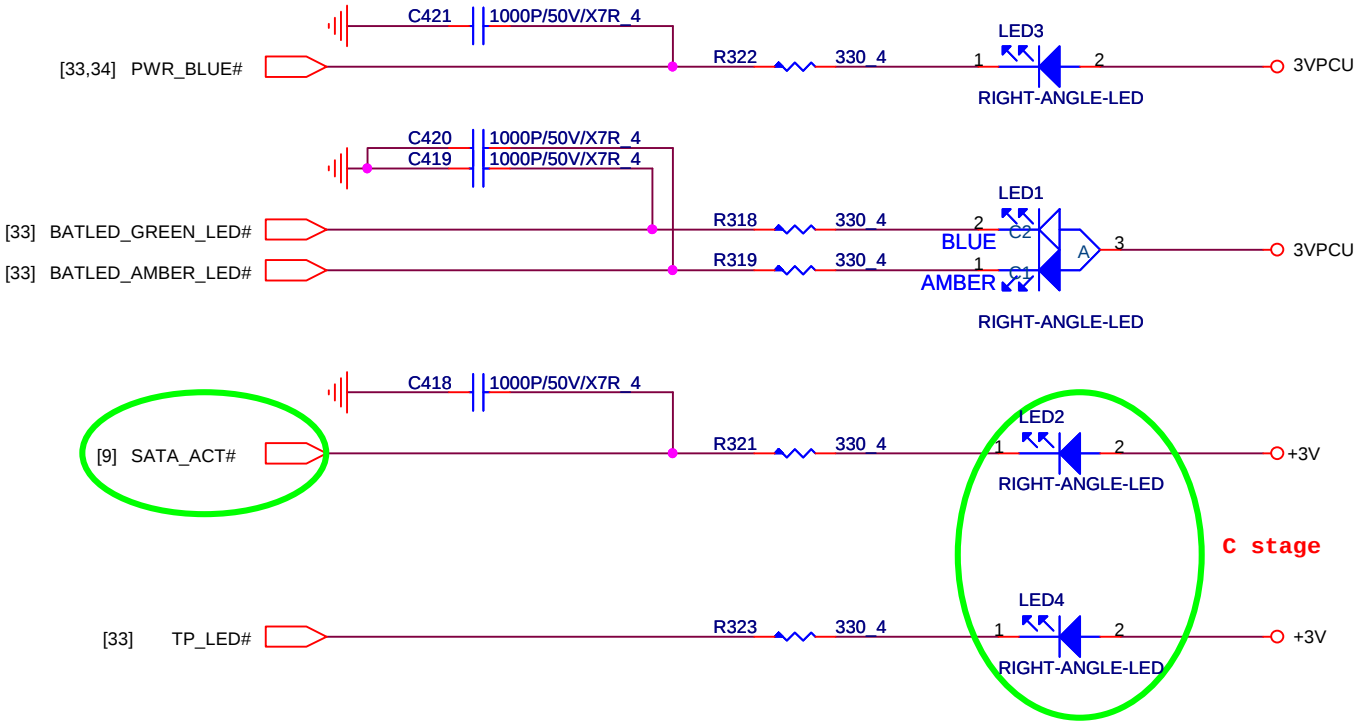


PROJECT : LL5A
Quanta Computer Inc.

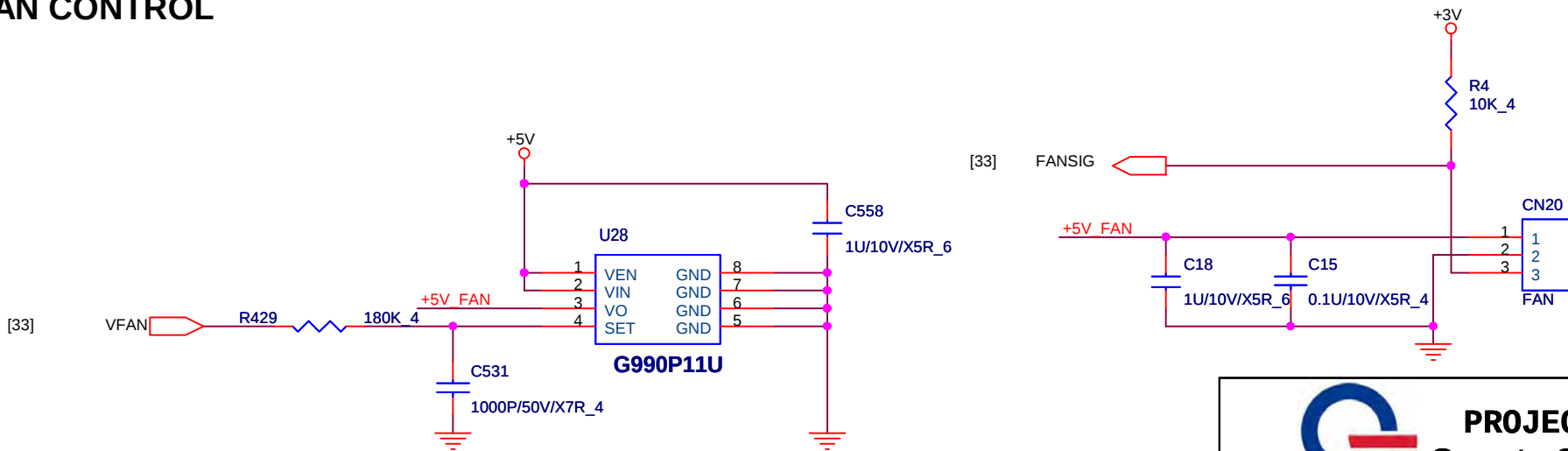
LED

[3,4,6,8,9,10,11,12,14,15,16,18,19,22,23,25,26,27,28,29,30,31,32,33,34,36,37,38,39,40,41,42] +3V
[12,22,23,25,27,32,33,34,37,38] +5V

35



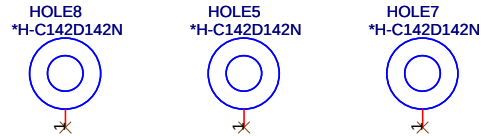
FAN CONTROL



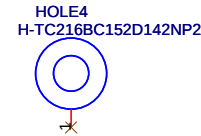
PROJECT : LL5A
Quanta Computer Inc.

Size Custom	Document Number LED/FAN	Rev 1B
Date: Tuesday, October 20, 2009	Sheet 35	of 43

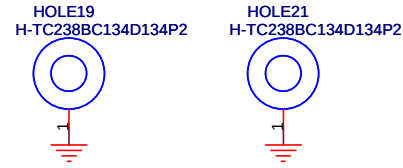
Hole for CPU support



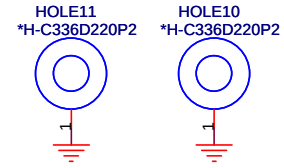
Hole for CPU Nut



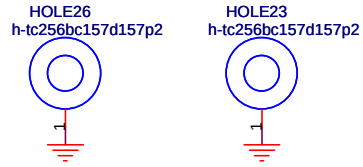
VGA nut



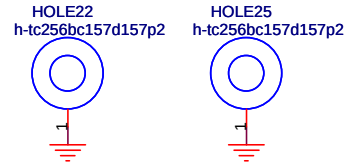
Drink Hole



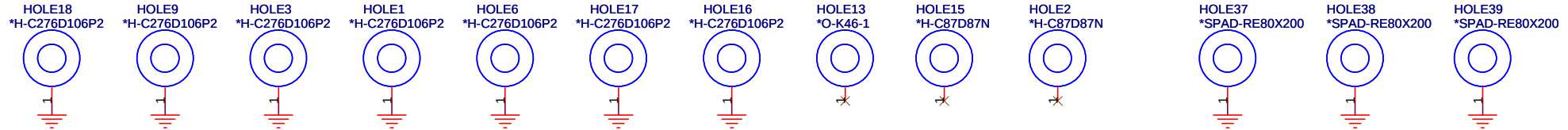
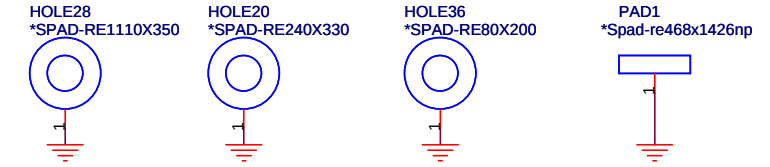
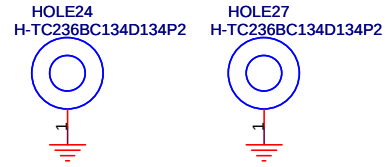
MINI CARD nut (WLAN)



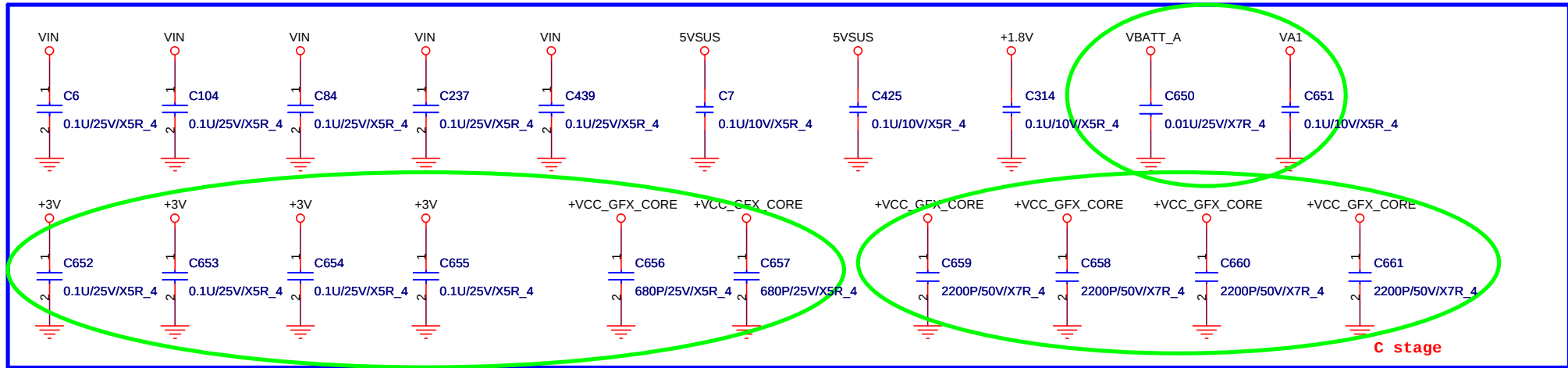
MINI CARD nut (WWAN)



Hole for PCH Thermal

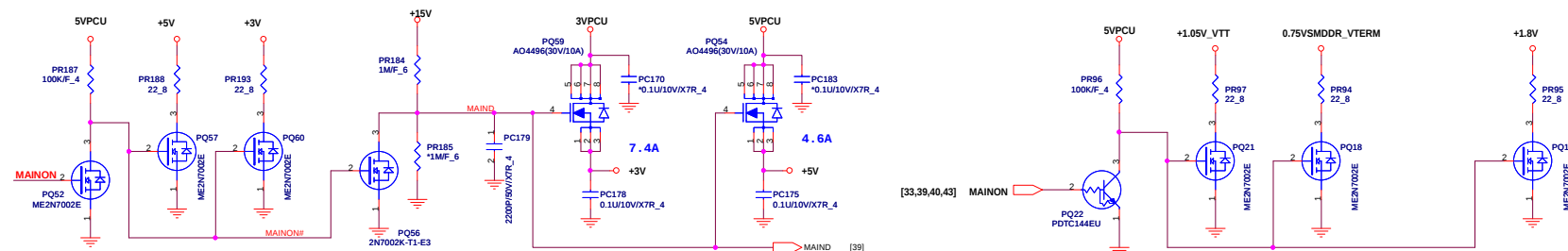


EMI Reserved

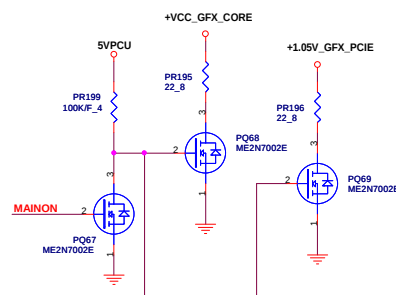
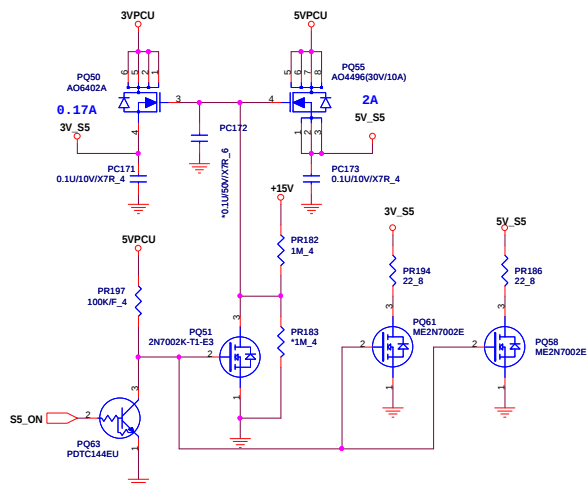


PROJECT : LL5A
Quanta Computer Inc.

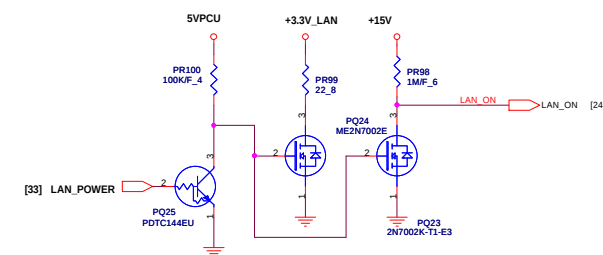
+3V, +5V



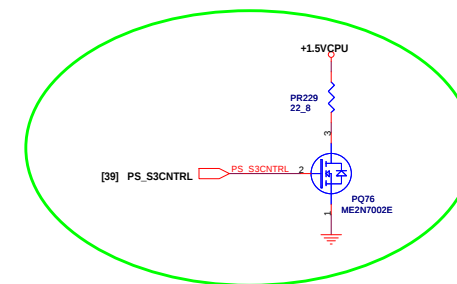
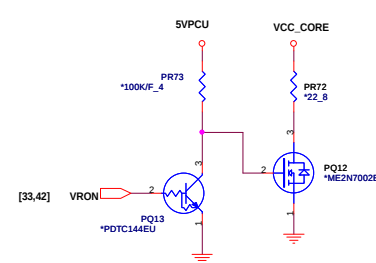
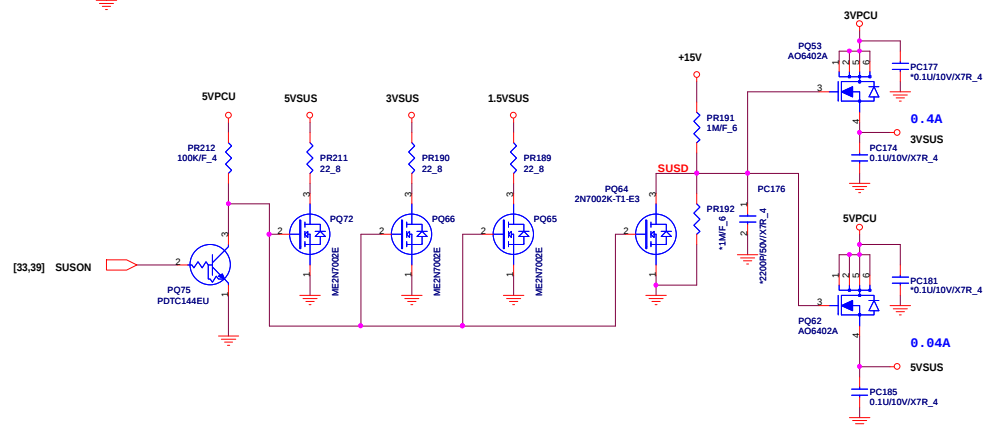
3V_S5, 5V_S5

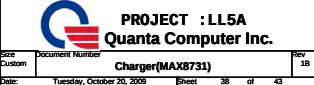


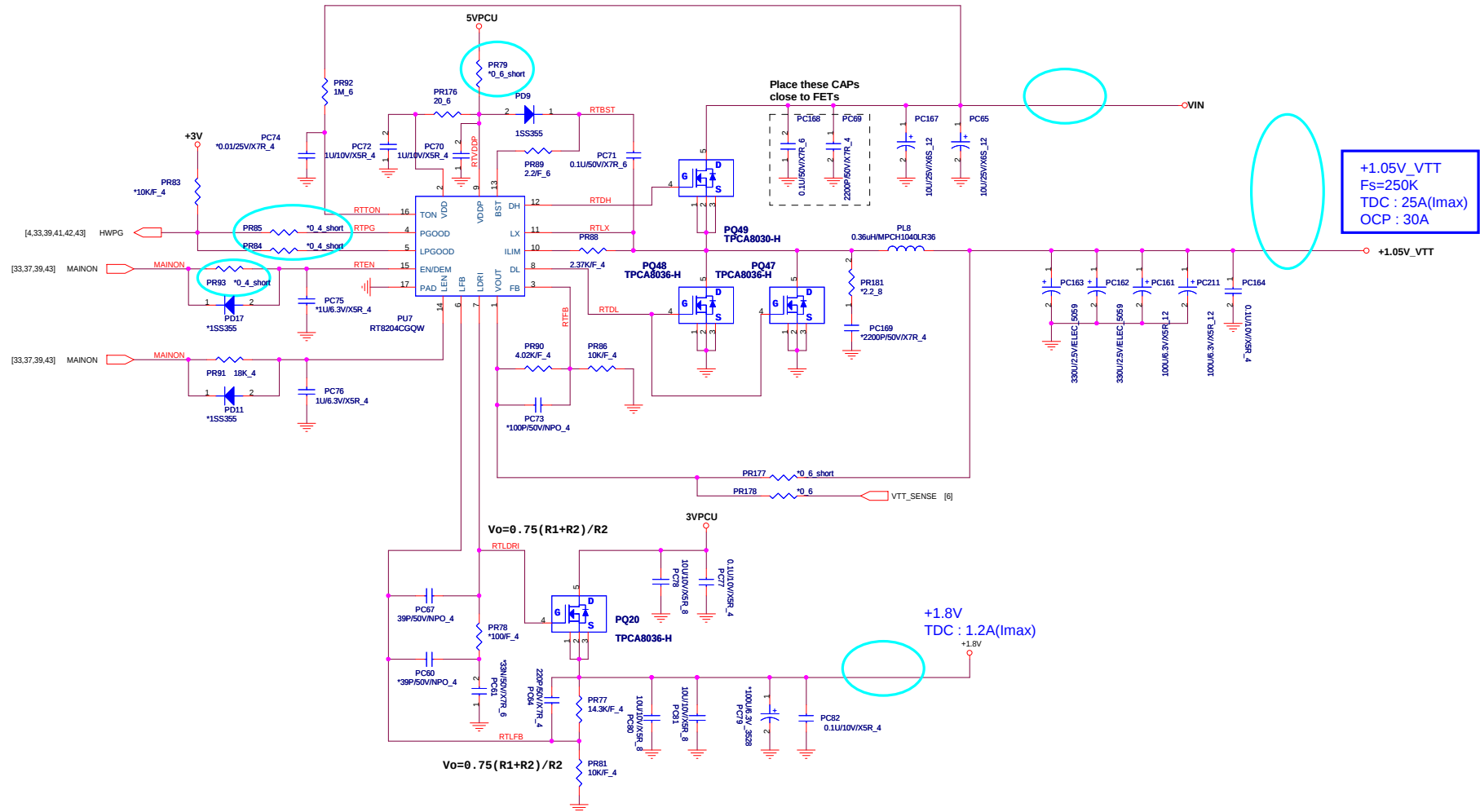
LANVCC



3VSUS, 5VSUS

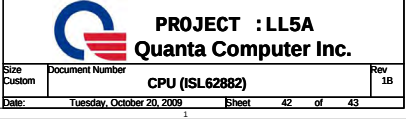




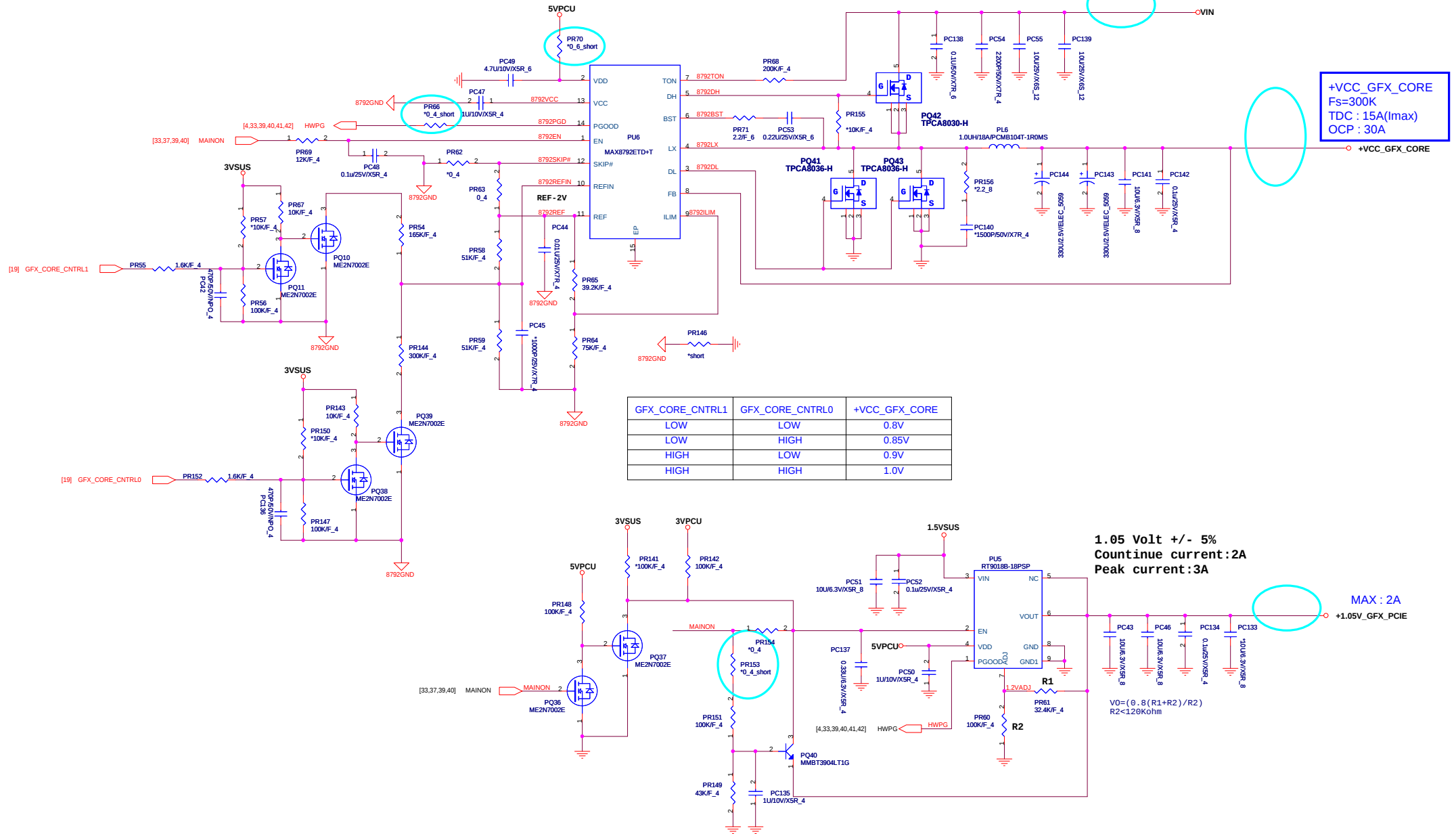


PROJECT : LL5A
Quanta Computer Inc.





For Descrete N10M VGA Only



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