Compal Confidential

Schematics Document
P4 uFCBGA/uFCPGA Northwood with SIS Core Logic

2001-5-30

REV:1.0A

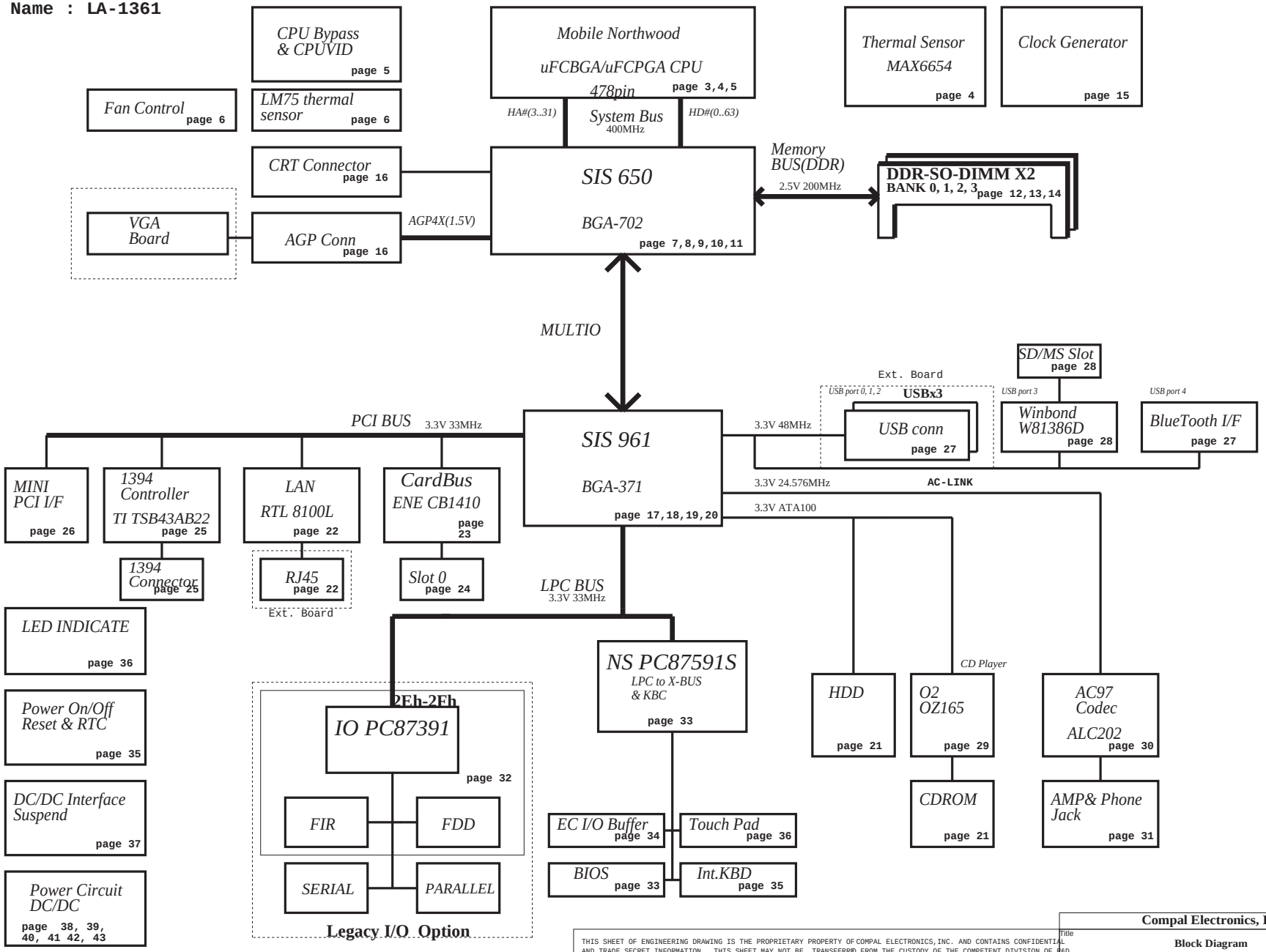
Compal Electronics, Inc.		
Title: Cover Sheet		
Size	Document Number: ACT10	Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 1 of 45	

Compal confidential

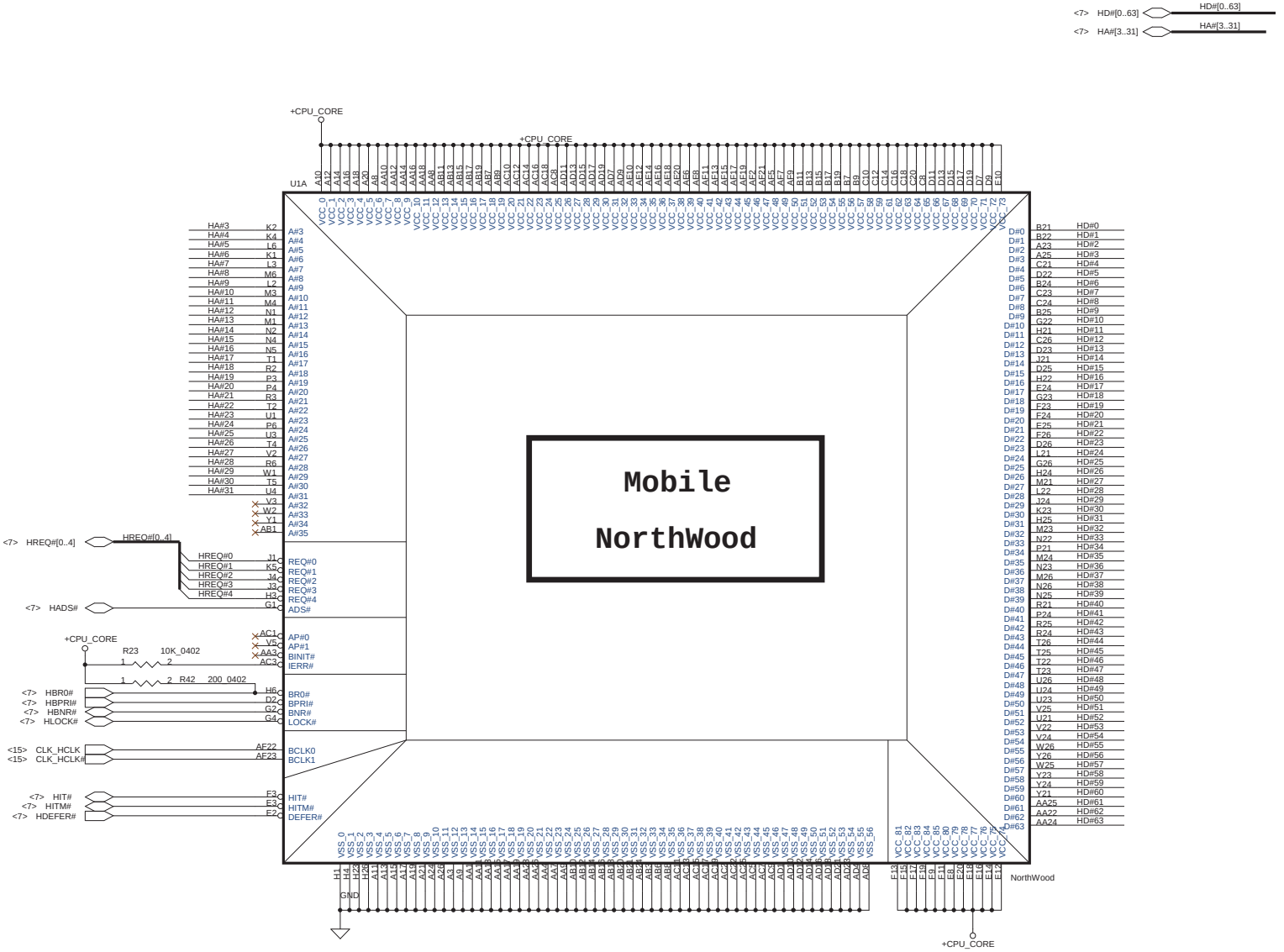
Model Name :CT10

File Name : LA-1361

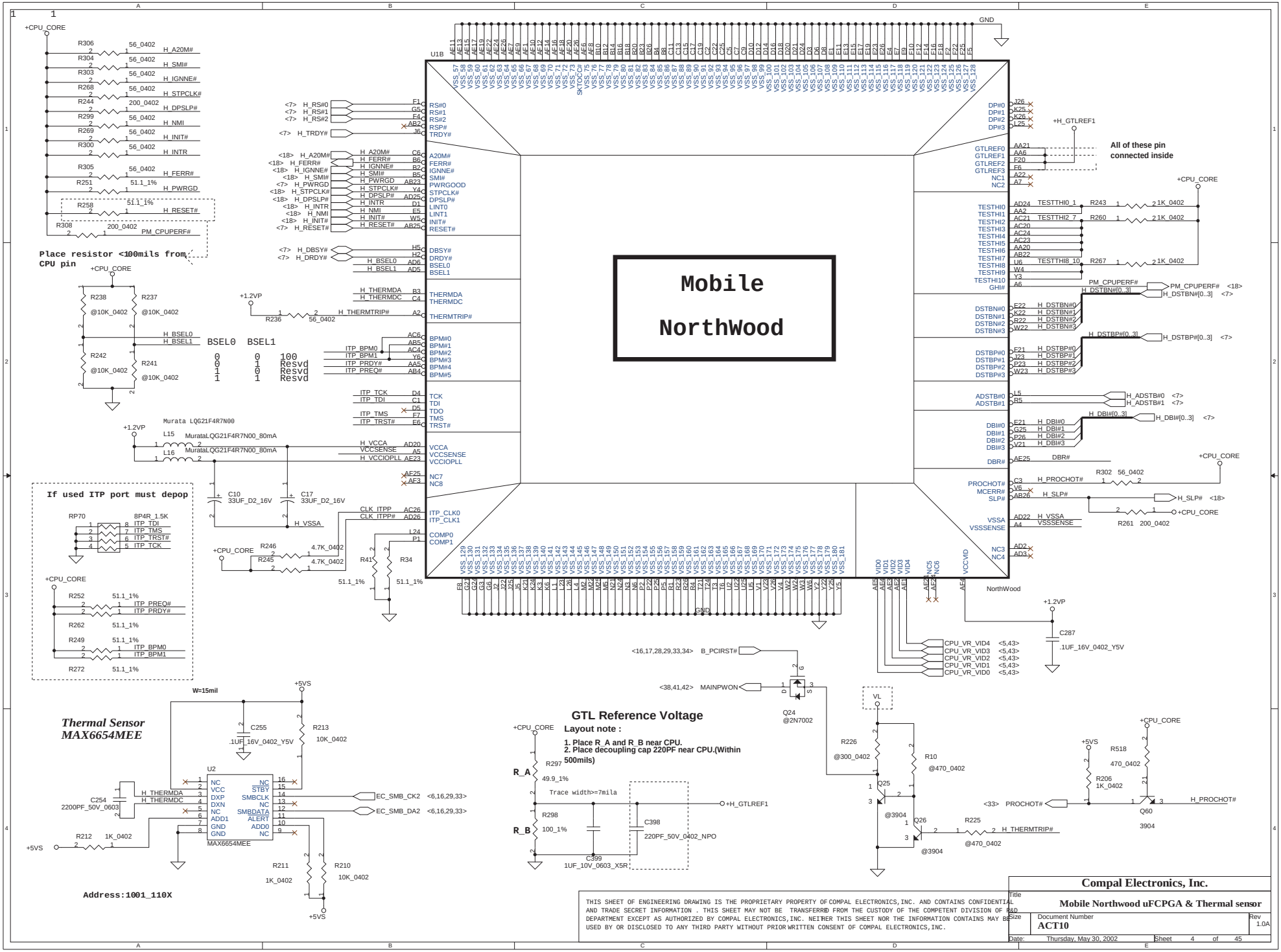
Block Diagram



Compal Electronics, Inc.		
Title: Block Diagram		
Size	Document Number: ACT10	Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 2 of 45	

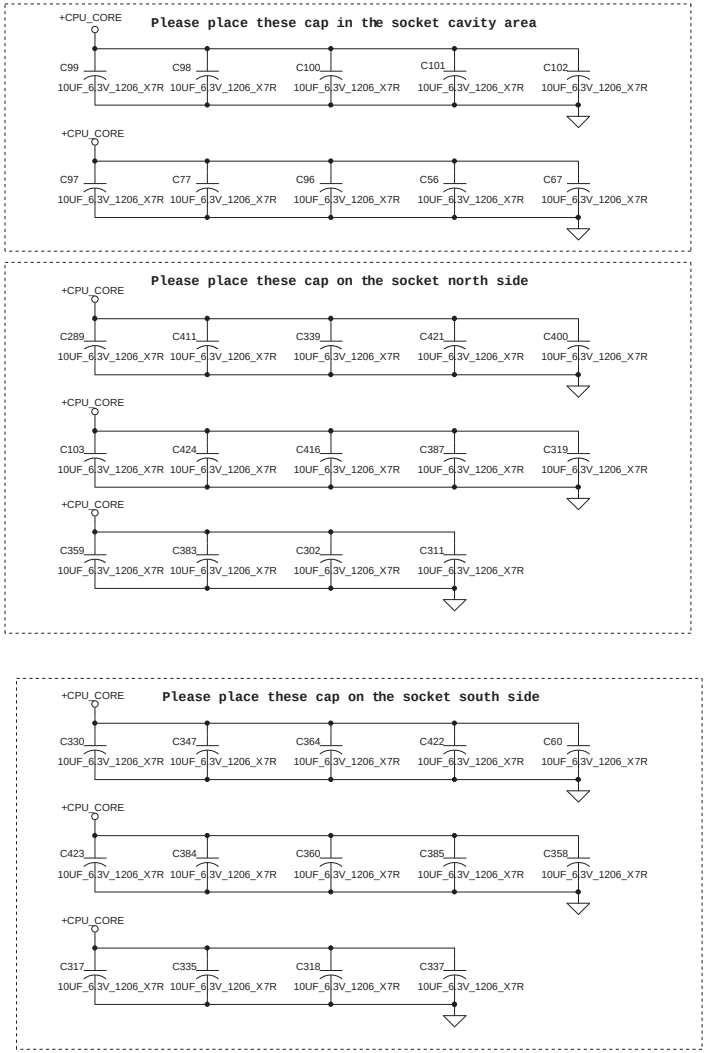


Compal Electronics, Inc.	
Title	Mobile Northwood uFCPGA
Size	Document Number: ACT10 — Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 3 of 45



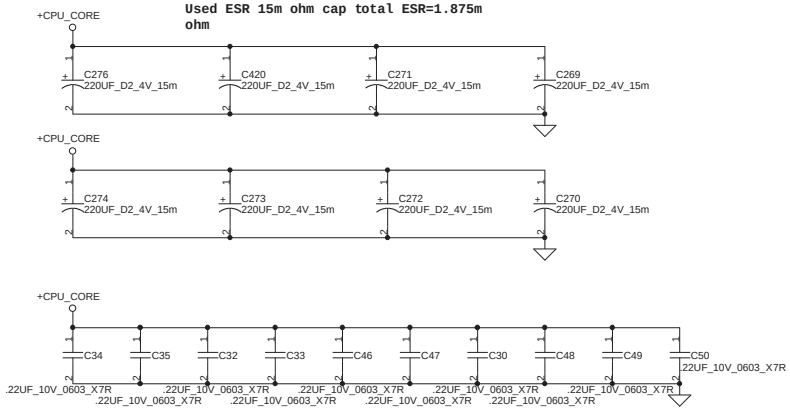
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

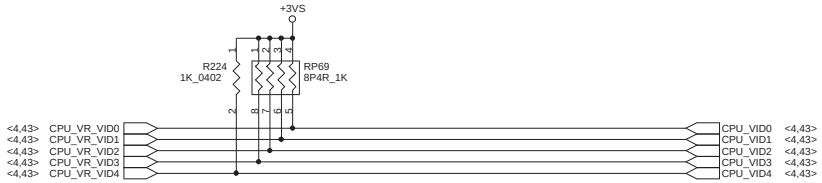


Layout note :

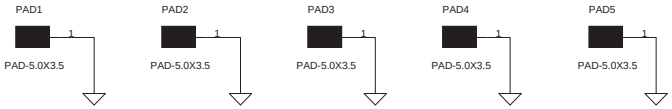
Place close to CPU power and ground pin as possible (<1inch)



CPU Voltage ID

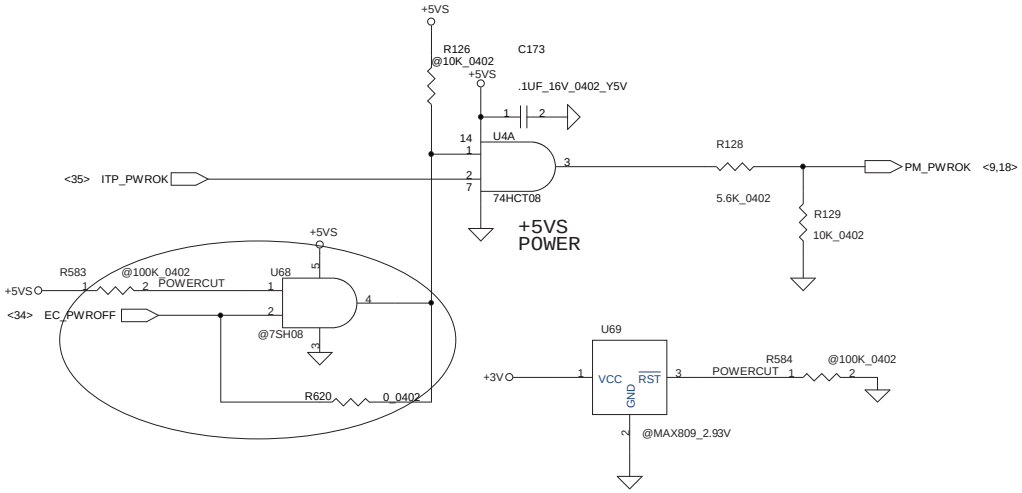


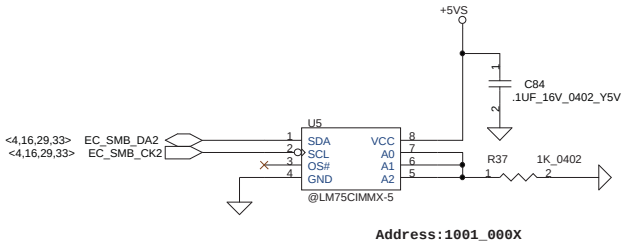
EMI Clip PAD for CPU



Compal Electronics, Inc.

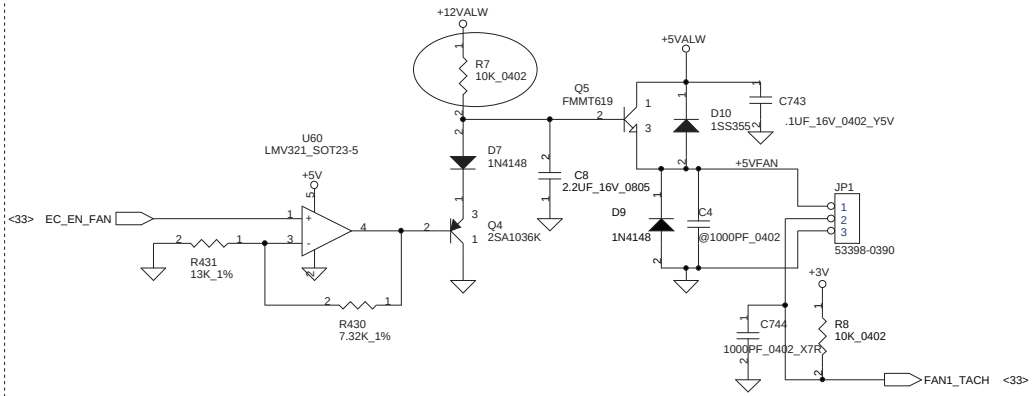
Title	CPU Bypass & CPU VID	
Size	Document Number ACT10	Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 5 of 45	





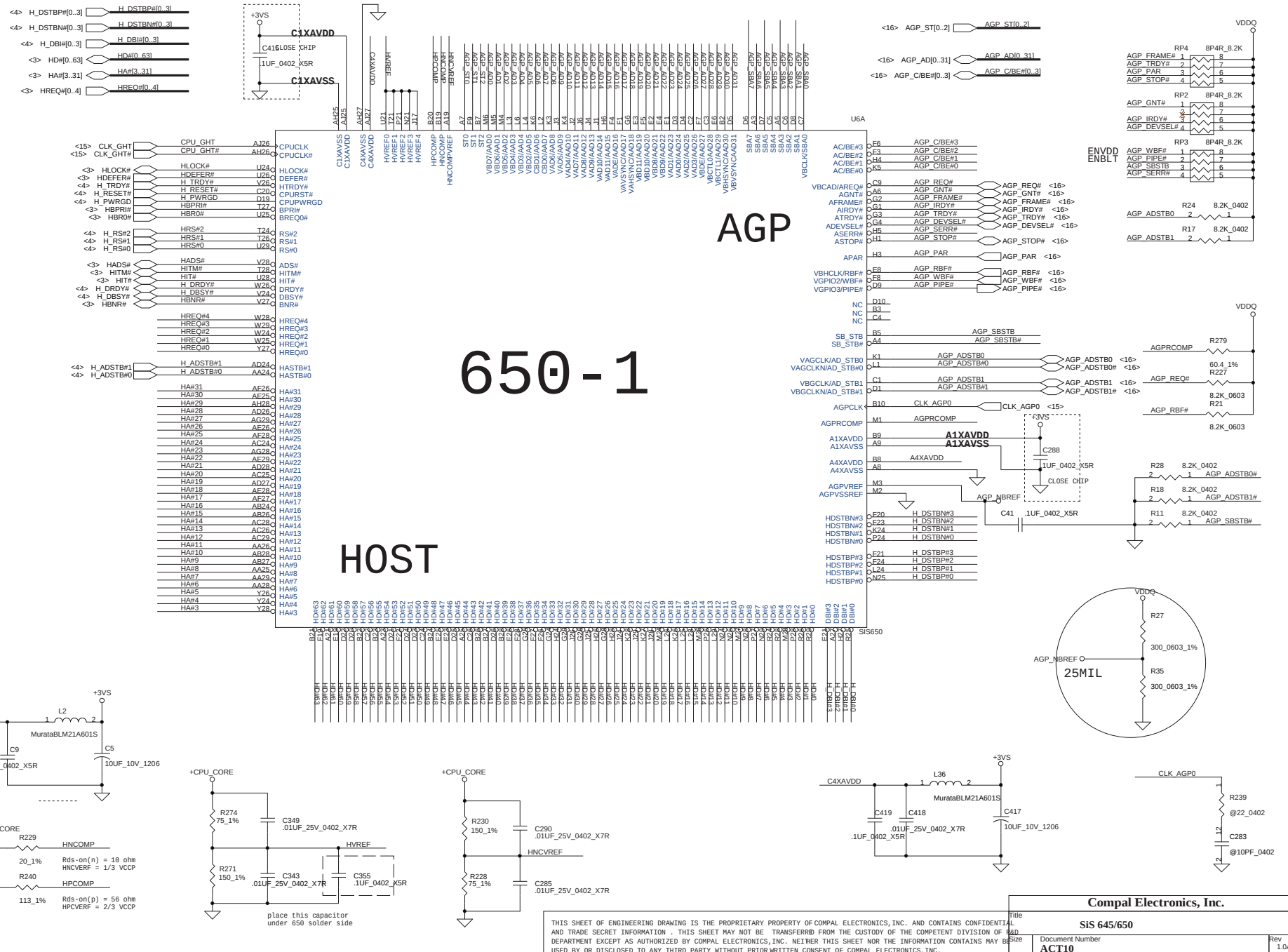
Dectect PCB Thermal

Fan1 Control circuit



COMPAL Electronics,Inc

Title	LM75 Thermal sensor & Fan control	
Size	Document Number ACT10	Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 6 of 45	

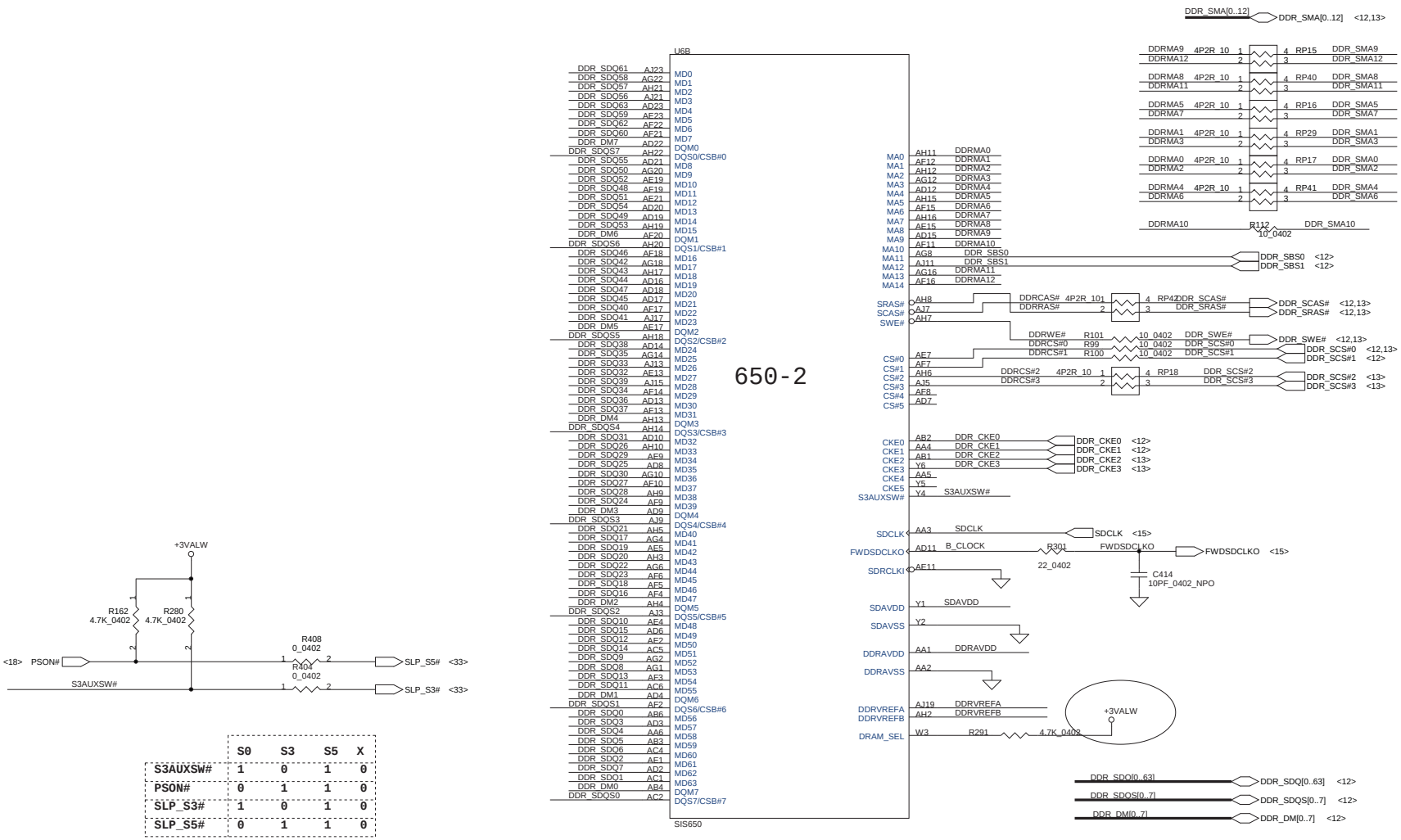


Compal Electronics, Inc.

Title: SiS 645/650

Size: Document Number: ACT10 Rev: 1.0A

Date: Thursday, May 30, 2002 Sheet 7 of 45



	S0	S3	S5	X
S3AUXSW#	1	0	1	0
PSON#	0	1	1	0
SLP_S3#	1	0	1	0
SLP_S5#	0	1	1	0

Compal Electronics, Inc.

Title: SiS 645/650

Size: | Document Number: ACT10 | Rev: 1.0A

Date: Thursday, May 30, 2002 | Sheet 8 of 45

NB Hardware Trap Table(For Mobil Only)

	0	1	Default
DLLEN#	enable PLL	disable PLL	0
DRAM_SEL	SDR	DDR	1(DDR)
TRAP0	normal	NB debug mode	0
TRAP1	Panel ID0		X
CSYNC	Panel ID1		X
RSYNC	enable VGA interface		1
LSYNC	Panel ID2		X

embedded pull-low (30~50K Ohm)
yes
yes
yes

CLK_NB14M — R248 @22_0402 — C299 @10PF_0402
ZCLK0 — R285 @22_0402 — C361 @10PF_0402

+1.8VS — R39 150_1% — C353 .1UF_0402_X5R — ZVREF — R38 150_1% — C357 .1UF_0402_X5R

<17> ZAD[0..15] ZAD[0..15]

U6C
SIS650

<15> ZCLK0	ZCLK0	V3	ZCLK
<17> ZUREQ	ZUREQ	U6	ZUREQ
<17> ZDREQ	ZDREQ	U1	ZDREQ
<17> ZSTB0	ZSTB0	T3	ZSTB0
<17> ZSTB#0	ZSTB#0	T1	ZSTB#0
<17> ZSTB1	ZSTB1	P1	ZSTB1
<17> ZSTB#1	ZSTB#1	P3	ZSTB#1
	ZAD0	T4	ZAD0
	ZAD1	R3	ZAD1
	ZAD2	T5	ZAD2
	ZAD3	T6	ZAD3
	ZAD4	R2	ZAD4
	ZAD5	R6	ZAD5
	ZAD6	R1	ZAD6
	ZAD7	R4	ZAD7
	ZAD8	P4	ZAD8
	ZAD9	N3	ZAD9
	ZAD10	P5	ZAD10
	ZAD11	P6	ZAD11
	ZAD12	N1	ZAD12
	ZAD13	N6	ZAD13
	ZAD14	N2	ZAD14
	ZAD15	N4	ZAD15
	ZVREF	U3	ZVREF
	VDDZCMP	V5	VDDZCMP
	ZCMP_N	U4	ZCMP_N
	ZCMP_P	U2	ZCMP_P
		V6	VSSZCMP
	Z4XAVDD	W1	Z1XAVDD
		W2	Z1XAVSS
	Z4XAVDD	V2	Z4XAVDD
		V1	Z4XAVSS
<17> 961_PCIRST#	R294 0_0402 PWRGD	Y3	PCIRST#
<6,18> PM_PWROK		W4	PWROK
<18,33,35> RSMRST#	R292 0_0402 AUXOK	W6	AUXOK
PID0_OLD	R257 1K_0402 TRAP0	D11	TRAP1
		E10	TRAP0
		C15	VOSCI
	ROUT	A12	ROUT
	GOUT	B13	GOUT
	BOUT	A13	BOUT
	HSYNC	F13	HSYNC
	VSYNC	E13	VSYNC
	VGPIO0	D13	VGPIO0
	VGPIO1	D12	VGPIO1
	INT#A	B11	INT#A
	CSYNC	E12	CSYNC
	RSYNC	A11	RSYNC
	LSYNC	F12	LSYNC
	VCOMP	E14	VCOMP
	VRSET	D14	VRSET
	VVBWN	F14	VVBWN
	DACAVDD1	B12	DACAVDD1
	DACAVSS1	C12	DACAVSS1
	DACAVDD2	C13	DACAVDD2
	DACAVSS2	C14	DACAVSS2
	DCLKAVDD	B15	DCLKAVDD
	DCLKAVSS	A15	DCLKAVSS
	ECLKAVDD	B14	ECLKAVDD
	ECLKAVSS	A14	ECLKAVSS
	ENTEST	F10	ENTEST
	DLLEN#	E11	DLLEN#
	TESTMODE0	C11	TESTMODE0
	TESTMODE1	F11	TESTMODE1
	TESTMODE2	A10	TESTMODE2

CLK_NB14M — CLK_NB14M <15>

ROUT — R13 0_0402 CRT_R_SIS — CRT_R_SIS <16>
GOUT — R12 0_0402 CRT_G_SIS — CRT_G_SIS <16>
BOUT — R14 0_0402 CRT_B_SIS — CRT_B_SIS <16>

HSYNC — R263 33_0402 HSYNC_SIS — HSYNC_SIS <16>
VSYNC — R253 33_0402 VSYNC_SIS — VSYNC_SIS <16>

VGPIO0 — RP68 4P2R_100 — DDCCL_SIS — DDCCL_SIS <16>
VGPIO1 — DDCDA_SIS — DDCDA_SIS <16>

INT#A — SIS_PIRQA# <16>

PID1_OLD
RSYNC
PID2_OLD

VCOMP — R250 130_1%

Ap Note:
DACAVDD1 & DACAVDD2 connect together
DACAVSS1 & DACAVSS2 connect together

for 650 only
+3VS
RSYNC — R234 4.7K_0402
PID0_OLD — R254 @10K_0402
PID1_OLD — R265 @10K_0402
PID2_OLD — R264 @10K_0402

ENTEST — R266 4.7K_0402
PWRGD — C388 .1UF_0402_X5R
AUXOK — C374 @.1UF_0402_X5R

+3VS — L28 MurataBLM21A601S — Z4XAVDD
C45 10UF_10V_1206 — C372 .01UF_25V_0402_X7R

C382 .01UF_25V_0402_X7R — Z4XAVDD

+1.8VS — R277 0_0603 — C366 .1UF_0402_X5R — C348 .01UF_25V_0402_X7R
R286 56_0402 ZCMP_N
R290 56_0402 ZCMP_P

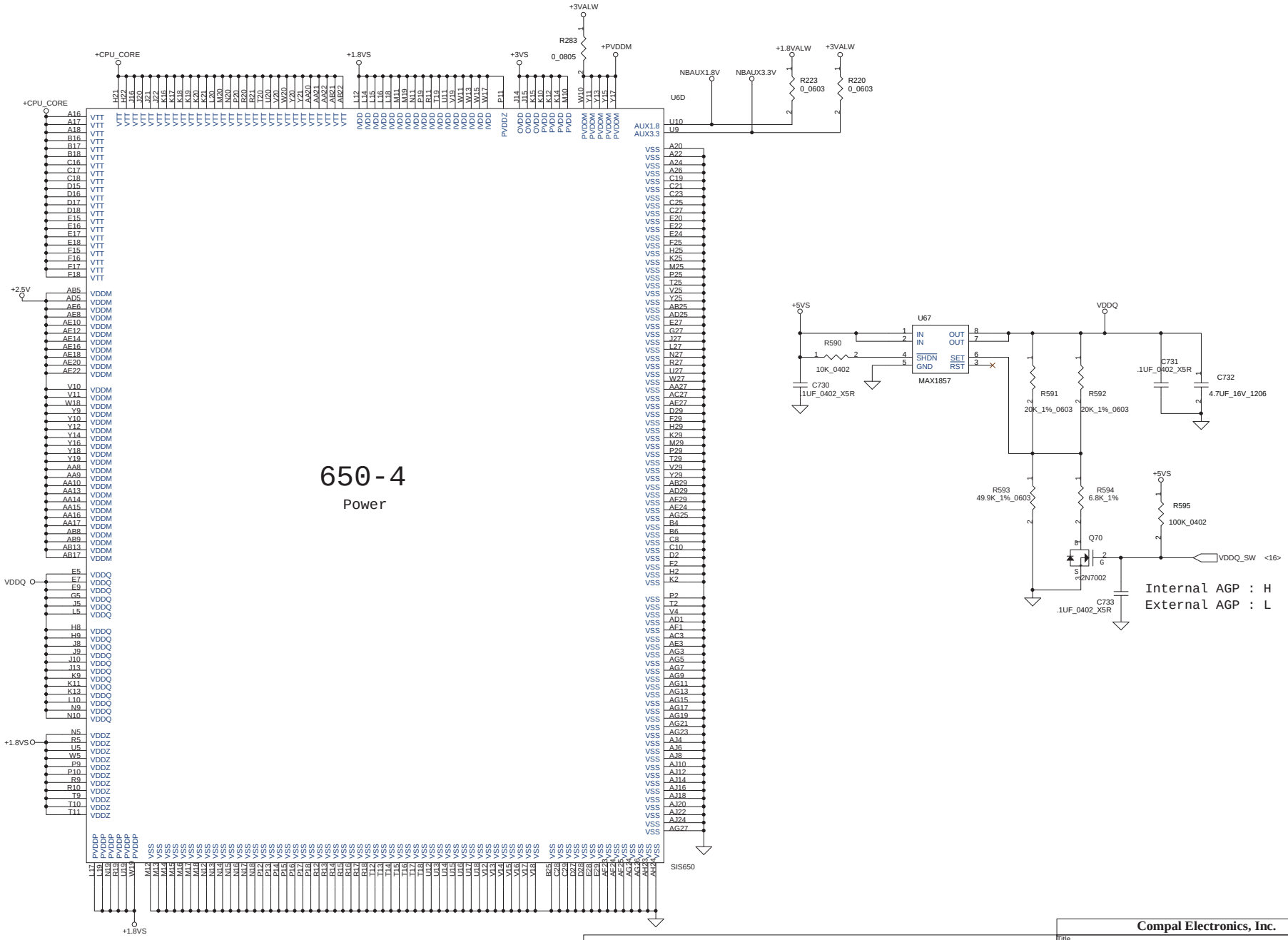
L13 MurataBLM21A601S — +3VS — DCLKAVDD — C292 .01UF_25V_0402_X7R — C291 .1UF_0402_X5R — C275 10UF_10V_1206

L14 MurataBLM21A601S — +3VS — ECLKAVDD — C294 .01UF_25V_0402_X7R — C293 .1UF_0402_X5R — C268 10UF_10V_1206

VVBWN — C300 .1UF_0402_X5R
VCOMP — C301 .1UF_0402_X5R

+1.8VS — L17 MurataBLM21A601S — DACAVDD2 — C297 1UF_0402_X5R — C286 1UF_10V_0603_X5R — C341 10UF_10V_1206

Compal Electronics, Inc.			
Title: SiS 645/650			
Size	Document Number: ACT10		Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 9 of 45		



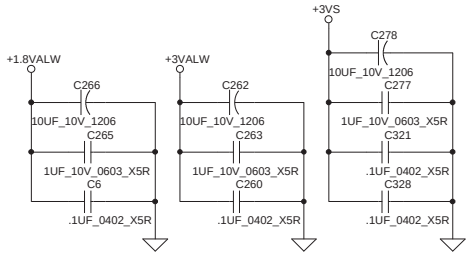
Compal Electronics, Inc.

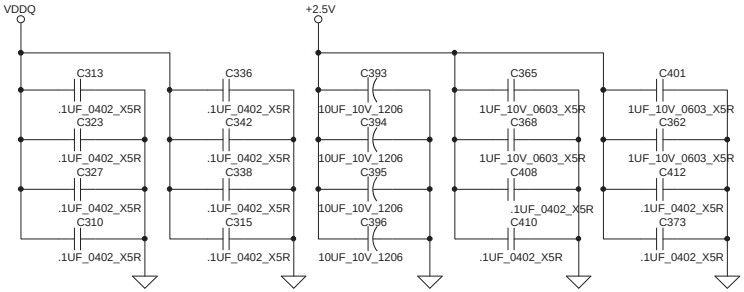
Title	SiS 645/650	
Size	Document Number ACT10	Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 10 of 45	

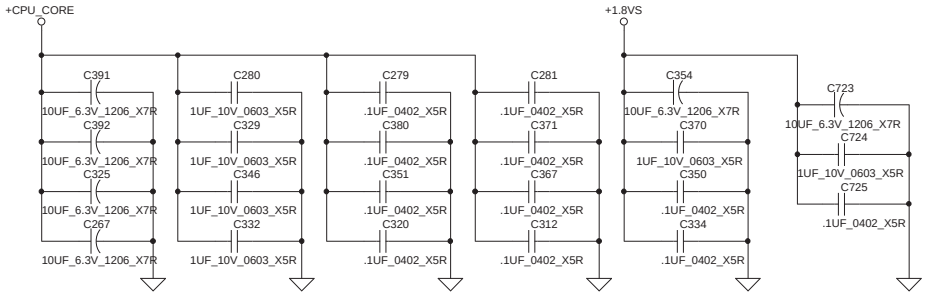
Layout note : Processor system bus

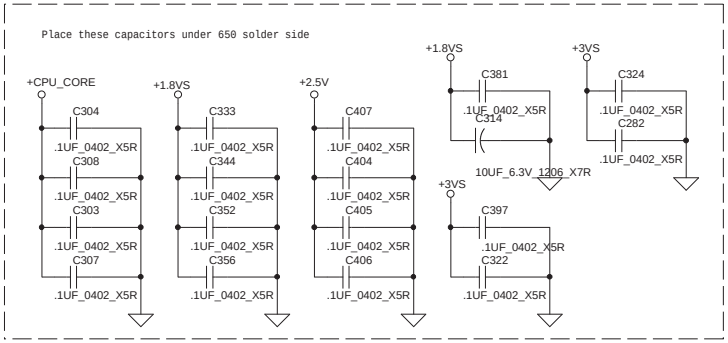
Distribute as close as possible to Processor Quadrant.(between VTTFSB and VSS pin)

CHECK SiS 650 CAP.
IT NEED HOW MANY ESR









Compal Electronics, Inc.		
Title: SiS 645/650 Decoupling		
Size	Document Number: ACT10	Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 11 of 45	

DDR SWAP NOW, SO DATA NOT CORRECT

Layout note

Place these resistor closely DIMM0, all trace length<750mil

RP5 4P2R_10: DDR_SDQ1, DDR_SDQ5 / DDR_DQ1, DDR_DQ5
RP30 4P2R_10: DDR_SDQ2, DDR_SDQ7 / DDR_DQ2, DDR_DQ7
RP6 4P2R_10: DDR_DM0, DDR_SDQS0 / DDR_F_DM0, DDR_DQS0
RP31 4P2R_10: DDR_SDQ4, DDR_SDQ3 / DDR_DQ4, DDR_DQ3
RP7 4P2R_10: DDR_SDQ0, DDR_SDQ6 / DDR_DQ0, DDR_DQ6
RP32 4P2R_10: DDR_SDQ14, DDR_SDQ11 / DDR_DQ14, DDR_DQ11
RP8 4P2R_10: DDR_SDQ12, DDR_SDQ15 / DDR_DQ12, DDR_DQ15
RP33 4P2R_10: DDR_DM1, DDR_SDQS1 / DDR_F_DM1, DDR_DQS1
RP9 4P2R_10: DDR_SDQ9, DDR_SDQ8 / DDR_DQ9, DDR_DQ8
RP34 4P2R_10: DDR_SDQ10, DDR_SDQ13 / DDR_DQ10, DDR_DQ13
RP10 4P2R_10: DDR_SDQ20, DDR_SDQ19 / DDR_DQ20, DDR_DQ19
RP35 4P2R_10: DDR_SDQ17, DDR_SDQ16 / DDR_DQ17, DDR_DQ16
RP11 4P2R_10: DDR_SDQS2, DDR_DM2 / DDR_DQS2, DDR_F_DM2
RP36 4P2R_10: DDR_SDQ18, DDR_SDQ21 / DDR_DQ18, DDR_DQ21
RP12 4P2R_10: DDR_SDQ23, DDR_SDQ22 / DDR_DQ23, DDR_DQ22
RP37 4P2R_10: DDR_SDQ31, DDR_SDQ25 / DDR_DQ31, DDR_DQ25
RP13 4P2R_10: DDR_SDQ28, DDR_SDQ29 / DDR_DQ28, DDR_DQ29
RP38 4P2R_10: DDR_SDQS3, DDR_DM3 / DDR_DQS3, DDR_F_DM3
RP14 4P2R_10: DDR_SDQ26, DDR_SDQ24 / DDR_DQ26, DDR_DQ24
RP39 4P2R_10: DDR_SDQ30, DDR_SDQ27 / DDR_DQ30, DDR_DQ27

RP43 4P2R_10: DDR_SDQ36, DDR_SDQ38 / DDR_DQ36, DDR_DQ38
RP20 4P2R_10: DDR_SDQ37, DDR_SDQ32 / DDR_DQ37, DDR_DQ32
RP44 4P2R_10: DDR_SDQS4, DDR_DM4 / DDR_DQS4, DDR_F_DM4
RP21 4P2R_10: DDR_SDQ39, DDR_SDQ33 / DDR_DQ39, DDR_DQ33
RP45 4P2R_10: DDR_SDQ34, DDR_SDQ35 / DDR_DQ34, DDR_DQ35
RP22 4P2R_10: DDR_SDQ43, DDR_SDQ44 / DDR_DQ43, DDR_DQ44
RP46 4P2R_10: DDR_SDQ41, DDR_SDQ45 / DDR_DQ41, DDR_DQ45
RP23 4P2R_10: DDR_DM5, DDR_SDQS5 / DDR_F_DM5, DDR_DQS5
RP47 4P2R_10: DDR_SDQ40, DDR_SDQ42 / DDR_DQ40, DDR_DQ42
RP24 4P2R_10: DDR_SDQ47, DDR_SDQ46 / DDR_DQ47, DDR_DQ46
RP48 4P2R_10: DDR_SDQ49, DDR_SDQ48 / DDR_DQ49, DDR_DQ48
RP25 4P2R_10: DDR_SDQ53, DDR_SDQ50 / DDR_DQ53, DDR_DQ50
RP49 4P2R_10: DDR_SDQS6, DDR_DM6 / DDR_DQS6, DDR_F_DM6
RP26 4P2R_10: DDR_SDQ51, DDR_SDQ52 / DDR_DQ51, DDR_DQ52
RP50 4P2R_10: DDR_SDQ55, DDR_SDQ54 / DDR_DQ55, DDR_DQ54
RP27 4P2R_10: DDR_SDQ58, DDR_SDQ60 / DDR_DQ58, DDR_DQ60
RP51 4P2R_10: DDR_SDQ57, DDR_SDQ56 / DDR_DQ57, DDR_DQ56
RP28 4P2R_10: DDR_DM7, DDR_SDQS7 / DDR_F_DM7, DDR_DQS7
RP52 4P2R_10: DDR_SDQ62, DDR_SDQ61 / DDR_DQ62, DDR_DQ61
RP71 4P2R_10: DDR_SDQ63, DDR_SDQ59 / DDR_DQ63, DDR_DQ59

Layout note

Place these resistor closely DIMM0, all trace length<=750mil

<8> DDR_SDQ[0..63] → DDR_SDQ[0..63]
<8> DDR_DM[0..7] → DDR_DM[0..7]
<8> DDR_SDQS[0..7] → DDR_SDQS[0..7]

+2.5V

JP2 (MOLEX 67589-2003 200P STD)

VREF	1	2	VREF
VSS	3	4	VSS
DDR_DQ1	5	6	DDR_DQ5
DDR_DQ2	7	8	DDR_DQ7
DQ1	9	10	VDD
VDD	11	12	DDR_F_DM0
DDR_DQS0	13	14	DDR_DQ3
DDR_DQ4	15	16	VSS
DDR_DQ0	17	18	DDR_DQ6
DDR_DQ14	19	20	DDR_DQ11
VDD	21	22	DQ12
DDR_DQ12	23	24	VDD
DDR_DQS1	25	26	DDR_DQ15
VSS	27	28	DDR_F_DM1
DDR_DQ9	29	30	DM1
DDR_DQ10	31	32	DDR_DQ8
DQ11	33	34	DDR_DQ13
VDD	35	36	VDD
<15> DDR_CLK1	37	38	VDD
<15> DDR_CLK1#	39	40	VSS
DDR_DQ20	41	42	DDR_DQ19
DDR_DQ17	43	44	DDR_DQ16
VDD	45	46	DDR_F_DM2
DDR_DQS2	47	48	DM2
DDR_DQ18	49	50	DDR_DQ21
VSS	51	52	DQ22
DDR_DQ23	53	54	VSS
DDR_DQ31	55	56	DDR_DQ22
VDD	57	58	DDR_DQ25
DDR_DQ28	59	60	VDD
DDR_DQS3	61	62	DDR_DQ29
VSS	63	64	DDR_F_DM3
DDR_DQ26	65	66	VSS
DDR_DQ30	67	68	DDR_DQ24
DDR_DQ27	69	70	DDR_DQ27
VDD	71	72	VDD
CB0	73	74	CB4
CB1	75	76	CB5
VSS	77	78	VSS
DQS8	79	80	DM8
CB2	81	82	CB6
VDD	83	84	VDD
CB3	85	86	CB7
DU	87	88	DU/RESET#
VSS	89	90	VSS
<15> DDR_CLK0	91	92	VSS
<15> DDR_CLK0#	93	94	VDD
DDR_CKE1	95	96	DDR_CKE0
VDD	97	98	DU/BA2
DDR_SMA12	99	100	DDR_SMA11
DDR_SMA9	101	102	DDR_SMA8
VSS	103	104	A8
DDR_SMA7	105	106	DDR_SMA6
DDR_SMA5	107	108	DDR_SMA4
DDR_SMA3	109	110	DDR_SMA2
DDR_SMA1	111	112	DDR_SMA0
VDD	113	114	VDD
DDR_SMA10	115	116	BA1
DDR_F_SBS0	117	118	DDR_SRAS#
<8,13> DDR_SWE#	119	120	DDR_SCAS#
<8,13> DDR_SCS#0	121	122	DDR_SCS#1
DU	123	124	S1#
VSS	125	126	DU
DDR_DQ36	127	128	VSS
DDR_DQ37	129	130	DDR_DQ38
VDD	131	132	DDR_DQ32
DDR_DQS4	133	134	VDD
DDR_DQ39	135	136	DDR_F_DM4
VSS	137	138	DDR_DQ33
DDR_DQ34	139	140	VSS
DDR_DQ43	141	142	DDR_DQ35
VDD	143	144	DDR_DQ44
DDR_DQ41	145	146	VDD
DDR_DQS5	147	148	DDR_DQ45
VSS	149	150	DDR_F_DM5
DDR_DQ40	151	152	VSS
DDR_DQ47	153	154	DDR_DQ42
VDD	155	156	DDR_DQ46
VDD	157	158	VDD
VSS	159	160	DDR_CLK2# <15>
VSS	161	162	DDR_CLK2 <15>
DDR_DQ49	163	164	VSS
DDR_DQ53	165	166	DDR_DQ48
VDD	167	168	DDR_DQ50
DDR_DQS6	169	170	VDD
DDR_DQ51	171	172	DDR_F_DM6
DDR_DQ50	173	174	DDR_DQ52
VSS	175	176	VSS
DDR_DQ55	177	178	DDR_DQ54
DDR_DQ58	179	180	DDR_DQ60
VDD	181	182	VDD
DDR_DQ57	183	184	DDR_DQ56
DDR_DQS7	185	186	DDR_F_DM7
VSS	187	188	DM7
DDR_DQ62	189	190	VSS
DDR_DQ63	191	192	DDR_DQ61
VDD	193	194	DDR_DQ59
<13,15,18,20> SMB_DATA	195	196	VDD
<13,15,18,20> SMB_CLK	197	198	SA0
+3VS	199	200	SA1
VDD_SPD			SA2
VDD_ID			DU

SDREF_R — L54 1 2 SDREF
C451 MurataBLM21A601S
.1UF_16V_0402_Y5V

DDR_DQ[0..63] <13>
DDR_F_DM[0..7] <13>
DDR_DQS[0..7] <13>
DDR_SMA[0..12] <8,13>

DDR_SRAS# <8,13>
DDR_SCAS# <8,13>
DDR_SCS#1 <8>

Layout note
Place these resistor closely DIMM0, all trace length Max=1.3"

+2.5V
RP58 4P2R_470: DDR_CKE0, DDR_CKE1
+1.25VS
R132: DDR_SCS#1 — 33_0402
PULL -UP AT PAGE 13

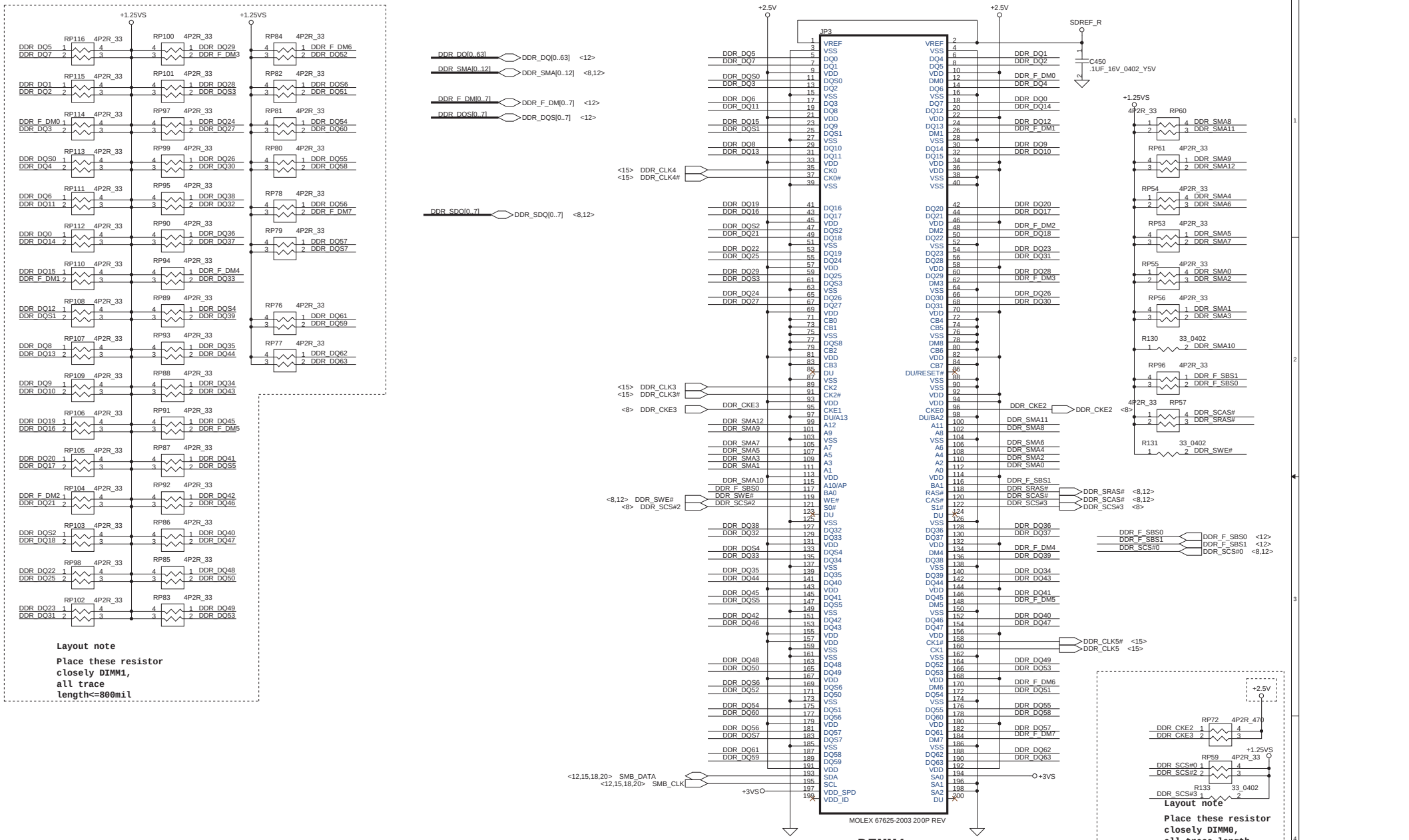
4P2R_10 RP19: DDR_F_SBS1 <13> → DDR_SBS1 <8>, DDR_SBS0 <8>
DDR_F_SBS0 <13>

DIMM0

top side

Compal Electronics, Inc.

Title: **DDR-SODIMM SLOT1**
Size: | Document Number: **ACT10** | Rev: 1.0A
Date: Thursday, May 30, 2002 | Sheet 12 of 45



Compal Electronics, Inc.

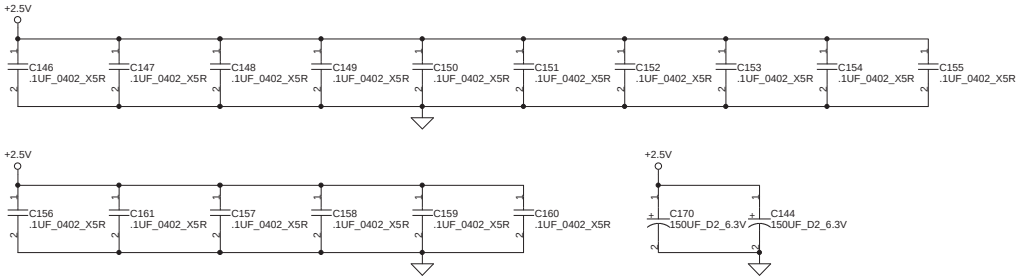
Title: DDR-SODIMM SLOT1

Size: | Document Number: ACT10 | Rev: 1.0A

Date: Thursday, May 30, 2002 | Sheet 13 of 45

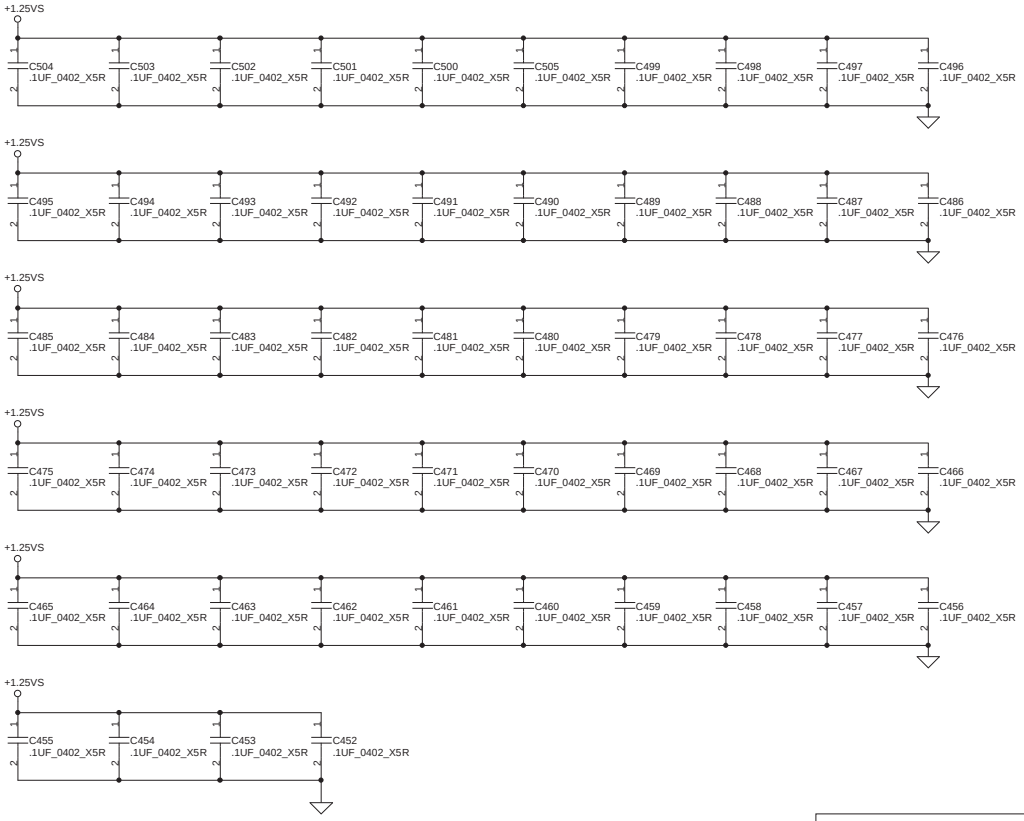
Layout note :

Distribute as close as possible to DDR-SODIMM.



Layout note :

Place one cap close to every 2 pull up resistors termination to +1.25V



Compal Electronics, Inc.

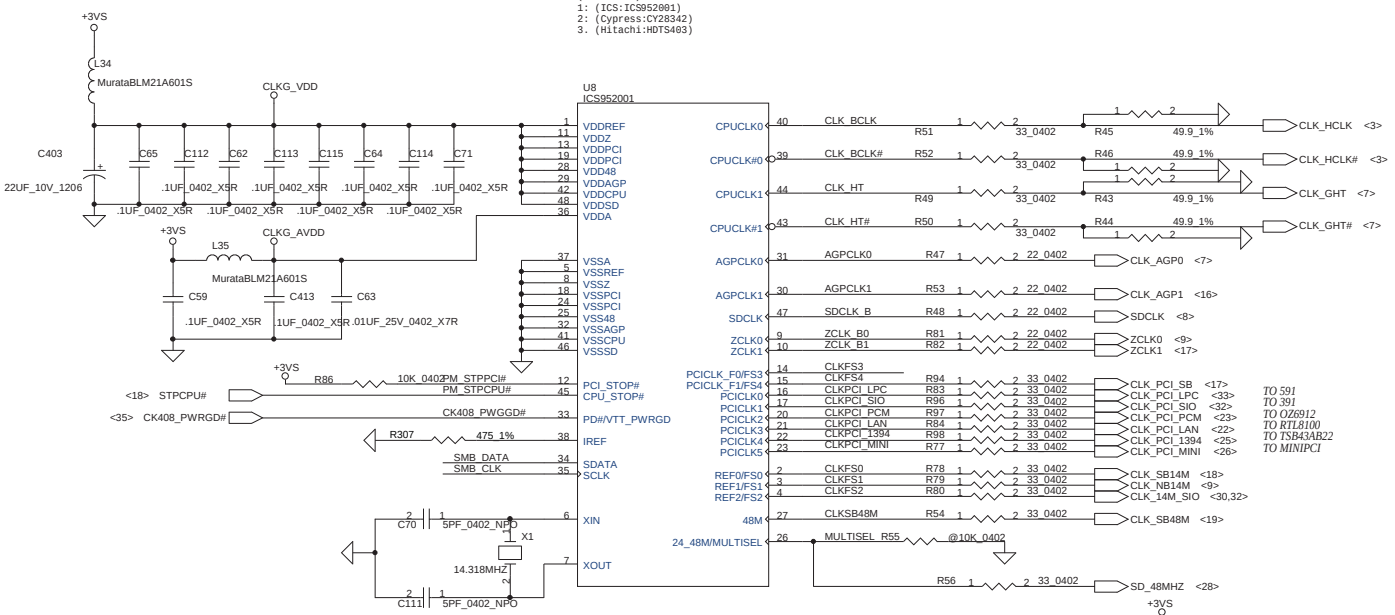
Title: **DDR SODIMM Decoupling**

Size: | Document Number: **ACT10** | Rev: 1.0A

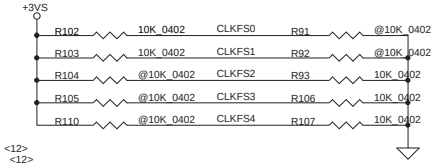
Date: Thursday, May 30, 2002 | Sheet 14 of 45

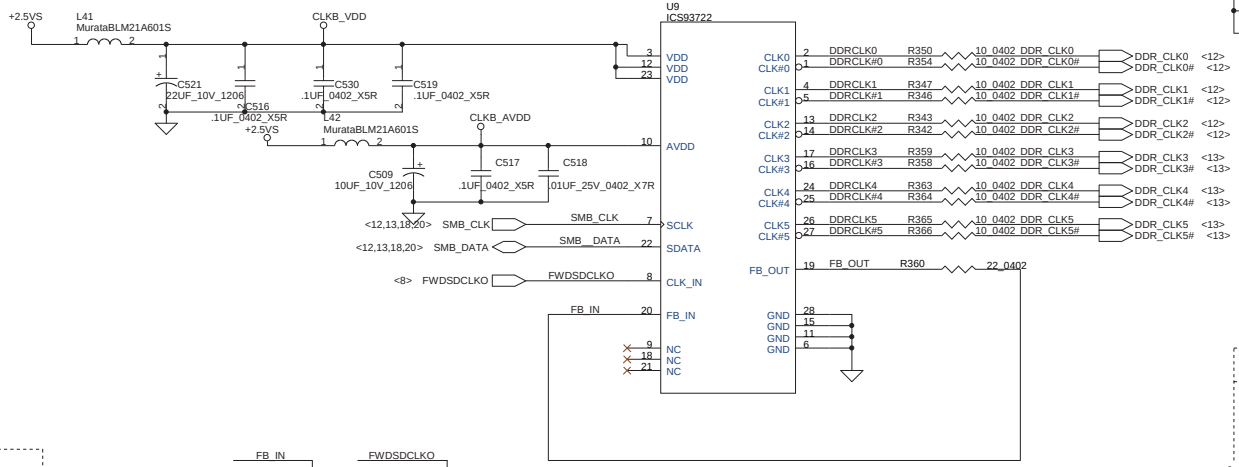
Main Clock Generator

(3 OPTIONS)
1: (ICS:ICS952001)
2: (Cypress:CY28342)
3. (Hitachi:HDTS403)

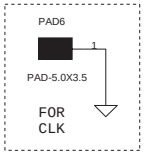


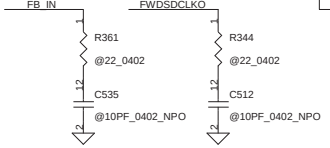
ICS suggestion 14.318MHz > 36pF, C273, C274 4pF





FS4	FS3	FS2	FS1	FS0	CPU	DDR	ZCLK	AGP	PCI
1	1	0	0	0	100.0	133.0	80.0	66.7	33.3
1	1	0	0	1	100.0	100.0	80.0	66.7	33.3
0	0	1	1	1	100.0	133.3	80.0	66.7	33.3
* 0	0	0	1	1	100.0	133.3	66.7	66.7	33.3





Compal Electronics, Inc.

Title: **Clock Generator**

Size: | Document Number: **ACT10** | Rev: 1.0A

Date: Thursday, May 30, 2002 | Sheet 15 of 45

AGP 140 Pin connector

JP4

FOXCONN_QTS0140A-1121_M140P_VGA

VDDQ_SW : (5V Level)
L : Enternal AGP
H : Internal VGA

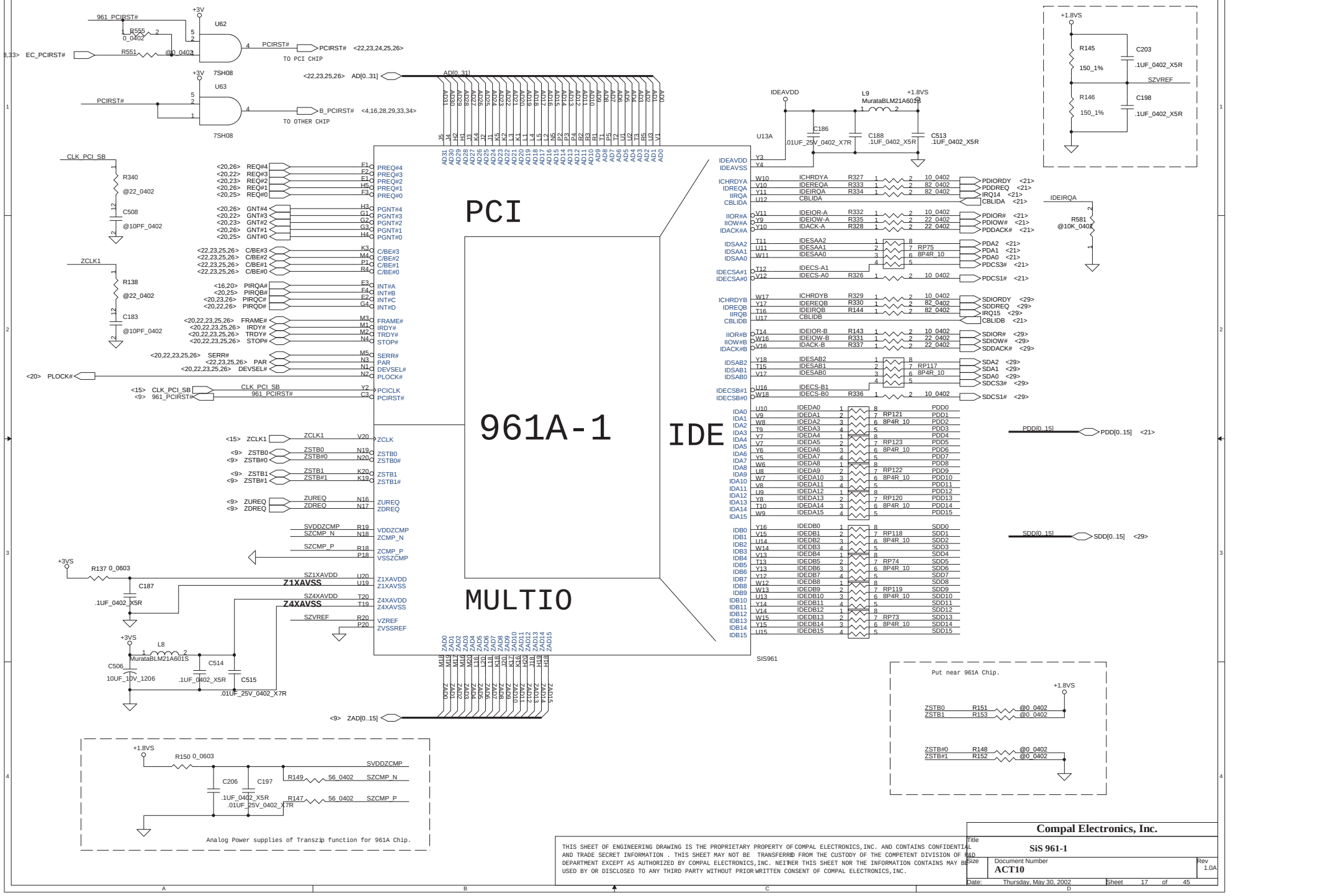
LVDS_PRES# : (3V Level)
H : Enternal AGP
L : Internal VGA

FDS4435: P CHANNAL

CRT Connector

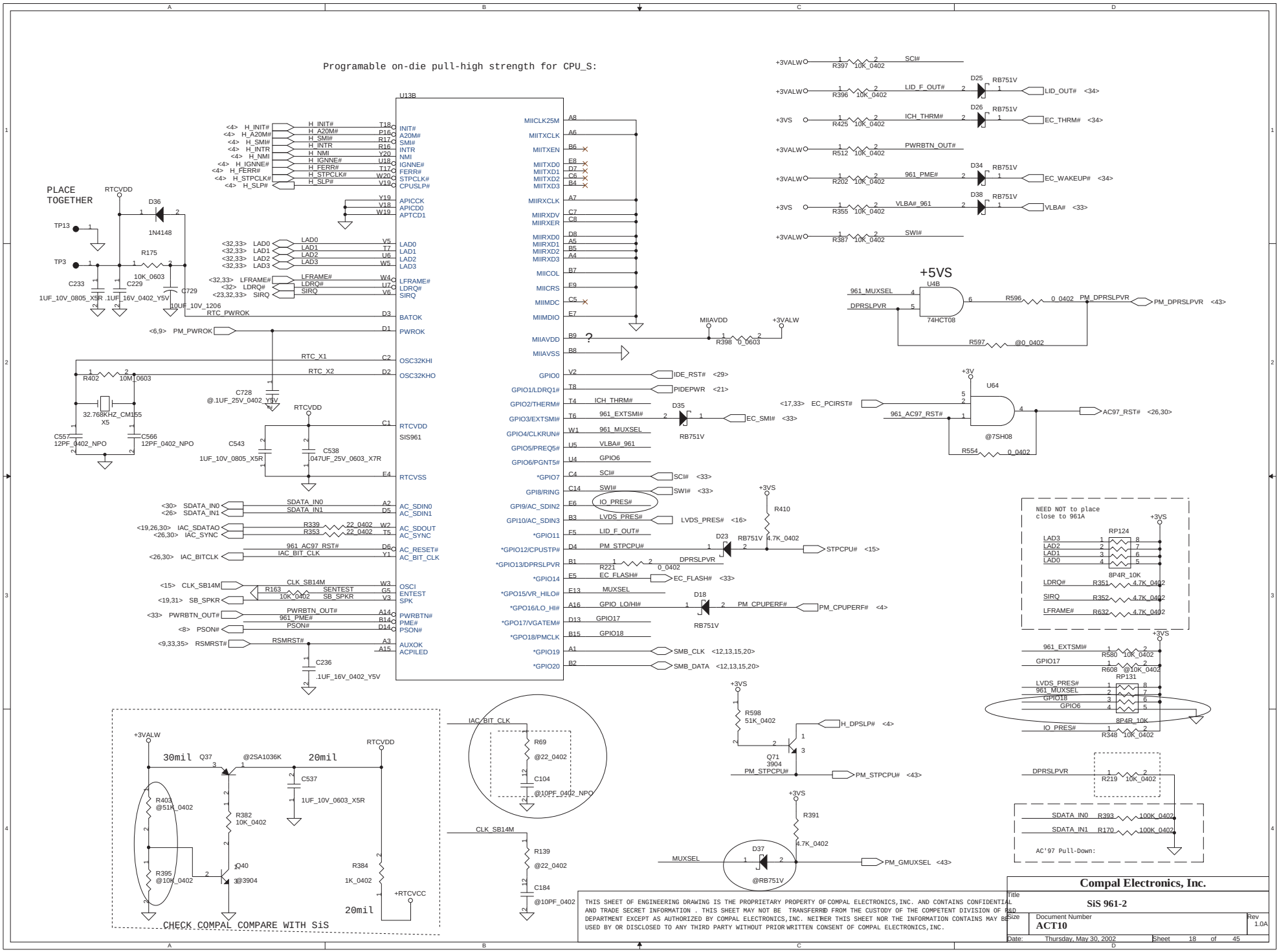
FOXCONNDZ11A91-L8

Compal Electronics, Inc.	
Title	AGPConn. & CRT
Size	Document Number: ACT10 — Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 16 of 45



Compal Electronics, Inc.

Title	SiS 961-1		
Size	Document Number ACT10		Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 17	of	45



THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS,INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION . THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS,INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS,INC.

Compal Electronics, Inc.

Title	SiS 961-2	
Size	Document Number ACT10	Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 18 of 45	

FOR 961 USB PIN DEFINITION

Control 0 : port 0 UV0+ B18 UV0- C18 OC0# G20
Control 0 : port 1 UV1+ E14 UV1- D15 OC1# J16
Control 0 : port 2 UV2+ E16 UV2- E15 OC2# H17
HW TRIP PULL LOW 1K SOUTH BIRDGE DEBUG MODE

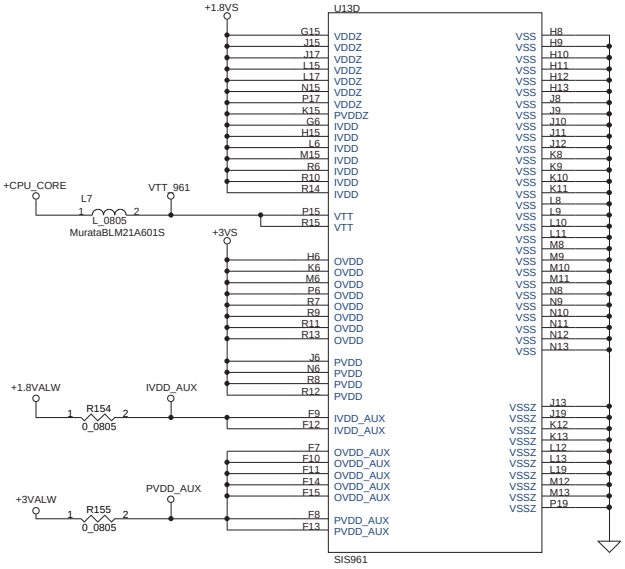
Control 1 : port 3 UV3+ D18 UV3- D19 OC3# G17
Control 1 : port 4 UV4+ E18 UV4- F18 OC4# H16
Control 1 : port 5 UV5+ G18 UV5- G19 OC5# G16
HW TRIP PULL LOW 1K TRIP FROM PCI AD0..31
PULL HIGH TRIP FROM FLASH ROM

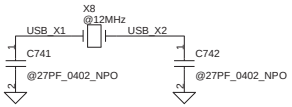
FOR 962 USB PIN DEFINITION

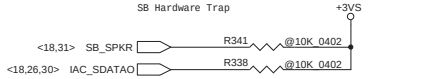
Control 0 : port 0 UV0+ B18 UV0- C18 OC0# G20
Control 0 : port 3 UV3+ E18 UV3- F18 OC3# H16

Control 1 : port 1 UV1+ D18 UV1- D19 OC1# G17
Control 1 : port 4 UV4+ E16 UV4- E15 OC4# H17

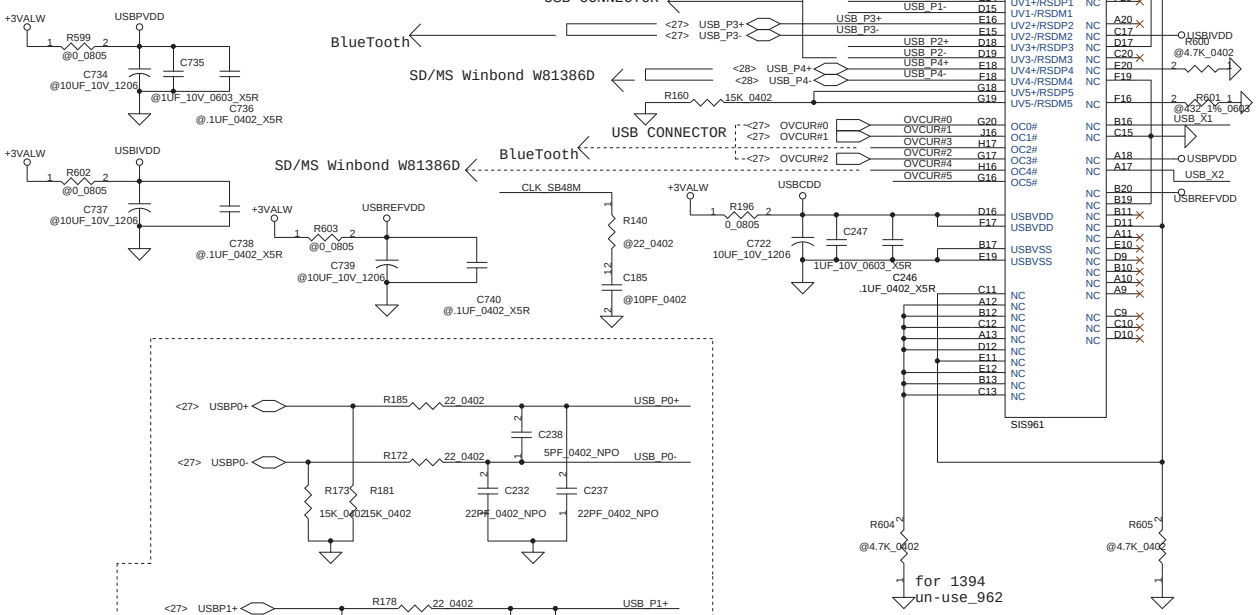
Control 2 : port 2 UV2+ E14 UV2- D15 OC2# J16
Control 2 : port 5 UV5+ G18 UV5- G19 OC5# G16

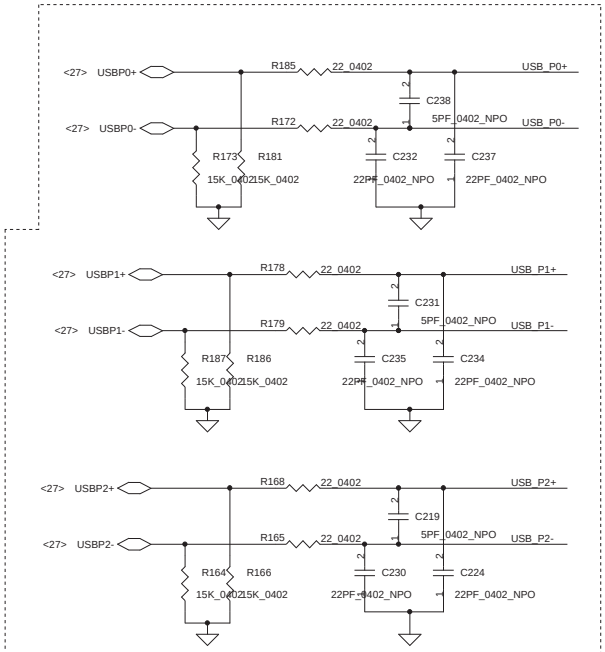


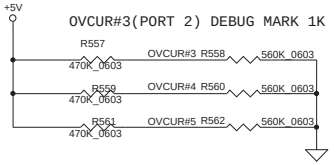




	0	1	Default
SPKR(LPC addr mapping)	disable	enable	0
SDATO(PCICLK PLL)	enable	disable	0
OC2-(SB debug mode)	enable	disable	1
OC5-(Trap mode)	PCI AD	ROM	1



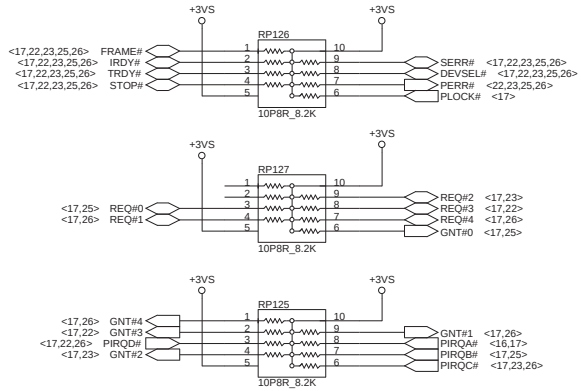


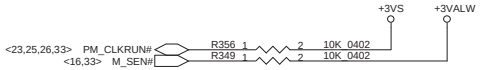


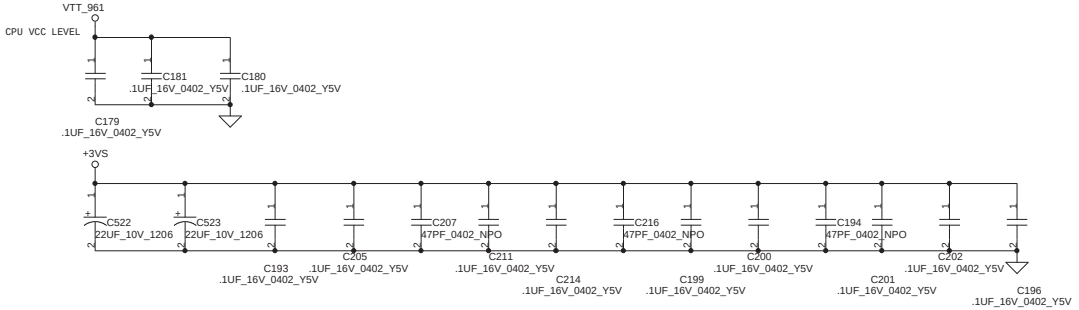
OVCUR#5 : PULL UP TRAP FROM SYSTEM FLASH ROM
PULL DOWN 1K TRAP FROM PCI AD31..0

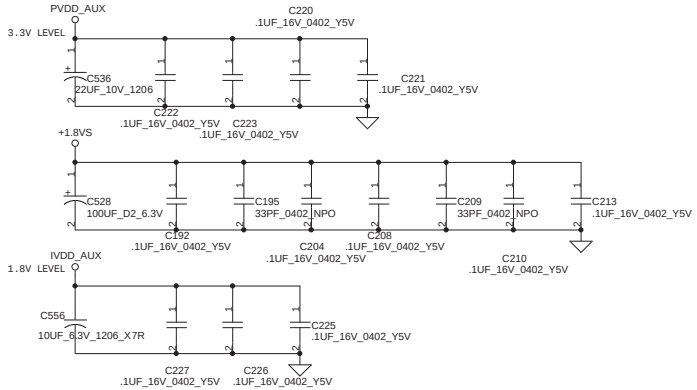
Compal Electronics, Inc.

Title: SiS 961(3) USB
Size: Document Number: ACT10 Rev: 1.0A
Date: Thursday, May 30, 2002 Sheet 19 of 45









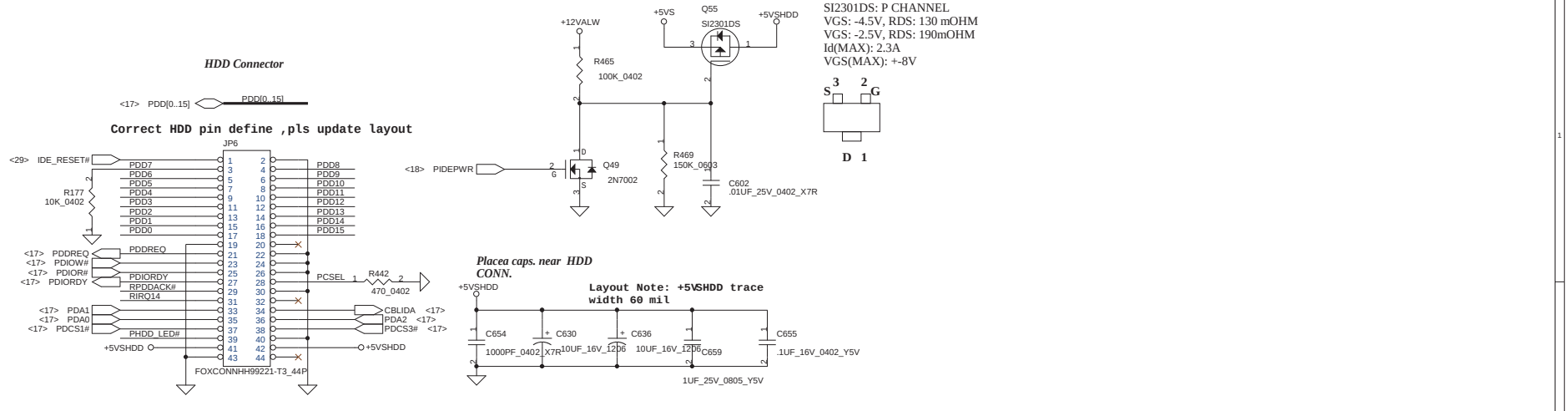
Compal Electronics, Inc.

Title: **SiS961 Decoupling & Pull-Up**

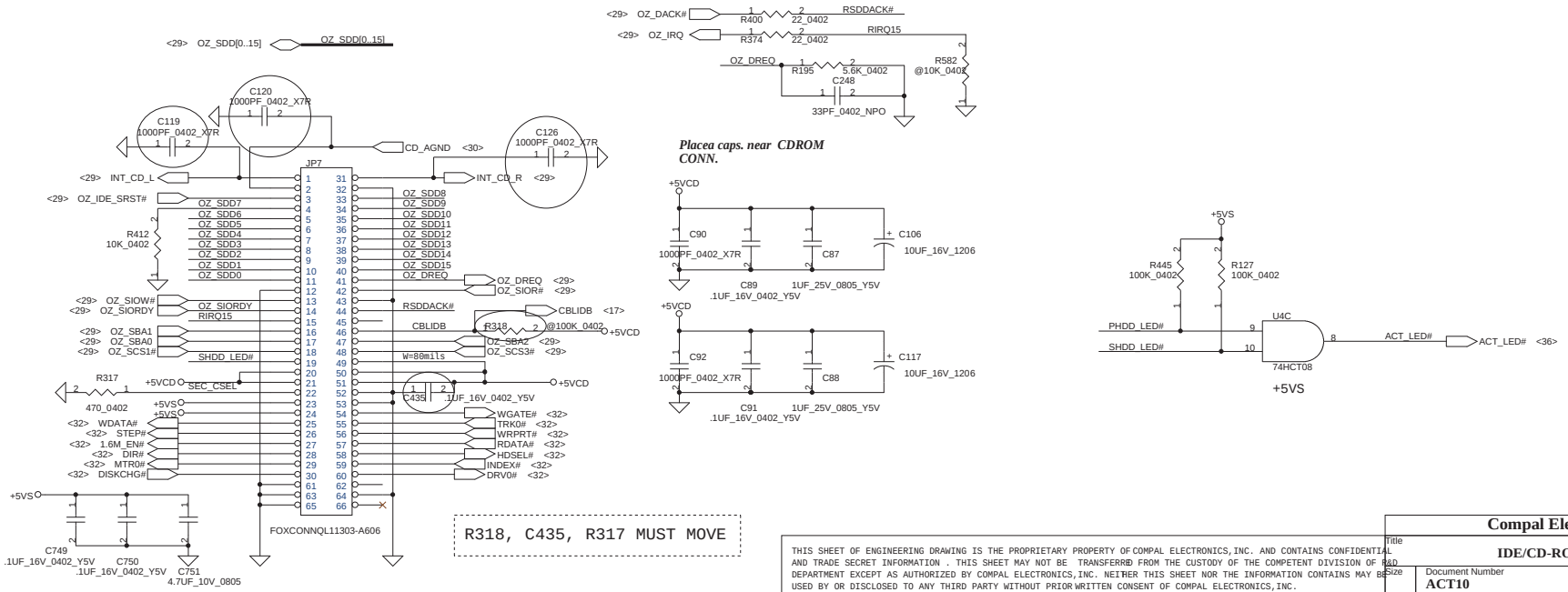
Size: | Document Number: **ACT10** | Rev: 1.0A

Date: Thursday, May 30, 2002 | Sheet 20 of 45

HDD Connector



CD-ROM Connector



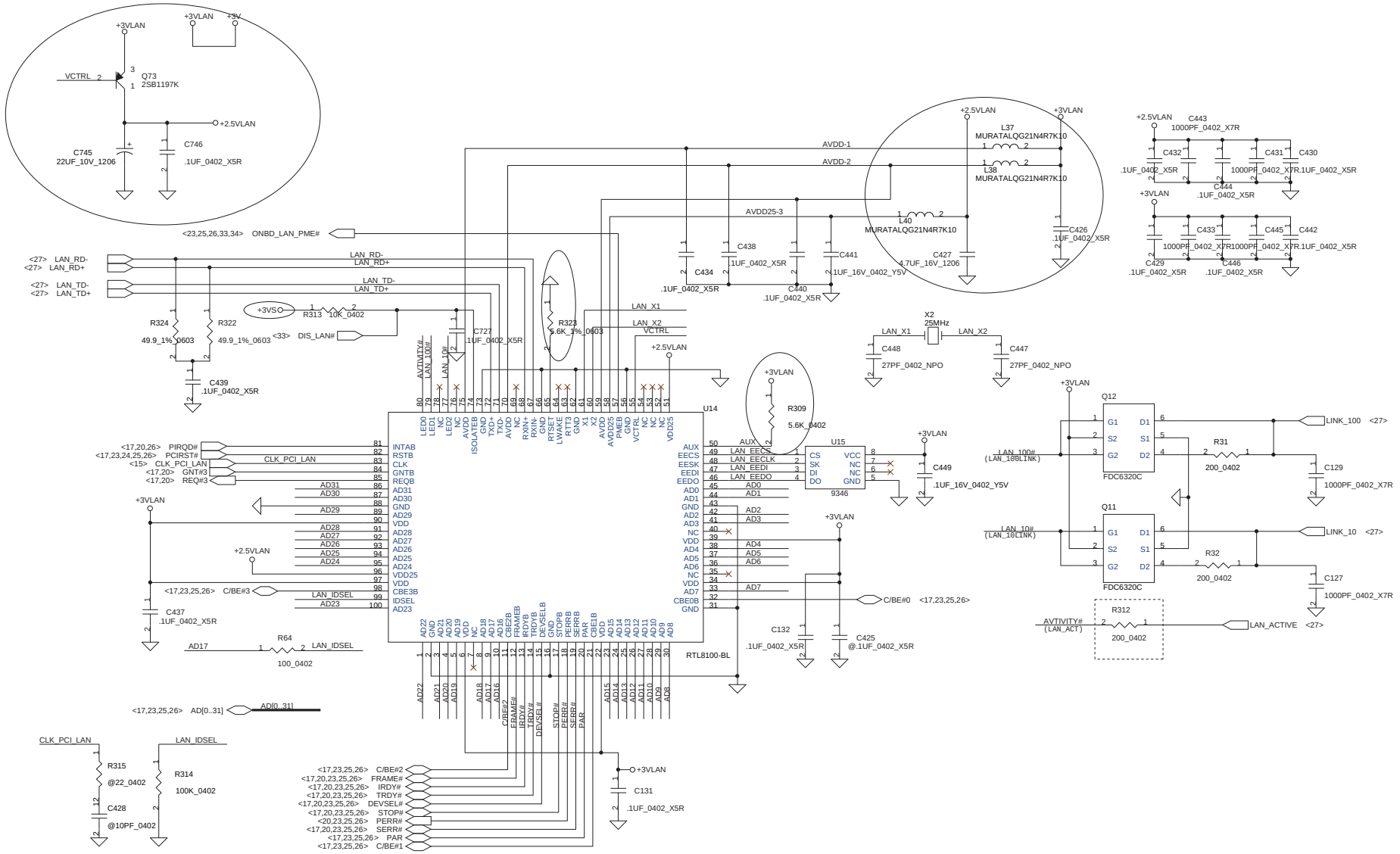
R318, C435, R317 MUST MOVE

Compal Electronics, Inc.

Title: **IDE/CD-ROM Module**

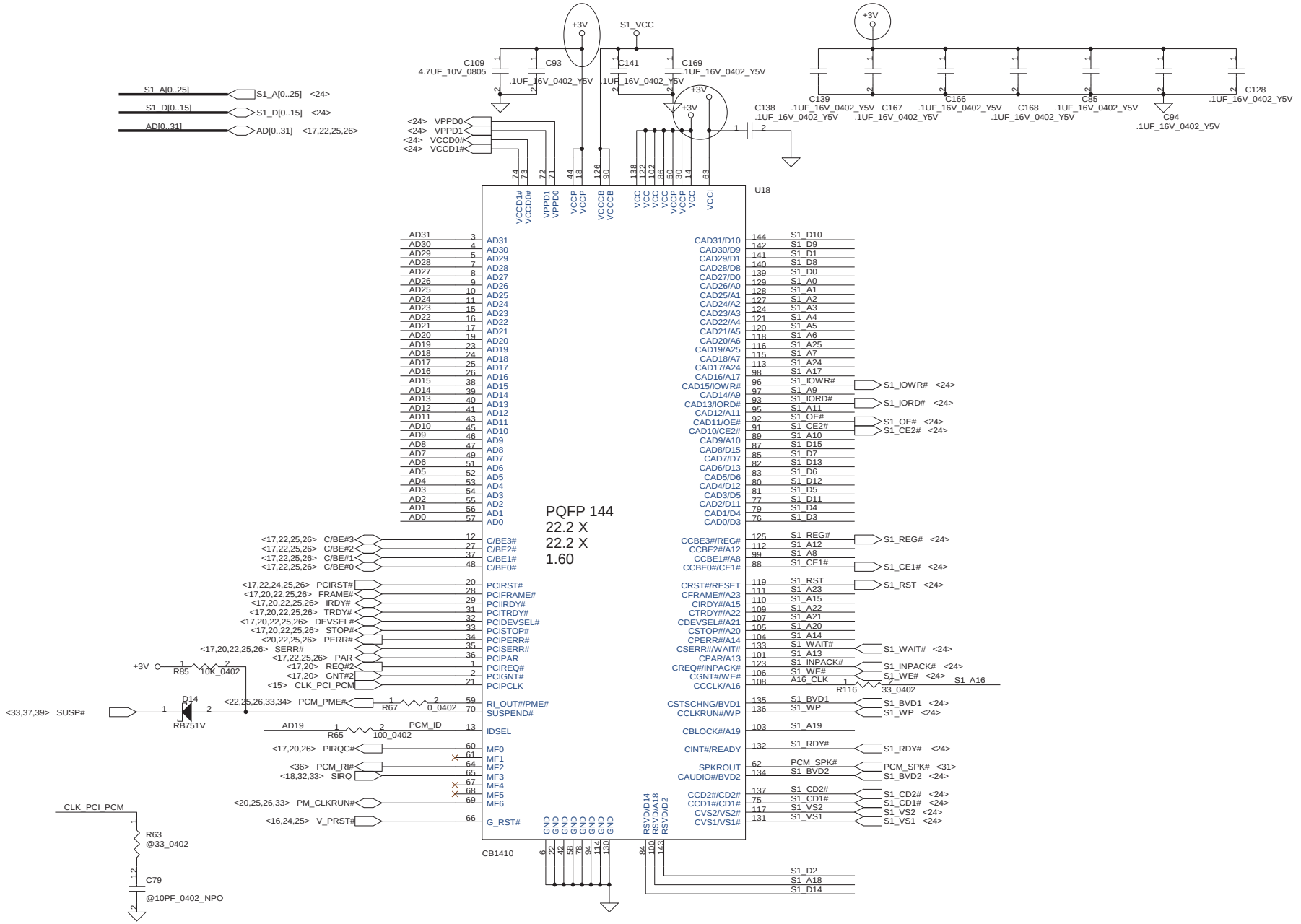
Size | Document Number: **ACT10** | Rev: 1.0A

Date: Thursday, May 30, 2002 | Sheet 21 of 45



Compal Electronics, Inc.

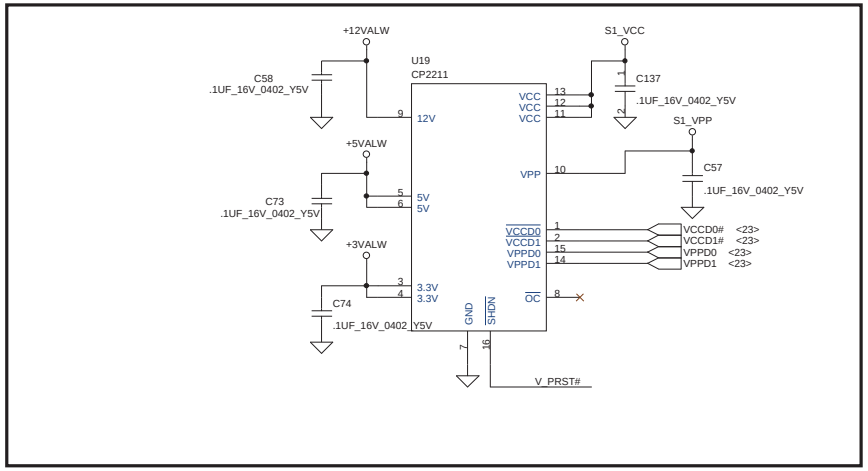
Title	Realtek RTL8100BL	
Size	Document Number: ACT10	Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 22 of 45	

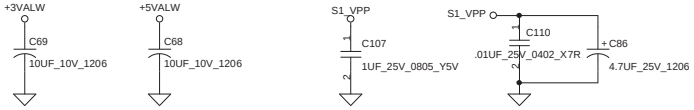


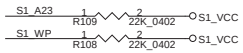
Compal Electronics, Ltd.

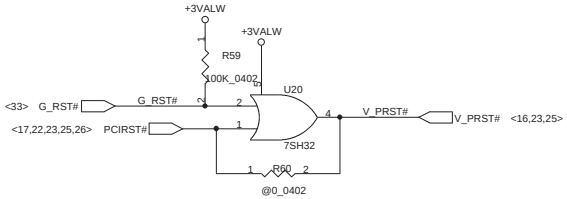
Title	PCMCIA controller ENE CB1410	
Size	Document Number ACT10	Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 23 of 45	

PCMCIA Power Controller

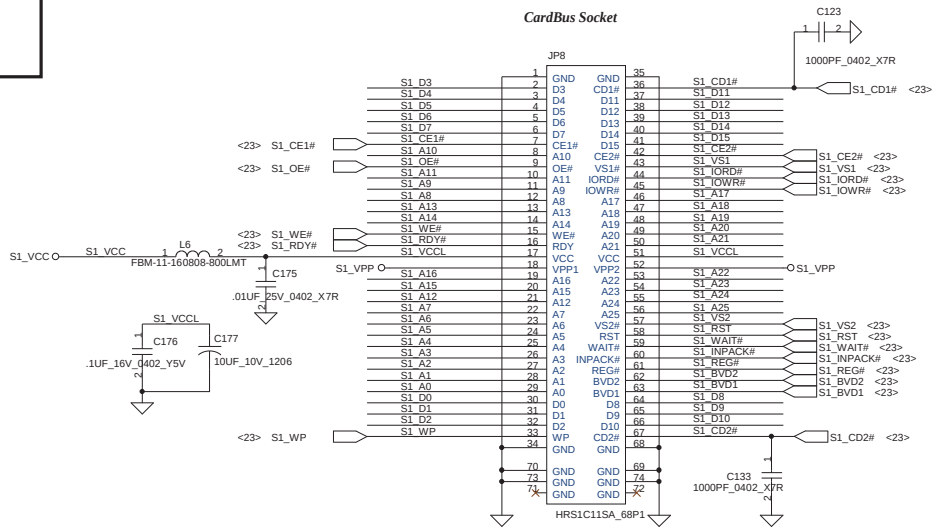








CardBus Socket

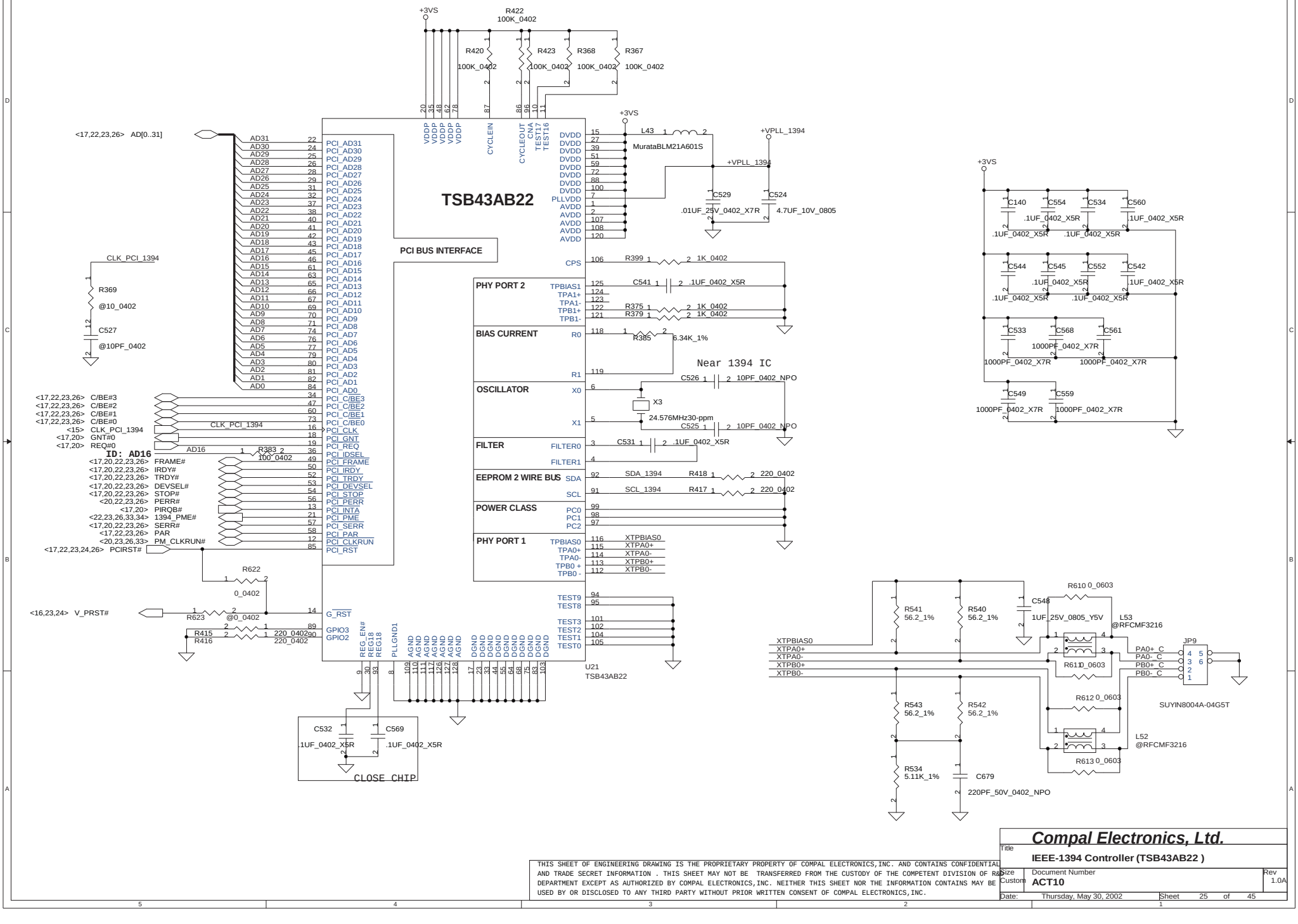


Compal Electronics, Inc.

Title: **CardBus Socket**

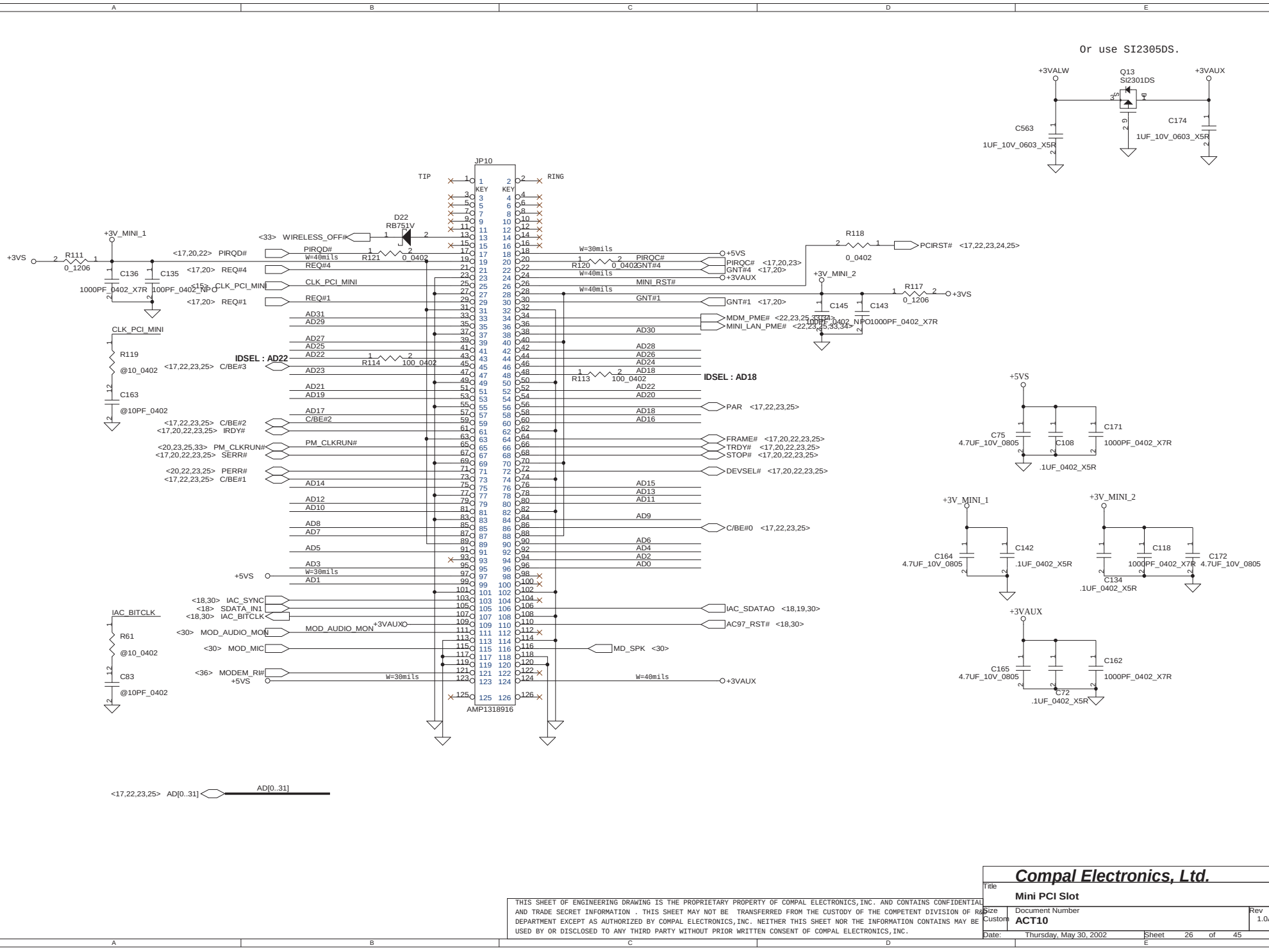
Size | Document Number: **ACT10** | Rev: 1.0A

Date: Thursday, May 30, 2002 | Sheet 24 of 45



Compal Electronics, Ltd.

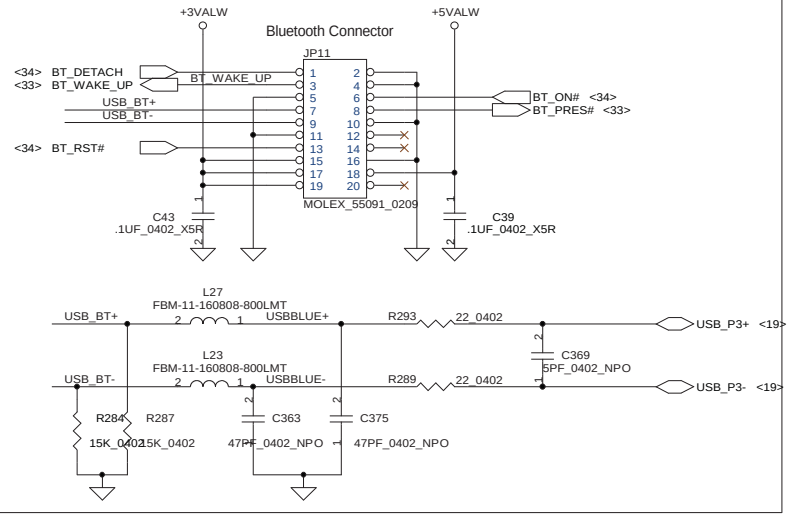
Title	IEEE-1394 Controller (TSB43AB22)	
Size: Custom	Document Number: ACT10	Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 25 of 45	

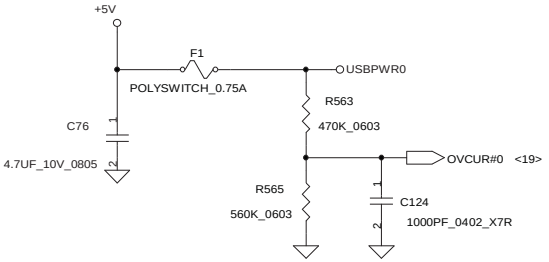


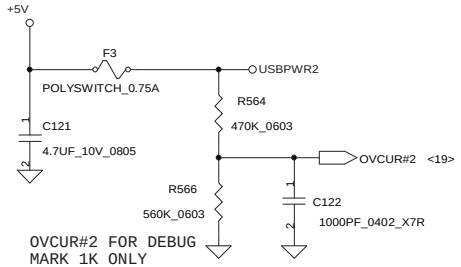
Compal Electronics, Ltd.

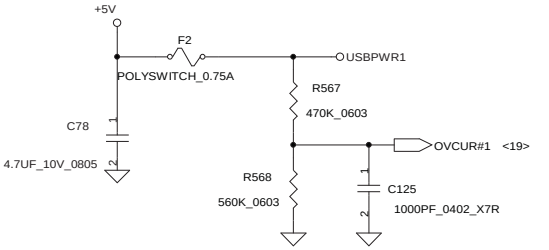
Title	Mini PCI Slot	
Size: Custom	Document Number: ACT10	Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 26 of 45	

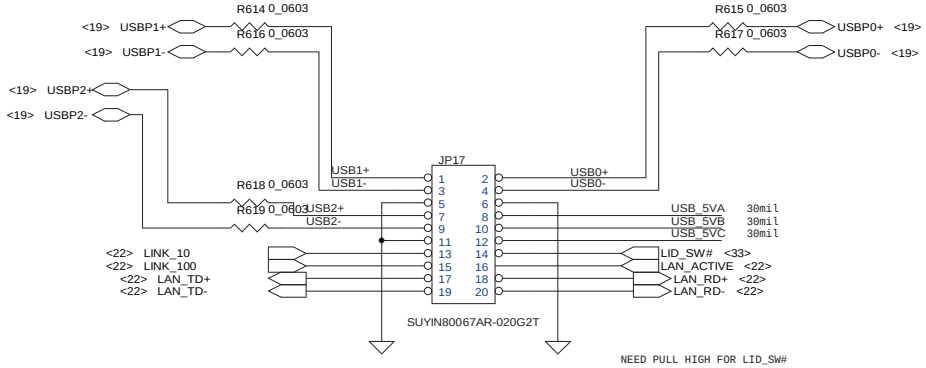
BlueTooth Interface

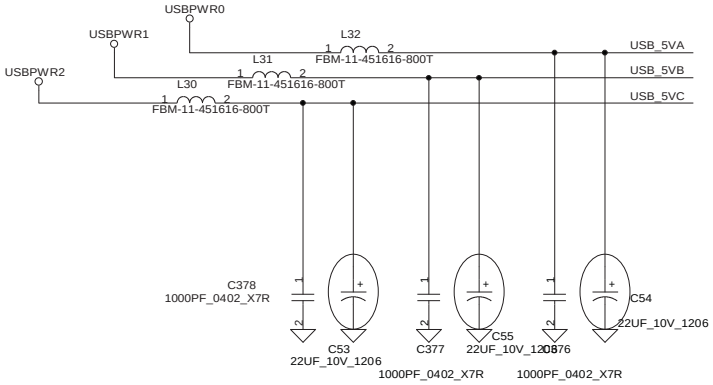






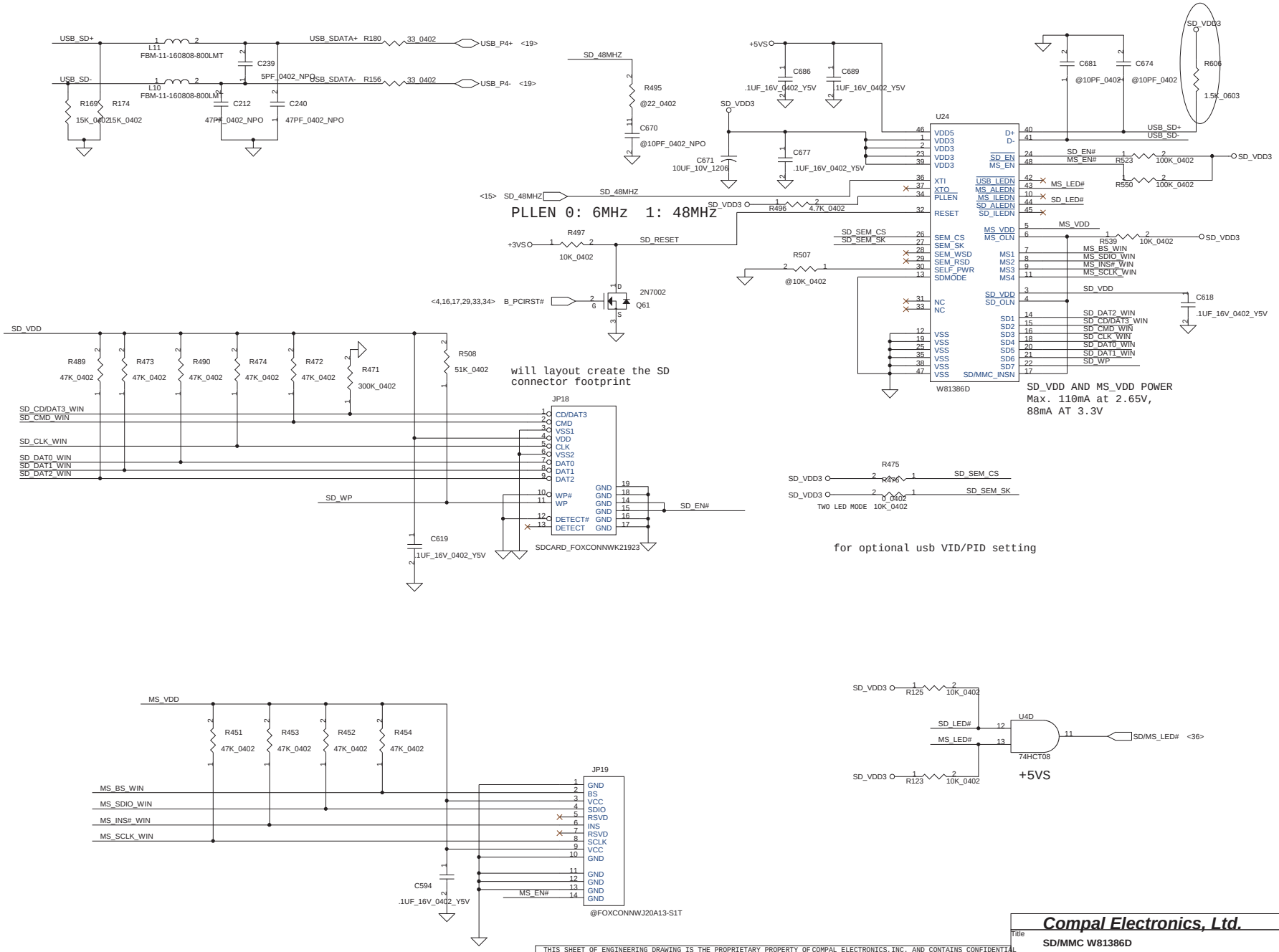






Compal Electronics, Ltd.

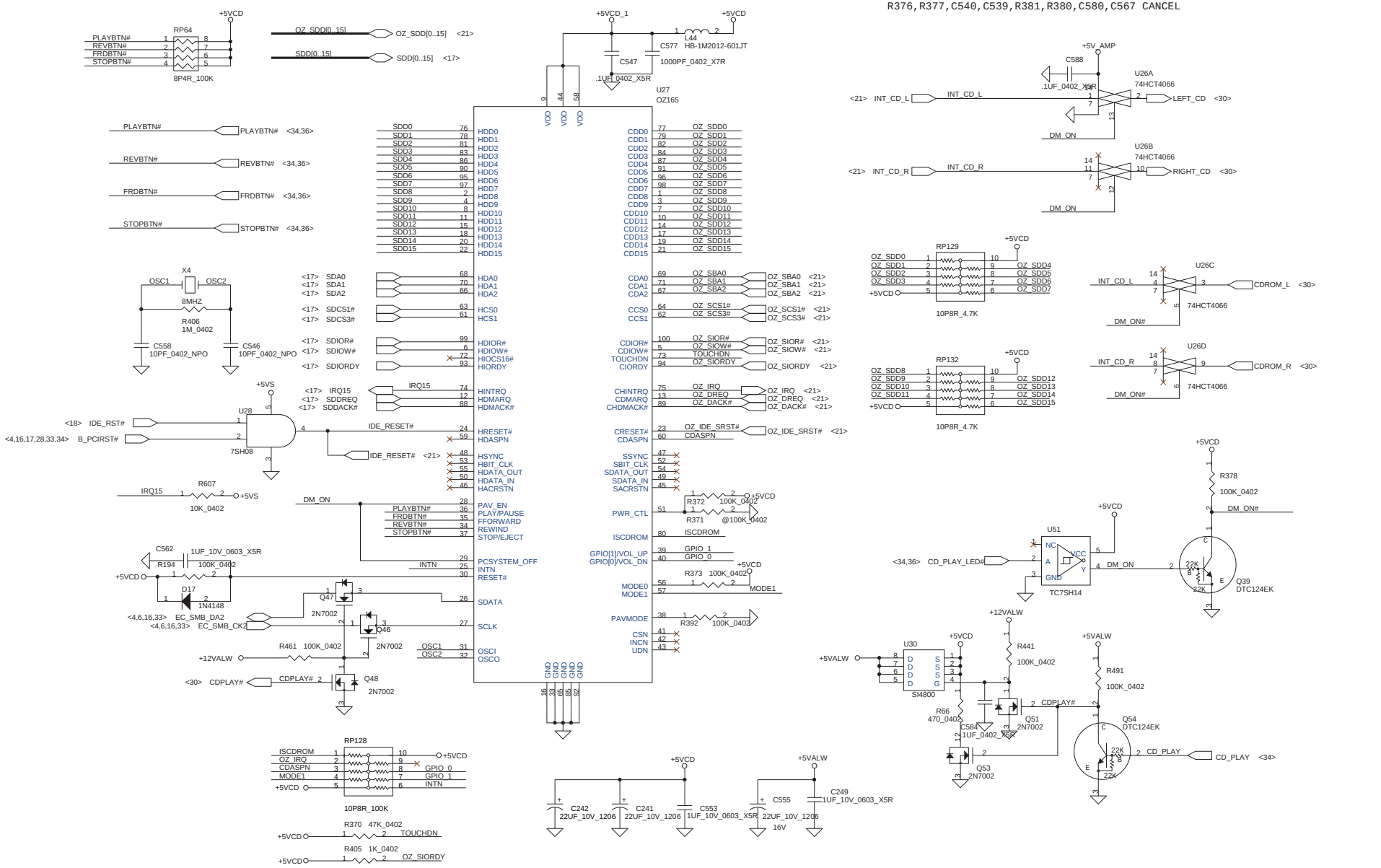
Title	USB & BlueTooth Connector	
Size: Custom	Document Number: ACT10	Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 27 of 45	



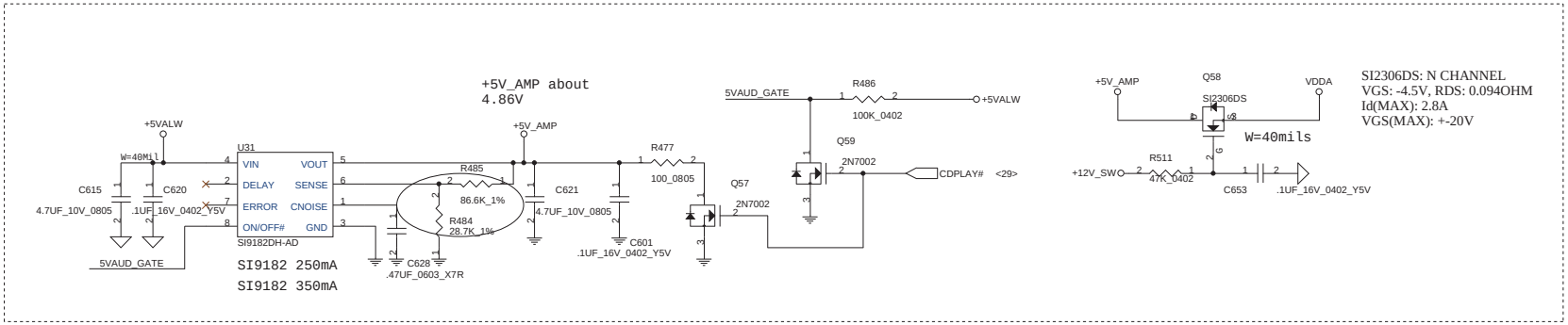
Compal Electronics, Ltd.

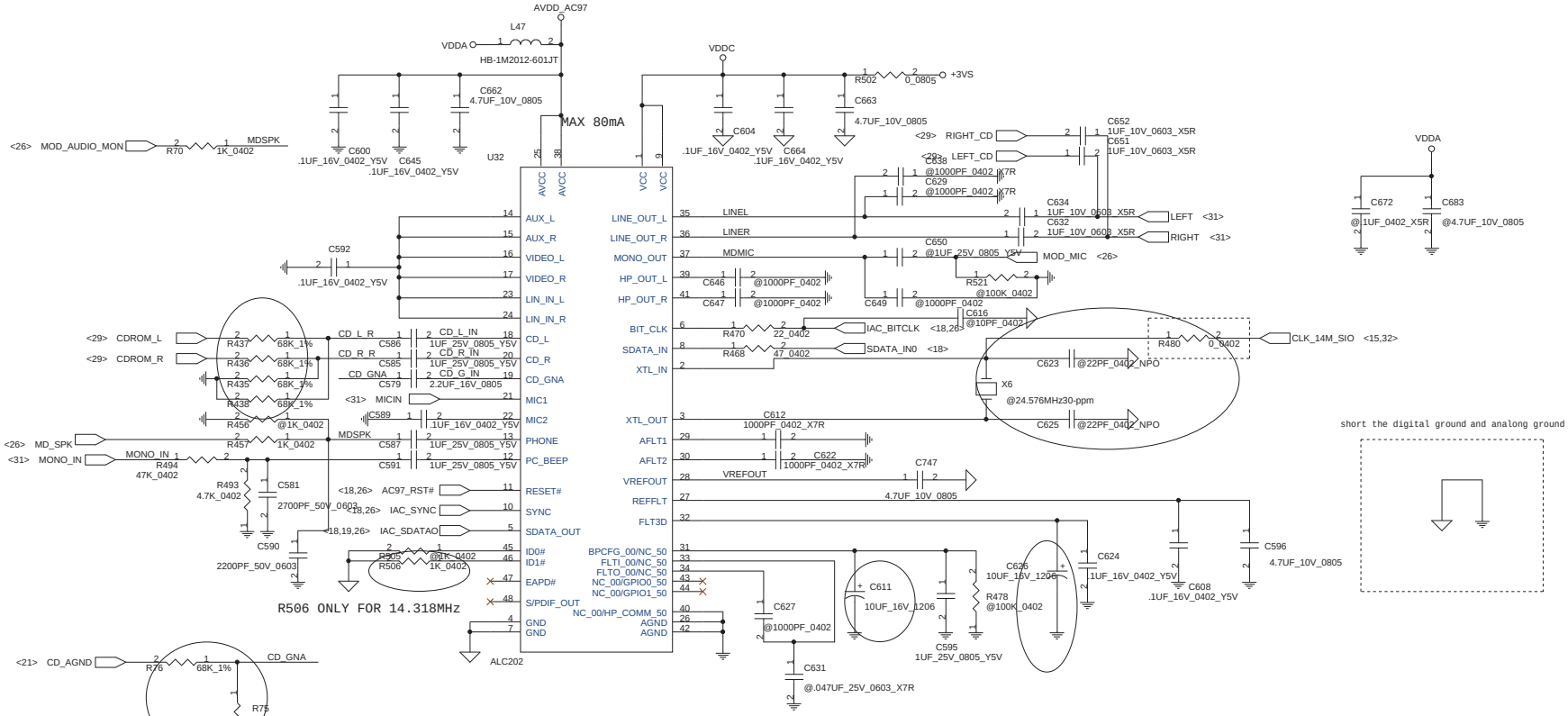
Title	SD/MMC W81386D	
Size: Custom	Document Number: ACT10	Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 28 of 45	

R376,R377,C540,C539,R381,R380,C580,C567 CANCEL



Compal Electronics, Ltd.	
Title	Direct CD Play OZ165
Size: Custom	Document Number: ACT10
Rev	1.0A
Date: Thursday, May 30, 2002	Sheet 29 of 45

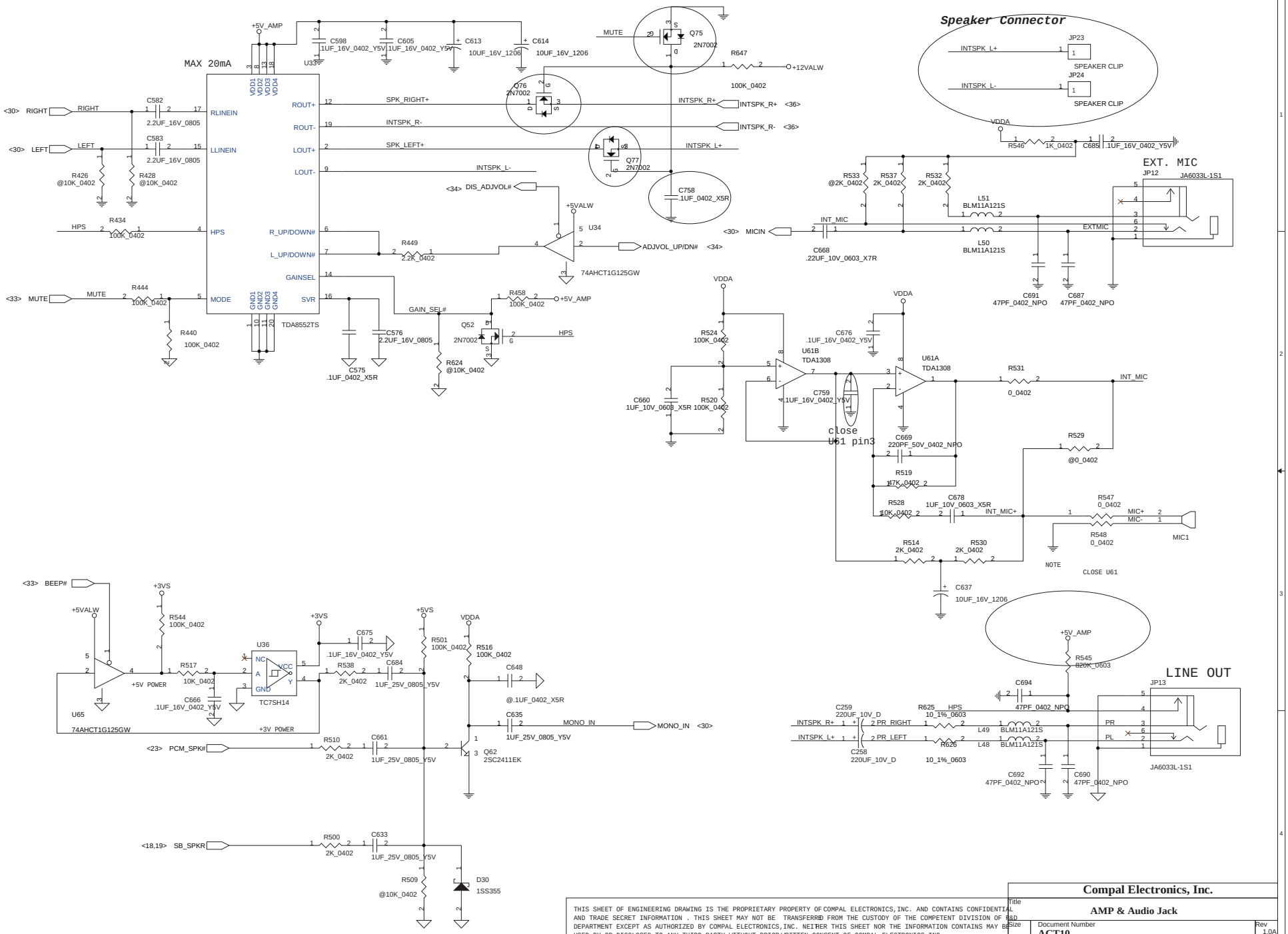




ID0#	ID1#	
1	1	14.318 OPEN
1	0	27MHZ
0	1	48MHZ
0	0	24.576MHZ

Compal Electronics, Inc.

Title	AC97 CODEC	
Size	Document Number ACT10	Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 30 of 45	



THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION . THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title	**AMP & Audio Jack**	
Size	Document Number **ACT10**	Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 31 of 45	

Fiduial Mark

FD1 FIDUCIALMARK
FD3 FIDUCIALMARK
FD2 FIDUCIALMARK
FD4 FIDUCIALMARK
FD6 FIDUCIALMARK
FD5 FIDUCIALMARK

Screw Hole

H20 O188X72D148X32
H21 O188X72D148X32
H26 O188X72D148X32
H27 O188X72D148X32

For HDD Case

H1 S354D118
H2 S354D118
H8 S354D118
H12 S354D118
H17 S354D118
H31 S354D118

H5 S315D118
H4 S315D118
H22 S315D118
H23 S315D118
H14 S315D118
H29 S315D118
H13 S315D118
H25 S315D118

H11 S315D173
H7 S315D173
H9 S315D173
H6 S315D173

4.4 Skew

H24 S354D173
H16 S276D142X173
H19 S335D118
H28 S354D122

CF2 SMDC40M80
CF4 SMDC40M80
CF5 SMDC40M80
CF6 SMDC40M80
CF9 SMDC40M80
CF12 SMDC40M80
CF13 SMDC40M80
CF17 SMDC40M80
CF10 SMDC40M80
CF14 SMDC40M80
CF11 SMDC40M80
CF15 SMDC40M80
CF1 SMDC40M80
CF3 SMDC40M80
CF7 SMDC40M80
CF8 SMDC40M80
CF18 SMDC40M80
CF16 SMDC40M80
CF20 SMDC40M80
CF19 SMDC40M80

H30 S217X146D197X126
H10 S217X146D197X126
H3 S354D169

+3VALW
R388 2.15K_1%_0603
TEMP_650 <33>
R389 0_0402
R40 Thermistor_0805_10K
SL210020F00

The temperature sensing for SIS650

CLK_PCI_SIO
R157 @10_0402
C218 @10PF_0402
CLK_14M_SIO
R158 @10_0402
C217 @10PF_0402
+3VS
R633 10K_0402
R634 10K_0402

U70 PC87391

<18,33> LAD0
<18,33> LAD1
<18,33> LAD2
<18,33> LAD3
<15> CLK_PCI_SIO
<34> LPC_RST#
<18,33> LFRAME#
<18> LDRQ#
IO_PD#
IO_CLKRUN#
<18,23,33> SIRQ
<15,30> CLK_14M_SIO

<21> DISKCHG#
<21> HDSEL#
<21> RDATA#
<21> WRPRT#
<21> TRK0#
<21> WGATE#
<21> WDATA#
<21> STEP#
<21> DIR#
<21> DRV0#
<21> MTR0#
<21> INDEX#
<21> 1.6M_EN#

PC87391_TQFP_100P

+3VS
C752 10UF_10V_1206
C753
C190 .1UF_0402_X5R
.1UF_16V_0402_Y5V

PD0/INDEX# PD1/TRK0# PD2/WP# PD3/RDATA# PD4/DSKCHG# PD5/MSEN0 PD6/DRATE0 PD7/MSEN1
PNF/XRDY SLCT/WGATE# PE/WDATA# BUSY_WAIT#/MTR1# ACK#/DR1# SLIN#_ASTRB#/STEP# INIT#/DIR# ERR#/HDSEL# AFD#_DSTRB#/DENSEL STB#_WRITE#
DCD1# DSR1# SIN1 RTS1#/TEST SOUT1/XCNF0 CTS1# DTR1#_BOUT1/BADDR RI1#
IRTX IRRX1 IRRX2_IRSL0 IRSL1 IRSL3/PWUREQ#
NC/XCNF1 WDO# MTR1#/DRATE0 IRSL2/DR1# DR1#

R635 100K_0402
IRTXOUT <36>
IRRX <36>
IRMODE <36>
XCNF1

RP135 1K_1206_10P8R
WDATA# WGATE# HDSEL# DIR# +5VS
STEP# MTR0# DRV0# RDATA# +5VS
XCNF2

RP136 8P4R_1K
DISKCHG# INDEX# WRPRT# TRK0# +5VS

+3VS R636 100K_0402
RP137 8P4R_100K

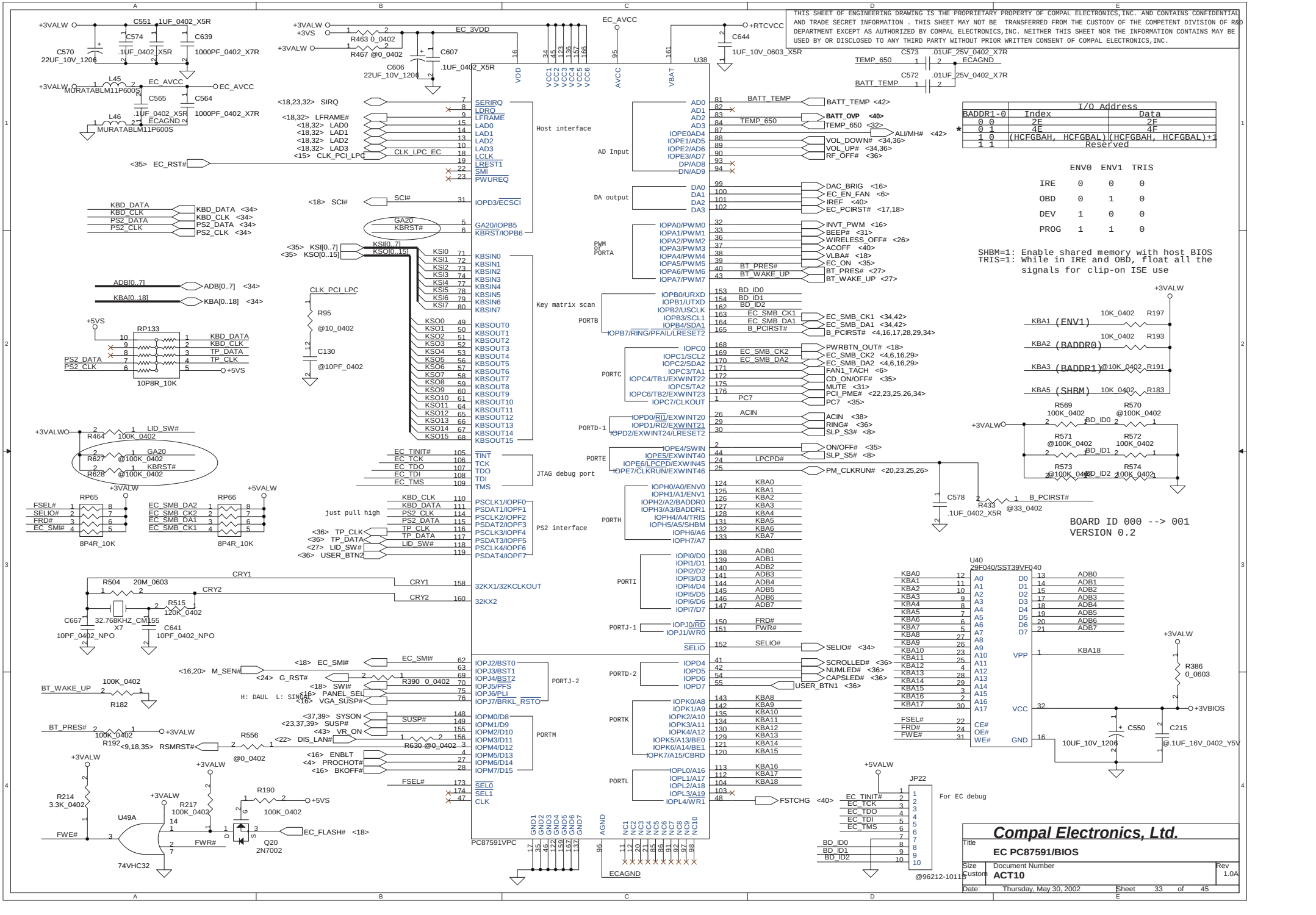
JP26 ACES 87153-2601
LPD0 LPD1 LPD2 LPD3 LPD4 LPD5 LPD6 LPD7 +5VS
LPTSLCT LPTPE LPTBUSY LPTACK# LPTSLCTIN# LPTINIT# LPTERR# LPTAFD# LPTSTB# DCDA# DSRA# RXDA# RTSA#
TXDA CTSA# DTRA# RIA#

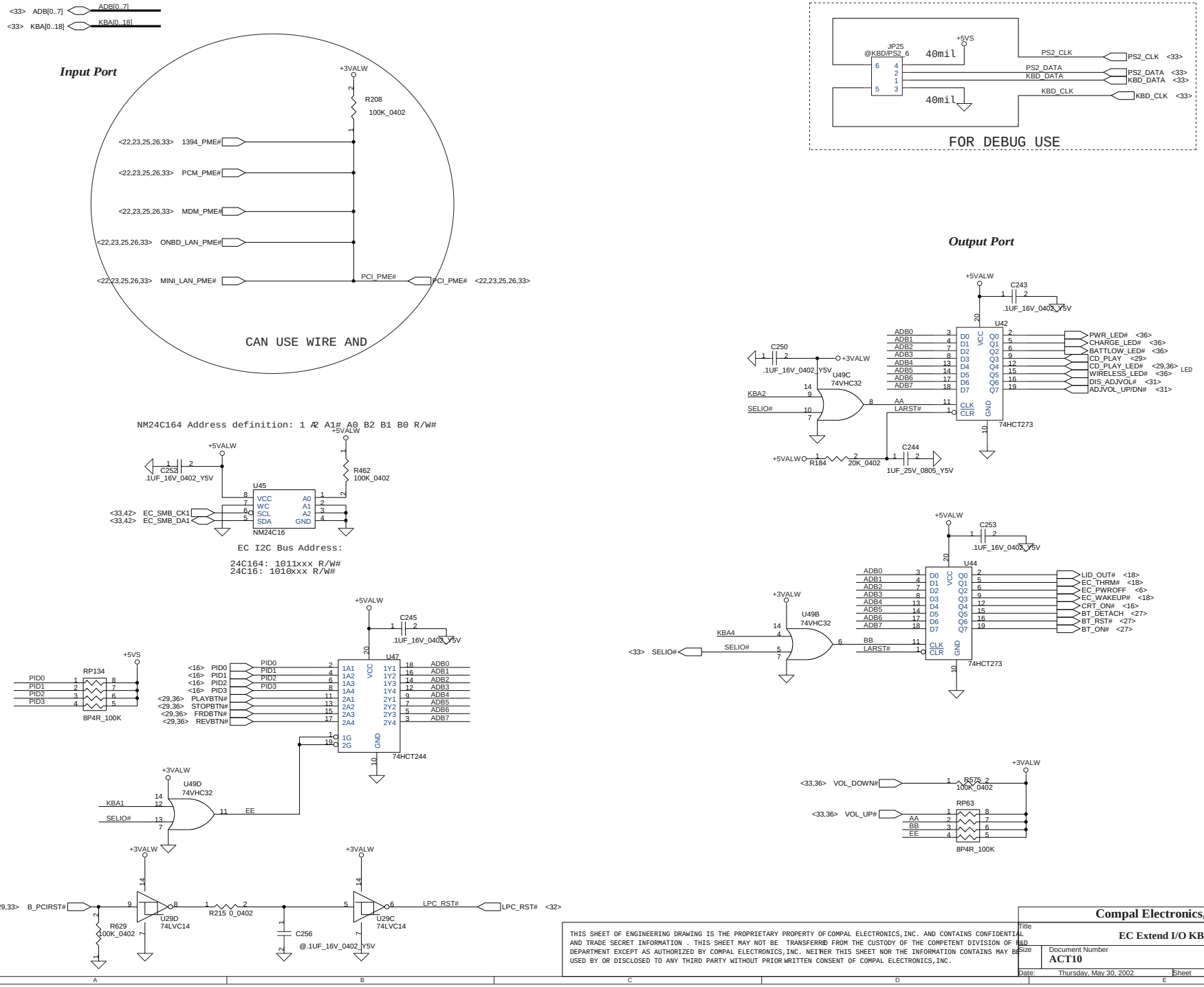
+5VS C189 .1UF_0402_X5R
+5VS C191 .1UF_0402_X5R

R637 TXDA @10K_0402
R639 XCNF1 @10K_0402
R641 XCNF2 @10K_0402
R643 DTRA# @10K_0402
R638 TXDA @10K_0402
R640 XCNF1 @10K_0402
R642 XCNF2 @10K_0402
R644 DTRA# @10K_0402

Signal	Pin #	Description
BADDR: DTRA#	61	BASE Address Selection "0": 2E~2F (Default) "1": 4E~4F

Compal Electronics, Inc.
Title: Skew Hole/SUPER IO
Size: Document Number: ACT10
Rev: 1.0A
Date: Thursday, May 30, 2002
Sheet 32 of 45

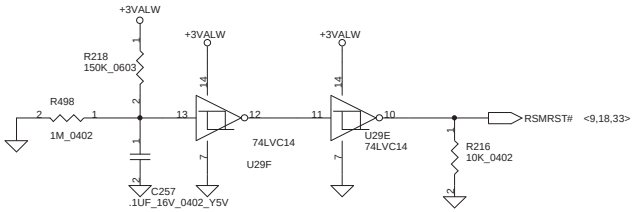

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS,INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION . THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS,INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS,INC.
U38
PC87591VPC
Host interface
Key matrix scan
JTAG debug port
PS2 interface
AD Input
DA output
PWM OR PORTA
PORTB
PORTC
PORTD-1
PORTE
PORTH
PORTI
PORTJ-1
PORTD-2
PORTJ-2
PORTK
PORTM
PORTL
I/O Address
BADDR1-0 Index Data
0 0 2E 2F
0 1 4E 4F
1 0 (HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1
1 1 Reserved
ENV0 ENV1 TRIS
IRE 0 0 0
OBD 0 1 0
DEV 1 0 0
PROG 1 1 0
SHBM=1: Enable shared memory with host BIOS
TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use
BOARD ID 000 --> 001
VERSION 0.2
U40
29F040/SST39VF040
JP22
For EC debug
Compal Electronics, Ltd.
EC PC87591/BIOS
Size Custom
Document Number ACT10
Rev 1.0A
Date: Thursday, May 30, 2002
Sheet 33 of 45

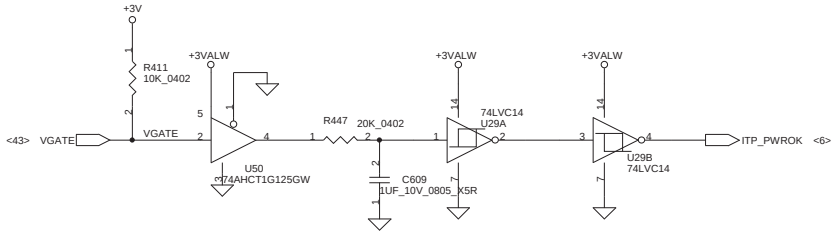


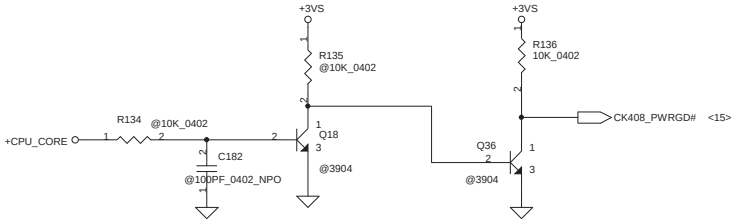
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION . THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.	
Title	EC Extend I/O KB Conn. & BIOS
Size	Document Number: ACT10 — Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 34 of 45

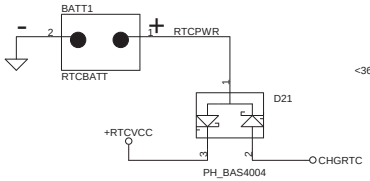
Power ON Circuit



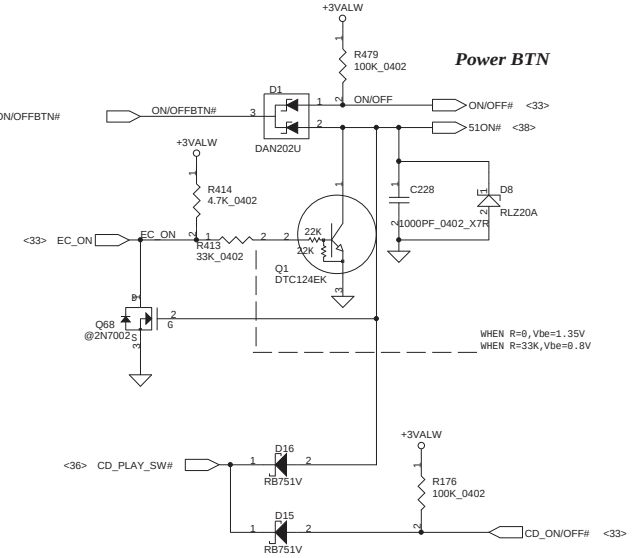


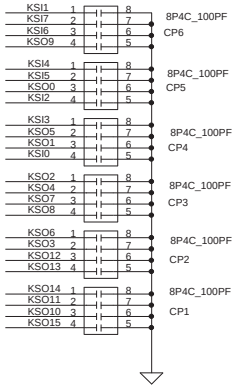


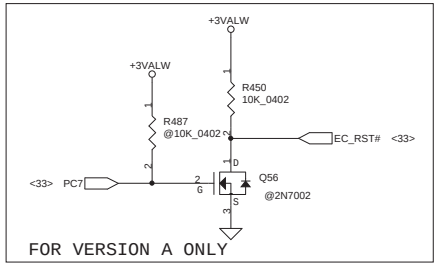
RTC Battery

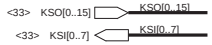


Power BTN

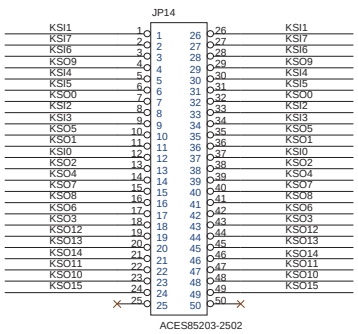








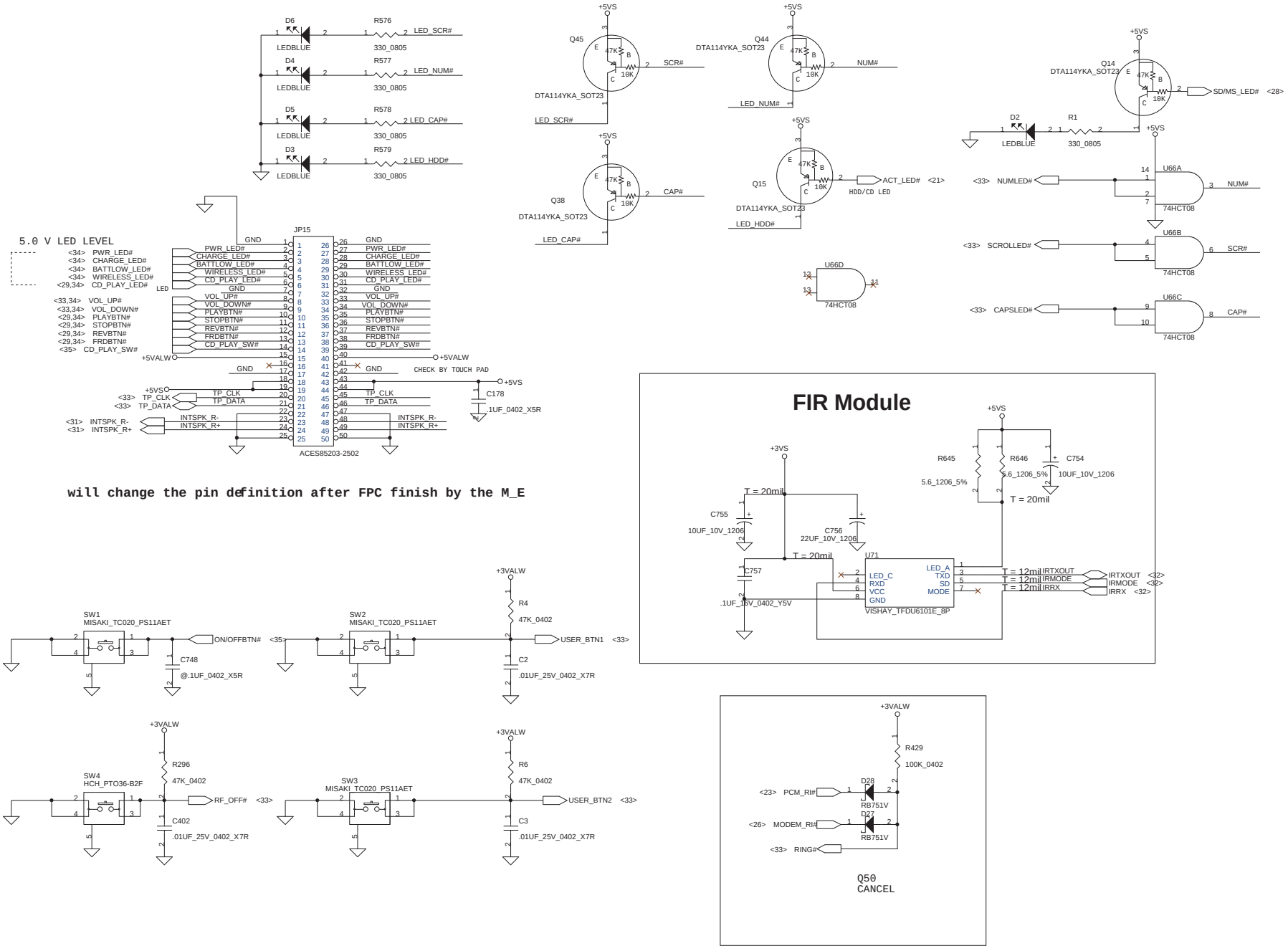
INT_KBD CONN.



THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION . THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

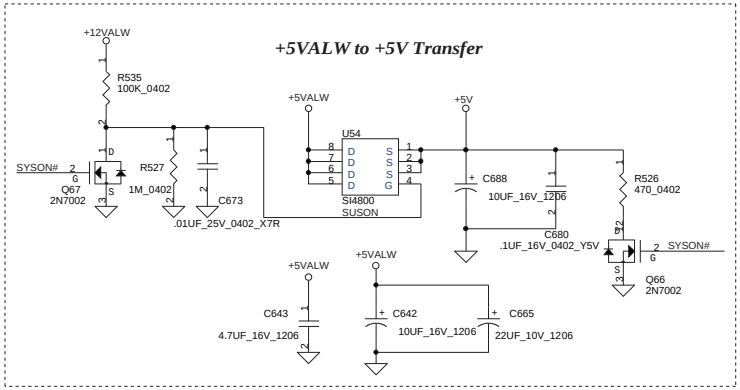
Compal Electronics, Inc.

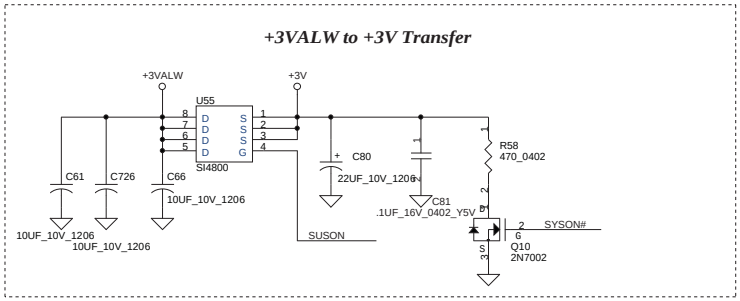
Title	Power OK/Reset/RTC battery/Lid Switch/Int. KB	
Size	Document Number: ACT10	Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 35 of 45	

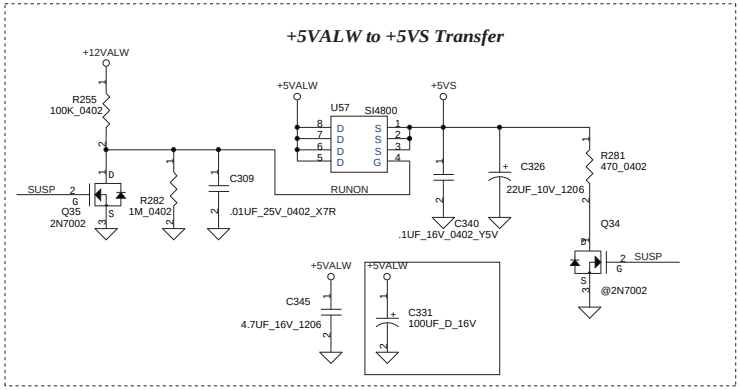


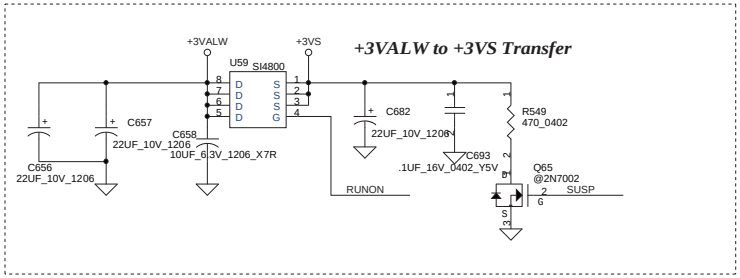
Compal Electronics, Ltd.

Title	SW/LED/RI#/IR/CD BUTTOM	
Size: Custom	Document Number: ACT10	Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 36 of 45	

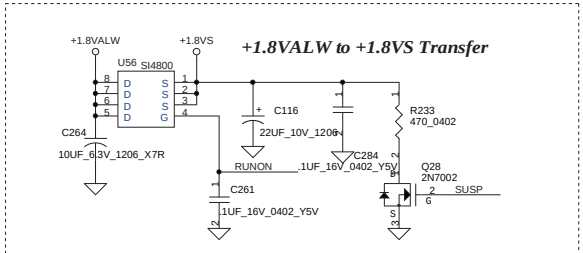


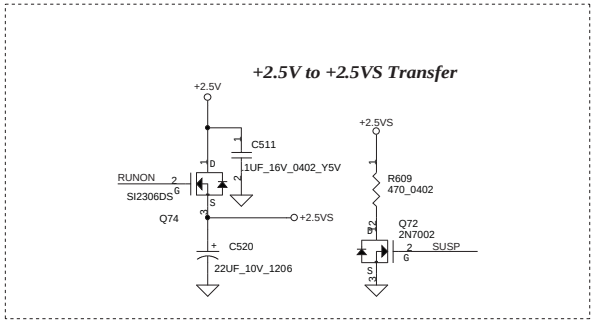


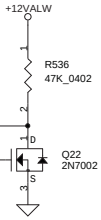


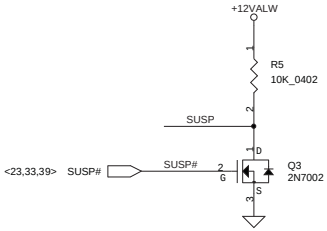


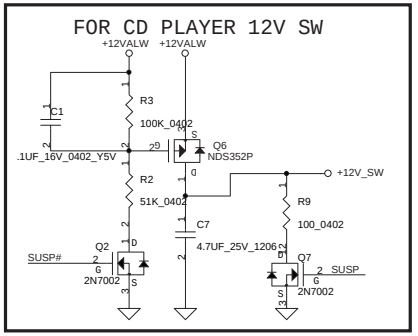
1.8VALW/+1.5VS Power direct provide







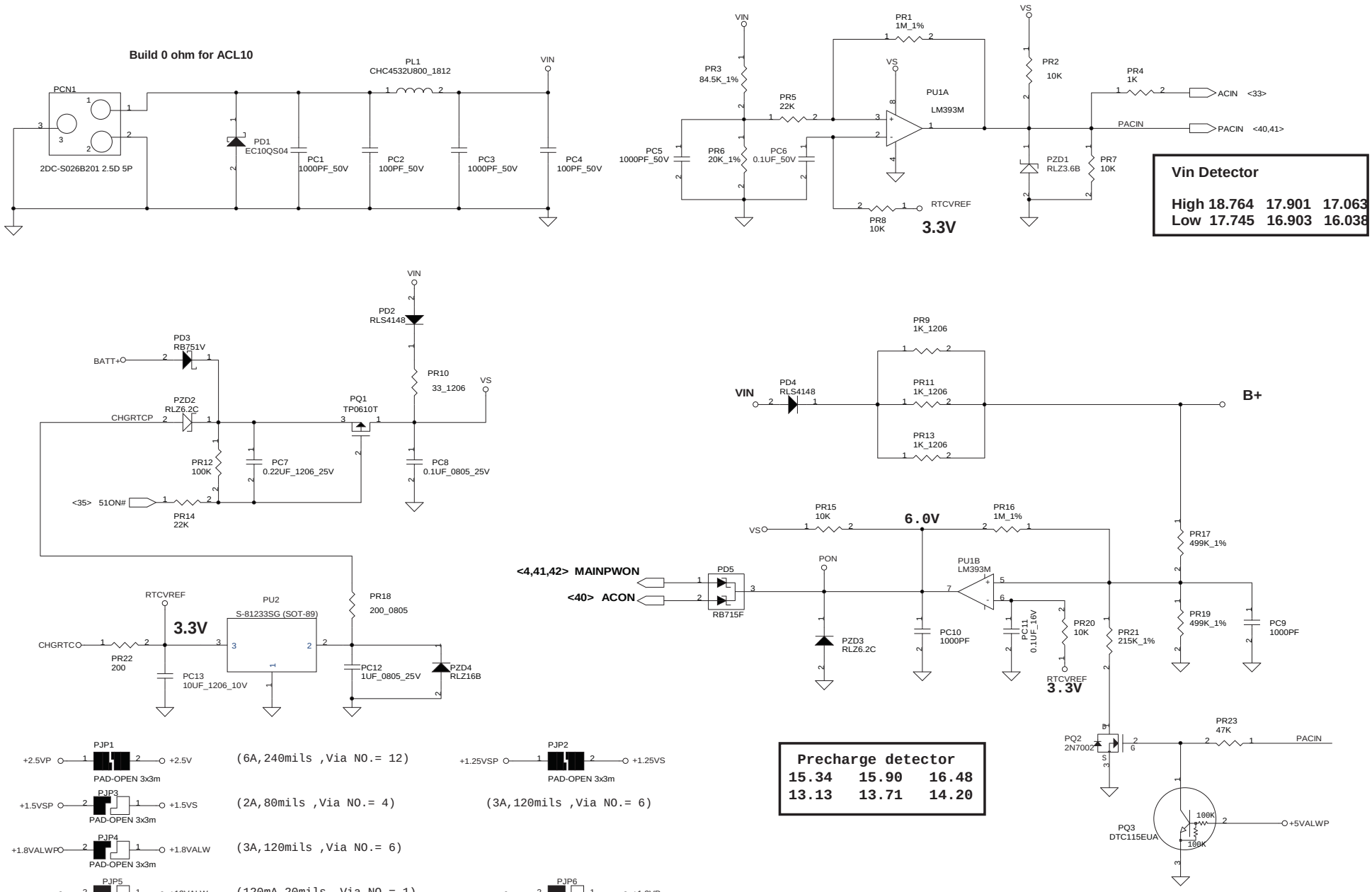




THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS,INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION . THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS,INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS,INC.

Compal Electronics, Inc.

Title	DC/DC Circuit Interface	
Size	Document Number ACT10	Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 37 of 45	

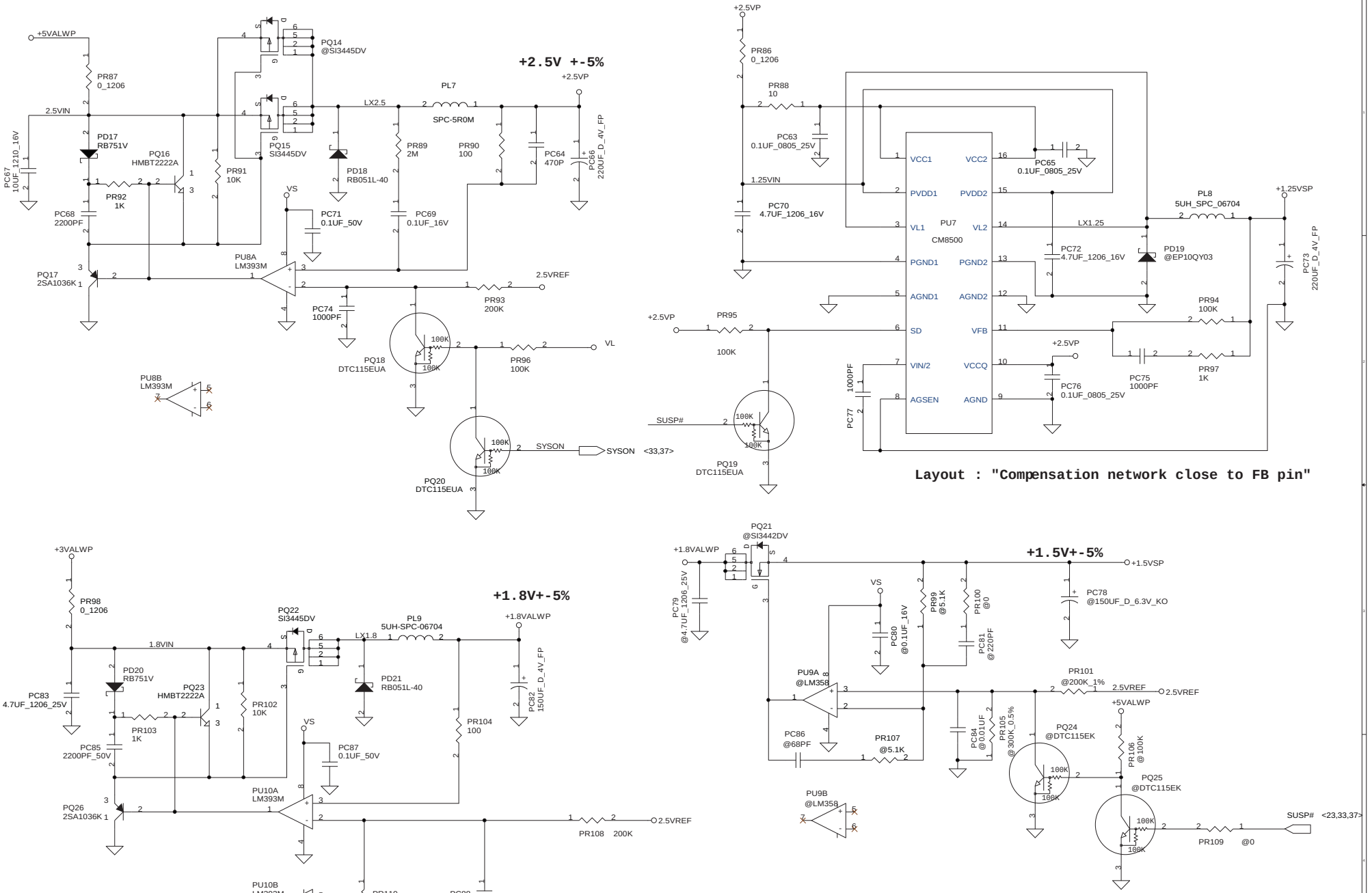


COMPAL ELECTRONICS, INC

Title: DCIN & DETECTOR

Size: B | Document Number: ACT10 | Rev: 1.0A

Date: Thursday, May 30, 2002 | Sheet 38 of 45

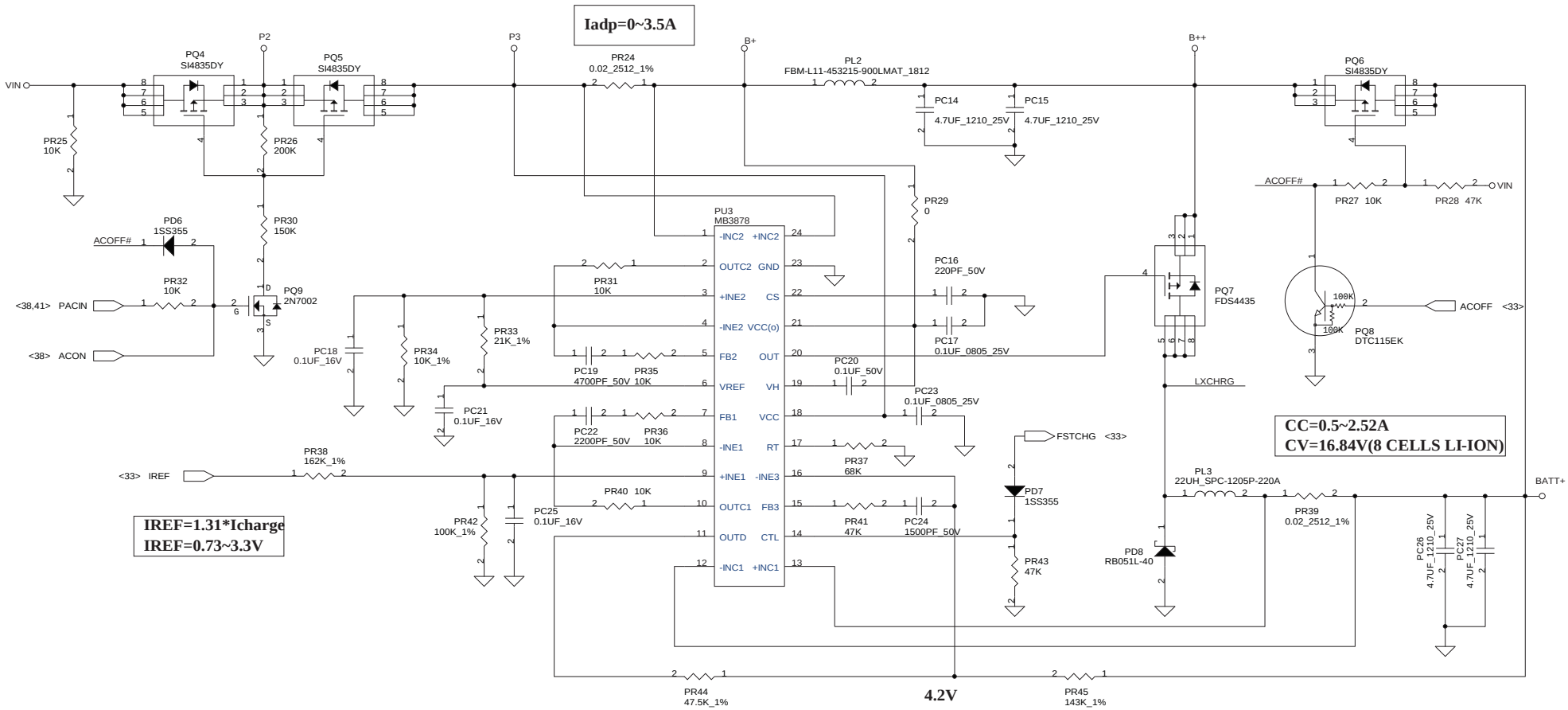


COMPAL ELECTRONICS, INC

Title: **DDR /2.5V / 1.8V/1.25V**

Size	Document Number	Rev
B	ACT10	1.0A

Date: Thursday, May 30, 2002 Sheet 39 of 45

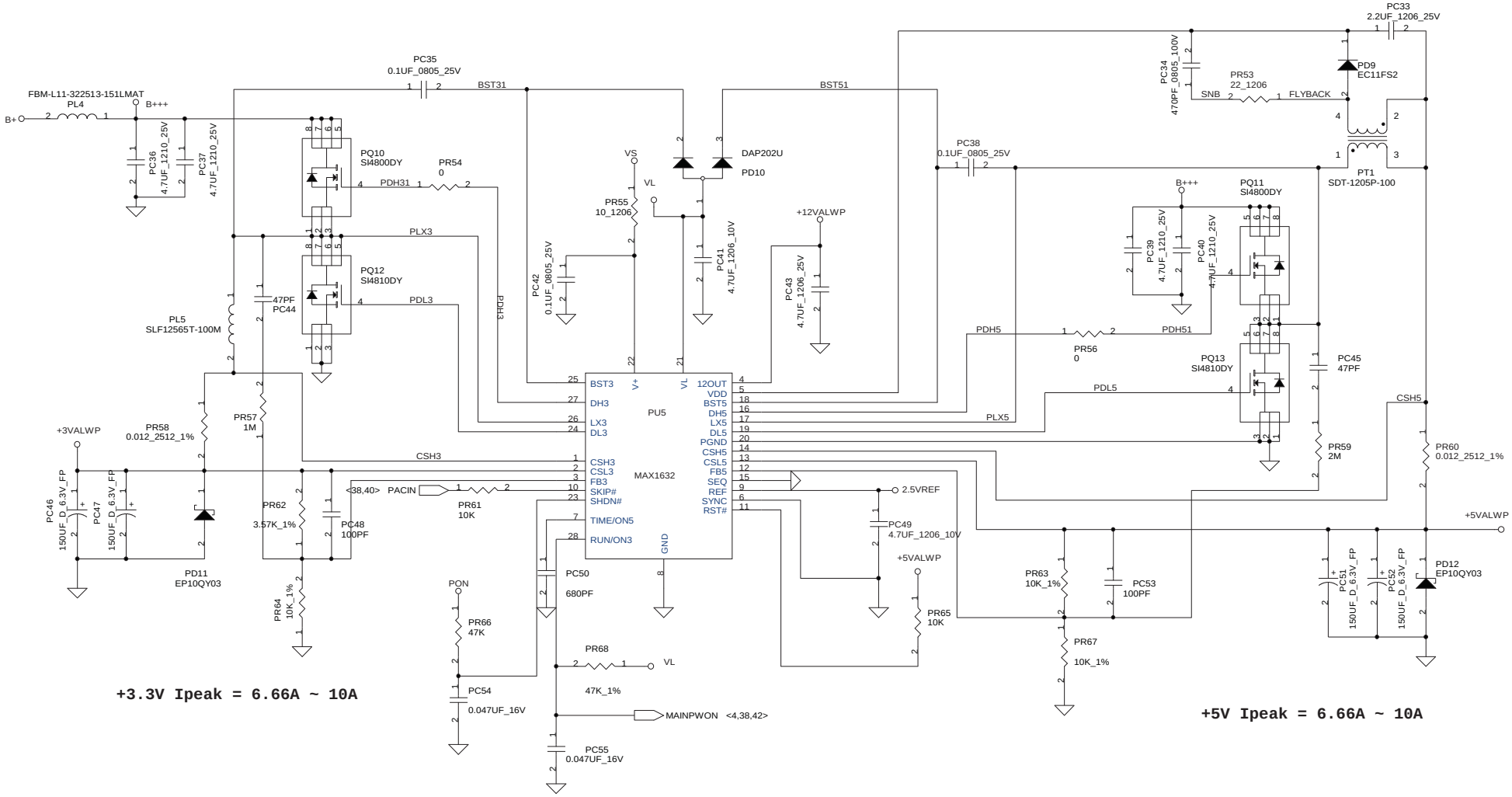


COMPAL ELECTRONICS, INC

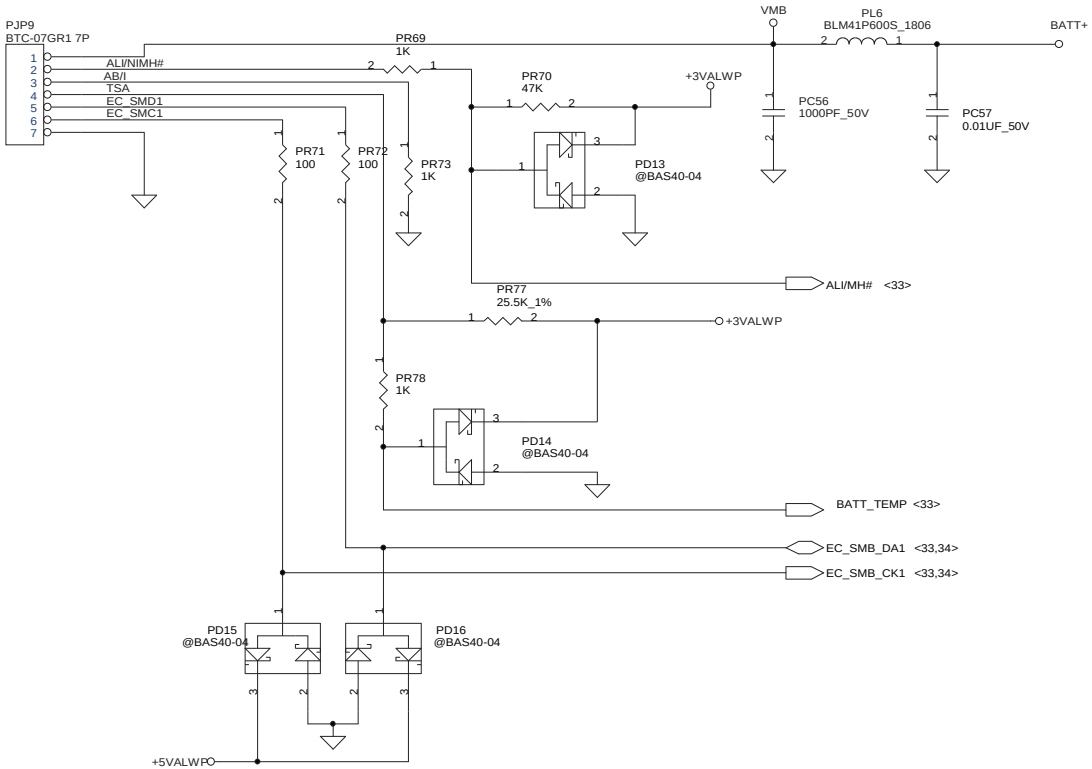
Title: CHARGER

Size: B | Document Number: ACT10 | Rev: 1.0A

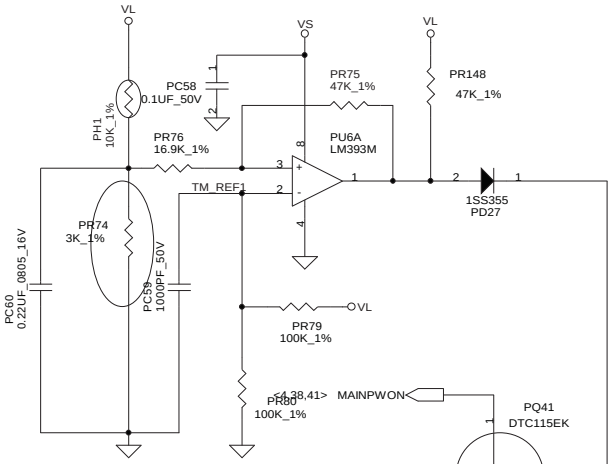
Date: Thursday, May 30, 2002 | Sheet 40 of 45



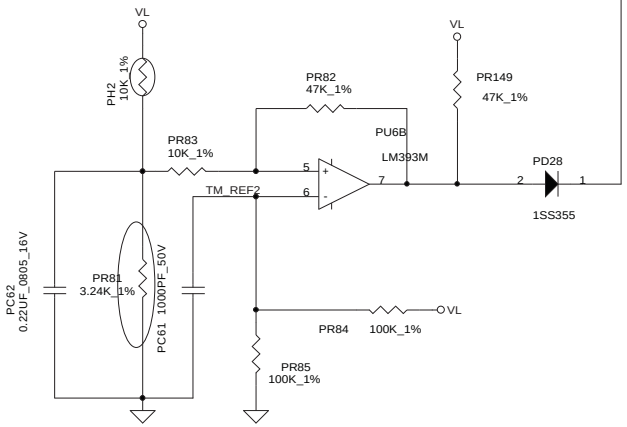
COMPAL ELECTRONICS, INC	
Title	5V/3.3V/12V
Size: B	Document Number: ACT10
Rev	1.0A
Date: Thursday, May 30, 2002	Sheet 41 of 45



PH1 under CPU botten side :
CPU thermal protection at 87 degree C
Recovery at 48 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 73 degree C
Recovery at 50(51) degree C

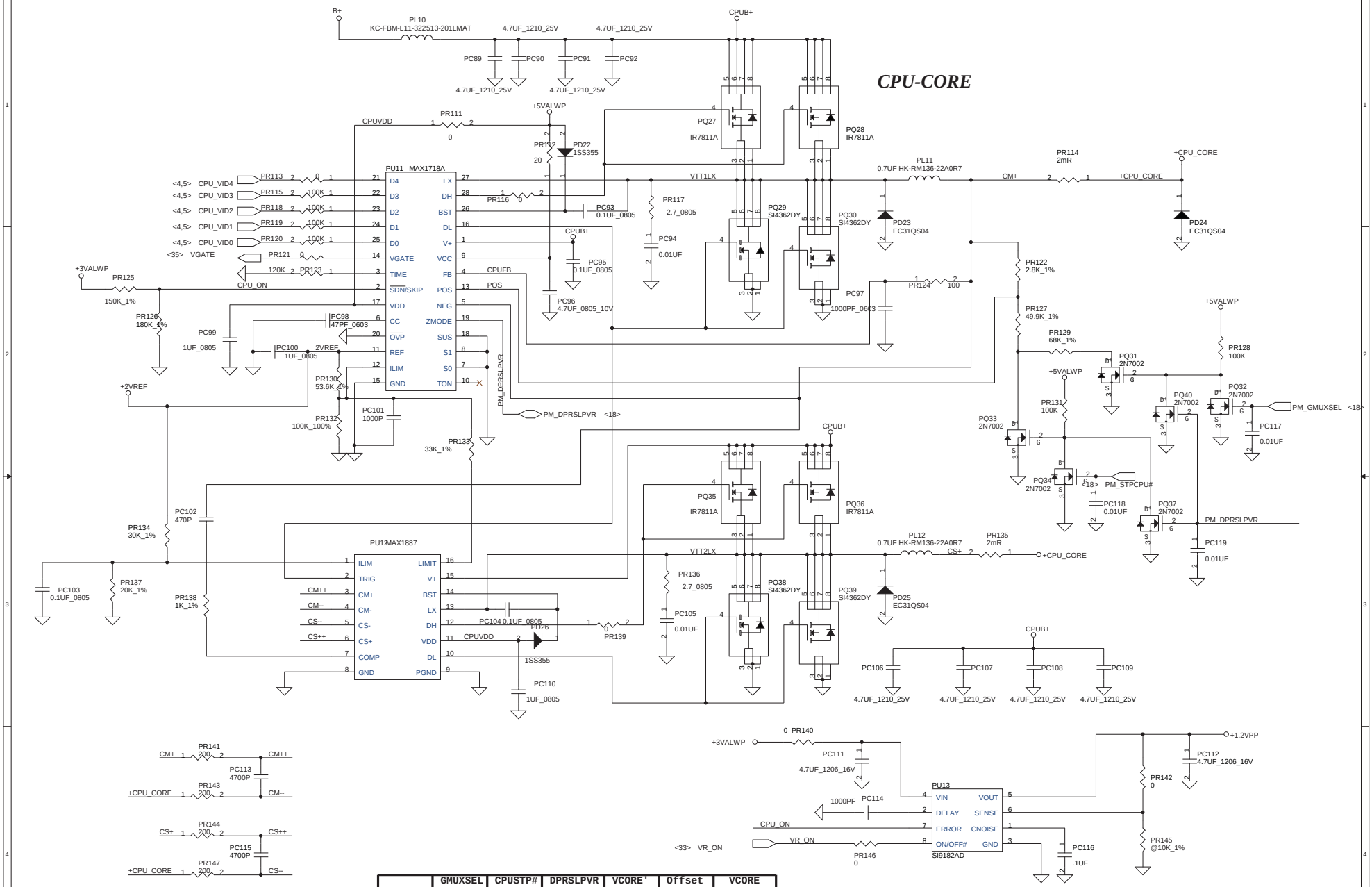


COMPAL ELECTRONICS, INC

Title: **BATTERY CONN / OTP**

Size	Document Number	Rev
B	ACT10	1.0A

Date: Thursday, May 30, 2002 Sheet 42 of 45



	GMUXSEL	CPUSTP#	DPRSLPVR	VCORE'	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0		4.62%	1.239V
BM	0	1	0	1.20V	2.0%	1.176V
BM D-S	0	0	0		4.62%	1.144V
Deeper	X	0	1	1.0V	0%	1.0V

COMPAL ELECTRONICS, INC

Title: +VCC_H_CORE

Size: B | Document Number: ACT10 | Rev: 1.0A

Date: Thursday, May 30, 2002 | Sheet 43 of 45

AGP Multiplexed Channel B List **Power Managment table**

AGP D0 : VBD7
AGP D1 : VBD6
AGP D2 : VBD5
AGP D3 : VBD4
AGP D4 : VBD3
AGP D5 : VBD2
AGP D6 : VBD1
AGP D7 : VBD0
AGP D19 : VBD11
AGP D20 : VBD10
AGP D21 : VBD8
AGP D22 : VBD9
AGP D27 : VBDE
AGP D28 : VBCTL0
AGP D29 : VBCTL1
AGP D30 : VBHSYNC
AGP D31 : VBVSYNC
AGP AREQ# : VBCD
AGP RBF# : VBHCLK
AGP SBA0 : VBCLK
AGP STB1 : VBGCLK
AGP STB1# : VBGCLK#

AGP D24 : VAD0
AGP D23 : VAD1
AGP D25 : VAD2
AGP D26 : VAD3
AGP D10 : VAD4
AGP D9 : VAD5
AGP D8 : VAD6
AGP D11 : VAD7
AGP D12 : VAD8
AGP D13 : VAD9
AGP D14 : VAD10
AGP D15 : VAD11
AGP D16 : VADE
AGP D18 : VAHSYNC
AGP D17 : VAVSYNC
AGP STB0 : VAGCLK
AGP STB0# : VAGCLK#

Signal / State	+3VALW +5VALW +1.8VALW +12VALW	+3V +5V +2.5V	+3VS +5VS +1.8VS +1.5VS +1.2VP +CPU_CORE +1.25VS
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

IDSEL :
1394 : AD16
LAN : AD17
CARDBUS : AD19
MINI_PCI : AD18, AD22

PCI MASTER :
1394 : REQ0#, GNT0#
MINI-PCI(Wireless Lan) : REQ1#, GNT1#
CARDBUS : REQ2#, GNT2#
LAN : REQ3#, GNT3#
MINI-PCI : REQ4#, GNT4#

PCI IRQ ROUTING :
VGA : INTA#
1394 : INTB#
CARDBUS/MINI-PCI : INTC#
LAN/MINI-PCI : INTD#

History List

Item	Description	Page	Note	Date
1	Layout Ver. 0.0		Power not Include	01/11/22
2	Layout Ver. 0.0 add power		Power Include	01/11/23
3	Add Part Number			01/12/25
4	Change some parts suggest from SiS		Add Jumpper	01/1/3

Compal Electronics, Inc.

Title: **Note & Revision**

Size | Document Number: **ACT10** | Rev: 1.0A

Date: Thursday, May 30, 2002 | Sheet 44 of 45

Title	<Title>
Size: Custom	Document Number: <Doc>
Rev	1.0A
Date: Thursday, May 30, 2002	Sheet 45 of 45