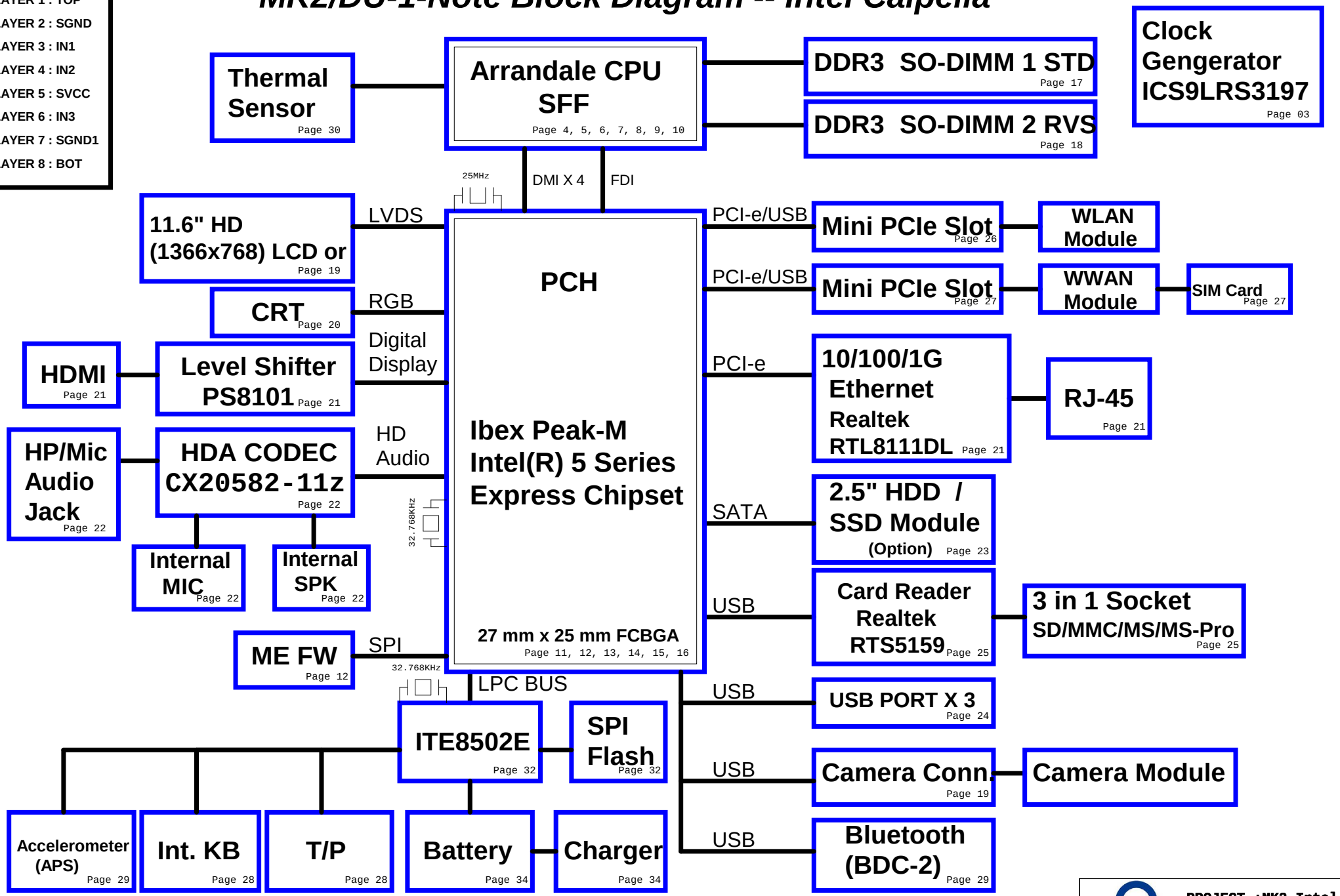
PCB STACK UP 8L

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : IN3
- LAYER 7 : SGND1
- LAYER 8 : BOT

MK2/DU-1-Note Block Diagram -- Intel Calpella



PROJECT :MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> BLOCK DIAGRAM	1C

Date: Wednesday, June 23, 2010 Sheet 1 of 42

INDEX

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	23,32,43,44,45,46,47,48,49,50	MAIN POWER		S0~S5
+3VRTC	+3.0V~+3.3V	9,12,41	RTC		S0~S5
3VPCU	+3.3V	9,23,27,30,32,35,39,41,43,44,47	ITE8052 POWER	3V5V_EN	S0~S5
5VPCU	+5V	14,43,44,45,46,47,49,50	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	23,38,43,45,46,47	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	27,43	LAN POWER	LAN_ON	
5V_S5	+5V	12,29,30,43	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	8,9,10,11,12,43,52	Sys Management,PCH Resume Well,Intel HD Audio,USB,WLAN WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V	23,39,43,48	SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V	14,15,30,34,41,43,49	SLP_S4# CTRLD POWER	SUSON	S0~S3
1.5VSUS	+1.5V	4,6,14,15,43,45,46,49,50	SODIMM POWER	SUSON	S0~S3
0.75VSMDDR_VTERM	+0.75V	14,15,43,45	DDR3 SODIMM REFERENCE POWER	MAIN_ON	S0
+5V	+5V	12,18,23,24,25,26,28,35,37,41,43,44	SLP_S3# CTRLD POWER	MAIN_ON	S0
+3V	+3.3V	3,4,8,9,10,11,12,14,15,17,23,25,26,27,28,29, 30,31,32,33,34,36,37,38,39,40,41,43,44,45,46 ,47,48,50,52	SLP_S3# CTRLD POWER	MAIN_ON	S0
+1.8V	+1.8V	6,12,17,18,21,22,33,43,50	LVDS,NVM POWER	MAIN_ON	S0
+1.5V	+1.5V	12,18,19,20,31,32,34,45,46	Mini PCIe,Express Card POWER	MAIN_ON	S0
+1.05V_VTT	+1.05V	4,6,11,12,43,46,48,52	AuBurndale VTT POWER	MAIN_ON	S0
+1.05V_PCH	+1.05V	3,10,12,43,46,52	PCH CORE POWER	1.05V_RUN_ON	S0
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,43,49	VGA CORE POWER	GFXVR_EN	S0
VCC_CORE		6,43,48	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	23	LCD Power	ENVDD	S0
+5V_HDD	+5V	28	HDD Power	MAIN_ON	S0
BAT-V	+10V~+17V	44	MAIN BATTERY	CHG_PBATT	S0~S5

PCH SM BUS

SB710 SMBUS	SMBUS Function Define
SMBCLK0 SMBDAT0 (+3V)	DDR / DDR THER / CLOCK GEN
SMBCLK1 SMBDAT1 (+3V_S5)	LAN IC//WI-FI
SMBCLK2 SMBDAT2 (+3V_S5)	not used

KBC(EC) SM BUS

KBC SMBUS (+3VPCU)	SMBUS Function Define
MBCLK MBDAT	BATTERY (+3VPCU)
2ND_MBCLK 2ND_MBDATA	CPU THER SENSOR(+3V) EC EEPROM (+3VPCU)
3ND_MBCLK 3ND_MBDATA	G-SENSOR(+3VS5)

PROJECT :MK2-Intel
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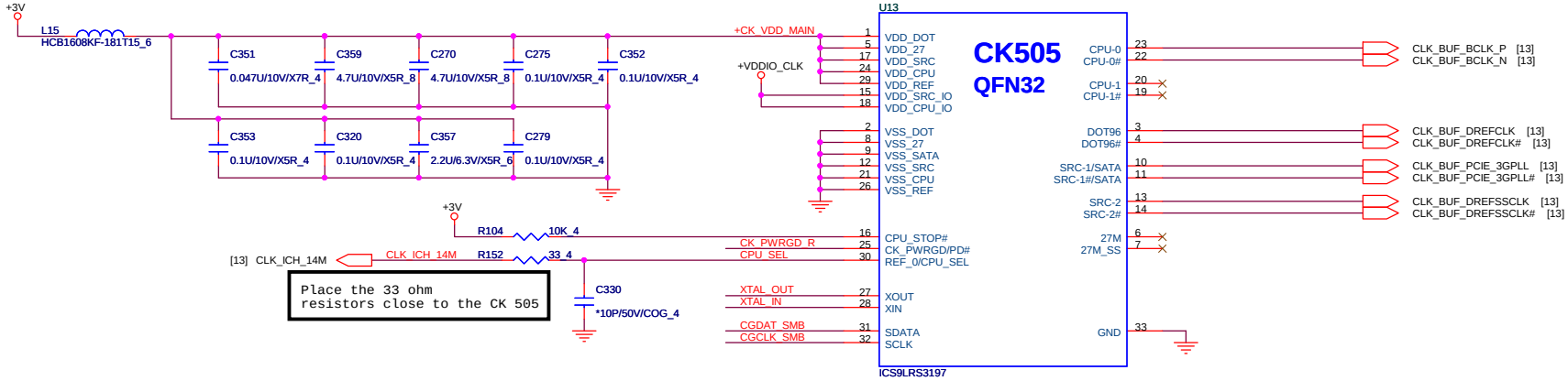
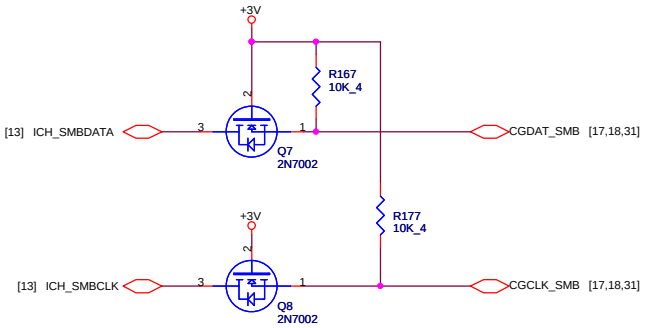
Size	Document Number	Rev
Custom	<Doc>	1C

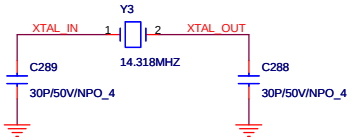
Date: Wednesday, June 23, 2010 Sheet 2 of 42

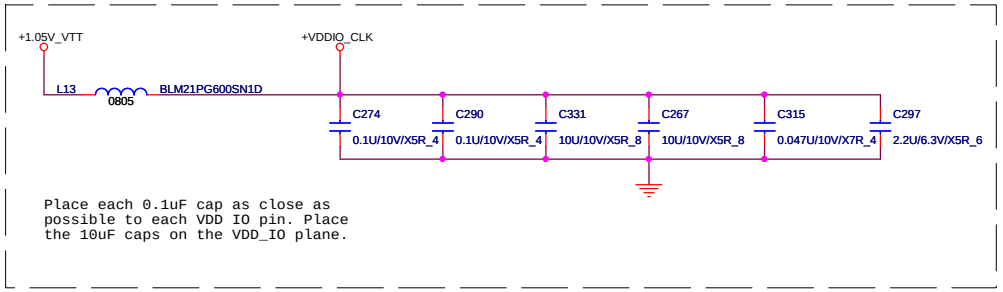
[4,11,12,13,14,15,17,18,19,20,21,22,23,25,26,27,29,30,31,32,33,35,36,38,39] +3V
[4,6,7,11,12,13,14,15,38,39,40] +1.05V_VTT

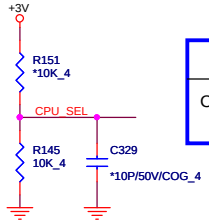
03



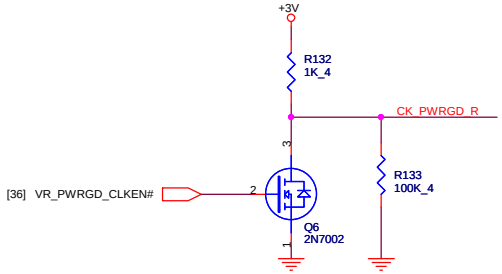






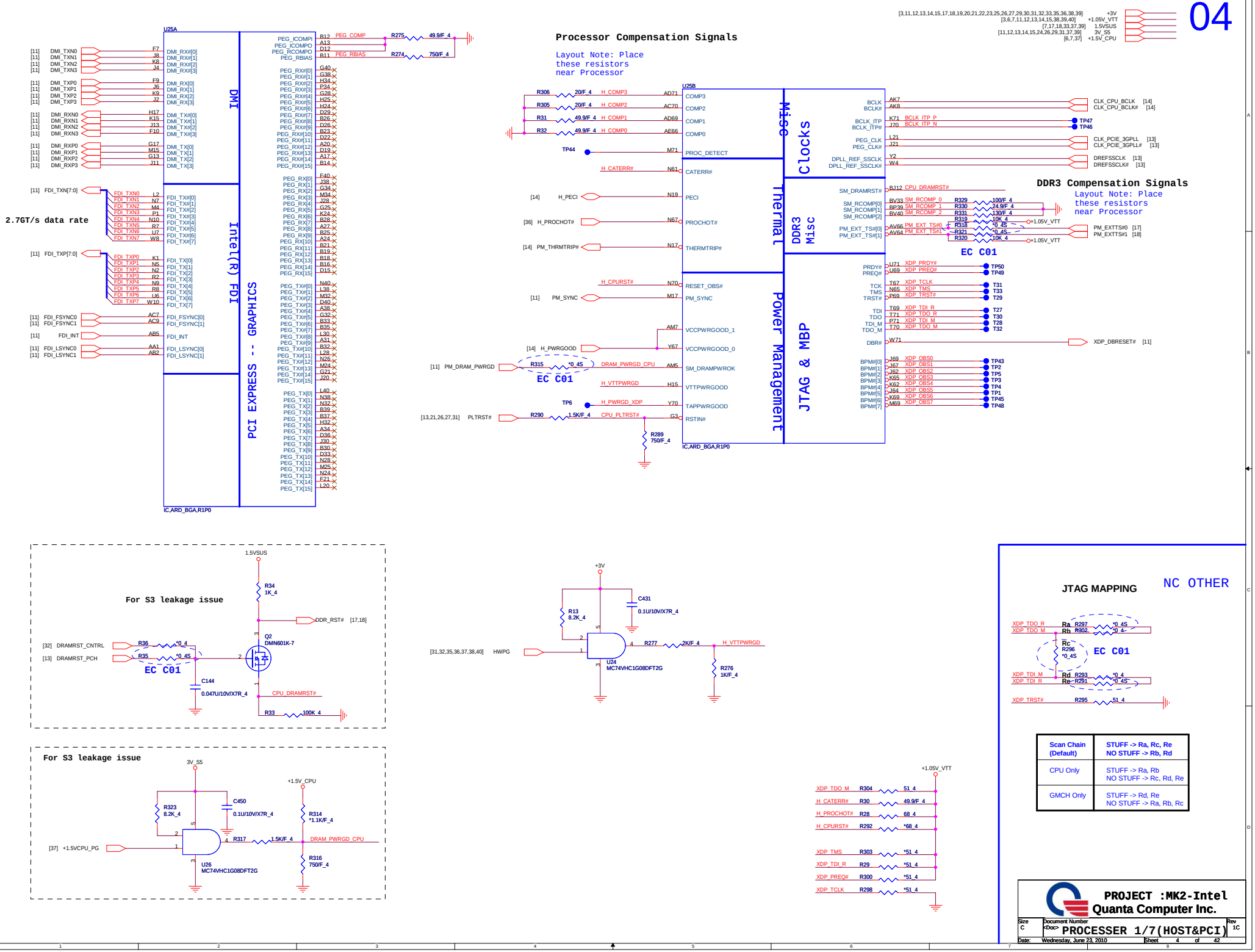


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz



PROJECT :MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Clock Generator	1C
Date: Wednesday, June 23, 2010	Sheet 3 of 42	



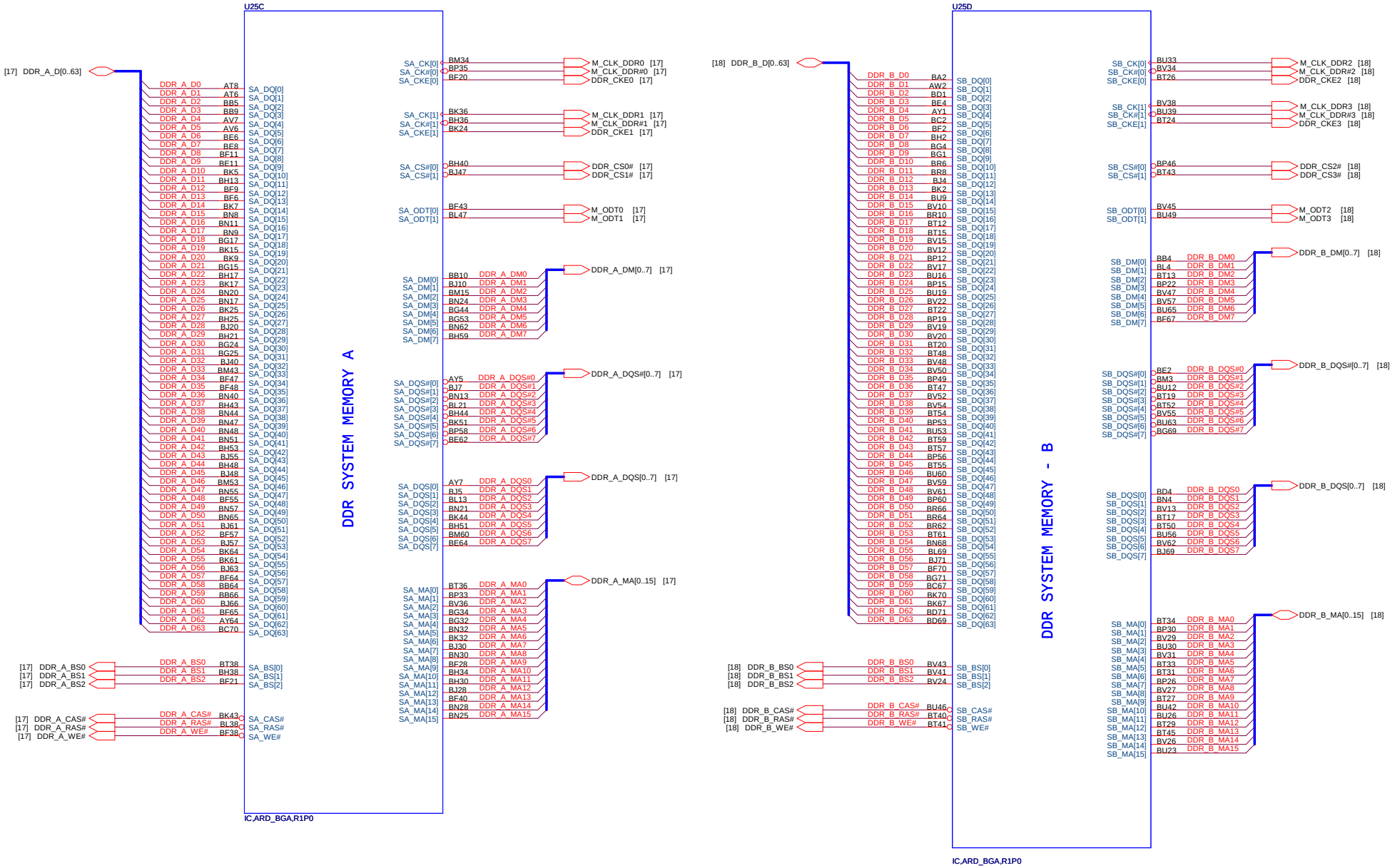
PROJECT :MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
C	<Doc> PROCESSER 1/7(HOST&PCI)	1C

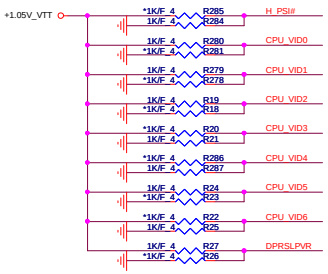
Date: Wednesday, June 23, 2010 Sheet 4 of 42

AUBURNDALE PROCESSOR (DDR3)

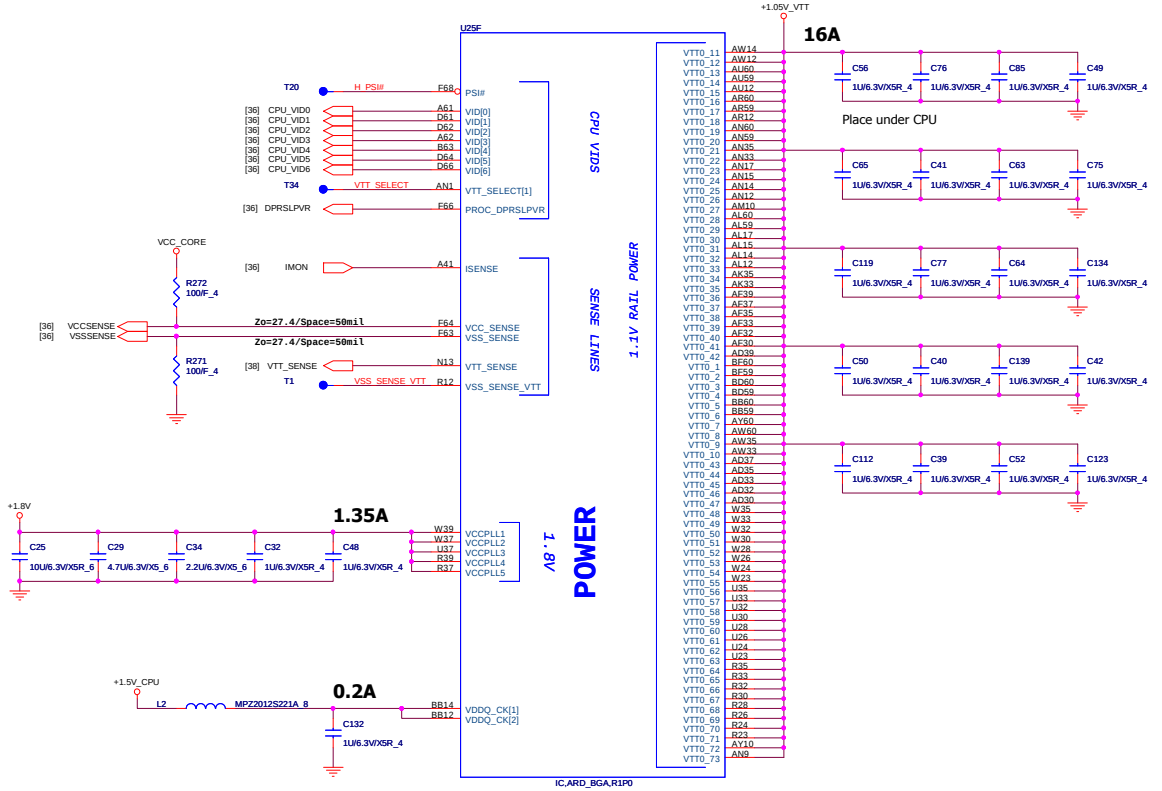
05



PROJECT : MK2-Intel		
Quanta Computer Inc.		
Size: Custom	Document Number: <Doc> PROCESSER 2/7(DDR3)	Rev: 1C
Date: Wednesday, June 23, 2010	Sheet 5 of 42	



HFM_VID : Max 1.4V
LFM_VID : Min 0.65V



PROJECT :MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> PROCESSER 3/7(POWER1)	1C

Date: Wednesday, June 23, 2010 Sheet 6 of 42

[39,40] +VCC_GFX_CORE
[3,4,6,11,12,13,14,15,38,39,40] +1.05V_VTT
[4,6,37] +1.5V_CPU
[4,17,18,33,37,39] 1.5VSUS

Max 12A

+VCC_GFX_CORE

Please note that +VCC_GFX_CORE should be 1.05V in Arrandale

U25G

C92 10U/6.3V/X5R_6, C91 10U/6.3V/X5R_6, C69 10U/6.3V/X5R_6

C68, C79, C78, C109 1U/6.3V/X5R_4

C66, C89, C99, C108 1U/6.3V/X5R_4

C101, C100, C87, C67 1U/6.3V/X5R_4

C111, C110, C86, C88 1U/6.3V/X5R_4

AN32 AN30 AN28 AN26 AN24 AN23 AN21 AN19 AL32 AL30 AL28 AL26 AL24 AL23 AL21 AL19 AK14 AK12 AJ10 AH14 AH12 AF28 AF26 AF24 AF23 AF21 AF19 AF17 AF15 AF14 AD28 AD26 AD24 AD23 AD21 AD19 AD17

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37

GRAPHICS

W21 W19 U21 U19 U17 U15 U14 U12 R21 R19 R17 R15

VTT1_1 VTT1_2 VTT1_3 VTT1_4 VTT1_5 VTT1_6 VTT1_7 VTT1_8 VTT1_9 VTT1_10 VTT1_11 VTT1_21

PEG & DMI

+1.05V_VTT

C113 1U/6.3V/X5R_4, C62 1U/6.3V/X5R_4

AK62 AK60 AK59 AH60 AH59 AF60 AF59 AD60 AD59 AB60 AB59 AA60 AA59 W60 W59 U60 U59 R60 R59

VCAP2_1 VCAP2_2 VCAP2_3 VCAP2_4 VCAP2_5 VCAP2_6 VCAP2_7 VCAP2_8 VCAP2_9 VCAP2_10 VCAP2_11 VCAP2_12 VCAP2_13 VCAP2_14 VCAP2_15 VCAP2_16 VCAP2_17 VCAP2_18 VCAP2_19

+VCAP2

C70, C102, C90, C55, C43 1U/6.3V/X5R_4

POWER

IC,ARD_BGA,R1P0

SENSE LINES

VAXG_SENSE AF12 → VCC_AXG_SENSE [40]
VSSAXG_SENSE AF10 → VSS_AXG_SENSE [40]

GRAPHICS VIDS

GFX_VID[0] AF71 → GFXVR_VID_0 [40]
GFX_VID[1] AG67 → GFXVR_VID_1 [40]
GFX_VID[2] AG70 → GFXVR_VID_2 [40]
GFX_VID[3] AH71 → GFXVR_VID_3 [40]
GFX_VID[4] AN71 → GFXVR_VID_4 [40]
GFX_VID[5] AM67 → GFXVR_VID_5 [40]
GFX_VID[6] AM70 → GFXVR_VID_6 [40]

EC C01

GFX_VR_EN AH69 GFXVR_EN → GFXVR_EN [40]
GFX_DPRSLPVR AL71 GFX_DPRSLPVR R310 *0_4S → GFXVR_DPRSLPVR [40]
GFX_IMON AL69 GFX_IMON R312 *0_4S → GFXVR_IMON [40]

GFXVR_EN R309 4.7K_4
GFX_IMON R311 *1K_4

DDR3 - 1.5V RAILS

VDDQ1 BU40, VDDQ2 BU35, VDDQ3 BU28, VDDQ4 BN38, VDDQ5 BM25, VDDQ6 BL30, VDDQ7 BJ38, VDDQ8 BH32, VDDQ9 BH28, VDDQ10 BG43, VDDQ11 BF16, VDDQ12 BF15, VDDQ13 BD35, VDDQ14 BD33, VDDQ15 BD32, VDDQ16 BD30, VDDQ17 BD28, VDDQ18 BD26, VDDQ19 BD24, VDDQ20 BD23, VDDQ21 BD21, VDDQ22 BD19, VDDQ23 BD17, VDDQ24 BD15, VDDQ25 BB35, VDDQ26 BB33, VDDQ27 BB32, VDDQ28 BB30, VDDQ29 BB28, VDDQ30 BB26, VDDQ31 BB24, VDDQ32 BB23, VDDQ33 BB21, VDDQ34 BB19, VDDQ35 BB17, VDDQ36 BB15

3A

+1.5V_CPU

C137, C124, C138, C130, C131 1U/6.3V/X5R_4

C141 *10U/6.3V/X5R_6, C140 10U/6.3V/X5R_6, C142 10U/6.3V/X5R_6, + C143 *330U/2.5V_3528

1.5VSUS — C146 0.1U/10V/X7R_4 — C147 0.1U/10V/X7R_4 — +1.5V_CPU

2.6A

VTT0_DDR AW32 AW30 AW28 AW26 AW24 AW23 AW21 AW19 AW17 AW15

VTT0_DDR[1] VTT0_DDR[2] VTT0_DDR[3] VTT0_DDR[4] VTT0_DDR[5] VTT0_DDR[6] VTT0_DDR[7] VTT0_DDR[8] VTT0_DDR[9]

+1.05V_VTT

C122, C120, C121 1U/6.3V/X5R_4

VTT1_12 AD15, VTT1_13 AD14, VTT1_14 AD12, VTT1_15 AB12, VTT1_16 AA12, VTT1_17 W17, VTT1_18 W15, VTT1_19 W14, VTT1_20 W12

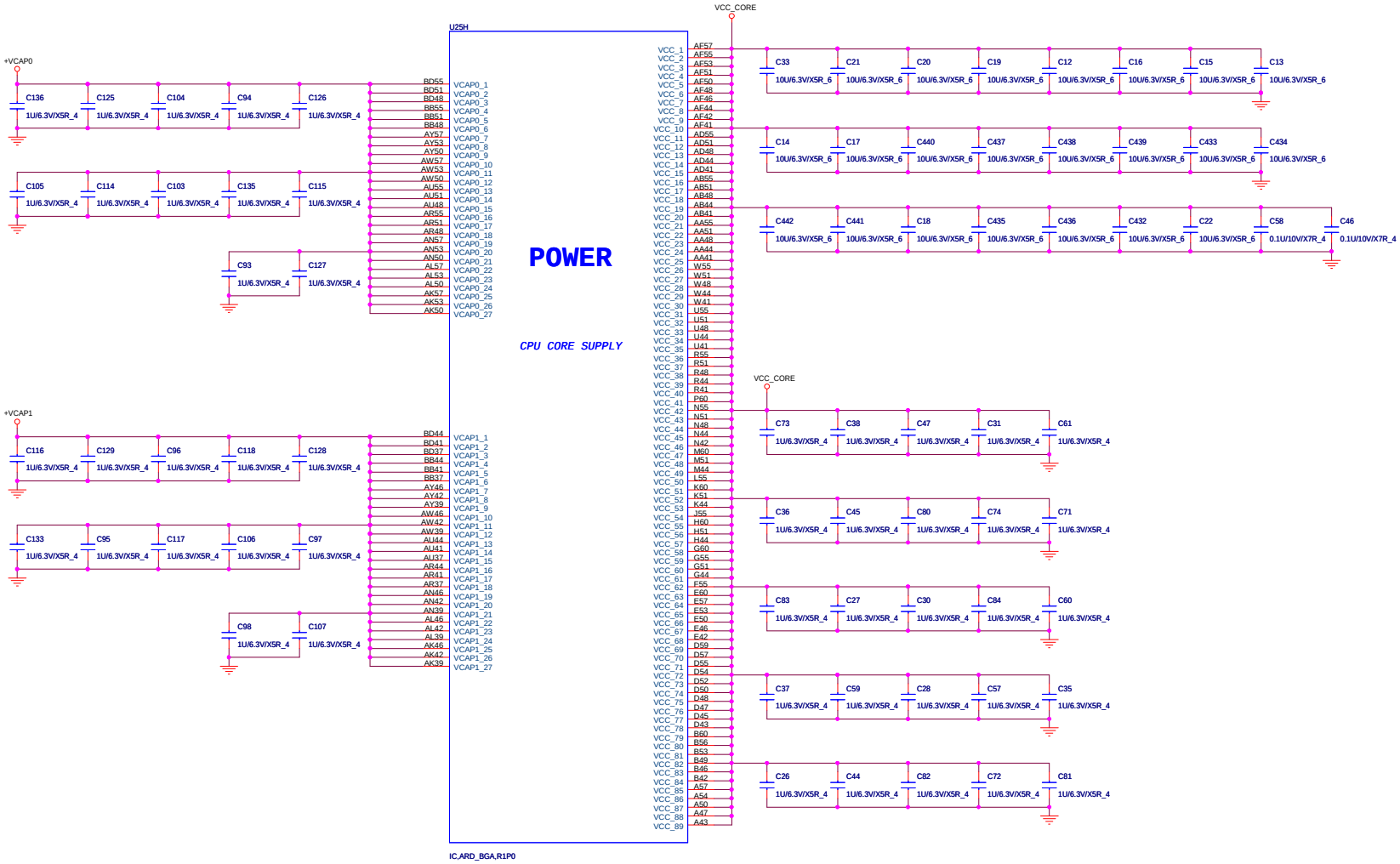
+1.05V_VTT

C54 10U/6.3V/X5R_6, C51 1U/6.3V/X5R_4, C53 1U/6.3V/X5R_4

PROJECT :MK2-Intel
Quanta Computer Inc.

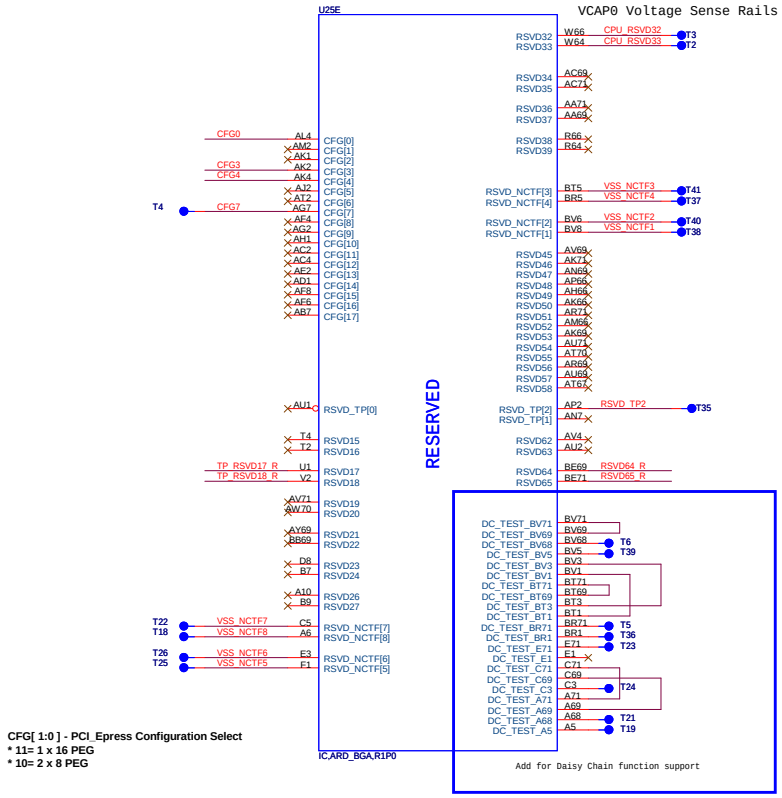
Size	Document Number	Rev
Custom	<Doc> PROCESSER 4/7(POWER2)	1C

Date: Wednesday, June 23, 2010 Sheet 7 of 42



Size C	Document Number <Doc>		Rev 1C
	PROCESSER 5/7(POWER3)		
Date: Wednesday, June 23, 2010		Sheet 8 of 42	

PROJECT :MK2-Intel
Quanta Computer Inc.

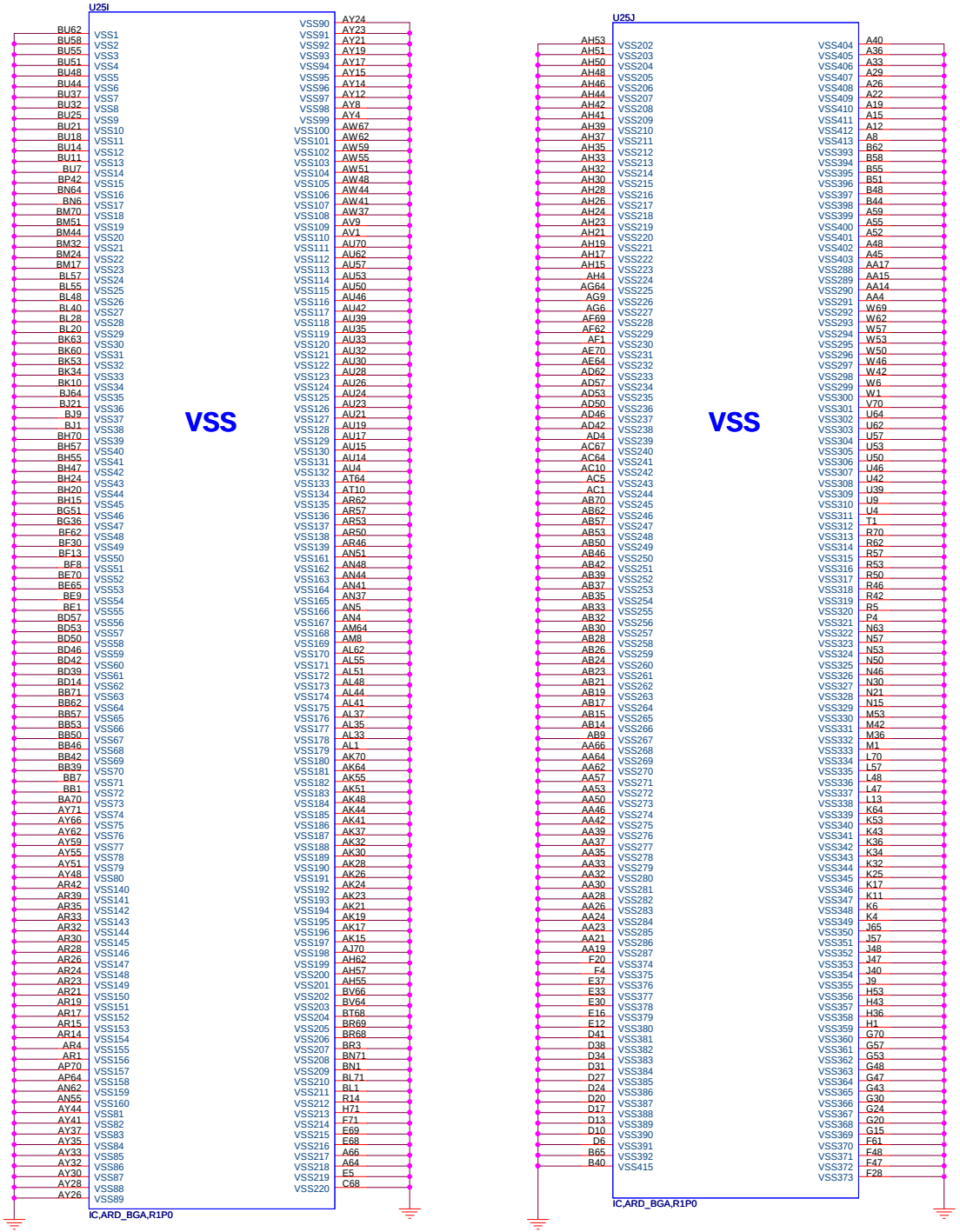


CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

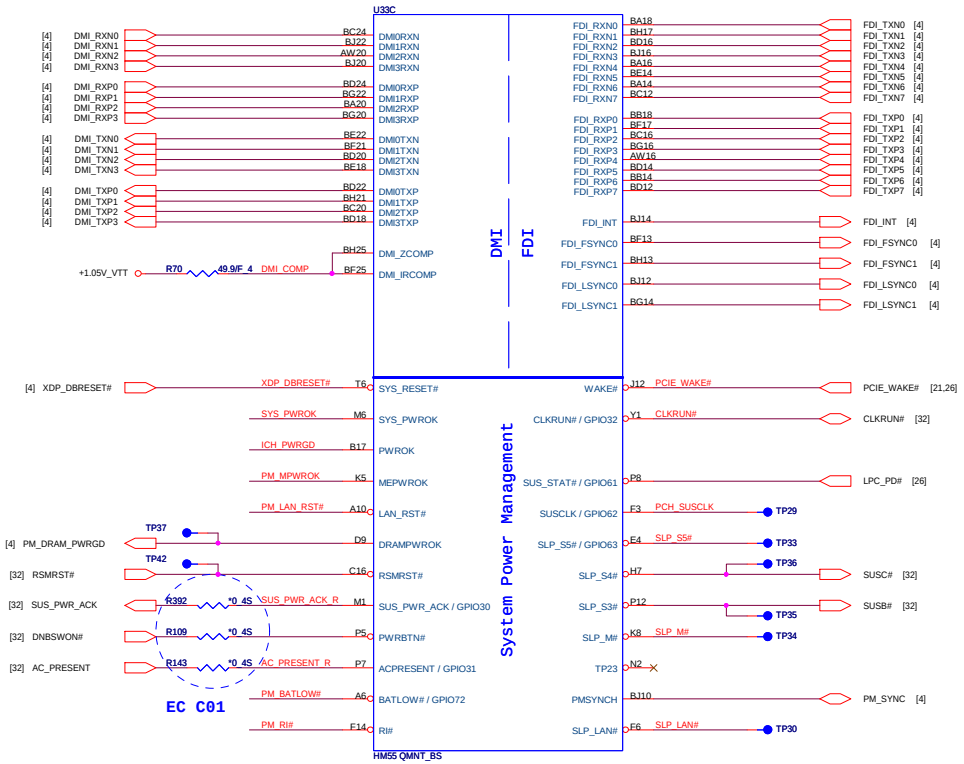
ARRANDALE PROCESSOR (GND)

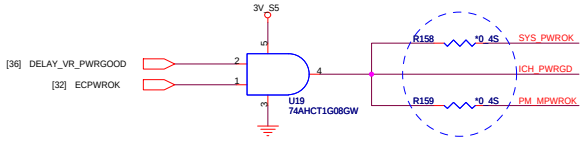


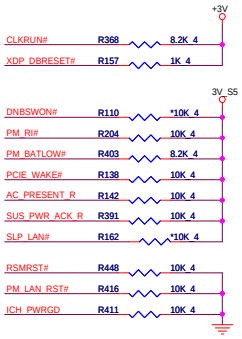
PROJECT :MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> PROCESSER 7/7(GND)	1C
Date: Wednesday, June 23, 2010	Sheet 10 of 42	

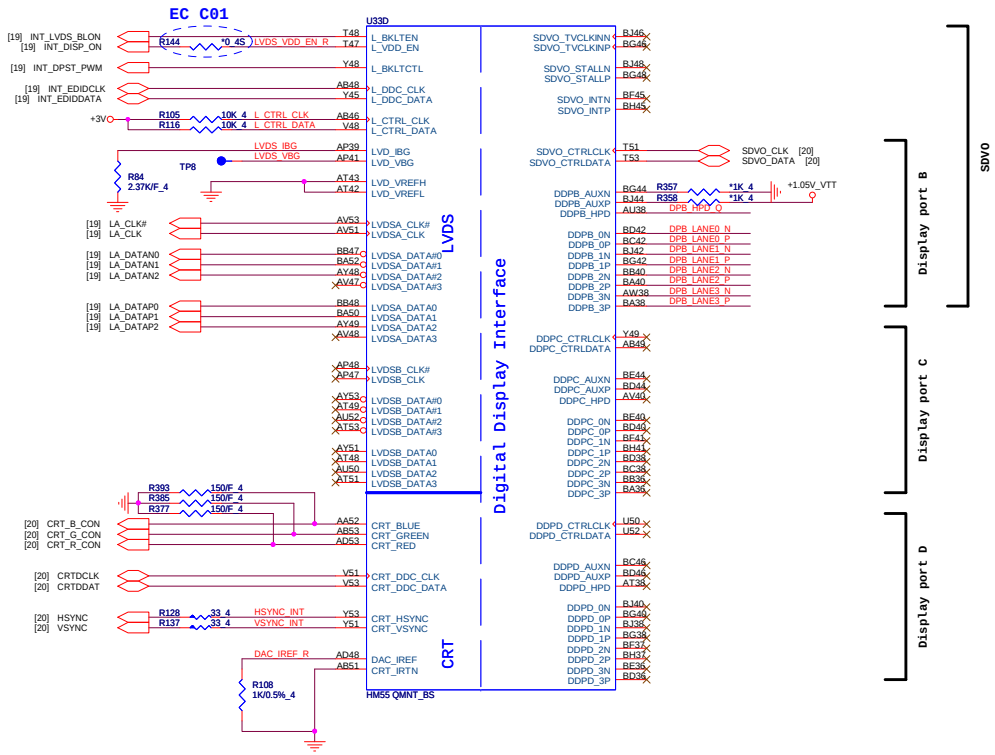
IBEX PEAK-M (DMI,FDI,GPIO)



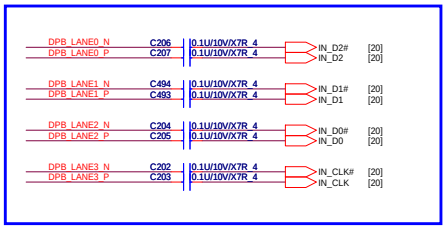


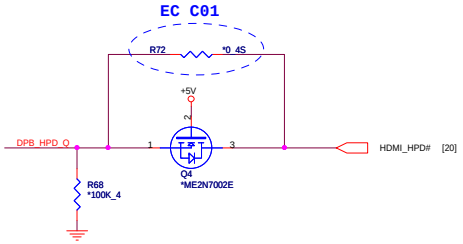


IBEX PEAK-M (LVDS,DDI)



For UMA HDMI Function





PROJECT :MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc>	1C

PCH 1/6 (DMI&VIDEO)

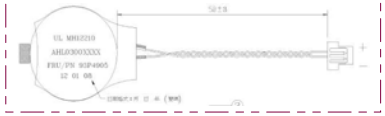
Date: Wednesday, June 23, 2010 Sheet 11 of 42

[15,32] +3VRTC
[19,20,21,24,28,31,32,34,35,38,39] 3VPCU
[3,4,11,13,14,15,17,18,19,20,21,22,23,25,26,27,29,30,31,32,33,35,36,38,39] +3V
[4,11,13,14,15,24,26,29,31,37,39] 3V_S5
[3,4,6,7,11,13,14,15,38,39,40] +1.05V_VTT

IBEX PEAK-M (HDA,JTAG,SATA)

+3VRTC
RB500V-40 D17
3VPCU
C376 1U/6.3V/X5R_4
+3VRTC_2
D18 RB500V-40
R226 20K/F_4
R244 20K/F_4
C404 1U/6.3V/X5R_4
G2 *SHORT_PAD1
C396 1U/6.3V/X5R_4
G1 *SHORT_PAD1
R445 1K/F_4
20MIL +3VRTC_BAT
R225 1M/F_4
BT1 RTC_CON
5VPCU 20MIL 20MIL
R449 *1.2K/F_4 VCCRTC_1
R450 *1K/F_4 VCCRTC_3
Q27 *MMBT3904-7-F
R454 *4.7K_4
VCCRTC_REF
R455 *15K/F_4

RTC P/N: AHL03002009 (CR2025)
Don't support chargeable Battery



C512 12P/50V/C0G_4
EC C09
Y6 32.768KHZ
R221 10M_4
C510 12P/50V/C0G_4
Cap values depend on Xtal

RTC_X1
RTC_X2
RTC_RST#
SRTC_RST#
SM_INTRUDER#
+3VRTC R232 330K_4 PCH_INVRMEN

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

[22] ACZ_SPKR
[22] ACZ_SDIN0
TP40
TP39
TP38
R219 *1K_4
ACZ_SDOUT
+3V R220 *1K_4 HDA_DOCK_EN#
3V_S5 R170 *10K_4 HDA_DOCK_RST#

TP61 PCH_JTAG_TCK_BUF
TP62 PCH_JTAG_TMS
TP60 PCH_JTAG_TDI
TP64 PCH_JTAG_TDO
TP63 PCH_JTAG_RST#

TP56 SPI_CS1#
SPI_CLK_R
SPI_CS0#_R
SPI_SI_R
SPI_SO

U33A

RTCX1	B13	RTC	
RTCX2	D13		
RTCRST#	C14		
SRTCRST#	D17		
INTRUDER#	A16		
INTVRMEN	A14		
HDA_BCLK	A30	IHDA	
HDA_SYNC	D29		
SPKR	P1		
HDA_RST#	C30		
HDA_SDIN0	G30		
HDA_SDIN1	F30		
HDA_SDIN2	E32		
HDA_SDIN3	F32		
HDA_SDO	B29		
HDA_DOCK_EN# / GPIO33	H32		
HDA_DOCK_RST# / GPIO13	J30		
JTAG_TCK	M3	JTAG	
JTAG_TMS	K3		
JTAG_TDI	K1		
JTAG_TDO	J2		
JTAG_RST#	J4		
SPI_CLK	BA2	SPI	
SPI_CS0#	AV3		
SPI_CS1#	AY3		
SPI_MOSI	AY1		
SPI_MISO	AV1		

FWH0 / LAD0	D33	LPC	LAD0 [26,32]
FWH1 / LAD1	B33		LAD1 [26,32]
FWH2 / LAD2	C32		LAD2 [26,32]
FWH3 / LAD3	A32		LAD3 [26,32]
FWH4 / LFRAME#	C34		LFRAME# [26,32]
LDRQ0#	A34		LPC_DRQ#0 [26]
LDRQ1# / GPIO23	E34		LCD_BK_OFF [19]
SERIRQ	AB9		SERIRQ [26,32]
SATA0RXN	AK7	SATA	SATA_RXN0_C
SATA0RXP	AK6		SATA_RXP0_C
SATA0TXN	AK11		SATA_TXN0_C
SATA0TXP	AK9		SATA_TXP0_C
SATA1RXN	AH6		
SATA1RXP	AH5		
SATA1TXN	AH9		
SATA1TXP	AH8		
SATA2RXN	AF11		
SATA2RXP	AF9		
SATA2TXN	AF7		
SATA2TXP	AF6		
SATA3RXN	AH3		
SATA3RXP	AH1		
SATA3TXN	AF3		
SATA3TXP	AF1		
SATA4RXN	AD9		
SATA4RXP	AD8		
SATA4TXN	AD6		
SATA4TXP	AD5		
SATA5RXN	AD3		
SATA5RXP	AD1		
SATA5TXN	AB3		
SATA5TXP	AB1		
SATAICOMPO	AF16		
SATAICOMPI	AF15		SATA_COMP R107 37.4/F_4 +1.05V_VTT
SATALED#	T3		SATA_LED# R380 *10K_4 +3V TP59
SATA0GP / GPIO21	Y9		PCH_GPIO21 R101 10K_4 +3V TP18
SATA1GP / GPIO19	V1		PCH_GPIO19 R372 10K_4 +3V TP58

HM55 QMNT_BS

C452 0.01U/16V/X7R_4
C453 0.01U/16V/X7R_4
C456 0.01U/16V/X7R_4
C455 0.01U/16V/X7R_4
SATA_RXN0 [23]
SATA_RXP0 [23]
SATA_TXN0 [23]
SATA_TXP0 [23]
SATA HDD

Place AC Coupling CAP near to CONN

Distance between the PCH and cap on the "P" signal should be identical distace between the PCH and cap on the "N" signal for the same pair.

[22] BIT_CLK_AUDIO R430 33_4 ACZ_BIT_CLK
C514 *10P/50V/COG_4
[22] ACZ_SYNC_AUDIO R435 33_4 ACZ_SYNC
[22] ACZ_RST#_AUDIO R429 33_4 ACZ_RST#
[22] ACZ_SDOUT_AUDIO R440 33_4 ACZ_SDOUT

Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R651, R652, R650 & R653 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

No Reboot Strap

+3V
Place near connector
R383 *1K_4 ACZ_SPKR
R118 10K_4 SERIRQ

iTPM ENABLE/DISABLE

+3V R342 *1K_4 SPI_SI

TPM Function	R292
Enable	Stuff
Disable	NC (Default)

For ME F/W
32Mbit (4M Byte), SPI

+3V R364 3.3K_4
SPI_CS0#_R R362 15_4 SPI_CS0#
SPI_CLK_R R360 15_4 SPI_CLK
SPI_SI_R R361 15_4 SPI_SI
SPI_SO R363 15_4 SPI_SO_R
C480 22P/50V/NPO_4

U31
CE# SCK SI SO WP# VDD HOLD# VSS
MX25L3205DM2I

C479 0.1U/10V/X7_4
+3V R339 *0_6S
R341 10K_4
EC C01

PROJECT :MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> PCH 2/6 (SATA&HDA&JTA)	1C
Date: Wednesday, June 23, 2010	Sheet 12 of 42	

IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

13

USB port Assignment function

USB0	USB Connector onboard
USB1	USB Connector onboard
USB2	USB Connector (Wire to board)
USB3	Camera
USB4	Mini PCI E-WLAN
USB5	Mini PCI E-WWAN
USB6	X
USB7	X
USB8	X
USB9	X
USB10	X
USB11	USB Card Reader
USB12	X
USB13	BLUETOOTH

EC C01

EC C01

FOR EMI

Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

No stuff XTAL25_IN and XTAL25_OUT circuitry until integrated CG becomes PCH POR.

Boot BIOS Strap		
PCI_GNT0#	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

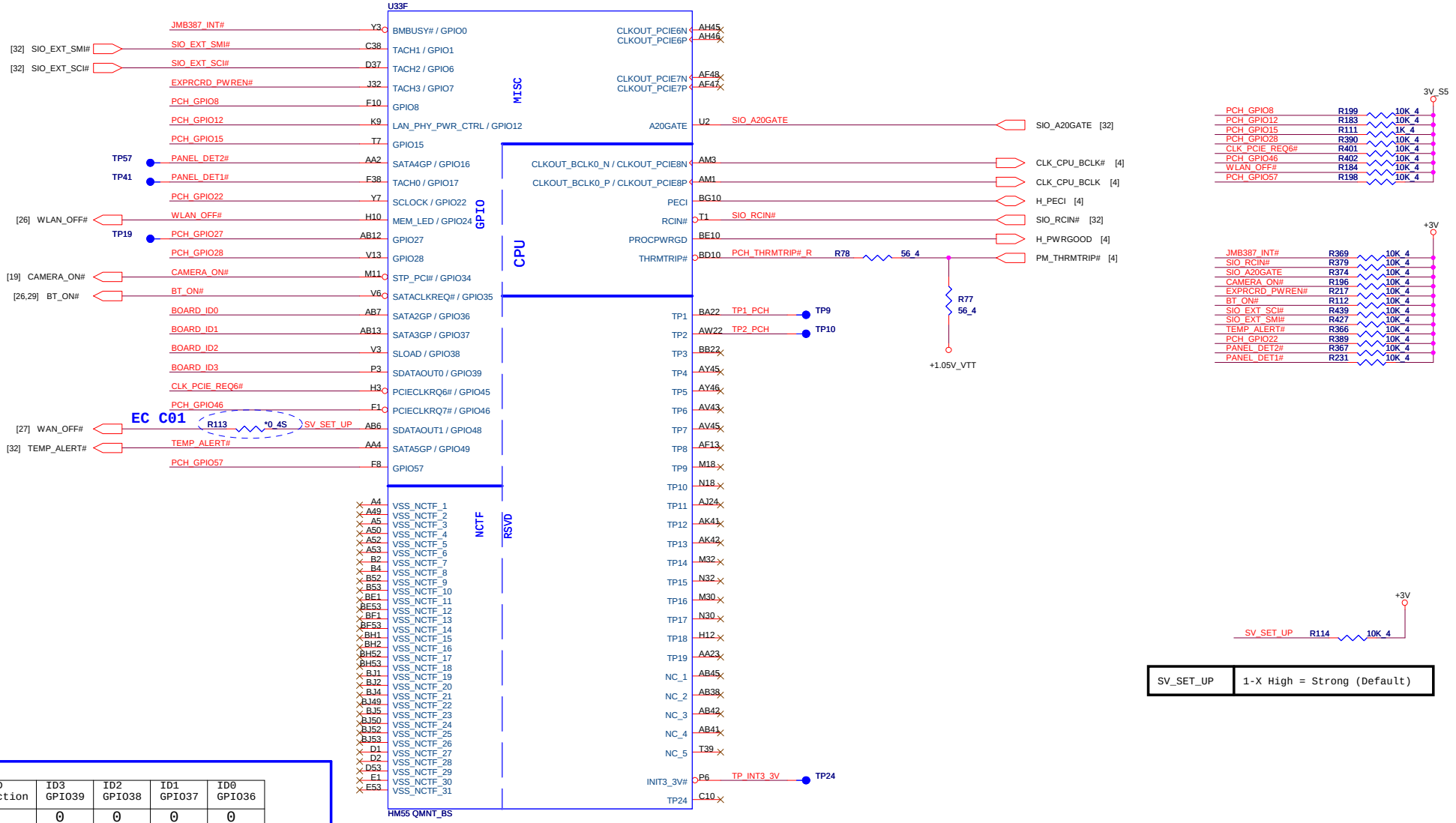
Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 Swap override/Top-Block Swap Override enabled High = Default

PROJECT :MK2-Intel
Quanta Computer Inc.

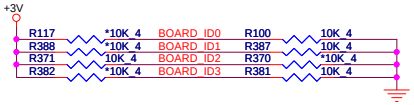
Size	Document Number	Rev
Custom	<Doc> PCH 3/6 (PCI)	1C
Date: Wednesday, June 23, 2010	Sheet 13 of 42	

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



SV_SET_UP	1-X High = Strong (Default)

Board ID For Function	ID3 GPIO39	ID2 GPIO38	ID1 GPIO37	ID0 GPIO36
DU1-SDV	0	0	0	0
MK2-SDV	0	0	0	1
DU1-SIT1(FL6)	0	0	1	0
MK2-SIT1(FL7)	0	0	1	1
DU1-SIT2(FL6)	0	1	0	0
MK2-SIT2(FL7)	0	1	0	1

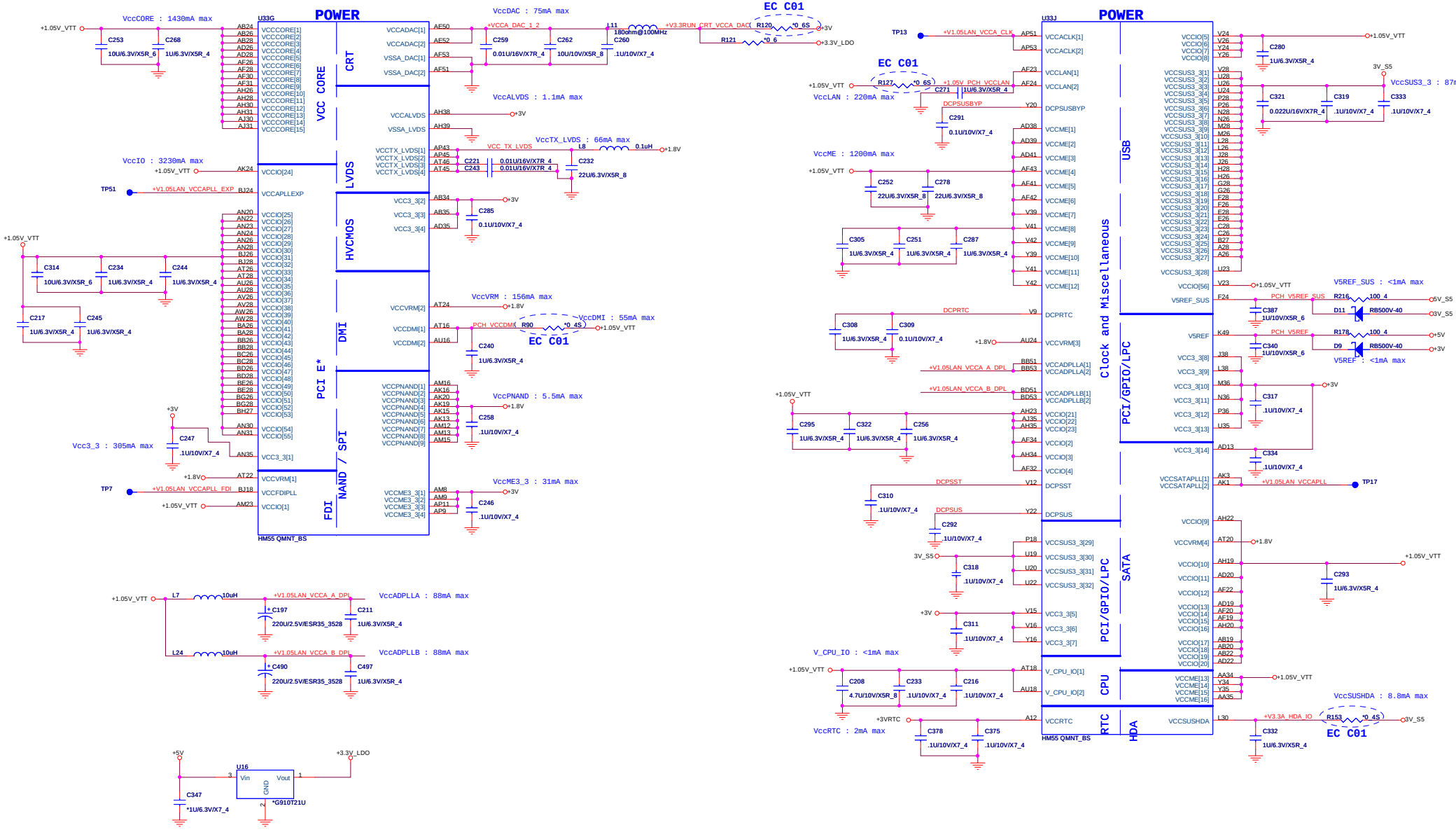


PROJECT :MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> PCH 4/6 (GPIO)	1C
Date: Wednesday, June 23, 2010	Sheet 14 of 42	

IBEX PEAK-M (POWER)

[3,4,11,12,13,14,17,18,19,20,21,22,23,25,26,27,29,30,31,32,33,35,36,38,39] +3V
[4,11,12,13,14,24,26,29,31,37,39] 3V_S5
[24,39] 5V_S5
[11,19,20,22,23,28,30,32,33,39] +5V
[3,4,6,7,11,12,13,14,38,39,40] +1.05V_VTT
[6,13,38,39] +1.8V
[12,32] +3VRTC



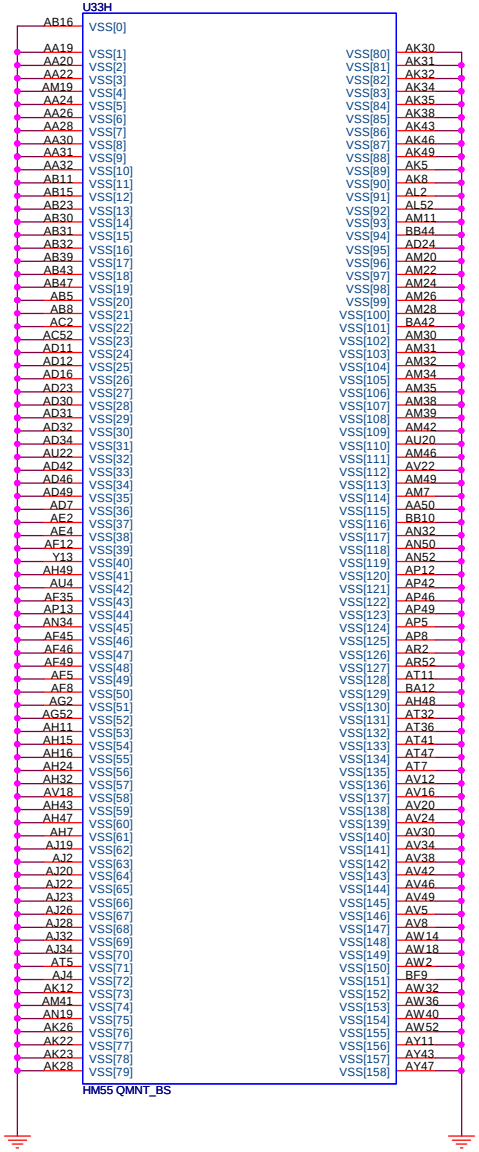
PROJECT :MK2-Intel
Quanta Computer Inc.

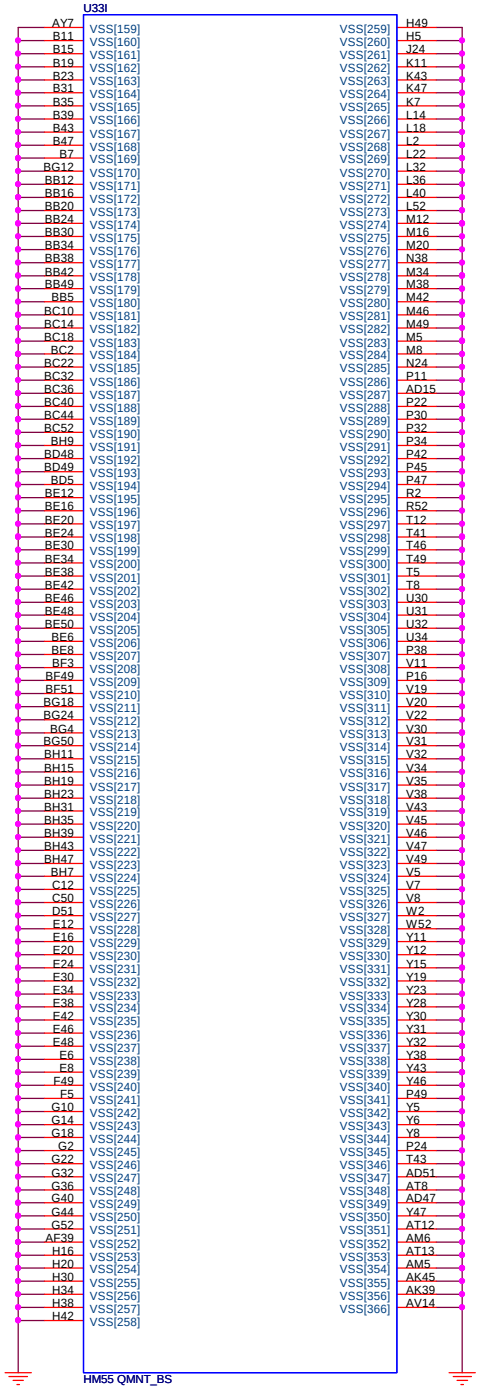
Size	Document Number	Rev
Custom	<Doc>	1C

PCH 5/6 (POWER)

Date: Wednesday, June 23, 2010 Sheet 15 of 42

IBEX PEAK-M (GND)

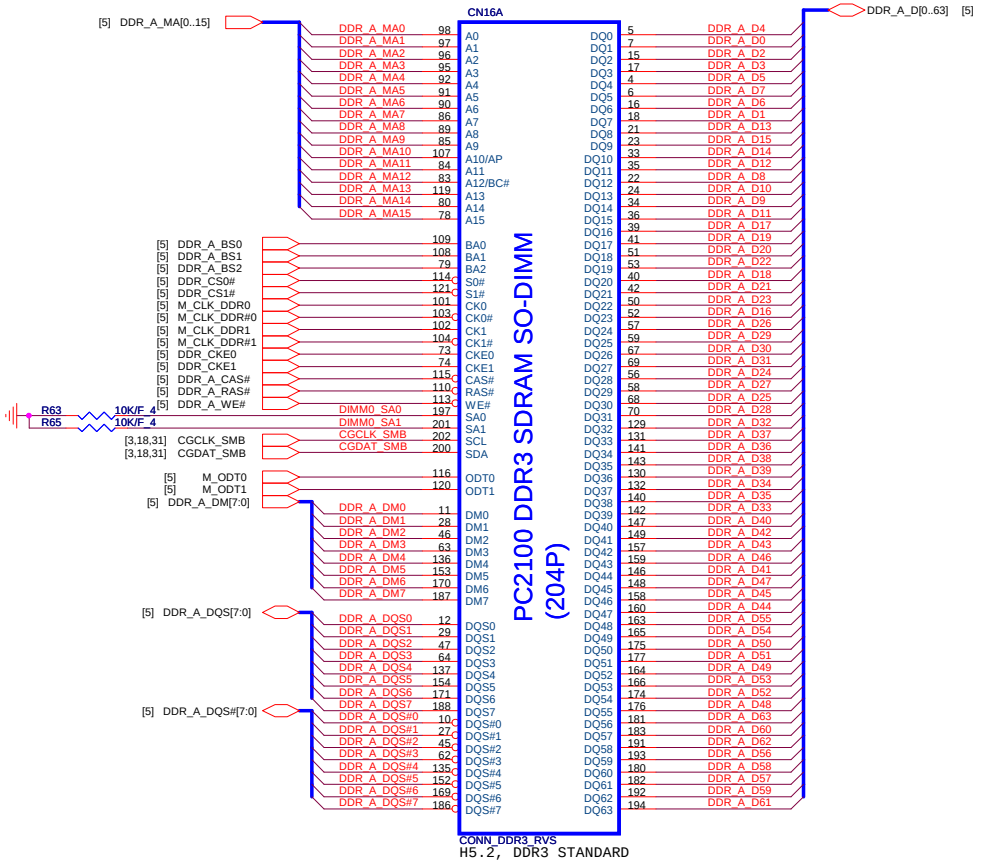


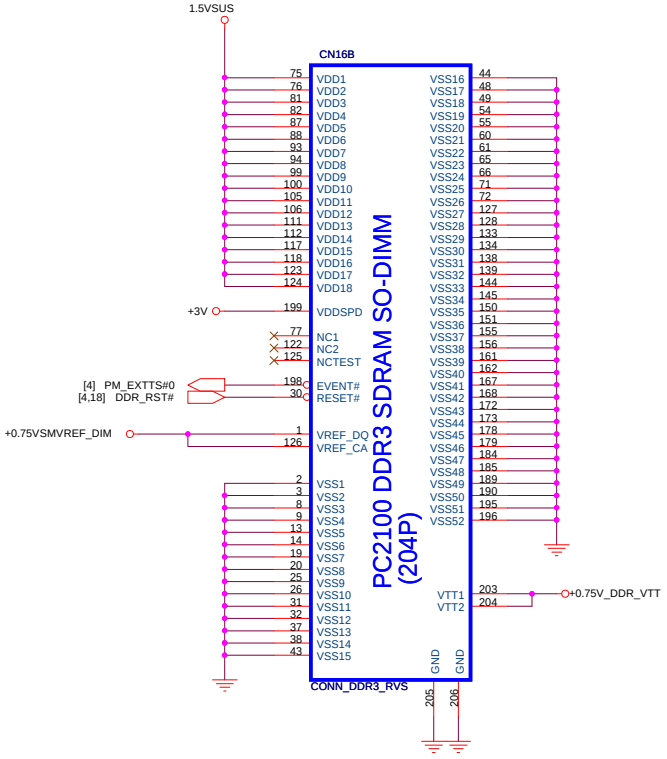


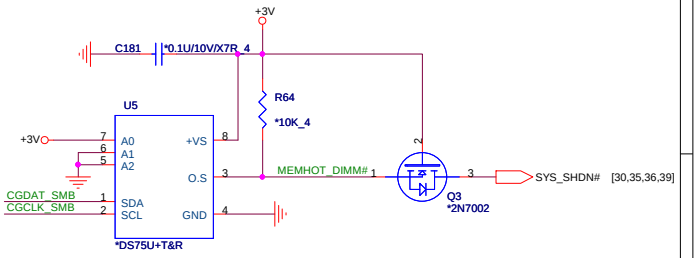
PROJECT :MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> PCH 6/6 (GND)	1C
Date: Wednesday, June 23, 2010	Sheet 16 of 42	

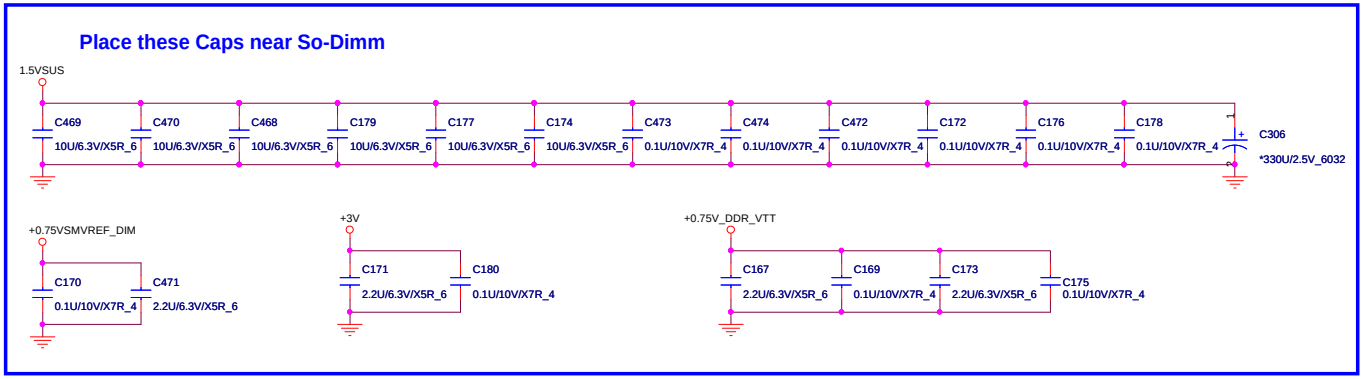
[4,7,18,33,37,39] 1.5VSUS
[3,4,11,12,13,14,15,18,19,20,21,22,23,25,26,27,29,30,31,32,33,35,36,38,39] +3V
[18] +0.75VSMVREF_DIM
[18,37,39] +0.75V_DDR_VTT







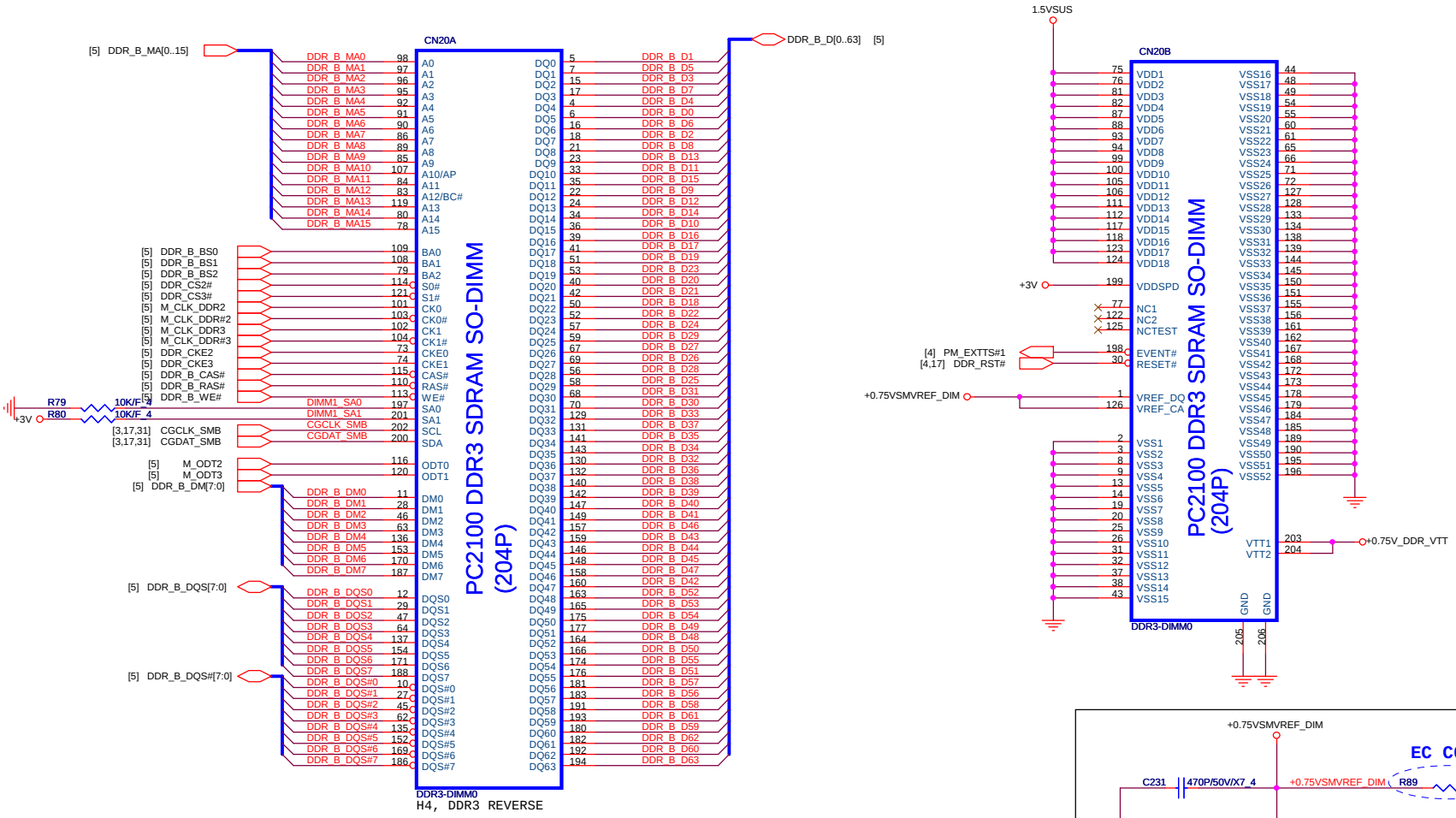
ADDRESS: 92H Close DDR3 socket CN22,CN23



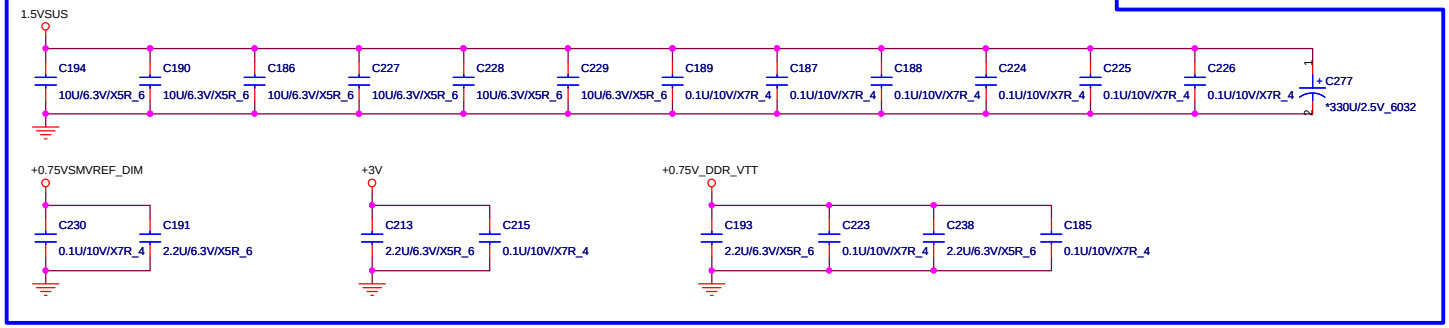
PROJECT :MK2-Intel
Quanta Computer Inc.

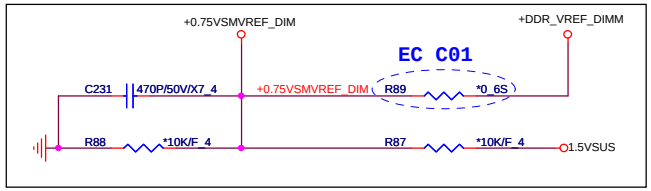
Size	Document Number	Rev
Custom	<Doc> DDR3 (A) SO-DIMM STD	1C
Date: Wednesday, June 23, 2010	Sheet 17 of 42	

[4,7,17,33,37,39] 1.5VSUS
[3,4,11,12,13,14,15,17,19,20,21,22,23,25,26,27,29,30,31,32,33,35,36,38,39] +3V
[17,37,39] +0.75V_DDR_VTT
[17] +0.75VSMVREF_DIM
[37] +DDR_VREF_DIMM



Place these Caps near So-Dimm

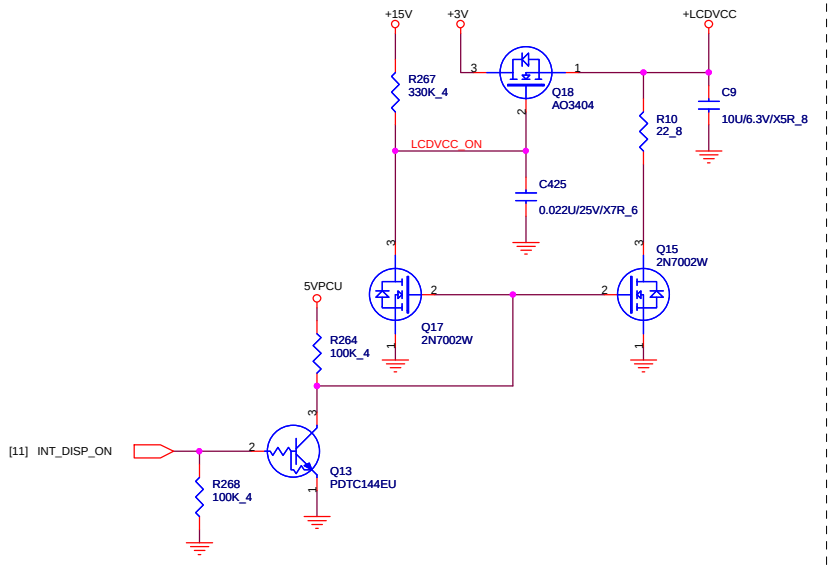




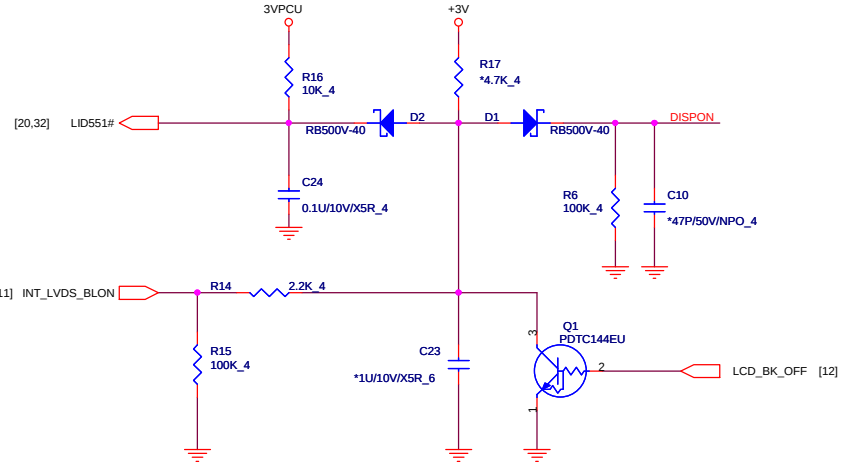
PROJECT :MK2-Intel
Quanta Computer Inc.

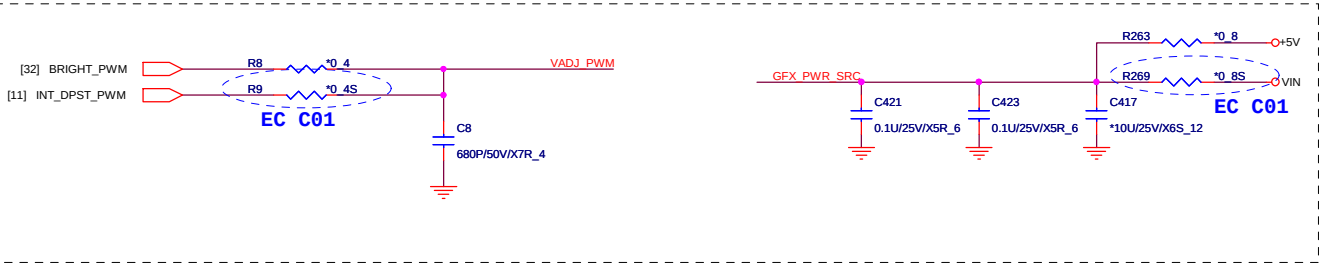
Size	Document Number	Rev
Custom	<Doc> DDR3 (B) SO-DIMM RVS	1C
Date: Wednesday, June 23, 2010	Sheet 18 of 42	

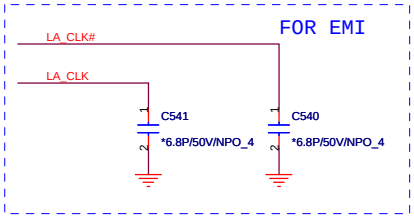
LCDVCC

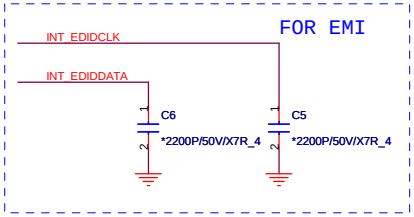


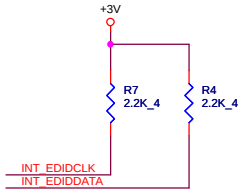
Back light



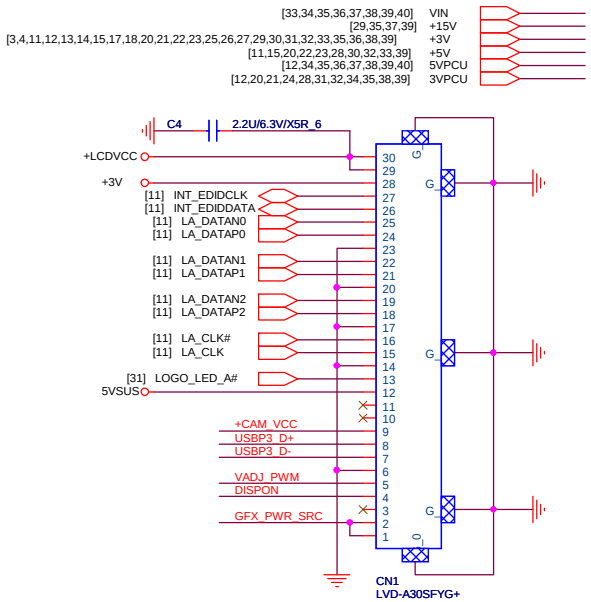




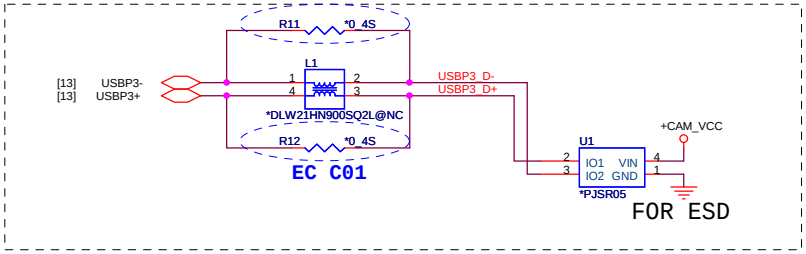




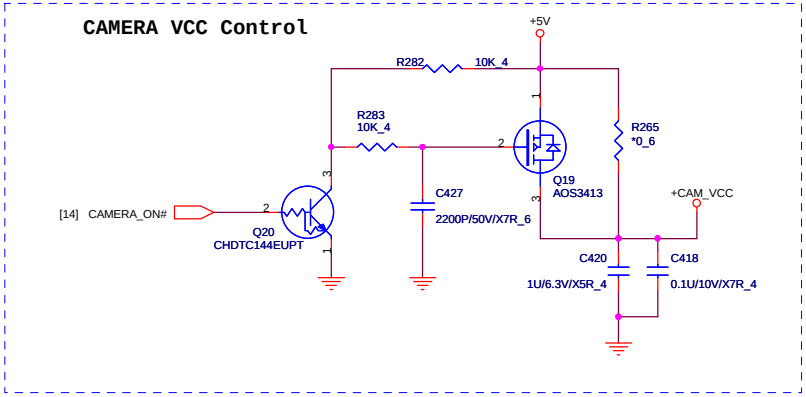
LVDS (11.6") (1024x600, 1366x768)



EC C01

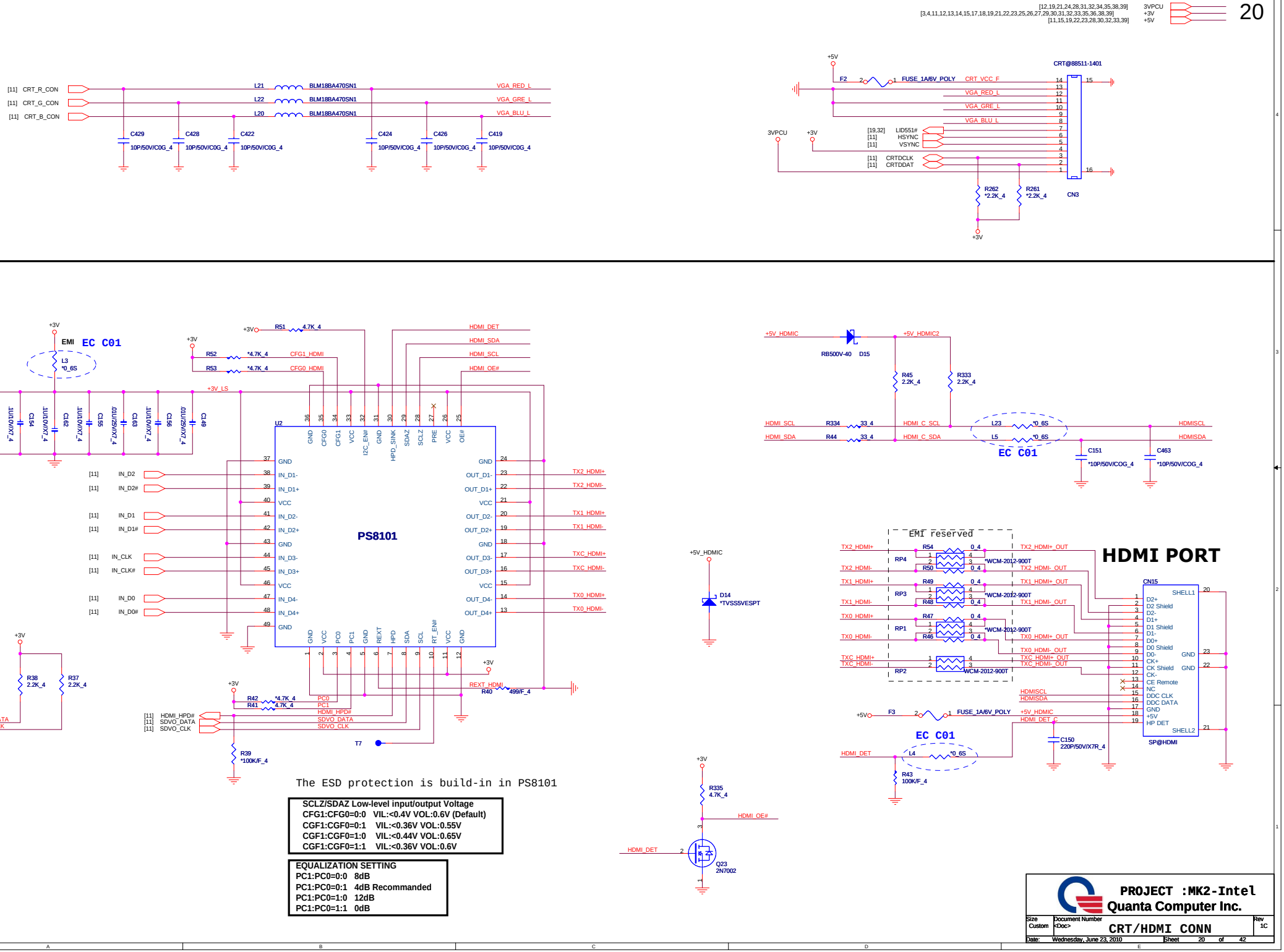


CAMERA VCC Control



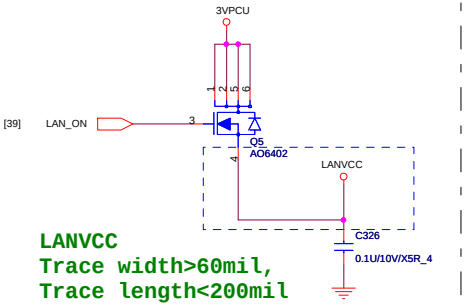
PROJECT :MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> LCD/CAMERA	1C
Date: Wednesday, June 23, 2010	Sheet 19 of 42	

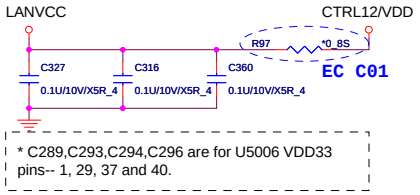

[12,19,21,24,28,31,32,34,35,38,39] 3VPCU
[3,4,11,12,13,14,15,17,18,19,21,22,23,25,26,27,29,30,31,32,33,35,36,38,39] +3V
[11,15,19,22,23,28,30,32,33,39] +5V
[11] CRT_R_CON
[11] CRT_G_CON
[11] CRT_B_CON
L21 BLM18BA470SN1
L22 BLM18BA470SN1
L20 BLM18BA470SN1
VGA_RED_L
VGA_GRE_L
VGA_BLU_L
C429 10P/50V/C0G_4
C428 10P/50V/C0G_4
C422 10P/50V/C0G_4
C424 10P/50V/C0G_4
C426 10P/50V/C0G_4
C419 10P/50V/C0G_4
+5V
F2 FUSE_1A/6V_POLY
CRT_VCC_F
CRT@88511-1401
[19,32] LID551#
[11] HSYNC
[11] VSYNC
[11] CRTDCLK
[11] CRTDDAT
R262 *2.2K_4
R261 *2.2K_4
CN3
EMI EC C01
L3 *0_6S
R51 4.7K_4
R52 *4.7K_4
R53 *4.7K_4
CFG1_HDMI
CFG0_HDMI
HDMI_DET
HDMI_SDA
HDMI_SCL
HDMI_OE#
+3V_LS
U2
PS8101
[11] IN_D2
[11] IN_D2#
[11] IN_D1
[11] IN_D1#
[11] IN_CLK
[11] IN_CLK#
[11] IN_D0
[11] IN_D0#
TX2_HDMI+
TX2_HDMI-
TX1_HDMI+
TX1_HDMI-
TXC_HDMI+
TXC_HDMI-
TX0_HDMI+
TX0_HDMI-
R38 2.2K_4
R37 2.2K_4
SDVO_DATA
SDVO_CLK
R42 *4.7K_4
R41 4.7K_4
PC0
PC1
HDMI_HPD#
R40 499/F_4
REXT_HDMI
[11] HDMI_HPD#
[11] SDVO_DATA
[11] SDVO_CLK
R39 *100K/F_4
T7
The ESD protection is build-in in PS8101
SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB
+5V_HDMIC
RB500V-40 D15
+5V_HDMIC2
R45 2.2K_4
R333 2.2K_4
HDMI_SCL
HDMI_SDA
R334 33_4
R44 33_4
HDMI_C_SCL
HDMI_C_SDA
L23 *0_6S
L5 *0_6S
EC C01
C151 *10P/50V/COG_4
C463 *10P/50V/COG_4
HDMISCL
HDMISDA
D14 *TVSS5VESPT
EMI reserved
R54 0_4
RP4 *WCM-2012-900T
R50 0_4
R49 0_4
RP3 *WCM-2012-900T
R48 0_4
R47 0_4
RP1 *WCM-2012-900T
R46 0_4
RP2 WCM-2012-900T
TX2_HDMI+_OUT
TX2_HDMI-_OUT
TX1_HDMI+_OUT
TX1_HDMI-_OUT
TX0_HDMI+_OUT
TX0_HDMI-_OUT
TXC_HDMI+_OUT
TXC_HDMI-_OUT
HDMI PORT
CN15
SHELL1
D2+
D2 Shield
D2-
D1+
D1 Shield
D1-
D0+
D0 Shield
D0-
CK+
CK Shield
CK-
CE Remote
NC
DDC CLK
DDC DATA
GND
+5V
HP DET
SHELL2
SP@HDMI
F3 FUSE_1A/6V_POLY
+5V_HDMIC
HDMI_DET_C
C150 220P/50V/X7R_4
EC C01
L4 *0_6S
R43 100K/F_4
R335 4.7K_4
Q23 2N7002
PROJECT :MK2-Intel
Quanta Computer Inc.
Size Custom
Document Number <Doc>
CRT/HDMI CONN
Rev 1C
Date: Wednesday, June 23, 2010
Sheet 20 of 42

[12,19,20,24,28,31,32,34,35,38,39] 3VPCU
[3,4,11,12,13,14,15,17,18,19,20,22,23,25,26,27,29,30,31,32,33,35,36,38,39] +3V

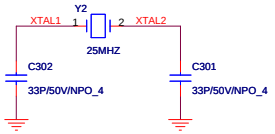
LANVCC



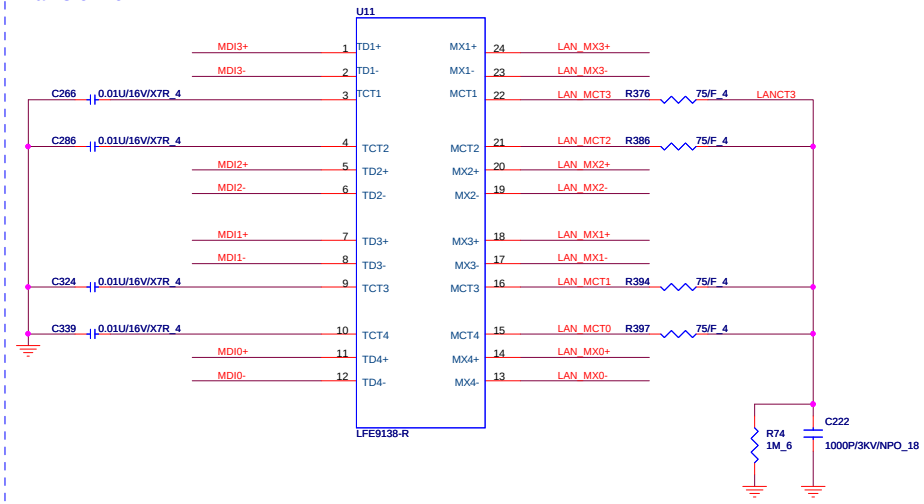
LANVCC
Trace width>60mil,
Trace length<200mil



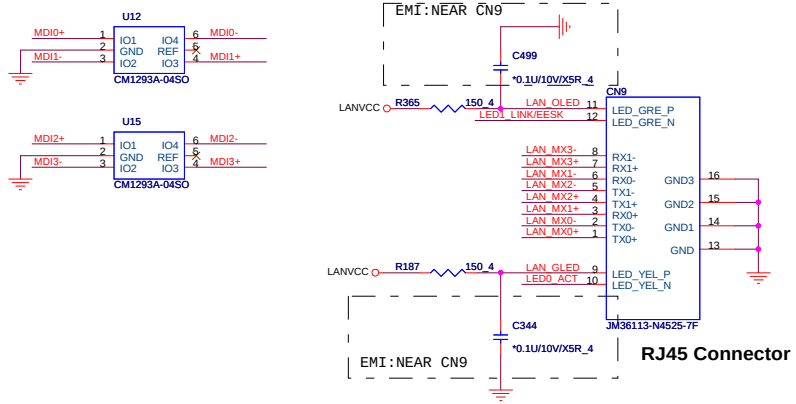
* C289,C293,C294,C296 are for U5006 VDD33 pins-- 1, 29, 37 and 40.



Tramsformer

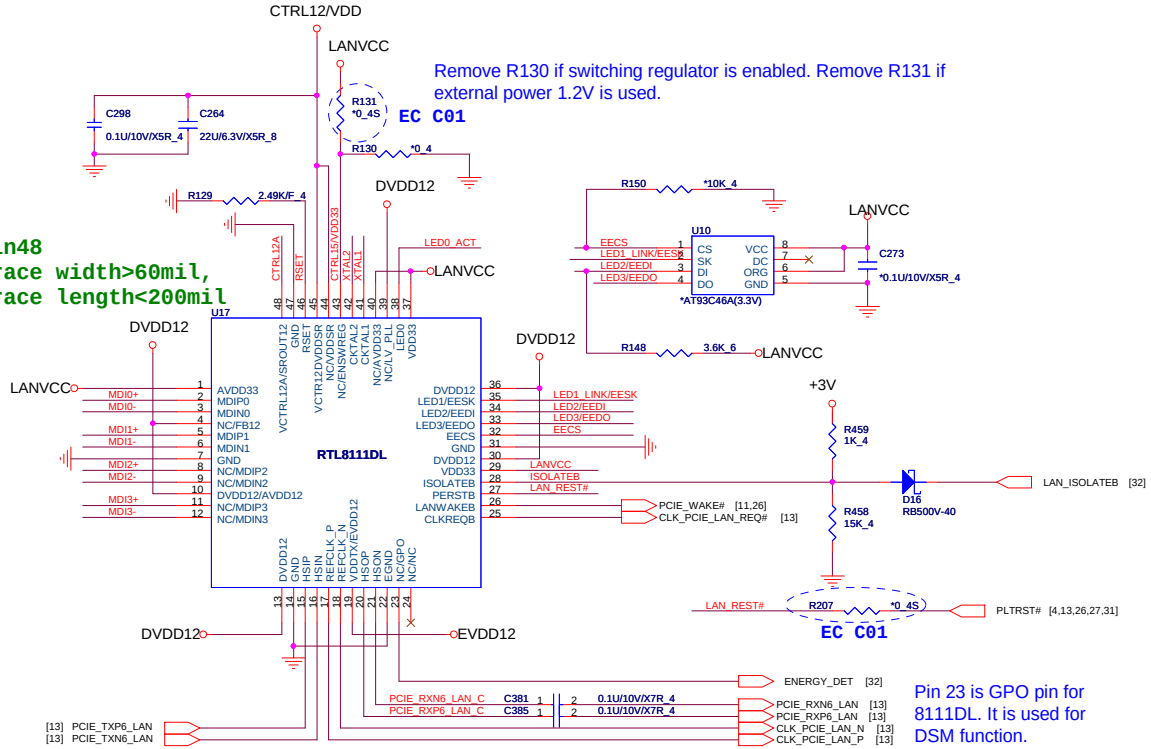


RJ45 Connector



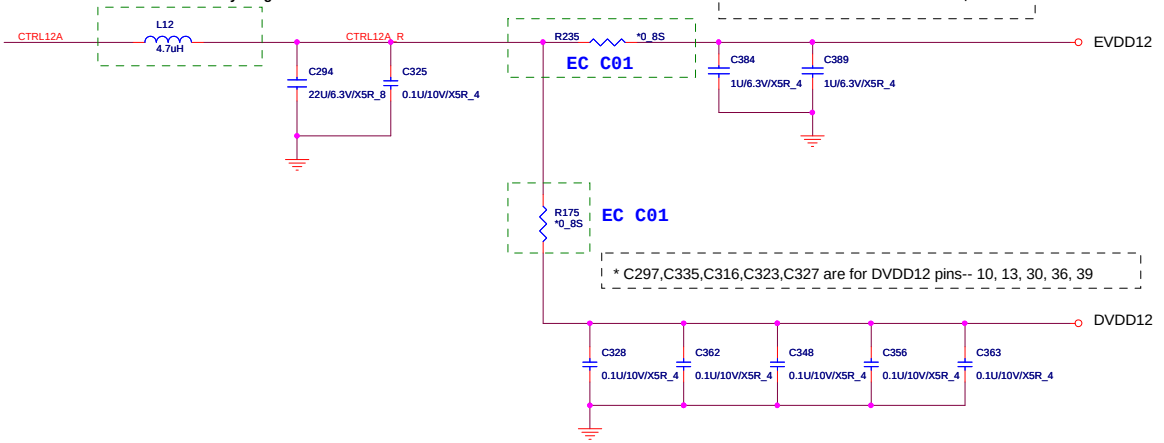
RJ45 Connector

Pin48 Trace width>60mil, Trace length<200mil



Pin 23 is GPO pin for 8111DL. It is used for DSM function.

Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.



PROJECT :MK2-Intel
Quanta Computer Inc.

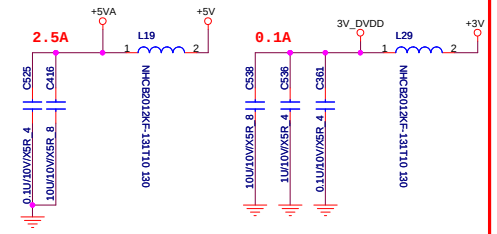
Size	Document Number	Rev
Custom	<Doc> LAN(RTL8111DL)	1C

Date: Wednesday, June 23, 2010 Sheet 21 of 42

Note:
To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 pins must be powered by a rail that is not removed unless AC power is removed.

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.



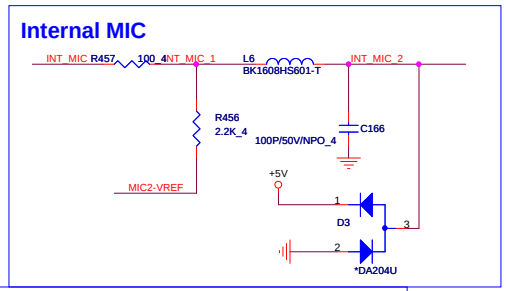
[3,4,11,12,13,14,15,17,18,19,20,21,23,25,26,27,29,30,31,32,33,35,36,38,39] +3V
[11,15,19,20,23,28,30,32,33,39] +5V

EC C01

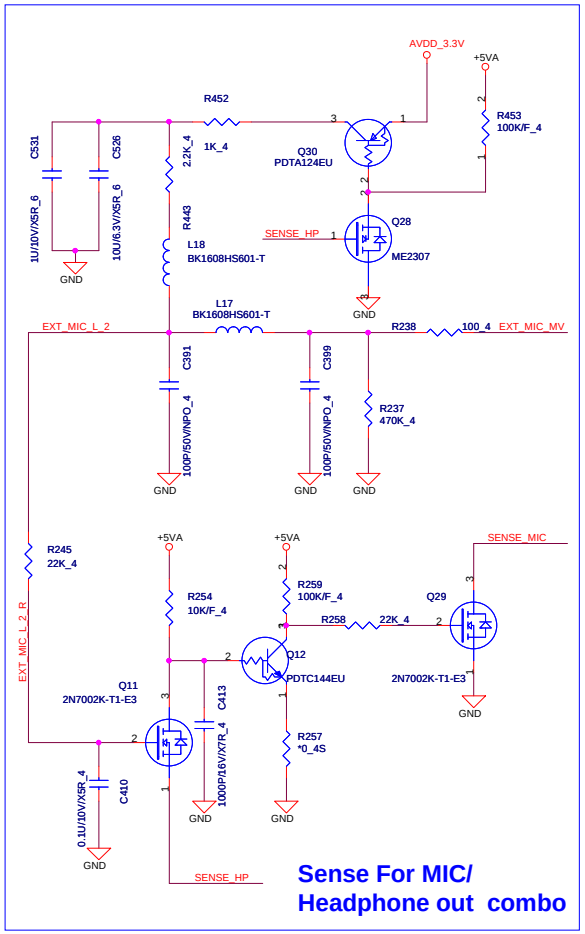
HD Audio Bus

DIGITAL_MIC

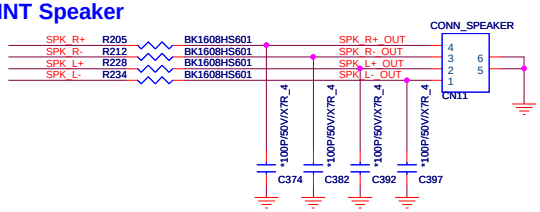
Internal MIC



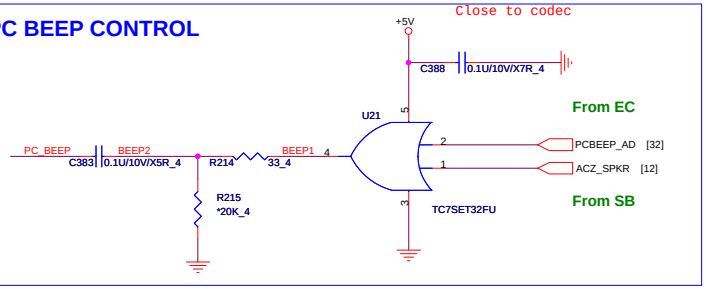
Sense For MIC/ Headphone out combo

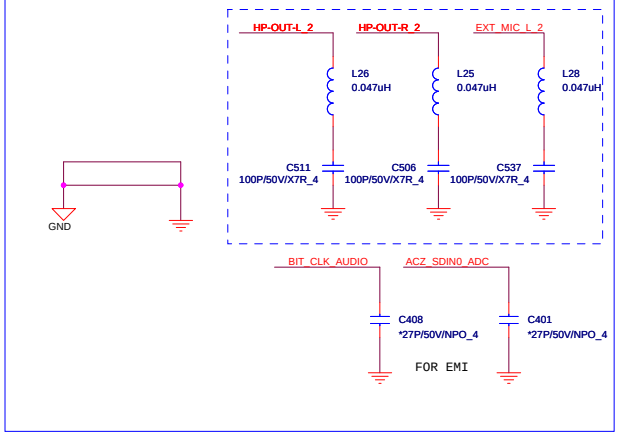


INT Speaker

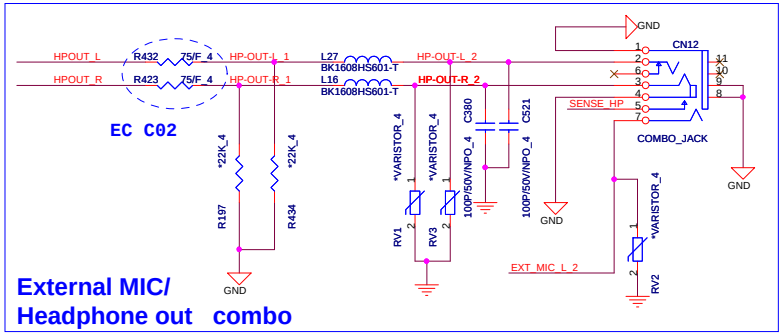


PC BEEP CONTROL





External MIC/ Headphone out combo



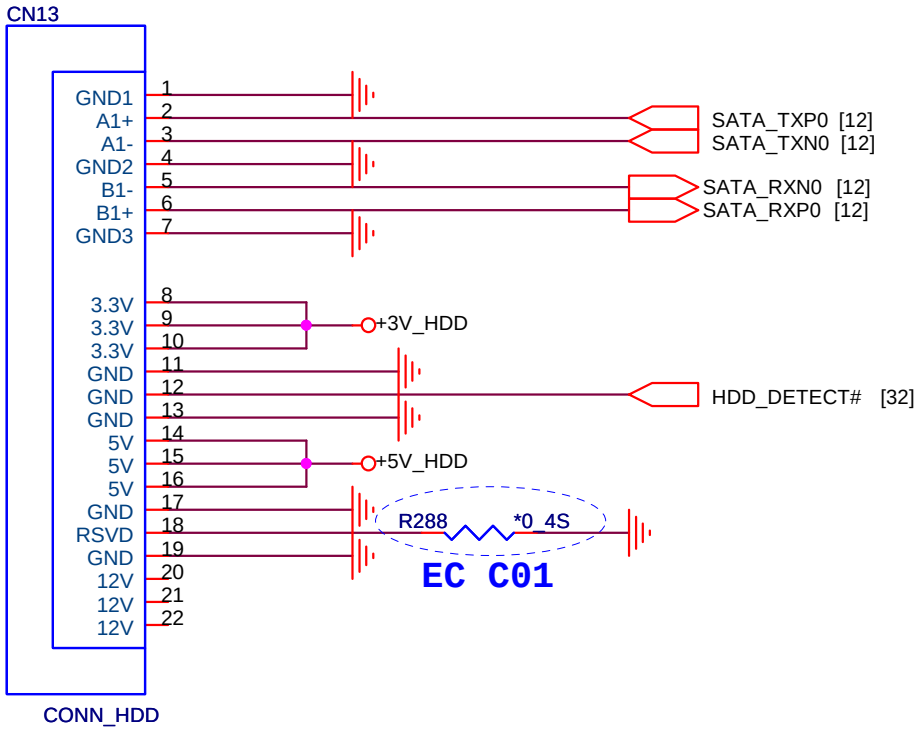
PROJECT :MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> AUDIO (CX20582, SPK)	1C

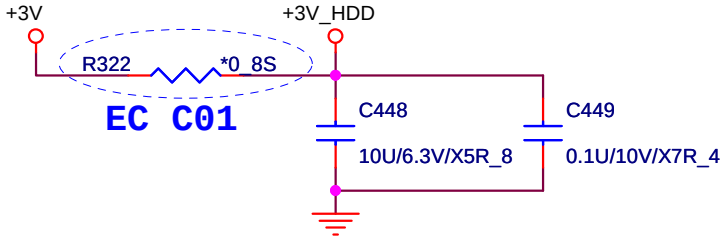
Date: Wednesday, June 23, 2010 Sheet 22 of 42

HDD

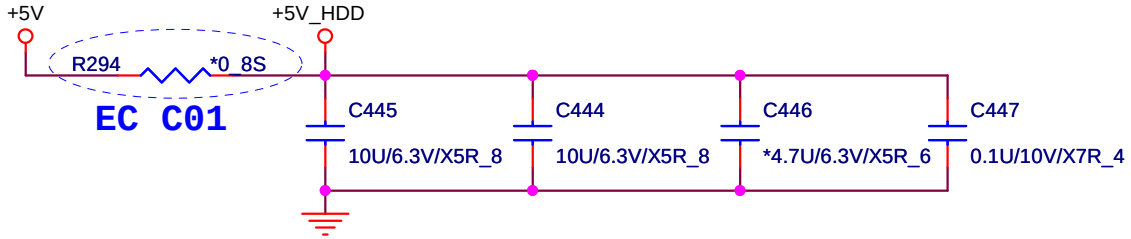
[11,15,19,20,22,28,30,32,33,39] +5V
[3,4,11,12,13,14,15,17,18,19,20,21,22,25,26,27,29,30,31,32,33,35,36,38,39] +3V



DC Current rating: 3 A (MAX)



DC Current rating: 2 A (MAX)



PROJECT :MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> SATA HDD	1C
Date: Wednesday, June 23, 2010	Sheet 23 of 42	

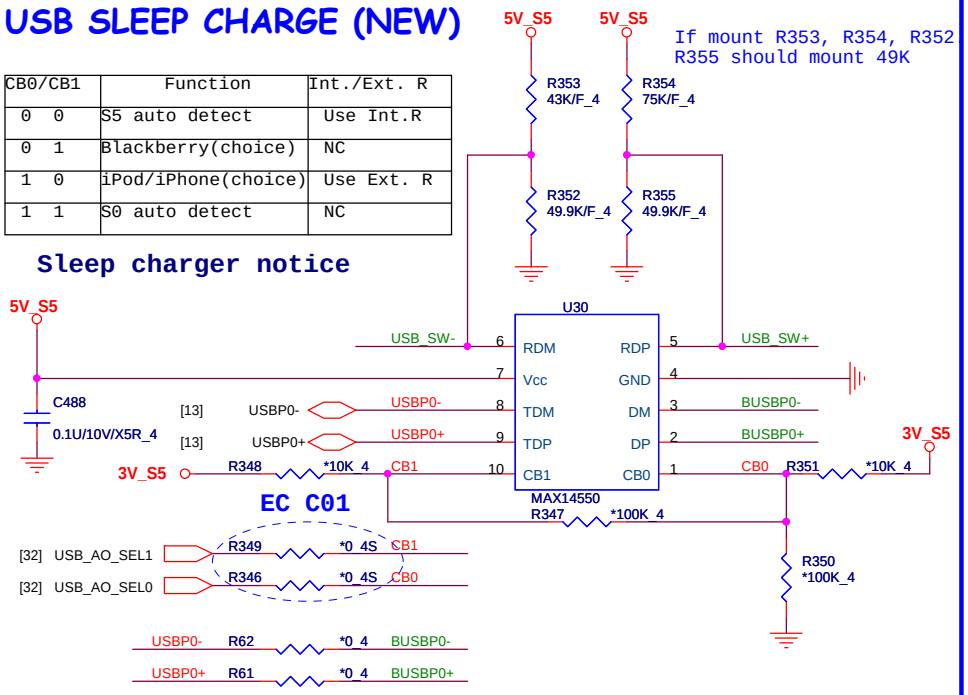
[15,39] 5V_S5
[4,11,12,13,14,15,26,29,31,37,39] 3V_S5
[12,19,20,21,28,31,32,34,35,38,39] 3VPCU

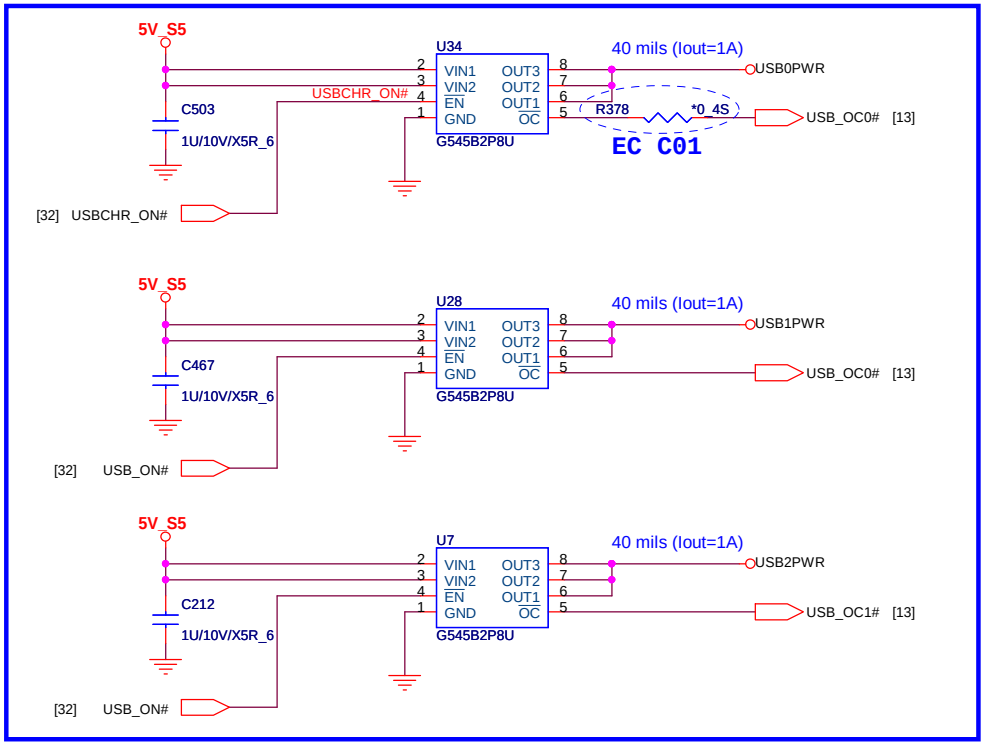
USB SLEEP CHARGE (NEW)

If mount R353, R354, R352
R355 should mount 49K

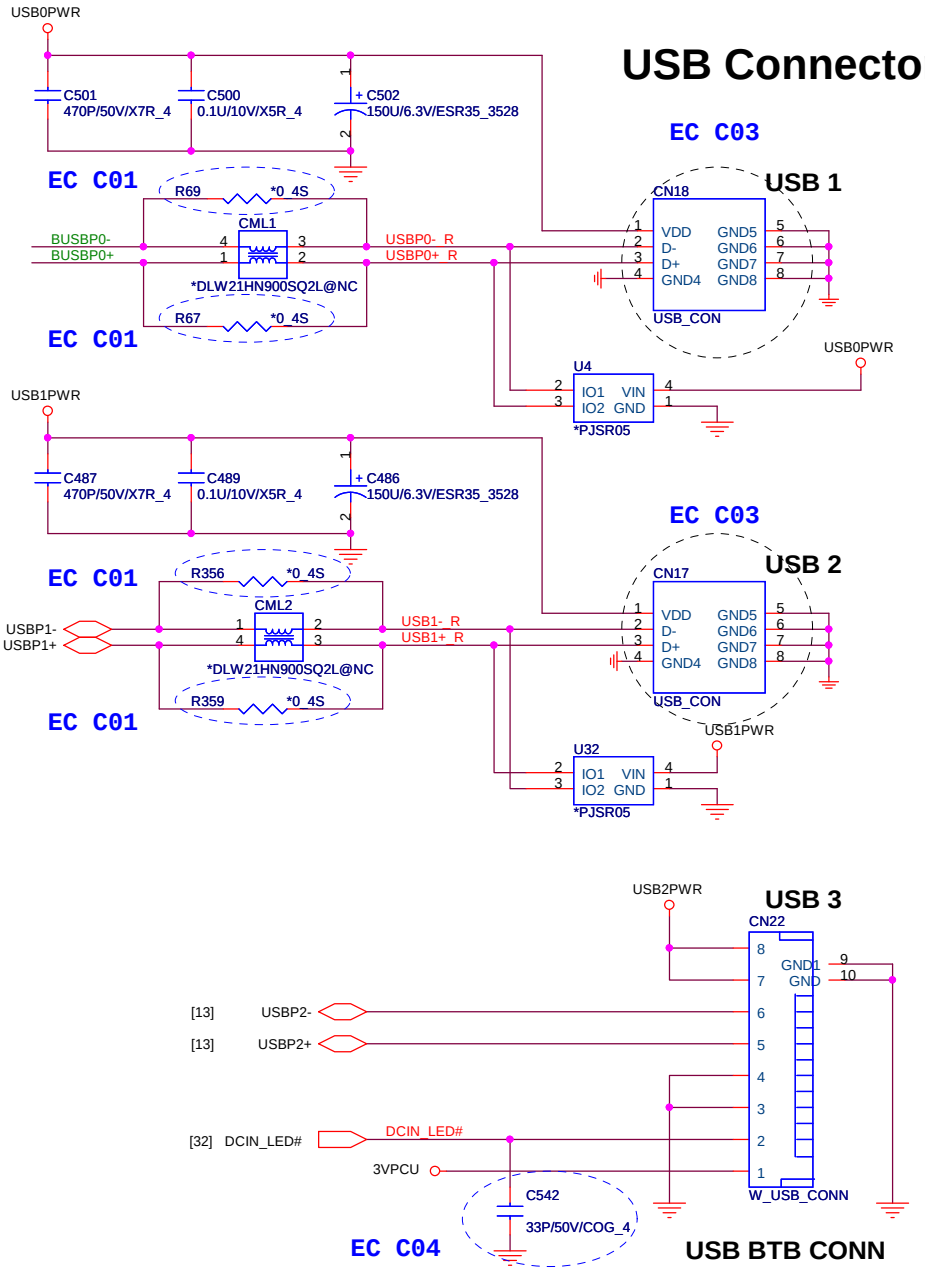
CB0/CB1	Function	Int./Ext. R
0 0	S5 auto detect	Use Int.R
0 1	Blackberry(choice)	NC
1 0	iPod/iPhone(choice)	Use Ext. R
1 1	S0 auto detect	NC

Sleep charger notice





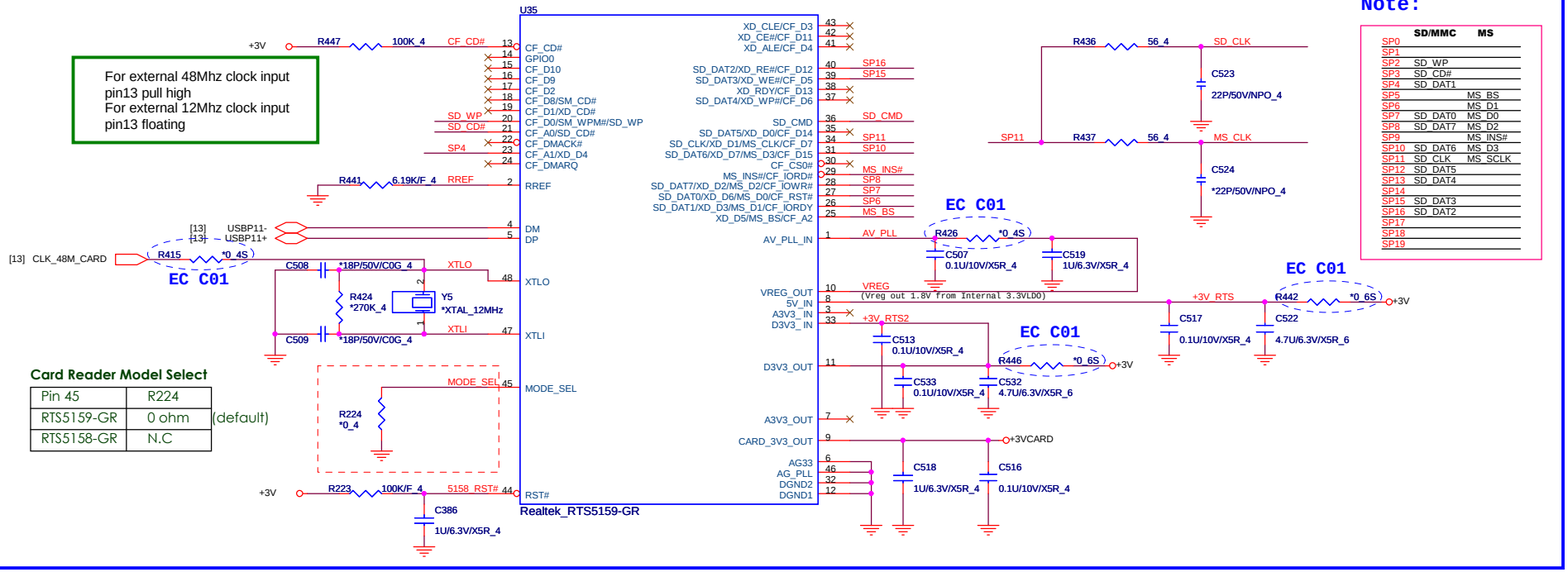
USB Connector



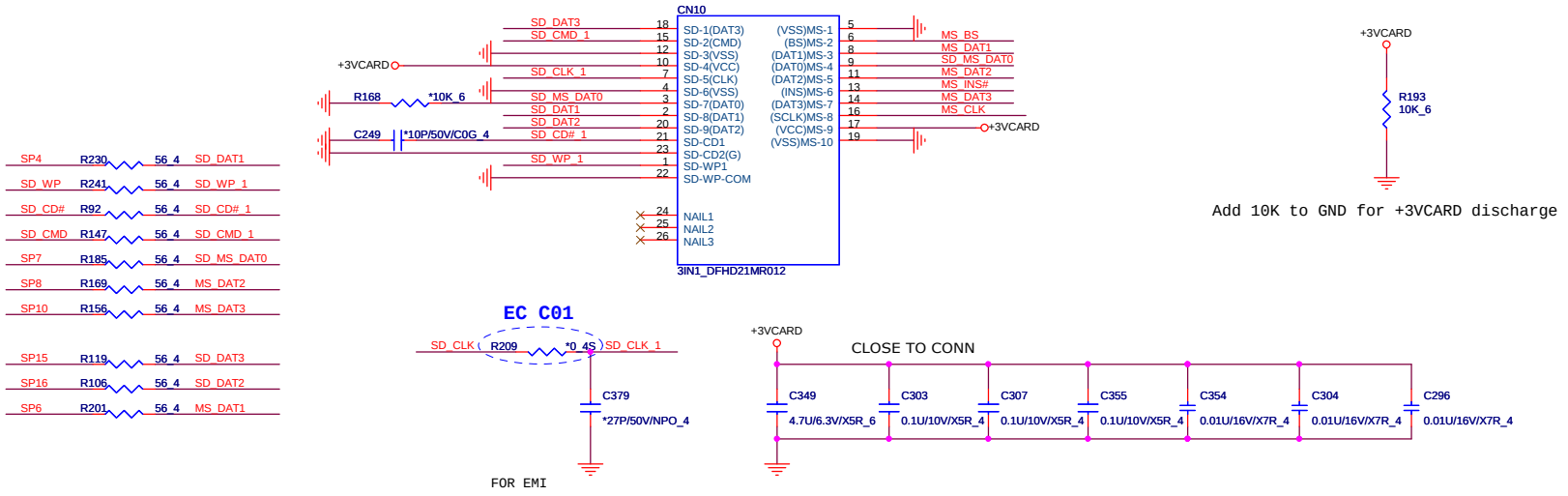
PROJECT :MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc>	1C
	USB x 3	
Date: Wednesday, June 23, 2010	Sheet 24 of 42	

RTS5159



3 IN 1 CARD READER



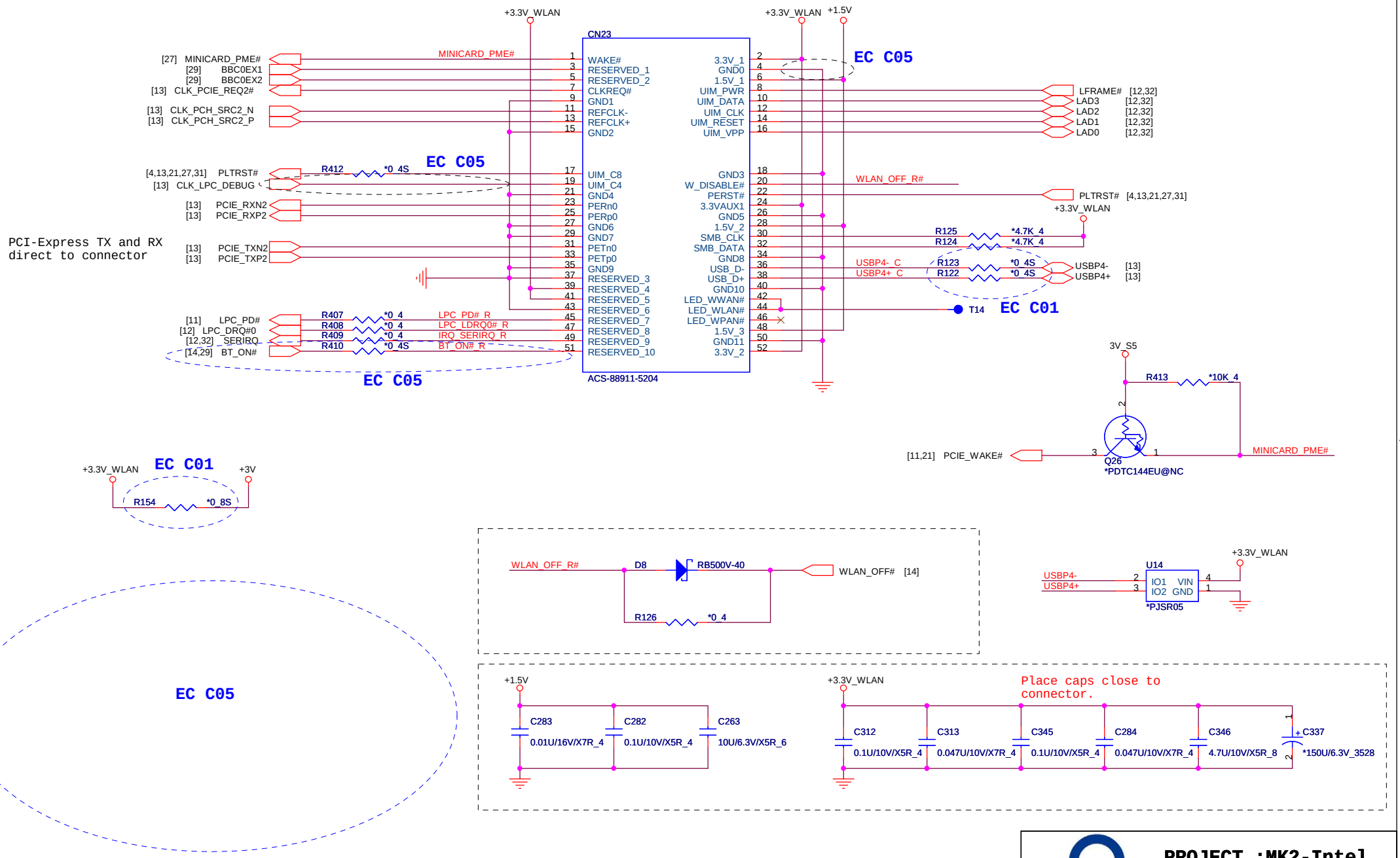
PROJECT :MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Card Reader-RTS5159	1C

Date: Wednesday, June 23, 2010 Sheet 25 of 42

MiniCard WLAN connector

[4,11,12,13,14,15,24,29,31,37,39] 3V_S5
[3,4,11,12,13,14,15,17,18,19,20,21,22,23,25,27,29,30,31,32,33,35,36,38,39] +3V
[27,37] +1.5V

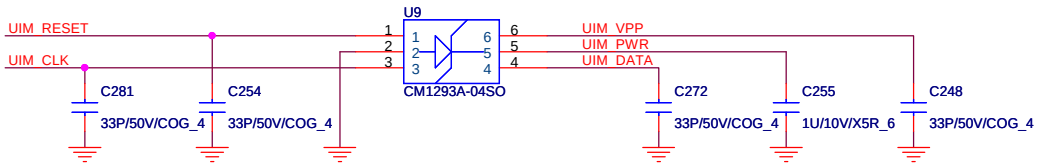


PROJECT :MK2-Intel
Quanta Computer Inc.

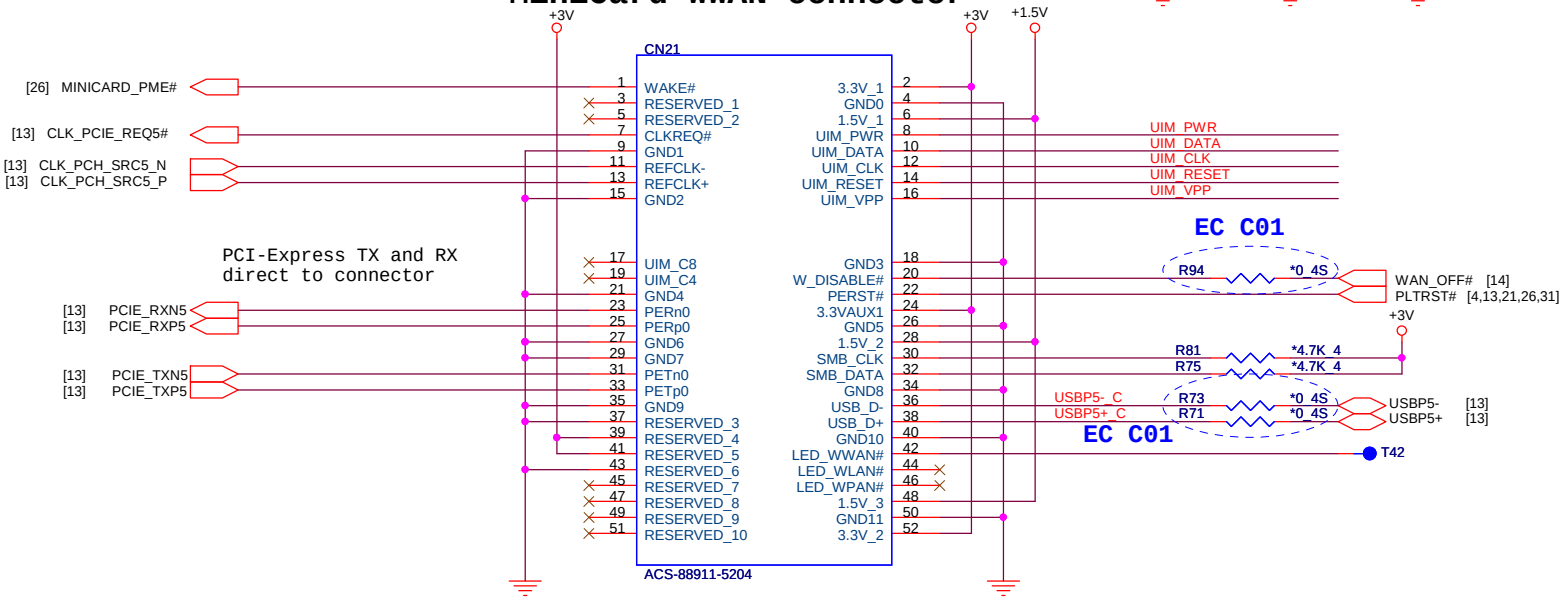
Size	Document Number	Rev
Custom	<Doc>	1C
	WLAN	
Date: Wednesday, June 23, 2010	Sheet 26 of 42	

[3,4,11,12,13,14,15,17,18,19,20,21,22,23,25,26,29,30,31,32,33,35,36,38,39] +3V
[26,37] +1.5V

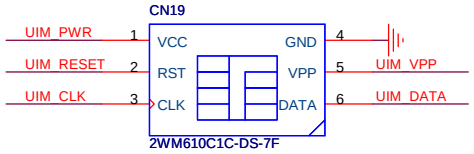
Layout Note:
UIM_RESET,UIM_CLK,UIM_DATA routting as short as possible

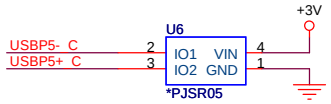


MiniCard WWAN connector

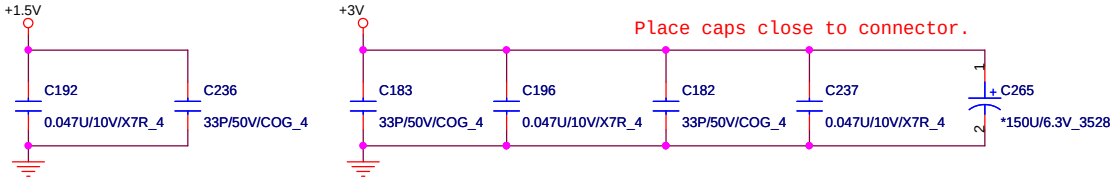


SIM Card CONN





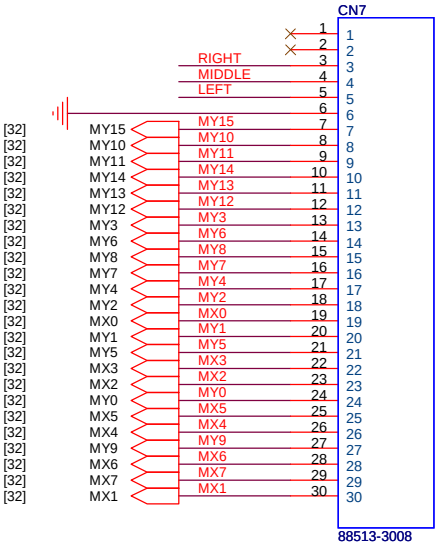
Place caps close to connector.

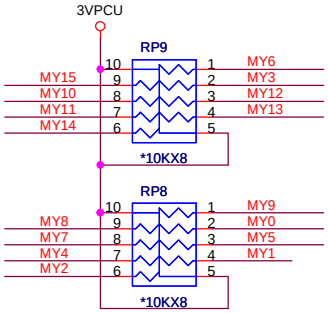


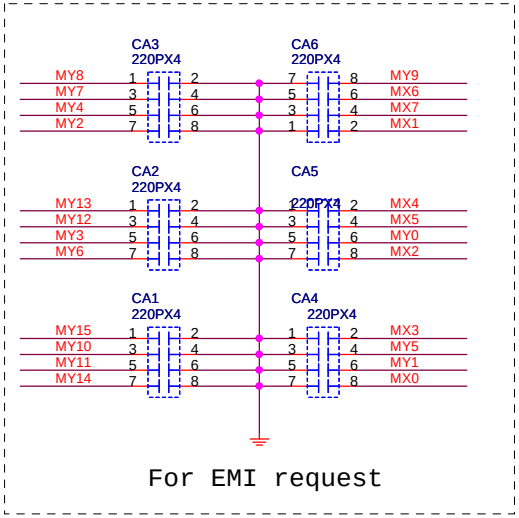
PROJECT :MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> WWAN	1C
Date: Wednesday, June 23, 2010	Sheet 27 of 42	

KEYBOARD

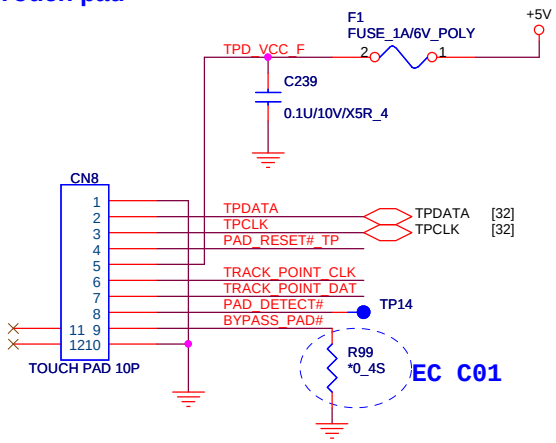


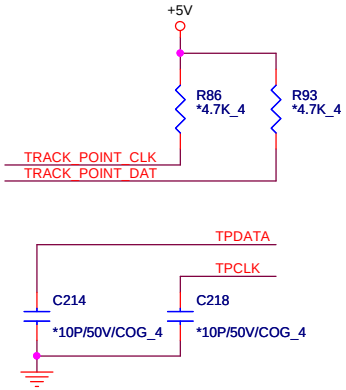


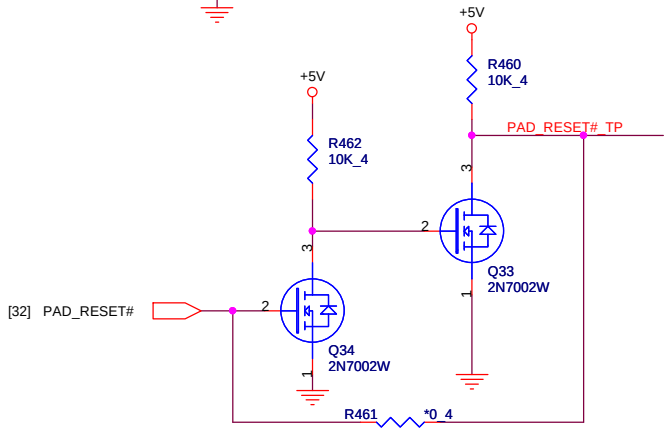


[11,15,19,20,22,23,30,32,33,39] +5V
[12,19,20,21,24,31,32,34,35,38,39] 3VPCU

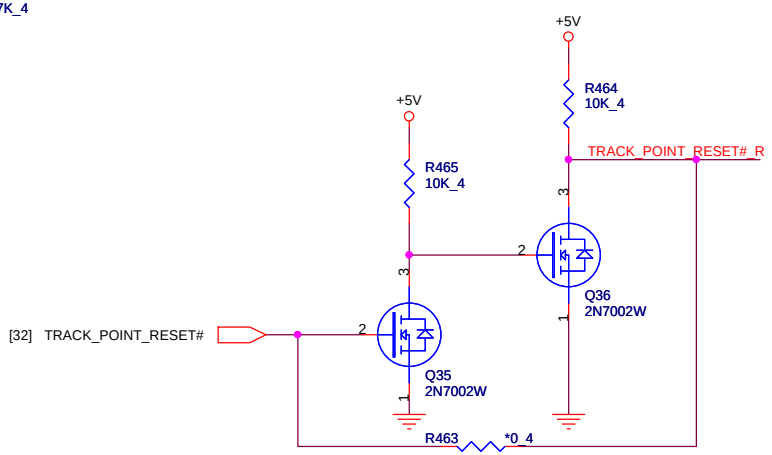
Touch pad

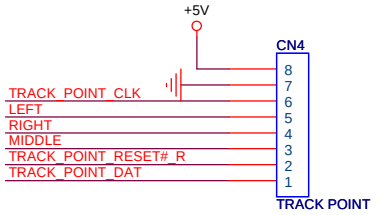


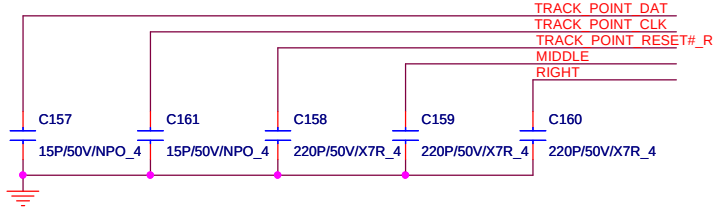




TRACK POINT





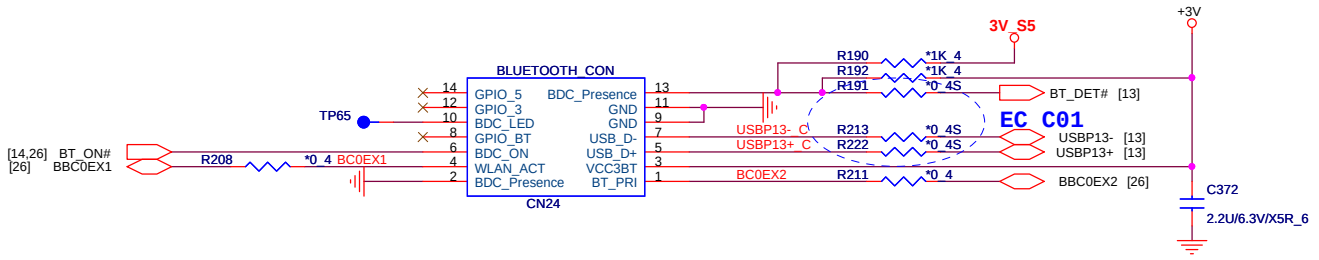


PROJECT :MK2-Intel
Quanta Computer Inc.

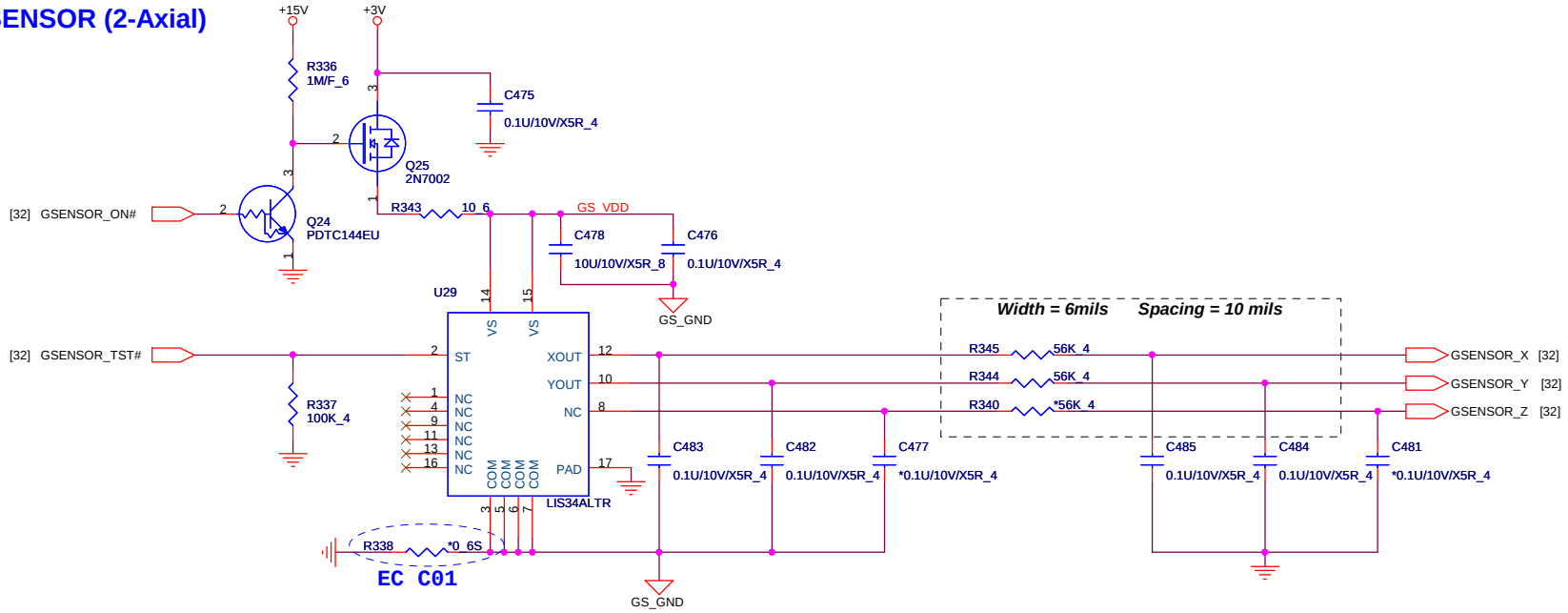
Size	Document Number	Rev
Custom	<Doc> KB/TP	1C
Date: Wednesday, June 23, 2010	Sheet 28 of 42	

[3,4,11,12,13,14,15,17,18,19,20,21,22,23,25,26,27,30,31,32,33,35,36,38,39] +3V
[19,35,37,39] +15V
[4,11,12,13,14,15,24,26,31,37,39] 3V_S5

BLUETOOTH



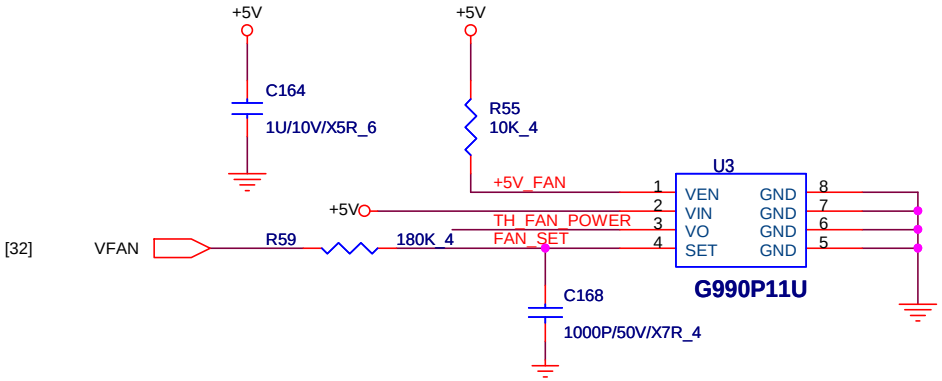
G-SENSOR (2-Axial)

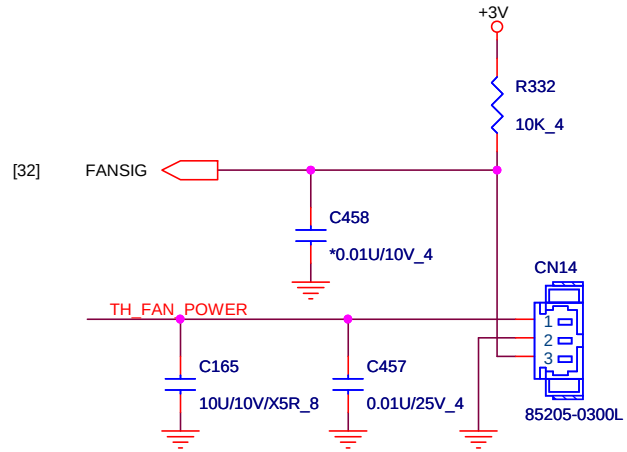


PROJECT :MK2-Intel
Quanta Computer Inc.

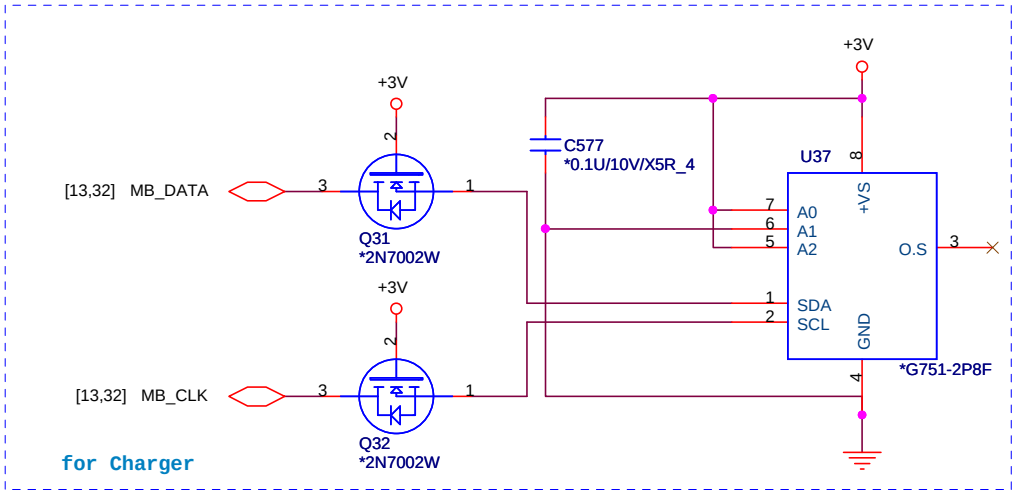
Size	Document Number	Rev
Custom	<Doc> BT/G-SENSOR	1C
Date: Wednesday, June 23, 2010	Sheet 29 of 42	

FANPWR = 1.6*VSET





EC C06



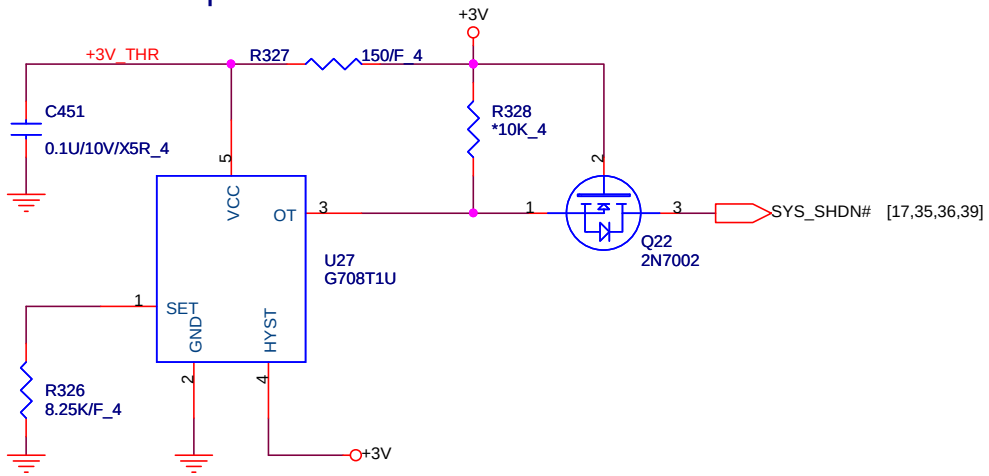
ADDRESS: 9AH

ADDRESS

1	0	0	1	A2	A1	A0	0

MSB LSB

CPU thermal protection



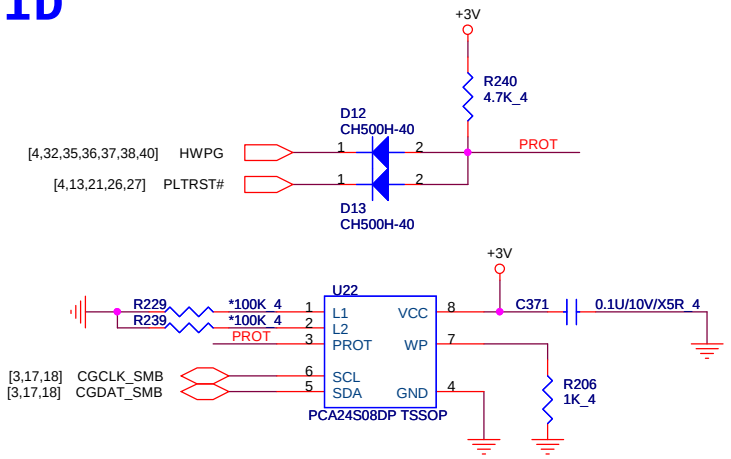
Size: Custom	Document Number: <Doc>
Rev: 1C	
Date: Wednesday, June 23, 2010	Sheet 30 of 42

PROJECT :MK2-Intel
Quanta Computer Inc.

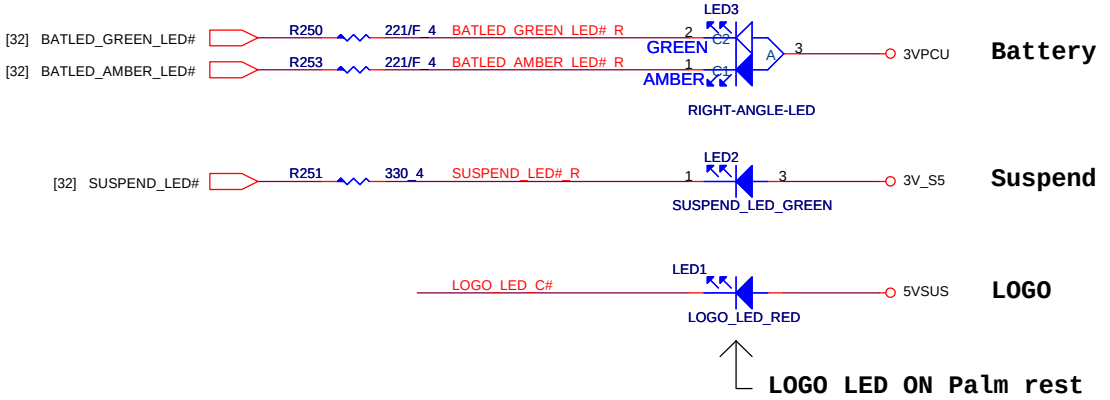
FAN/Thermal

[3,4,11,12,13,14,15,17,18,19,20,21,22,23,25,26,27,29,30,32,33,35,36,38,39] +3V
[4,11,12,13,14,15,24,26,29,37,39] 3V_S5
[12,19,20,21,24,28,32,34,35,38,39] 3VPCU
[19,39] 5VSUS

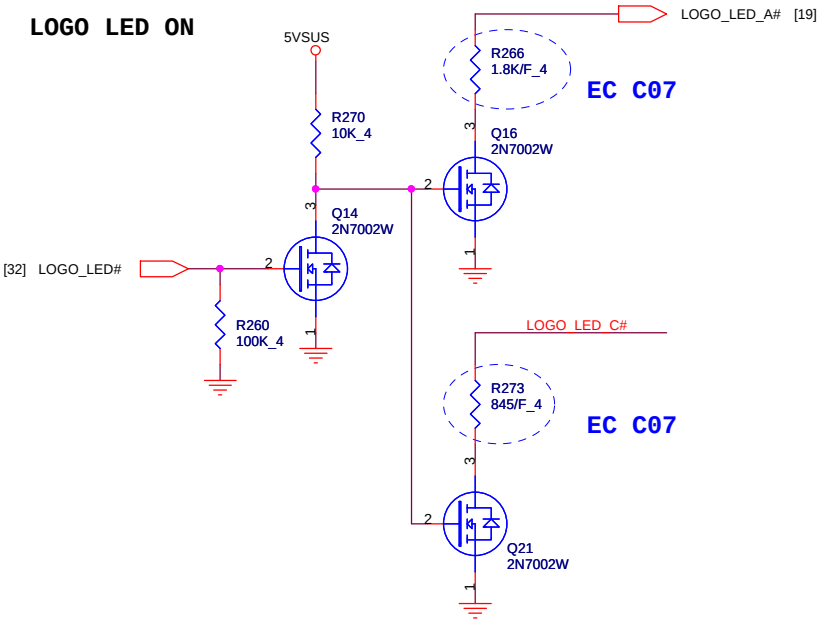
RFID



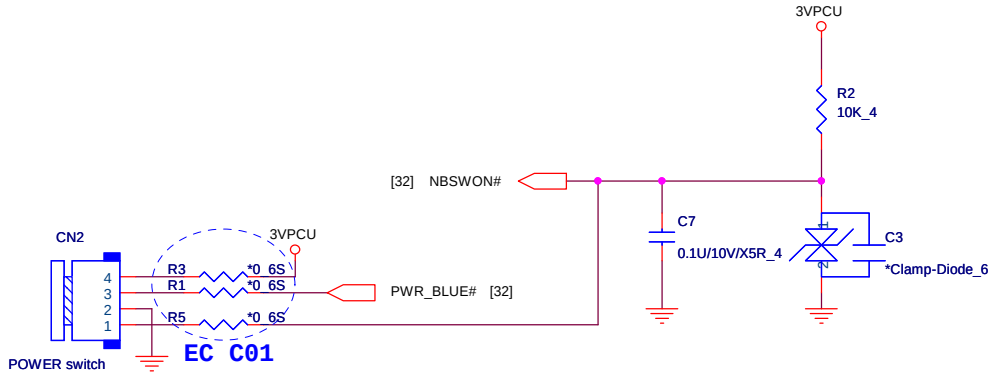
LED



LOGO LED on panel cover



POWER BUTTON



PROJECT :MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> SW/LED/RFID_EEPROM	1C
Date: Wednesday, June 23, 2010	Sheet 31 of 42	

IT8512E

(For PLL Power)

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

TMKBC Function	
High	Enable
Low	Disable

R609	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

Close to EC

4Mbit (512K Byte), SPI
FLASH_512KB_MX25L4005CM2I-12G

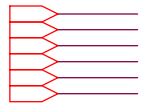
EC C01
EC C10

PROJECT : MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBC IT8502E	1C

Date: Wednesday, June 23, 2010 Sheet 32 of 42

[3,4,11,12,13,14,15,17,18,19,20,21,22,23,25,26,27,29,30,31,32,35,36,38,39] +3V
[4,7,17,18,37,39] 1.5VSUS
[11,15,19,20,22,23,28,30,32,39] +5V
[34,39] VA
[34] VBATT
[19,34,35,36,37,38,39,40] VIN



Hole for CPU support

HOLE4 *H-C142D142N
HOLE6 *h-tc142B236d142pb
HOLE3 *H-C142D142N
HOLE7 *H-C142D142N

Hole for PCH

HOLE18 *H-C197D102P2
HOLE21 *H-C197D102P2

HOLE1 *H-C197D91P2
HOLE8 *H-C47D47N
HOLE5 H-C256D130P2

Hole for WLAN

HOLE17 h-c197d35p2
HOLE16 h-c197d102p2

Hole for WWAN

HOLE19 h-c197d102p2

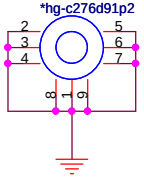
EC C08

Hole for BT

HOLE20 h-tc217bc59i99d59pt

HOLE9 *h-c295d91p2
HOLE10 *o-mk-note-1
HOLE13 *H-O102X91D102X91N
HOLE11 *h-c197d91p2

HOLE12 *hg-c276d91p2



HOLE14 *h-tc236bc276d91p2
GND

HOLE15 *h-c236i131d91p2
HOLE2 *O-FL6-X
HOLE22 *SPAD-RE230X585NP

EMI

1.5VSUS
C459 2200P/50V/X7R_4
C461 2200P/50V/X7R_4
C465 2200P/50V/X7R_4
C466 2200P/50V/X7R_4
C462 2200P/50V/X7R_4
C460 2200P/50V/X7R_4

+3V
C1 2200P/50V/X7R_4
C145 2200P/50V/X7R_4
C498 2200P/50V/X7R_4
C11 2200P/50V/X7R_4
C390 2200P/50V/X7R_4
C358 2200P/50V/X7R_4
C403 2200P/50V/X7R_4
C235 2200P/50V/X7R_4

+5V
C148 2200P/50V/X7R_4
C210 2200P/50V/X7R_4
C412 2200P/50V/X7R_4
C398 2200P/50V/X7R_4
C534 2200P/50V/X7R_4

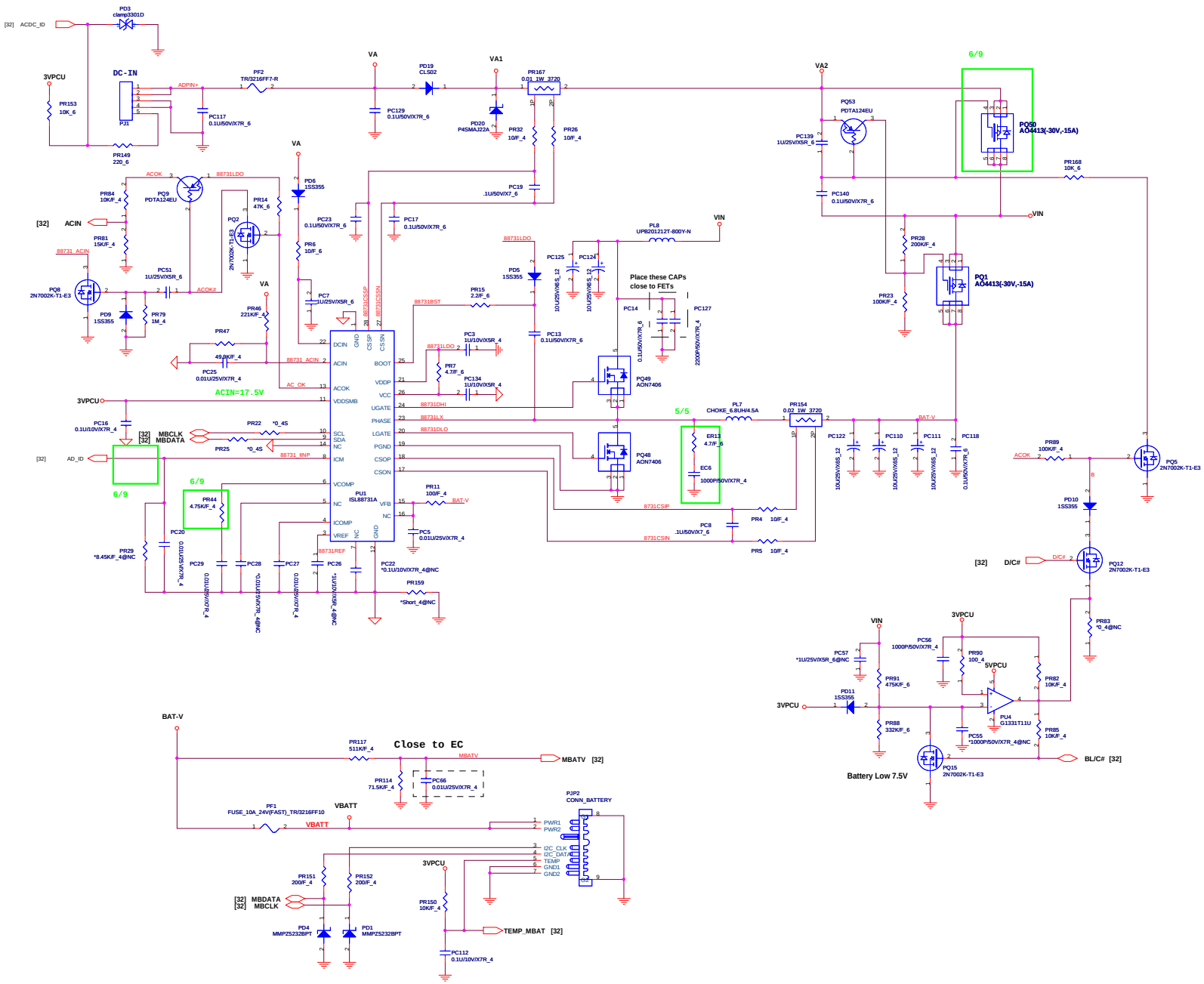
VA
C430 *4.7U/25V/X5R_8
C443 *4.7U/25V/X5R_8

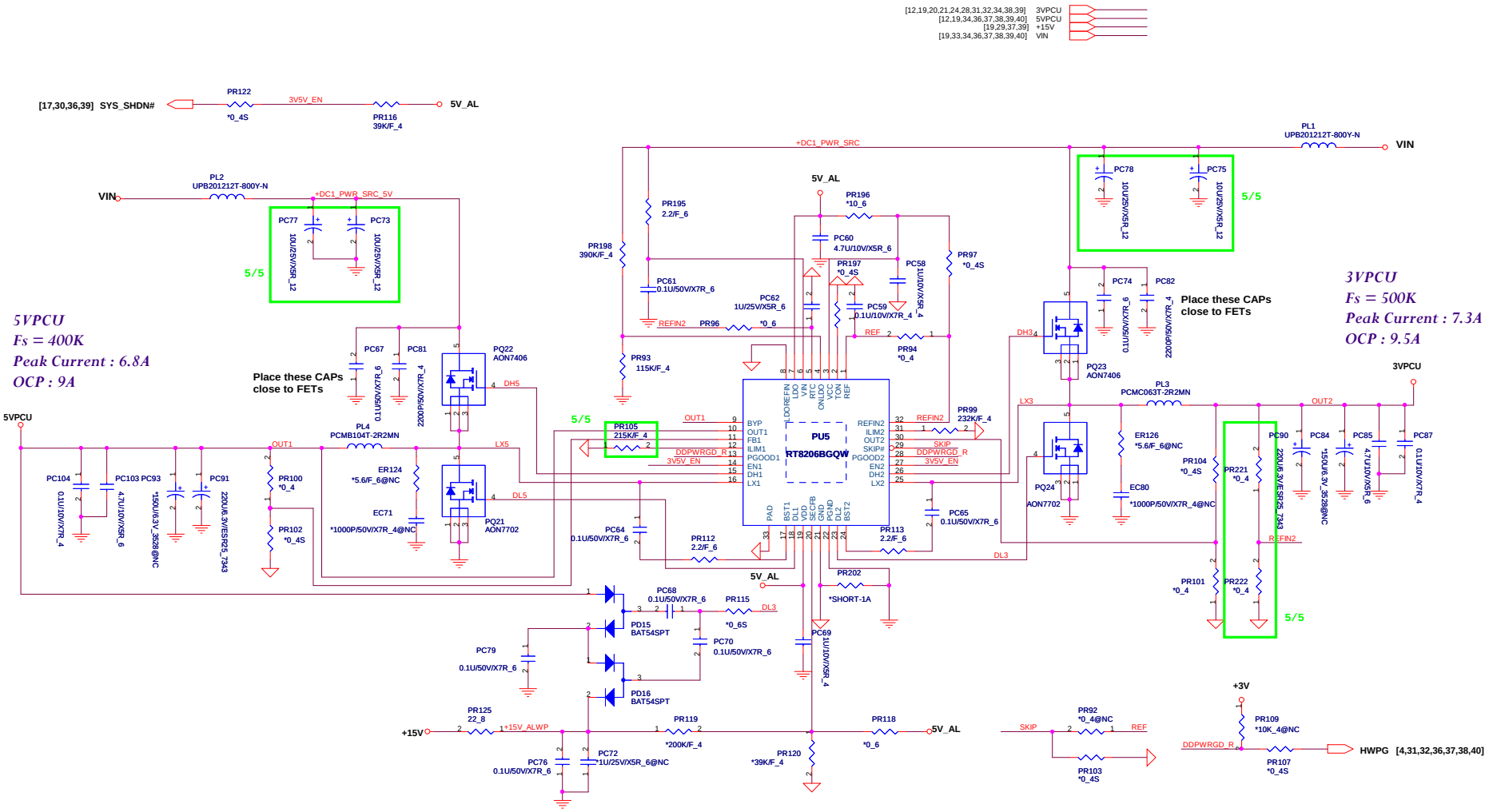
VIN
C454 *0.1U/25V/X5R_4
C184 *0.1U/25V/X5R_4
C464 *0.1U/25V/X5R_4

VBATT
C2 *0.1U/25V/X5R_4

PROJECT :MK2-Intel
Quanta Computer Inc.

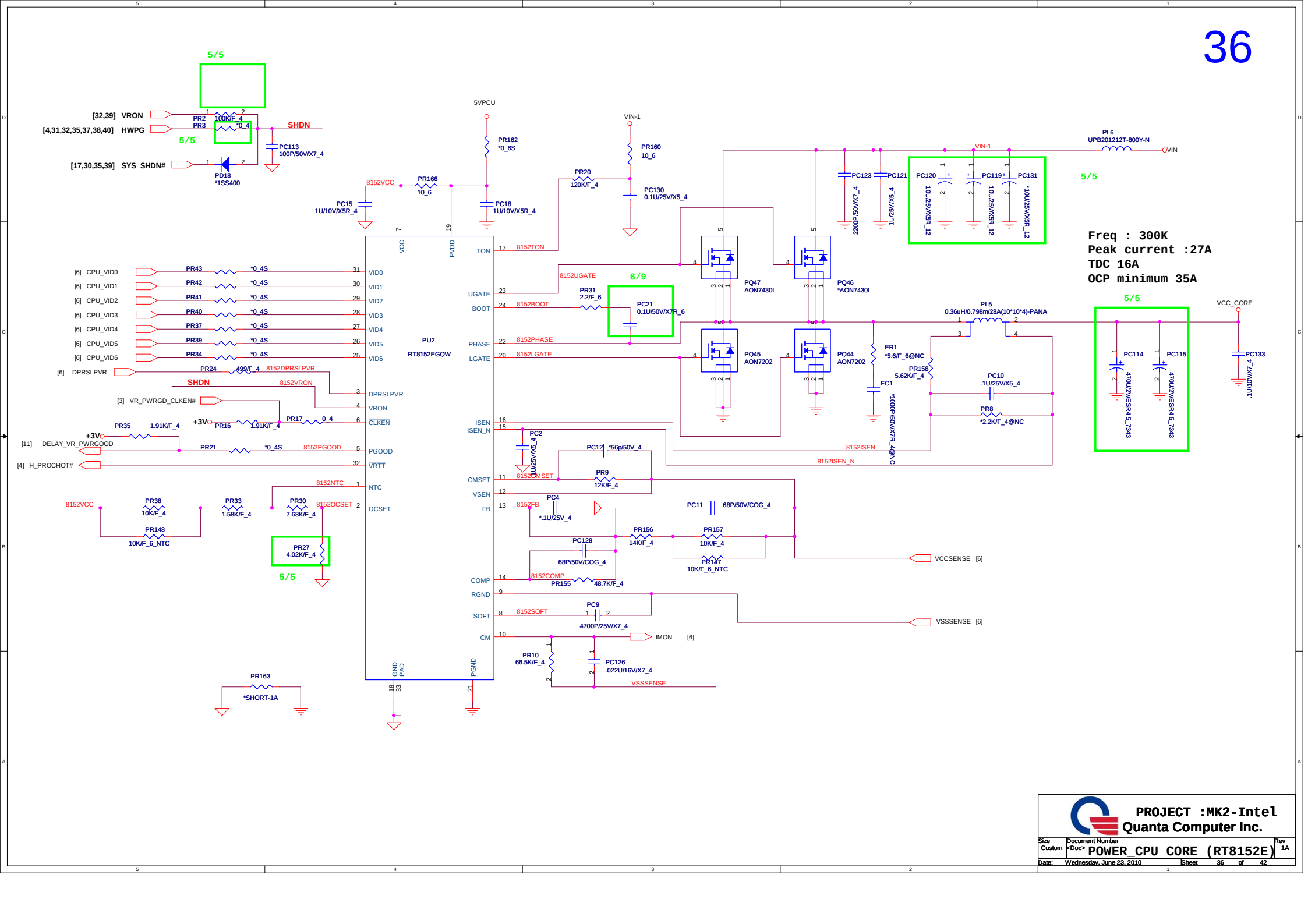
Size	Document Number	Rev
Custom	<Doc> Screw Hole/EMI	1C
Date: Wednesday, June 23, 2010	Sheet 33 of 42	


DC-IN
ACIN=17.5V
Place these CAPs close to FETs
Close to EC
Battery Low 7.5V
PROJECT :MK2-Intel
Quanta Computer Inc.
POWER_Charger (ISL88731A)
Wednesday, June 23, 2010
Sheet 34 of 42

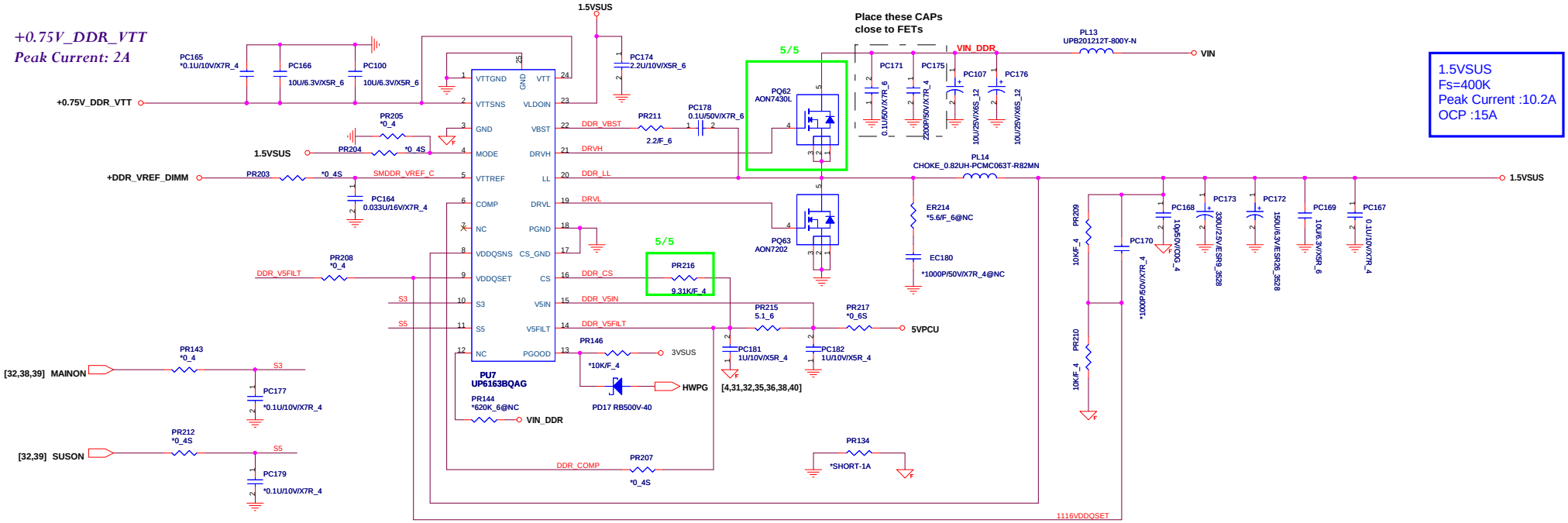


PROJECT :MK2-Intel
Quanta Computer Inc.

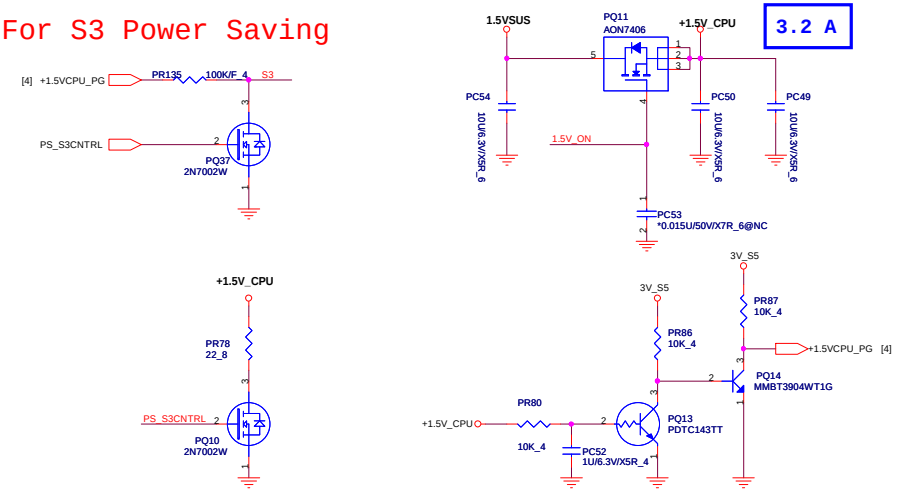
Size	Document Number	Rev
Custom	<Doc> POWER_3V/5V (RT8206BGQW)	1A
Date: Wednesday, June 23, 2010	Sheet 35 of 42	

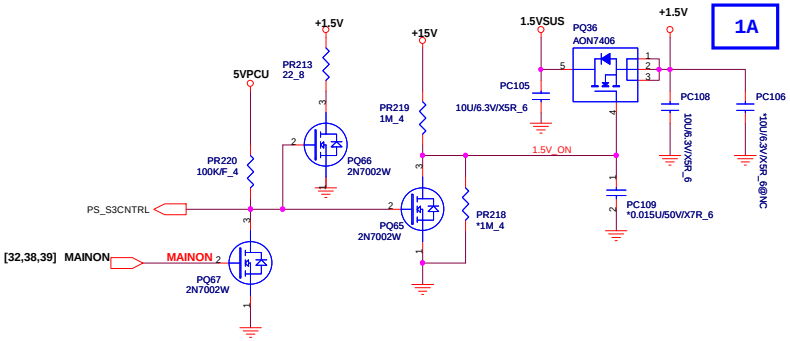


Quanta Computer Inc.	PROJECT :MK2-Intel		
Size: Custom	Document Number: <Doc> POWER_CPU CORE (RT8152E)		Rev: 1A
Date: Wednesday, June 23, 2010	Sheet 36 of 42		



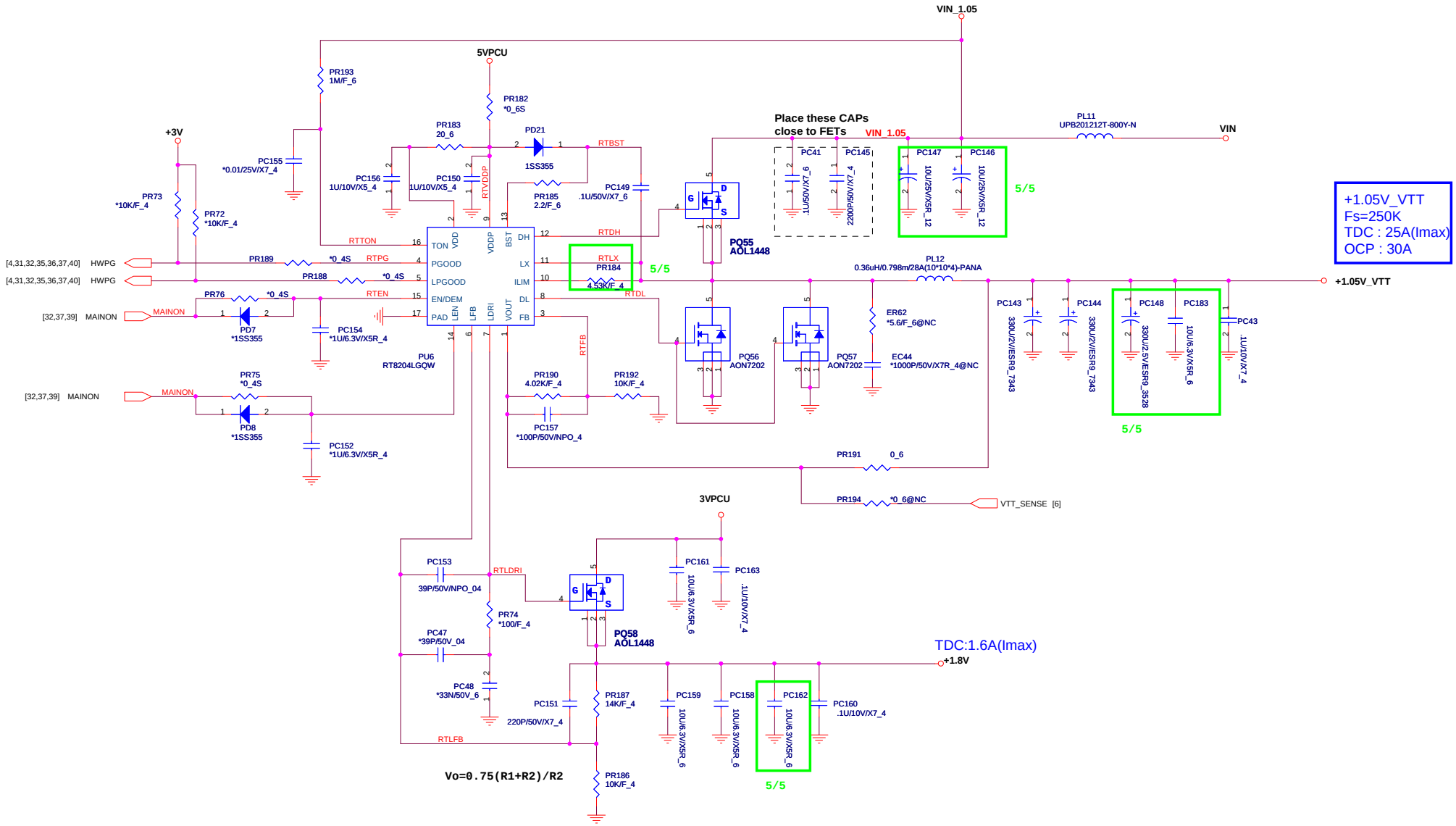
For S3 Power Saving





PROJECT :MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> POWER_DDR3 (UP6163BQAG)	1A
Date: Wednesday, June 23, 2010	Sheet 37 of 42	

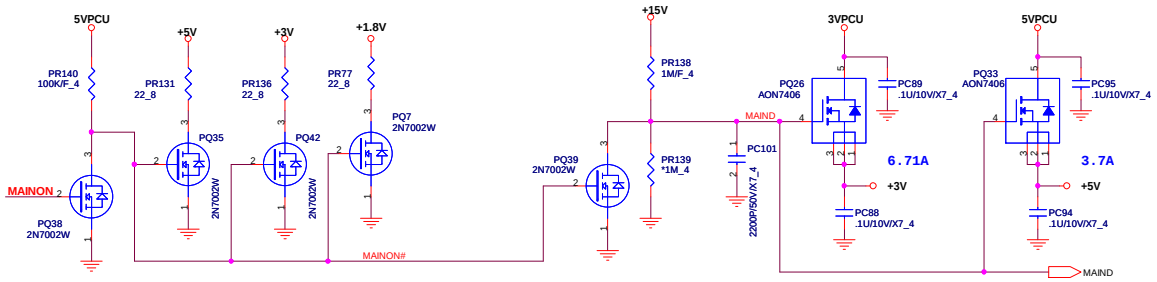


PROJECT :MK2-Intel
Quanta Computer Inc.

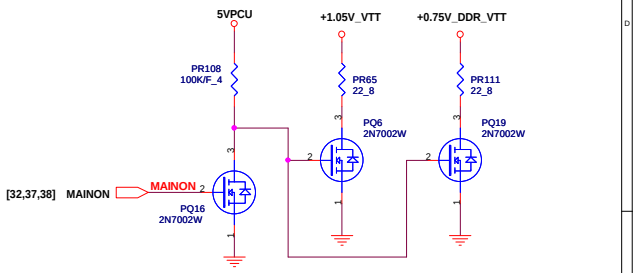
Size	Document Number	Rev
Custom	<Doc> POWER_1.05V&1.8V(RT8204L)	1A

Date: Wednesday, June 23, 2010 Sheet 38 of 42

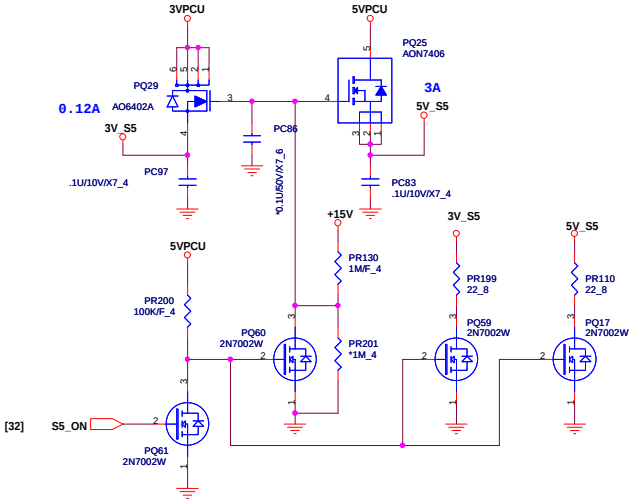
+3V, +5V



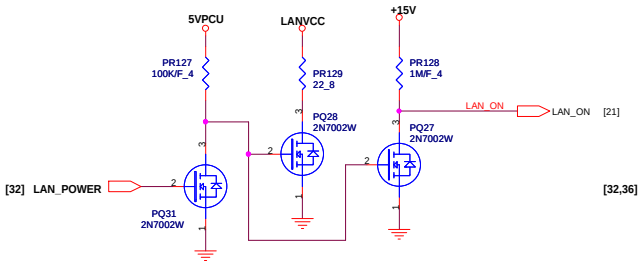
+1.05V, SMDDR_VTERM



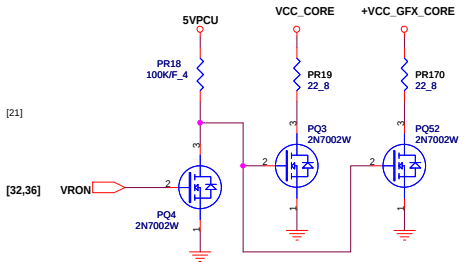
3V_S5, 5V_S5

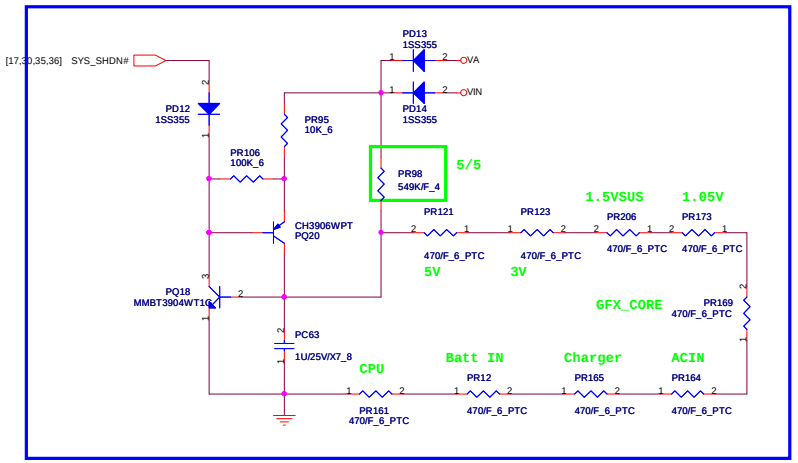


LANVCC

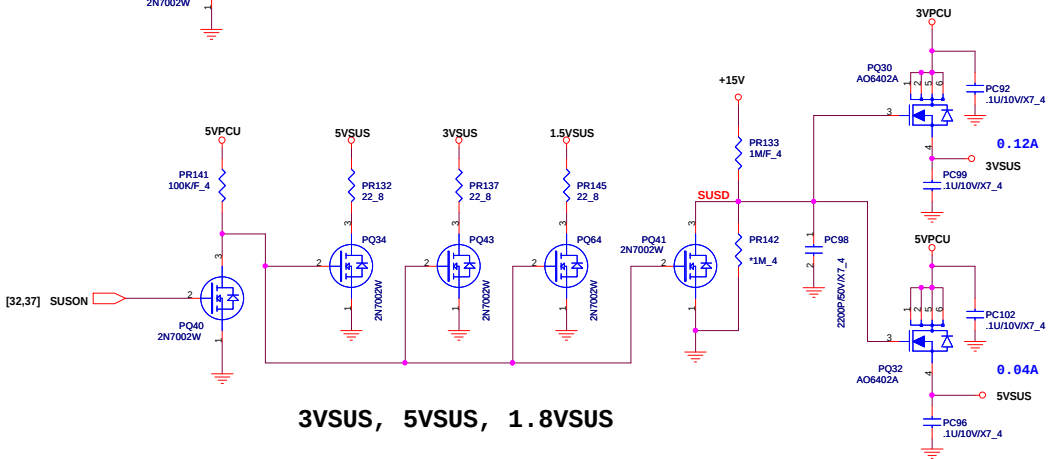


VCC_CORE



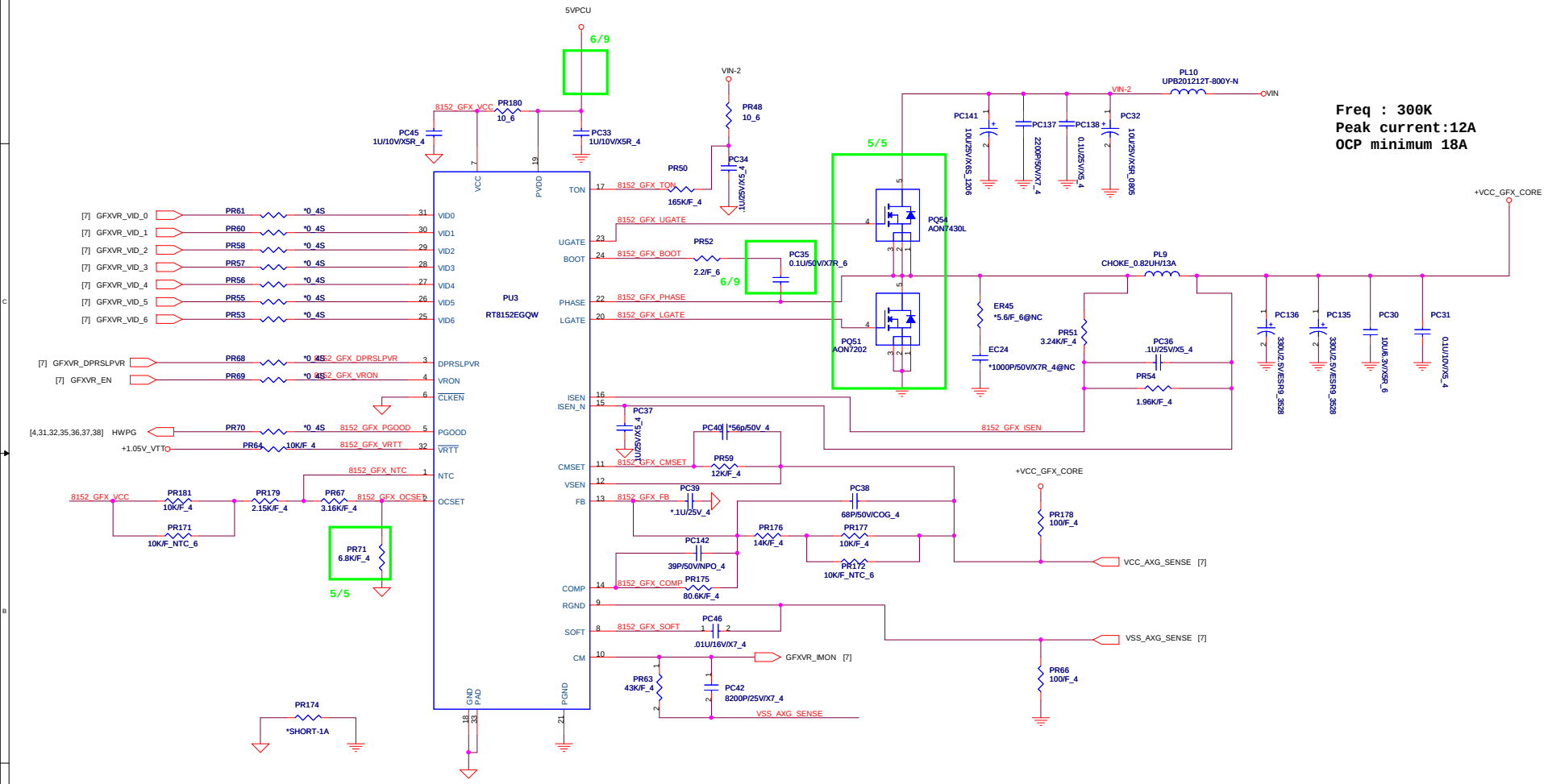


3VSUS, 5VSUS, 1.8VSUS



PROJECT :MK2-Intel
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc>	1A
	POWER_Discharge	
Date: Wednesday, June 23, 2010	Sheet 39 of 42	



Freq : 300K
Peak current:12A
OCP minimum 18A

PROJECT :MK2-Intel Quanta Computer Inc.			
Size: Custom	Document Number: <Doc> +VCC_GFX_CORE (RT8152E)		Rev: 1A
Date: Wednesday, June 23, 2010		Sheet 40 of 42	