E540

NM-A161 Rev1.0 Schematic

Intel Haswell Processor with DDRIII + Lynx point PCH
nVIDIA N14P-GV2/ N14M-GL

2013-07-11 Rev 1.0

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Title: Cover Page

LCFC

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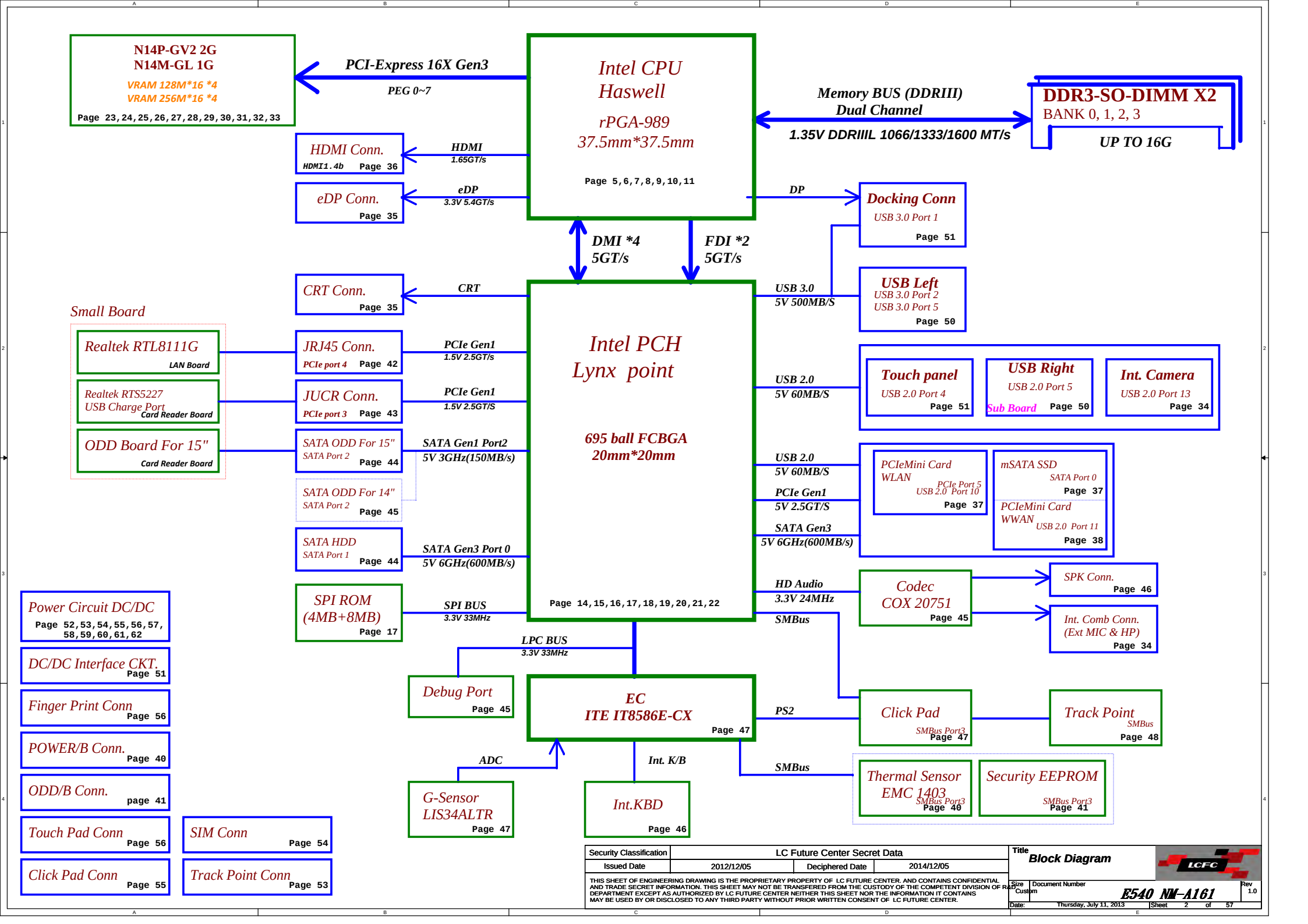

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Title: **Block Diagram**

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	0	0	0	0
S3	0	0	0	X
S5 S4/AC Only	0	0	X	X
S5 S4 Battery only	0	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
EHCI1	XHCI 1	0	Camera
	2	1	USB Port (Right Side)
		2	USB Port (Left Side)
	3	3	
	4	4	
		5	USB Port (Right Side)
		6	
		7	
EHCI2		8	
		9	
		10	Mini Card(WLAN)
		11	
		12	
		13	Blue Tooth

BOM Structure Table

BOM Structure	BTO Item
HDMI@	HDMI part
CHG@	USB charger part
NOCHG@	No USB charger part
CMOS@	CMOS Camera part
8171@	QCA8171 LAN part
8171S@	QCA8171 LAN surge part
SURGE@	QCA8171&8172 LAN surge part
X76@	X76 Level part for VRAM
GC6@	NV CG6 support part
NOGC6@	
AOAC@	AOAC support part
KBL@	K/B Light part
ME@	ME part
SLI@	For SLI function part
DS3@	Deep S3 support part
S3@	For S3 function part
GT@	NV chip part
@	Unpop
EDP@	Support EDP panel function
daul@	Support daul channel panel function

SMBUS Control Table

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module
EC_SMB_CK1 EC_SMB_DA1	IT8580E +3VALW	X	X	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580E +3VS	V +3VS	V +3VS	X	X	X	X	V +3VS	V +3V_PCH	X
PM_SMBCLK PM_SMBDATA	PCH +3V_PCH	X	X	X	X	V +3VS	V +3VS	X	V +3V_PCH	V +3VS

PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	Card Reader
5	
6	
7	
8	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Master VGA	0x9E
Slave VGA	0x9C

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

ZZZ1

DA80000TX00

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Title: Notes List

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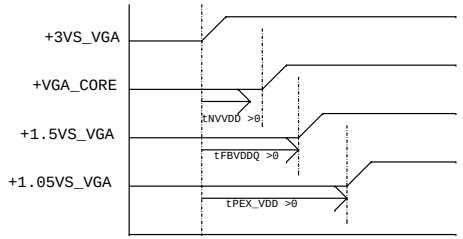
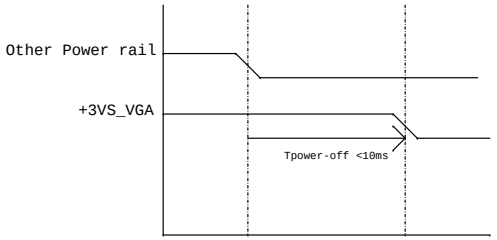
Hot plug detect for IFP link E

VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	_	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	-	DPRSLPVR_VGA
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GPIO9
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	-	FRMLCK#
GPIO17	IN	N/A	
GPIO18	IN	-	dGPU_HDMI_HPD
GPIO19	IN	-	HPD_IRQ



1. all power rail ramp up time should be larger than 40us



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID
N13P-GT (28nm)	0x0FDB

	setting	I2C Slave addrees ID
SMB_ALT_ADDR (ROM_SO Bit 1)	0	0x9E
	1	0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	PU 10K	PU 25K	PU 45K	PD 35K	PD 10K	PU 5K	PD 10K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

GPU		N13P-GT		
FB Memory (GDDR5)		ROM_SI		
Samsung 2500MHz	K4G10325FG-HC04			
	32Mx32	PD 45K		
Hynix 2500MHz	H5GQ1H24BFR-T2C			
	32Mx32	PD 35K		
Samsung 2500MHz	K4G20325FD-FC04			
	64Mx32	PD 30K		
Hynix 2500MHz	H5GQ2H24MFR-T2C			
	64Mx32	PD 25K		

Title: VGA Notes List

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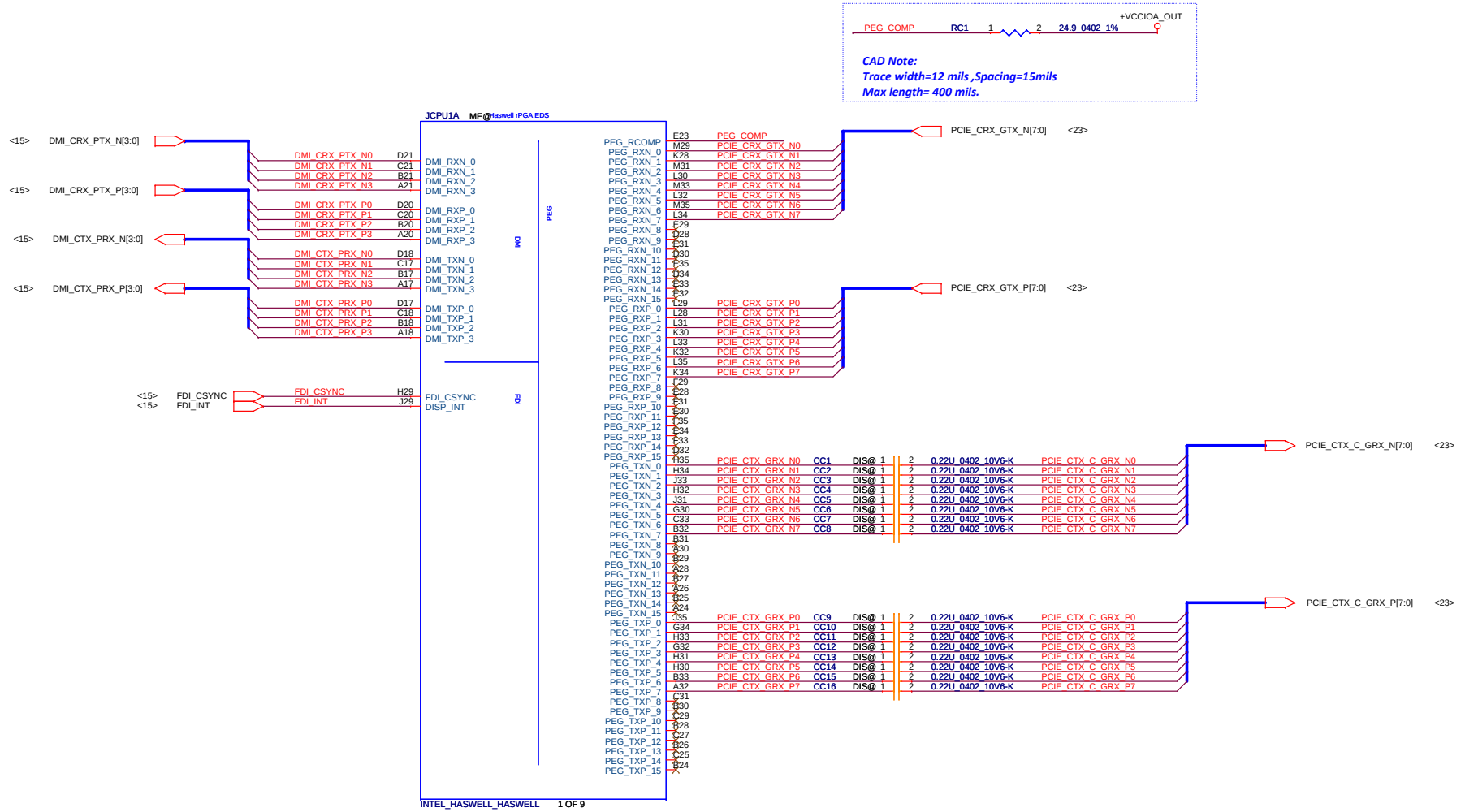

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Title: CPU_DMI/PEG/FDI

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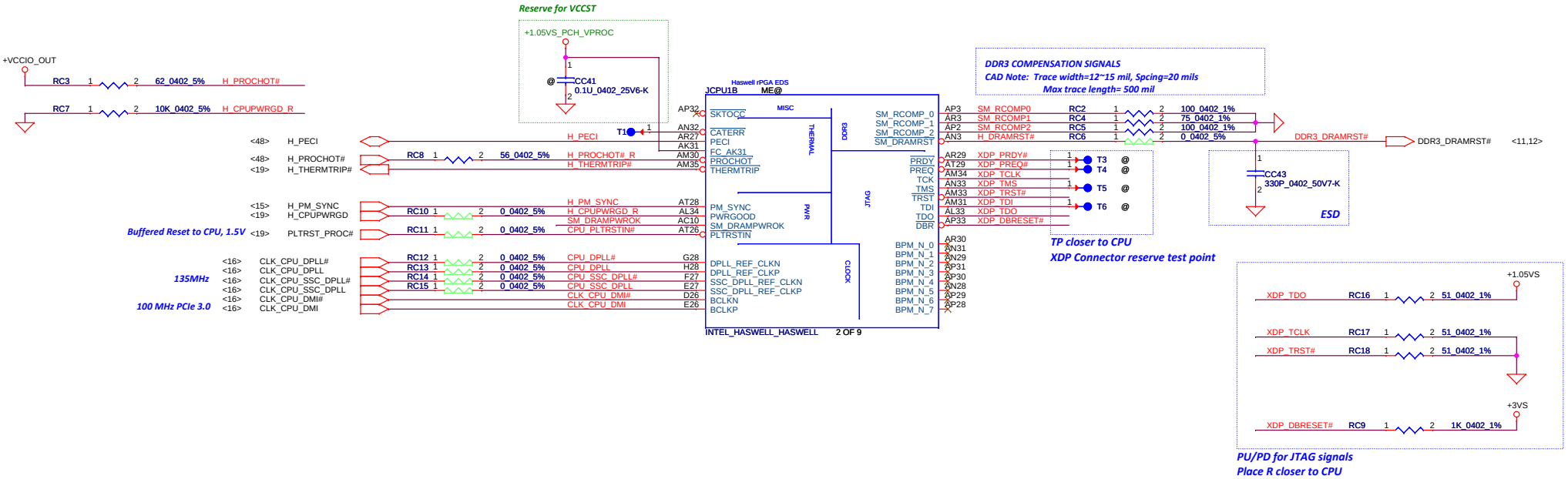
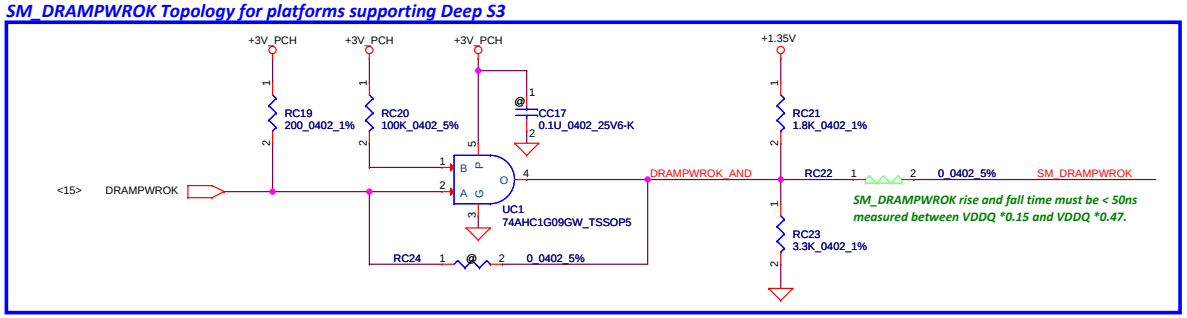
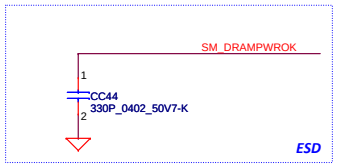


SM_DRAMPWROK Topology for platforms supporting Deep S3



Close to JCPU. AC10



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Title: CPU_JTAG/XDP/CLK

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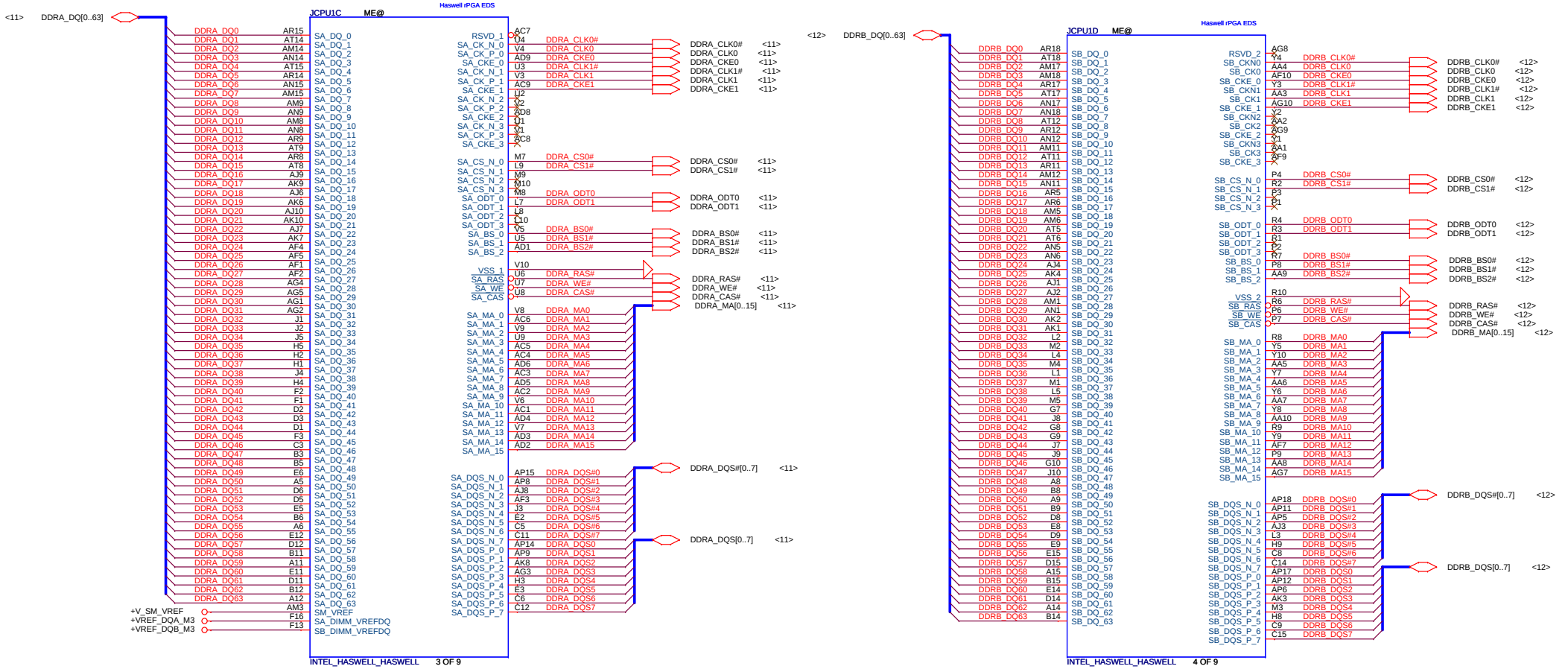

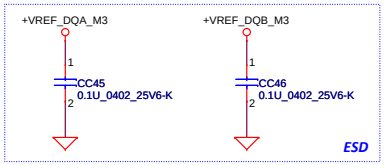

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Title: CPU_DDR3 INTERFACE

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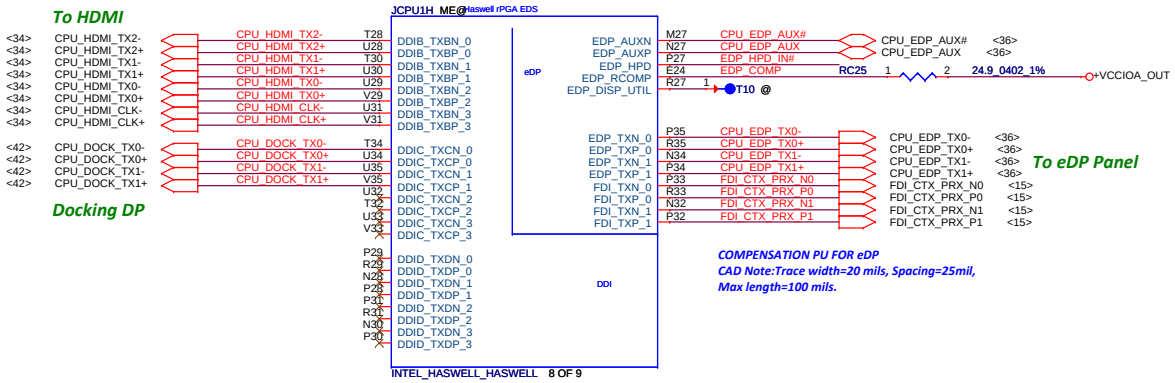
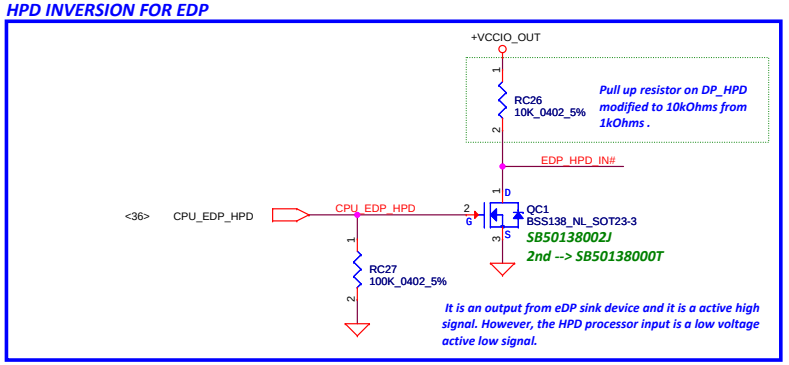
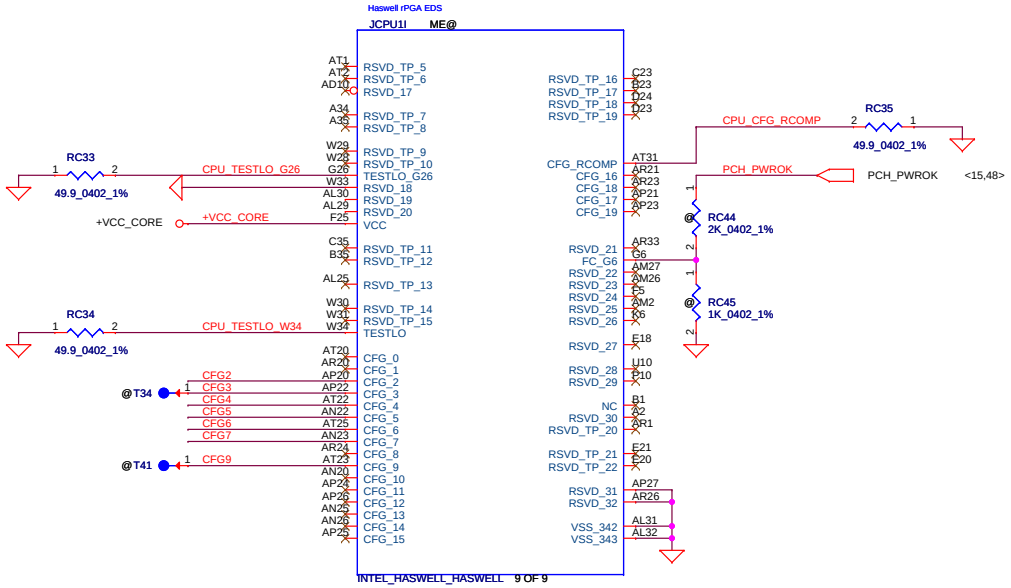


COMPENSATION PU FOR eDP
CAD Note:Trace width=20 mils, Spacing=25mil,
Max length=100 mils.

HPD INVERSION FOR EDP





CFG STRAPS For CPU
(CFG[17:0] internal pull high 5～15K to VCCIO)

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: (Default) Normal Operation; Lane# definition matches socket pin map definition 0: Lane Reversed

CFG2 RC28 1 @ 2 1K_0402_1%

Display Port Presence Strap	
CFG4	1 : Disabled No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG4 RC29 1 2 1K_0402_1%

PCIE Port Bifurcation Straps	
CFG[6:5]	11 : Func 1 Disabled, Func 2 Disabled (x16,---,---) * 10 : Func 1 Enabled, Func 2 Disabled (x8,x8,---) 01 : Func 1 Disabled, Func 2 Enabled 00 : Func 1 Enabled, Func 2 Enabled (x8,x4,x4)

CFG5 RC30 1 @ 2 1K_0402_1%
CFG6 RC31 1 @ 2 1K_0402_1%

PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train Immediately Following XXRESETB Deassertion 0 : PEG Wait for BIOS for Training

CFG7 RC32 1 @ 2 1K_0402_1%

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Title: CPU_eDP/DDI/RSVD/CFG

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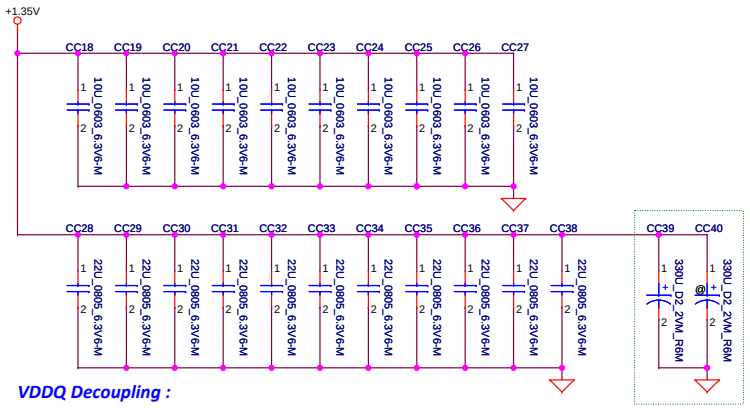
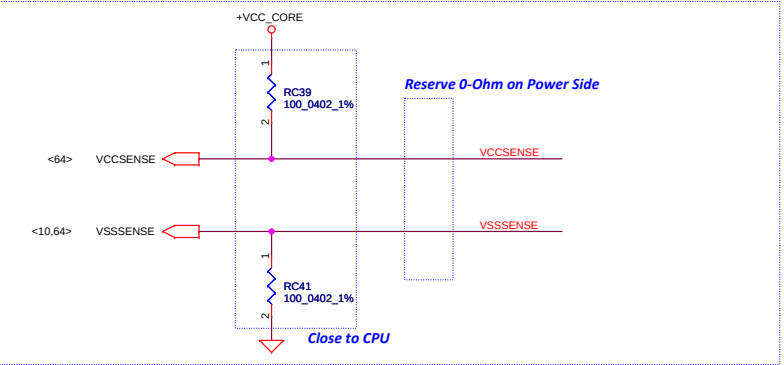
CPU VDDQ DECOUPLING

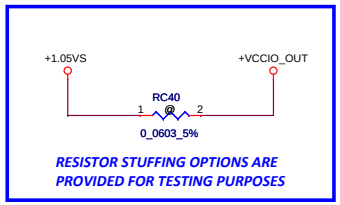


VDDQ Decoupling :

1. MB Bottom Socket Edge --> 2* 330uf, 6mΩ
2. 6x MB Bottom Socket Cavity --> 11* 22 µF (0805), 3mΩ
   5x MB Top Socket Cavity
3. 5x MB Bottom Socket Cavity --> 10 x 10 µF (0805), 3mΩ
   5x MB Top Socket Cavity

VCC/VSS SENSE





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Title: CPU_POWER

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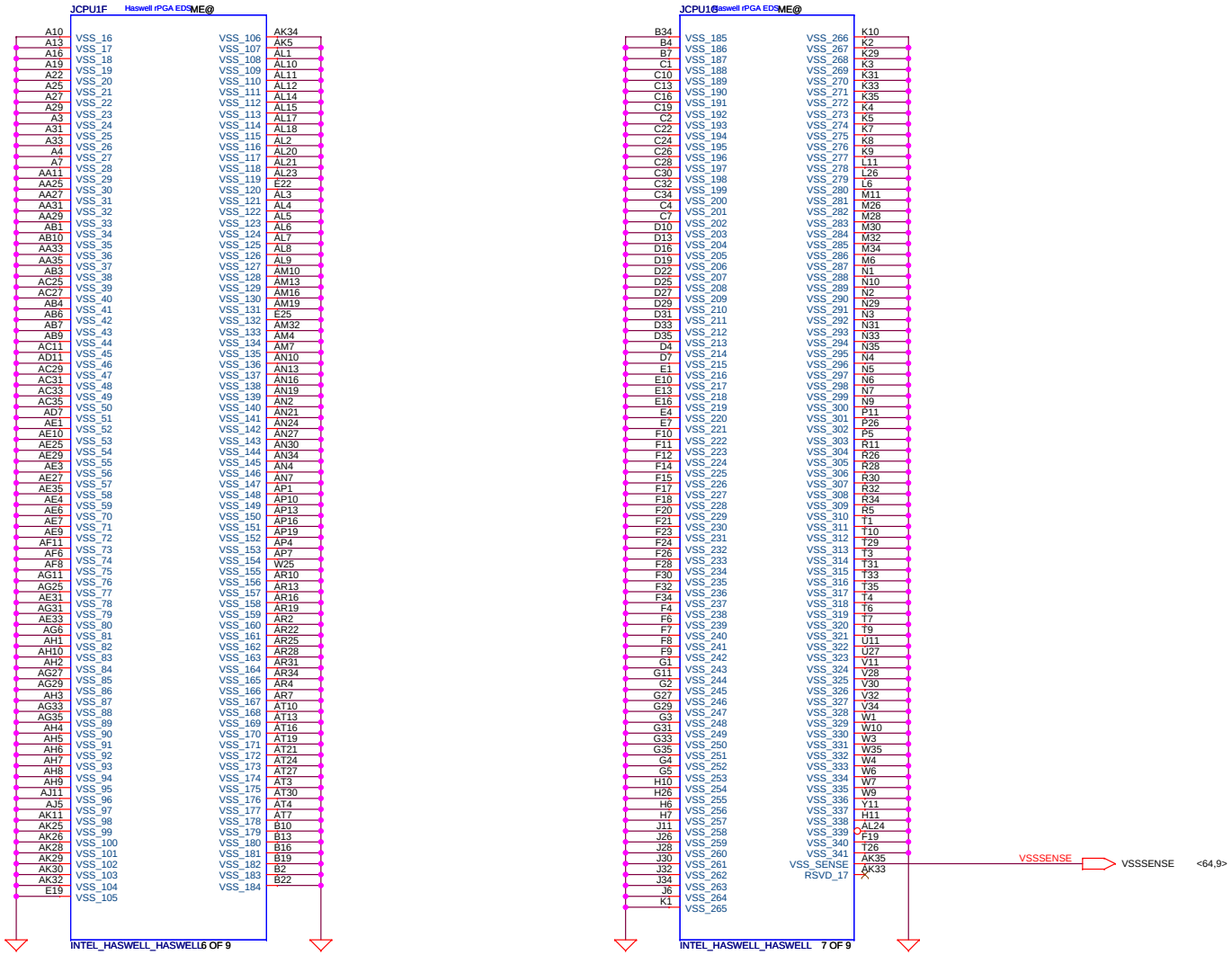

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Title: CPU_GND

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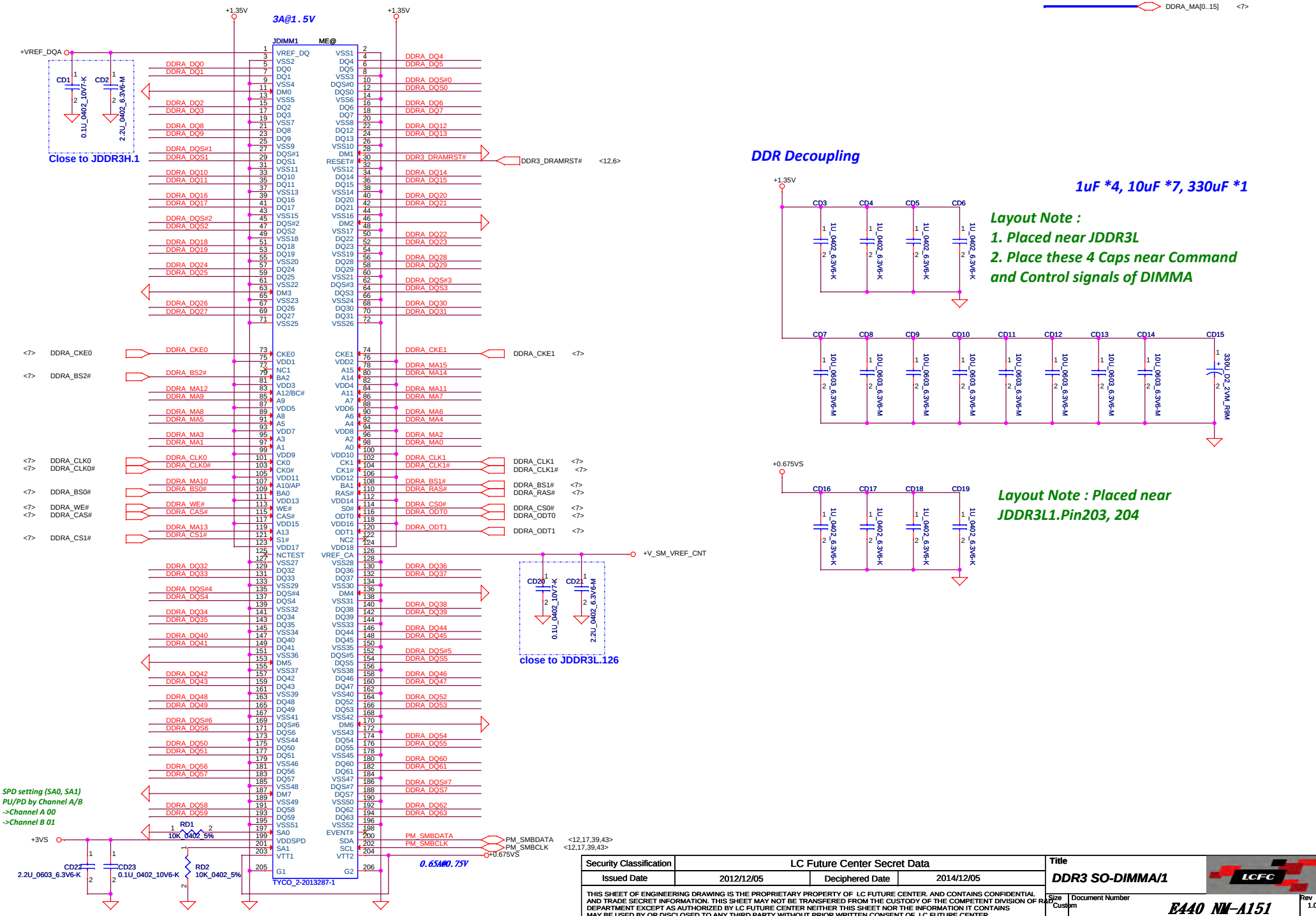
DDR3 SO-DIMM A



DDR Decoupling

1uF *4, 10uF *7, 330uF *1

Layout Note :

1. Placed near JDDR3L
2. Place these 4 Caps near Command and Control signals of DIMMA

Layout Note : Placed near JDDR3L1.Pin203, 204

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DDR3 SO-DIMM B

3A@1.5V

JDIMM2 ME@

+1.35V

+VREF_DQB

CD25 0.1U_0402_10V7-K

CD24 2.2U_0402_6.3V6-M

Close to JDDR3L.1

1	VREF_DQ	VSS1	2				
3	VSS2	DQ4	4	DDRB_DQ0	DDRB_DQ4		
5	DQ0	DQ5	6	DDRB_DQ1	DDRB_DQ5		
7	DQ1	VSS3	8				
9	VSS4	DQS#0	10		DDRB_DQS#0		
11	DM0	DQS0	12	DDRB_DQ2	DDRB_DQS0		
13	VSS5	VSS6	14				
15	DQ2	DQ6	16	DDRB_DQ3	DDRB_DQ6		
17	DQ3	DQ7	18		DDRB_DQ7		
19	VSS7	VSS8	20				
21	DQ8	DQ12	22	DDRB_DQ8	DDRB_DQ12		
23	DQ9	DQ13	24	DDRB_DQ9	DDRB_DQ13		
25	VSS9	VSS10	26				
27	DQS#1	DM1	28				
29	DQS1	RESET#	30	DDRB_DQS#1	DDR3_DRAMRST#	DDR3_DRAMRST#	<11,6>
31	VSS11	VSS12	32	DDRB_DQS1			
33	DQ10	DQ14	34		DDRB_DQ14		
35	DQ11	DQ15	36	DDRB_DQ10	DDRB_DQ15		
37	VSS13	VSS14	38	DDRB_DQ11			
39	DQ16	DQ20	40		DDRB_DQ20		
41	DQ17	DQ21	42	DDRB_DQ16	DDRB_DQ21		
43	VSS15	VSS16	44	DDRB_DQ17			
45	DQS#2	DM2	46				
47	DQS2	VSS17	48	DDRB_DQS#2			
49	VSS18	DQ22	50	DDRB_DQS2	DDRB_DQ22		
51	DQ18	DQ23	52		DDRB_DQ23		
53	DQ19	VSS19	54	DDRB_DQ18			
55	VSS20	DQ28	56	DDRB_DQ19	DDRB_DQ28		
57	DQ24	DQ29	58		DDRB_DQ29		
59	DQ25	VSS21	60	DDRB_DQ24			
61	VSS22	DQS#3	62	DDRB_DQ25	DDRB_DQS#3		
63	DM3	DQS3	64		DDRB_DQS3		
65	VSS23	VSS24	66				
67	DQ26	DQ30	68	DDRB_DQ26	DDRB_DQ30		
69	DQ27	DQ31	70	DDRB_DQ27	DDRB_DQ31		
71	VSS25	VSS26	72				
73	CKE0	CKE1	74	DDRB_CKE0	DDRB_CKE1	DDRB_CKE1	<7>
75	VDD1	VDD2	76				
77	NC1	A15	78		DDRB_MA15		
79	BA2	A14	80	DDRB_BS2#	DDRB_MA14		
81	VDD3	VDD4	82				
83	A12/BC#	A11	84	DDRB_MA12	DDRB_MA11		
85	A9	A7	86	DDRB_MA9	DDRB_MA7		
87	VDD5	VDD6	88				
89	A8	A6	90	DDRB_MA8	DDRB_MA6		
91	A5	A4	92	DDRB_MA5	DDRB_MA4		
93	VDD7	VDD8	94				
95	A3	A2	96	DDRB_MA3	DDRB_MA2		
97	A1	A0	98	DDRB_MA1	DDRB_MA0		
99	VDD9	VDD10	100				
101	CK0	CK1	102	DDRB_CLK0	DDRB_CLK1	DDRB_CLK1	<7>
103	CK0#	CK1#	104	DDRB_CLK0#	DDRB_CLK1#	DDRB_CLK1#	<7>
105	VDD11	VDD12	106				
107	A10/AP	BA1	108	DDRB_MA10	DDRB_BS1#	DDRB_BS1#	<7>
109	BA0	RAS#	110	DDRB_BS0#	DDRB_RAS#	DDRB_RAS#	<7>
111	VDD13	VDD14	112				
113	WE#	S0#	114	DDRB_WE#	DDRB_CS0#	DDRB_CS0#	<7>
115	CAS#	ODT0	116	DDRB_CAS#	DDRB_ODT0	DDRB_ODT0	<7>
117	VDD15	VDD16	118				
119	A13	ODT1	120	DDRB_MA13	DDRB_ODT1	DDRB_ODT1	<7>
121	S1#	NC2	122	DDRB_CS1#			
123	VDD17	VDD18	124				
125	NCTEST	VREF_CA	126				
127	VSS27	VSS28	128				
129	DQ32	DQ36	130	DDRB_DQ32	DDRB_DQ36		
131	DQ33	DQ37	132	DDRB_DQ33	DDRB_DQ37		
133	VSS29	VSS30	134				
135	DQS#4	DM4	136	DDRB_DQS#4			
137	DQS4	VSS31	138	DDRB_DQS4			
139	VSS32	DQ38	140		DDRB_DQ38		
141	DQ34	DQ39	142	DDRB_DQ34	DDRB_DQ39		
143	DQ35	VSS33	144	DDRB_DQ35			
145	VSS34	DQ44	146		DDRB_DQ44		
147	DQ40	DQ45	148	DDRB_DQ40	DDRB_DQ45		
149	DQ41	VSS35	150	DDRB_DQ41			
151	VSS36	DQS#5	152		DDRB_DQS#5		
153	DM5	DQS5	154		DDRB_DQS5		
155	VSS37	VSS38	156				
157	DQ42	DQ46	158	DDRB_DQ42	DDRB_DQ46		
159	DQ43	DQ47	160	DDRB_DQ43	DDRB_DQ47		
161	VSS39	VSS40	162				
163	DQ48	DQ52	164	DDRB_DQ48	DDRB_DQ52		
165	DQ49	DQ53	166	DDRB_DQ49	DDRB_DQ53		
167	VSS41	VSS42	168				
169	DQS#6	DM6	170	DDRB_DQS#6			
171	DQS6	VSS43	172	DDRB_DQS6			
173	VSS44	DQ54	174		DDRB_DQ54		
175	DQ50	DQ55	176	DDRB_DQ50	DDRB_DQ55		
177	DQ51	VSS45	178	DDRB_DQ51			
179	VSS46	DQ60	180		DDRB_DQ60		
181	DQ56	DQ61	182	DDRB_DQ56	DDRB_DQ61		
183	DQ57	VSS47	184	DDRB_DQ57			
185	VSS48	DQS#7	186		DDRB_DQS#7		
187	DM7	DQS7	188		DDRB_DQS7		
189	VSS49	VSS50	190				
191	DQ58	DQ62	192	DDRB_DQ58	DDRB_DQ62		
193	DQ59	DQ63	194	DDRB_DQ59	DDRB_DQ63		
195	VSS51	VSS52	196				
197	SA0	EVENT#	198				
199	VDDSPD	SDA	200		PM_SMBDATA	PM_SMBDATA	<11,17,39,43>
201	SA1	SCL	202		PM_SMBCLK	PM_SMBCLK	<11,17,39,43>
203	VTT1	VTT2	204			+0.675VS	
205	G1	G2	206				

LCN_DAN06-K4806-0103

+V_SM_VREF_CNT

CD43 0.1U_0402_10V7-K

CD44 2.2U_0402_6.3V6-M

Close to JDDR3H.126

0.65A@0.75V

SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

+3VS

RD14 10K_0402_5%

RD16 10K_0402_5%

CD48 2.2U_0603_6.3V6-K

CD49 0.1U_0402_10V6-K

DDRB_DQ[0..63] <7>
DDRB_DQS[0..7] <7>
DDRB_DQS#[0..7] <7>
DDRB_MA[0..15] <7>

DDR Decoupling

1uF *4, 10uF *7, 330uF *1

+1.35V

CD26 CD27 CD28 CD29 1U_0402_6.3V6-K

CD30 CD31 CD32 CD33 CD34 CD35 CD36 CD37 10U_0603_6.3V6-M

CD38 330U_D2_2VM_R9M

Layout Note :
1. Placed near JDDR3H
2. Place these 4 Caps near Command and Control signals of DIMMA

+0.675VS

CD39 CD40 CD41 CD42 1U_0402_6.3V6-K

Layout Note : Placed near JDDR3H.Pin203, 204

All VREF traces should have 20 mil trace width

+1.35V +VREF_DQA +VREF_DQA_M3 RD3 1K_0402_0.5% RD6 2_0402_1% RD9 1K_0402_0.5% CD45 0.022U_0402_25V7-K RD15 24.9_0402_1%

+1.35V +VREF_DQB +VREF_DQB_M3 RD4 1K_0402_0.5% RD7 2_0402_1% RD10 1K_0402_0.5% CD46 0.022U_0402_25V7-K RD12 24.9_0402_1%

+1.35V +V_SM_VREF_CNT +V_SM_VREF RD5 1K_0402_0.5% RD8 2_0402_1% RD11 1K_0402_0.5% CD47 0.022U_0402_25V7-K RD13 24.9_0402_1%

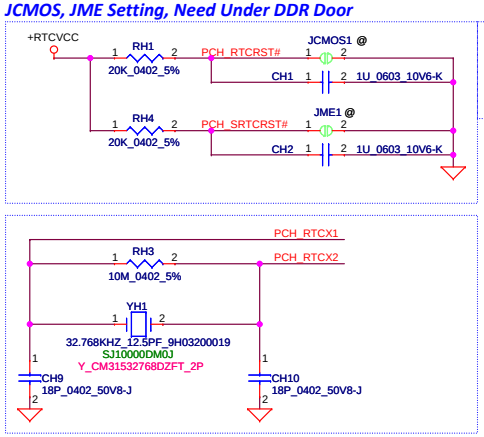
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: DDR3 SO-DIMMB/2

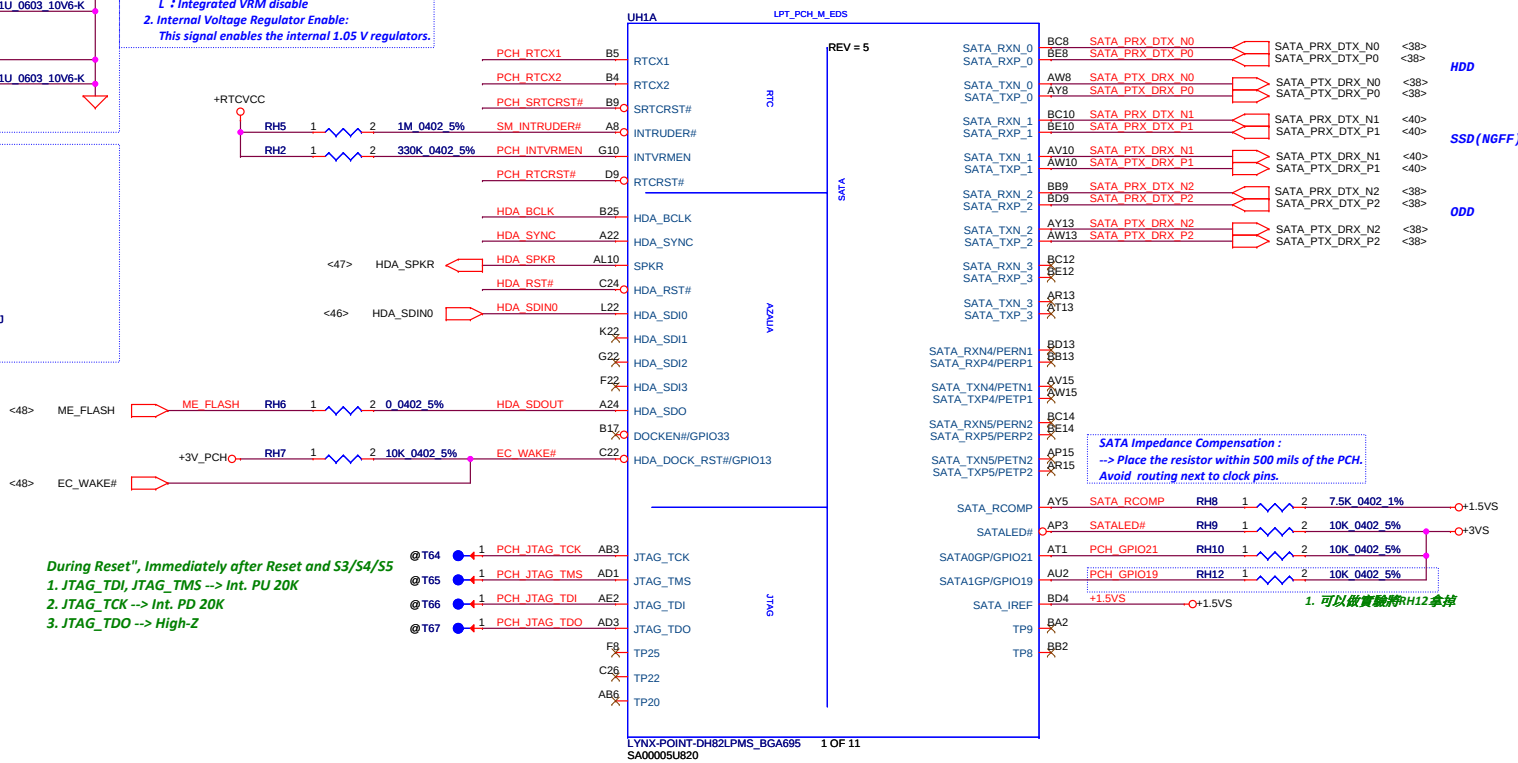
Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

Date: Thursday, July 11, 2013 | Sheet 12 of 57

JCMOS, JME Setting, Need Under DDR Door



* 1. INTVRMEN, should always be pull high
H : Integrated VRM enable (Default)
L : Integrated VRM disable
2. Internal Voltage Regulator Enable:
This signal enables the internal 1.05 V regulators.



SATA_PRX_DTX_N0 <38> SATA_PRX_DTX_P0 <38>
SATA_PTX_DRX_N0 <38> SATA_PTX_DRX_P0 <38>
HDD
SATA_PRX_DTX_N1 <40> SATA_PRX_DTX_P1 <40>
SATA_PTX_DRX_N1 <40> SATA_PTX_DRX_P1 <40>
SSD(NGFF)
SATA_PRX_DTX_N2 <38> SATA_PRX_DTX_P2 <38>
SATA_PTX_DRX_N2 <38> SATA_PTX_DRX_P2 <38>
ODD

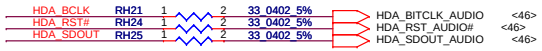
During Reset", Immediately after Reset and S3/S4/S5
1. JTAG_TDI, JTAG_TMS --> Int. PU 20K
2. JTAG_TCK --> Int. PD 20K
3. JTAG_TDO --> High-Z

SATA Impedance Compensation :
--> Place the resistor within 500 mils of the PCH.
Avoid routing next to clock pins.

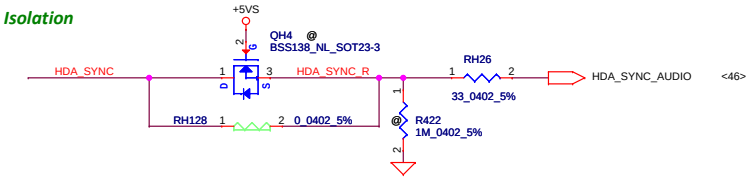
1. 可以做實驗將RH12拿掉

HDA AUDIO SIGNAL

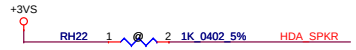
HDA AUDIO For Codec



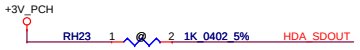
Isolation



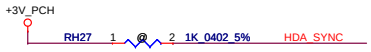
HDA STRAP



* HIGH= Enable (No Reboot)
LOW= Disable (Default)
1. The internal pull-down is disabled after PLTRST# deasserts.
2. When Sampled : Rising edge of PWROK

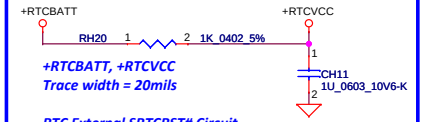


* Low = Disabled (Default)
High = Enabled
[Flash Descriptor Security Overide]



1. This signal has a weak internal pull-down 15K
2. The internal pull-down on AZA_SYNC and AZA_SDO are enabled during reset.

RTCVCC Circuit



+RTCBATT, +RTCVCC
Trace width = 20mils

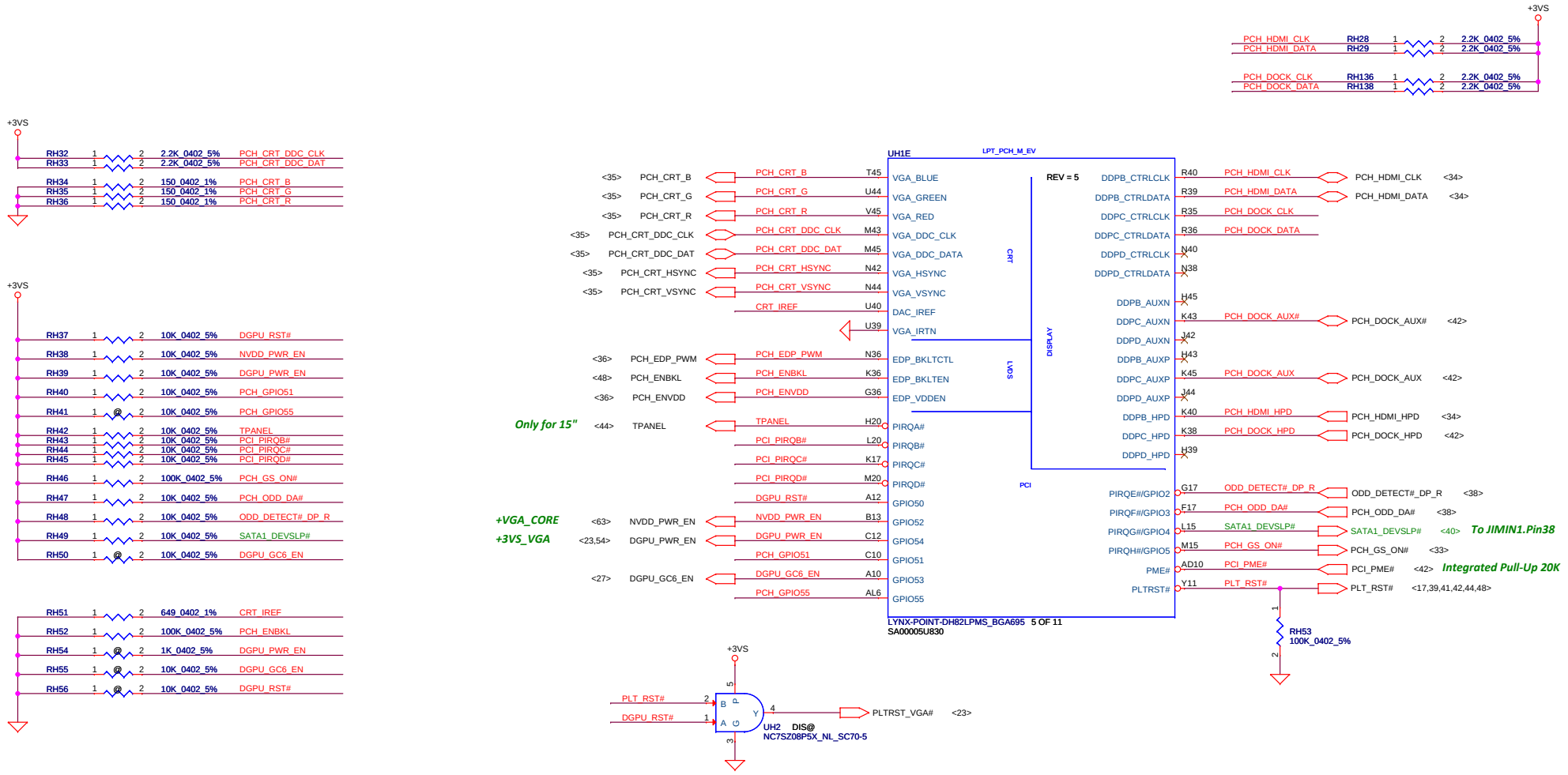
RTC External SRTCRST# Circuit

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: PCH_RTC/HDA/SATA

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

Date: Thursday, July 11, 2013 | Sheet 13 of 57



A16 swap overide Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled * **High=Default

1. The signal has a weak internal pull-up, which is disabled after PLTRST# deasserts.
2. When sampled : Rising edge of PWROK

Boot BIOS Straps (BBS)

BBS_BIT1 (GPIO51)	BBS_BIT0 (GPIO19)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI *

1. GPIO51/19 has weak internal pull-up via 20kohm
2. The internal pull-up is disabled after PLTRST# deasserts.
3. GPIO51 (bit 11) at the rising edge of PWROK
   SATA1GP/GPIO19 (bit 10) at the rising edge of PWROK.

Title			
PCH_CRT/EDP/DDP			
Size: Custom	Document Number: E540 NM-A161		Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 14 of 57		

+3V_PCH
RH57 1 2 10K_0402_5% SUSWARN#_R
+3VALW
RH58 1 2 200K_0402_5% AC_PRESENT
RH59 1 2 10K_0402_5% EC_RSMRST#

SUSACK#_R RH61 1 @ 2 0_0402_5% SUSWARN#_R

Stuff RH289 if EC does not want to involve in the handshake mechanism for the DeepSX state entry and exit

+3VS
CH13 .1U_0402_16V4-Z
<64> VGATE
VGATE
PCH_PWROK
UH3 MC74VHC1G08DFT2G SC70 5P
SYS_PWROK
RH62 10K_0402_5%
@ R1 100K_0402_5%

DPWROK RH60 1 2 100K_0402_5%

100 kOhms ±1% pull-down to GND

UH1B
LPT_PCH_M_EDS
REV = 5

<5> DMI_CTX_PRX_N[3:0]
<5> DMI_CTX_PRX_P[3:0]
<5> DMI_CRX_PTX_N[3:0]
<5> DMI_CRX_PTX_P[3:0]

DMI_CTX_PRX_N0 AW22 — DMI_RXN_0
DMI_CTX_PRX_N1 AR20 — DMI_RXN_1
DMI_CTX_PRX_N2 AP17 — DMI_RXN_2
DMI_CTX_PRX_N3 AV20 — DMI_RXN_3
DMI_CTX_PRX_P0 AY22 — DMI_RXP_0
DMI_CTX_PRX_P1 AP20 — DMI_RXP_1
DMI_CTX_PRX_P2 AR17 — DMI_RXP_2
DMI_CTX_PRX_P3 AW20 — DMI_RXP_3
DMI_CRX_PTX_N0 BD21 — DMI_TXN_0
DMI_CRX_PTX_N1 BE20 — DMI_TXN_1
DMI_CRX_PTX_N2 BD17 — DMI_TXN_2
DMI_CRX_PTX_N3 BE18 — DMI_TXN_3
DMI_CRX_PTX_P0 BB21 — DMI_TXP_0
DMI_CRX_PTX_P1 BC20 — DMI_TXP_1
DMI_CRX_PTX_P2 BB17 — DMI_TXP_2
DMI_CRX_PTX_P3 BC18 — DMI_TXP_3
+1.5VS — BE16 DMI_IREF
AW17 TP12
AV17 TP7
+1.5VS RH67 1 2 7.5K_0402_1% DMI_RCOMP AY17 DMI_RCOMP

DMI

FDI_RXN_0 AJ35 FDI_CTX_PRX_N0 — FDI_CTX_PRX_N0 <8>
FDI_RXN_1 AL35 FDI_CTX_PRX_N1 — FDI_CTX_PRX_N1 <8>
FDI_RXP_0 AJ36 FDI_CTX_PRX_P0 — FDI_CTX_PRX_P0 <8>
FDI_RXP_1 AL36 FDI_CTX_PRX_P1 — FDI_CTX_PRX_P1 <8>
TP16 AV43
TP5 AY45
TP15 AV45
TP10 AW44
FDI_CSYNC AL39 FDI_CSYNC — FDI_CSYNC <5>
FDI_INT AL40 FDI_INT — FDI_INT <5>
FDI_IREF AT45 FDI_IREF RH65 1 2 0_0402_5% +1.5VS
TP17 AU42
TP13 AU44
FDI_RCOMP AR44 FDI_RCOMP RH66 1 2 7.5K_0402_1% +1.5VS

FDI

DSWVREN must be always pulled high to +RTCVCC
DSWVREN - Internal Deep Sleep 1.05V regulator
***H : Enable*
L : Disable

EC to PCH <48> SUSACK# RH68 1 2 0_0402_5% SUSACK#_R R6 — SUSACK#
+3VS SYS_RESET# RH70 1 2 10K_0402_5% SYS_RESET# AM1 — SYS_RESET#
SYS_PWROK AD7 — SYS_PWROK
APWROK may come up earlier than PWROK but no later
<48,8> PCH_PWROK RH73 1 2 0_0402_5% PWROK F10 — PWROK
<48> PCH_APWROK RH74 1 2 0_0402_5% APWROK AB7 — APWROK
<6> DRAMPWROK — DRAMPWROK H3 — DRAMPWROK
<48> EC_RSMRST# — EC_RSMRST# J2 — RSMRST#
PCH to EC <48> SUSWARN# RH75 1 2 0_0402_5% SUSWARN#_R J4 — SUSWARN#/SUSPWRNACK/GPIO30
<48> PBTN_OUT# — PBTN_OUT# K1 — PWRBTN#
<48> AC_PRESENT — AC_PRESENT E6 — ACPRESENT/GPIO31
+3VALW RH76 1 2 10K_0402_5% PCH_BATLOW# K7 — BATLOW#/GPIO72
+3V_PCH RH78 1 2 10K_0402_5% RI# N4 — RI#
AB10 TP21
D2 SLP_WLAN#/GPIO29

System Power Management

DSWVRMEN C8 DSWVRMEN RH69 1 2 330K_0402_5% +RTCVCC
DPWROK L13 DPWROK RH71 1 2 0_0402_5% EC_DPWROK — EC_DPWROK <48> *For Deep S3*
WAKE# K3 WAKE# RH72 1 @ 2 0_0402_5% WLAN_WAKE# — WLAN_WAKE# <39> *For WLAN WAKE# (Disable)*
CLKRUN# AN7 PM_CLKRUN# — PM_CLKRUN# <44>
SUS_STAT#/GPIO61 U7 SUS_STAT# 1 T72 @
SUSCLK/GPIO62 Y6 SUSCLK 1 T73 @
SLP_S5#/GPIO63 Y7 PM_SLP_S5# — PM_SLP_S5# <48>
SLP_S4# C6 PM_SLP_S4# — PM_SLP_S4# <48>
SLP_S3# H1 PM_SLP_S3# — PM_SLP_S3# <48>
SLP_A# F3 PM_SLP_A# — PM_SLP_A# <48>
SLP_SUS# F1 PM_SLP_SUS#_R RH77 1 2 0_0402_5% PM_SLP_SUS# — PM_SLP_SUS# <48,55> *For Deep S3*
PMSYNCH AY3 H_PM_SYNC — H_PM_SYNC <6>
SLP_LAN# G5 PCH_SLPLAN# 1 T74 @

Can be left NC if no use integrated LAN. 10/06 Test point request

Can be left NC when IAMT is not support on the platfrom

+3VALW
WAKE# RH63 1 2 10K_0402_5%
+3VS
PM_CLKRUN# RH64 1 2 10K_0402_5%

LYNX-POINT-DH82LPMS_BGA695 4 OF 11
SA00005U830

APWROK only for A phase

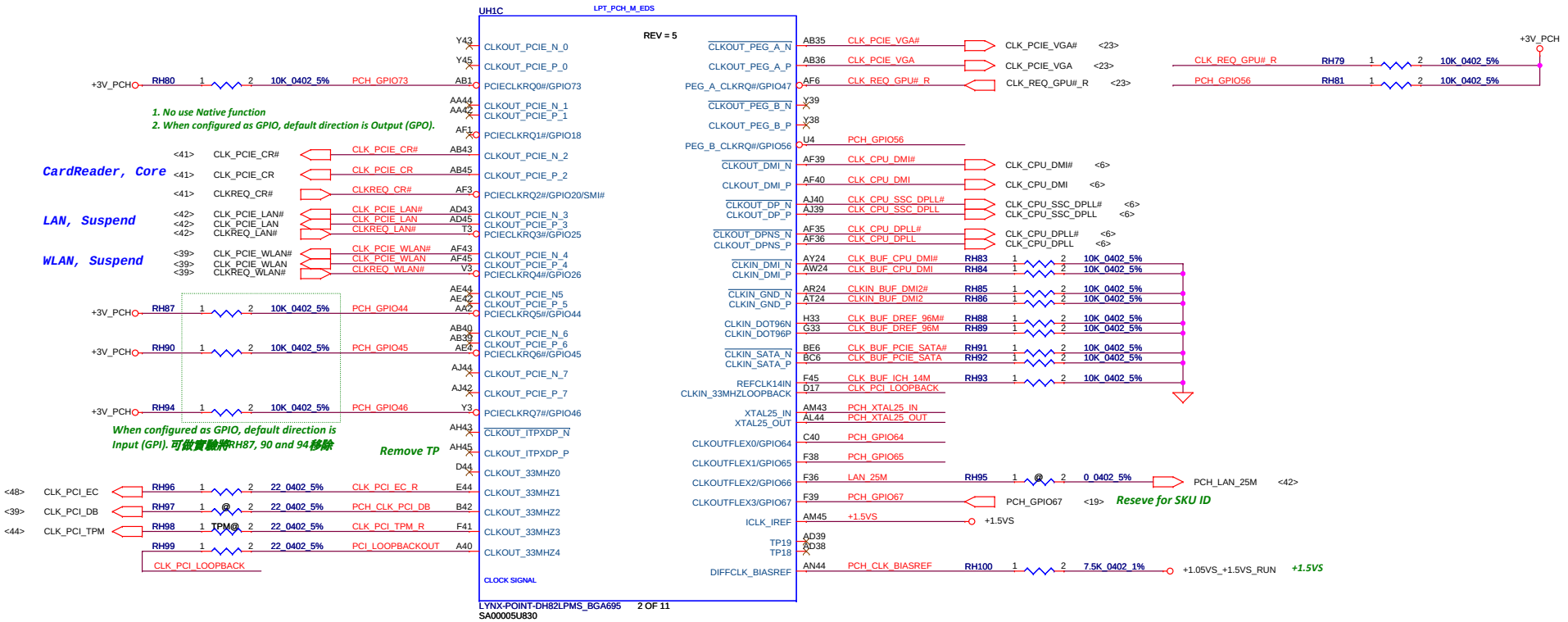
PWROK RH13 1 @ 2 0_0402_5% APWROK

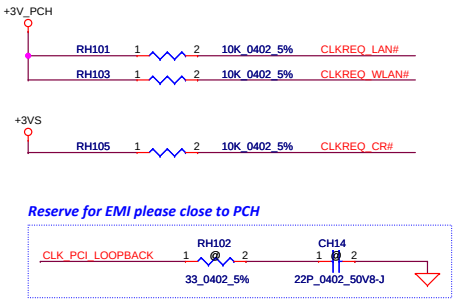
SUSCLK/GPIO62

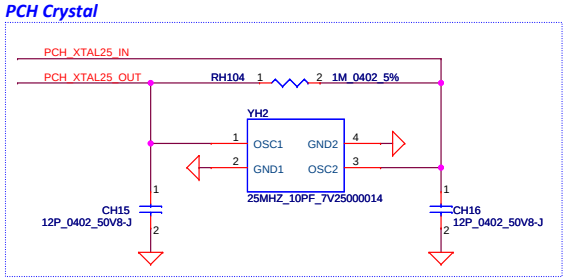
This signal has a weak internal pull-up.
0 = Disable PLL On-Die voltage regulator.
** 1 = Enable PLL On-Die voltage regulator.*
NOTES:
1. The internal pull-up is disabled after RSMRST# deasserts.
2. This signal is in the Suspend well.

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: PCH_DMI/FDI/PM
Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0
Date: Thursday, July 11, 2013 | Sheet 15 of 57

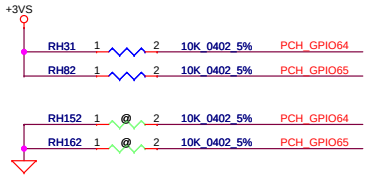






Project Phase ID

Project Phase	PCH_GPIO64	PCH_GPIO65
SDV, FVT	0	0
SIT2 (R 0.5)	0	1
SIT (R 0.4)	1	0
*SVT	1	1

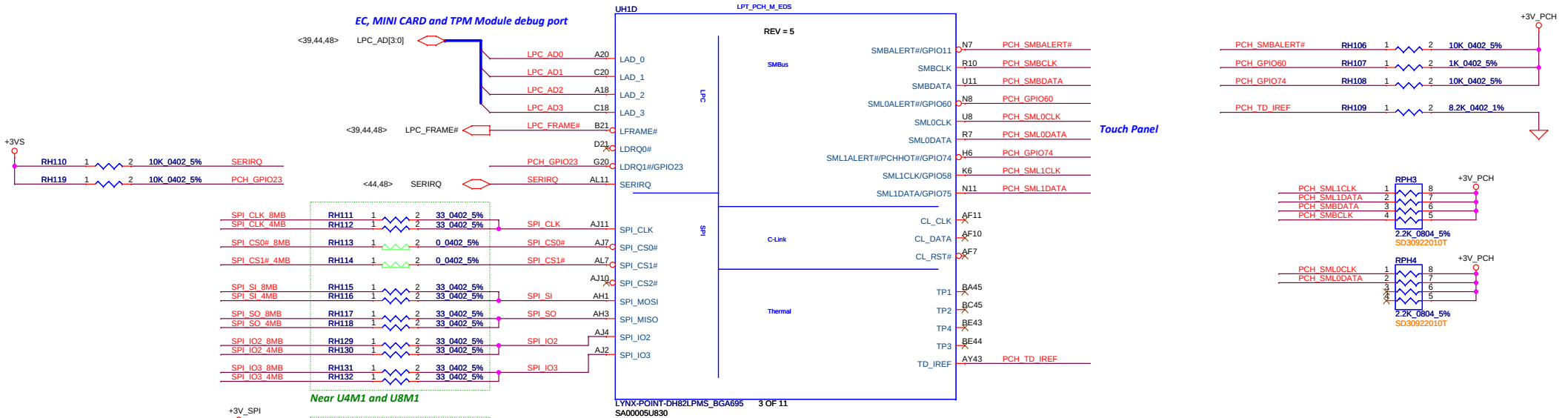


Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: PCH_PCIE/CLK

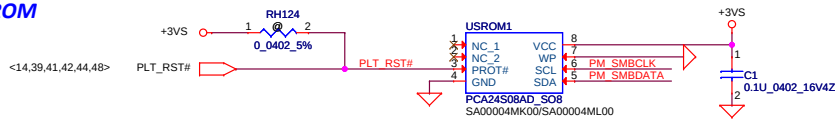
Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

Date: Thursday, July 11, 2013 | Sheet 16 of 57

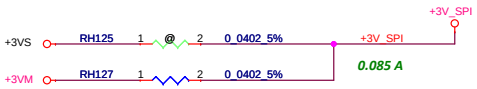


8MB + 4MB SPI ROM, 5MB ME(SBA), Security EEPROM

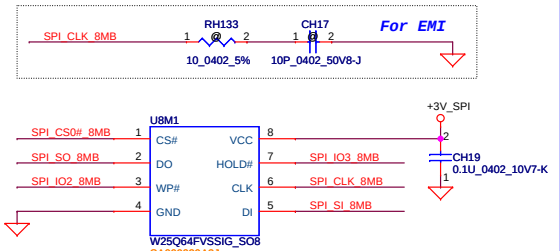
Security EEPROM



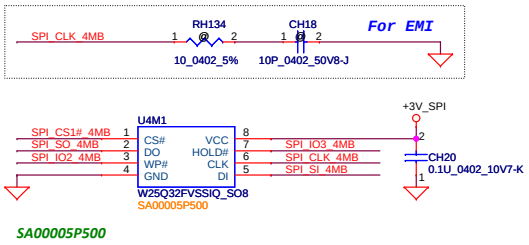
SBA Fun. Power rail



8MB(64Mb)

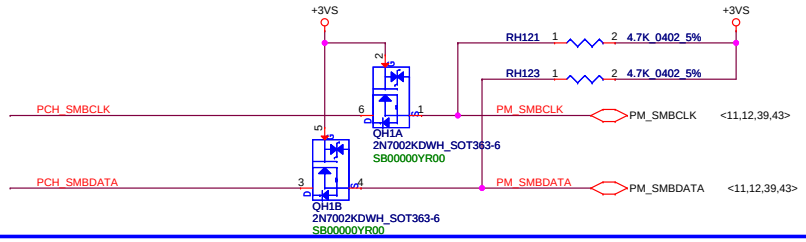


4MB(32Mb)

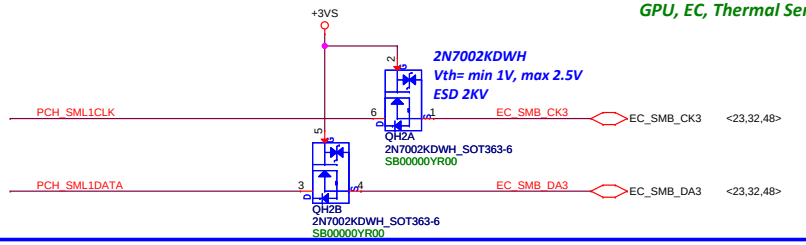


SM Bus

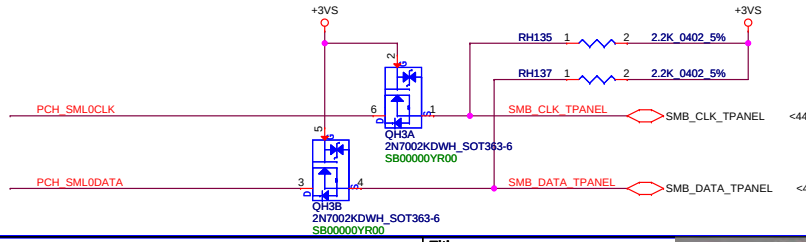
DIMM1, DIMM2, WLAN(@), CP, Security EEPROM



GPU, EC, Thermal Sensor



Touch Panel

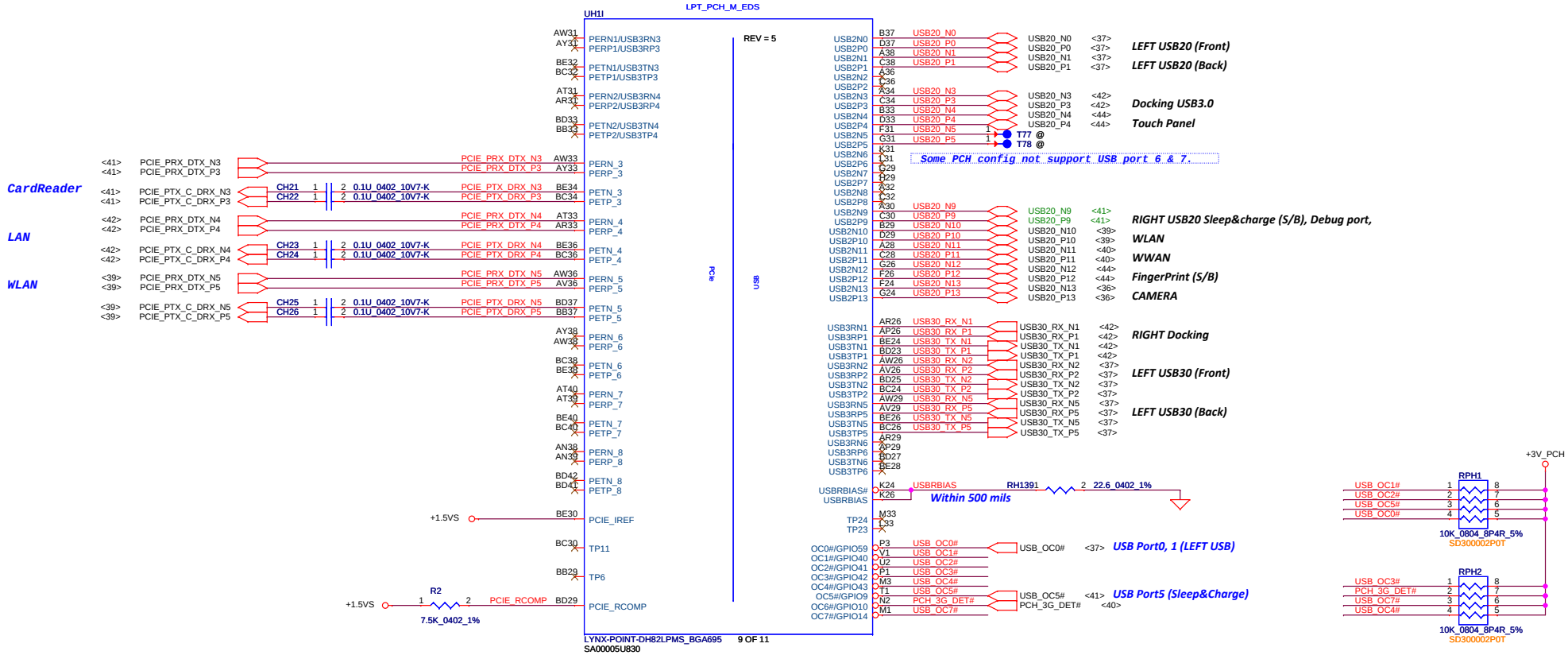


Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: PCH_LPC/SPI/SM BUS

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

Date: Thursday, July 11, 2013 Sheet 17 of 57



USB3.0	USB2.0	OC#	Note
Port1	Port3	X	Docking (Right)
Port2	Port0	OC0#	LEFT USB (Front)
Port5	Port1	OC0#	LEFT USB (Back)
X	Port9	OC5#	Sleep&Charge (Right)

USB2.0 :
OC#0-3 --> Port 0-7
OC#4-7 --> Port 8-13

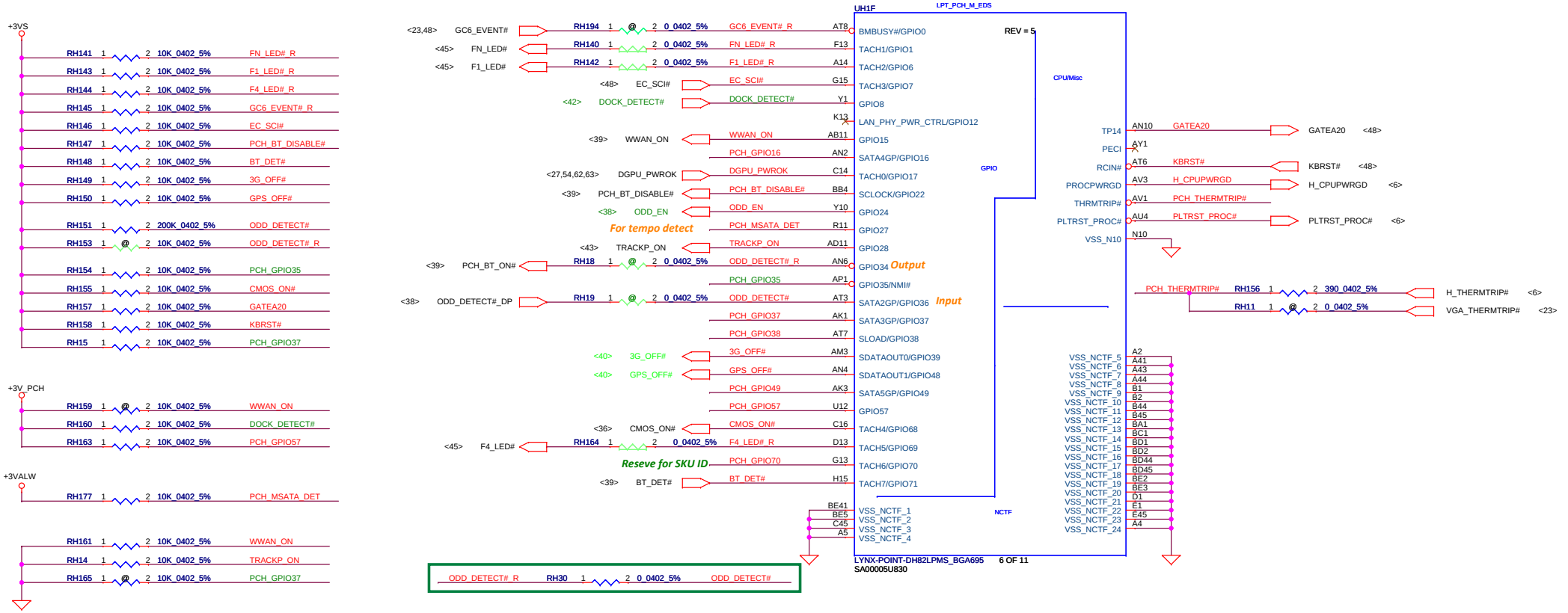
OC[3:0]# should be connected with USB 2.0 ports 0 - 7 and any 4 of USB 3.0 ports 1 - 6.

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

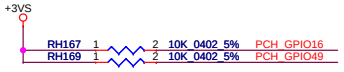
Title: PCH_PCIE/USB/OC#

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

Date: Thursday, July 11, 2013 | Sheet 18 of 57



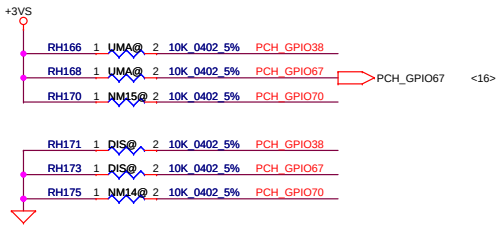
CONFIG	GPIO16, 49
* USB X4,PCIEX8,SATAX6	11
USB X6,PCIEX8,SATAX4	01

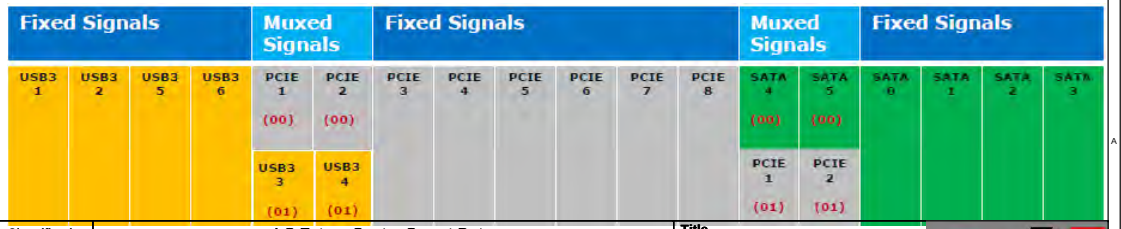


No use Flexible I/O pin, delete RH172, RH174

SKU ID

Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70
* Optimus	0	0	
Reserve	0	1	
DIS	1	0	
* UMA	1	1	
* 14"			0
* 15"			1





Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: PCH_GPIO/CPU-MISC

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

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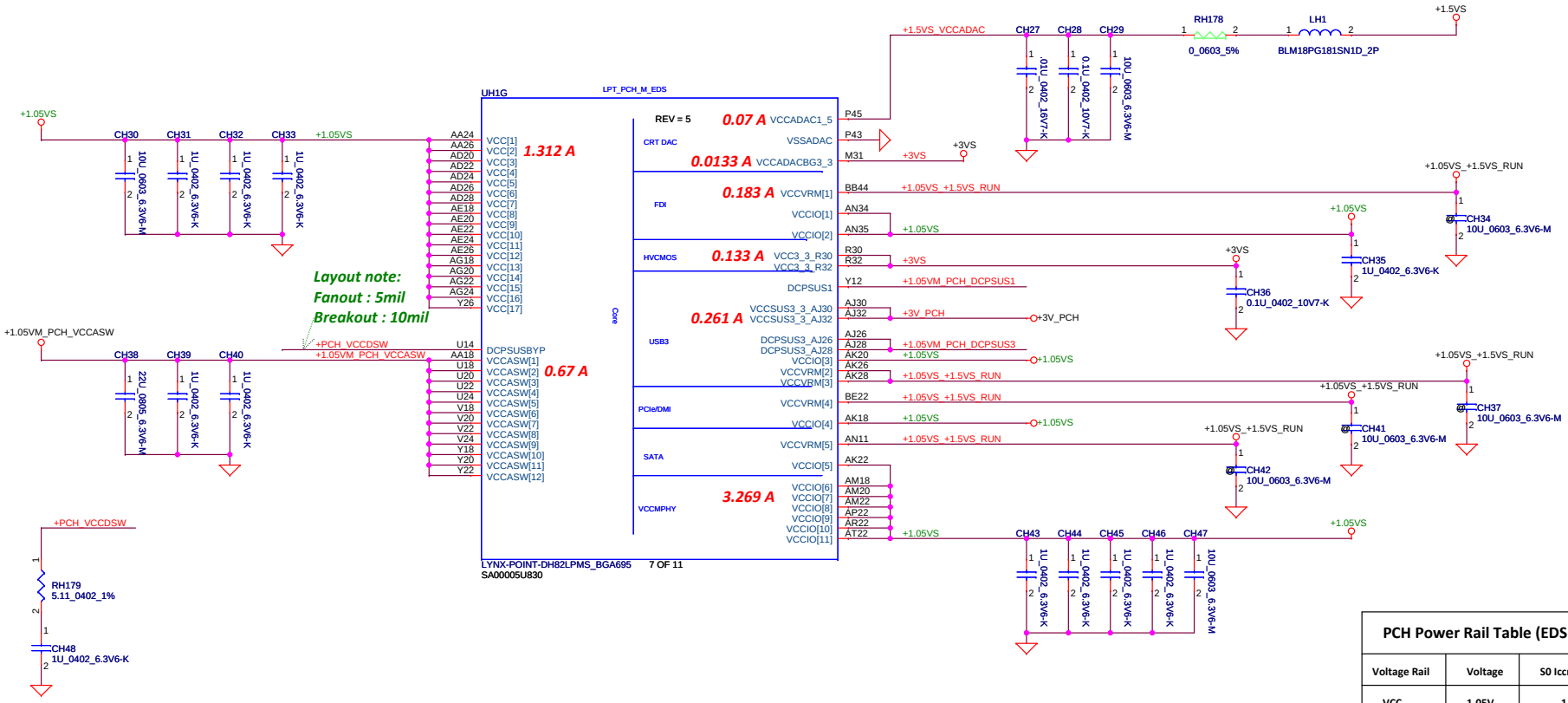

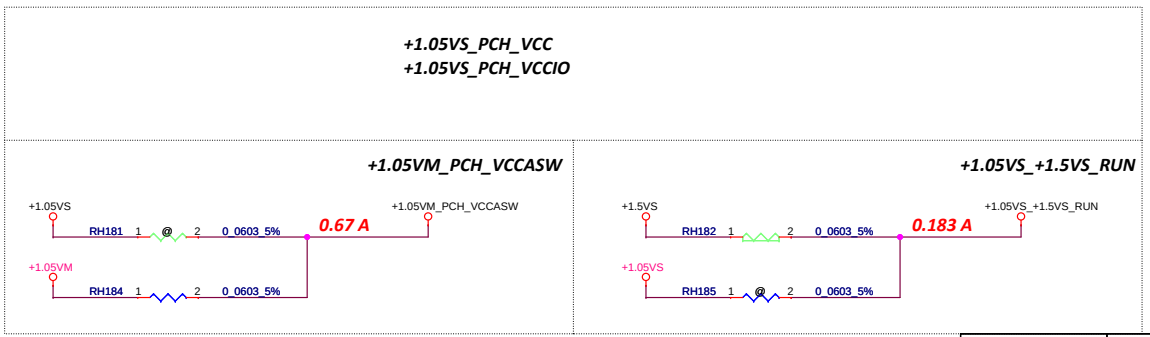

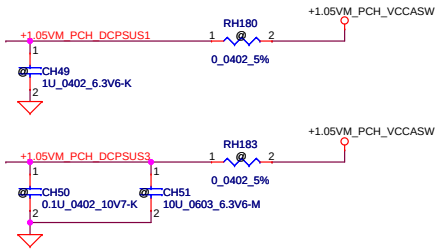

PCH Power Rail Table (EDS Rev1.0)

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.312 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.07 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.183 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: PCH_POWER-1

Size	Document Number	Rev
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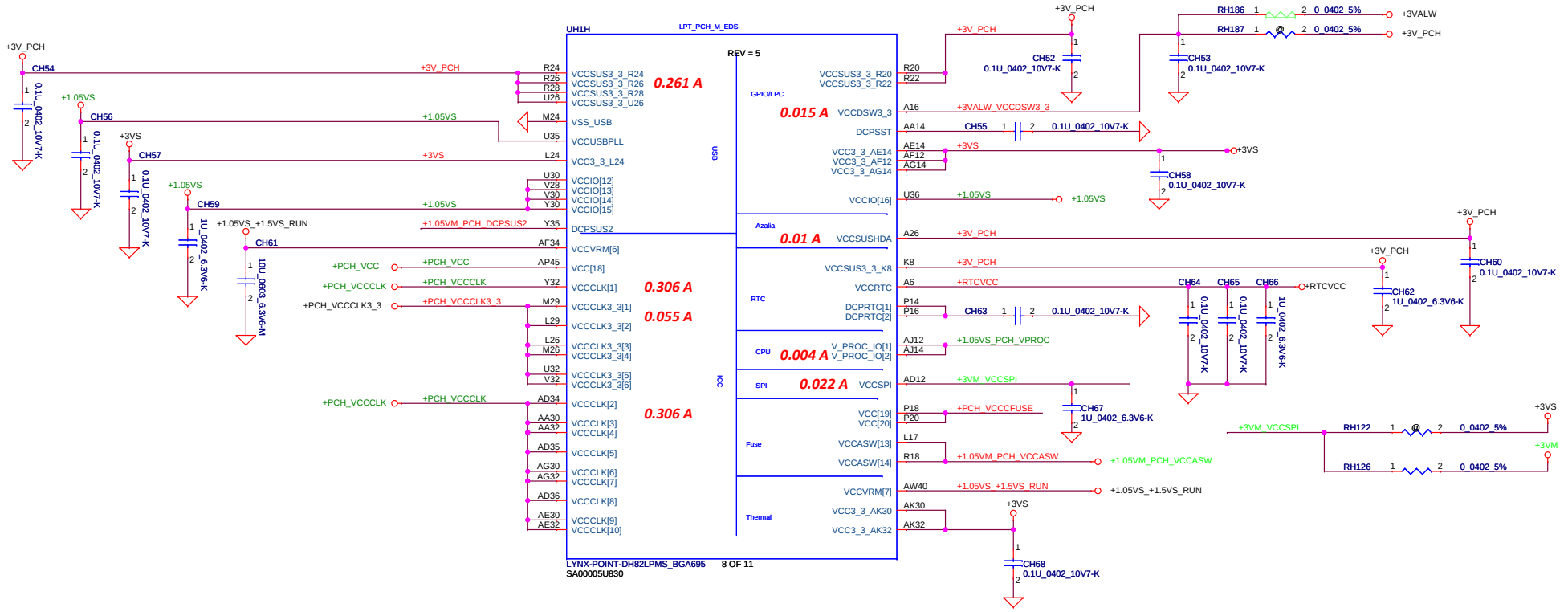
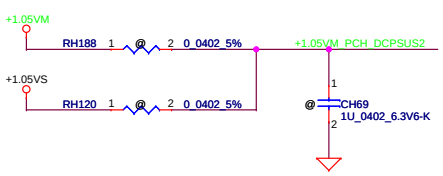
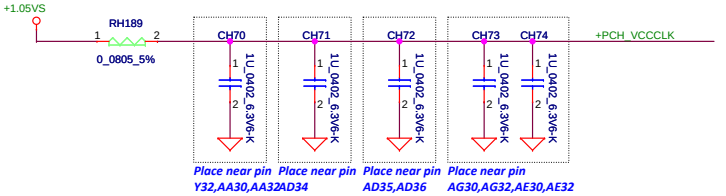


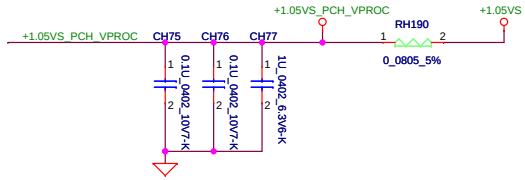
+1.05VM_PCH_DCPSUS2



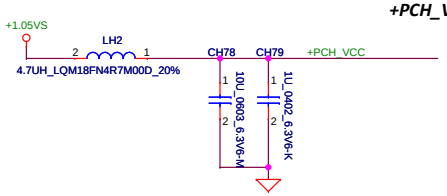
+PCH_VCCCLK



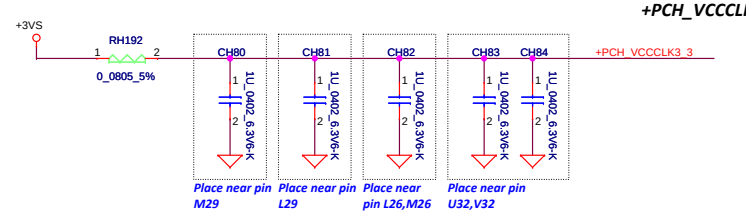
+V_VPROC



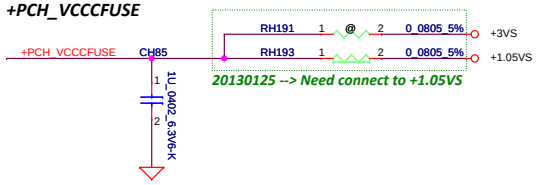
+PCH_VCC



+PCH_VCCCLK3_3



+PCH_VCCCFUSE



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: PCH_POWER-2

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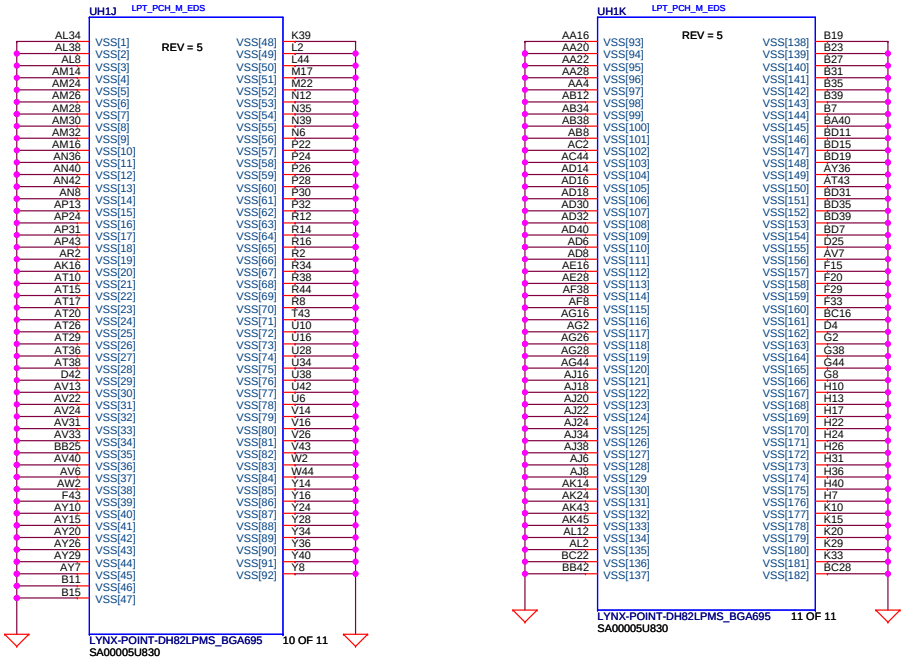

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: PCH_GND

Size	Document Number	Rev
Custom	E540 NM-A161	1.0

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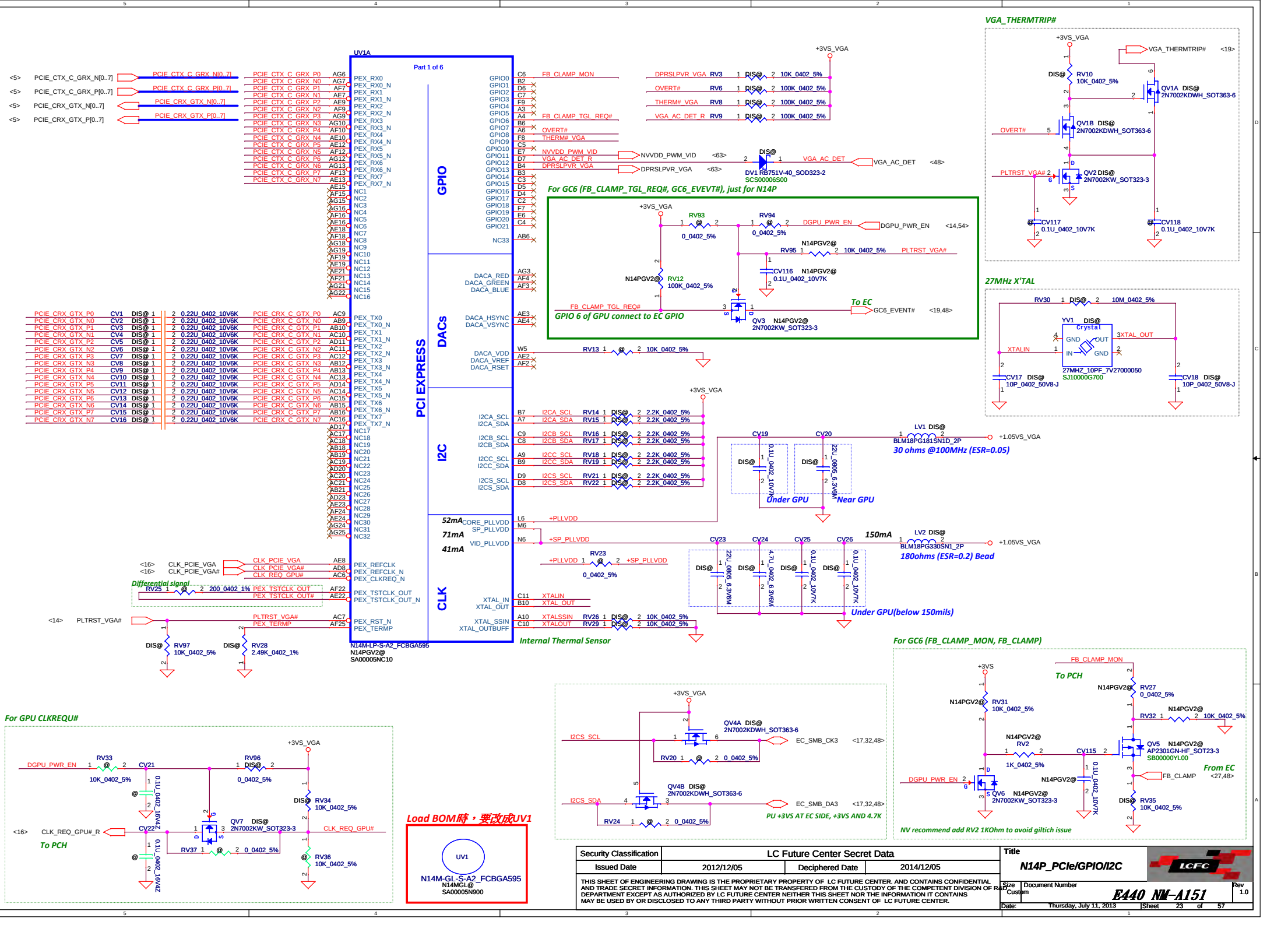
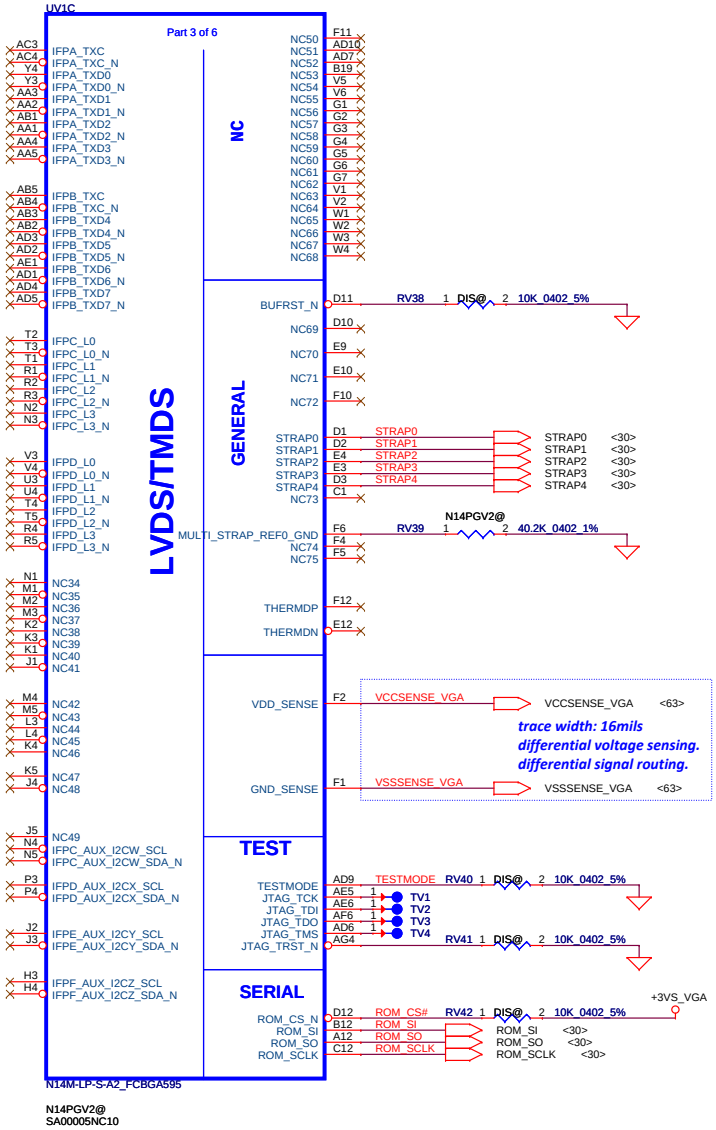


Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: N14P_PCIe/GPIO/I2C

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

Date: Thursday, July 11, 2013 | Sheet 23 of 57



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: N14P_SPI ROM/SENSE

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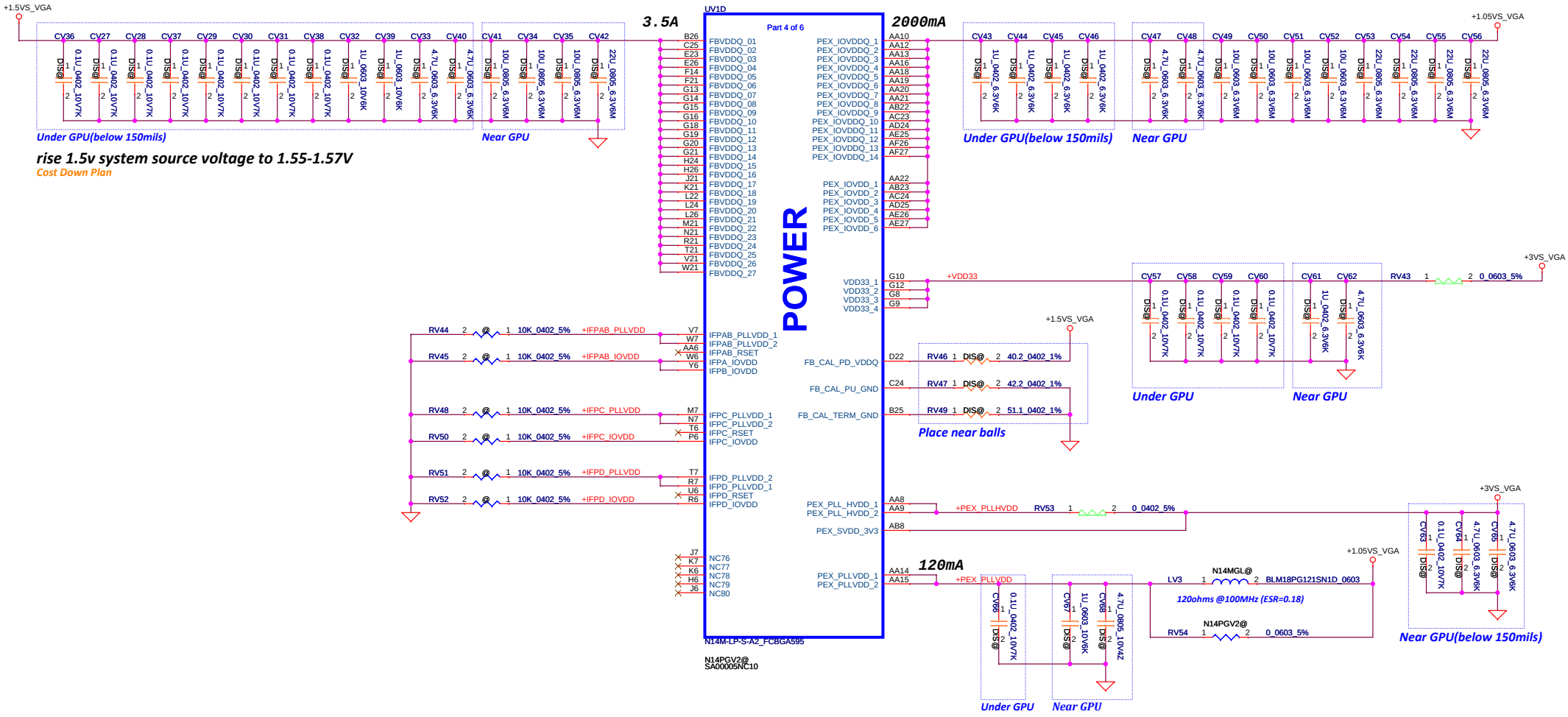

CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	42.2Ohm
FB_CAL_xTERM_GND	51.1Ohm

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: N14P_POWER

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

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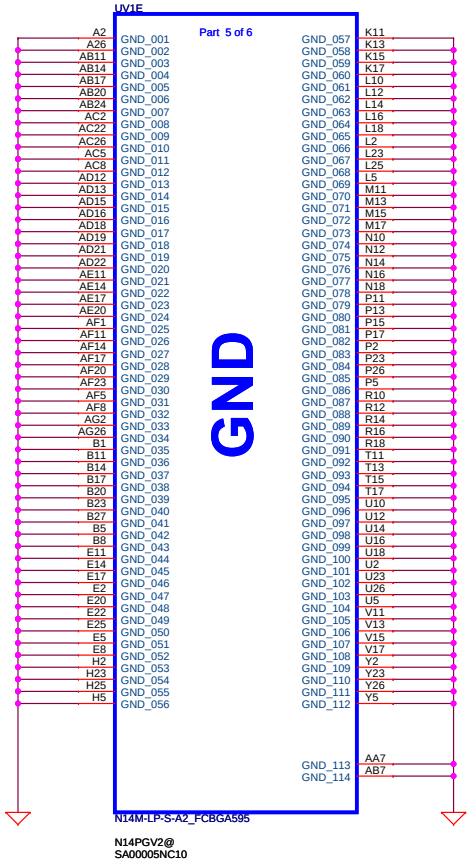
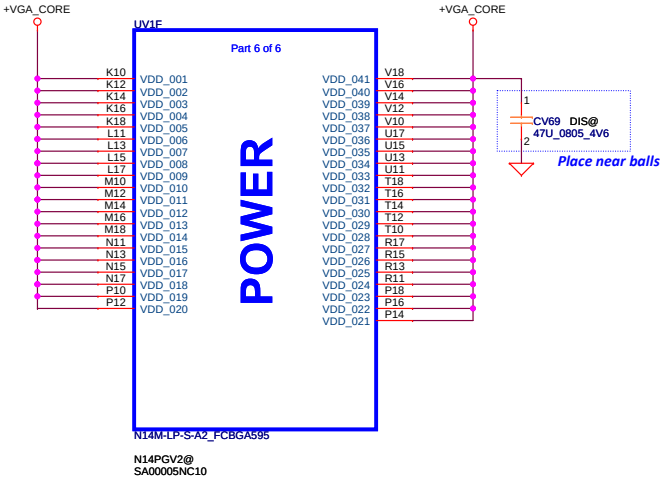
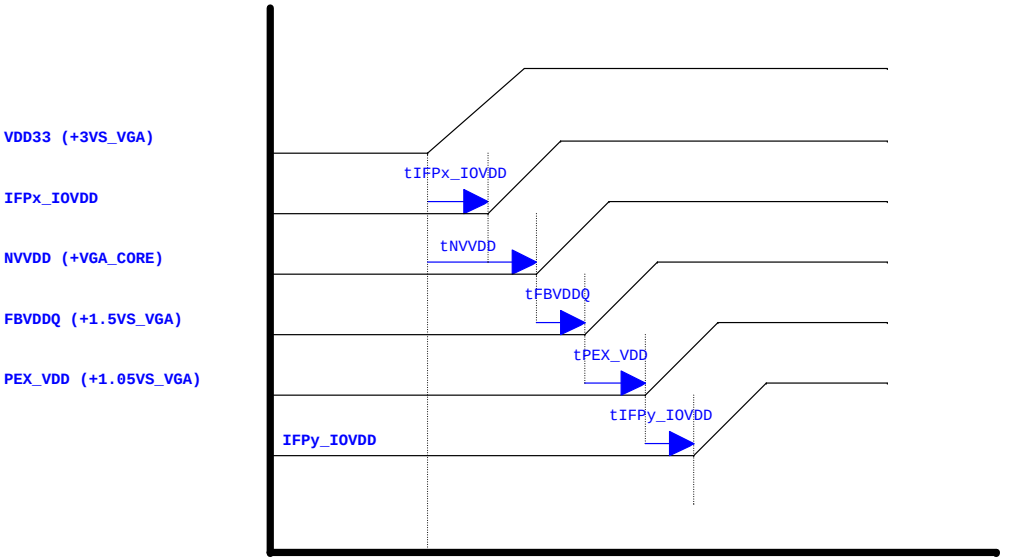






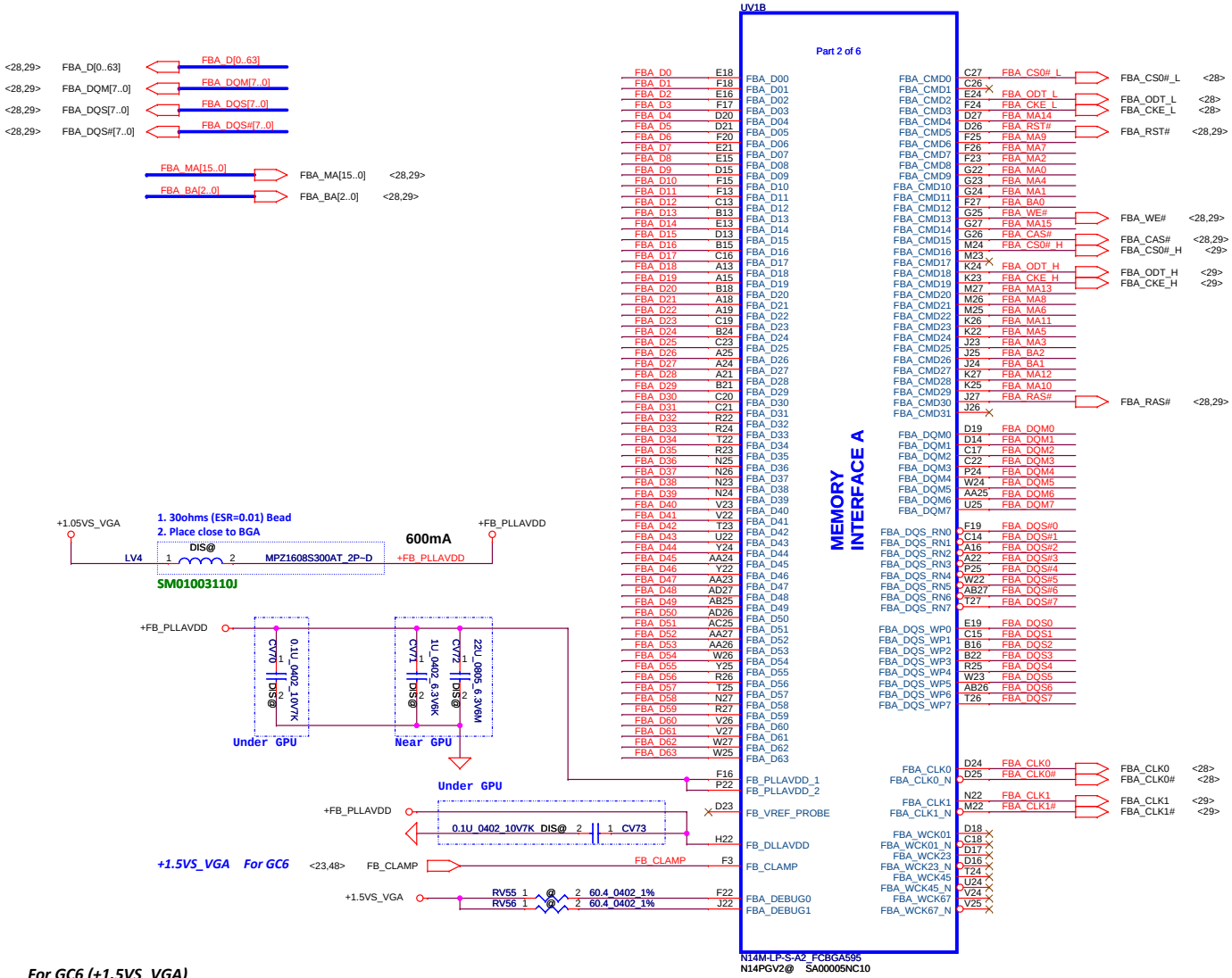
NV Recommended Power On Sequencing Order

X=A and B
Y=C,D,E and F

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: N14P_VDD/GND

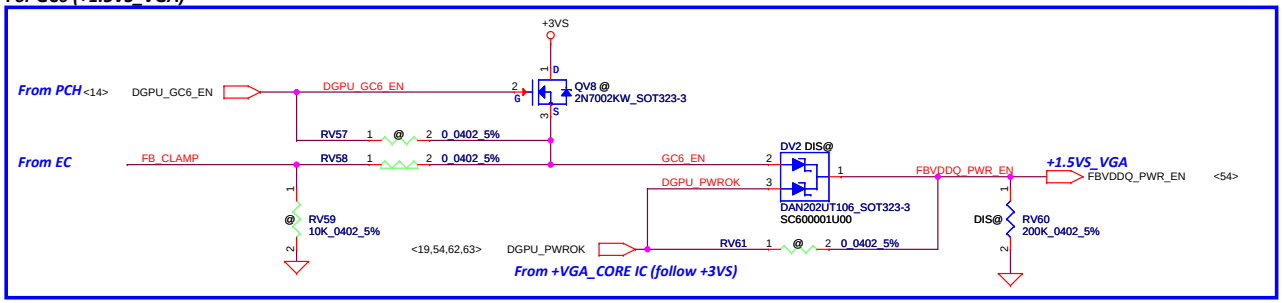
Size: Custom	Document Number: E540 NM-A161	Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 26 of 57	



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

For GC6 (+1.5VS_VGA)



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: N14P_MEM IF/FB CLAMP

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

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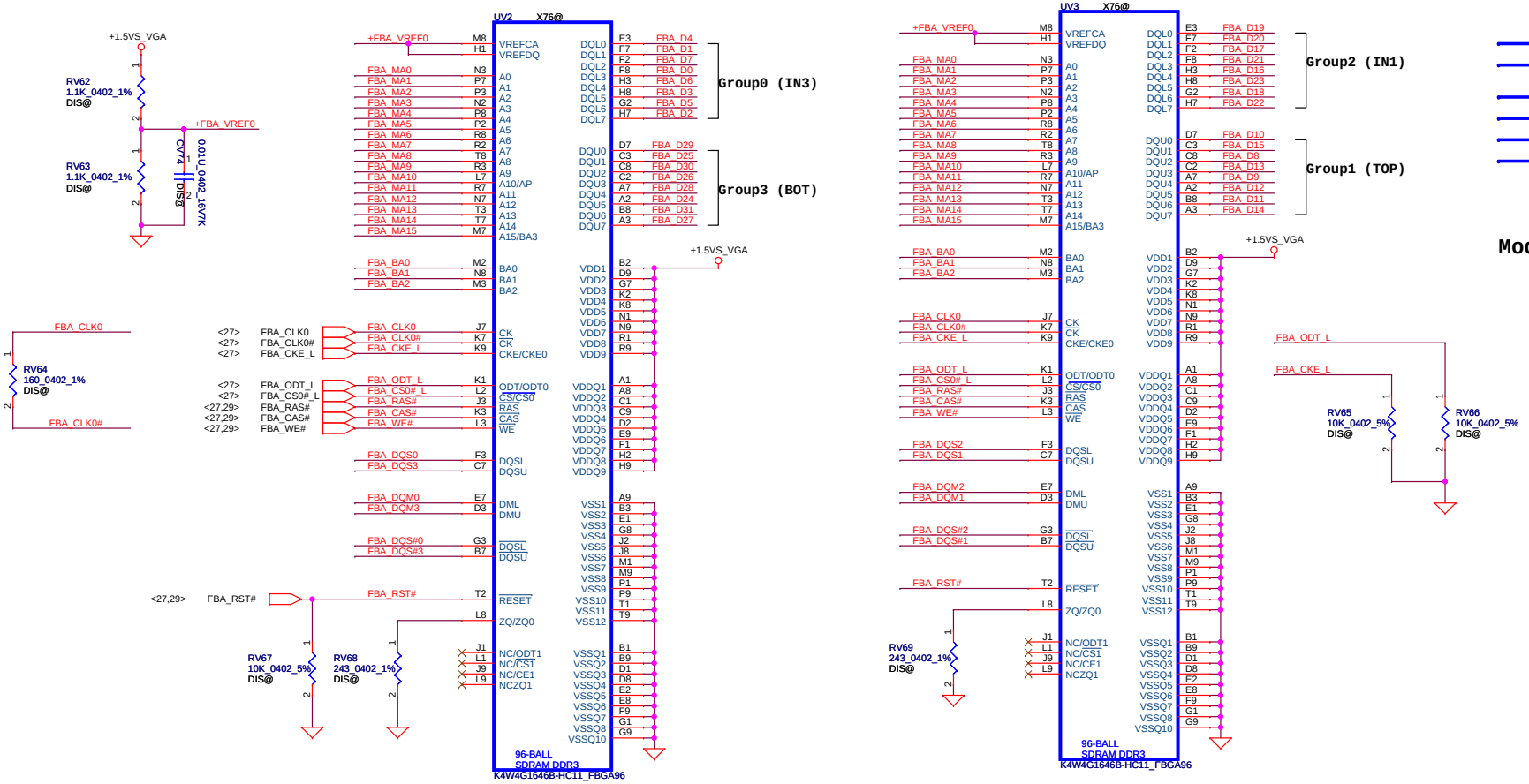
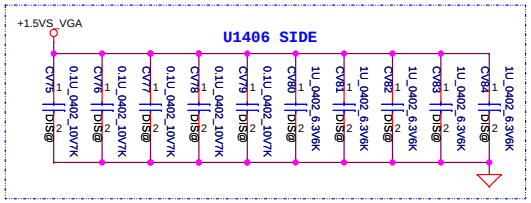
Memory Partition A - Lower 32 bits

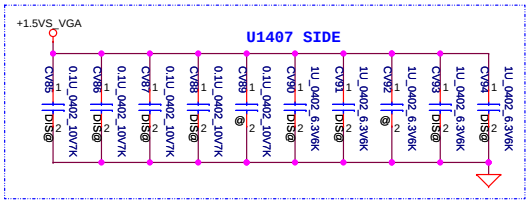


FBA_MA[15..0] <27,29>
FBA_BA[2..0] <27,29>
FBA_D[0..63] <27,29>
FBA_DQM[7..0] <27,29>
FBA_DQS[7..0] <27,29>
FBA_DQS#[7..0] <27,29>

Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#





Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: N14P_DDR3-A LOWER

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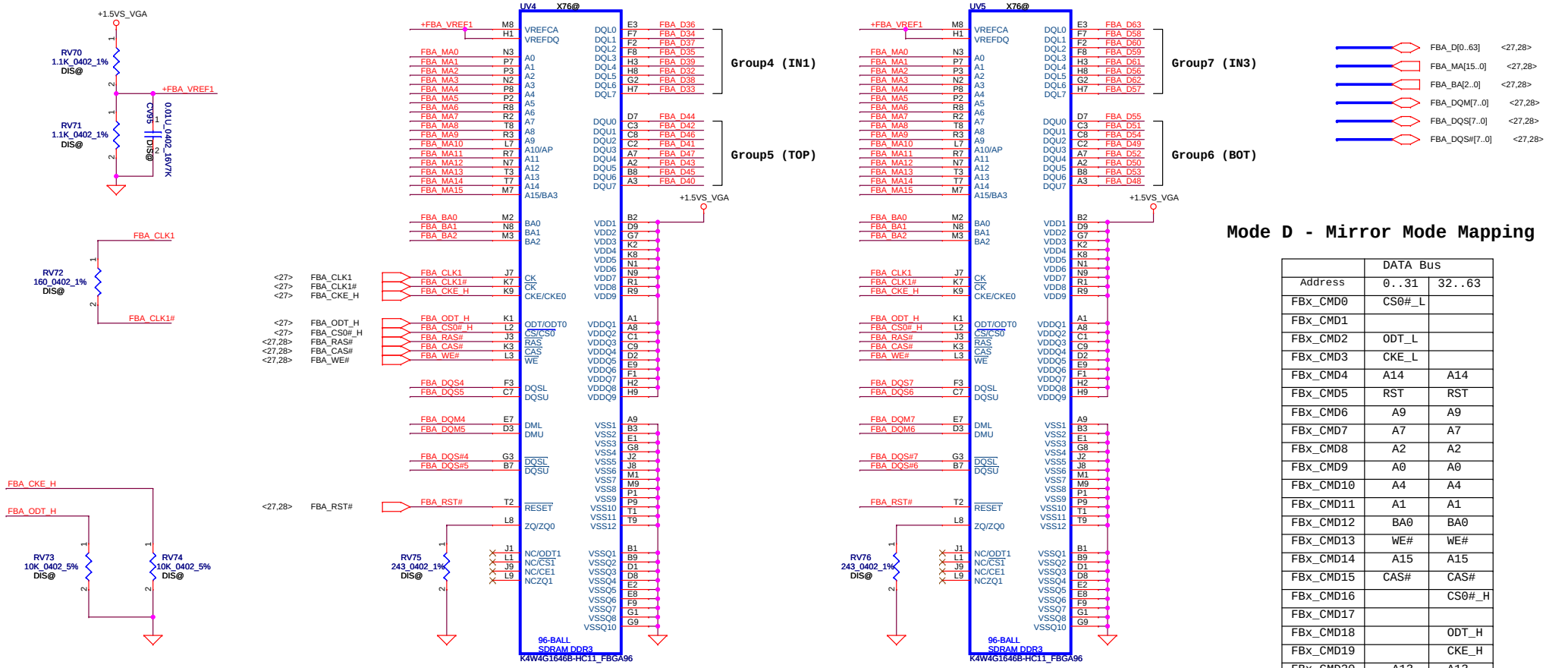
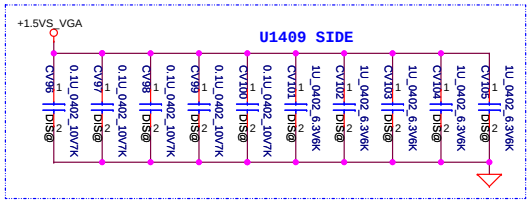
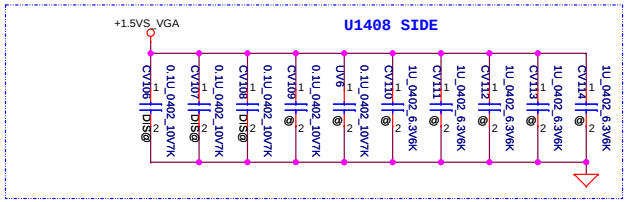
Memory Partition A - Upper 32 bits







Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Title: N14P_DDR3-A UPPER

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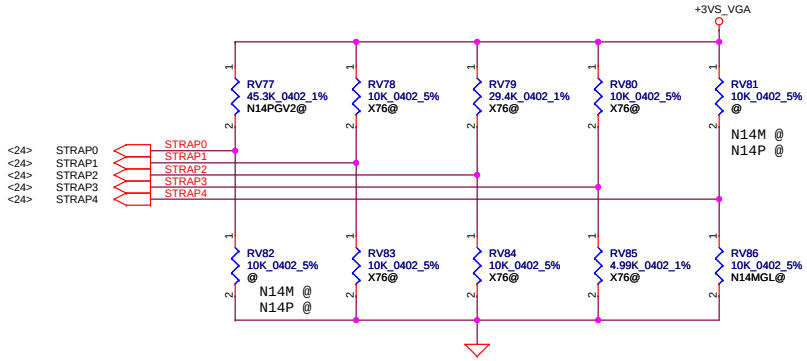

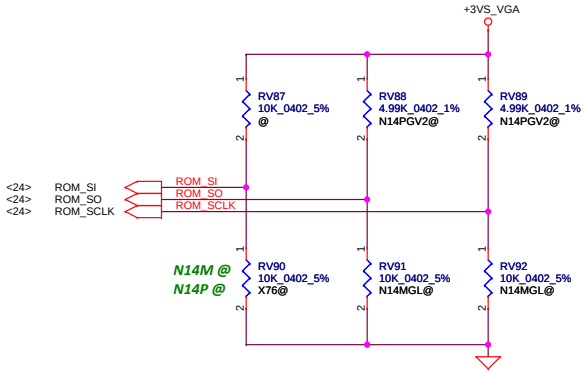

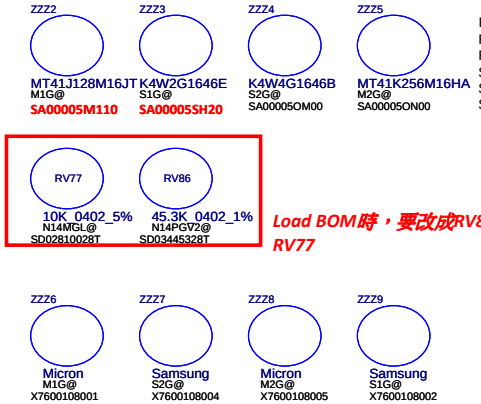

For N14P-GV2 QS Sample
ROM_SO change from PU 10K to PU 5K
ROM_SCLK change from PD 15K to PU 5K
STRAP1 change from PD 5K to PD 45K
STRAP2 change from PU 30K to PD 15K
STRAP4 change from PD 5K to PD 45K

Load BOM時，要改成RV86, RV77

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG[3:0]	
0110	Gen1/Gen2 support only
0000	Gen3 support

FB[1:0]	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

PCIE_MAX_SPEED	
0	Limit booting to PCIE Gen1
1	Allow booting to PCIE Gen 2/3

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_SPEED_CHANGE_GEN3	
0	Disable PCIE Gen3 operation
1	Enable PCIE Gen3 operation

DP_PLL_VDD33V	
0	Reserved
1	Default

Title: N14P_MISC(1/2)

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						X76 RV90	RV77	PU, RV78 PD, RV83	PU, RV79 PD, RV84	PU, RV80 PD, RV85	PD, RV86
	GPU	FB Memory GDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
S2G, X76~04 SA00005OM00 M2G, X76~05 SA00005ON00	N14P-GV2	Samsung 1000MHz	K4W2G1646E-BC1A 128Mx16	PU 5K		PD 45K PD 30K PD 20K PD 10K	PU 45.3K	PD 45.3K	PD 15K	PD 5K	PD 45.3K
		Micron 1000MHz	MT41J128M16JT-093G 128Mx16								
		*Samsung 900MHz	K4W4G1646B-HC11 256Mx16								
		*Micron 900MHz	MT41K256M16HA-107G 256Mx16								

							RV77	PU, RV78 PD, RV83	PU, RV79 PD, RV84	PU, RV80 PD, RV85	PD, RV86
	GPU	FB Memory GDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
S1G, X76~02 SA00005SH20	N14M-GL	*Samsung 1000MHz	K4W2G1646E-BC1A 128Mx16	PD 10K			PU 10K	PD 10K	PU 10K	PD 10K	PD 10K
		Hynix 1000MHz	H5TQ2G63DFR-N0C 128Mx16				PD 10K	PU 10K	PU 10K	PD 10K	
M1G, X76~01 SA00005M110		*Micron 1000MHz	MT41J128M16JT-093G 128Mx16				PU 10K	PD 10K	PD 10K	PD 10K	
		Samsung 900MHz	K4W4G1646B-HC11 256Mx16				PU 10K	PU 10K	PU 10K	PU 10K	
		Hynix 900MHz	H5TQ4G63MFR-11C 256Mx16				PU 10K	PU 10K	PD 10K	PD 10K	
		Micron 900MHz	MT41K256M16HA-107G 256Mx16				PD 10K	PD 10K	PU 10K	PU 10K	

Title: N14P_MISC(2/2)

Size: Custom | Document Number: E540 NM-A161 | Rev: 1.0

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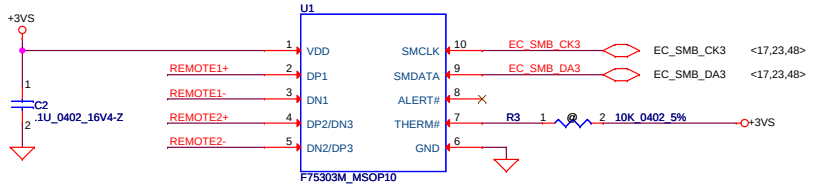
Thermal Sensor

Thermal Sensor
placed near by VRAM

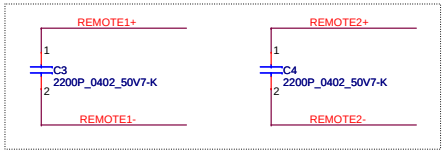


Address 1001_101xb

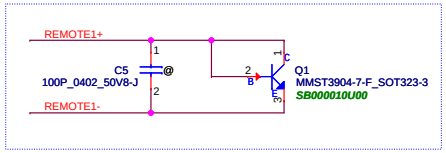
Internal pull up 1.2K to 1.5V

R for initial thermal shutdown temp

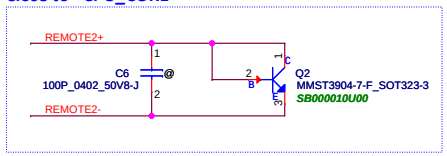
Close to U2



Close to BOTTOM DDR3



Close to +CPU_CORE



REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: THERMAL SENSOR

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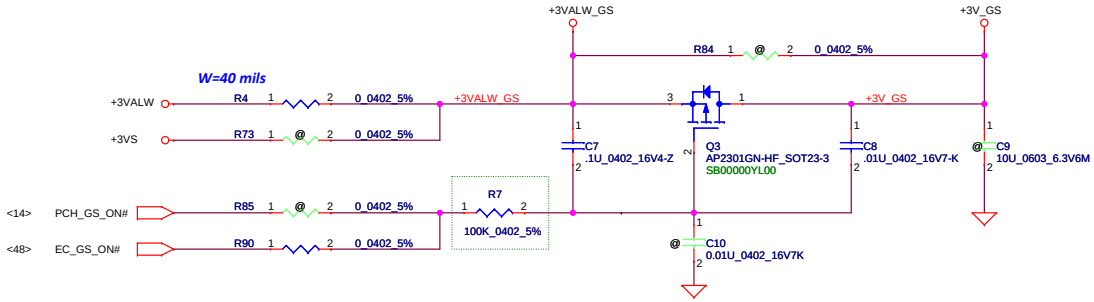
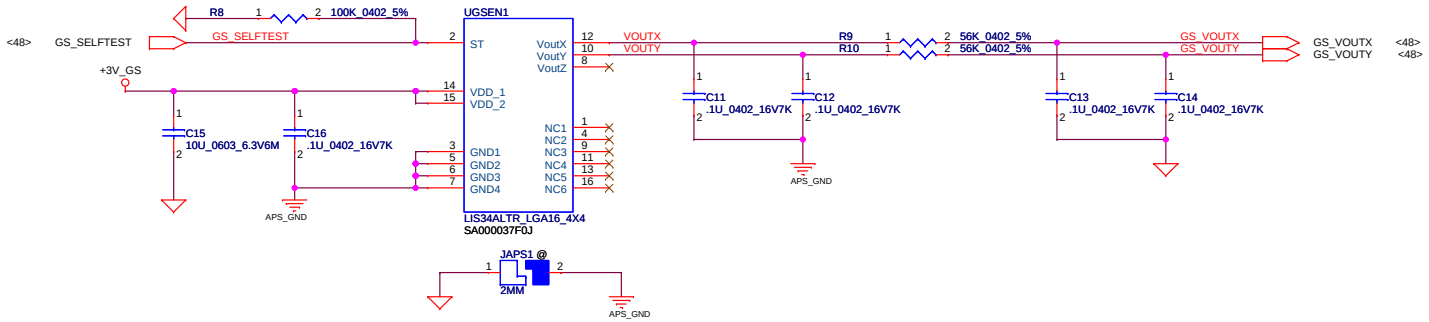
APS G-Sensor





Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: APS G-SENSOR

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

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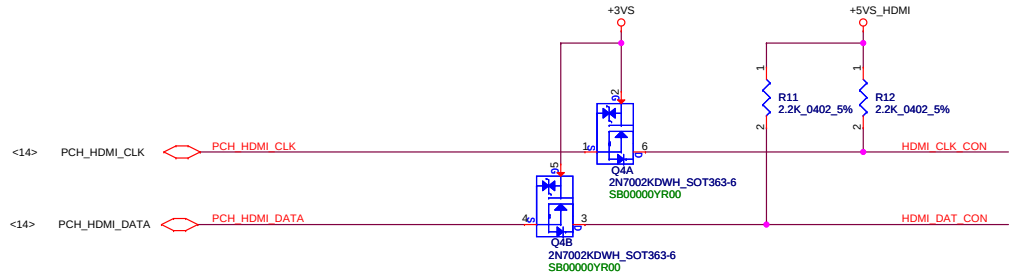
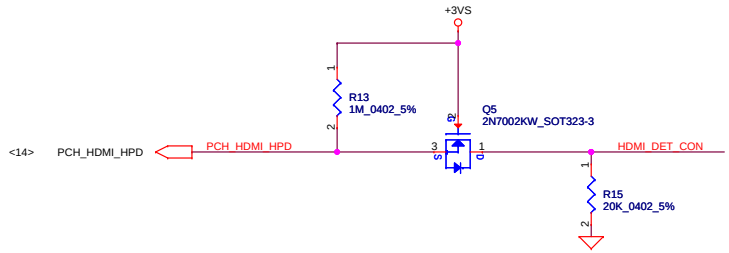
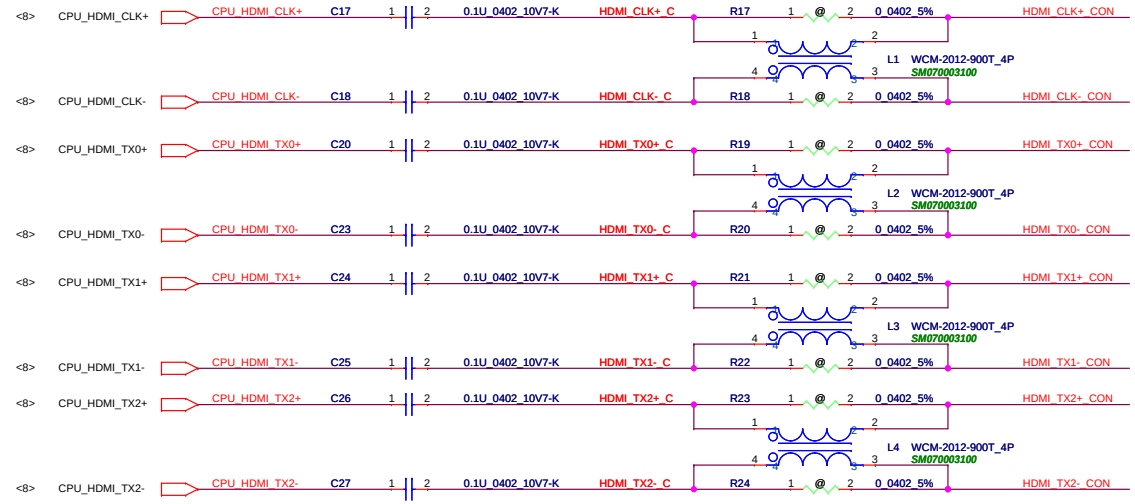
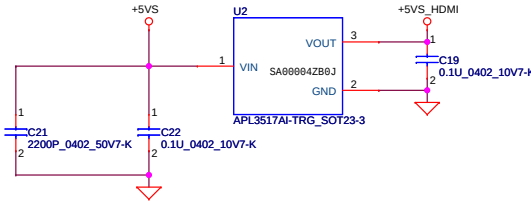
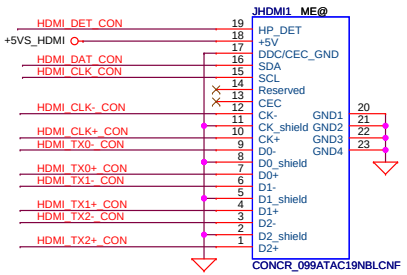


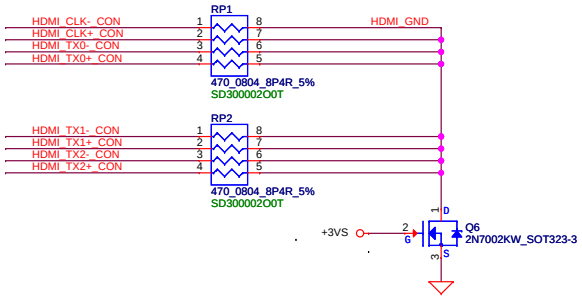




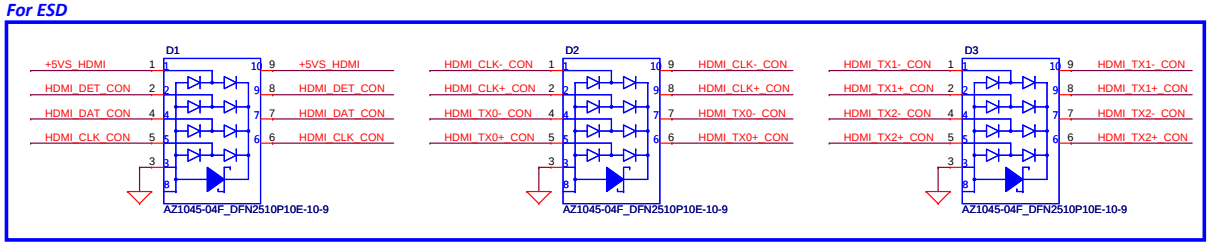


HDMI CONN.





For ESD



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: HDMI CONN.

Size	Document Number	Rev
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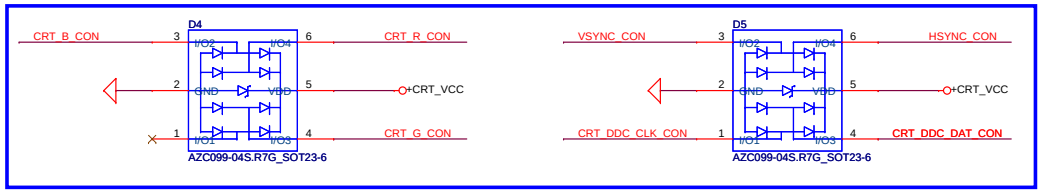
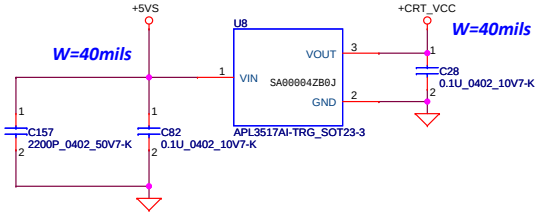
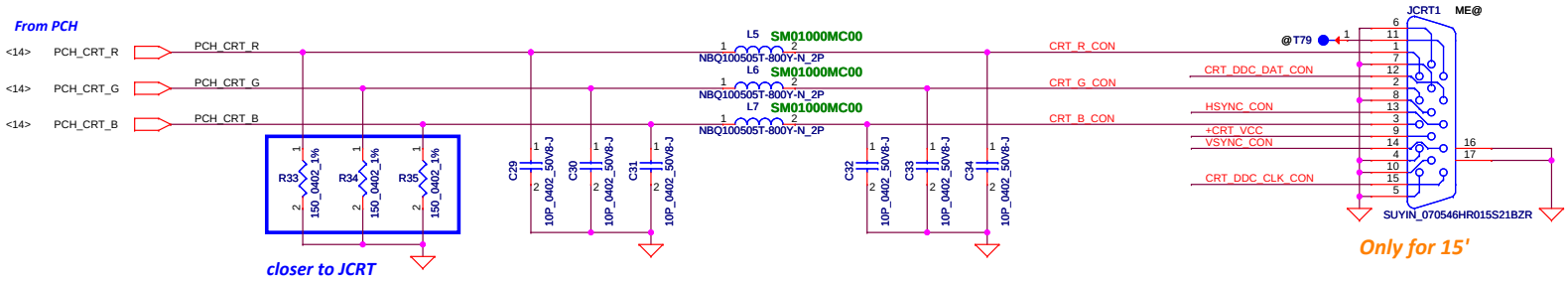
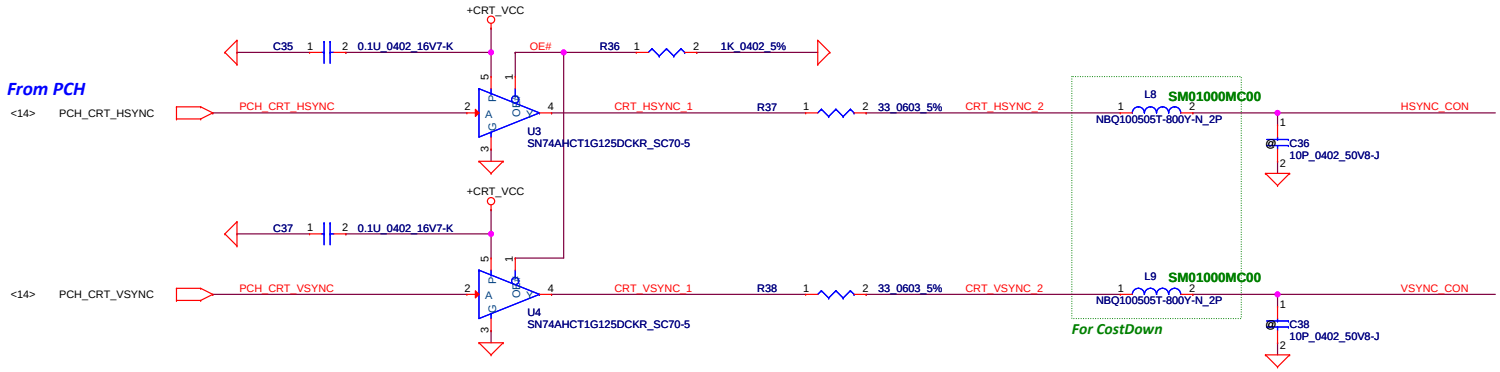


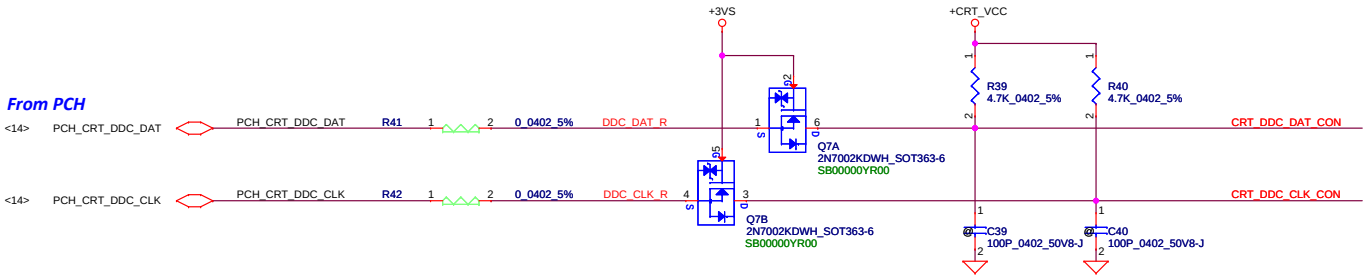
closer to JCRT



CRT Connector







Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title	CRT CONN.		
Size	Document Number		Rev
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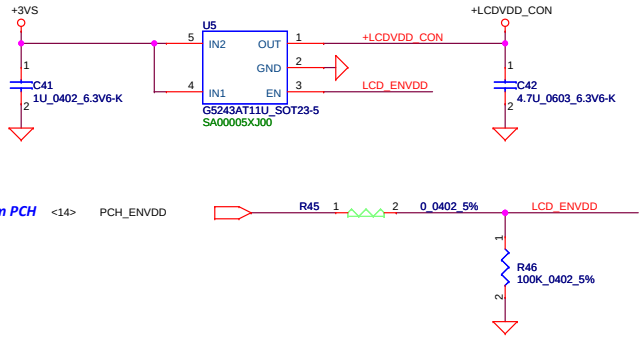
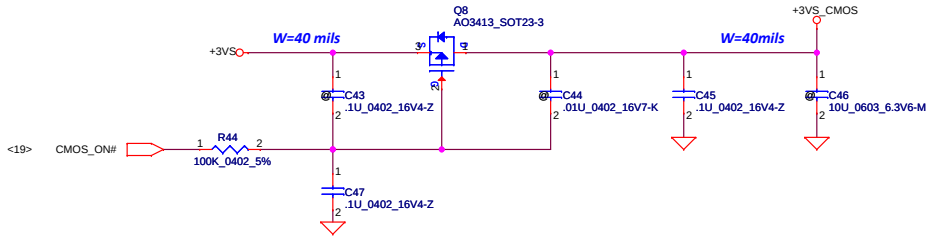
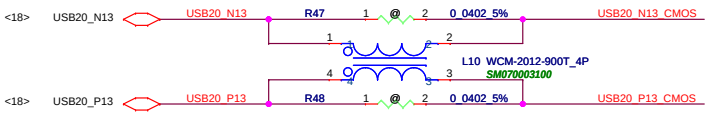
LCDVDD Circuit

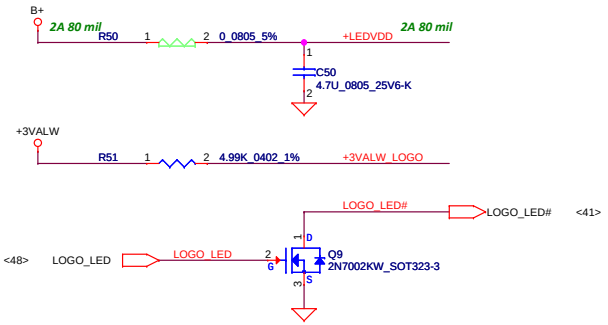


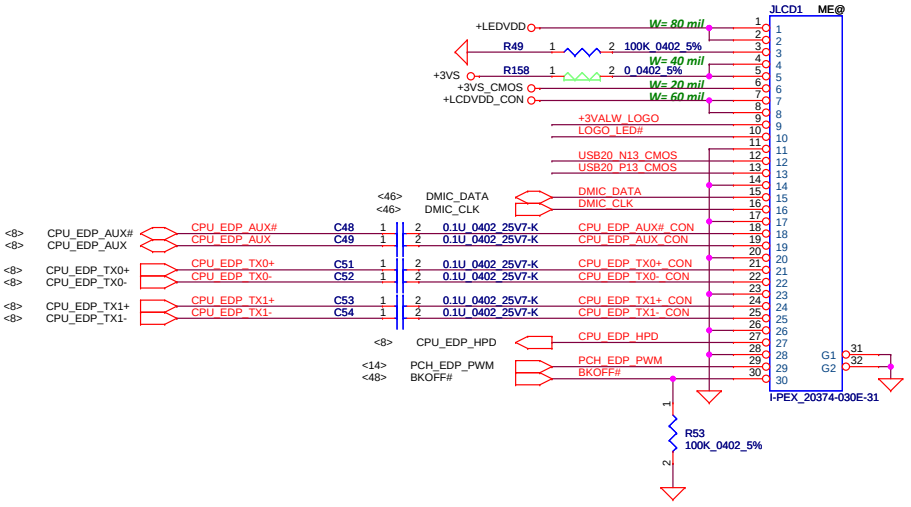
CMOS Camera



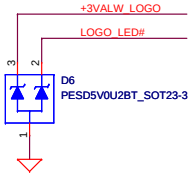
CMOS USB Port10



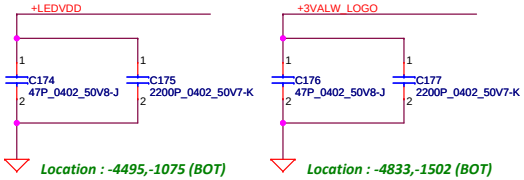




ESD request



EMI



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title	LCD/CMOS CONN.		
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Custom	E440 NM-A151		1.0
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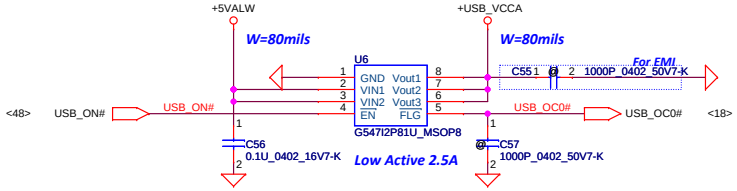
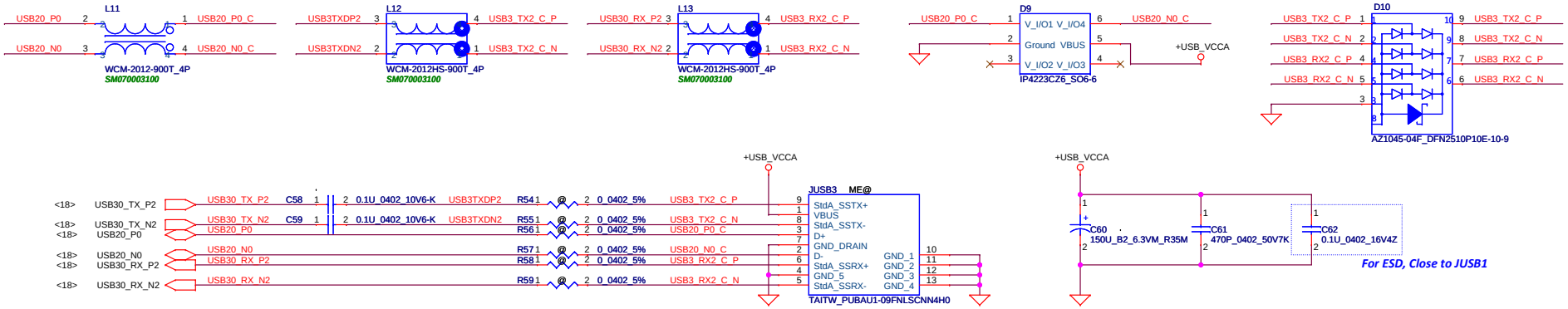
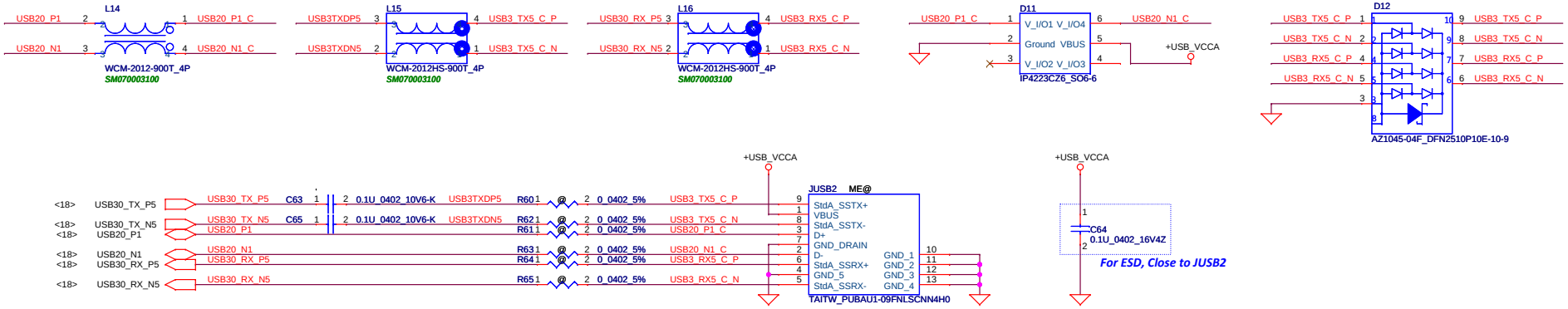


USB30 Front



USB30 Back



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: **USB30 PORT CONN.**

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

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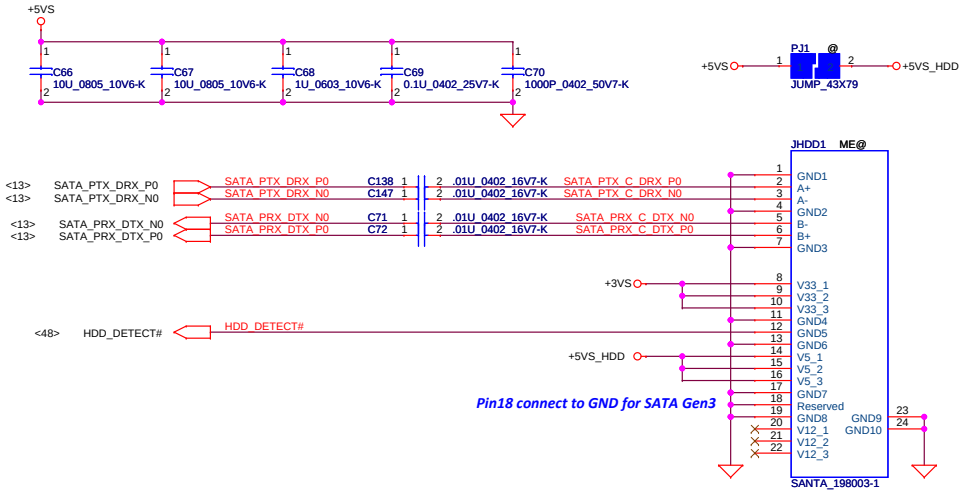
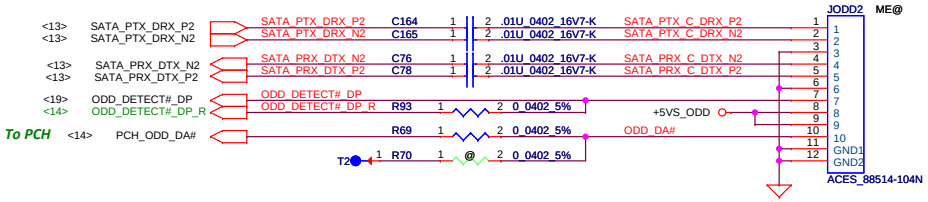
SATA HDD CONN.



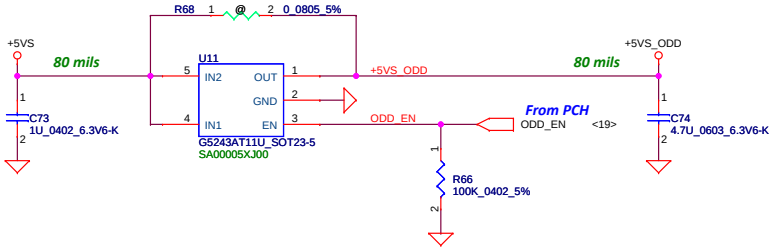
Pin18 connect to GND for SATA Gen3

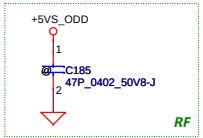
SATA ODD CONN & ODD Power Control



Only for 15"

+5VS TO +5VS_ODD





Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: SATA HDD/ODD CONN.

Size	Document Number	Rev
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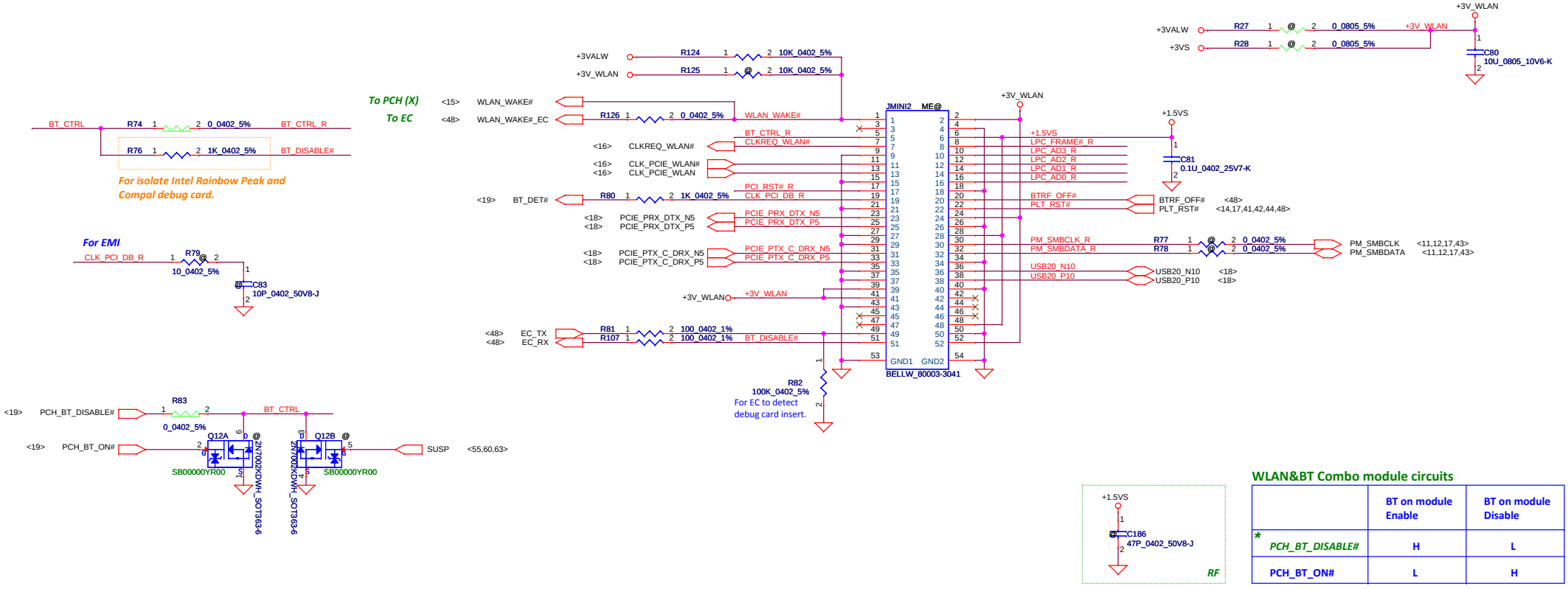
Mini-Express Card(WLAN/WiMAX)



WLAN&BT Combo module circuits

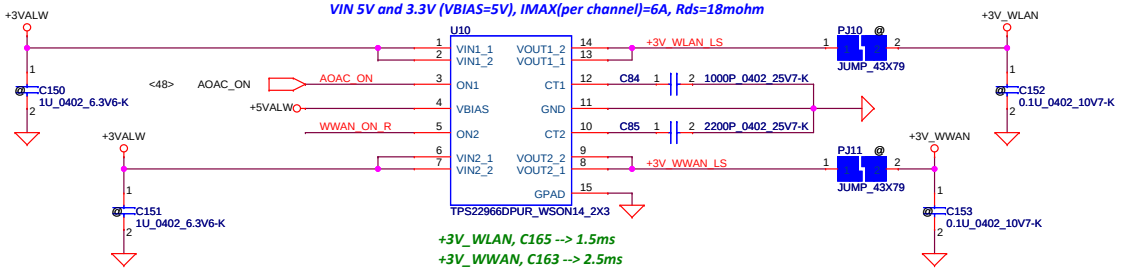
	BT on module Enable	BT on module Disable
* PCH_BT_DISABLE#	H	L
PCH_BT_ON#	L	H

Load Switch

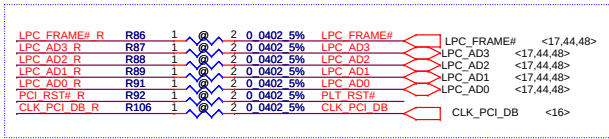
+3VALW To +3V_LAN

+3VALW To +3V_WWAN

1. softstart (RC) will check on EVT PCB
2. if AOAC enable +3V_WLAN always ON
   if AOAC disable +3V_WLAN is same as +3VS



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title	PCIe-WLAN SLOT		
Size	Document Number		Rev
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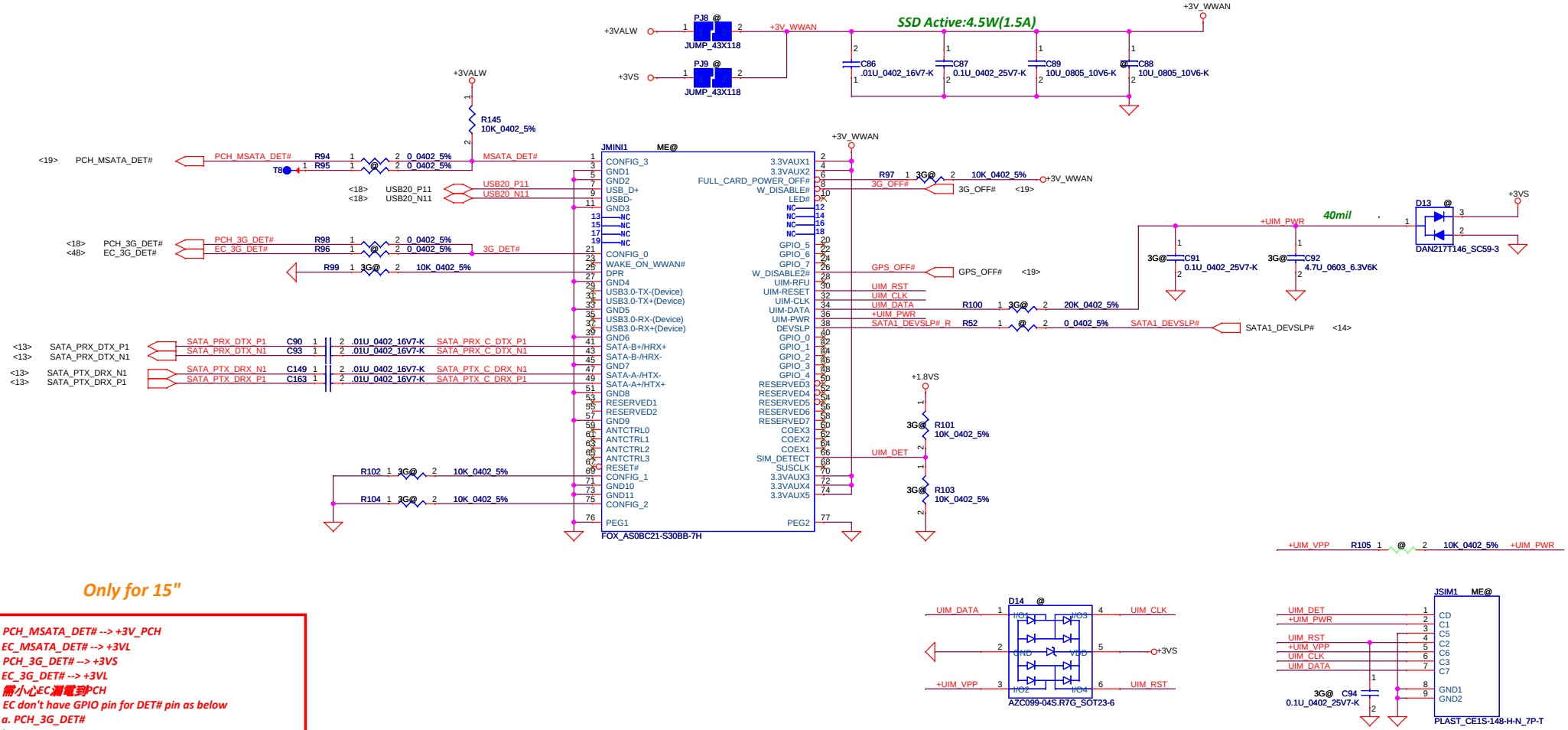
NGFF(SSD) & SIM CARD CONN.



Only for 15"

1. PCH_MSATA_DET# --> +3V_PCH
   EC_MSATA_DET# --> +3VL
2. PCH_3G_DET# --> +3VS
   EC_3G_DET# --> +3VL
   需小心EC漏電到PCH
3. EC don't have GPIO pin for DET# pin as below
   a. PCH_3G_DET#
   b. PCH_MSATA_DET#

NGFF Detect Desc.

	MSATA_DET#	3G_DET#
No Card	1	1
WWAN CARD	1	0
SSD CARD	0	0

Title: PCIe-WWAN/SIM SLOT

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

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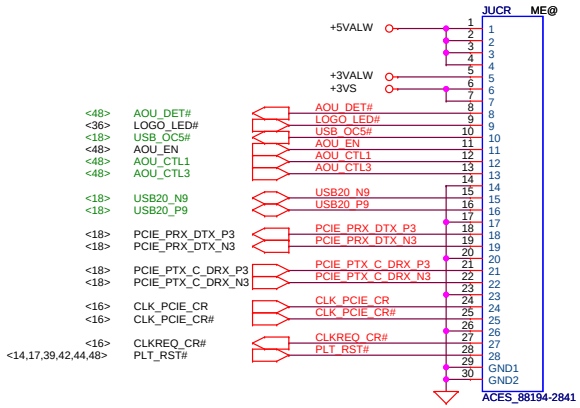
USB2.0, CR & LOGO Board



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: PCIe-CR/USB-Charge CONN.

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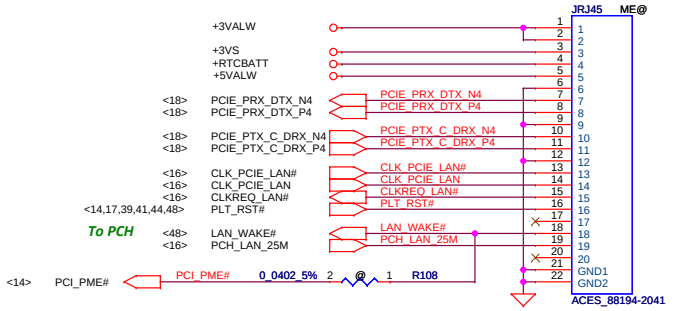
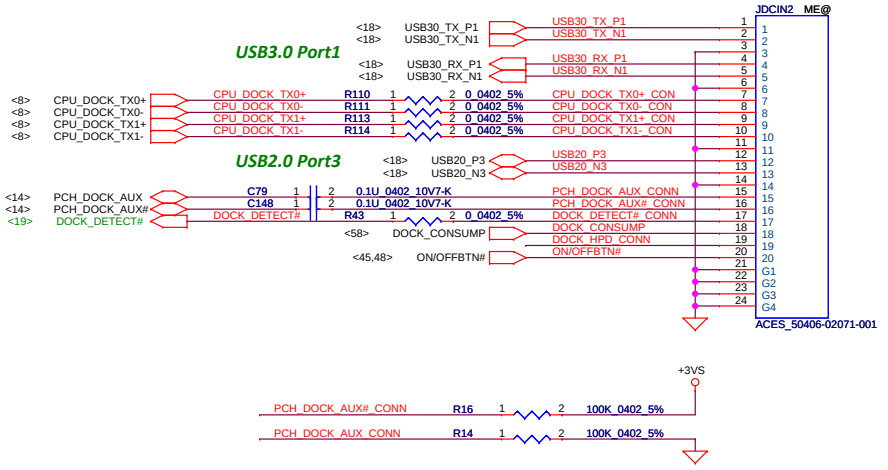
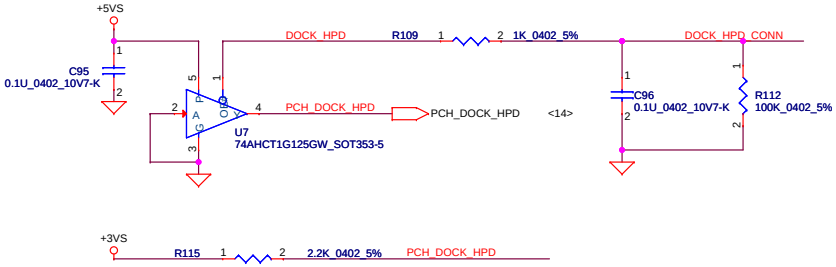
LAN (Port4)
USB3.0/2.0 (Port1/3)
DP(DDIC)

LAN CONN. (FFC)



DCIN CONN. (Coaxial)





Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: PCIe-RJ45/RTC/Docking CON

Size	Document Number	Rev
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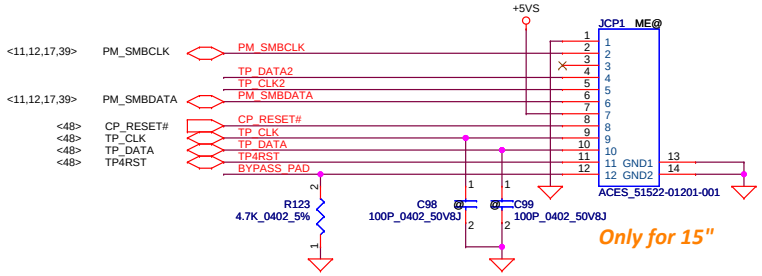
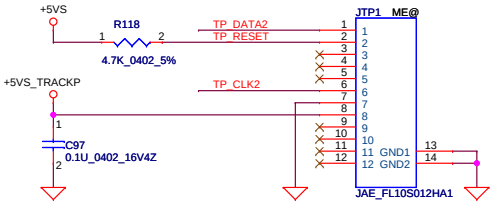
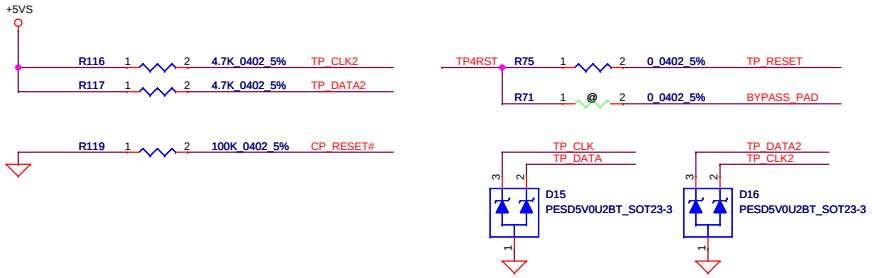
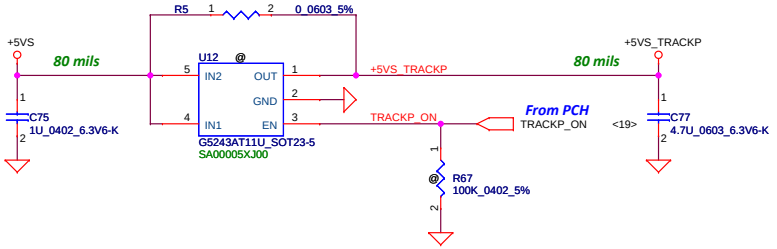
Click Pad



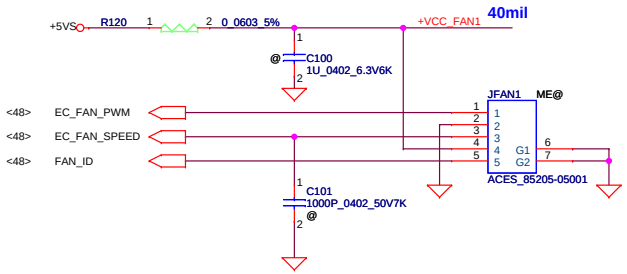
Track point







FAN CONN.



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: CP/TP/FAN CONN.

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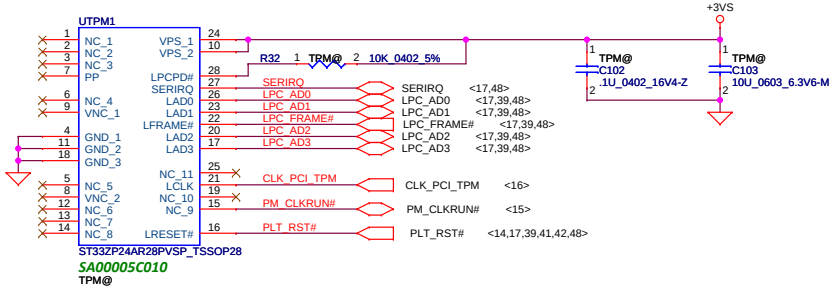
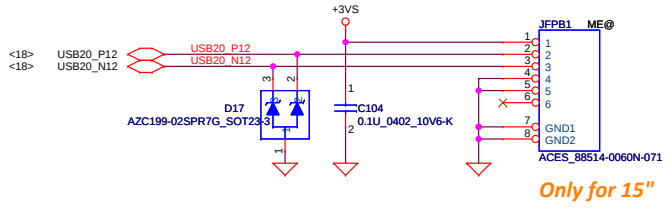
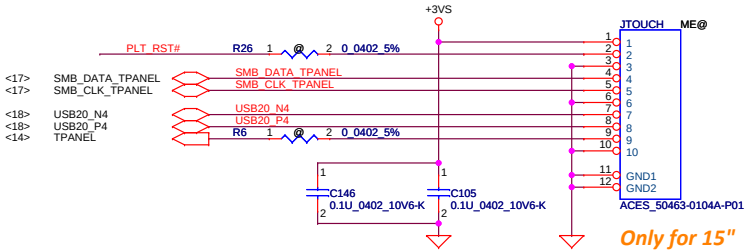
TPM IC



FingerPrint CONN.



Touch Panel CONN.



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title	TPM/TPanel/FP CONN.		
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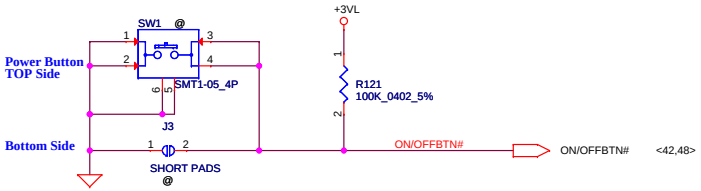
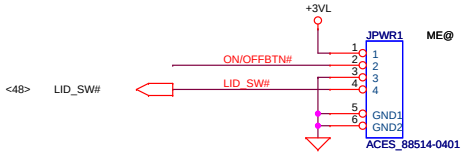
PWR BTN/LID SW CONN.

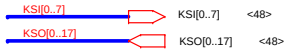
1. Power Button/B link to Function/B Conn. 10pin
2. Lid Switch

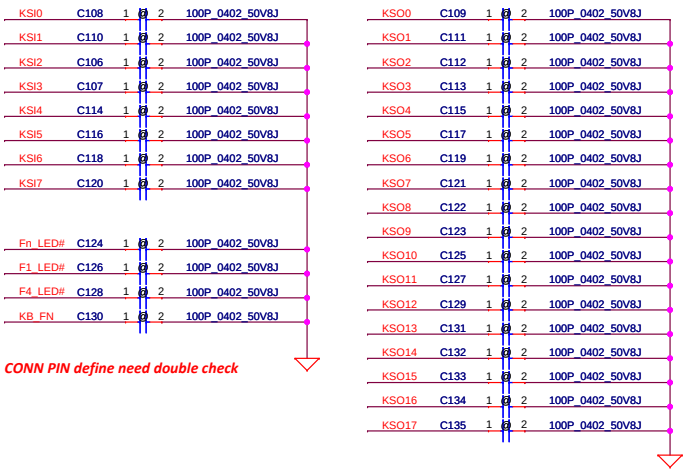
ON/OFF switch



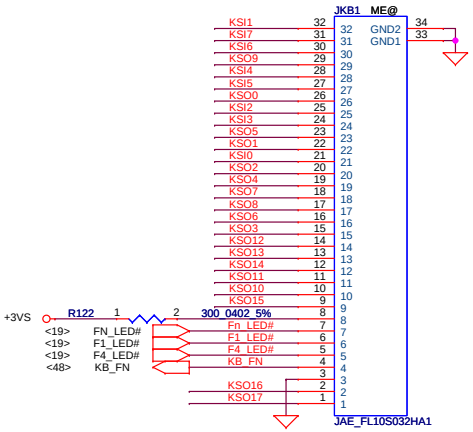


KeyBoard CONN.(14")





CONN PIN define need double check



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: KB/PWR BTN CONN.

Size: Custom | Document Number: E540 NM-A161 | Rev: 1.0

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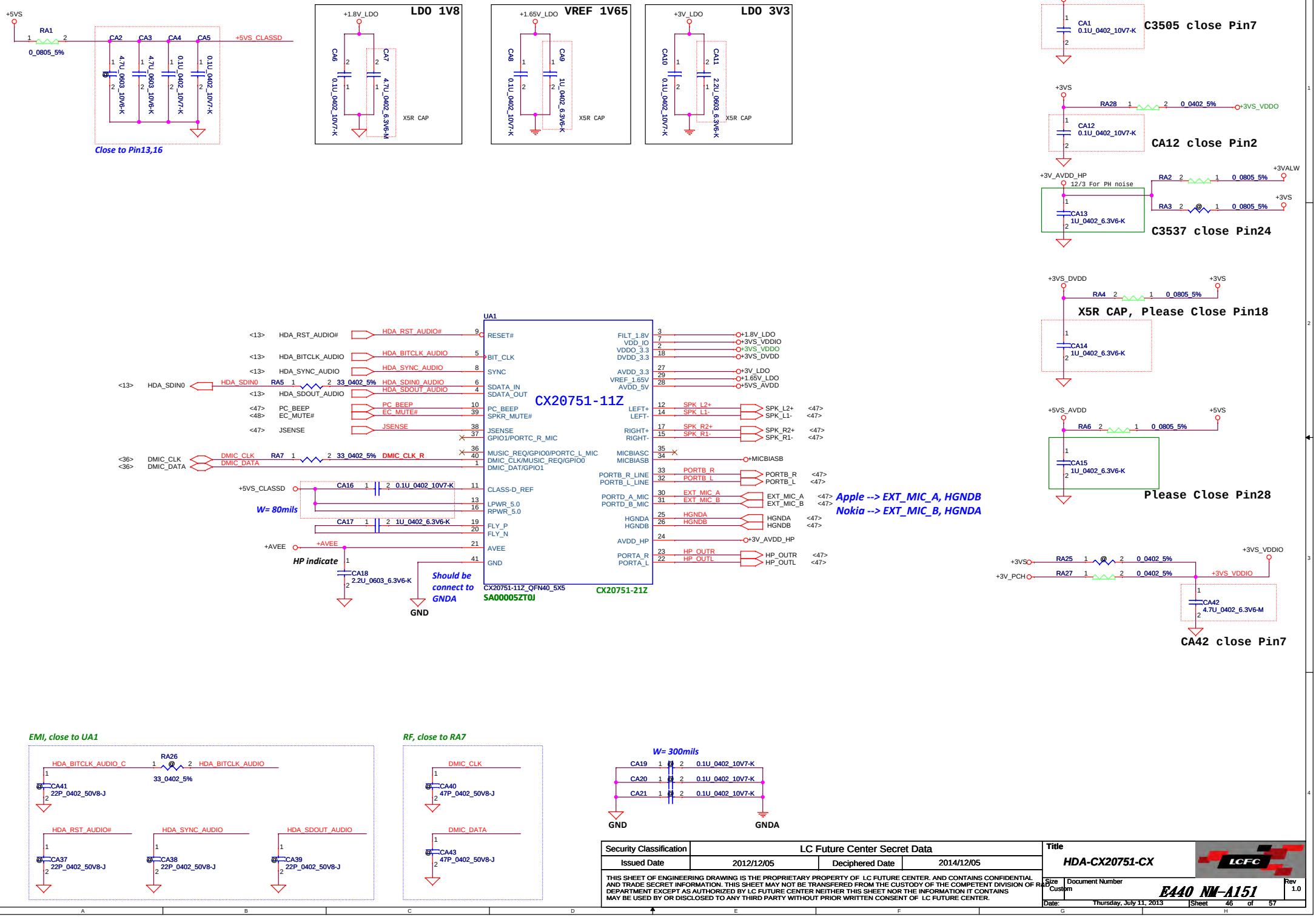

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: HDA-CX20751-CX

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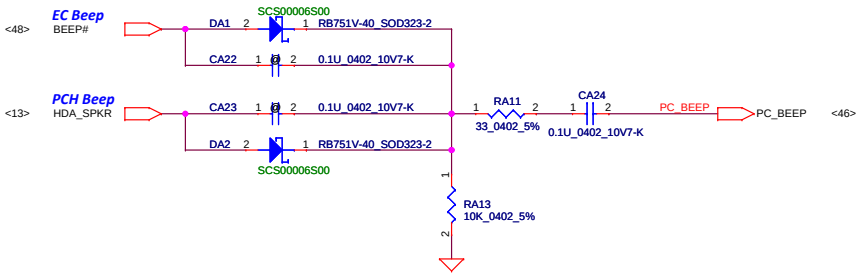
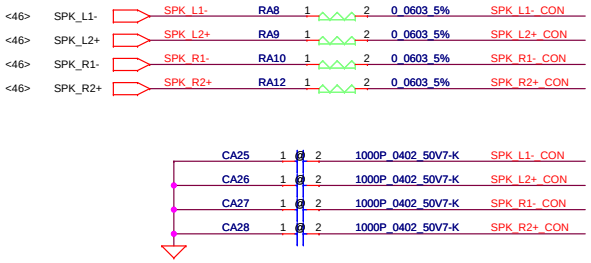
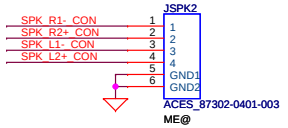
PC Beep



Speaker OUT



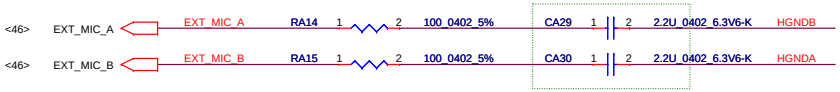
SPK CONN.



Only for 15"

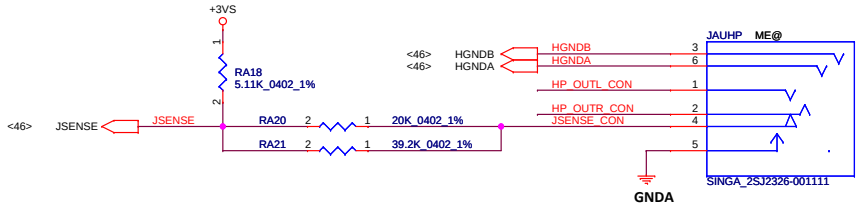
EXT. MIC/LINE IN

Apple --> EXT_MIC_A, HGNDB
Nokia --> EXT_MIC_B, HGNDA

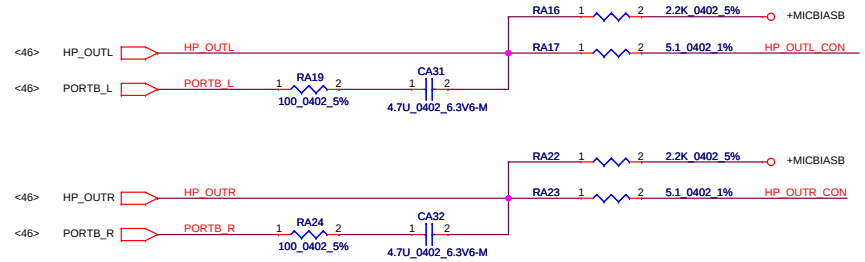


Changed CA29 & CA30 from 1uF to 2.2uF/X5R to meet Port-D(headset-Mic) THD+N <= -65 dB

Audio Jack

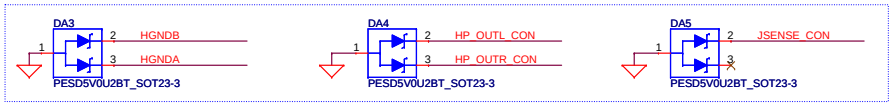


HeadPhone/LINE OUT

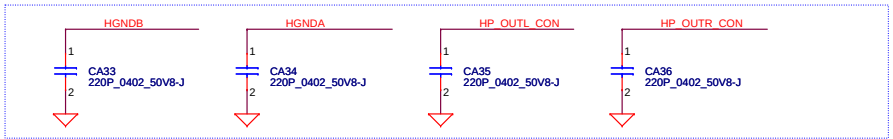


CA31, CA32 change to 4.7U for Quality requirement

ESD Diode, close to JAUHP



EMI, close to JAUHP



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: HDA-HP/EXT MIC/SPK CO

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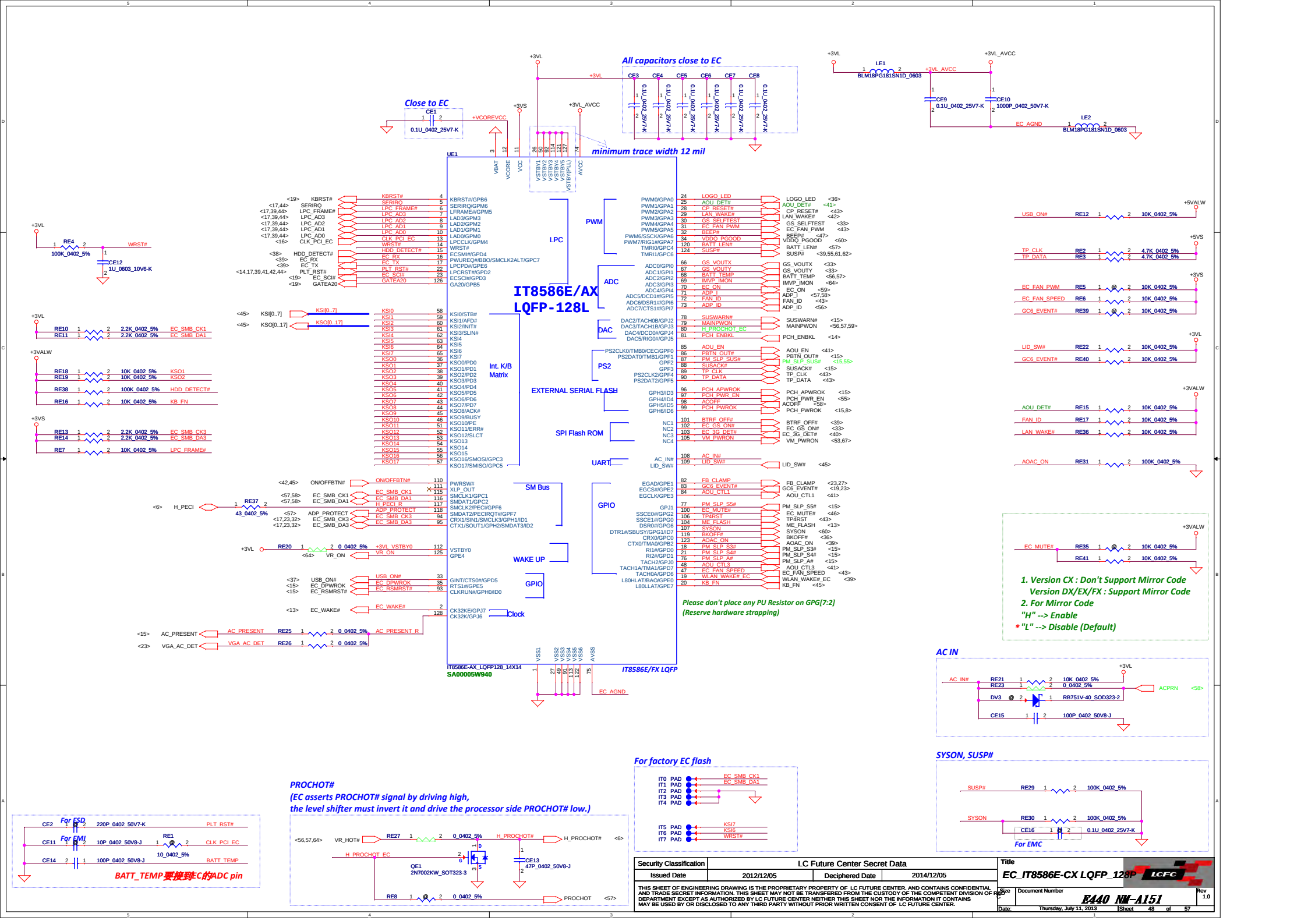

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Issued Date	2012/12/05	Deciphered Date	2014/12/05

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Title: EC_IT8586E-CX LQFP_128P

Size: C | Document Number: E440 NM-A151 | Rev: 1.0

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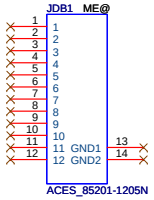

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: BLANK

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

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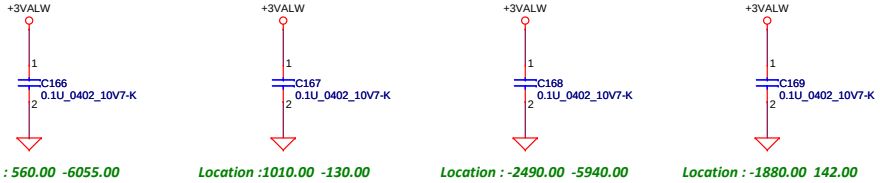
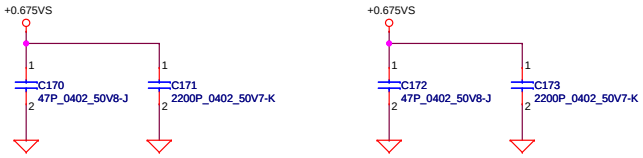


Location : 560.00 -6055.00

Location :1010.00 -130.00

Location : -2490.00 -5940.00

Location : -1880.00 142.00



close to JDDR3L and Pin .203/.204
1. 47P --> Location : -3885,-5914 (BOT)
2. 2200P --> Location : -3885,-5877 (BOT)

close to JDDR3H and Pin .203/.204
1. 47P --> Location : -4198,-5416 (TOP)
2. 2200P --> Location : -4204,-5384 (Top)

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: ***BLANK***

LCFC

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Security Classification	LC Future Center Secret Data		
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Title

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LCFC

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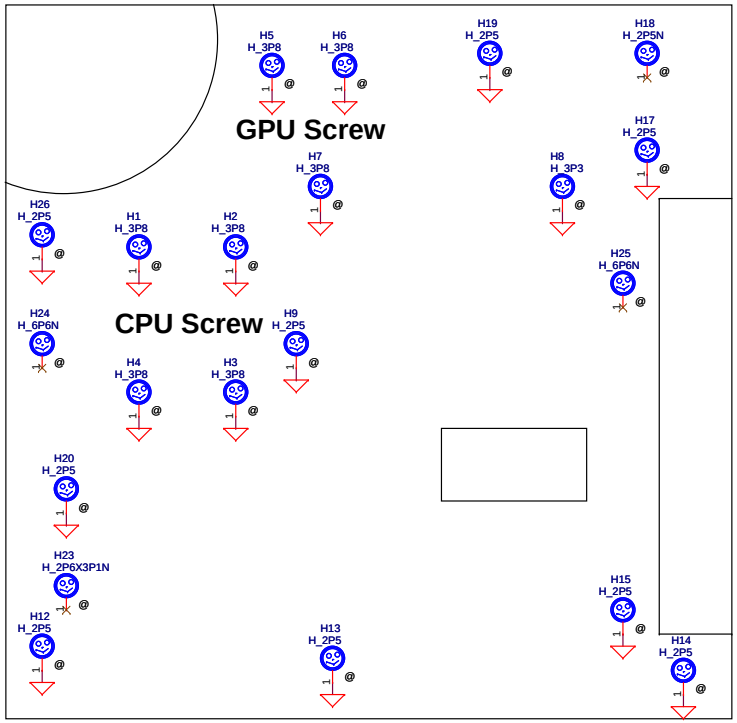
Screw Hole



PCB Fedical Mark PAD

LED3 POWER | LED2 BATTERY | LED1 T/P | LED4 CapsLK | FD1 | FD2 | FD3 | FD4

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: PLM/SCREW HOLE

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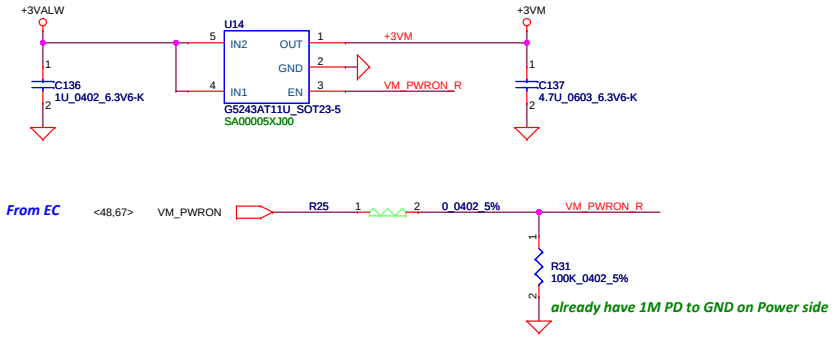
+3VALW to +3VM

FOR SBA Function POWER(always mount)



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: ***ONOFF SW/ PWR-B CONN/ ISPD***

Size: Custom	Document Number: JITR1_LA-4141P ***E540 NM-A161***	Rev: 1.0
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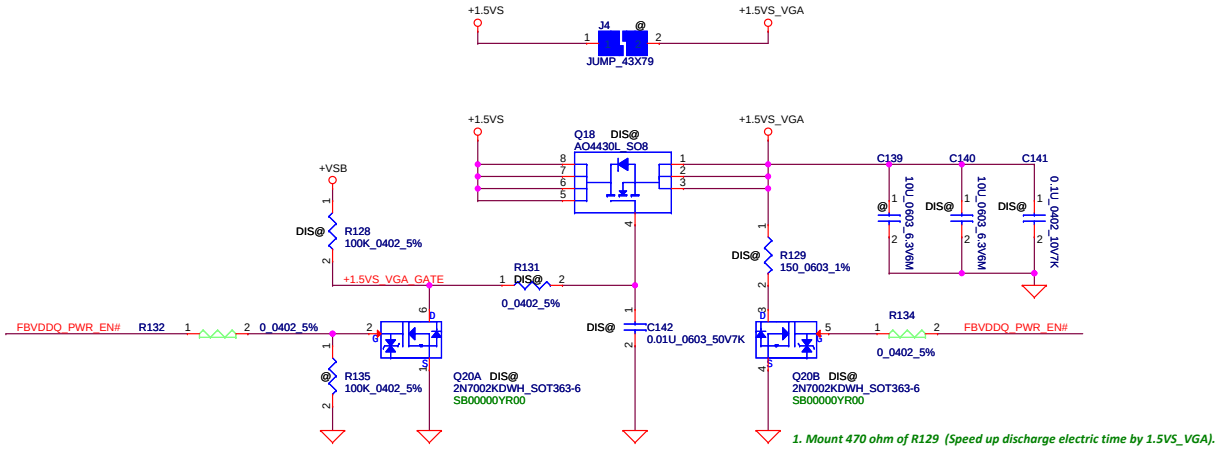
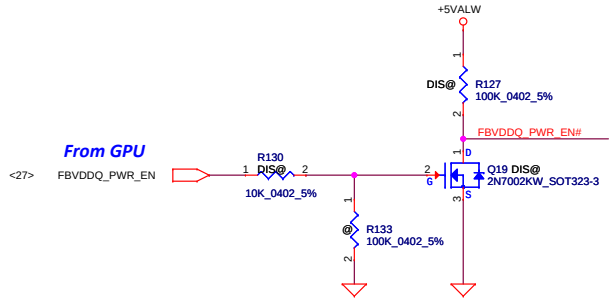
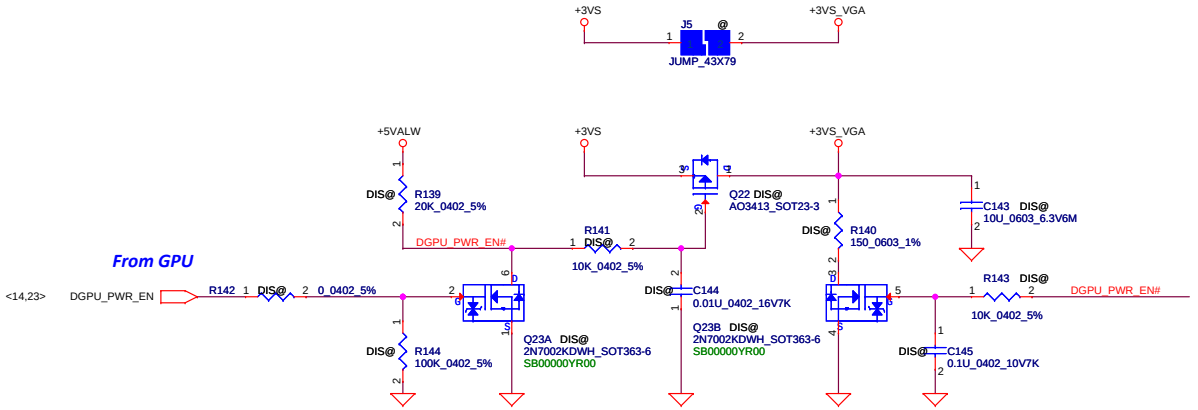
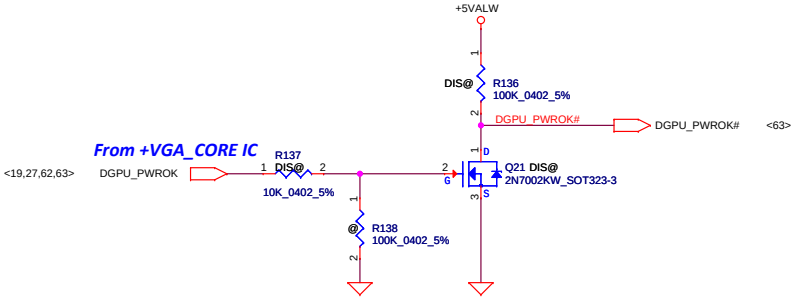
+1.5V to +1.5VS_VGA





+3VS to +3VS_VGA





Power Up -->

+3VS_VGA (En:DGPU_PWR_EN)

+VGA_CORE (En:NVDD_PWR_EN, POK:DGPU_PWROK)

+1.5VS_VGA (En:FBVDDQ_PWR_EN# = FB_CLAMP and DGPU_PWROK)

+1.05VS_VGA (En:DGPU_PWROK#)

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: DOCKING USB30/DP

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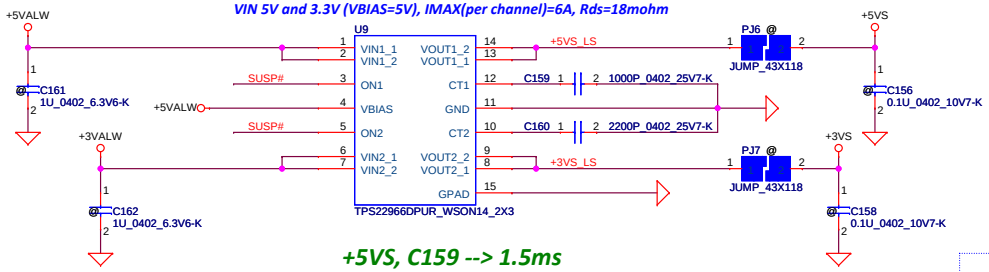
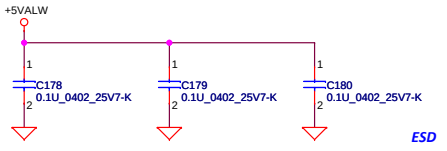
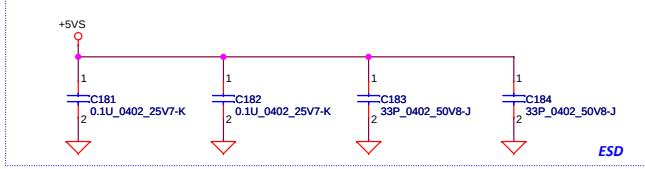
Load Switch
+5VALW To +5VS
+3VALW To +3VS

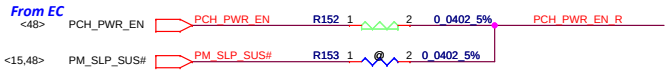


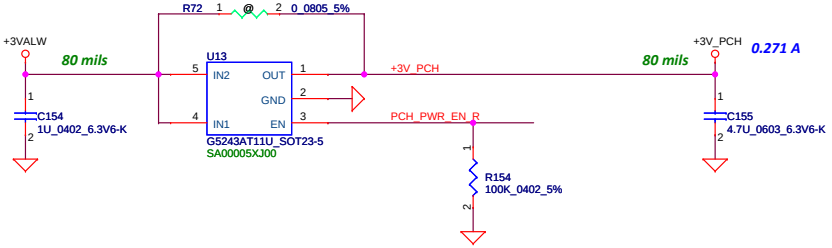
+5VS, C159 --> 1.5ms
+3VS, C160 --> 2.5ms



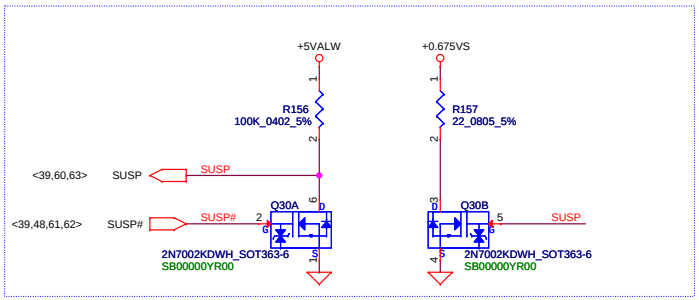


+3VALW To +3V_PCH





For DisCharge



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: DC V TO V/VS INTERFACE

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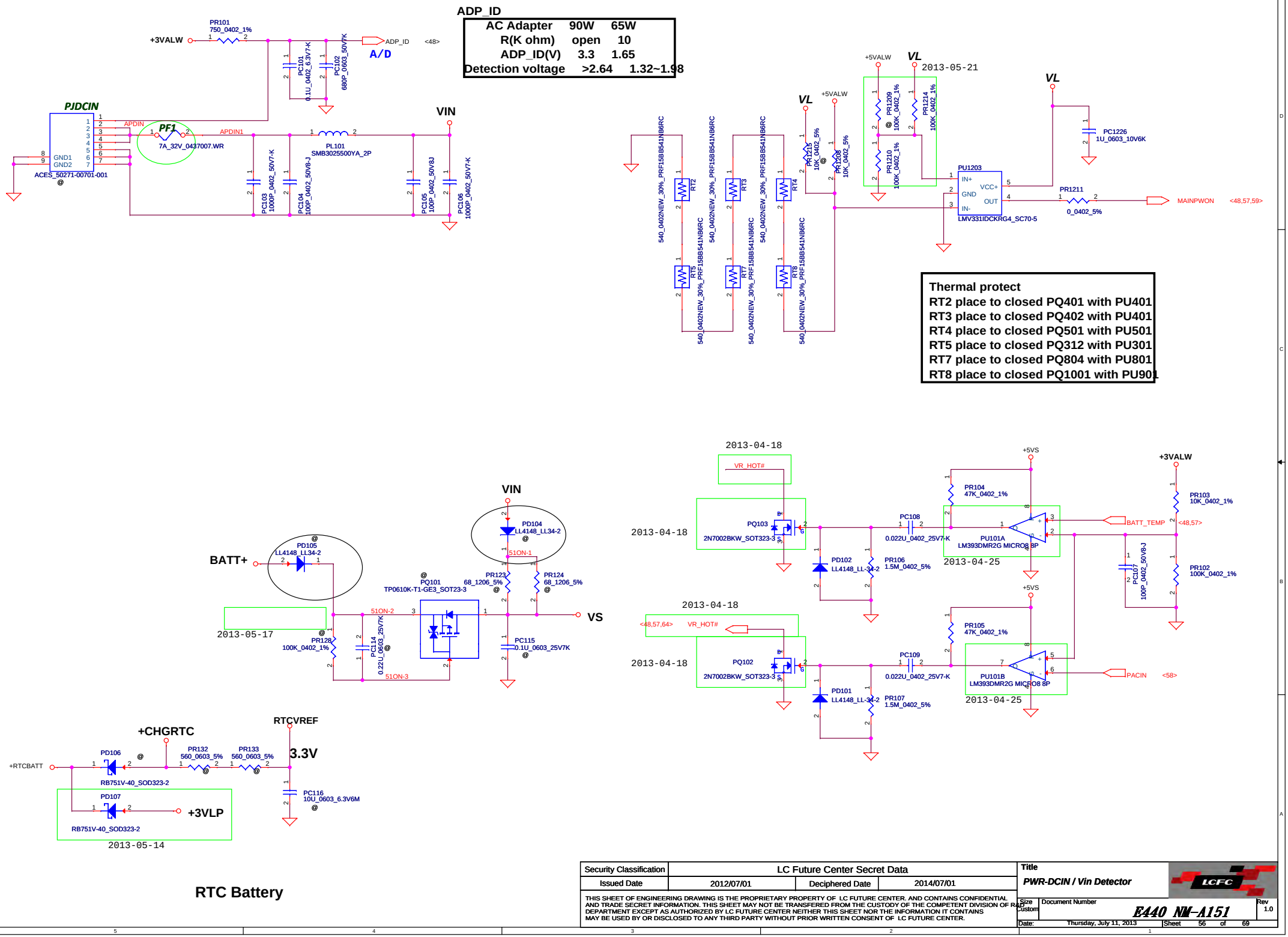
ADP_ID
AC Adapter 90W 65W
R(K ohm) open 10
ADP_ID(V) 3.3 1.65
Detection voltage >2.64 1.32~1.98
PR101 750_0402_1%
+3VALW
ADP_ID <48>
A/D
PC101 0.1U_0402_6.3V7-K
PC102 680P_0603_50V7K
PJDCIN
APDIN
PF1
7A_32V_0437007.WR
APDIN1
PL101 SMB3025500YA_2P
VIN
GND1
GND2
ACES_50271-00701-001
PC103 1000P_0402_50V7-K
PC104 100P_0402_50V8-J
PC105 100P_0402_50V8J
PC106 1000P_0402_50V7-K
VL
+5VALW
2013-05-21
PR1209 100K_0402_1%
PR1214 100K_0402_1%
PR1210 100K_0402_1%
PC1225 10K_0402_5%
PC1226 1U_0603_10V6K
PU1203
IN+
GND
IN-
VCC+
OUT
LMV331IDCKRG4_SC70-5
PR1211 0_0402_5%
MAINPWON <48,57,59>
RT2
RT3
RT4
RT5
RT7
RT8
540_0402NEW_30%_PRF15BB541N86RC
Thermal protect
RT2 place to closed PQ401 with PU401
RT3 place to closed PQ402 with PU401
RT4 place to closed PQ501 with PU501
RT5 place to closed PQ312 with PU301
RT7 place to closed PQ804 with PU801
RT8 place to closed PQ1001 with PU901
2013-04-18
VR_HOT#
PQ103
2N7002BKW_SOT323-3
PC108 0.022U_0402_25V7-K
PR104 47K_0402_1%
PU101A
LM393DMR2G MICRO8 8P
2013-04-25
PD102 LL4148_LL-34-2
PR106 1.5M_0402_5%
+5VS
+3VALW
PR103 10K_0402_1%
BATT_TEMP <48,57>
PC107 100P_0402_50V8-J
PR102 100K_0402_1%
PQ102
PC109 0.022U_0402_25V7-K
PR105 47K_0402_1%
PU101B
PACIN <58>
PD101 LL4148_LL-34-2
PR107 1.5M_0402_5%
<48,57,64>
VIN
PD104 LL4148_LL34-2
51ON-1
PD105 LL4148_LL34-2
BATT+
PQ101 TP0610K-T1-GE3_SOT23-3
PR123 68_1206_5%
PR124 68_1206_5%
51ON-2
51ON-3
VS
PR128 100K_0402_1%
PC114 0.22U_0603_25V7K
PC115 0.1U_0603_25V7K
2013-05-17
RTCVREF
+CHGRTC
3.3V
PD106
PR132 560_0603_5%
PR133 560_0603_5%
+RTCBATT
RB751V-40_SOD323-2
PD107
+3VLP
PC116 10U_0603_6.3V6M
2013-05-14
RTC Battery
Security Classification
LC Future Center Secret Data
Issued Date
2012/07/01
Deciphered Date
2014/07/01
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Title
PWR-DCIN / Vin Detector
LCFC
Size
Custom
Document Number
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Rev
1.0
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PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

JBATT1
SUYIN_200082GR007M211ZR
2011_0823
change 9P JBATT1

VMB2
PF201 12A_65V_451012MRL
VMB
PL201 SMB3025500YA_2P
PR223 0.01_1206_1%
BATT+
EC_SMDA
EC_SMCA
PC201 1000P_0402_50V7K
PC202 0.01U_0402_25V7K
DCP
DCN
PESD5V0U2BT_SOT23-3
PD805
PR202 100_0402_1%
PR201 100_0402_1%
EC_SMB_CK1 <48,58>
EC_SMB_DA1 <48,58>
PR203 100K_0402_1%
+3VALW
A/D
PR204 750_0402_5%
<BOM Structure>
BATT_TEMP <48,56>
PESD5V0U2BT_SOT23-3
PD806

VL
PC203 0.1U_0603_16V7K
+3VS
PU201
VCC TMSNS1
GND RHYST1
OT1 TMSNS2
OT2 RHYST2
G718TM1U_SOT23-8
PR209 100K_0402_1%
<48,58,64> VR_HOT#
PQ201 2N7002BKW_SOT323-3
ADP_OCP_1
OTP_N_003
PR212 @ 0_0402_5%
<48> PROCHOT
PR213 0_0402_5%
MAINPWON <48,56,59>
OTP_N_002
Turbo_V_1
ADP_OCP_2
PR210 27.4K_0402_1%
<48,58> ADP_I
PR205 4.42K_0402_1%
PR227 2.1K_0402_1%
PQ206 2N7002BKW_SOT323-3
ADP_PROTECT <48>
NTC_V_1
PR206 12.7K_0402_1%
PR207 30K_0402_1%
PR208 499K_0402_1%
PR230 0_0402_5%
PR228 0_0402_5%
PR229
PR211 10K_0402_1%
PR231 47K_0402_1%
PR232 47K_0402_1%
PH201 100K_0402_1%_NCP15WF104J03RC
+3VLP
+3VALW
2013-04-18
2013-07-08
2013-05-23
@ T135 Turbo_V
@ T136 NTC_V

PR248 0_0402_5%
VCP
PU102
REF OUT
GND IN-
V+ IN+
INA199A1DCKR_SC70-6
PR247 150K_0402_1%
PR246 100K_0402_1%

2011_0731 add circuit for battery learning function
2011_1119 change circuit to unmount from mount

P2
VMB2
PR224 255K_0402_1%
PR219 10K_0402_1%
PR221 150K_0402_1% <BOM Structure>
PC207 .01U_0402_25V7-K
PR218 10M_0402_5%
PU202A
LM393DMR2G MICRO8 8P
2013-04-25
PR222 100K_0402_1%
PR220 100K_0402_1%
PQ204 2N7002BKW_SOT323-3
PR226 100K_0402_1%
PQ205 2N7002BKW_SOT323-3
2013-04-18
PR225 10K_0402_1%
<48> BATT_LEN#

+1.05VS
PC214 0.1U_0402_25V6
PC212 0.1U_0402_25V6
PC213 0.1U_0402_25V6
PR250
PR251 1K_0402_1%
PC215 0.1U_0402_25V6
PR249 10K_0402_1%
2013-05-15
BATT_OUT <58>
VR_HOT#
MAINPWON
PR255 0_0402_5%
PR254 0_0402_5%
PVIN2 PG LX1
PVIN1 LX2
SVIN1 LX3
END GND NC FB
PU203 RT9553
PR257 13K_0402_1%
PR260 20K_0402_1%
PR261 374K_0402_1%
PR252 10K_0402_1%
PR253 10K_0402_1%
PR259 20K_0402_1%
PR258 10K_0402_1%
PR256 2.2_0402_5%
PC218 0.1U_0402_25V6

PQ202 TP0610K-T1-GE3_SOT23-3
B+
+VSBP
PC205 0.1U_0603_25V7K
PR214 100K_0402_1%
PC204 0.22U_0603_25V7K
PR215 22K_0402_1%
PJ201 JUMP_43X39
+VSB
VL
PR216 100K_0402_1%
PR217 1K_0402_5%
<59> SPOK
PQ203 2N7002BKW_SOT323-3
PC206 1U_0402_10V6K
2013-04-18

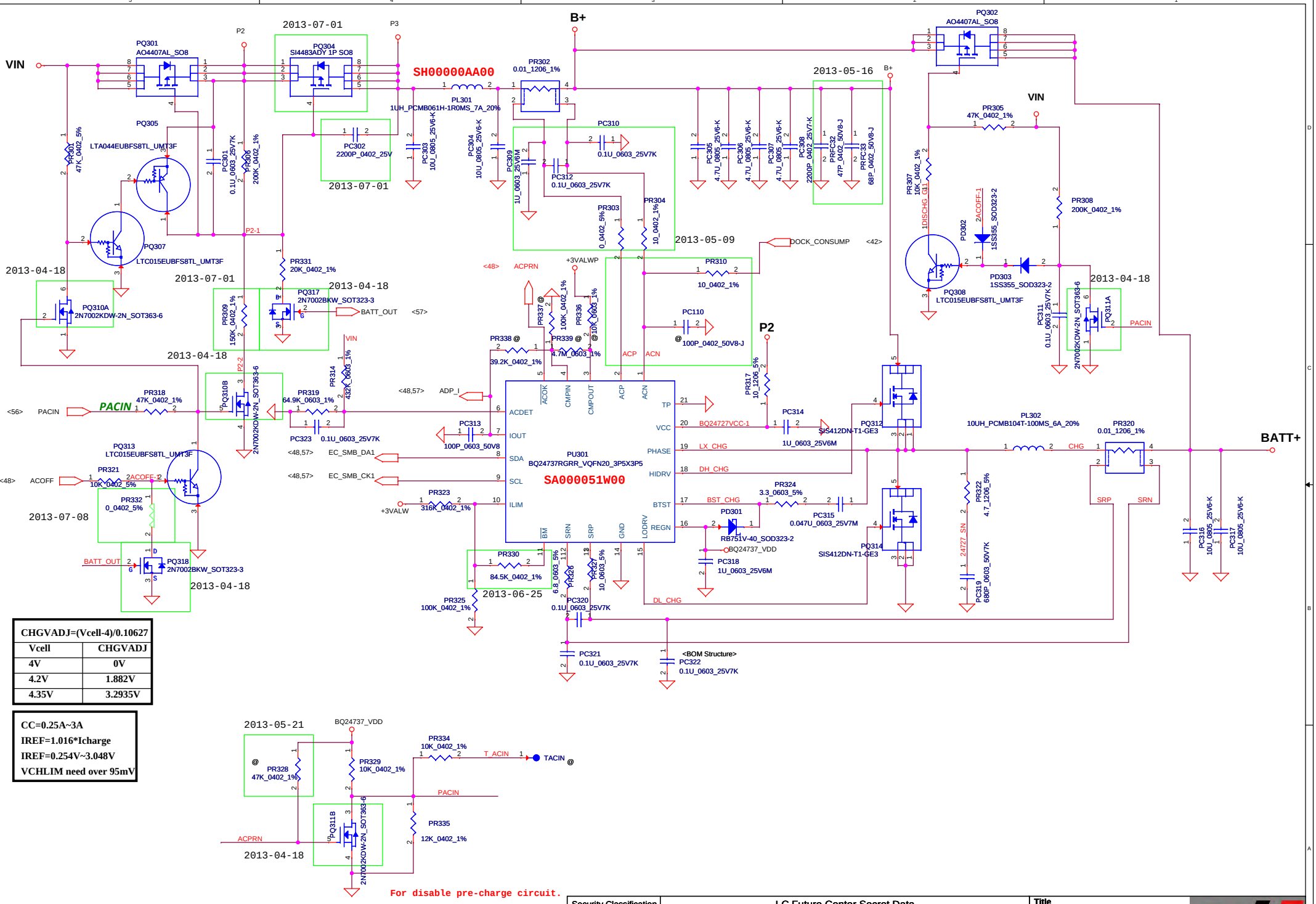
2011_1005 PQ105 change
form SB000006800(2N7002W T/R7 1N SOT-323)
to SB000009Q80(2N7002KW 1N SOT323-3)

+5VS
+3VS
PR237 100K_0402_1%
PR236 20K_0402_1%
PR238 100K_0402_1%
PC209 100P_0402_50V8-J
PC208 220P_0402_50V7-K
PR235 1.78M_0402_1%
PR234 221K_0402_1%
PU1204A
LM393DMR2G MICRO8 8P
2013-04-25
PR233 0_0402_5%
PQ207 2N7002BKW_SOT323-3
2013-04-18
Battery Protection Circuit for Turbo Mode

+5VS
+3VS
Turbo_V_1
PR243 150K_0402_1%
PR240 20K_0402_1%
PR244 84.5K_0402_1%
PC211 100P_0402_50V8-J
PC210 220P_0402_50V7-K
PR245 10K_0402_1%
PR239 1.78M_0402_1%
PR242 221K_0402_1%
PU1204B
LM393DMR2G MICRO8 8P
2013-04-25
PR241 0_0402_5%
PQ208 2N7002BKW_SOT323-3
2013-04-18
2013-07-01
Adaptor Protection Circuit for Turbo Mode

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: PWR-BATTERY CONN/OTP
Size: Custom
Document Number: E440 NM-A151
Rev: 1.0
Date: Thursday, July 11, 2013
Sheet 57 of 69



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

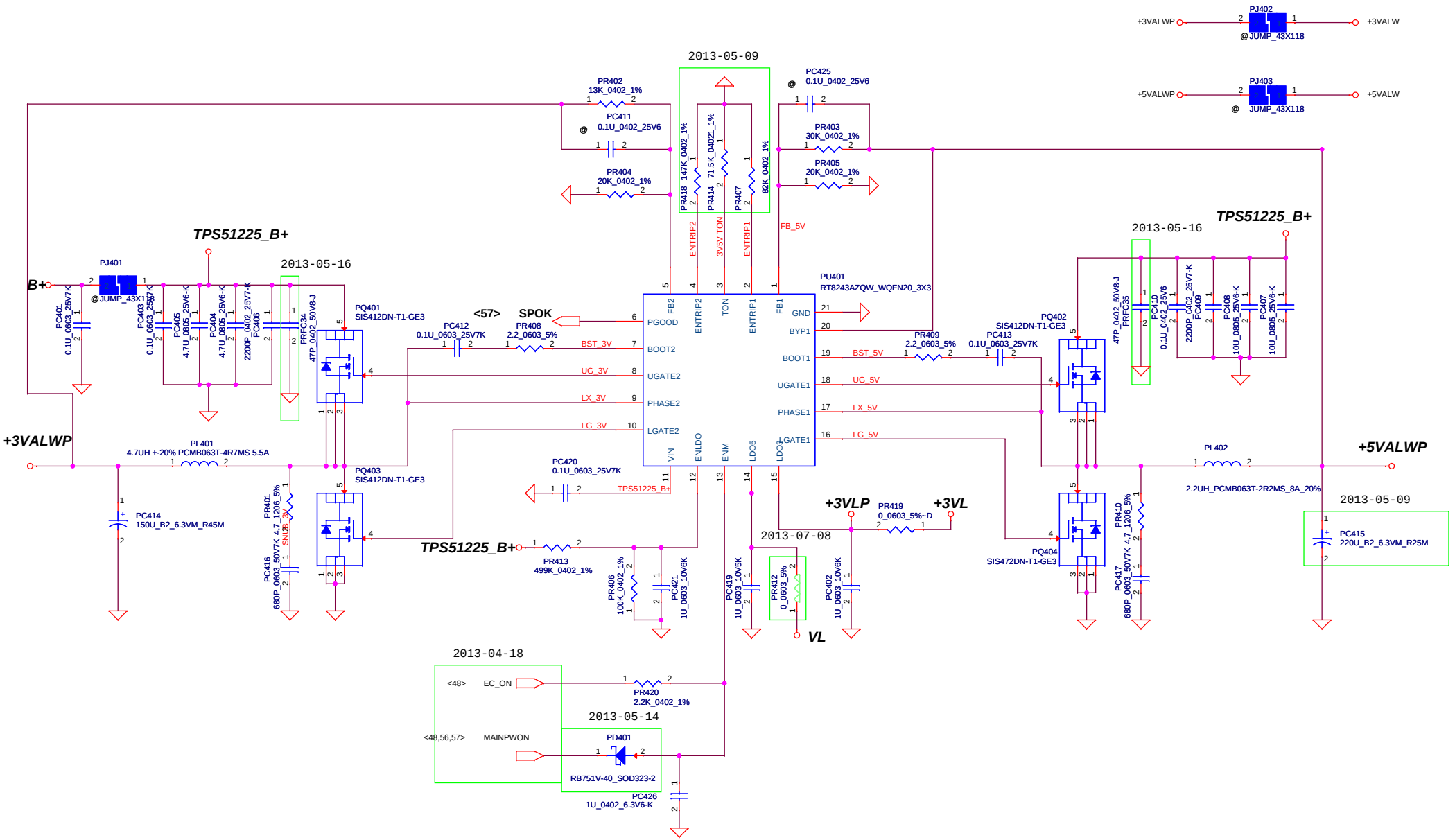
CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: PWR-CHARGER-BQ24737

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

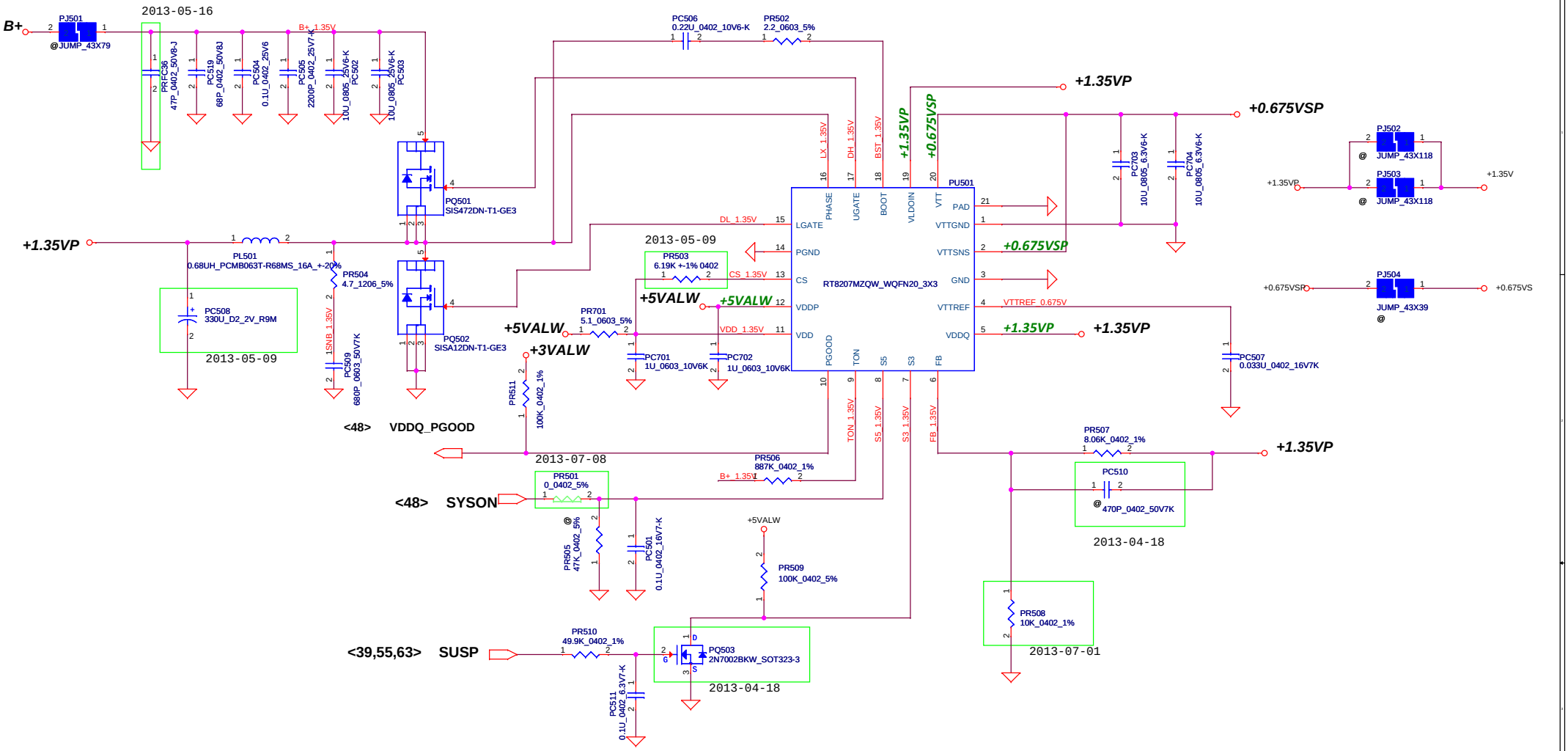
Date: Thursday, July 11, 2013 | Sheet 58 of 69



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

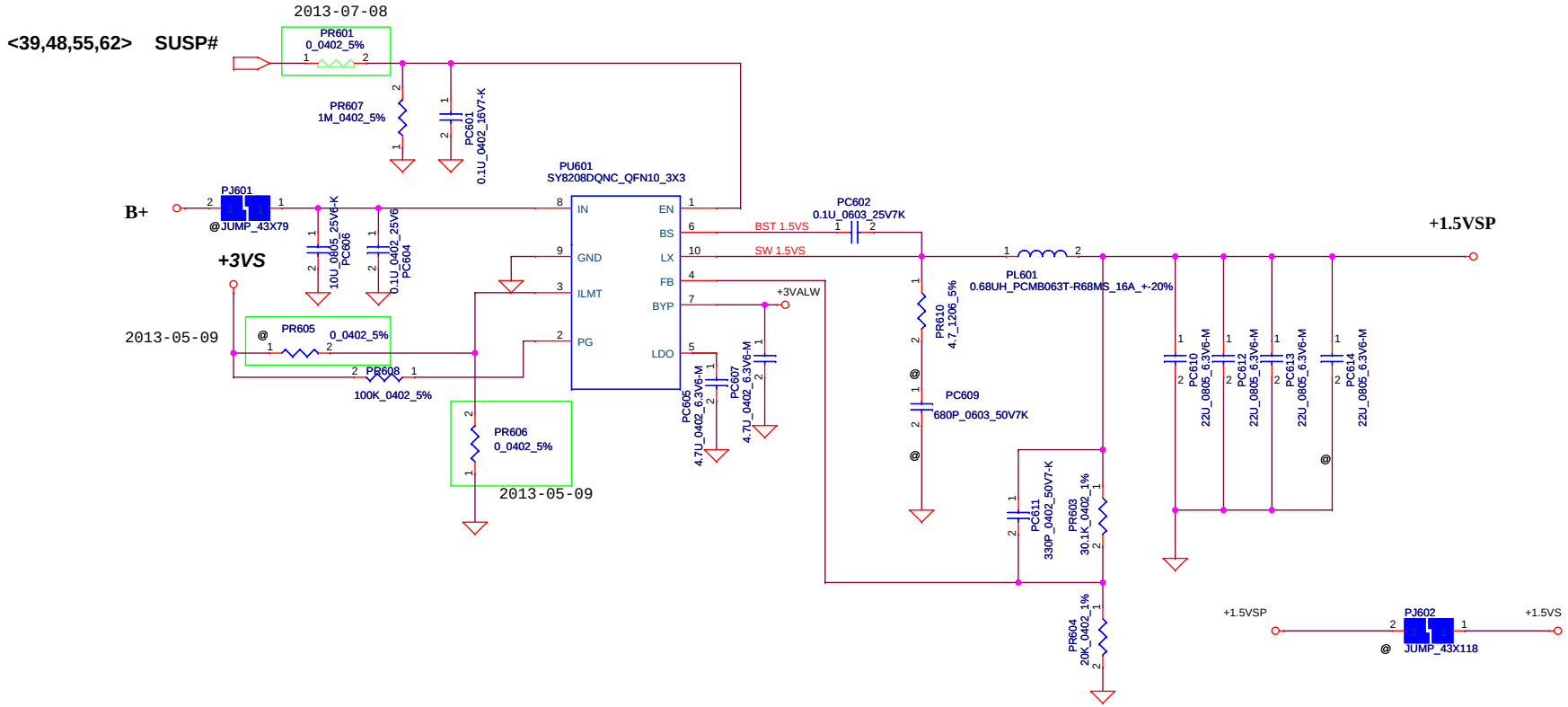
Title: PWR-3VALWP/5VALWP

Size: Custom	Document Number: E440 NM-A151	Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 59 of 69	



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	PWR-+1.35VP/+0.675VSP		
Size: Custom	Document Number: E440 NM-A151		Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 60 of 69		

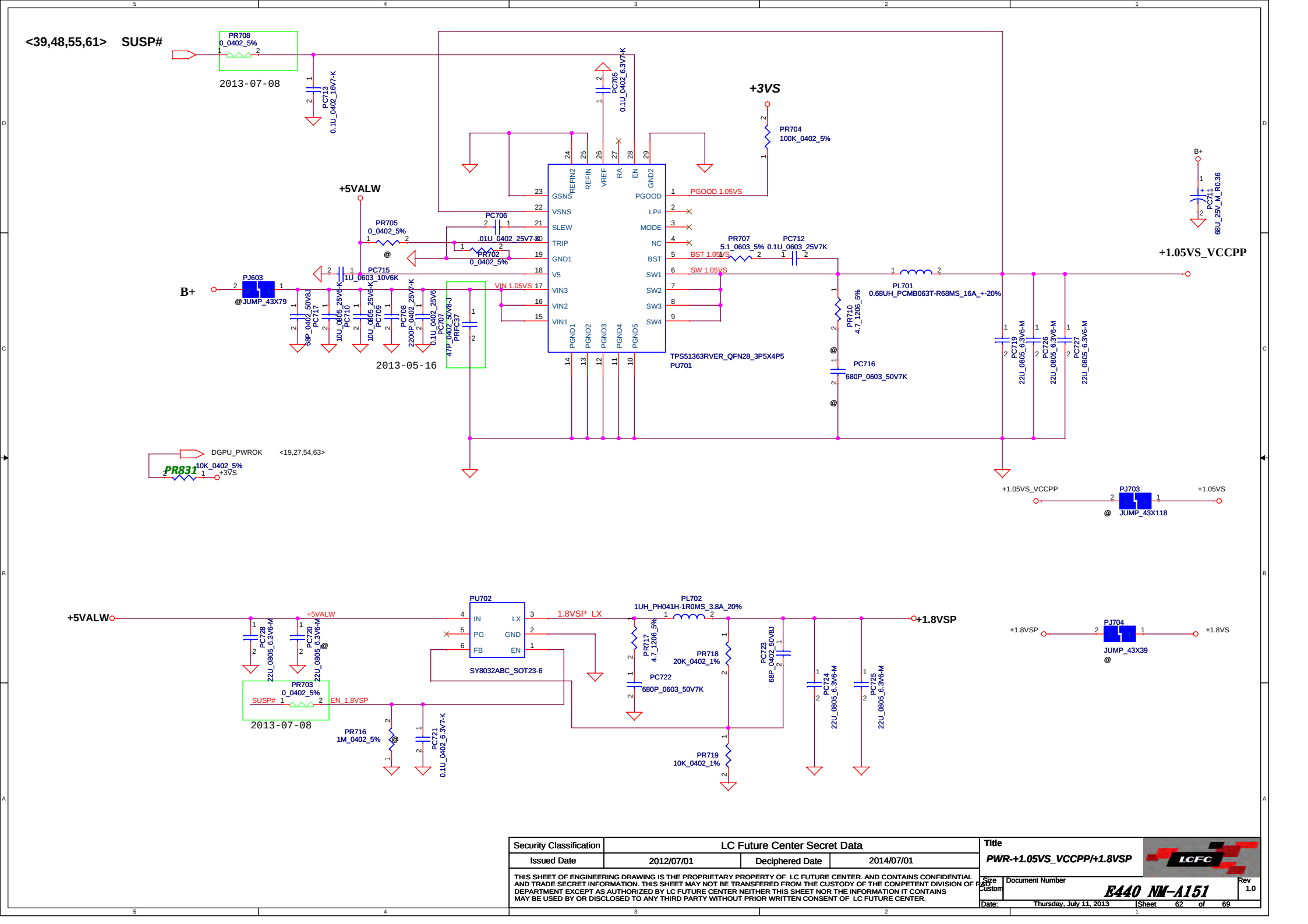


Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: PWR-+1.5VSP

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

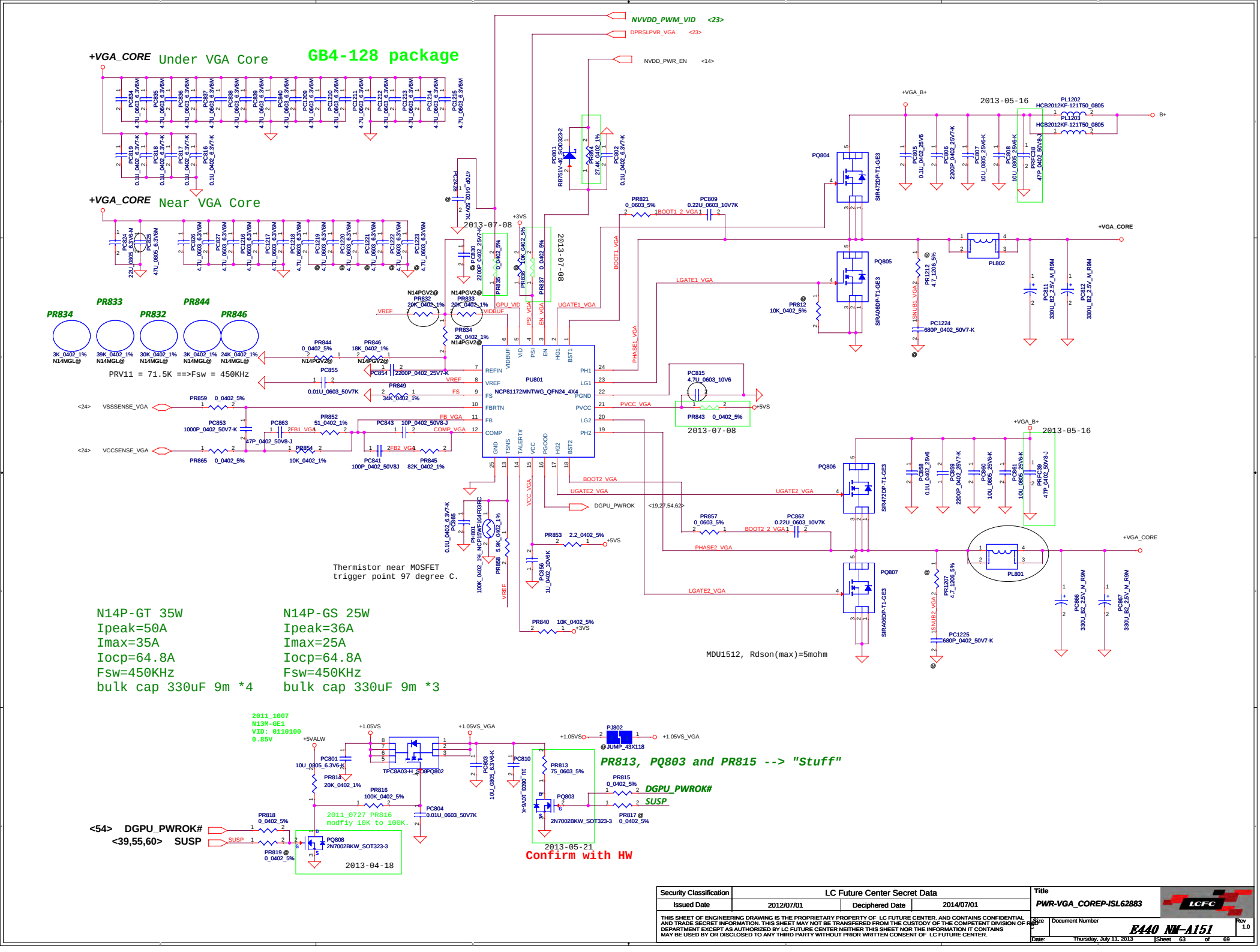
Date: Thursday, July 11, 2013 Sheet 61 of 69



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: PWR-+1.05VS_VCCPP/+1.8VSP

Size: Custom	Document Number: E440 NM-A151	Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 62 of 69	

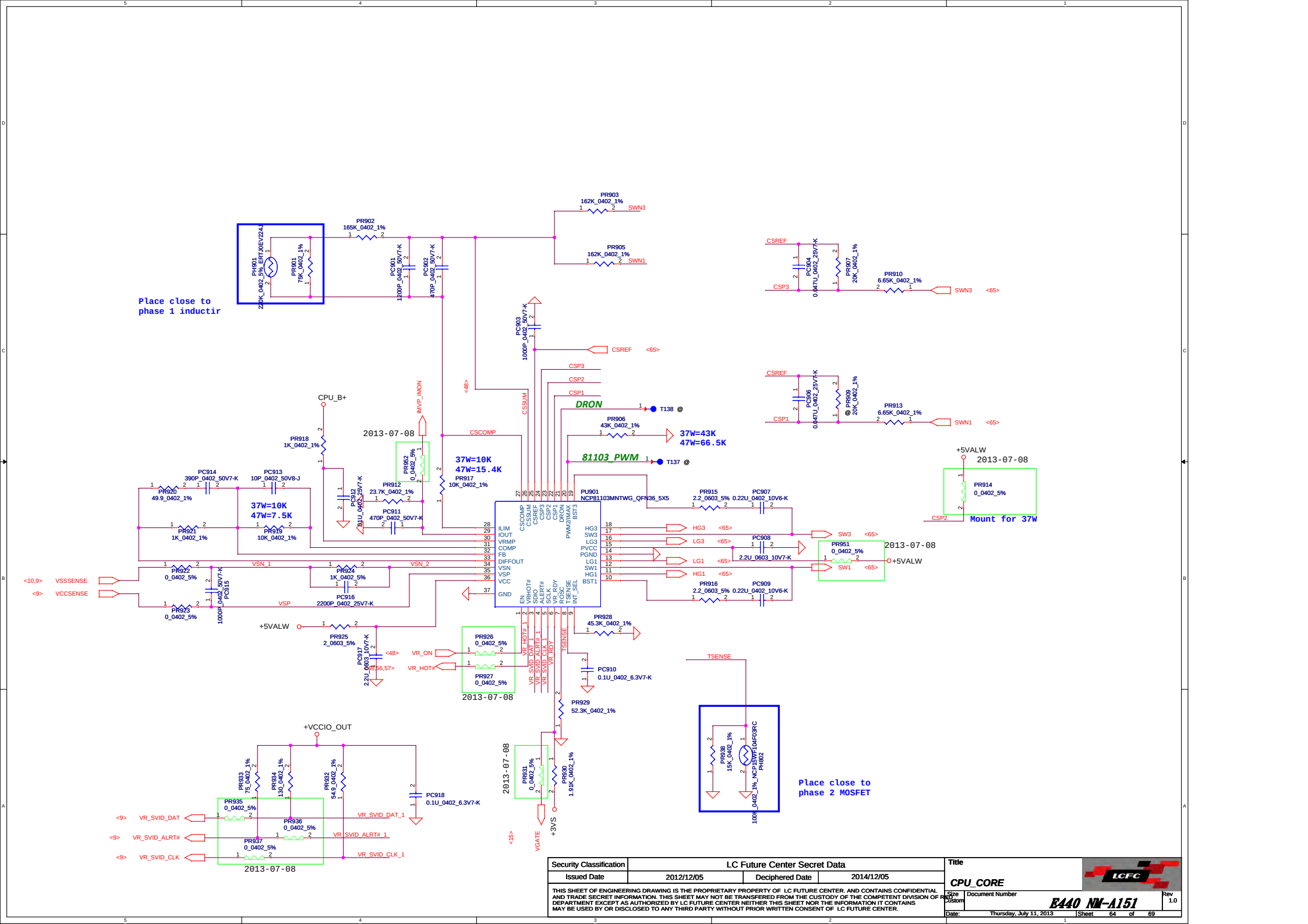


Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: PWR-VGA_COREP-ISL62883

Size: | Document Number: E440 NM-A151 | Rev: 1.0

Date: Thursday, July 11, 2013 | Sheet 63 of 69

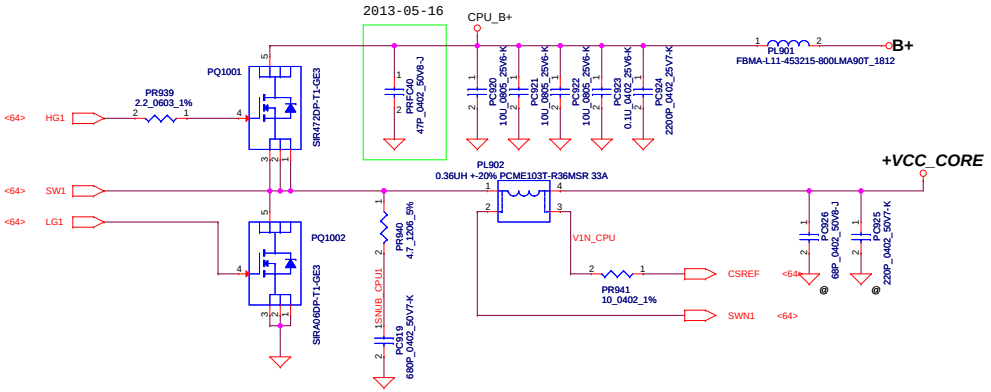


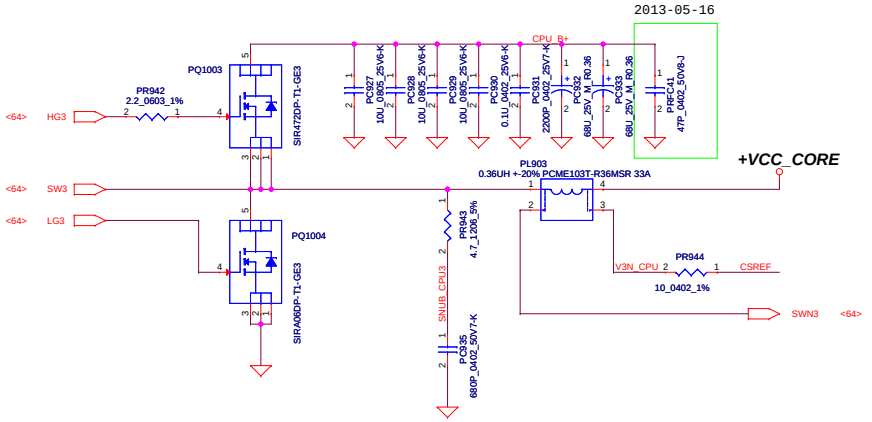
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: CPU_CORE

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

Date: Thursday, July 11, 2013 | Sheet 64 of 69





Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title	CPU_CORE		
Size	Document Number		Rev
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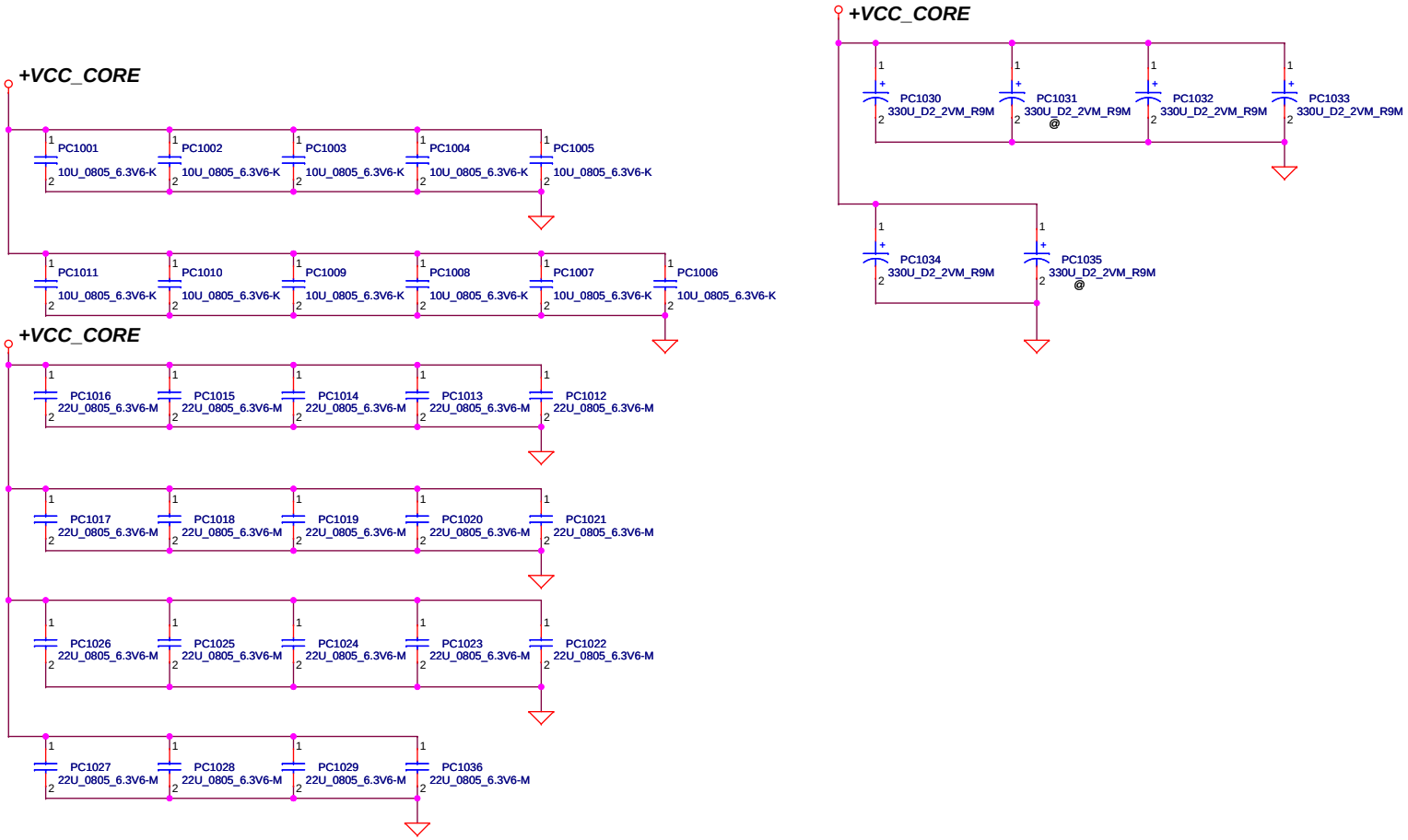
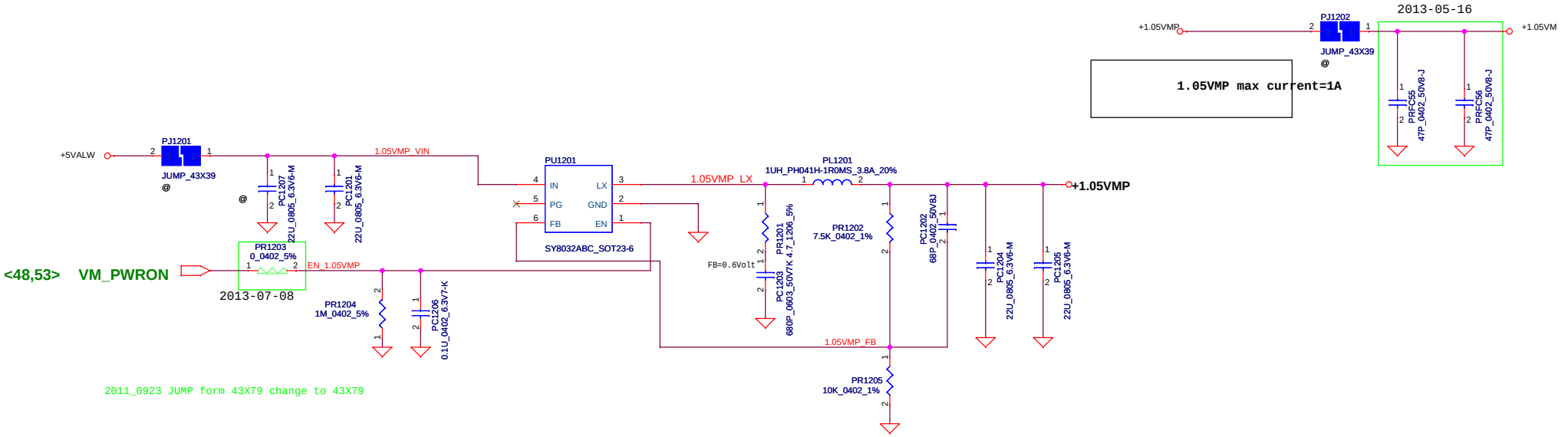
Date:	Thursday, July 11, 2013	Sheet	65 of 69



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: PWR-PROCESSOR DECOUPLING

Size: Custom	Document Number: E440 NM-A151	Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 66 of 69	



Title: PWR-+1.05VMP

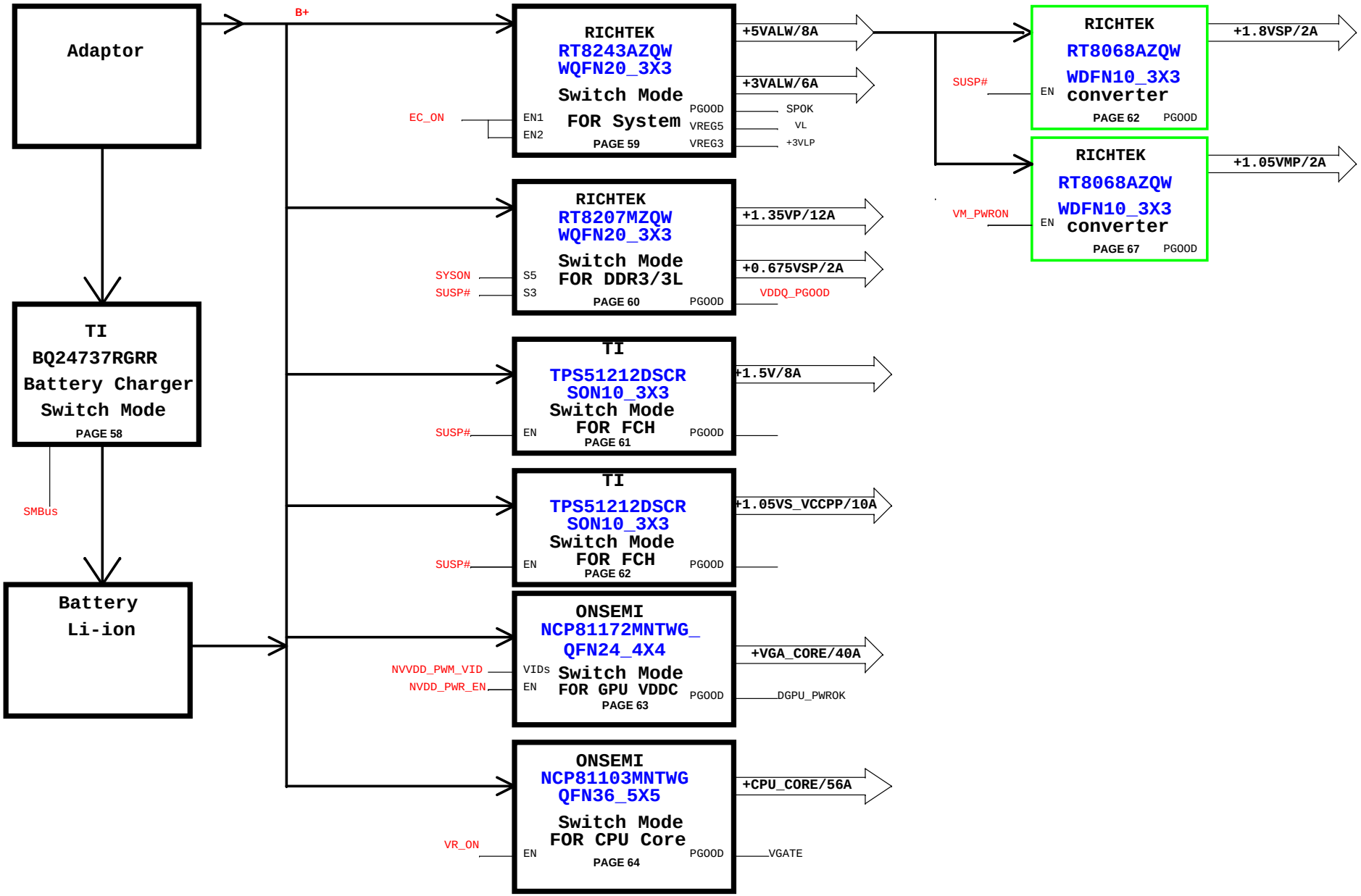
Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

Date: Thursday, July 11, 2013 | Sheet 67 of 69

POWER PIR (Product Improve Record)

AILE1 NM-A151 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1
GERBER-OUT DATE: 2013/01/16

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: HW-PIR

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

Date: Thursday, July 11, 2013 | Sheet 68 of 69

HW PIR (Product Improve Record)

AILE1 NM-A151 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1
GERBER-OUT DATE: 2013/01/16

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01)	03/14	10	R64 Change R64 BOM structure from "@" to "DS3@"	For Deep S3 Function

Compal Electronics, Inc.

Title	PIR (PWR)		
Size: Custom	Document Number: Y490-LA8691P		Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 69 of 69		