Compal Confidential

VALEA/VALEB Schematics Document

AMD APU Richland FS1r2 + FCH Bolton-M3 + GPU Sun Pro M2

2012-11-22

REV:1.0

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Title: Cover Page

Size: B | Document Number: LA-8126P | Rev: 1.0

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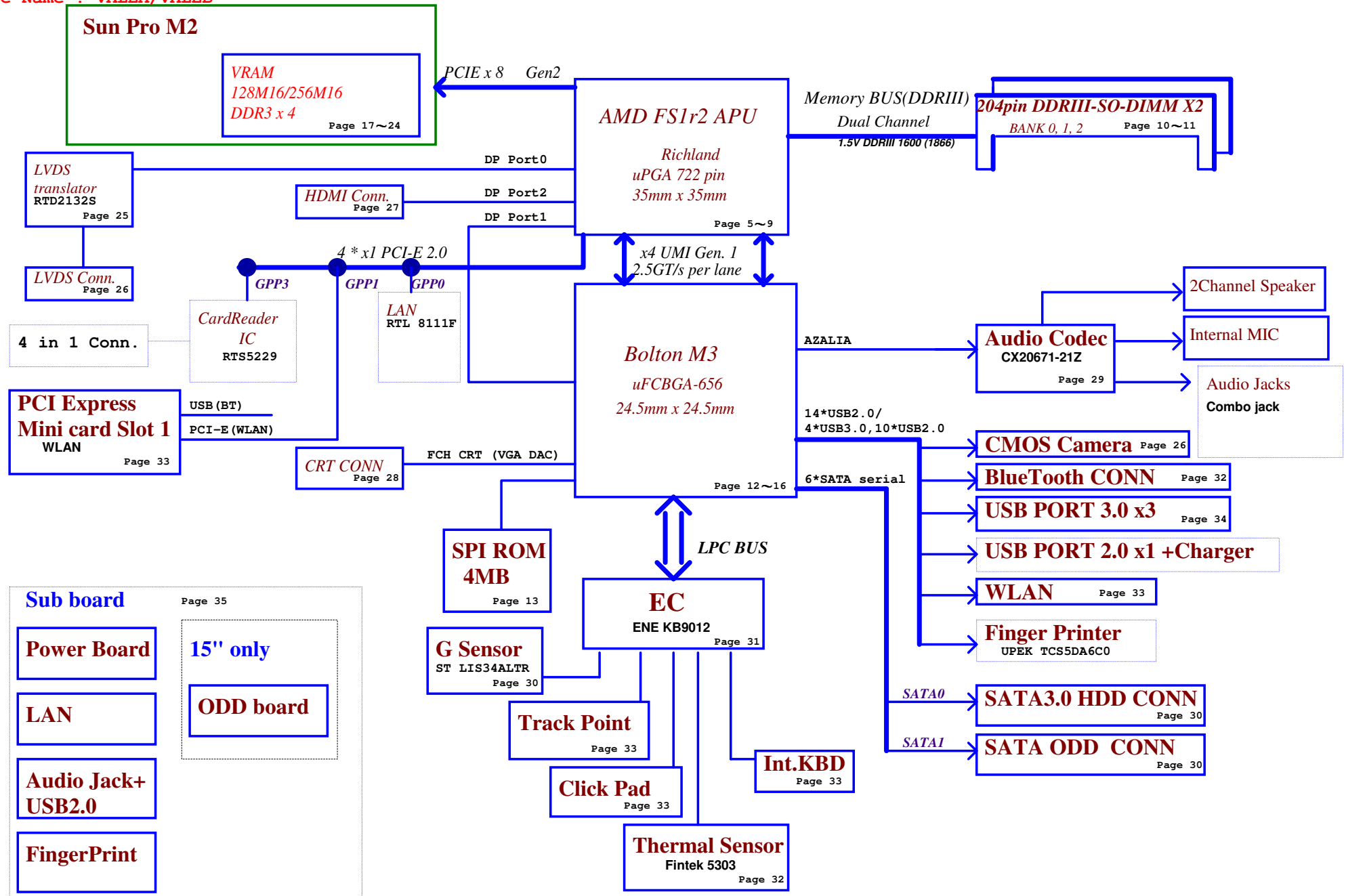
File Name : VALEA/VALEB



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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+1.5V	1.5V power rail for APU VDDIO and DDR	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.2VS	1.2V (VDDR, VDDP) switched power rail for APU	ON	OFF	OFF
+2.5VS	2.5V for APU VDDA	ON	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VGS	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+0.95VGS	0.95V switched power rail for VGA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS_WLAN	3.3V power rail for WLAN	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

FCH Hudson-M2/3 SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

Comal PCIE Port List

APU	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	Card Reader
FCH	PCIE0	NC
	PCIE1	NC
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M2/3 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	USB2.0 Port
Port1	NC
Port2	NC
Port3	NC
Port4	NC
Port5	WLAN
Port6	CMOS
Port7	FP
Port8	BT
Port9	NC
Port10	USB 3.0
Port11	USB 3.0
Port12	USB 3.0
Port13	NC

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001-011xb	15H

EC SM Bus2 address

Device	Address	HEX
F75303 (DDR,VRAM,CPUCORE)	1001-101xb	9AH
SB-TSI	1001-100xb	98H
Sun Pro M2	1000-0010b	82H
LVDS translator		

BOM Structure

UMA@ : UMA only
DIS@ : DIS muxless

CMOS@ : USB camera

CONN@ : ME components
X76@, H1G@, S1G@ : VRAM

BOM option and stencil

SDV:
CMOS@/DIS@ + X76@

PJ201,PJ401,PJ502,PJ503,PJ504,PJ601,PJ603,PJ604,
PJ701,PJ702,PJ703,PJ704,J1,J2301,J2401,J2402,J2403
PJ402,PJ403,PJ501,PJ602,PJ801,PJ802,PJ803,PJ805

FCH SMB0

(FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		
Security ROM		

Stencil Memo

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Title: Notes List

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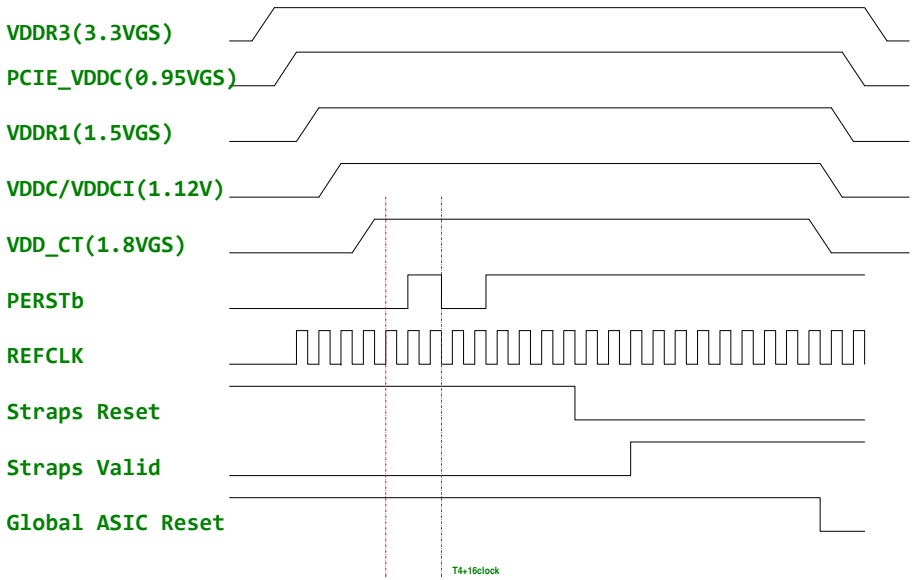
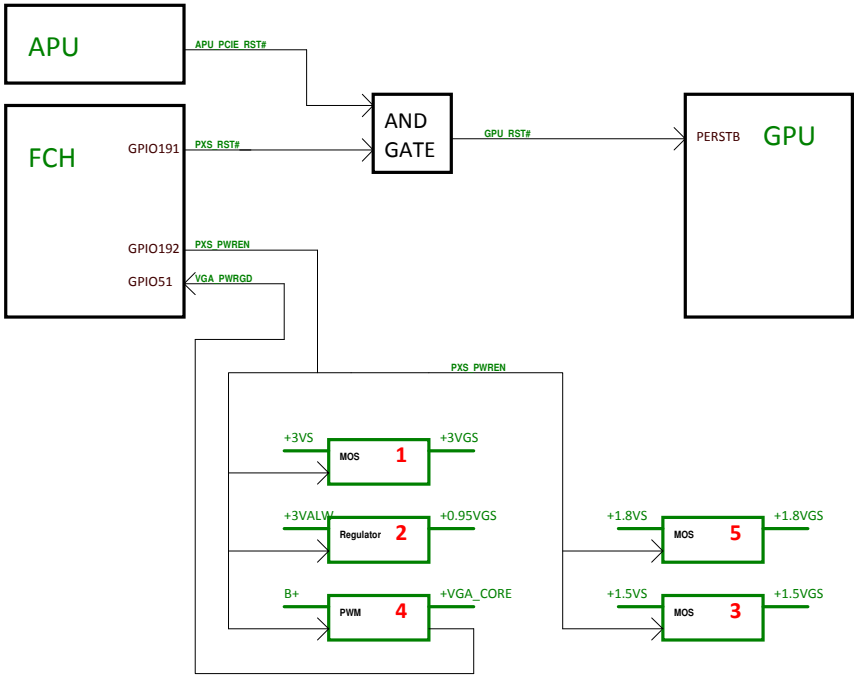
Power-Up/Down Sequence

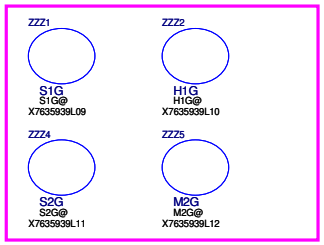
- All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.





SUN PRO VRAM STRAP

	Vendor	PS_3[2]	PS_3[1]	PS_3[0]	R_pu	R_pd
	H5TQ2G63DFR-11C SA00003YO70	0	0	0	R1430 NC	R1436 4.75K
1G	K4W2G1646E-BC11 SA00005SH00	0	0	1	R1430 8.45K	R1436 2K
	MT41J128M16JT-093G SA000067510 FBGA Code:D9PTD	0	1	0	R1430 4.53K	R1436 2K
	K4W4G1646B-HC11 SA000068R00	0	1	1	R1430 6.98K	R1436 4.99K
2G	MT41K256M16HA-107G SA000065D00 FBGA Code:D9PZD	1	0	0	R1430 4.53k	R1436 4.99K
	MT41J128M16JT-107G SA00005SM30 FBGA Code:D9PRS	1	0	1	R1430 3.24k	R1436 5.62k
1G	K4W2G1646E-BC1A SA000068U10	1	1	0	R1430 3.4k	R1436 10k
		1	1	1	R1430 4.75K	R1436 NC



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Title: dGPU Block Diagram

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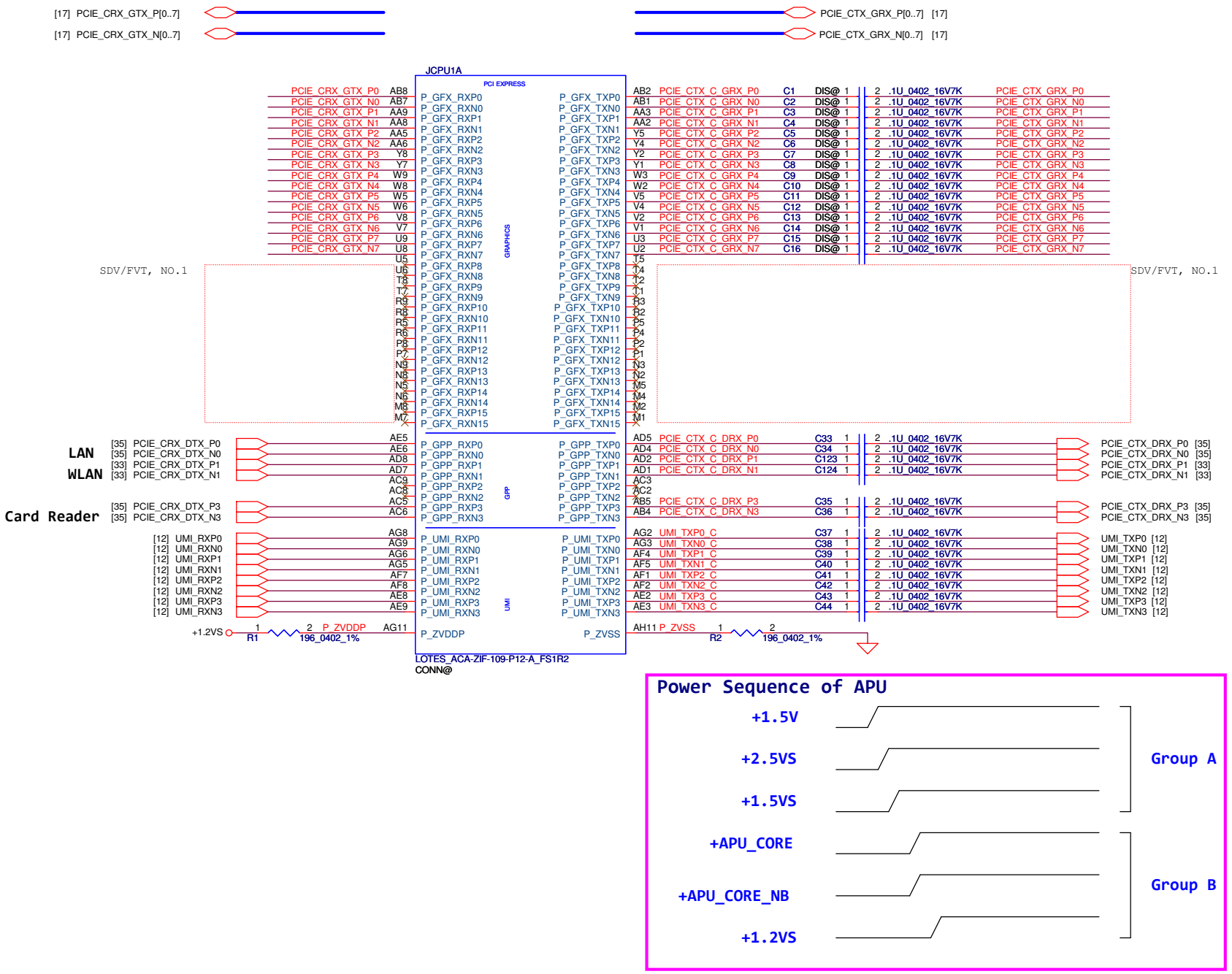

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Title: FS1r2 PCIE/UMI

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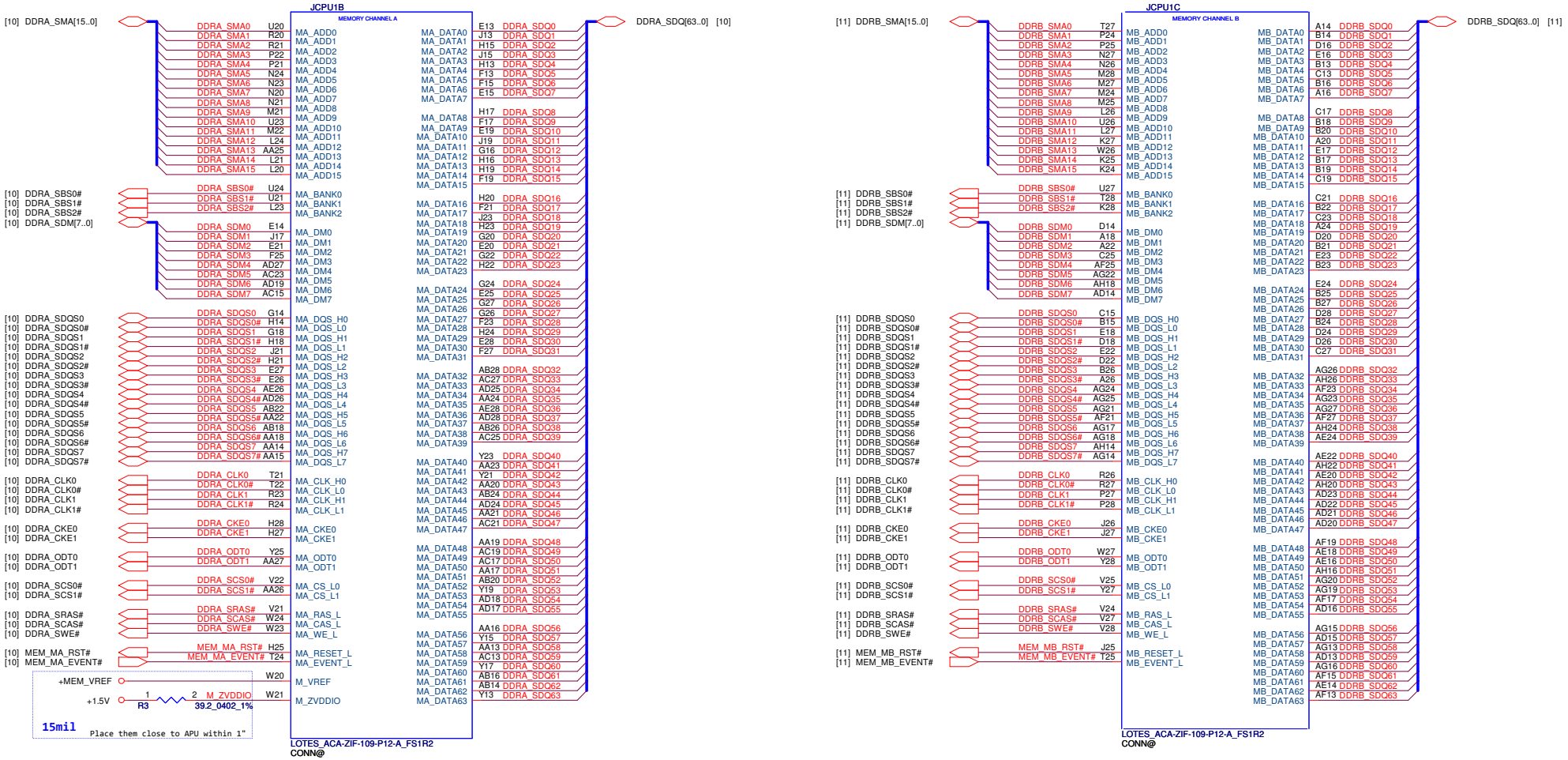
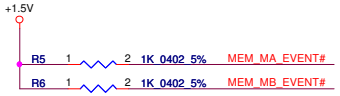
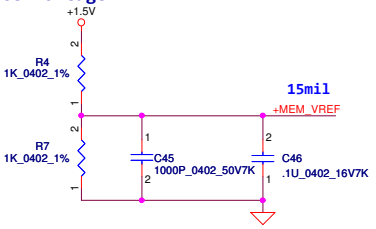


EVENT# pull high



0.75V reference voltage



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Compal Electronics, Inc.

Title: FS1r2 DDRIII Memory I/F

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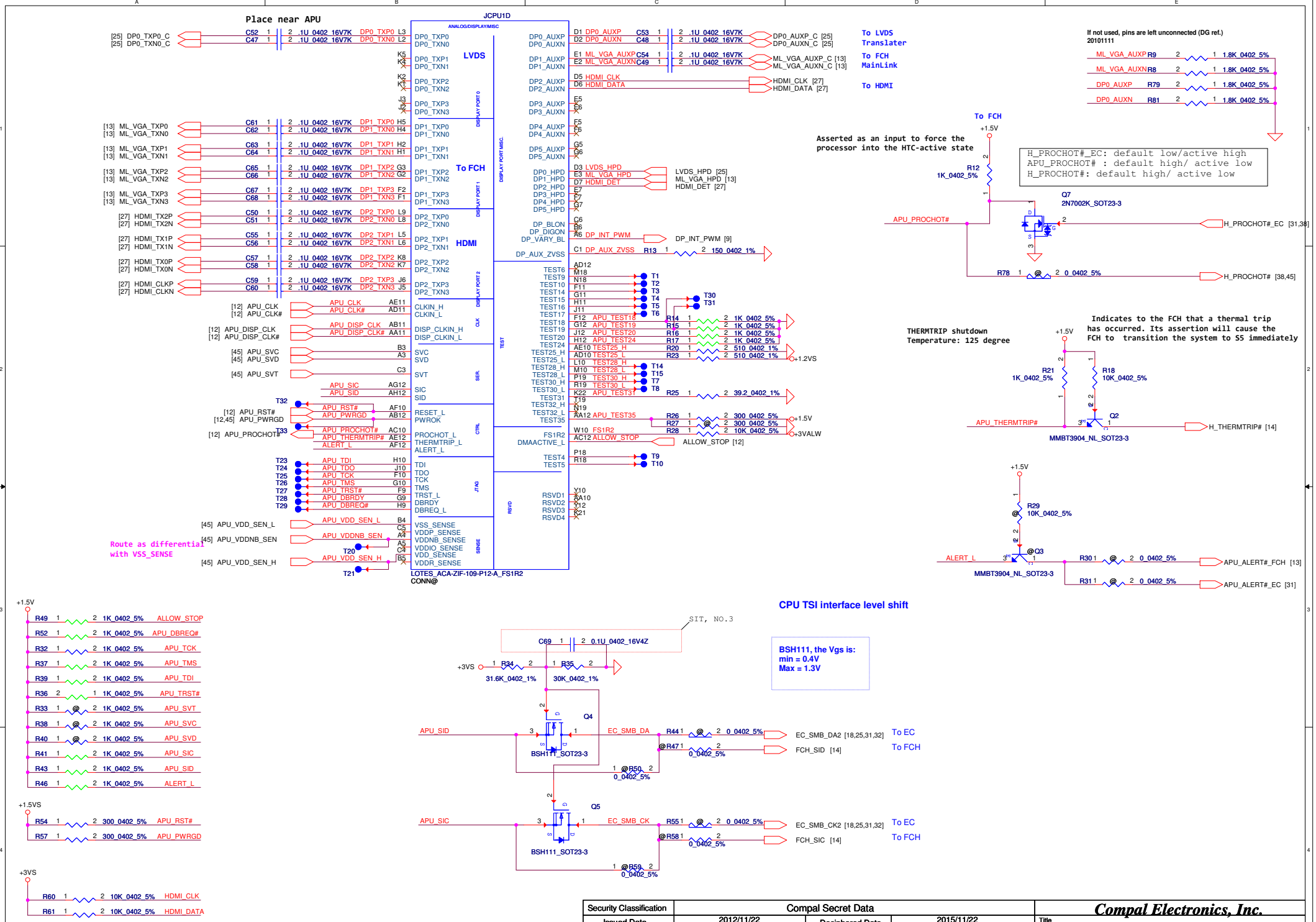

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Title: FS1r2 Display/MISC/HDT

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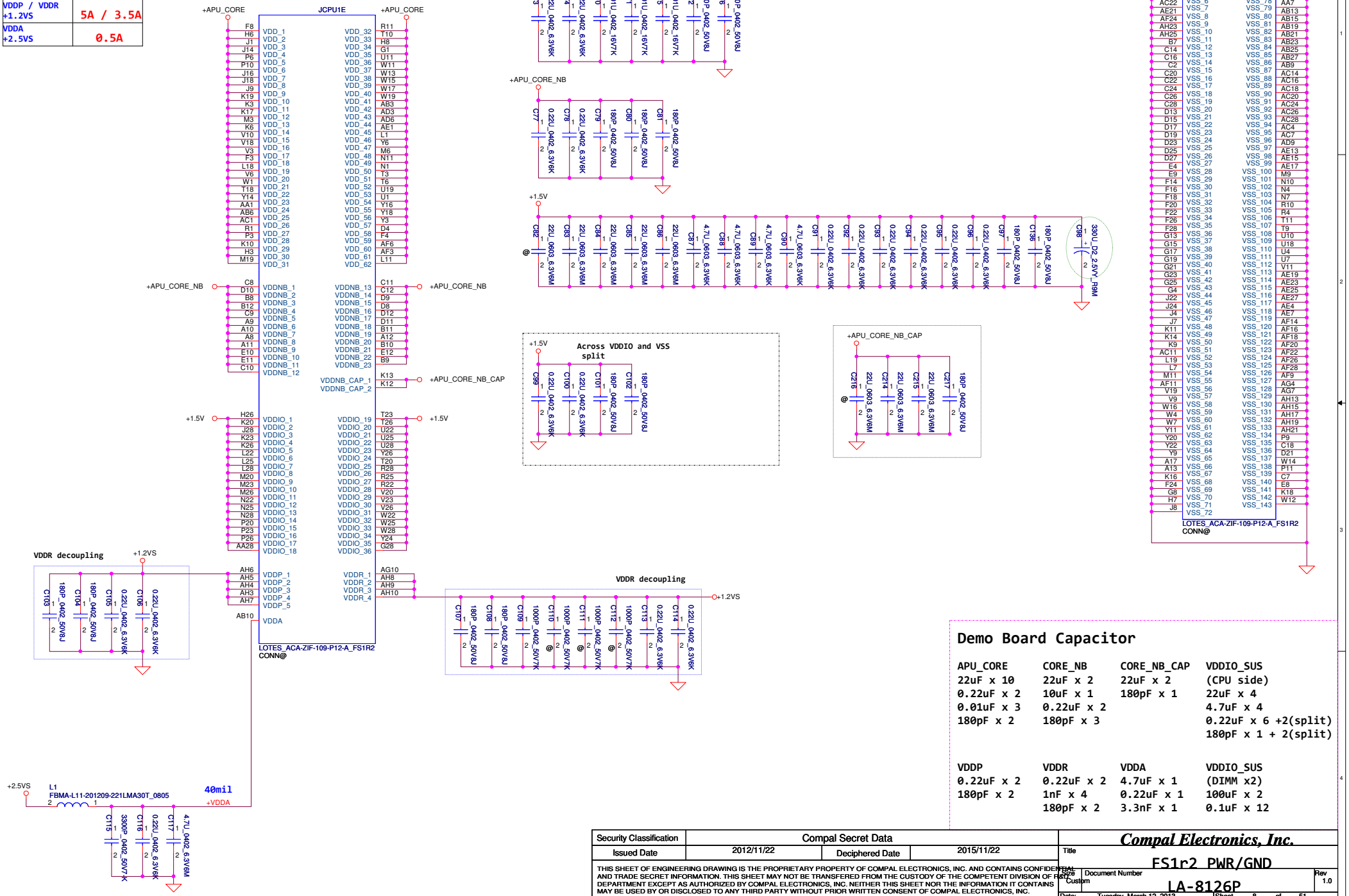
Power Name	Consumption
VDD +APU_CORE	60A
VDDNB +APU_CORE_NB	44A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A



Demo Board Capacitor

APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	180pF x 1	22uF x 4
0.01uF x 3	0.22uF x 2		4.7uF x 4
180pF x 2	180pF x 3		0.22uF x 6 +2(split)
			180pF x 1 + 2(split)

VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 4	0.22uF x 1	100uF x 2
	180pF x 2	3.3nF x 1	0.1uF x 12

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Title: FS1r2 PWR/GND

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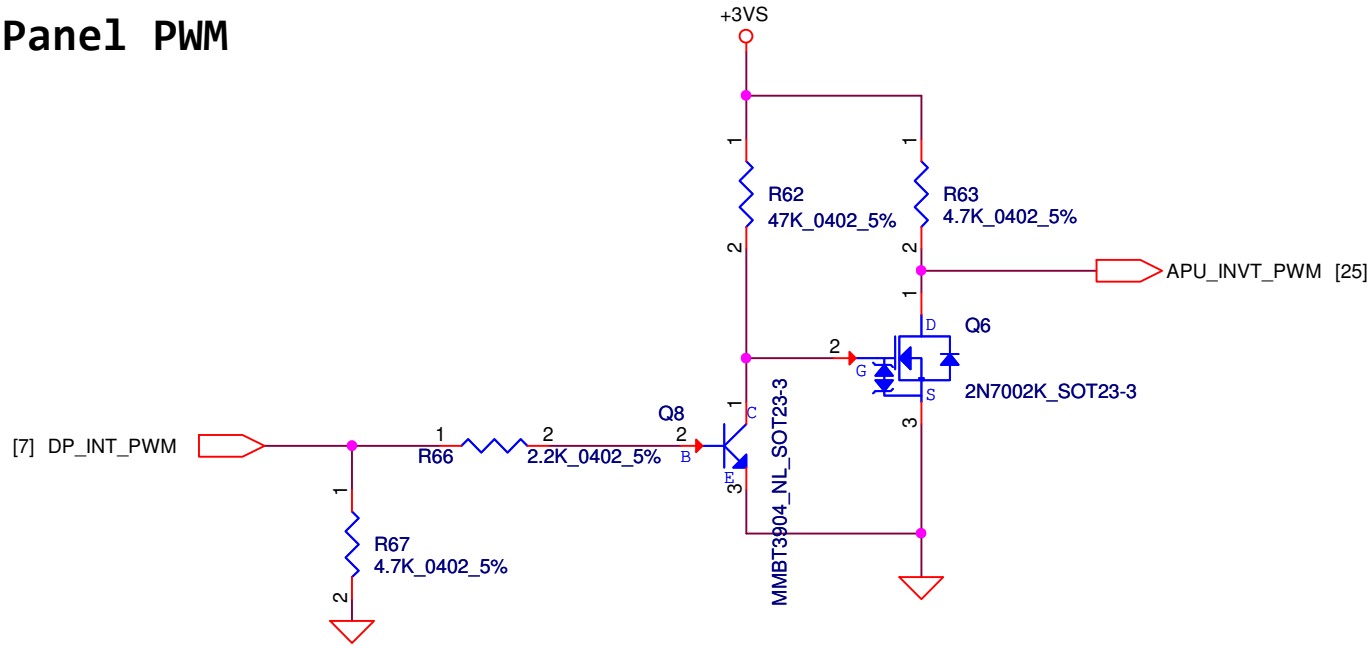
Panel PWM



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Title: FS1r2 Signal Level Shifter

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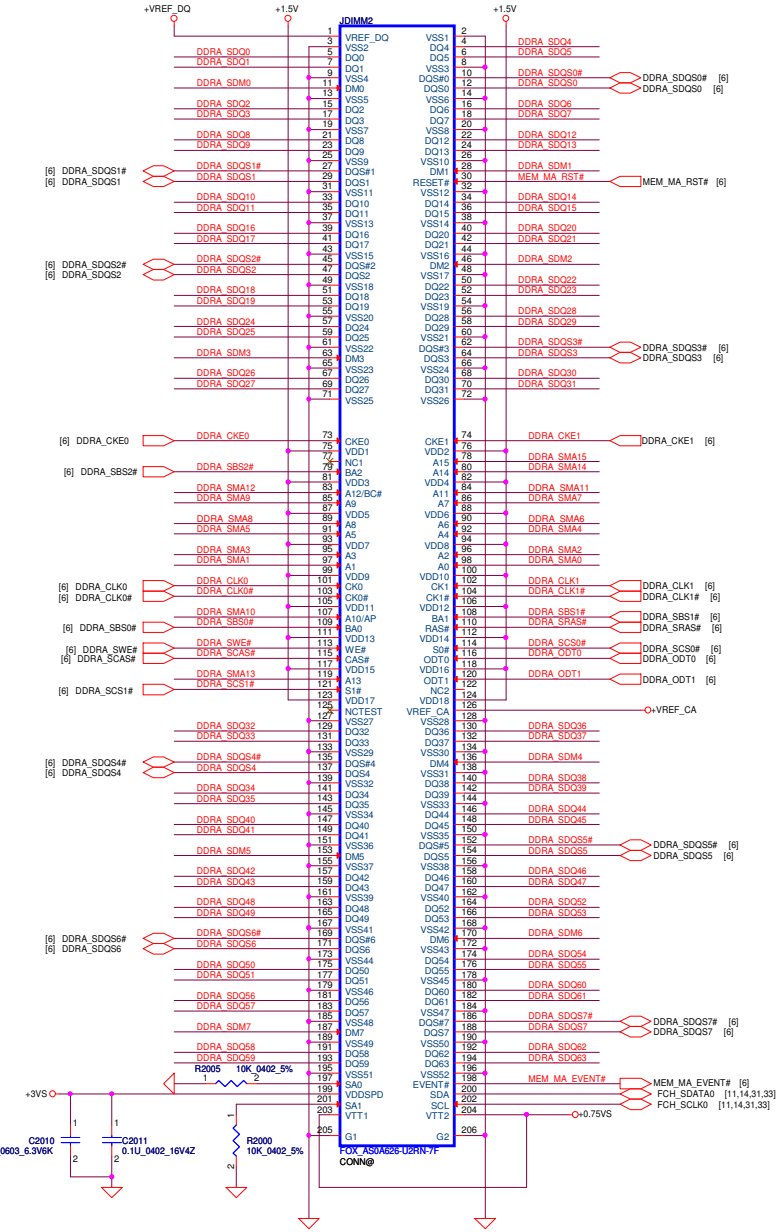
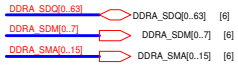
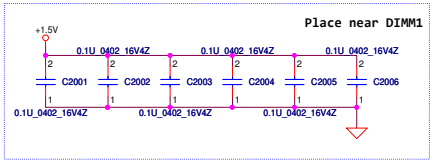
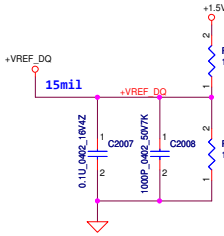
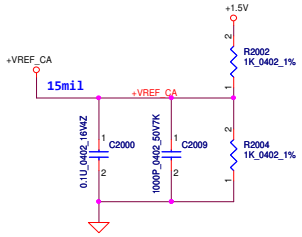


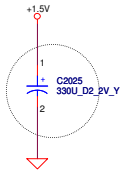
Reverse H:5.2mm











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Title: DDRIII SO-DIMM 1

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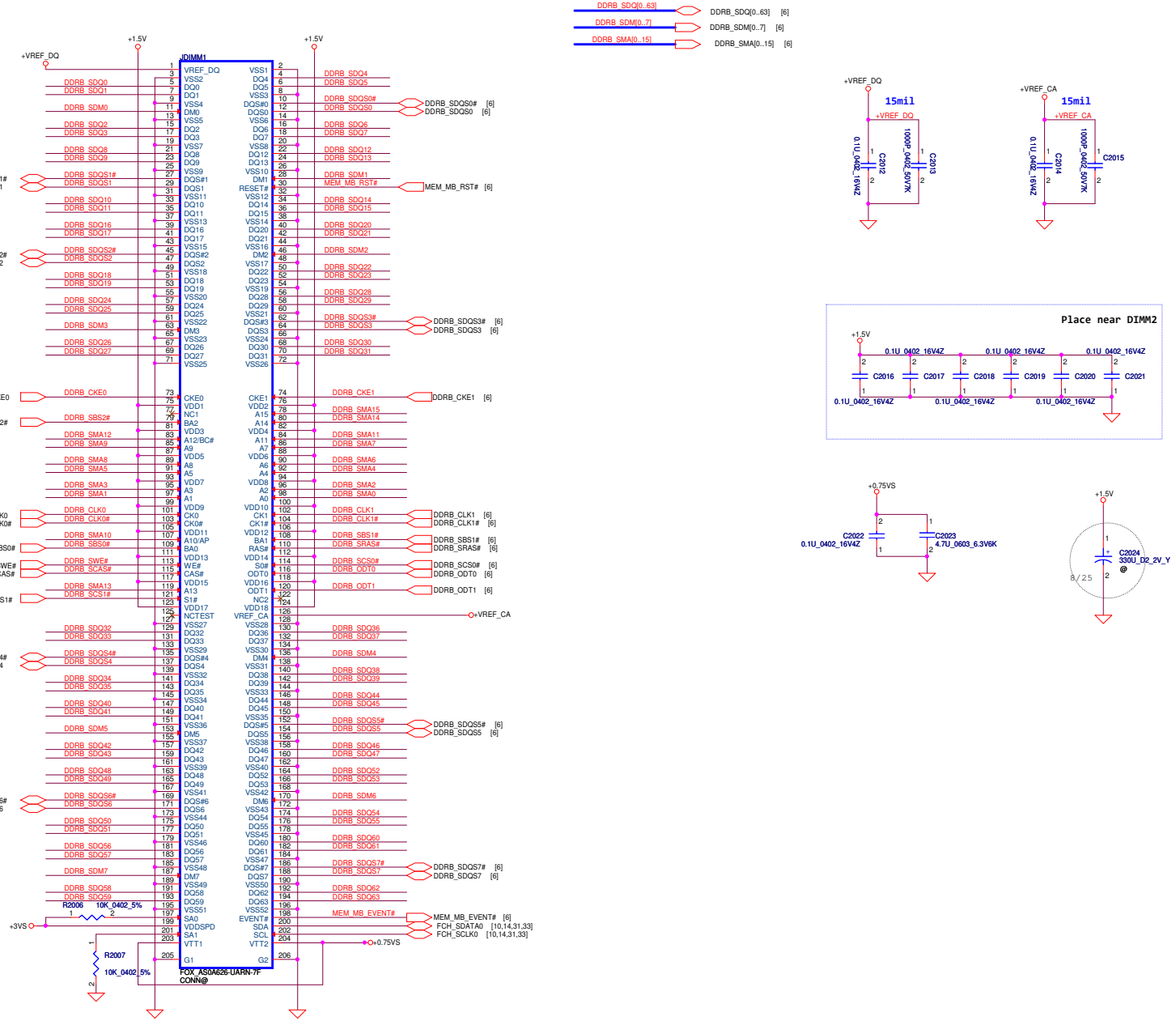

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Title: DDRIII SO-DIMM 2

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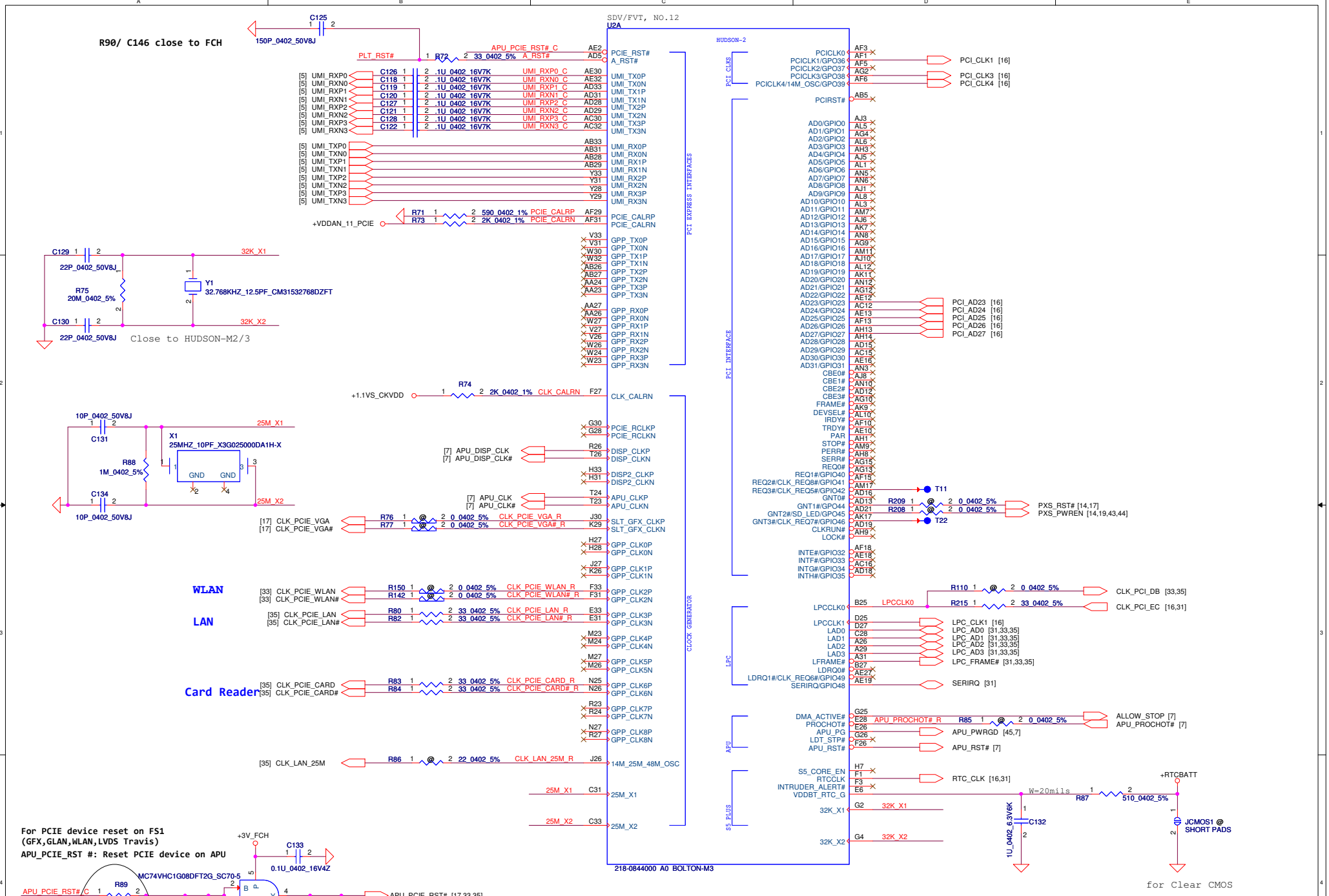

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Title: FCH PCIE/CLK/PCI/LPC/RTC

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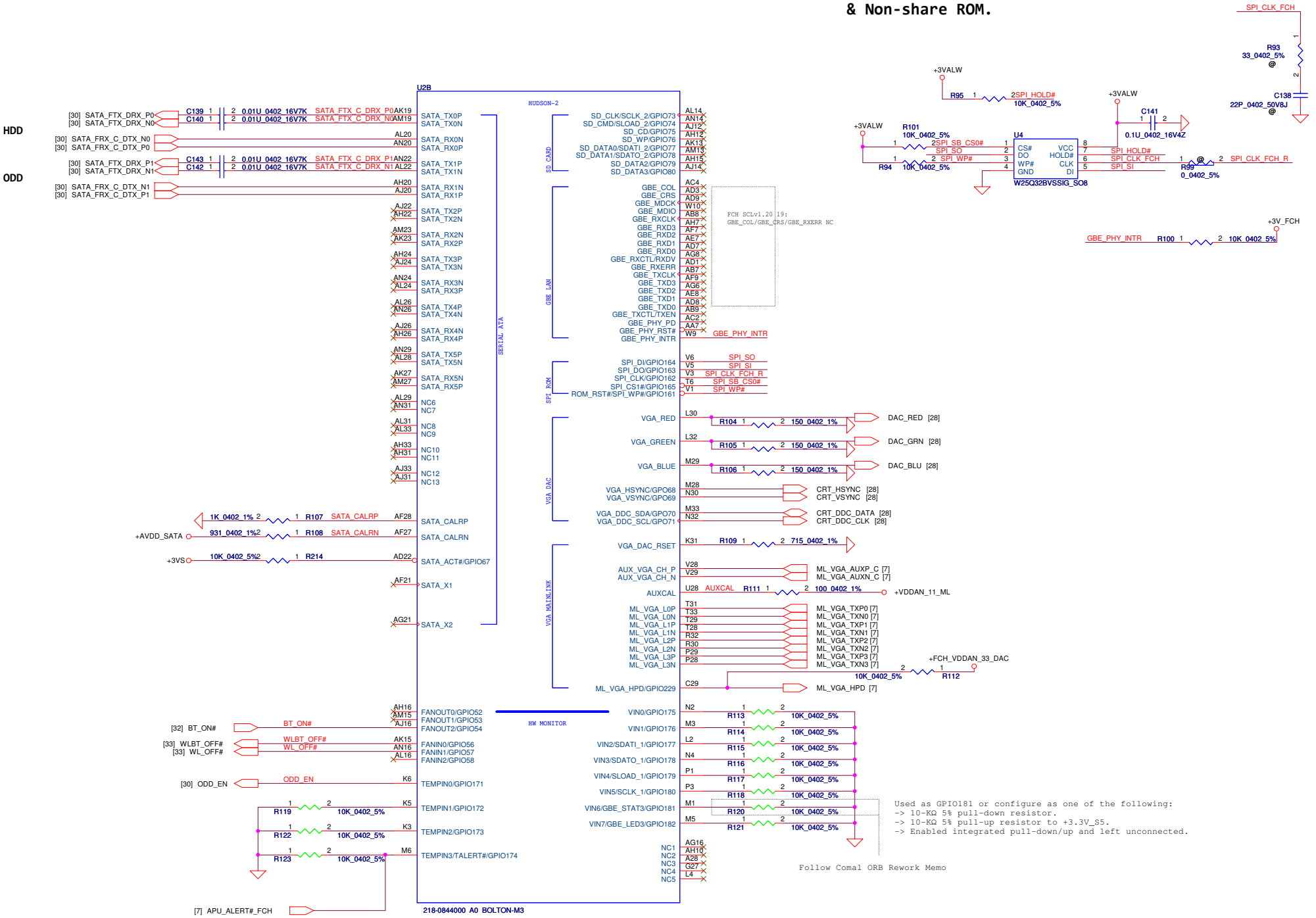
4MB SPI ROM
& Non-share ROM.



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Title: FCH SATA/SPI/VGA/HWM/SD

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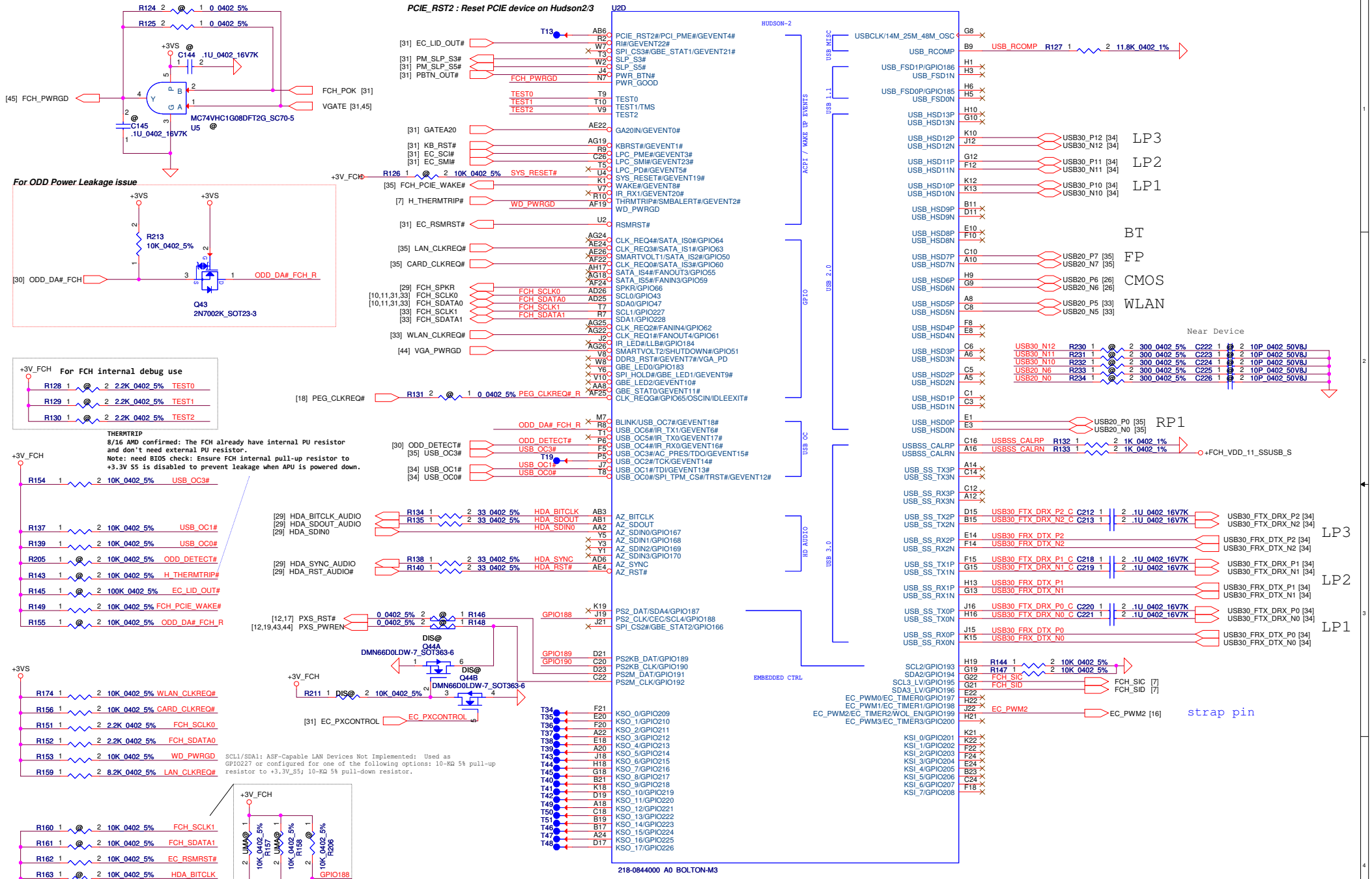

GPIO188	GPIO189	GPIO190	Function
0	0	0	PX
0	0	1	Reserved
0	1	0	DISCRET
0	1	1	UMA

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Compal Electronics, Inc.

Title: FCH_SATA/SPI/VGA/HWM/SD

Size: Custom | Document Number: LA-8126P | Rev: 1.0

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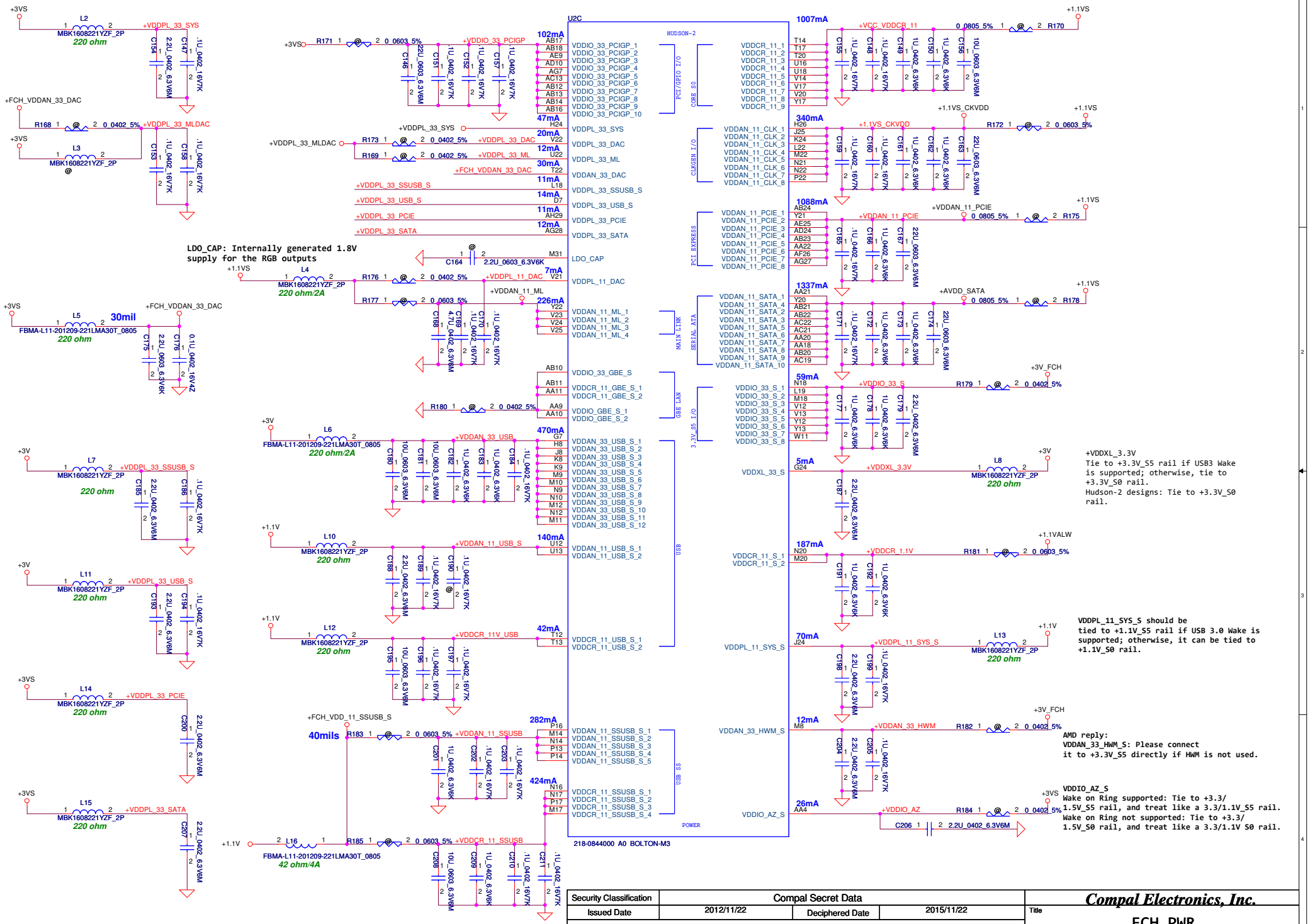

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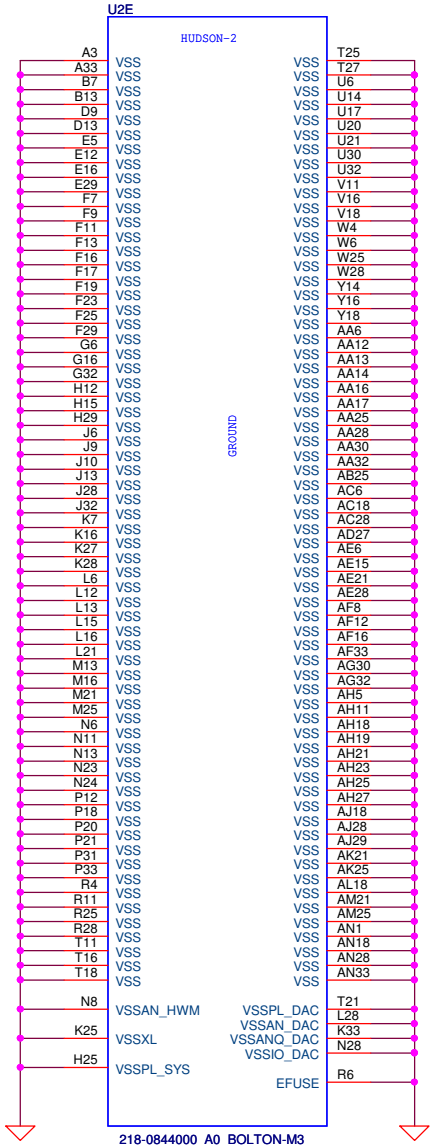
Compal Electronics, Inc.

Title: FCH PWR

Size: B/25 Custom | Document Number: LA-8126P | Rev: 1.0

Date: Tuesday, March 12, 2013 | Sheet 15 of 51



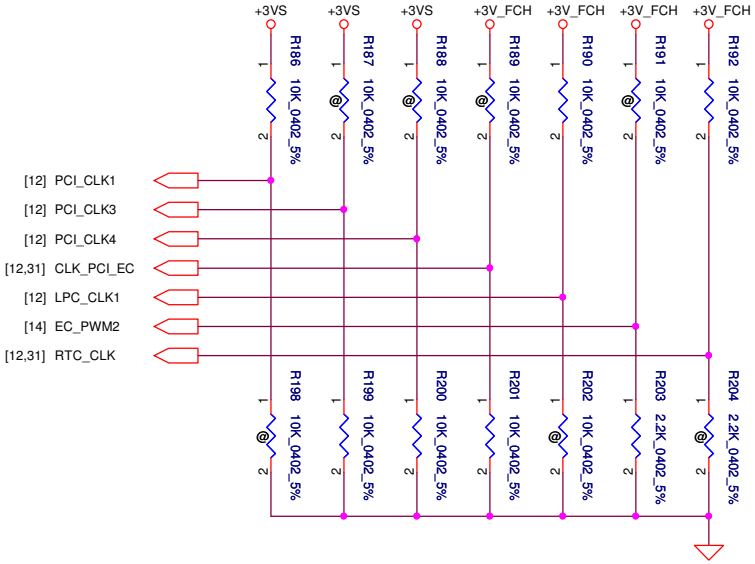
STRAP PINS

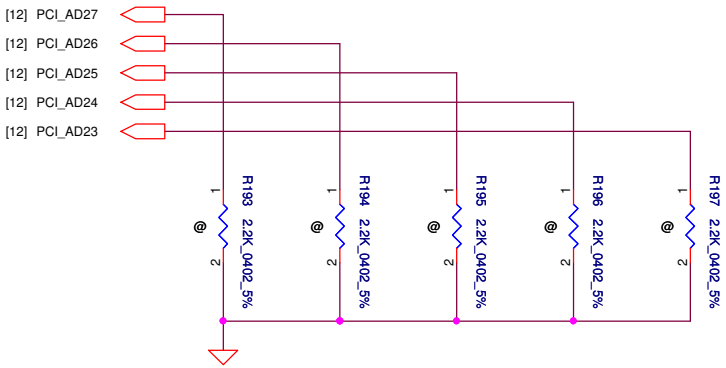
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





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Compal Electronics, Inc.

Title: FCH-VSS/Strap

Size: B | Document Number: LA-8126P | Rev: 1.0

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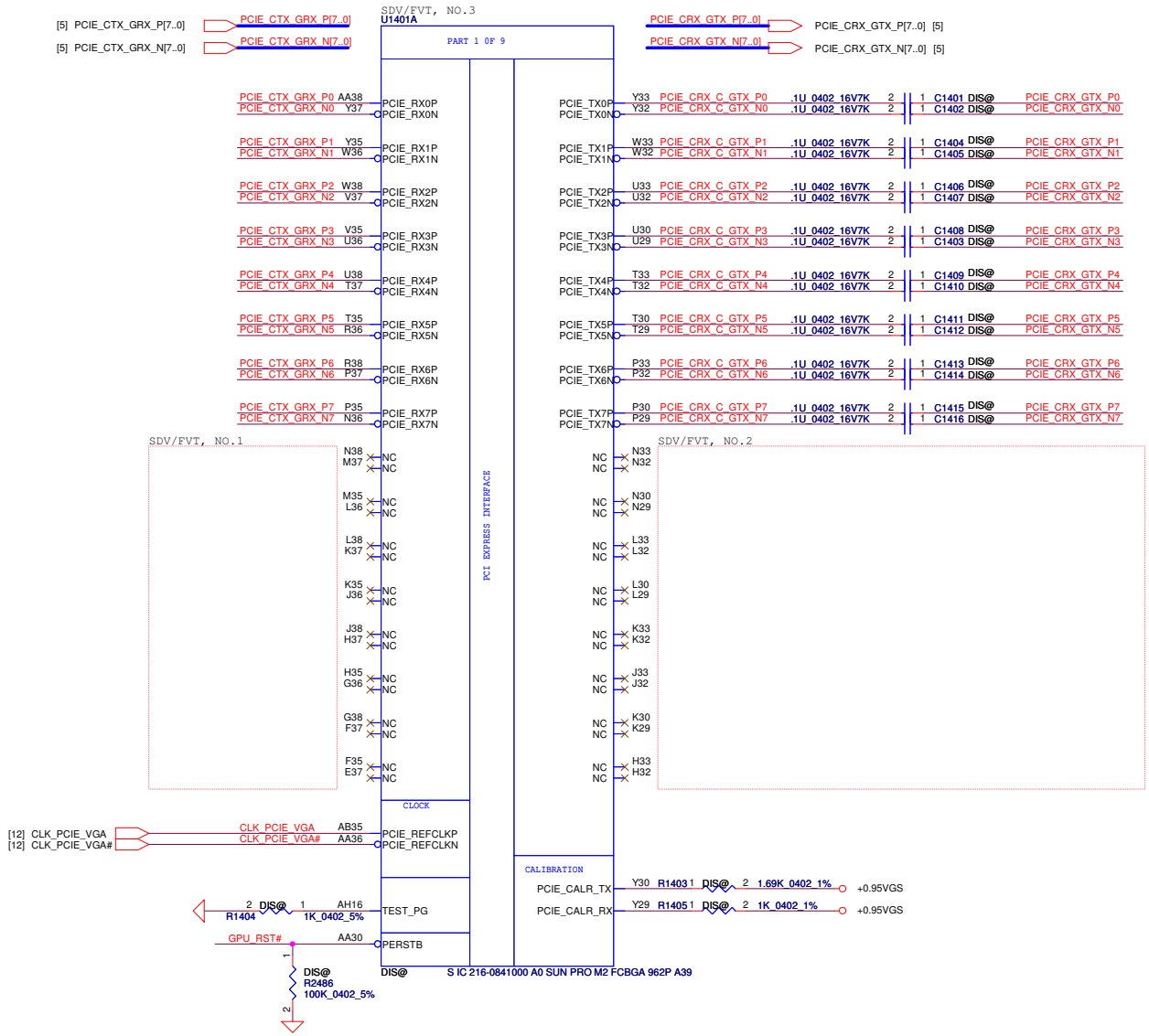
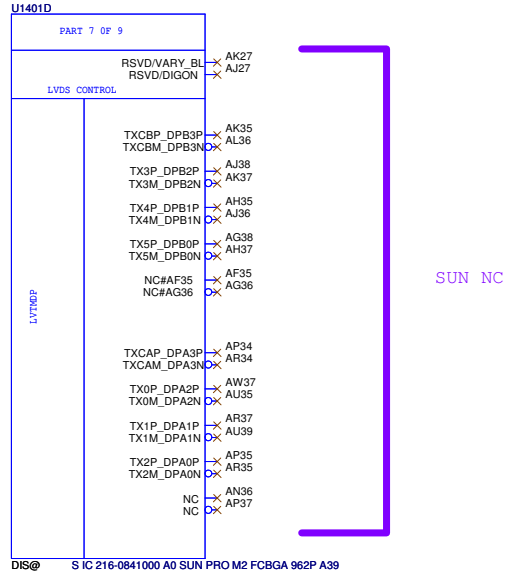
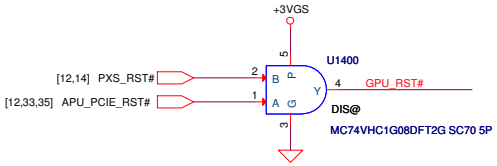


LVDS Interface





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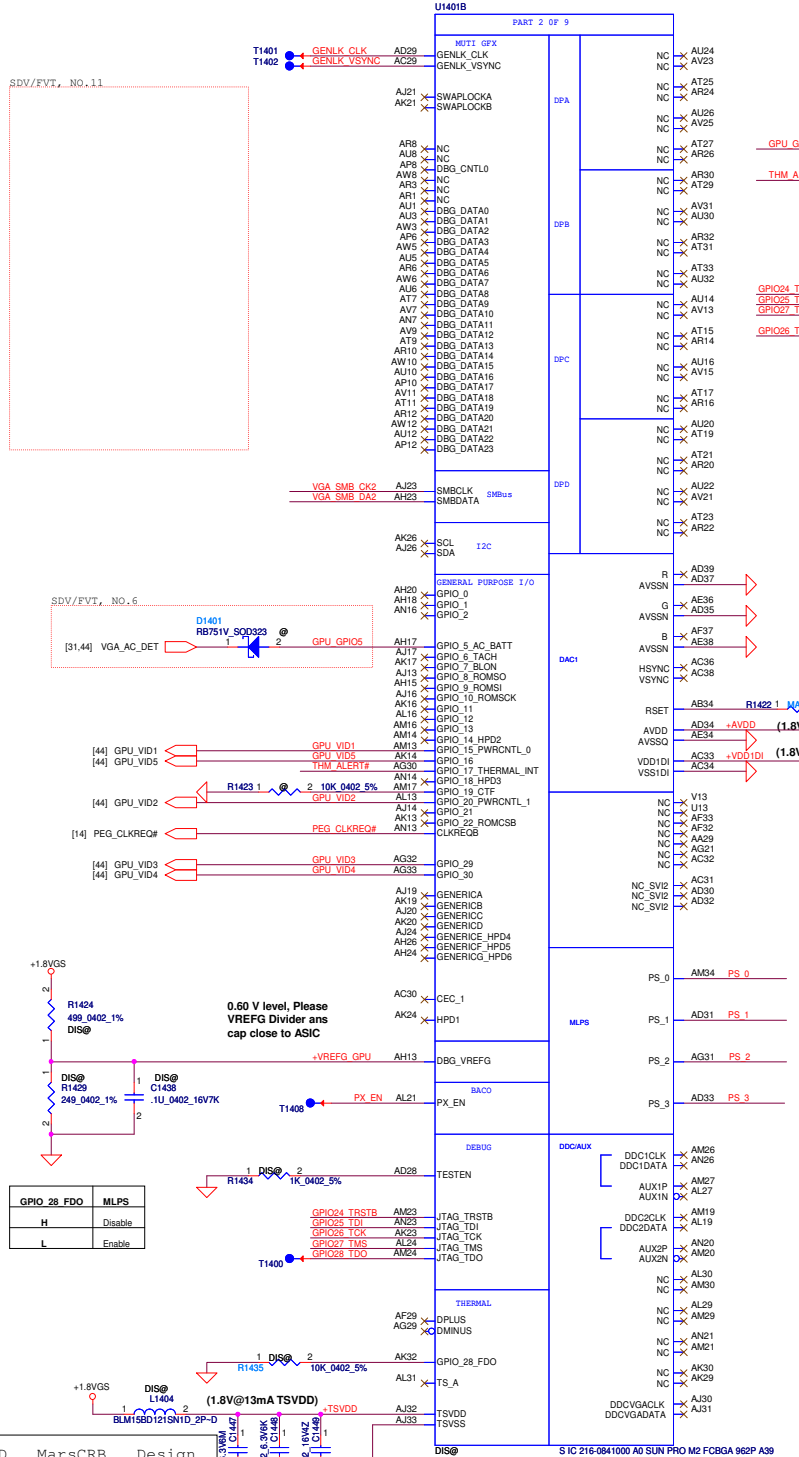
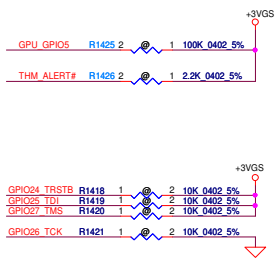
			Date: Tuesday, March 12, 2013 / Sheet 17 of 51



STRAPS



Resistor Divider Lookup Lable

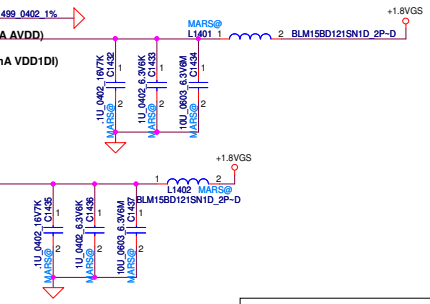
R_pu (ohm) R1430	R_pd (ohm) R1436	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are equired

Capacitor Divider Lookup Lable

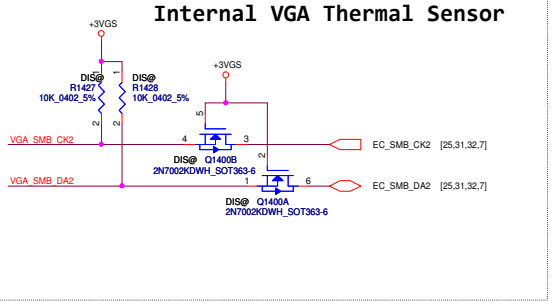
Cap (nF) C1439	Bitd [5:4]	Compal PN
680nF	00	SE00000YJ80
82nF	01	SE076823K80
10nF	10	SE074103KN0
NC	11	

AVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



VDD1DI	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

Internal VGA Thermal Sensor



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

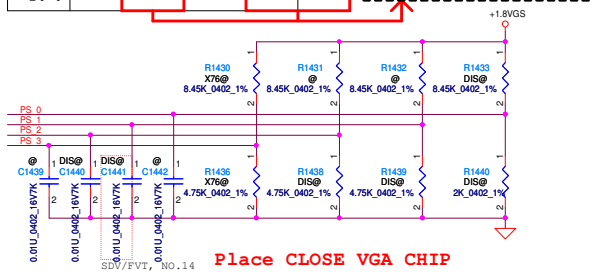
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_ENB	PS_1[4]	Transmitter Power Savings Enable 0:50% Tx output swing 1:Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	PCIE Transmitter De-emphasis Enable 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	PCIE Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped to 0) 0:GEN3 not support at power-on 1:GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	VGA control 0:VGA controller capacity enabled 1:VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	Serial ROM type or Memory Aperture Size Select If PS_2[3]=0, defines memory aperture size If PS_2[3]=1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV010 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	Enable external BIOS ROM device 0:Disabled 1:Enabled	X
AUD[1] AUD[0]	NA NA	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It isthe responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	Reserved for future ASIC	0
		NOTE:ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED	PS_1[3]	Reserved	0
RESERVED	PS_1[2]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 1	NC	8.45K	2K
PS_1[5:1]	1 1	0 0 0	NC	NC	4.75K
PS_2[5:1]	0 0	0 0 0	680 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X

Mapping to VRAM type please refer to page 04



GPIO_28_FDO	MLPS
H	Disable
L	Enable

TSVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

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Compal Electronics, Inc.

Title: ATI_Sun Pro_M2_Main_MSIC

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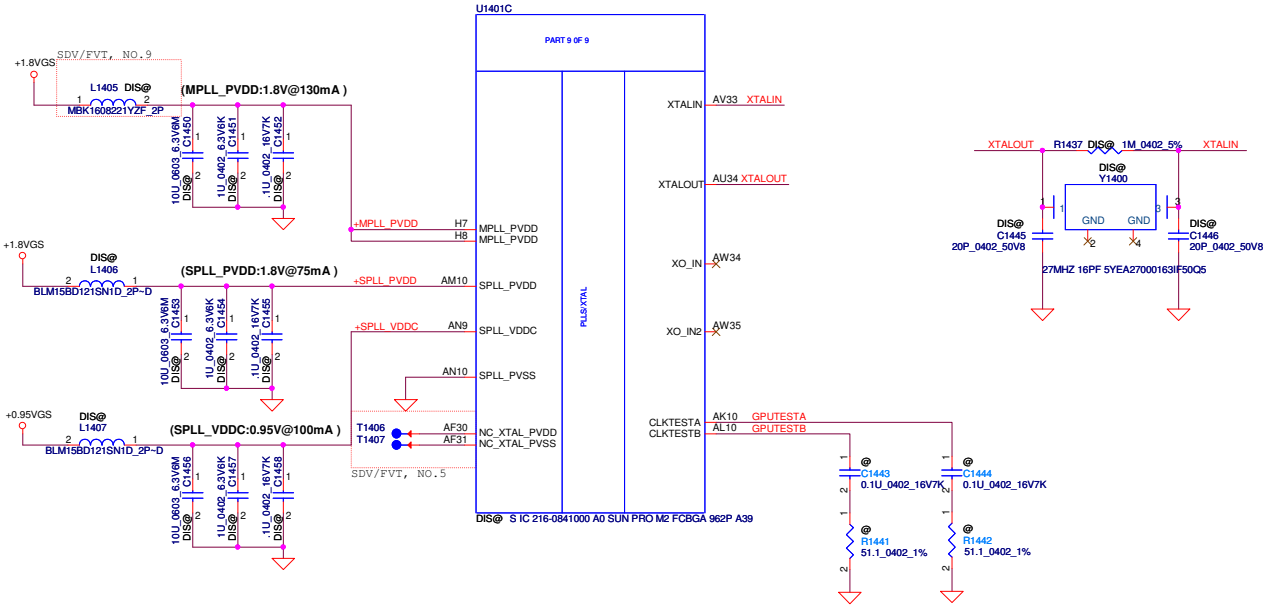
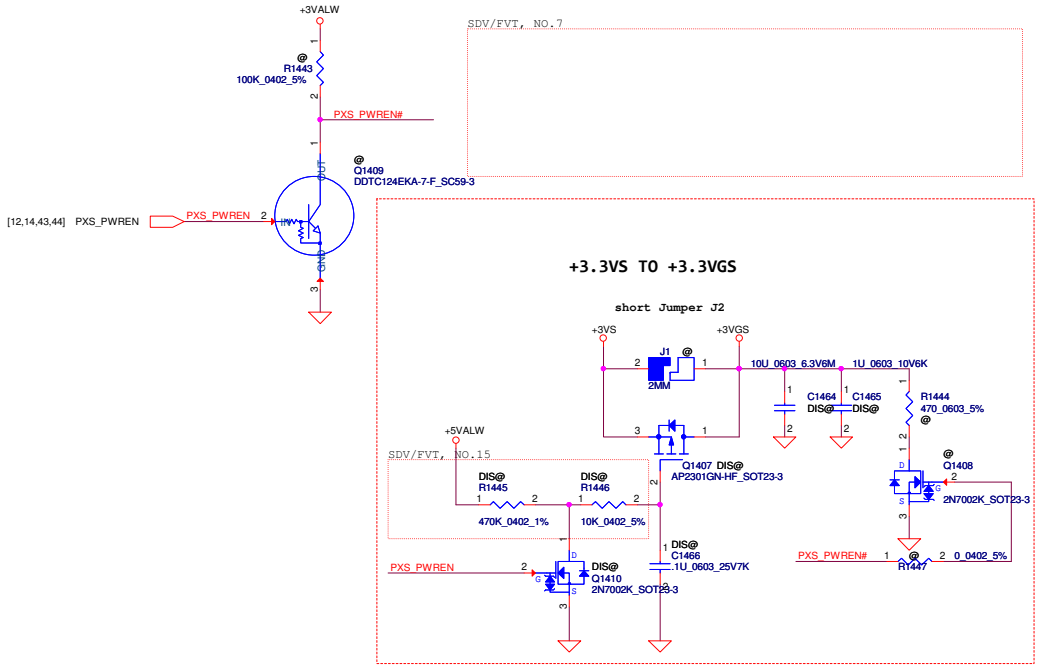
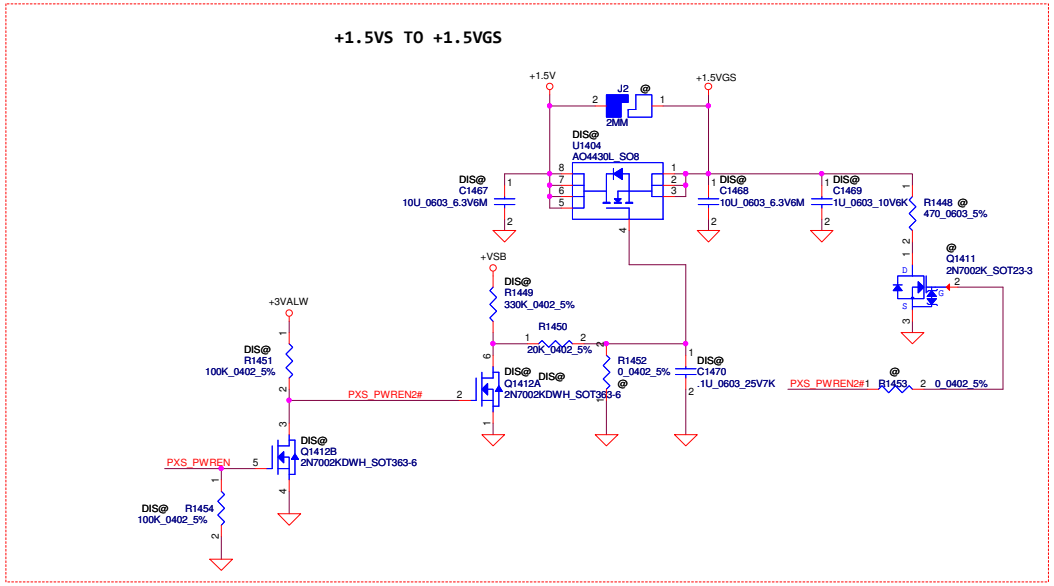
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1







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Compal Electronics, Inc.

Title: ATI_Sun Pro_M2_BACO POWER

Size: Custom | Document Number: LA-8126P | Rev: 1.0

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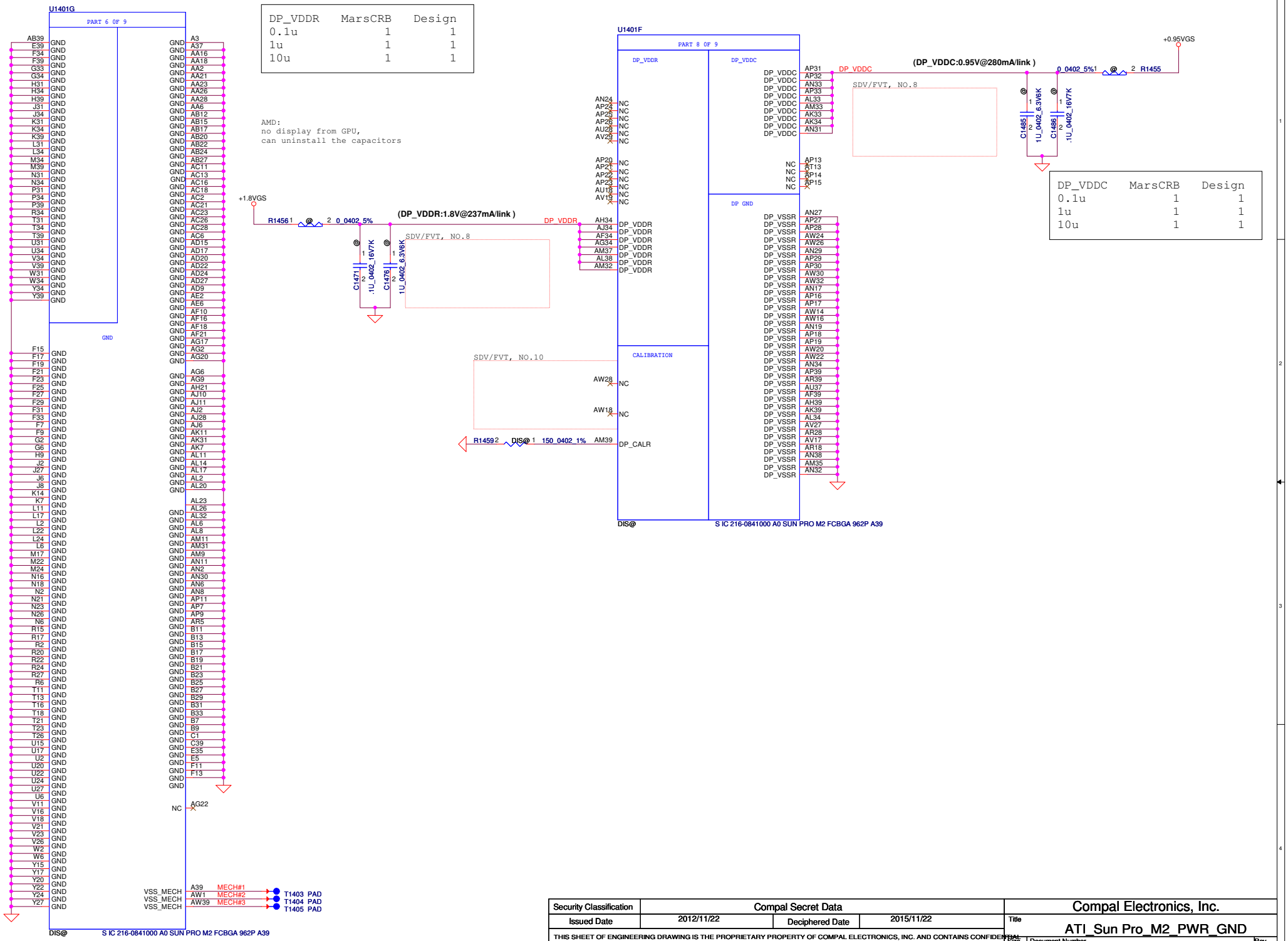

DP_VDDR	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

DP_VDDC	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

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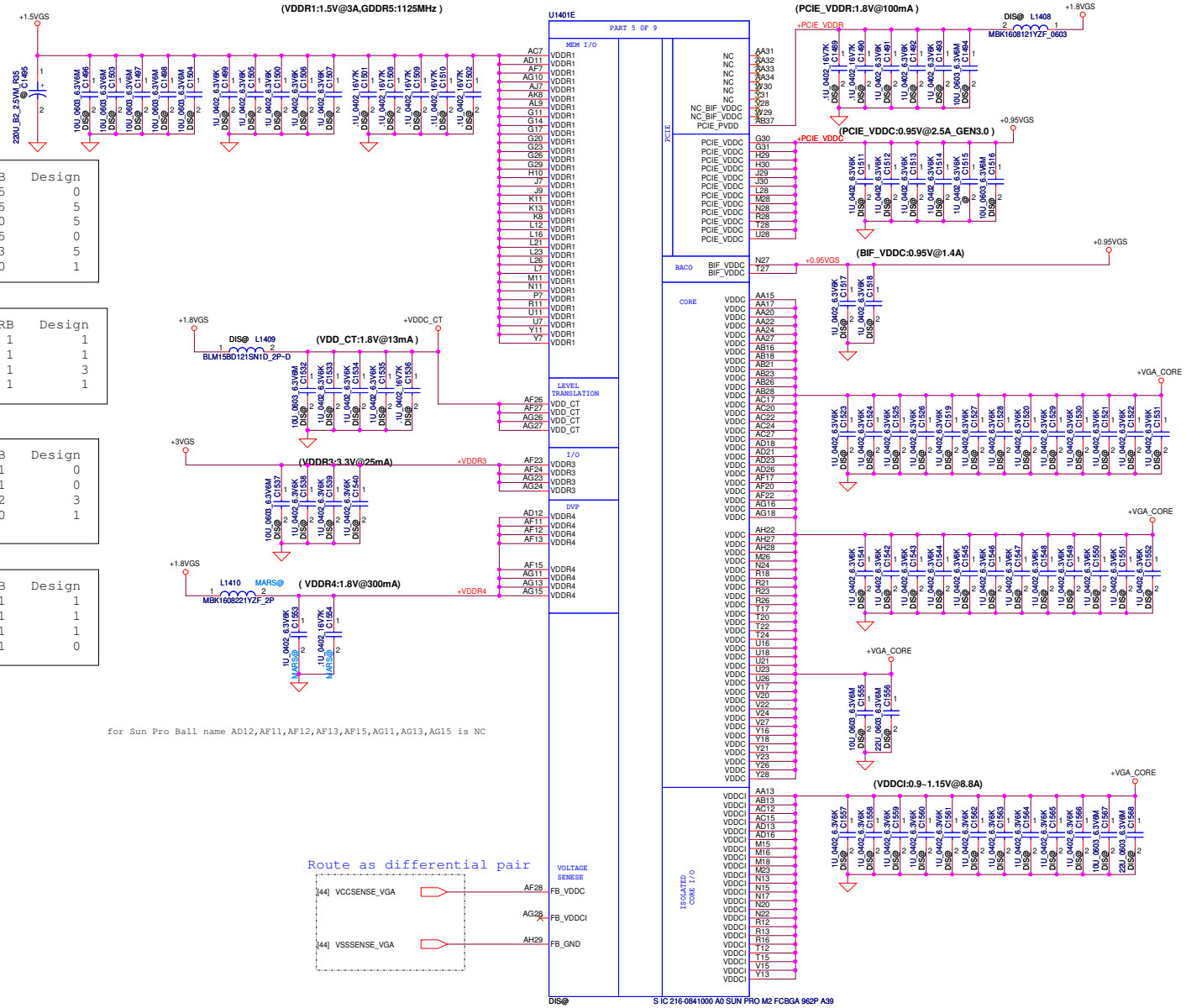
For GDDR5, MVDDQ = 1.5V



VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0

for Sun Pro Ball name AD12,AF11,AF12,AF13,AF15,AG11,AG13,AG15 is NC

PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

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Title: ATI_Sun Pro_M2_Power

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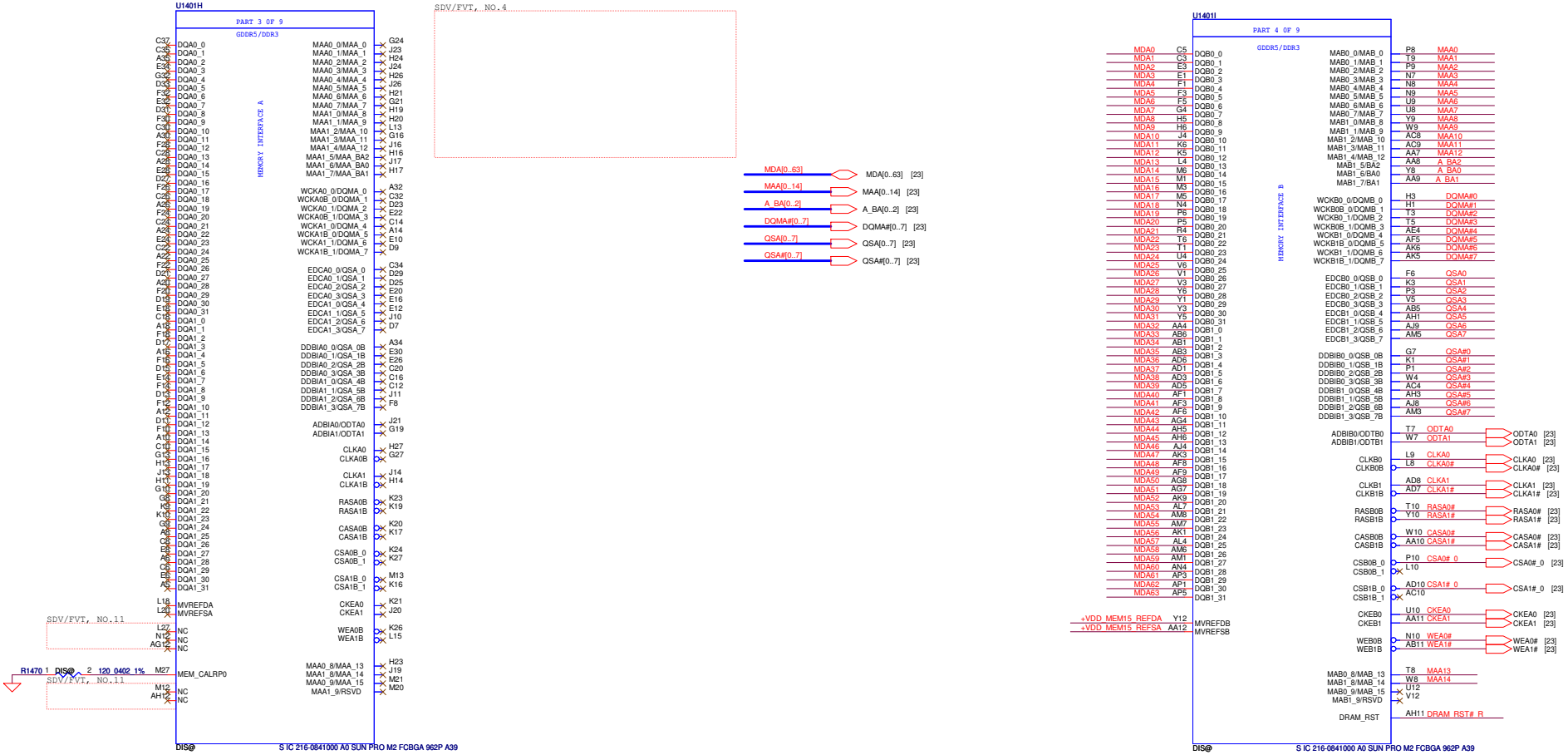

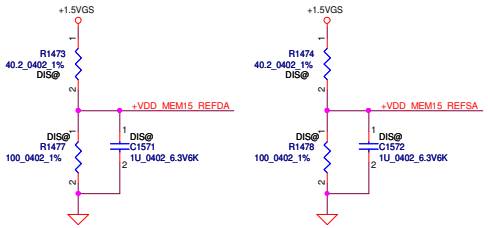

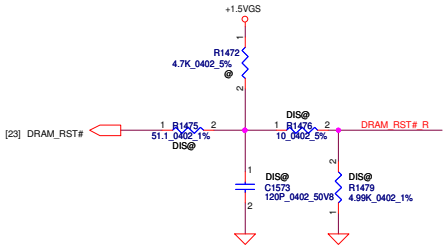

DRAM_RST# is a daisy-chain net that connects to all VRAM

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

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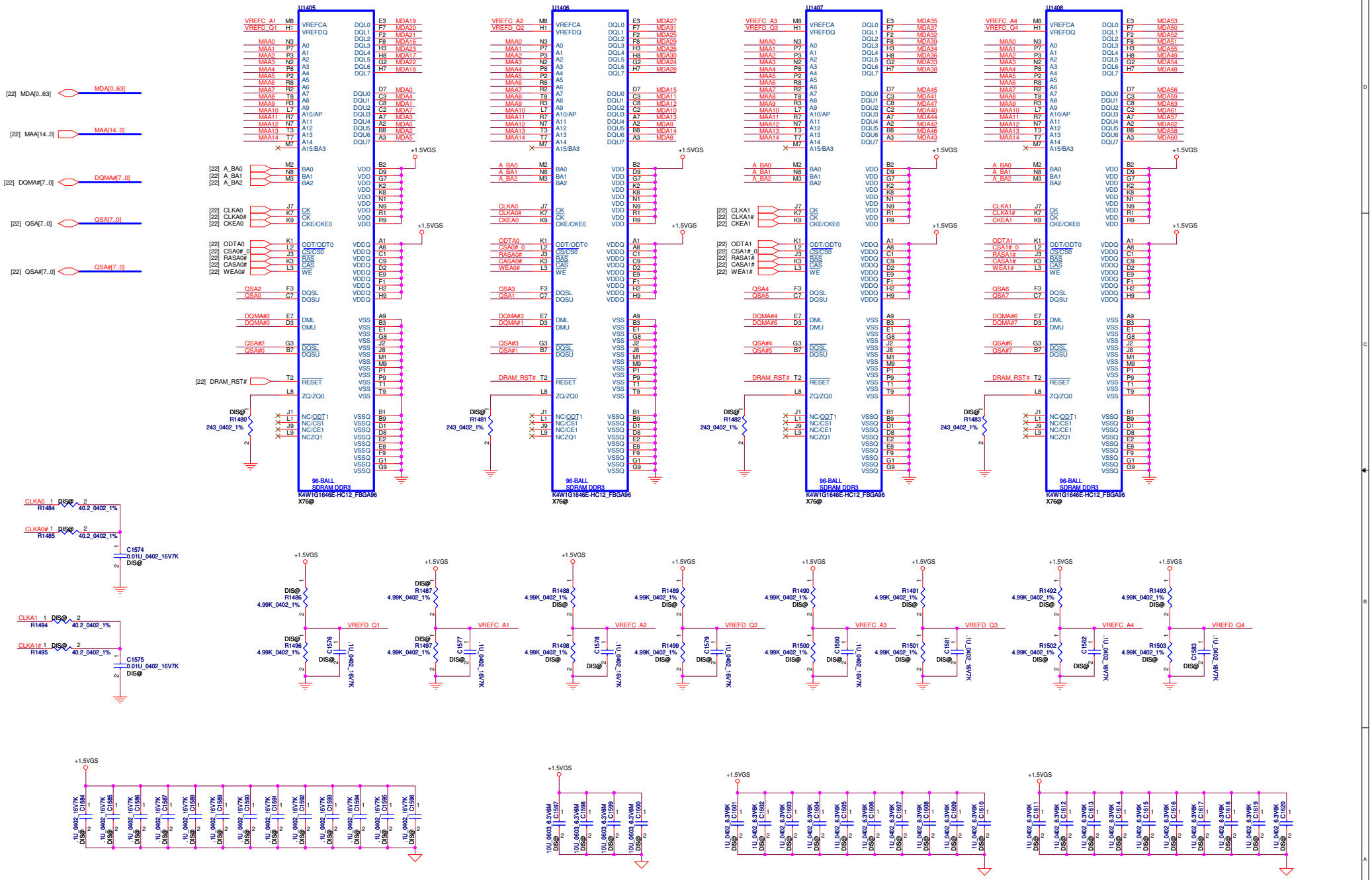
The Seymour M2 only support channel B (64 bit),
this page unmount all parts



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Compal Electronics, Inc.

Title: ATI Sun Pro_M2_VRAM_A

Size: C | Document Number: LA-8126P | Rev: 1.0

Date: Tuesday, March 12, 2013 | Sheet 23 of 51

The Mars Pro M2 only support channel B (64 bit)

SDV/FVT, NO.4

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Title: ATI_Sun_Pro_M2_VRAM_B

Size: C | Document Number: LA-8126P | Rev: 1.0

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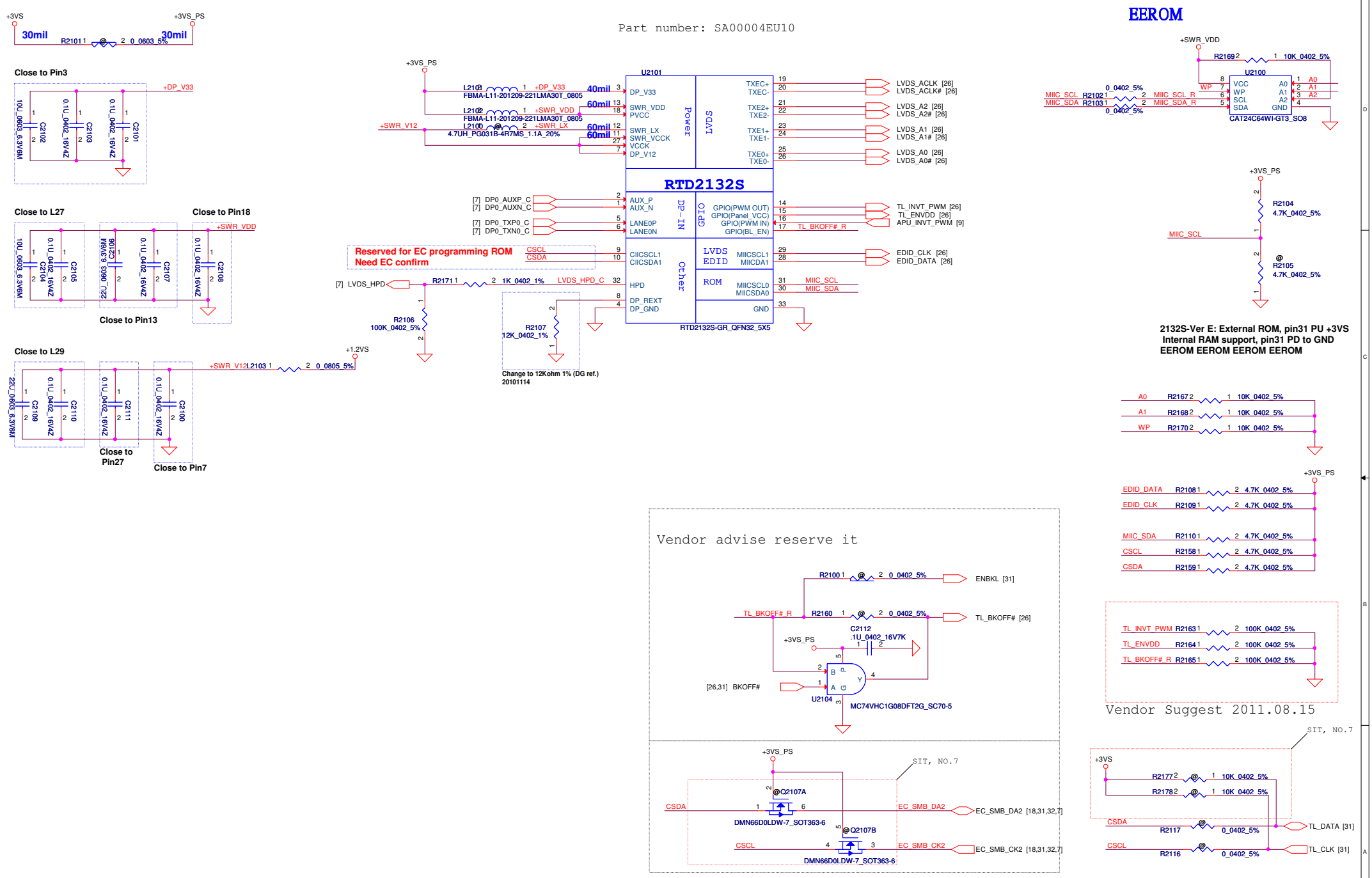

Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

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Compal Electronics, Inc.

Title: LVDS Translator - RTD2132S

Size: Custom | Document Number: LA-8126P | Rev: 1.0

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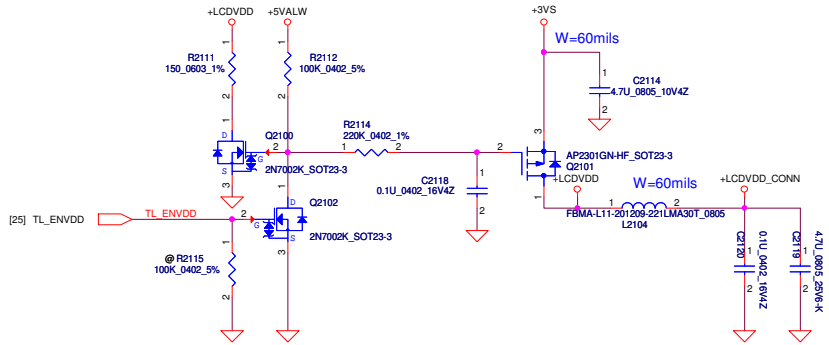
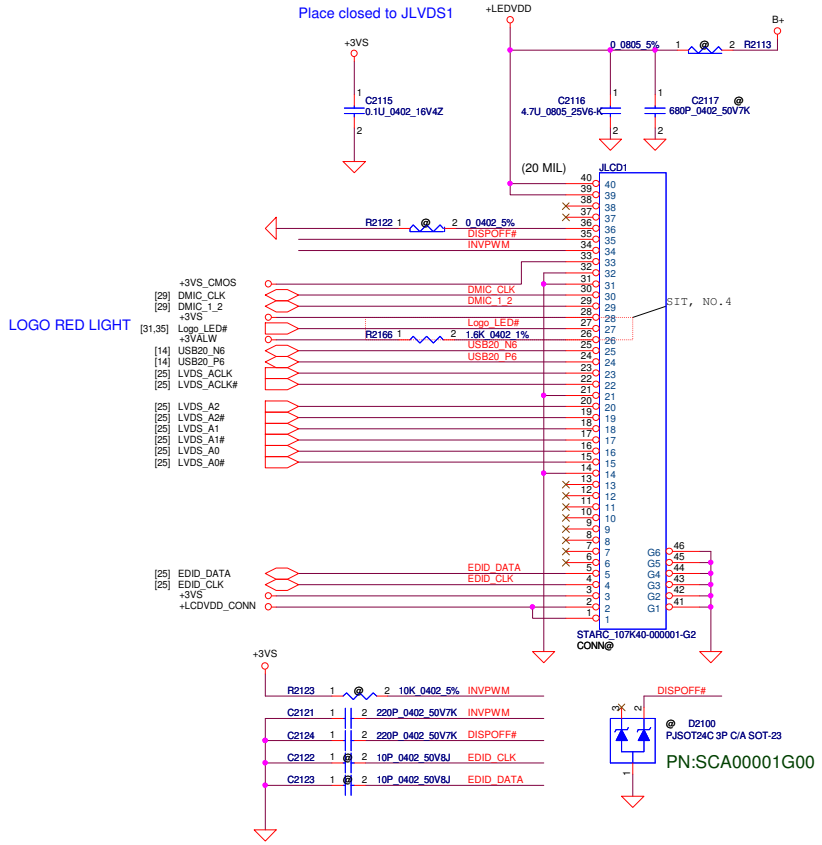
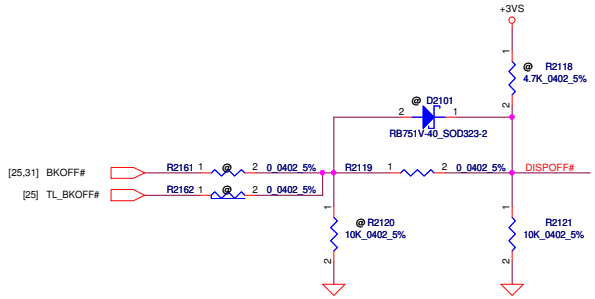
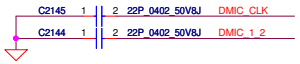
LCD POWER CIRCUIT

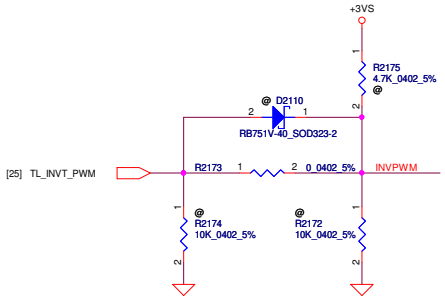


LCD/LED PANEL Conn.

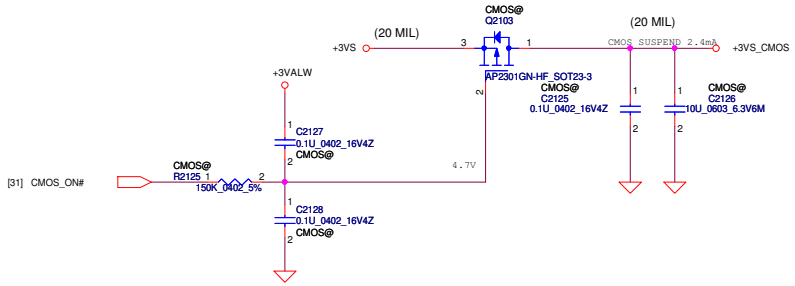








CMOS Camera Conn



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Compal Electronics, Inc.

Title: LVDS CONN/CAMERA

Size: Custom | Document Number: LA-8126P | Rev: 1.0

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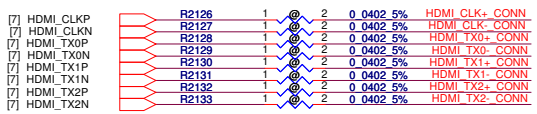
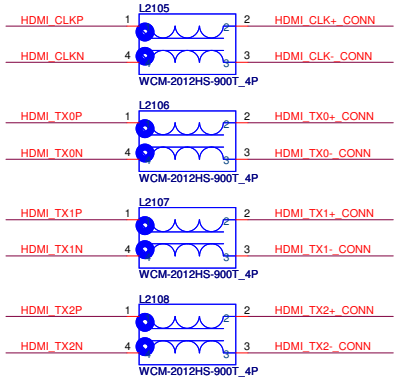
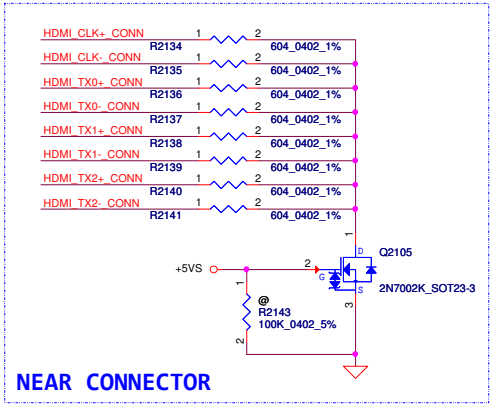
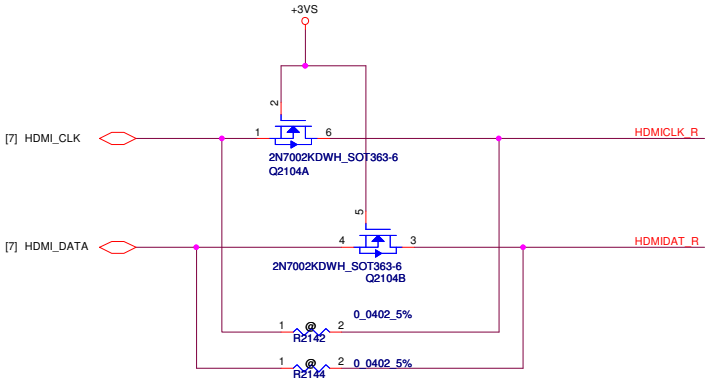
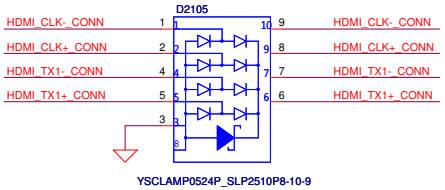


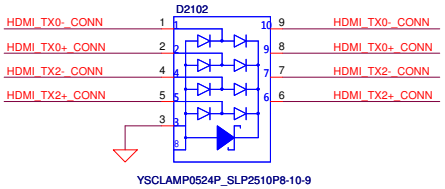


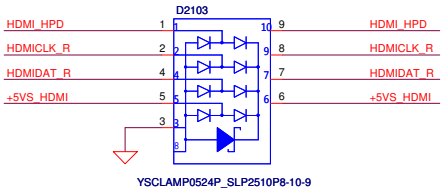


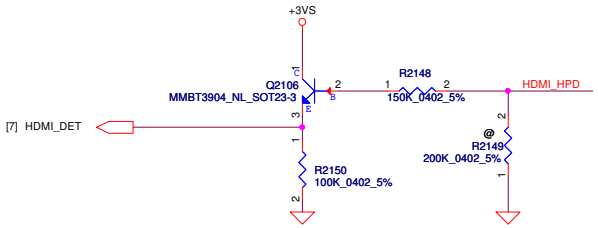


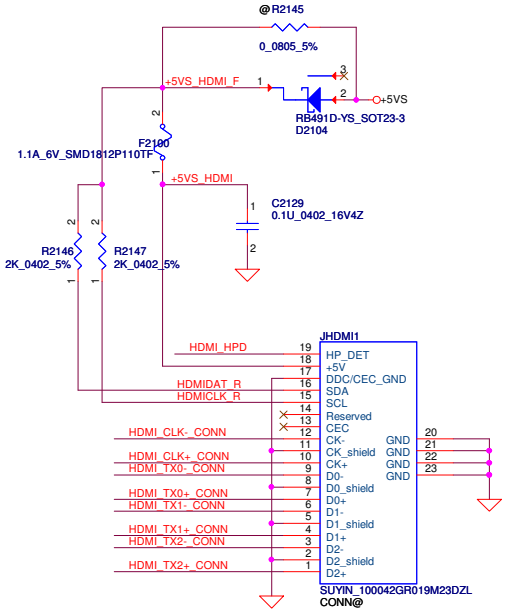
ESD Request











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Compal Electronics, Inc.

Title: HDMI Connector

Size: B/25 Custom | Document Number: LA-8126P | Rev: 1.0

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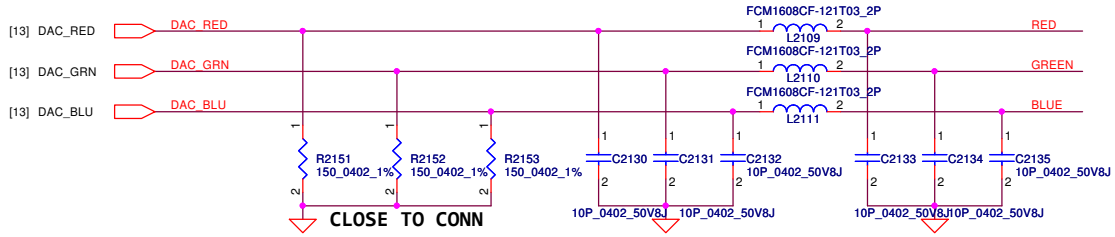
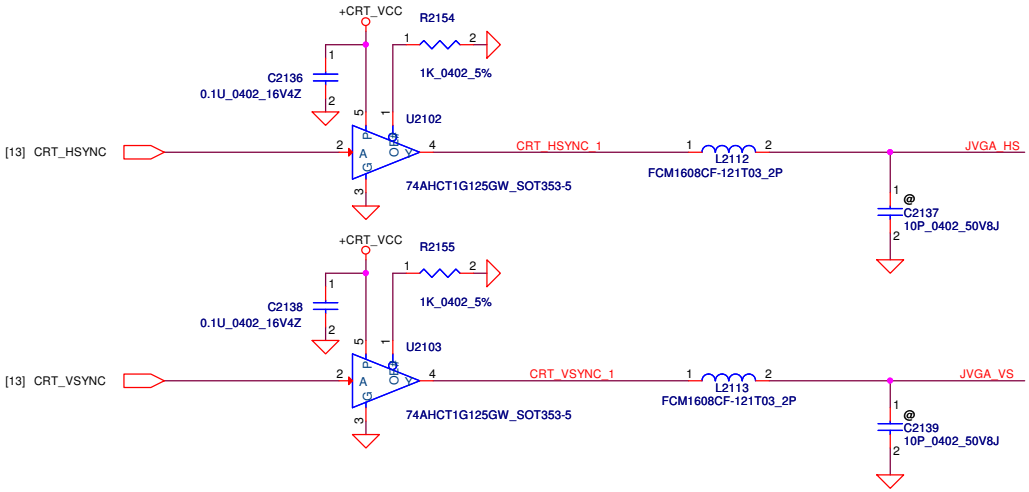
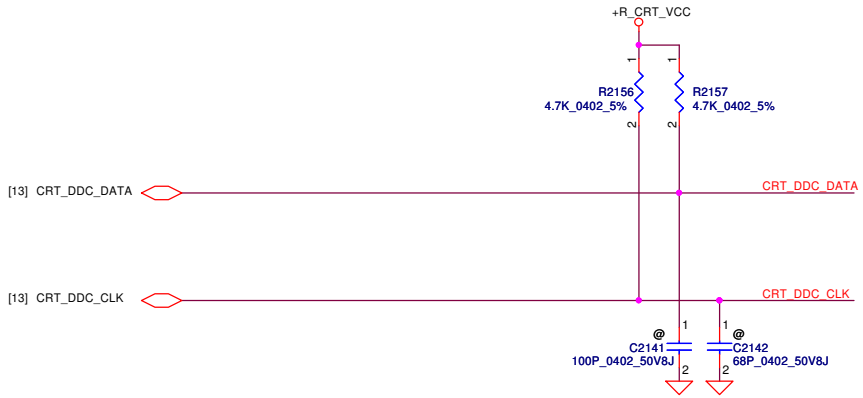
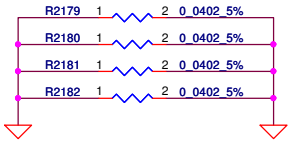
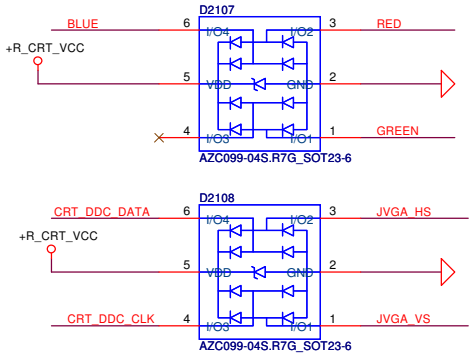




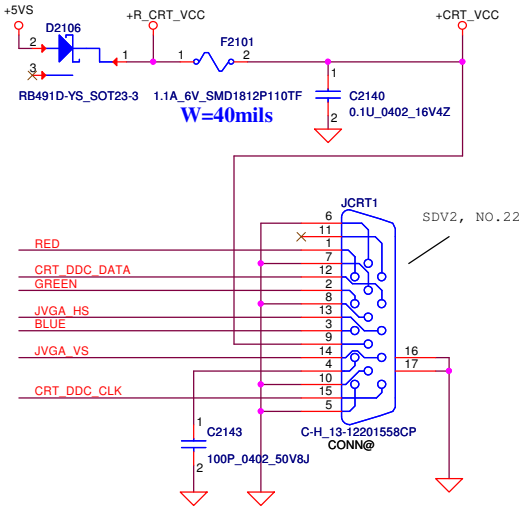




ESD Request



CRT Connector



AMD check list update
20101110

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Compal Electronics, Inc.

Title: CRT Connector

Size: Custom | Document Number: LA-8126P | Rev: 1.0

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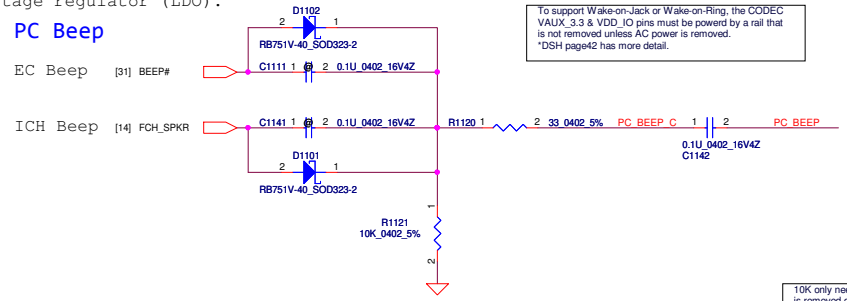
CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

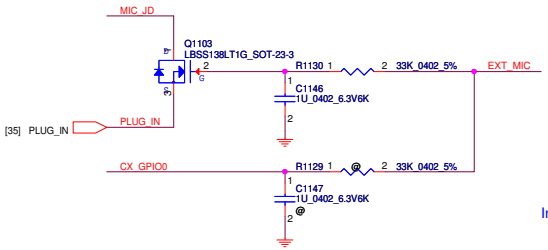
Layout Note:Path from +5VS to Pin12, Pin15 must be very low resistance (<0.01 ohms)

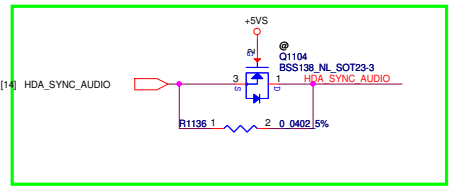
To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 & VDD_IO pins must be powerd by a rail that is not removed unless AC power is removed.
*DSH page42 has more detail.

PC Beep



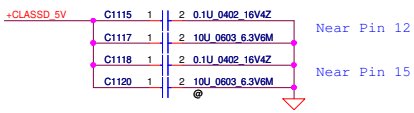
Combo Jack detect (normal close)



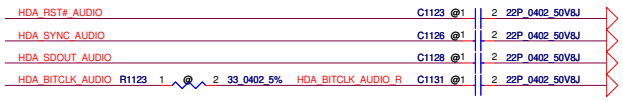


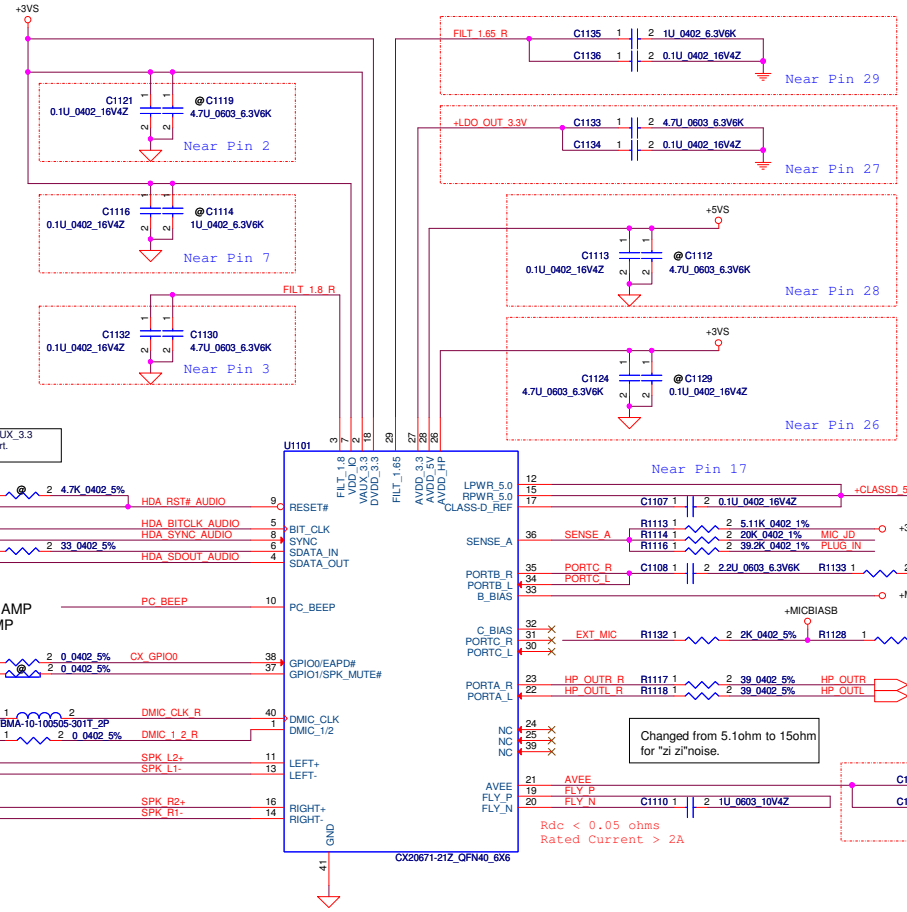
potential leakage concern

Decoupling CAP



EMI





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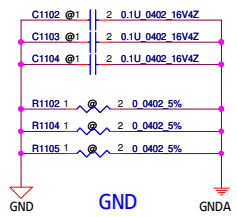
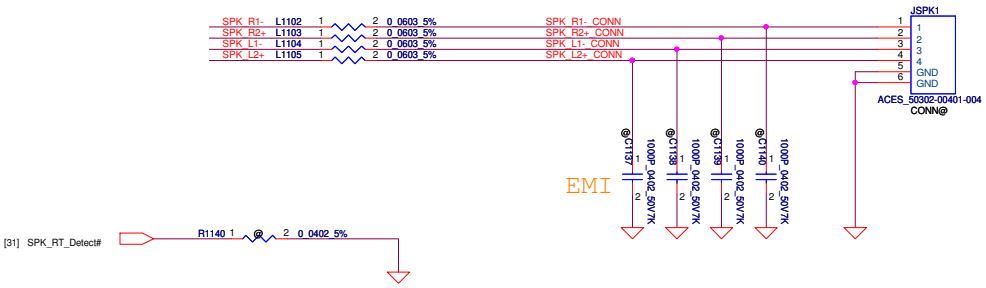


Internal Speaker



Note.
QALEA 14" => JSPK1 => 4Pin
QALEB 15" => JSPK1 => 6Pin

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Compal Electronics, Inc.

Title: HD Audio Codec CX20671

Size: Custom | Document Number: LA-8126P | Rev: 1.0

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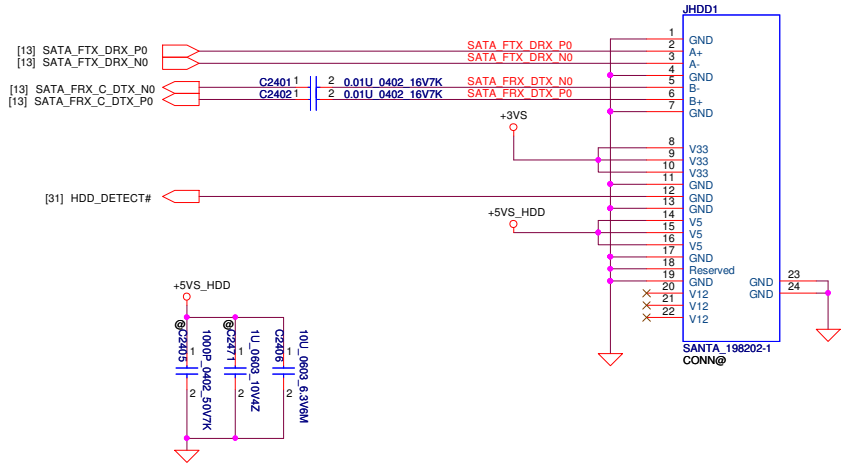
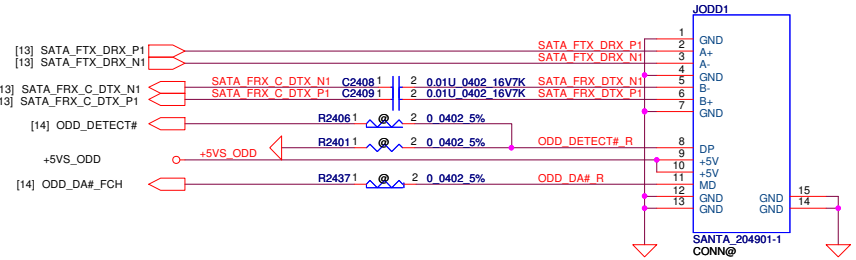
SATA HDD Conn.

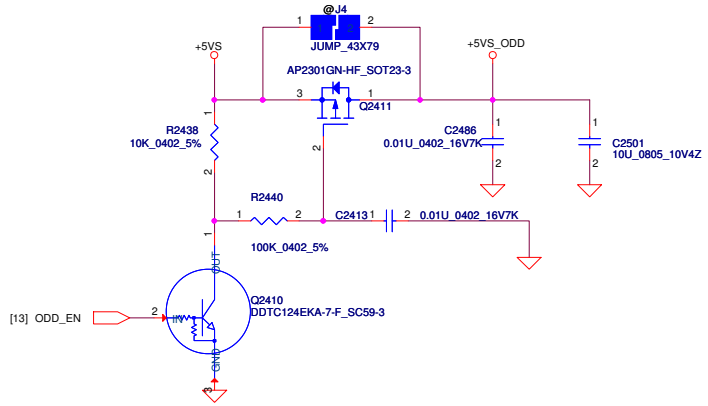


SATA ODD Conn.

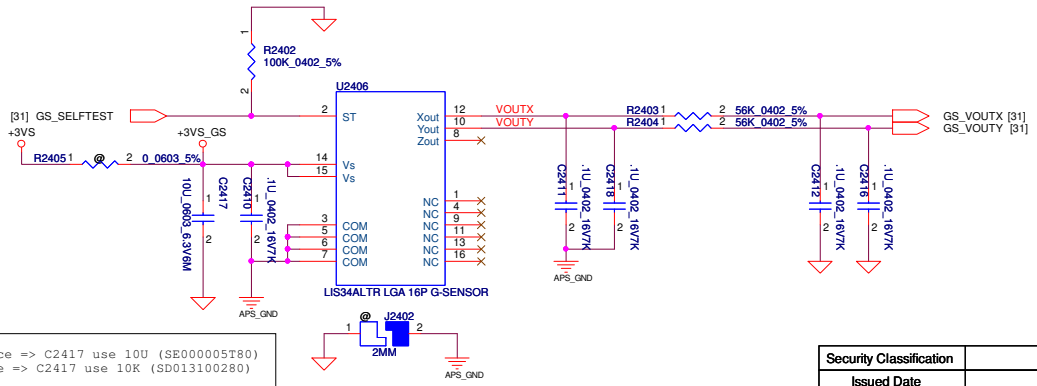


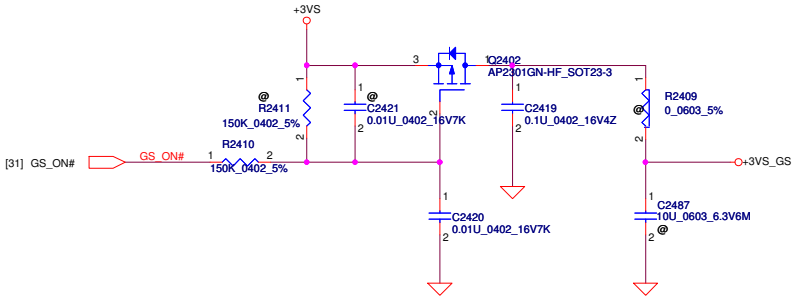
Note.
QALEA 14" => JODD1
QALEB 15" => JODD2

ODD Power Control



APS G-Sensor





Note.
Main Source => C2417 use 10U (SE000005T80)
2nd Source => C2417 use 10K (SD013100280)

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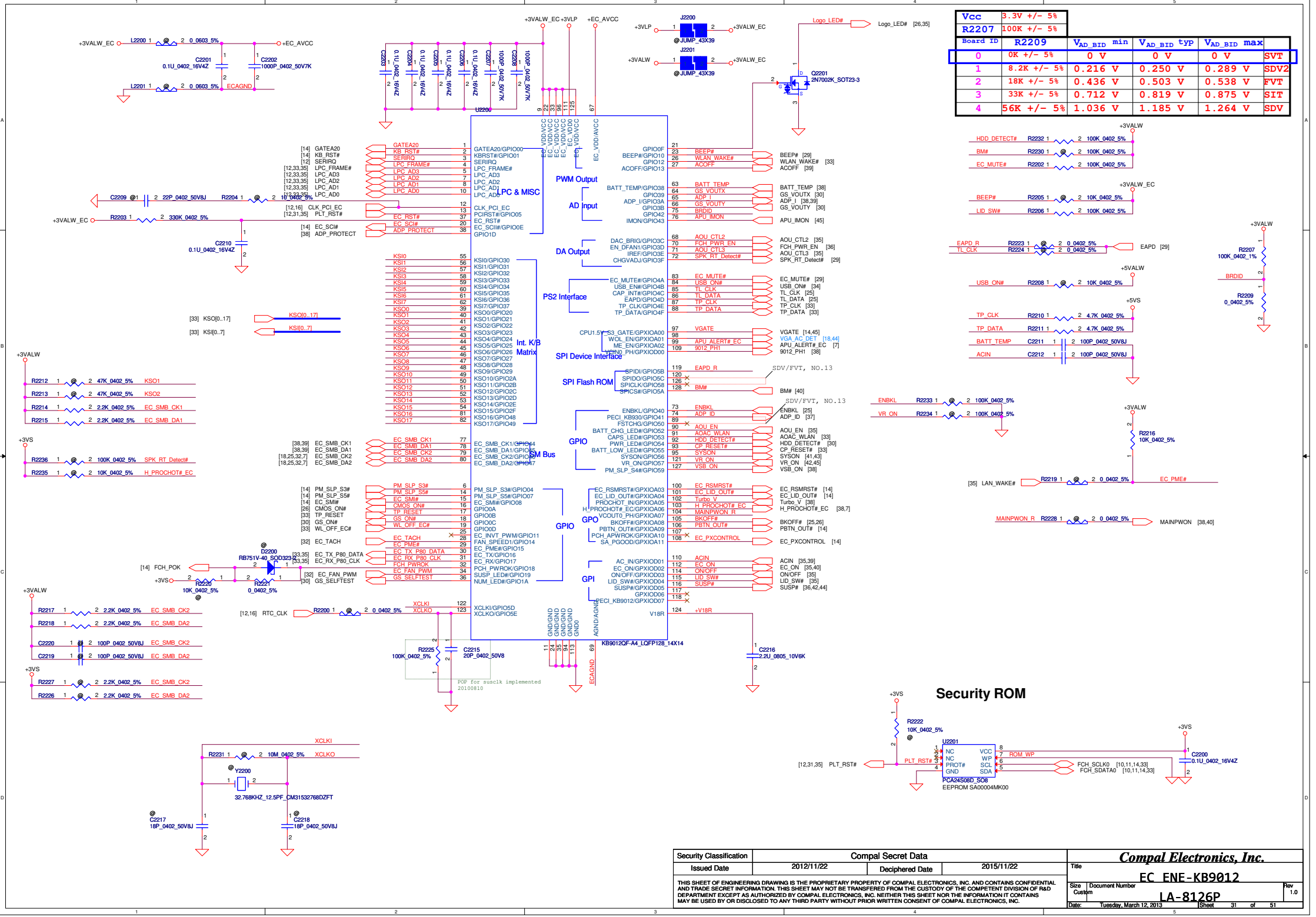
Compal Electronics, Inc.

Title: HDD/ODD/G-Sensor

Size: B | Document Number: LA-8126P | Rev: 1.0

Date: Tuesday, March 12, 2013 | Sheet 30 of 51



Vcc	3.3V +/- 5%				
R2207	100K +/- 5%				
Board ID	R2209	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0K +/- 5%	0 V	0 V	0 V	SVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	SDV2
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	FVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SIT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	SDV

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Compal Electronics, Inc.

Title: EC ENE-KB9012

Size: Custom | Document Number: LA-8126P | Rev: 1.0

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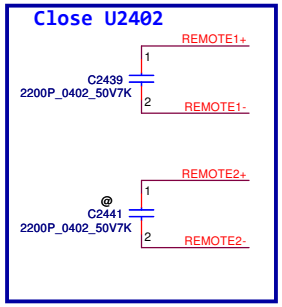
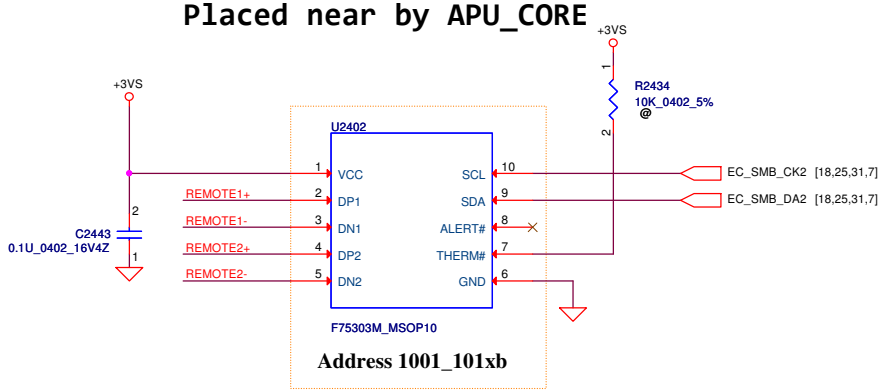
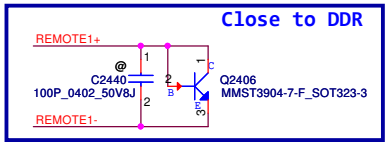
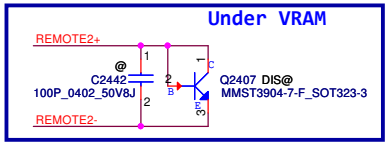
Fintek Thermal sensor
Placed near by APU_CORE









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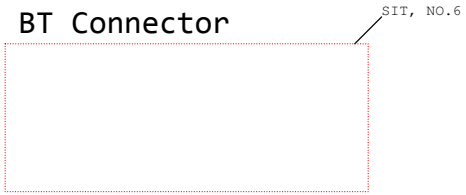
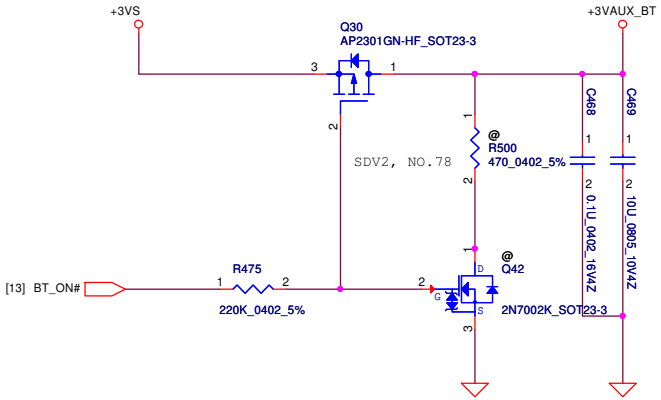
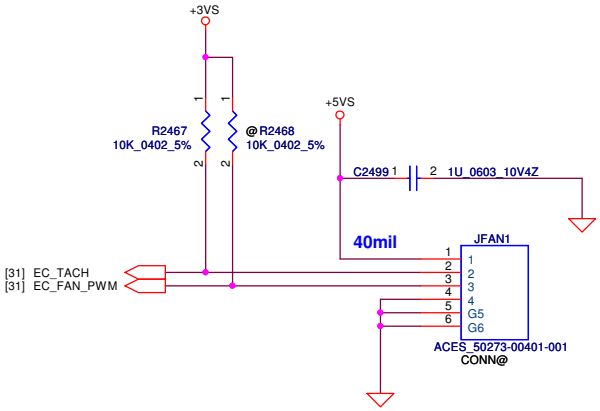
Trace width/space:10/10 mil
Trace length:<8"

BT Connector





FAN1 Conn



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Issued Date	2012/11/22	Deciphered Date	2015/11/22

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Compal Electronics, Inc.

Title: Thermal/FAN/BT

Size: B | Document Number: LA-8126P | Rev: 1.0

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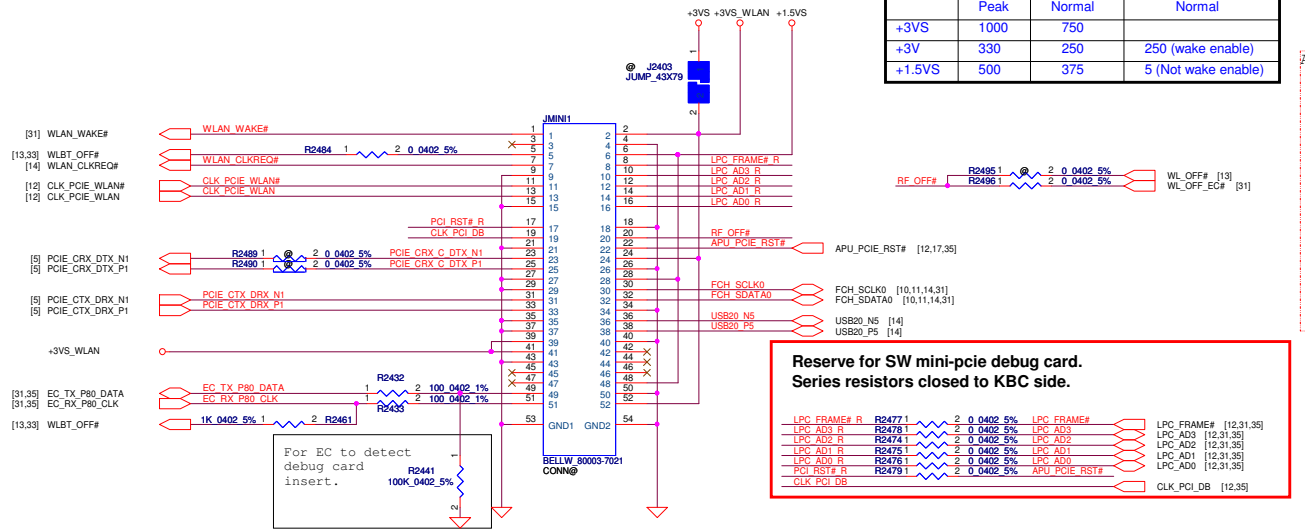
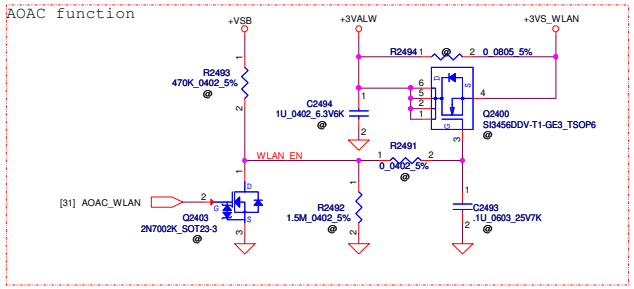
WLAN Conn

Mini Card Power Rating

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



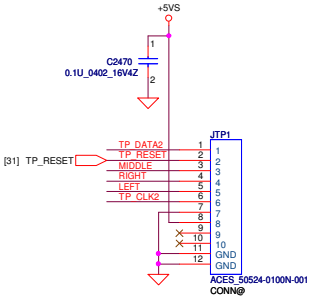


For AOAC assessment
+3VS_WLAN path:
1. +3VS (default)
2. +3VALW
3. +3VALW + Switch

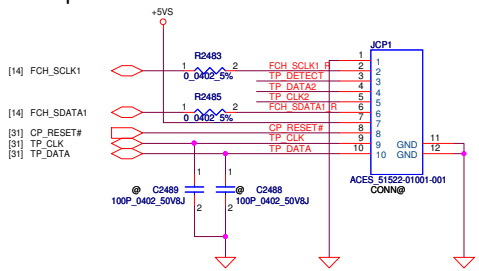
INT_KBD Conn.

CONN PIN define need double check

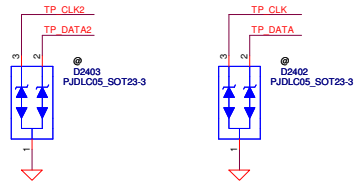
Track Point Conn

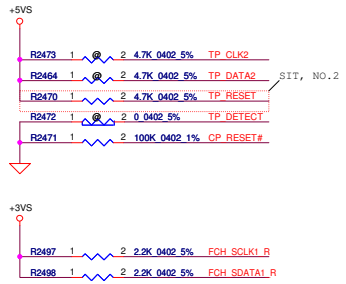


Click pad 10PIN

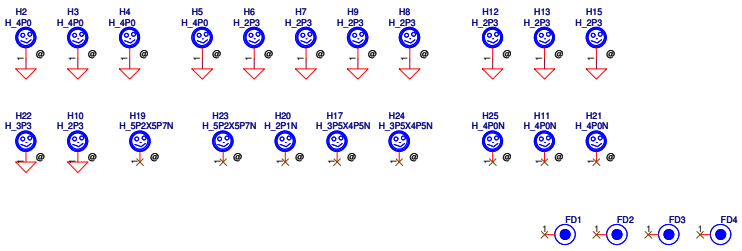


ESD Request





Screw Holes



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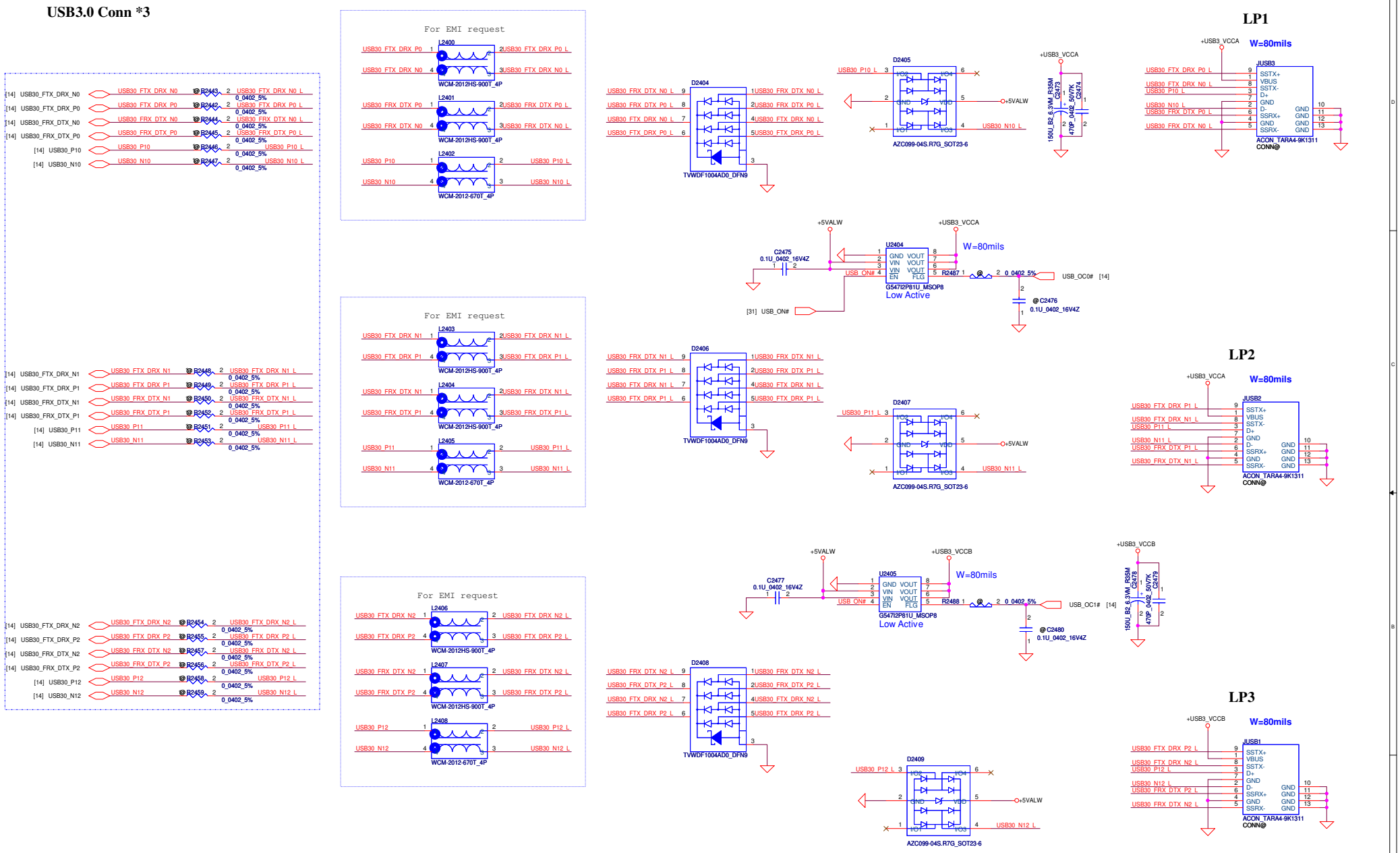
Compal Electronics, Inc.

Title: TP/KBD/Screw Hole/Debug

Size: C | Document Number: LA-8126P | Rev: 1.0

Date: Tuesday, March 12, 2013 | Sheet 33 of 51

USB3.0 Conn *3



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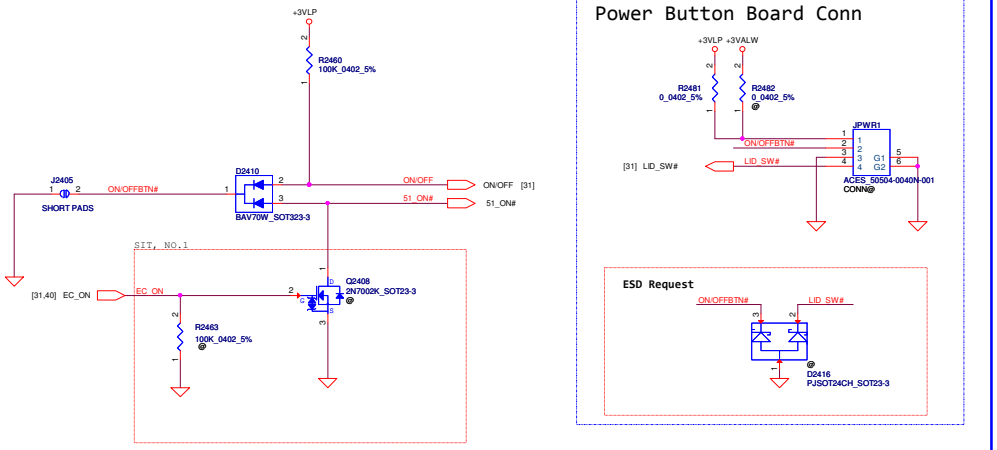
Compal Electronics, Inc.

Title: USB 3.0 Conn

Size: C | Document Number: LA-8126P | Rev: 1.0

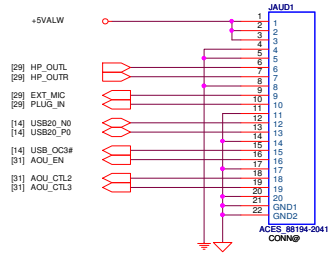
Date: Tuesday, March 12, 2013 | Sheet 34 of 51

ON/OFF switch

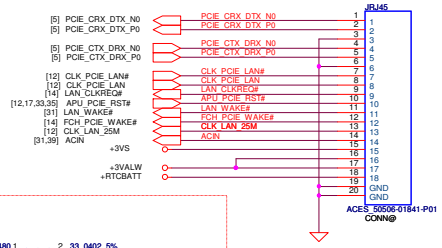


Power Button Board Conn

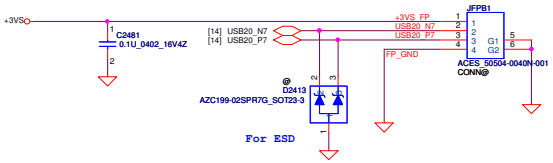
USB2.0/Audio Jack SB CONN



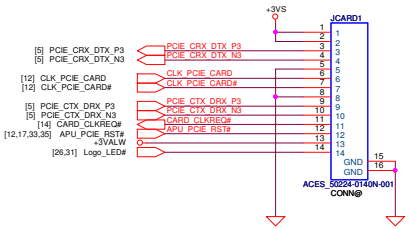
Lan Conn



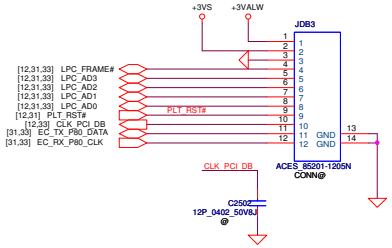
Finger Printer



Card Reader



Debug Conn.



Security Classification	Compal Secret Data		
Issued Date	2012/11/22	Deciphered Date	2015/11/22

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Compal Electronics, Inc.

Title: Sub Board

Size: Custom | Document Number: LA-8126P | Rev: 1.0

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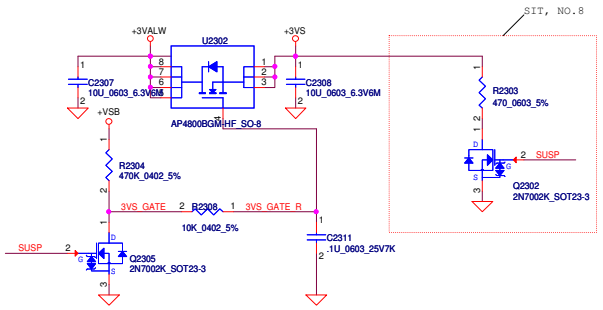
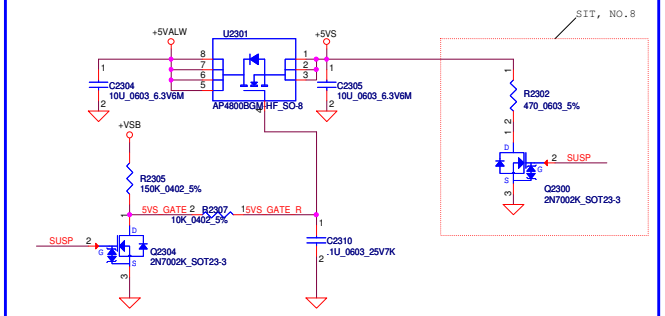
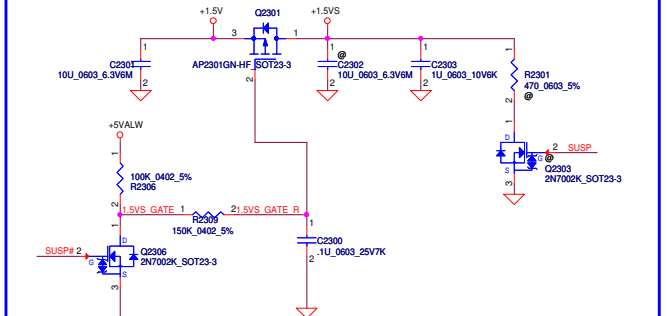
+3VALW TO +3VS



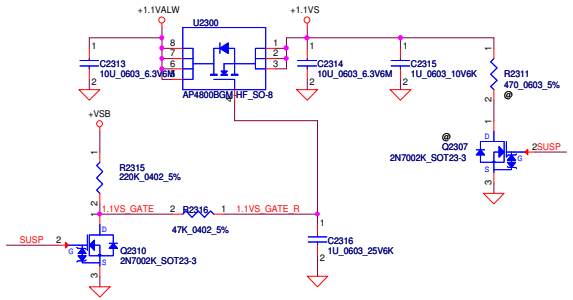
+5VALW TO +5VS



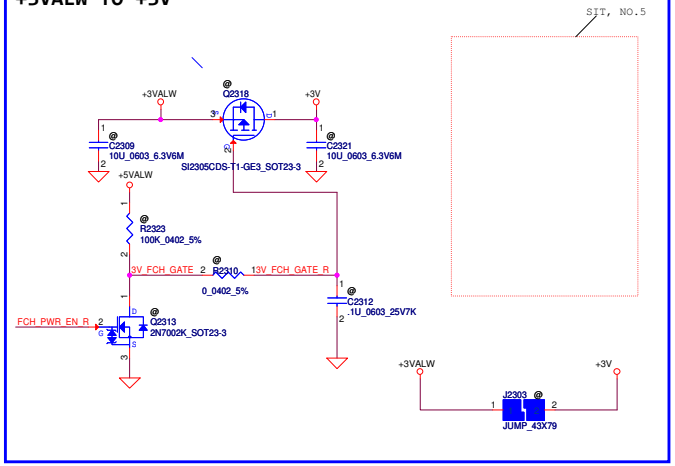
+1.5V to +1.5VS



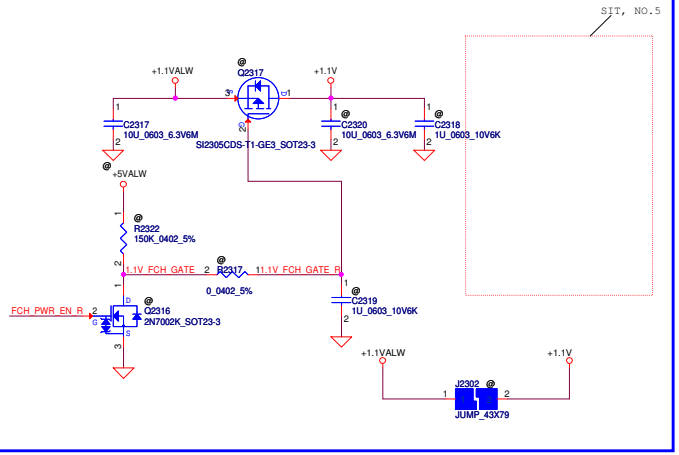
+1.1VALW to +1.1VS

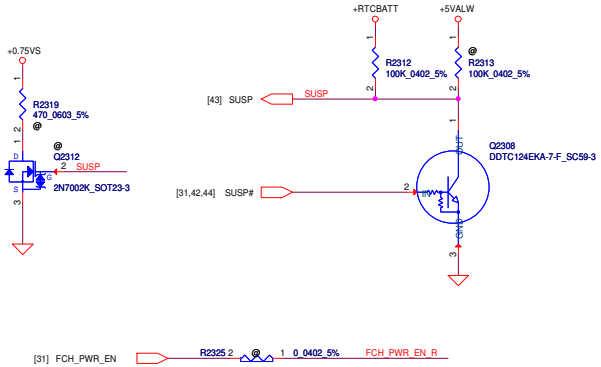


+3VALW TO +3V



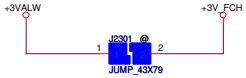
+1.1VALW to +1.1V





+3VALW TO +3V_FCH

Short J2301 for PCH VCCSUS3.3



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Compal Electronics, Inc.

Title: DC_V_TO_VS_INTERFACE

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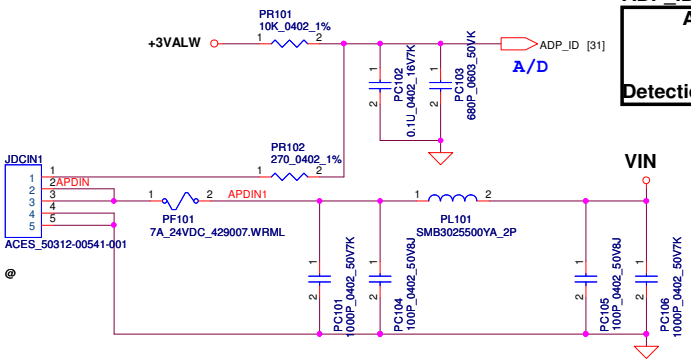
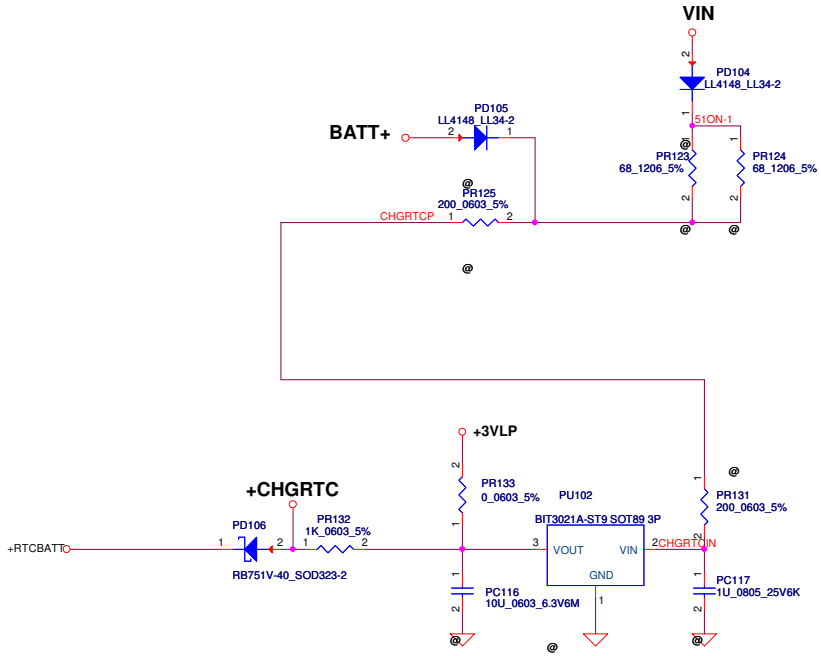
ADP_ID

AC Adapter	135W	90W	65W
R(K ohm)	0	open	10
ADP_ID(V)	0	3.3	1.65
Detection voltage	<0.33	>2.64	1.32~1.98





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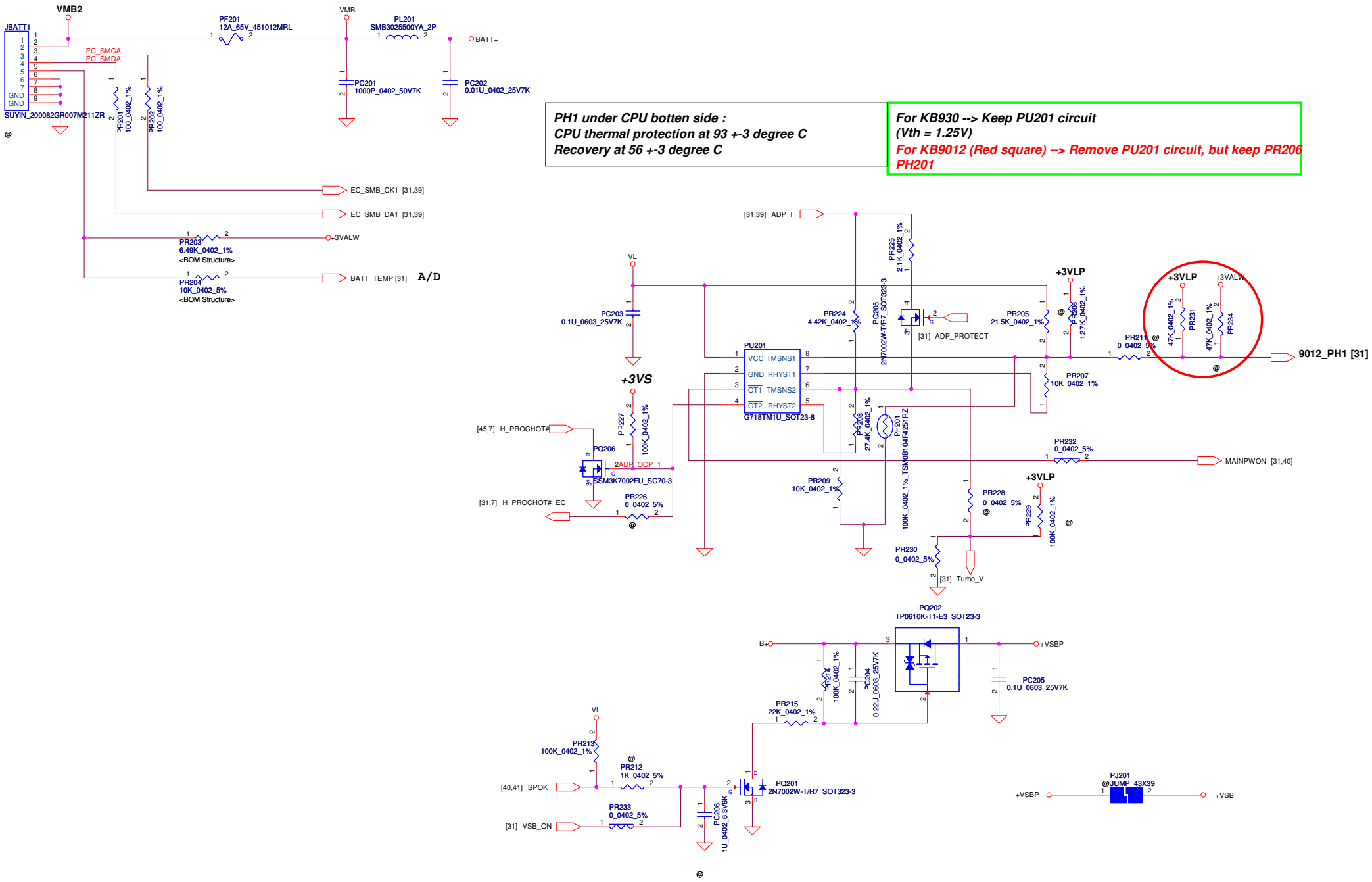
Compal Electronics, Inc.

Title: ***PWR DCIN / Vin Detector /Pre-charge***

Size: Custom | Document Number | Rev: 1.0

Date: Tuesday, March 12, 2013 | Sheet 37 of 51



Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

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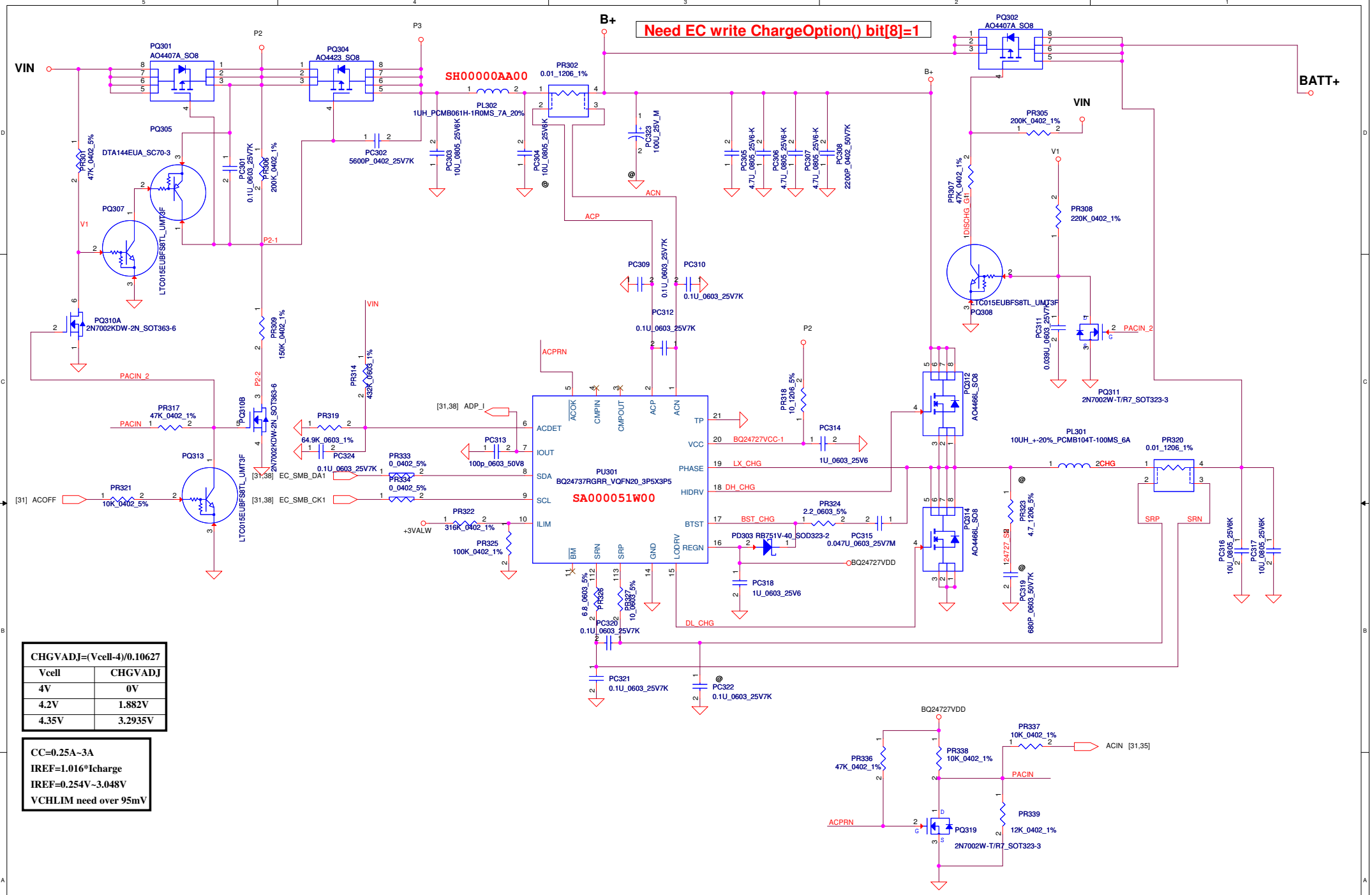
Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number | Rev 1.0

Date: Tuesday, March 12, 2013 | Sheet 38 of 51



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

Title: **CHARGER**

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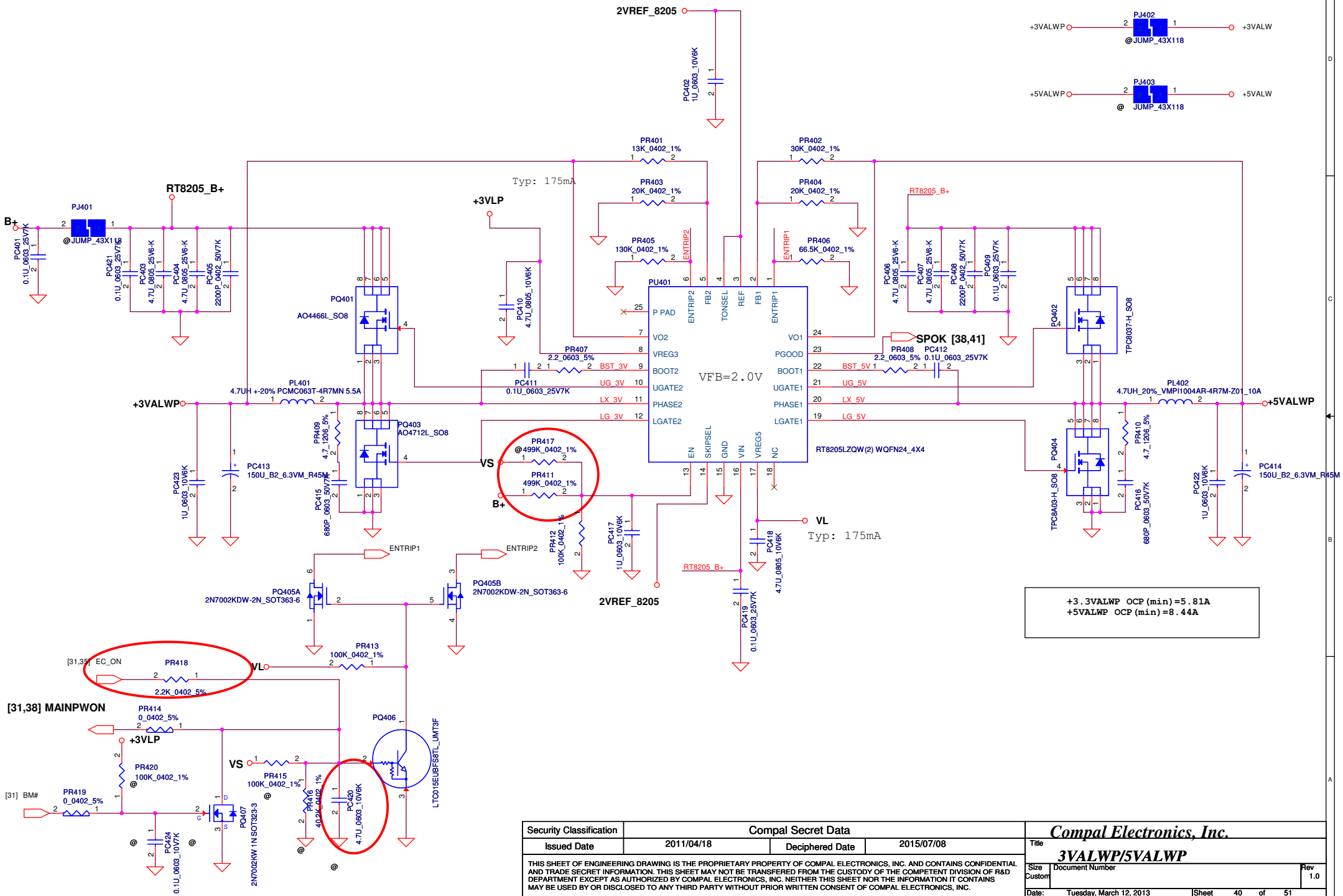
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

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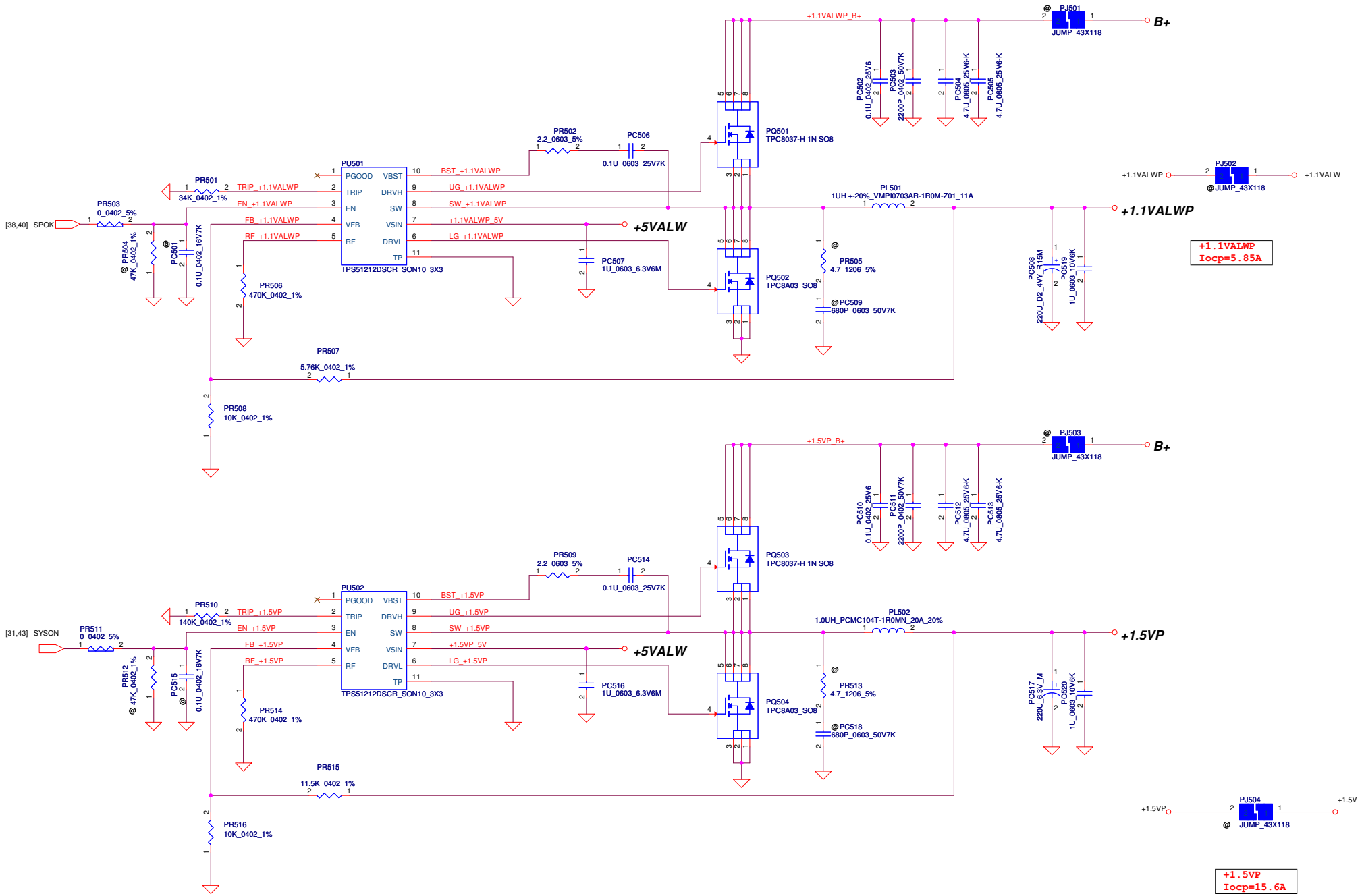
Compal Electronics, Inc.

Title: **3VALWP/5VALWP**

Size: Custom | Document Number | Rev 1.0

Date: Tuesday, March 12, 2013 | Sheet 40 of 51



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Issued Date	2011/04/18	Deciphered Date	Title: +1.1VALWP/+1.5VP

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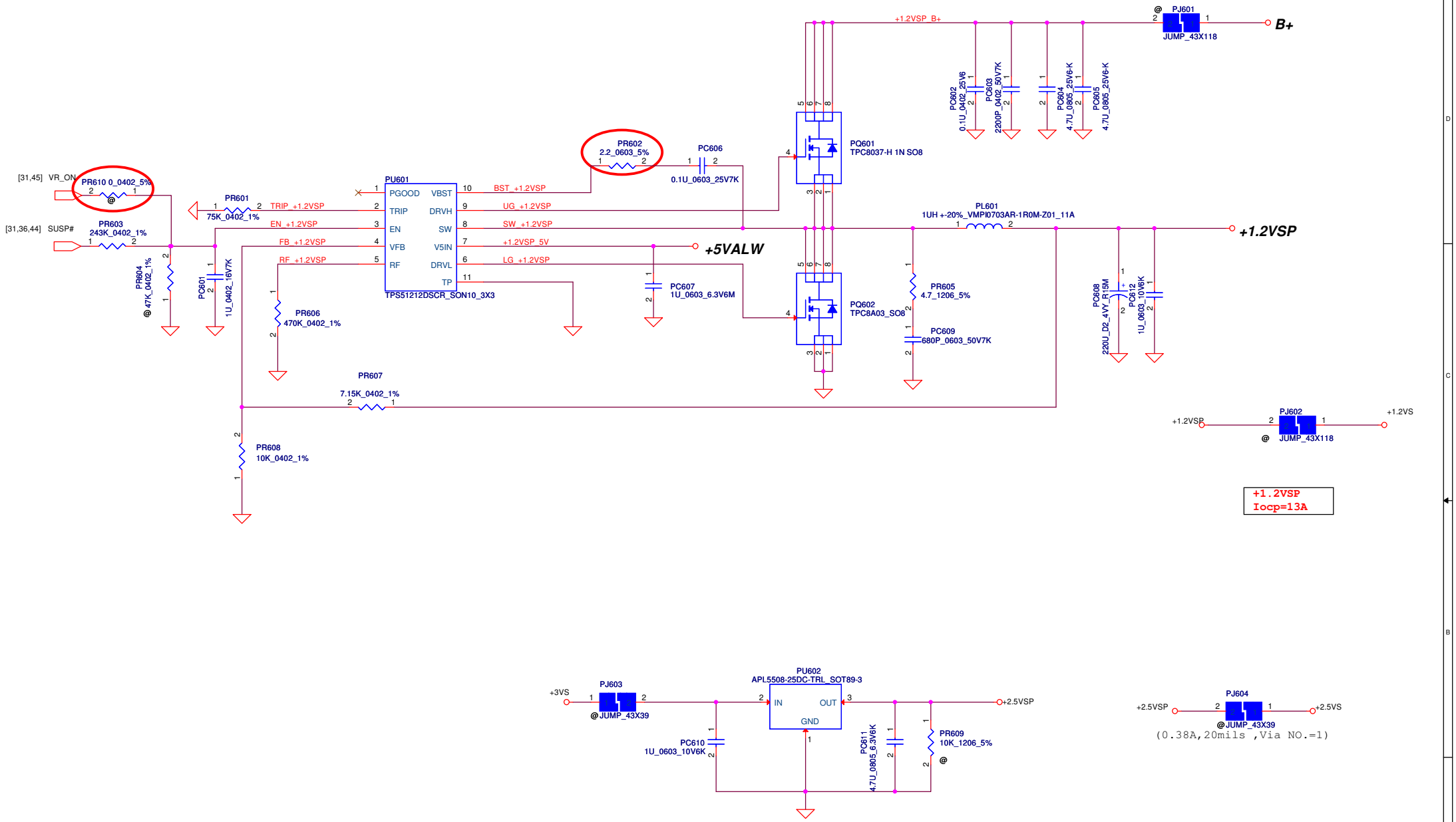

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/04/18	Deciphered Date	Title: +1.2VSP/+2.5VSP
			Size / Document Number / Rev 1.0
			Date: Tuesday, March 12, 2013 Sheet 42 of 51

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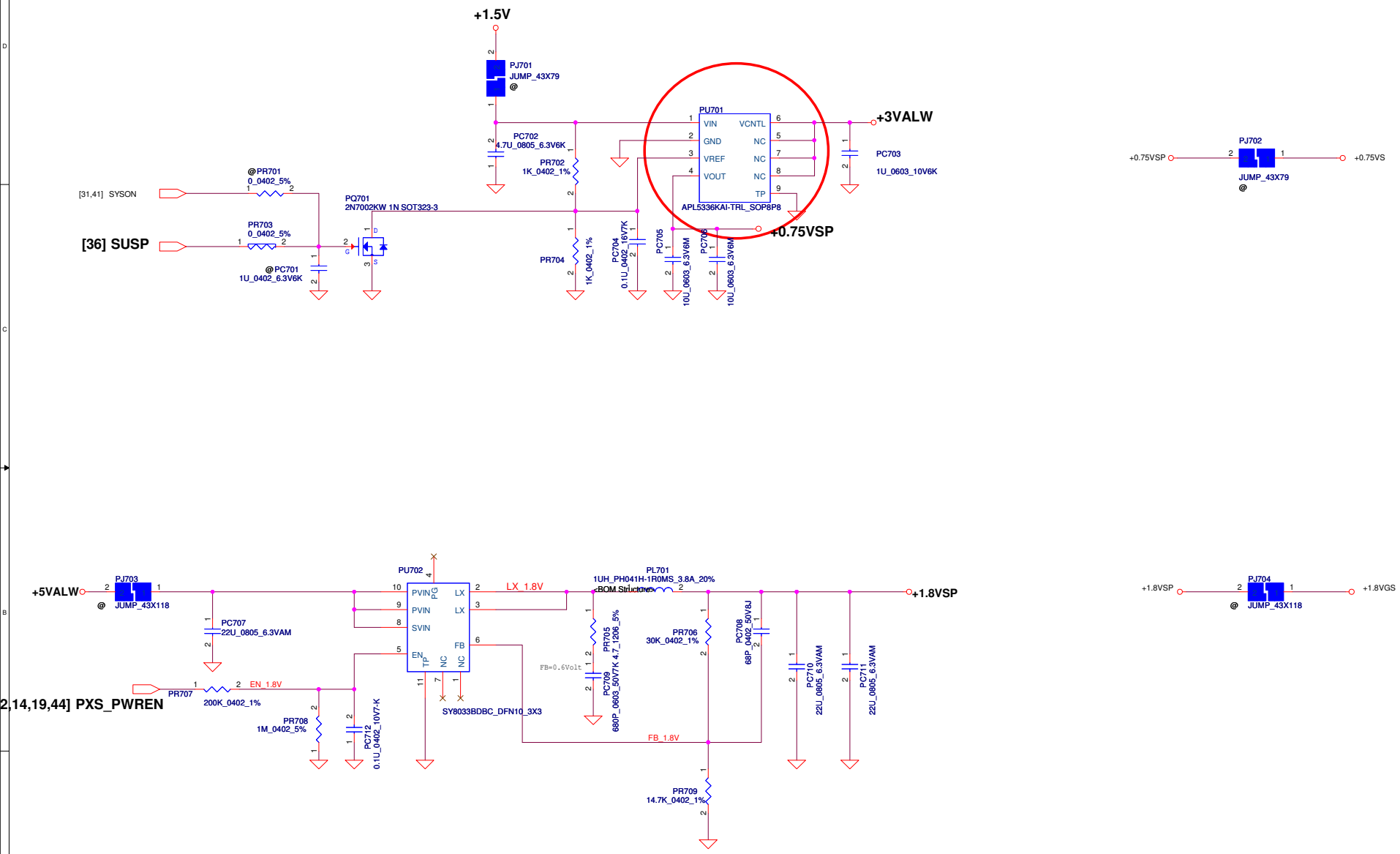

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Issued Date	2011/04/18	Deciphered Date	Title: +0.75VP/+1.8VP
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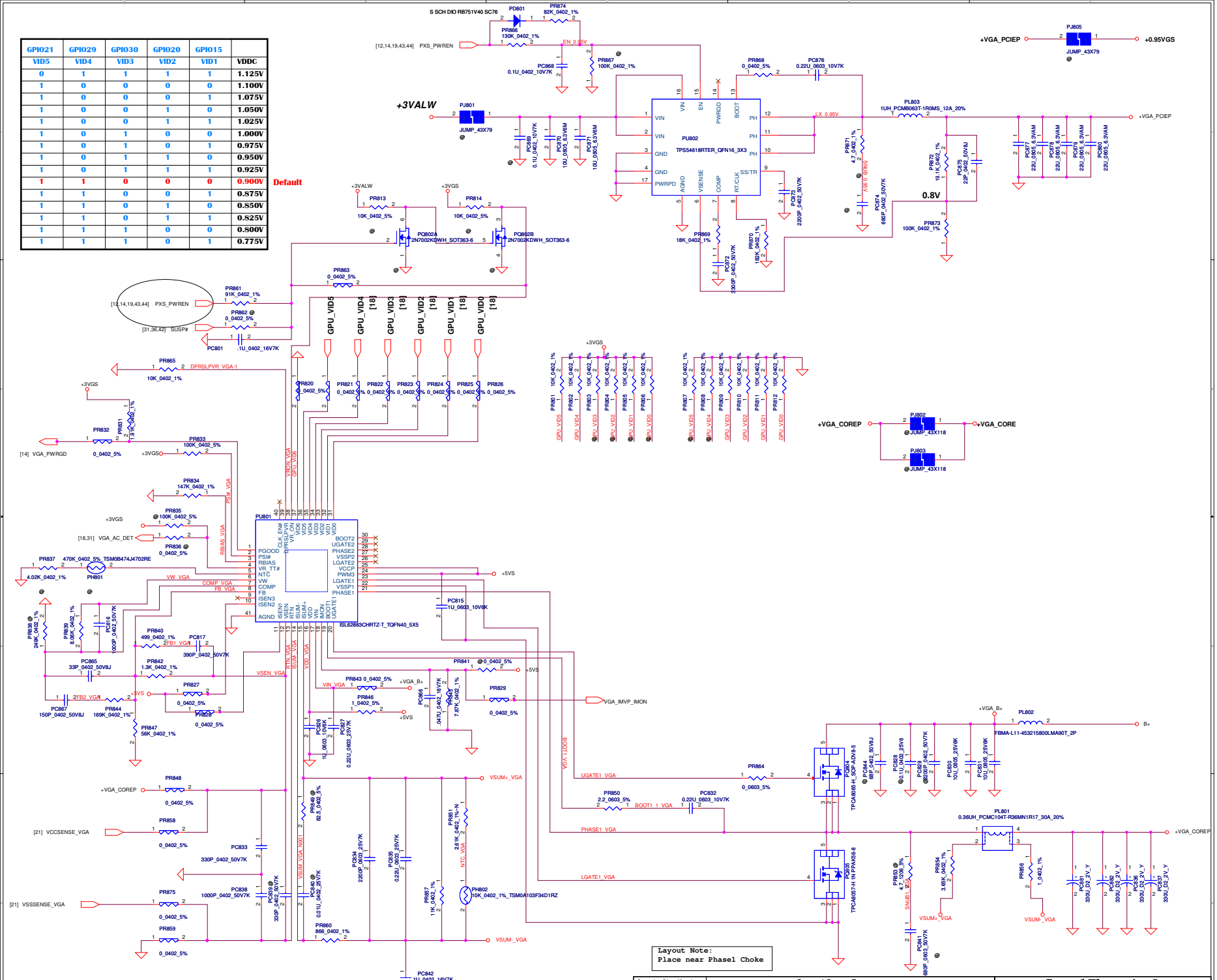
			Date: Tuesday, March 12, 2013 / Sheet 43 of 51

GPIO21	GPIO29	GPIO30	GPIO20	GPIO15	
VID5	VID4	VID3	VID2	VID1	VDDC
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default



Security Classification	Compal Secret Data		
Issued Date	2012/07/03	Deciphered Date	2013/07/03

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Compal Electronics, Inc.

Title: VGA_COREP

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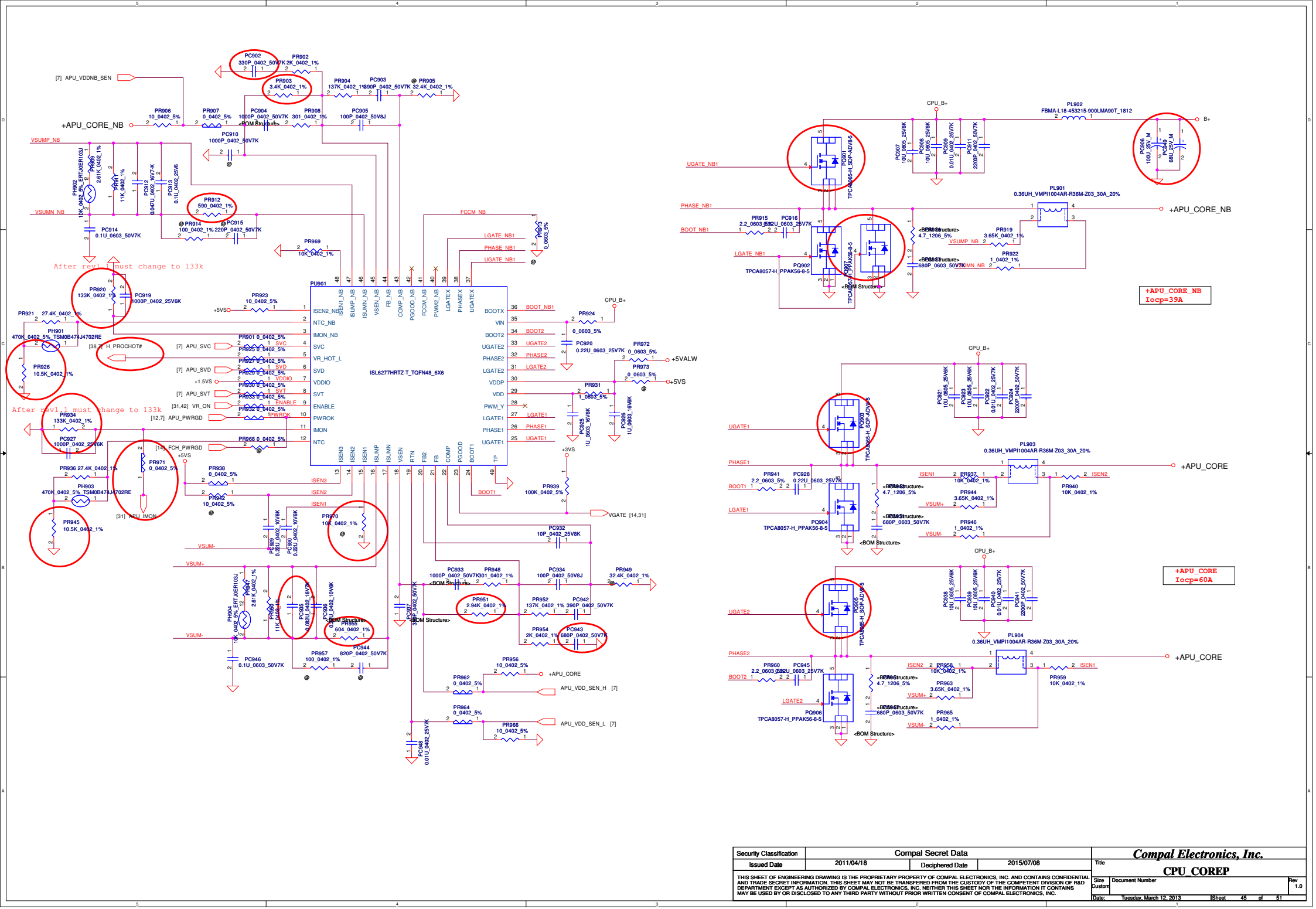

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Issued Date	2011/04/18	Deciphered Date	2015/07/08	Title: CPU_COREP
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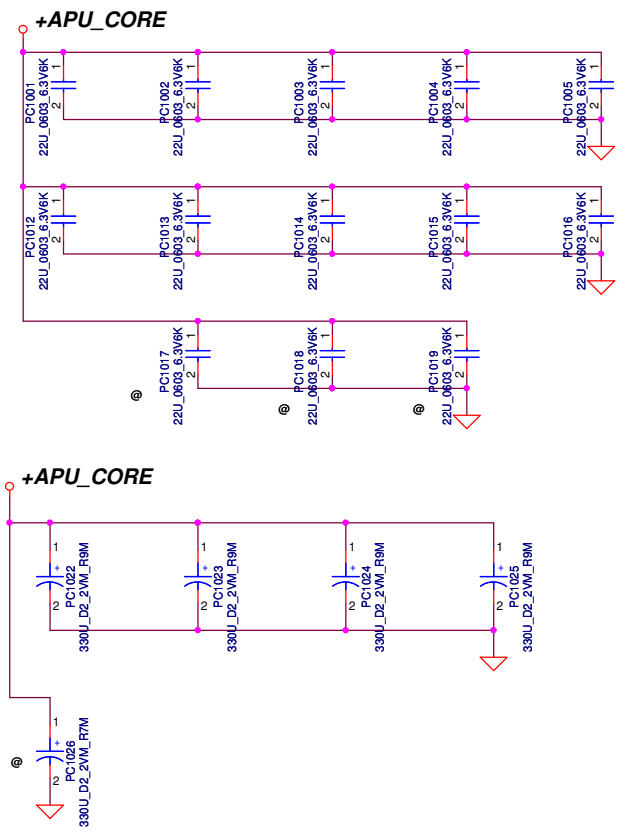
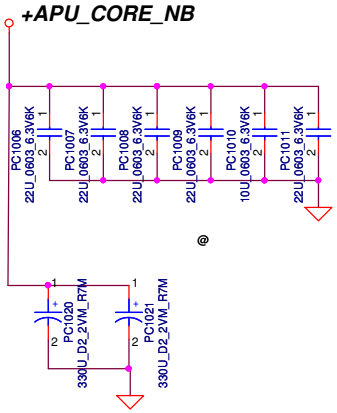
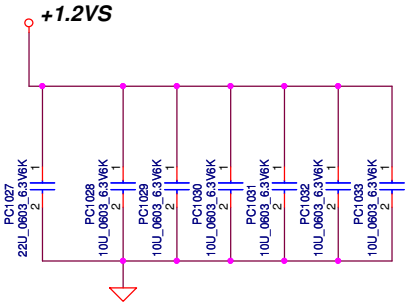
+CPU_CORE



+CPU_CORE_NB



+1.2VS



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Issued Date	2011/04/18	Deciphered Date	Title: PROCESSOR DECOUPLING

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A3		1.0

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Base on EE's request for fine tune power sequence.	P44	Change PR866 from 2.49k to 130k.	2013.1.11	From 0.1 to 0.2
2	For fine tune OCP set up point of VGA core.	P44	Change PR860 from 604ohm to 866ohm.	2013.1.11	From 0.1 to 0.2
3	Base on EE's request for fine tune power sequence.	P44	Change PR861 from 47k to 91k.	2013.1.11	From 0.1 to 0.2
4	Base on must meet EUP spec, change power design.	P37	Remove PR110, PC108, PR114, PC109, PR109, PC107,PU101, PR111, PD101, PR138, PR116, PR112, PD105, PR125, PR128, PC114, PR129, PQ101, PD104, PR123, PR124, PC115, PR131, PC117, PR103, PR104, PR105, PD102, PQ102, PR106, PR107, PQ103, PQ104, PR108, PR118, PR121, PC113, PR127, PQ106, PQ105, PR120, PR115, PC110, PC112, PR126, PR119, PR122, PD103.	2013.1.11	From 0.2 to 0.3
5	Base on must meet EUP spec, change power design.	P39	RemovePQ315, PR328, PR329, PQ316, PD304, PD301, PD302, PQ303, PR303, PR304, PQ306, PQ309.	2013.1.11	From 0.2 to 0.3
6	Base on must meet EUP spec, change power design.	P39	Add PR336, PR338, PR337, PR339, PQ319.	2013.1.11	From 0.2 to 0.3
7	Base on must meet EUP spec, change power design.	P40	Remove PR417, PC420, PQ407, PR420, PC424. Add PR411. Change PR418 from 47K to 2.2K.	2013.1.11	From 0.2 to 0.3
8					
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Phase	Date	No.	BOM	Sch	Layout	Description
SDV/FVT	2012/11/22	No.1	V	V	V	Page 5, Delete for Sun Pro M2 C17,C18,C19,C20,C21,C22,C23,C24,C25,C26,C27,C28,C29,C30,C31,C32 Delete PCIE_CRX_GTX_P8~15 PCIE_CTX_C_GRX_P8~15 PCIE_CTX_GRX_P8~15 PCIE_CRX_GTX_N8~15 PCIE_CTX_C_GRX_N8~15 PCIE_CTX_GRX_N8~15
SDV/FVT	2012/11/22	No.2	V	V	V	Page 17, Delete for Sun Pro M2 C1400,C1417,C1418,C1419,C1420,C1421,C1422,C1423,C1424,C1425,C1426,C1427,C1428,C1429,C1430,C1431 Delet PCIE_CRX_C_GTX_P8~15 PCIE_CRX_C_GTX_N8~15
SDV/FVT	2012/11/22	No.3	V	V	V	Page 17 ,U1401 change Part Number from SA000047H50 to SA00006BA30 for Sun Pro M2
SDV/FVT	2012/11/22	No.4	V	V	V	Page 24, Delete for Sun Pro M2 no Channel B C1621,C1622,C1623,C1624,C1625,C1626,C1627,C1628,C1629,C1630,C1631,C1632,C1633,C1634,C1635,R1462,R1463 C1636,C1637,C1638,C1639,C1640,C1641,C1642,C1643,C1644,C1645,C1646,C1647,C1648,C1649,C1650,R1464,R1465 C1651,C1652,C1653,C1654,C1655,C1656,C1657,C1658,C1659,C1660,C1661,C1662,C1663,C1664,C1665,C1569 C1666,C1667,R1504,R1504,R1505,R1505,R1506,R1507,R1508,R1509,R1510,R1510,R1511,R1511,R1512,C1570 R1513,R1514,R1515,R1516,R1517,R1518,R1519,R1520,R1521,R1522,R1523,R1524,R1525,R1526,R1527,U1409,U1410,U1411,U1412
SDV/FVT	2012/11/22	No.5		V	V	Page 19, Reserved T1406,T1407 for Sun Pro M2
SDV/FVT	2012/11/22	No.6	V	V	V	Page 18, Reserved D1401 for Sun Pro M2 PX5.5
SDV/FVT	2012/11/22	No.7	V	V	V	Page 19, Delete PX4.0 and PX5.0 schematic C1459,C1460,C1461,C1462,C1463,D1400,Q1401,Q1402,Q1403A,Q1403B,Q1404,Q1405,Q1406,R1401,R1438,R1439,,R1440, R1442,R1460,R1461,U1402,U1403
SDV/FVT	2012/11/22	No.8	V	V	V	Page 20, Delete DGPU Display Power not need reserved C1472,C1473,C1474,C1475,C1477,C1478,C1479,C1480,C1481,C1482,C1483,C1484,C1487,C1488
SDV/FVT	2012/11/22	No.9	V	V	V	Page 20, L1405 change Part Number from SM010009U00 to SM01000AX00 for Sun Pro M2 Spec Suggetion 120 to 220 ohm
SDV/FVT	2012/11/22	No.10	V	V	V	Page 20, Delete R1457,R1458 ,Because the Sun Pro M2 AW28,AW18 are NC.
SDV/FVT	2012/11/22	No.11	V	V	V	Page 20, Delete Thames&Seymour reserved R1407,R1408,R1409,R1410,R1411,R1412,R1413,R1414,R1415,R1416,R1417,R1466,R1467,R1468,R1469,R1471
SDV/FVT	2013/1/10	No.12	V	V	V	Page 12 U2 change Part Number from SA000066K10 to SA000066K60
SDV/FVT	2013/1/10	No.13		V	V	Page 31, for Power Eulot 6 modfiy Delete net FSTCHG,BATT_LEN#
SDV/FVT	2013/1/11	No.14	V	V	V	Page 18, for fine tune VGA Power saving Stuff C1441
SDV/FVT	2013/1/11	No.15	V	V	V	Page 19, for fine tune VGA Power Sequence R1445 change value from 20K to 470K R1446 change value from 20K to 10K

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Phase	Date	No.	BOM	Sch	Layout	Description
SIT	2013/1/10	No.1	V	V	V	Page 35, for Power Eulot 6 modfiy Un-Stuff @ Q2408,R2463
SIT	2013/1/10	No.2	V	V	V	Page 33, for Touch Pad Module requirment Stuff R2470
SIT	2013/2/1	No.3	V	V	V	Page 07, for APU_SID and APU_SIC voltage smothly Stuff C69
SIT	2013/2/1	No.4	V	V	V	Page 26, for Logo LED brightness change Resistor Valve from 4.99K to 1.6K
SIT	2013/2/20	No.5		V	V	Page 36, for delete Discharge circuit ,remove R2324,Q2314,R2321,Q2309
SIT	2013/3/05	No.6		V	V	Page 32, for Factory issue ,remove JBT1
SIT	2013/3/12	No.7	V	V	V	Page 25, for cost down ,not need reserved for EC ,non-stuff Q2107,R2177,R2178
SIT	2013/3/12	No.8	V	V	V	Page 36, for customer request , Stuff R2302,R2303,Q2300,Q2302

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Issued Date	2012/11/22	Deciphered Date	2015/11/22

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