



SE000008600

Compal Confidential

Everest Schematics Document

Intel Merom Processor with Crestline + DDRII + ICH8M

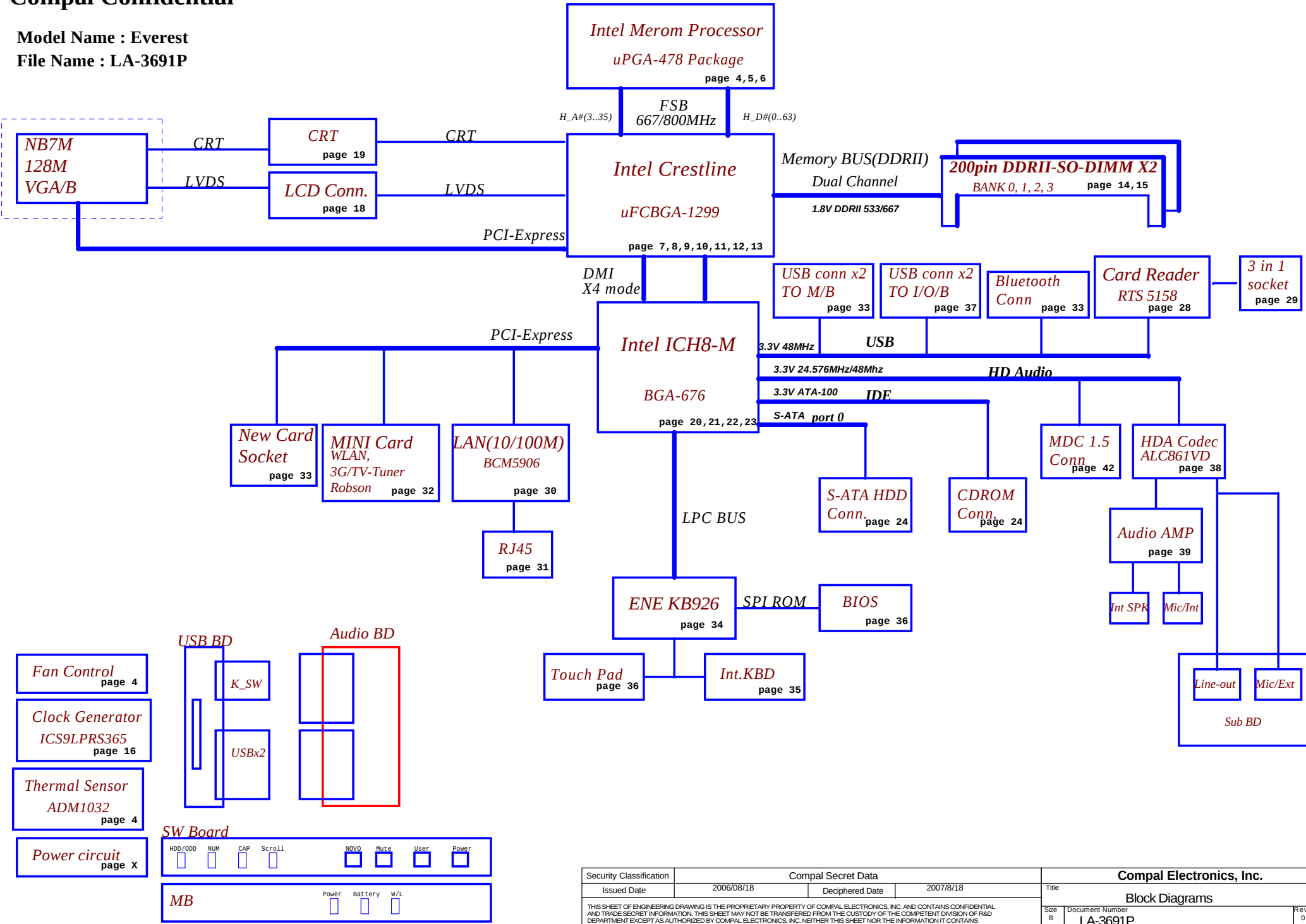
2007 - 03 - 05

REV: 0.2

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Model Name : Everest
File Name : LA-3691P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE	SIGNAL							
	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

ID1	ID0	TEST
0(R744)	0(R745)	A-TEST
0(R744)	1(R742)	B-TEST
1(R741)	0(R745)	C-TEST

PANEL ID Table

R	Size
Ra (R743)	15W
Rb (R740)	14W

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

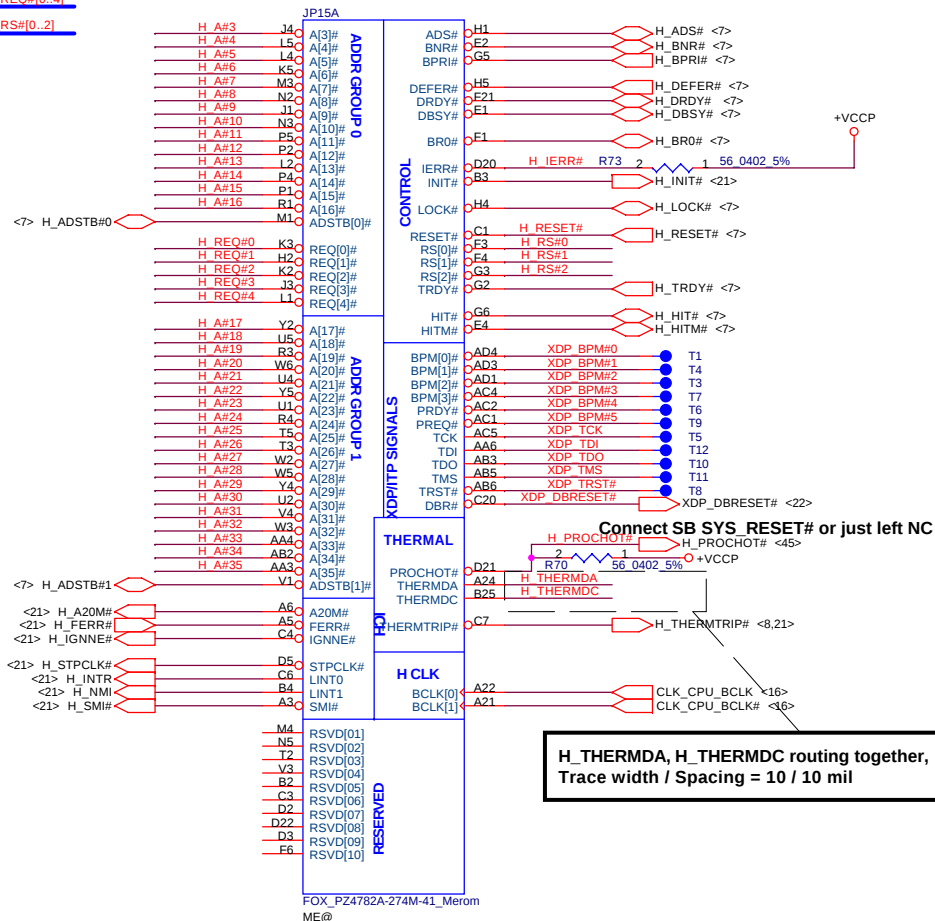
EC SM Bus2 address

Device	Address
GMT-781	1001 100X b
NVIDIA NB8X	

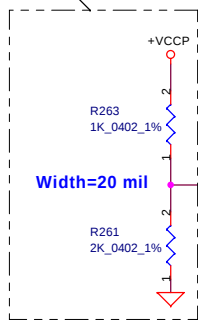
ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

<7> H_A# [3..35] H_A# [3..35]
<7> H_REQ# [0..4] H_REQ# [0..4]
<7> H_RS# [0..2] H_RS# [0..2]



Close to CPU pin AD26 within 500mils.



Width=20 mil

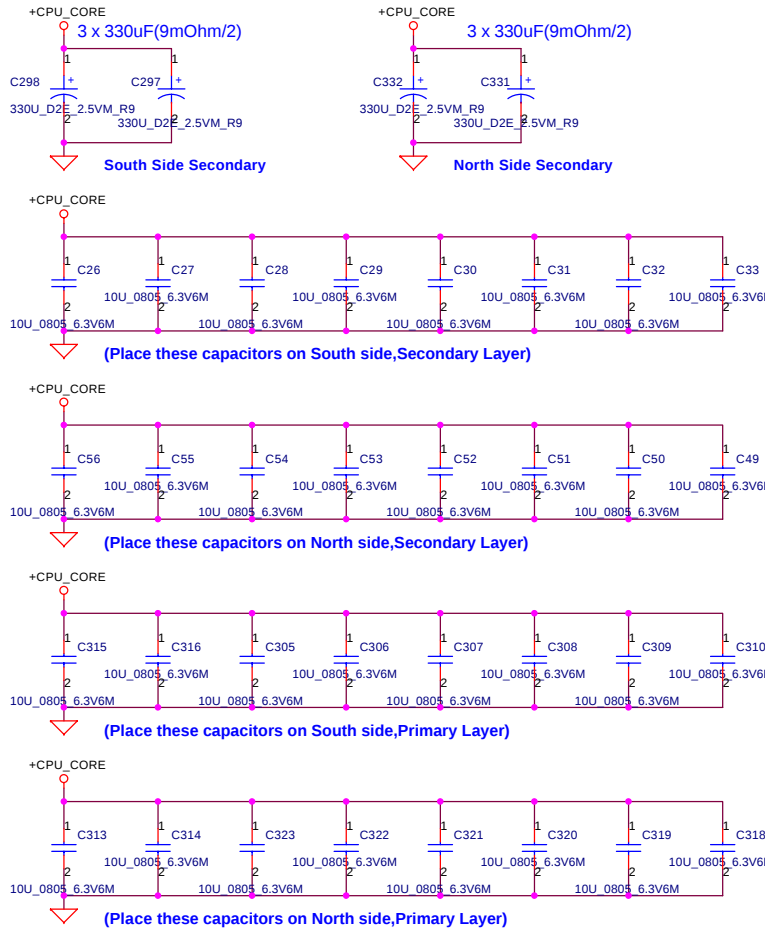
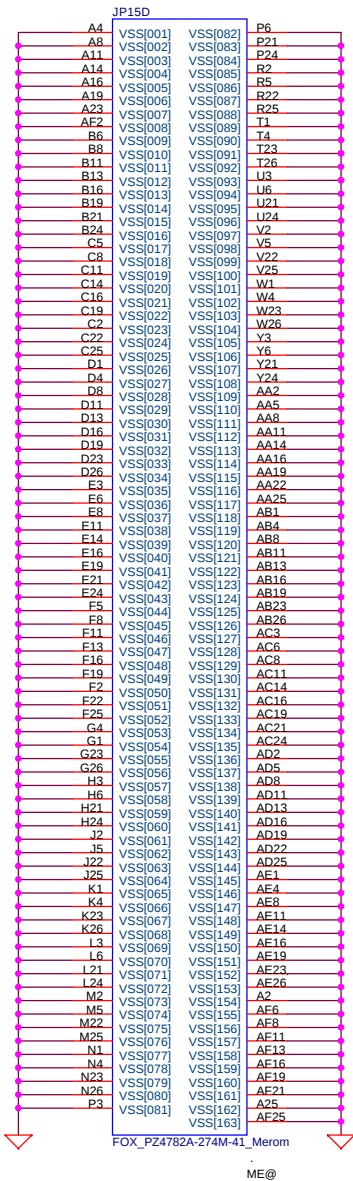
Layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

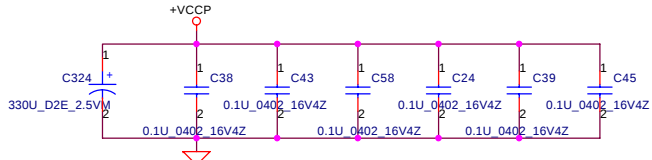
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.

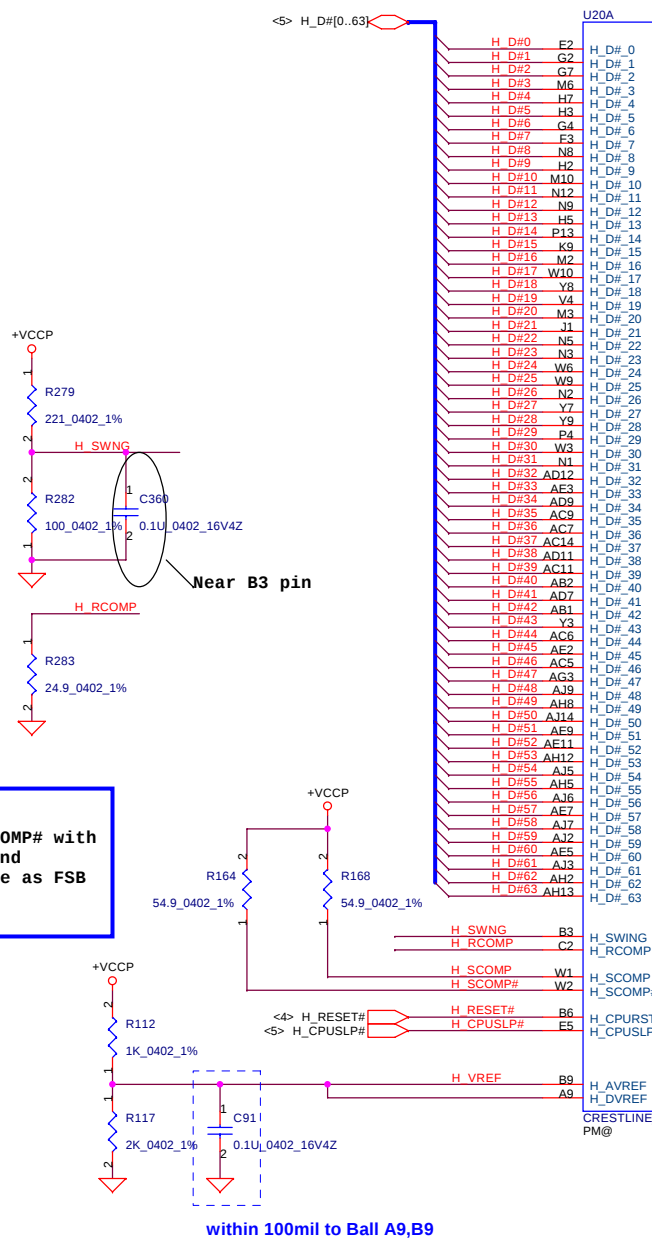
Close to CPU pin within 500mils.



+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



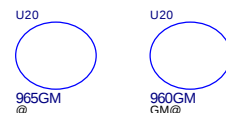
9/25 10U checked. OK for use!



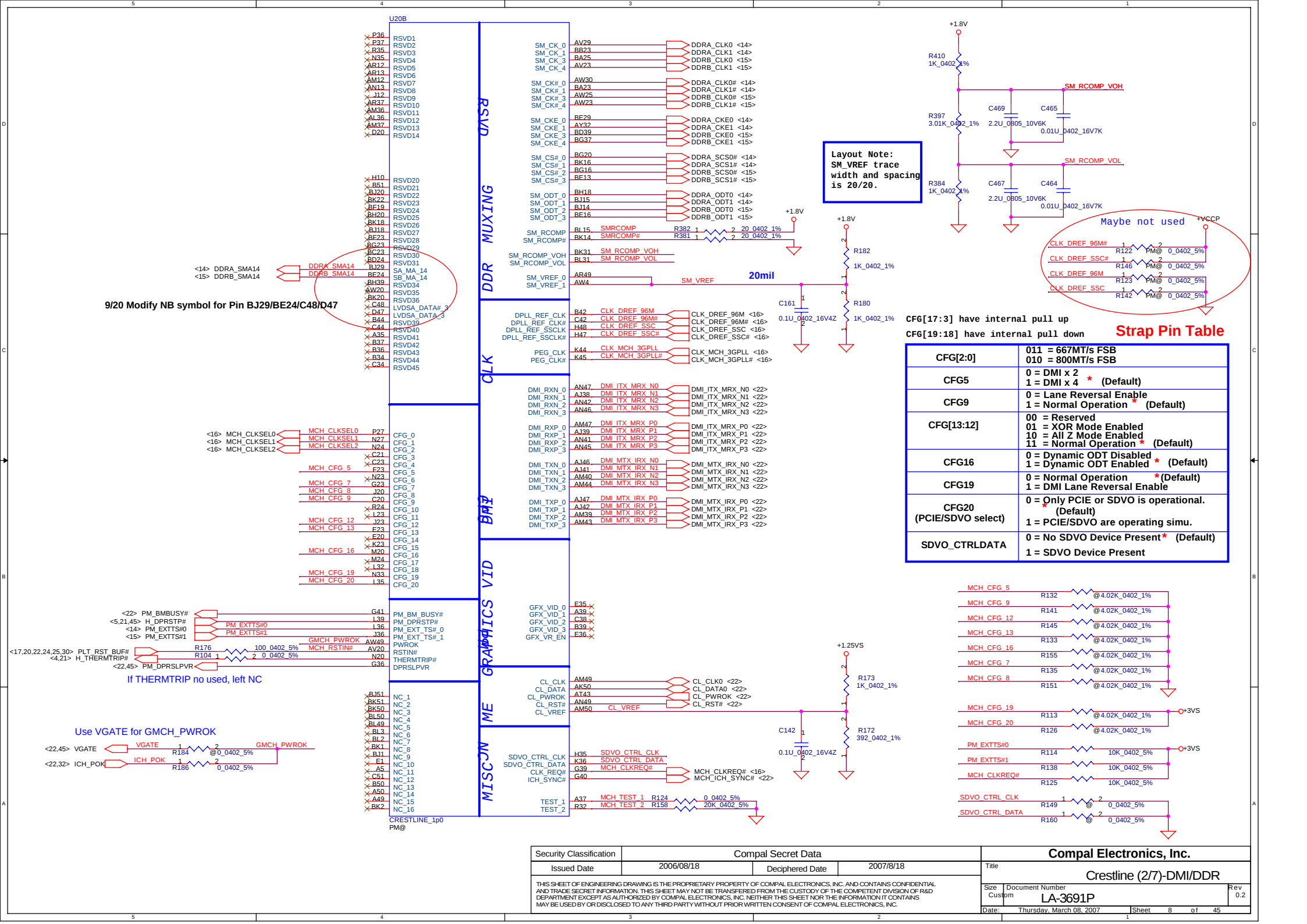
layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCOMP / H_VREF / H_SWNG trace width and spacing is 10/20

HOST

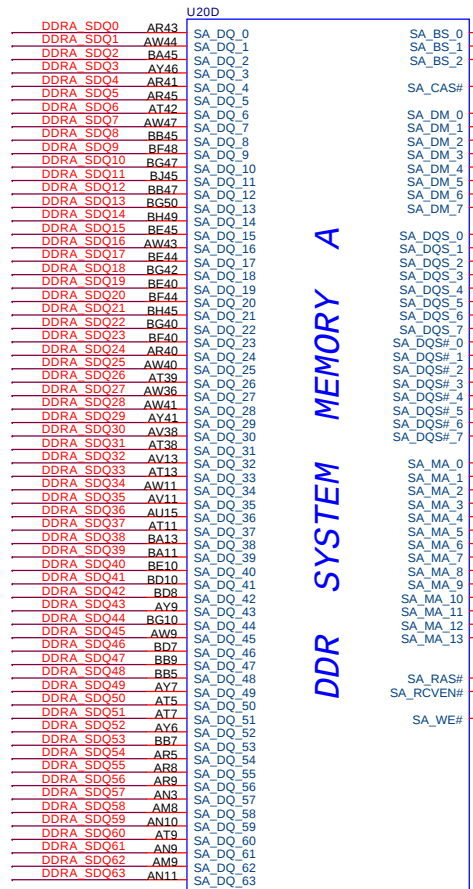


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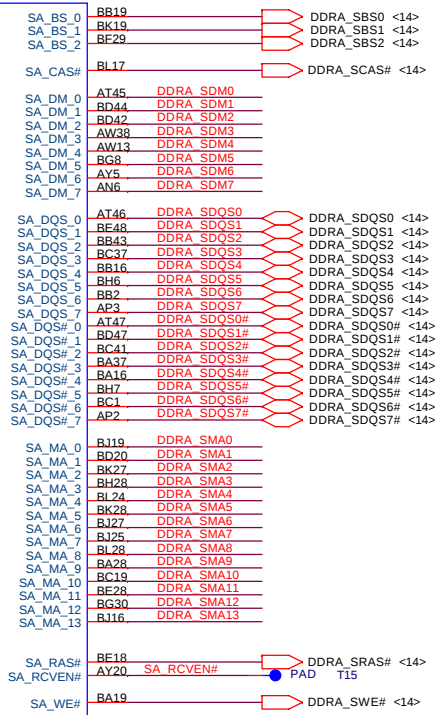


<14> DDRA_SDQ[0..63] <14> DDRA_SDM[0..7] <14> DDRA_SMA[0..13]

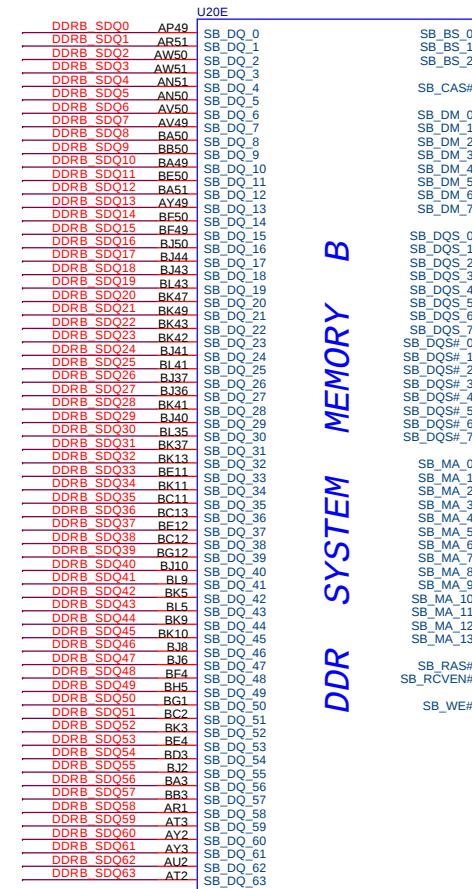
<15> DDRB_SDQ[0..63] <15> DDRB_SDM[0..7] <15> DDRB_SMA[0..13]



DDR SYSTEM MEMORY A



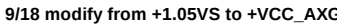
CRESTLINE_1p0
PM@



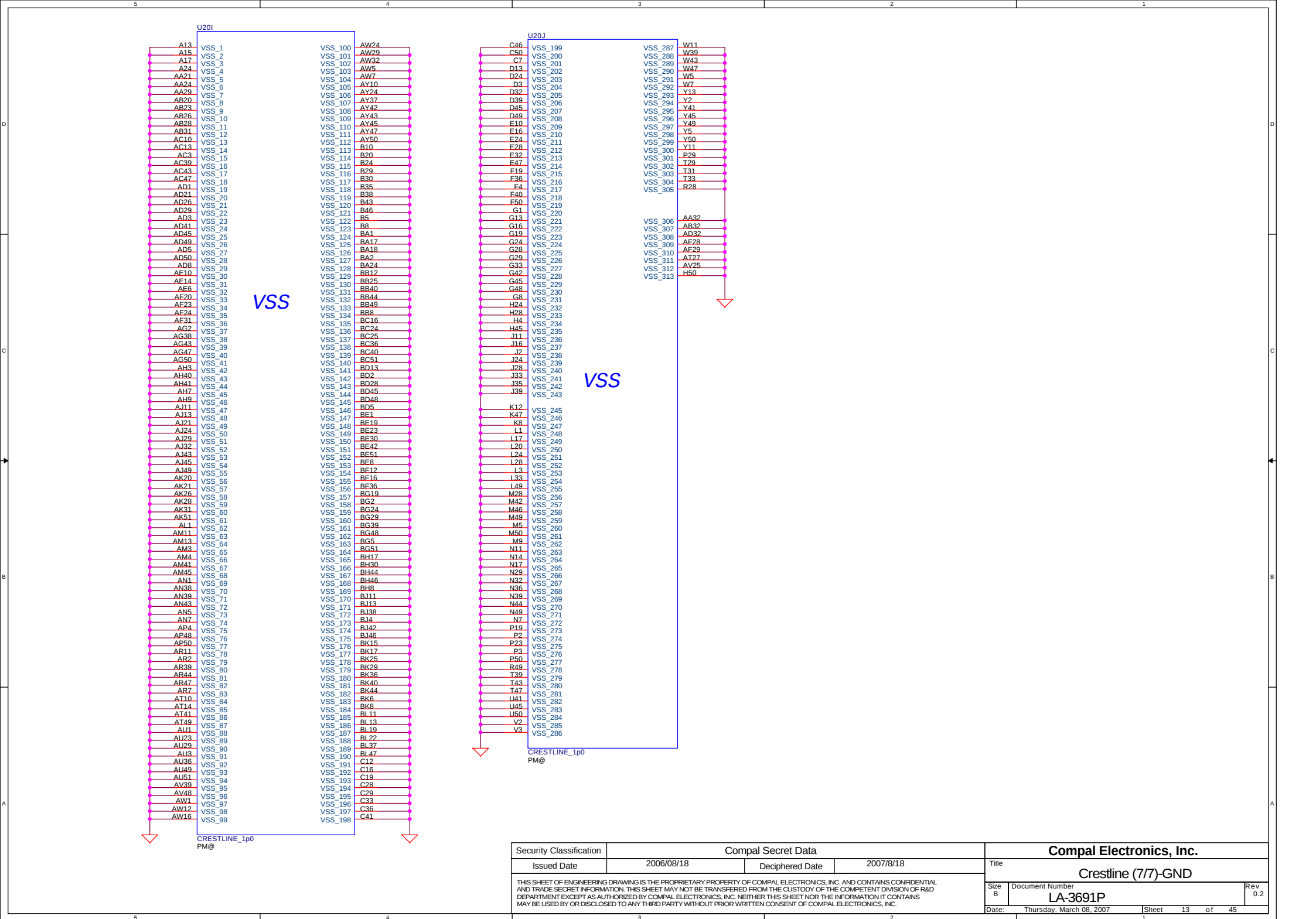
DDR SYSTEM MEMORY B

CRESTLINE_1p0
PM@

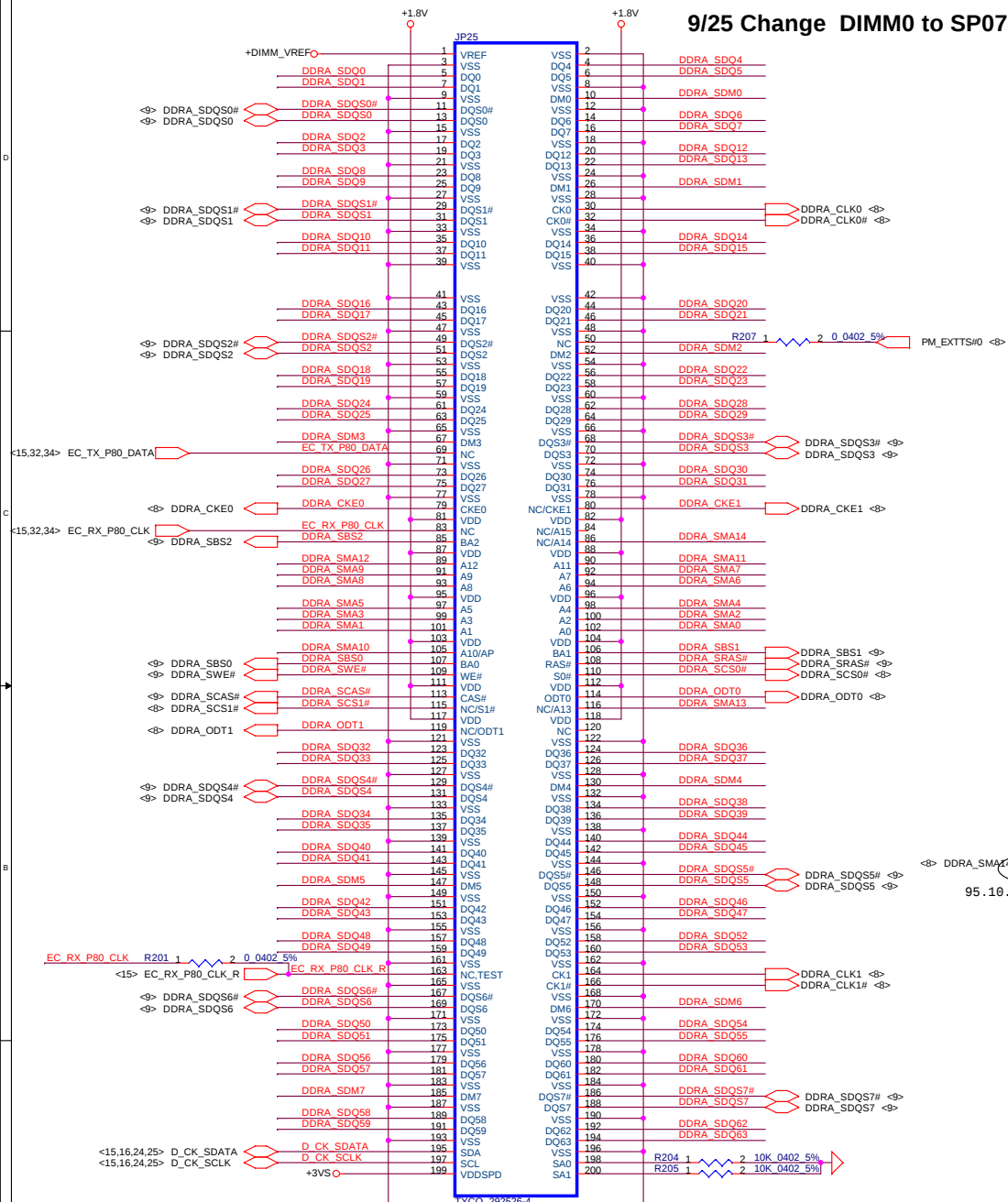
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3				2		1					



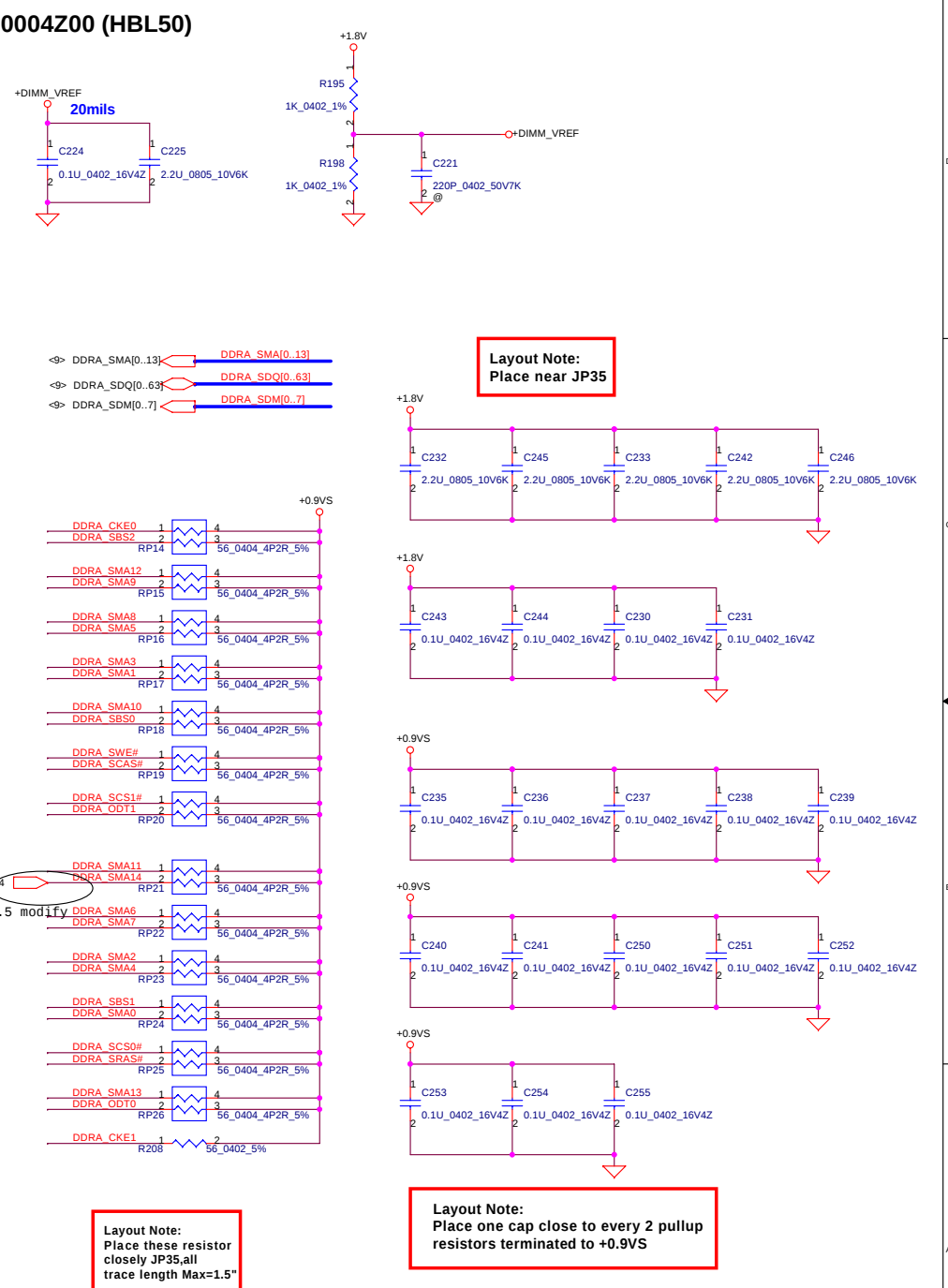




9/25 Change DIMM0 to SP070004Z00 (HBL50)

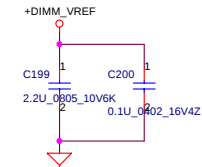
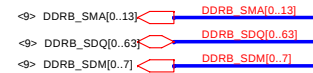
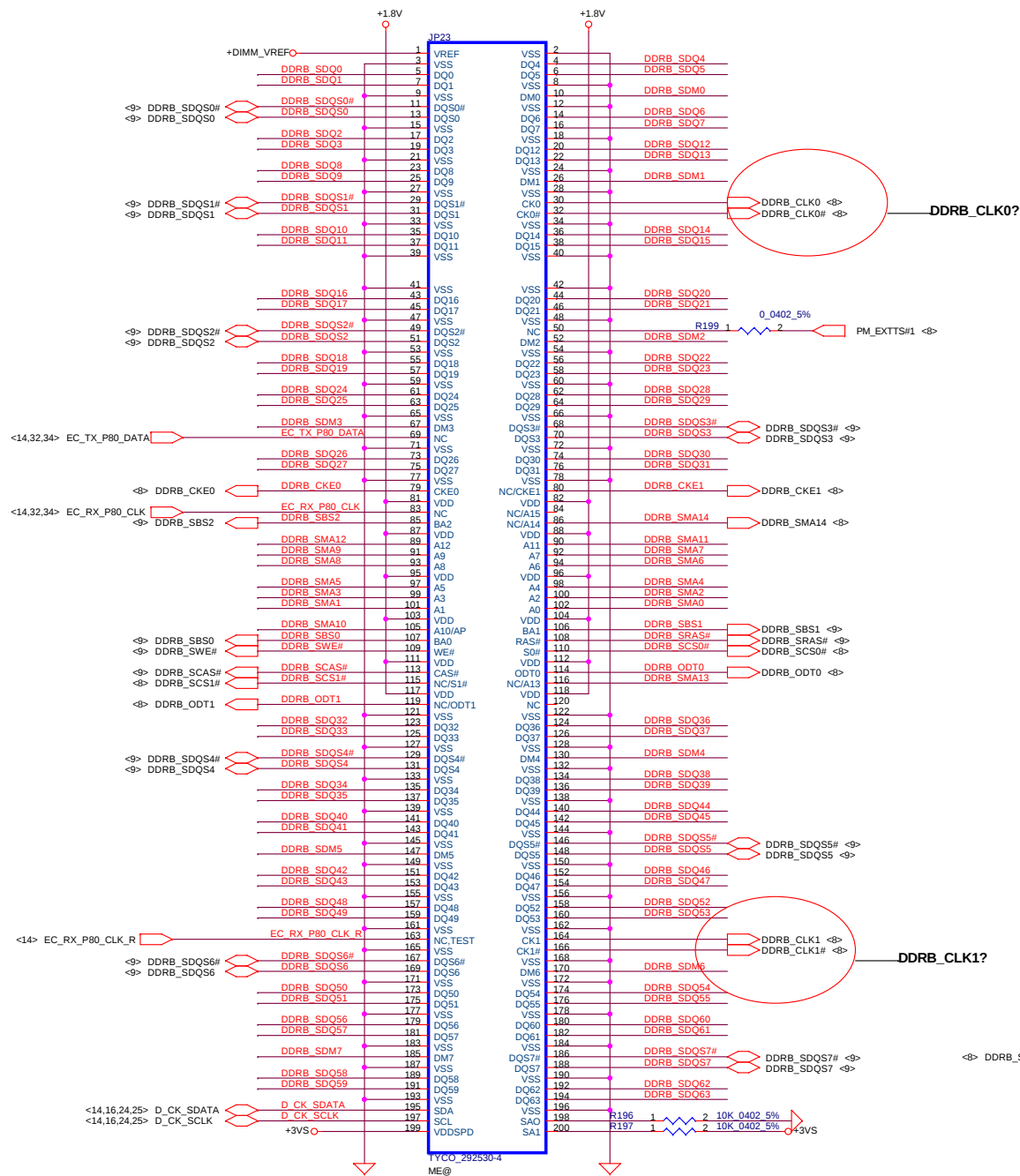


DIMM0 STD H:5.2mm (BOT)

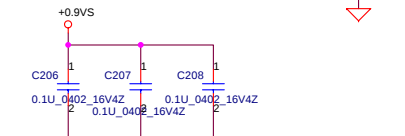
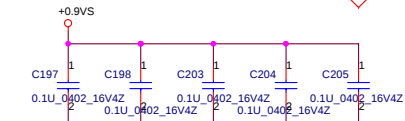
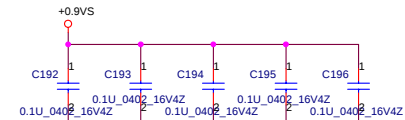
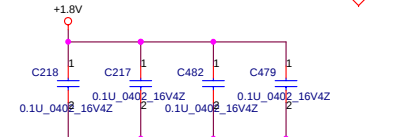
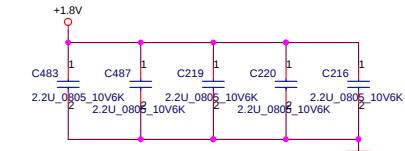


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9/25 Change DIMM1 to SP070006F00



Layout Note:
Place near JP34



Layout Note:
Place these resistor
closely JP35,all
trace length Max=1.5'

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

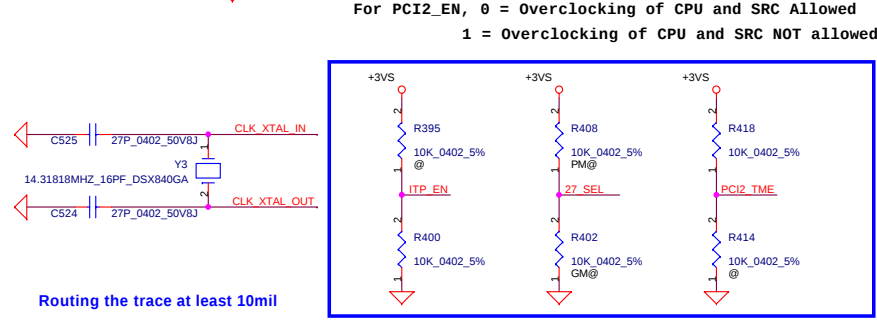
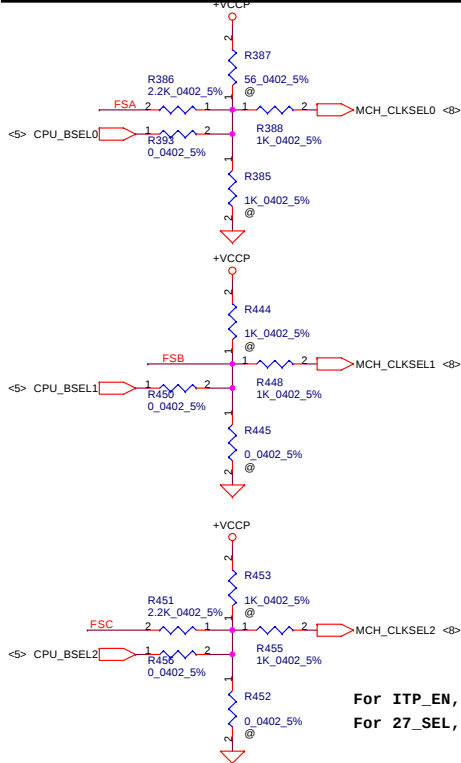
DIMM1 STD H:9.2mm (BOT)

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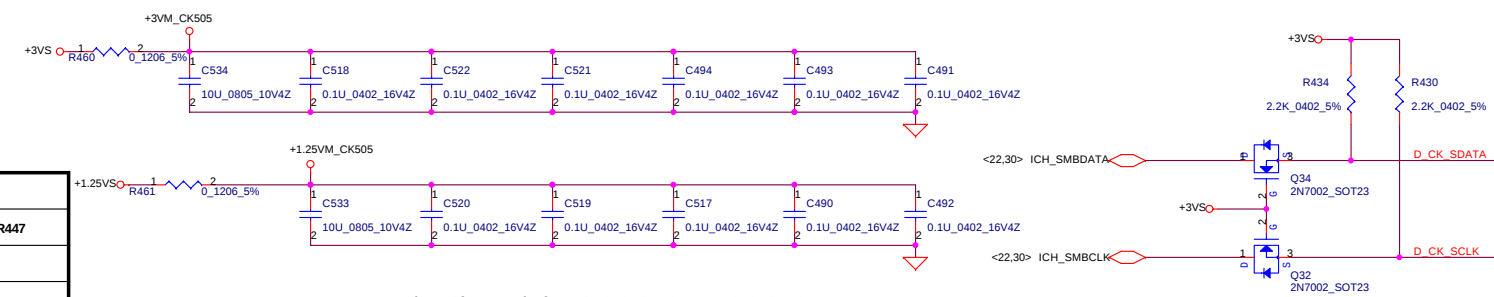
FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHZ	MHZ	MHZ
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff						
*(Default)	No Stuff	R401	R408	R417	R430	R438	R447
667MHz	Stuff	R401	R417	R447			
	No Stuff	R408	R430	R438			
800MHz	Stuff	R408	R417	R447			
	No Stuff	R401	R430	R438			

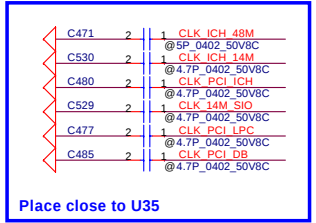
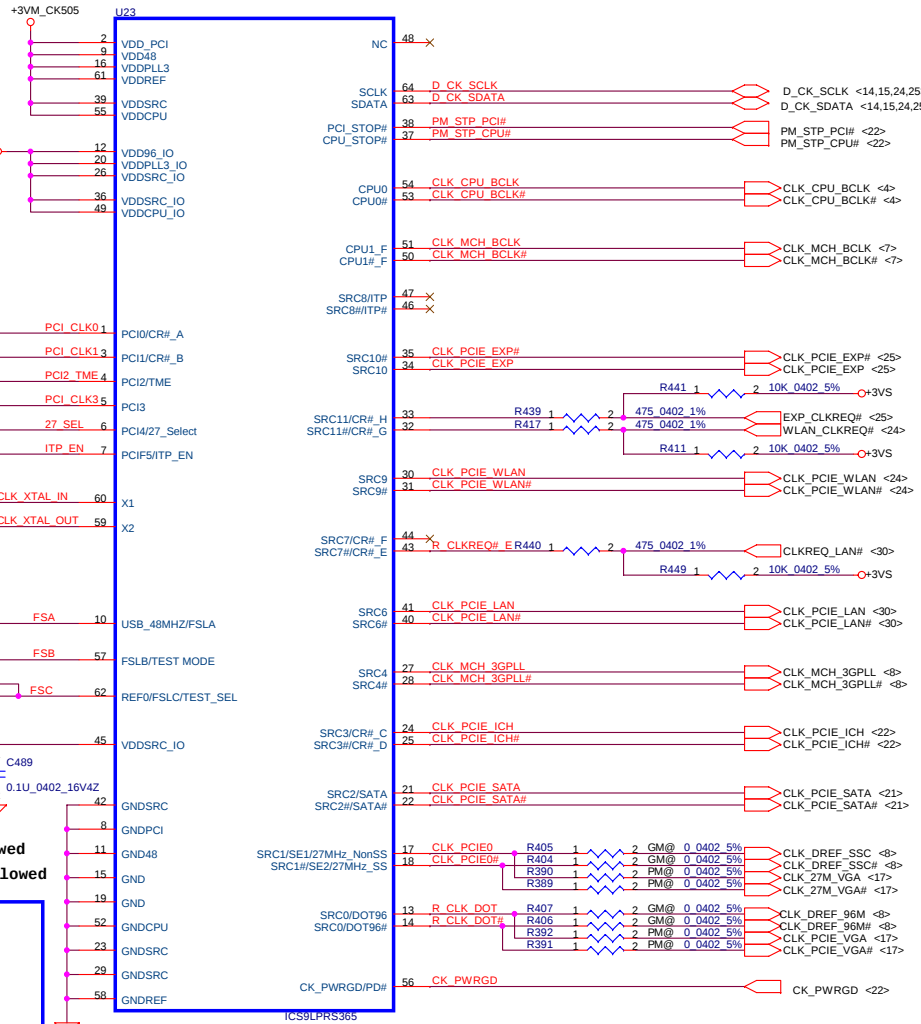


Routing the trace at least 10mil



10/17 : Change P/N from SA0001GT00 to SA00001GT10

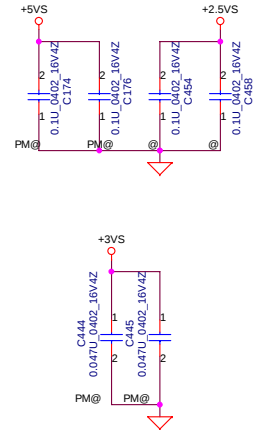
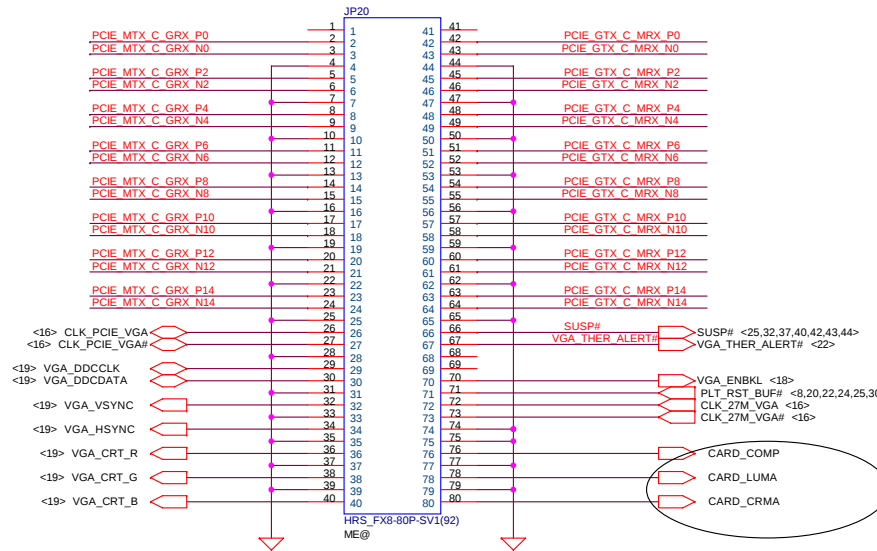
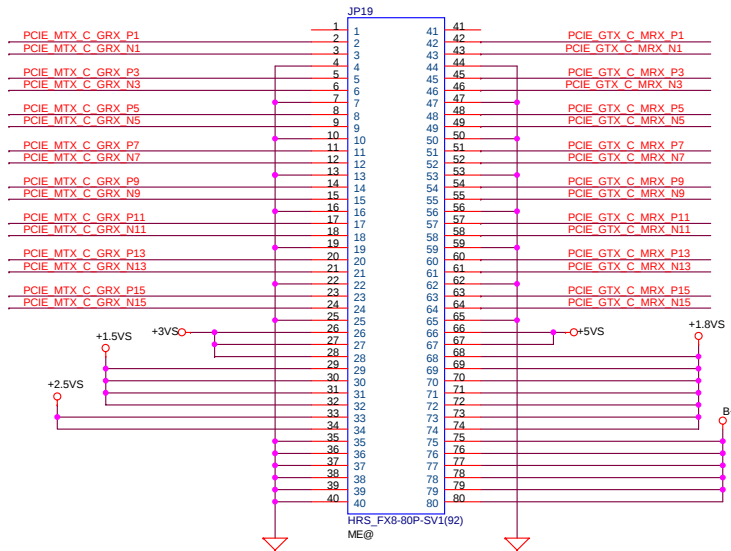
Need to update Symbol



Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	Clock generator	
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MAX. 4.06A @ 1.8V
MAX. 130mA @ 2.5V
MAX. 655mA @ 3.3V

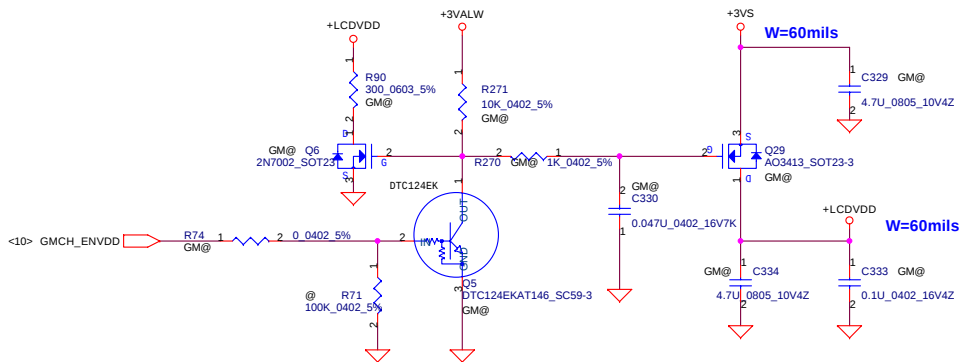
<10> PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N0..15
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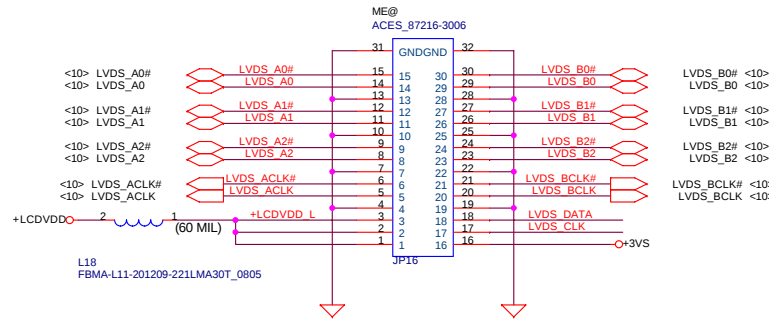
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Title			
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VGA/B connector			
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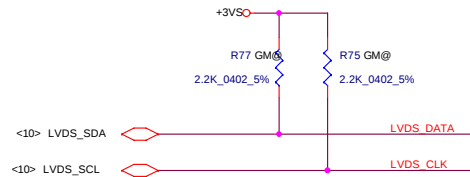
LCD POWER CIRCUIT



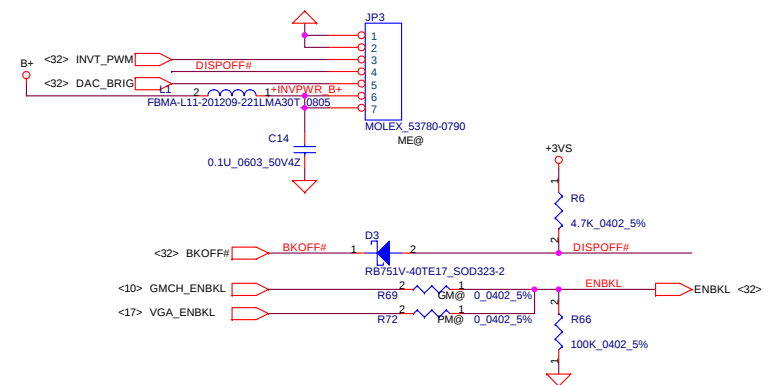
LCD/PANEL BD. Conn.



Follow HEL80's pin definition
Except pin 29



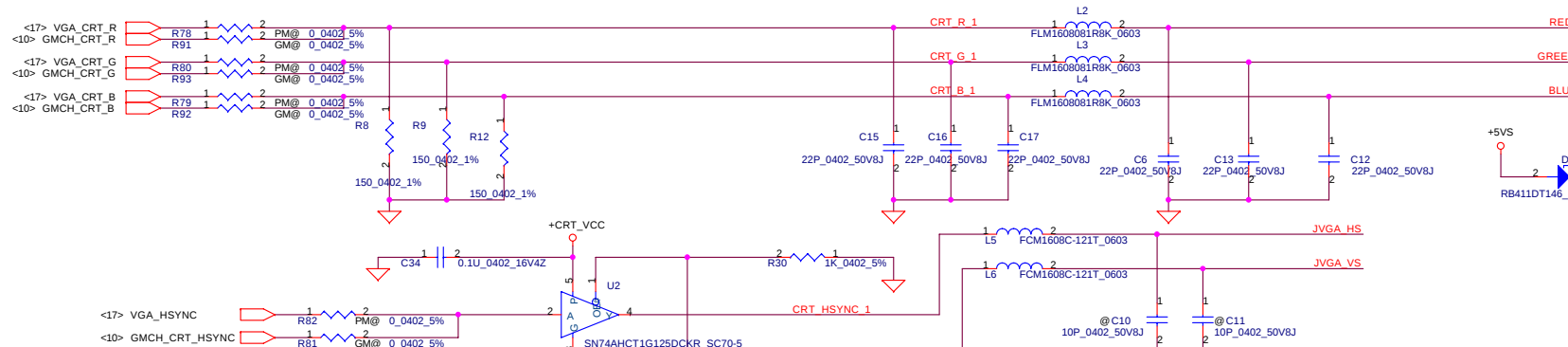
INVERTER Conn.



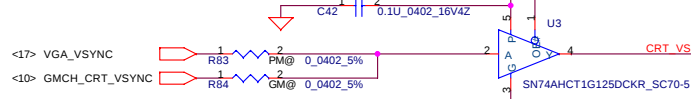
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CRT Connector

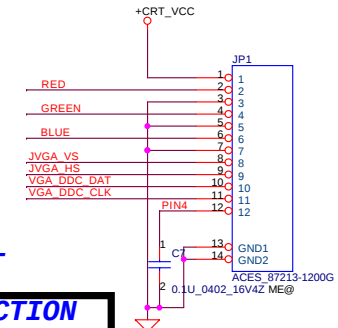
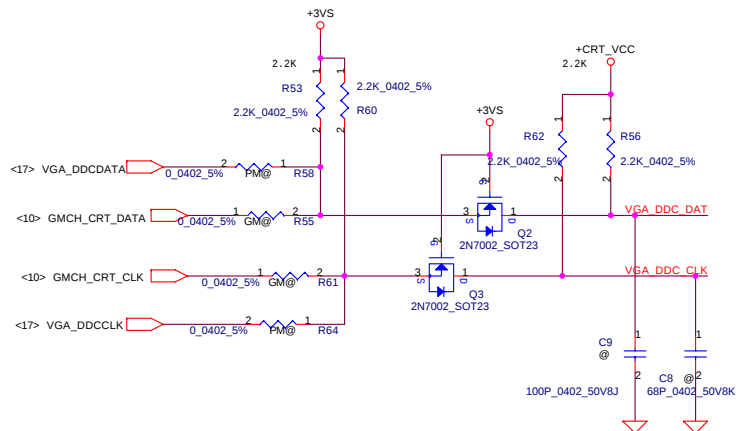
Place closed to chipset



Place closed to chipset

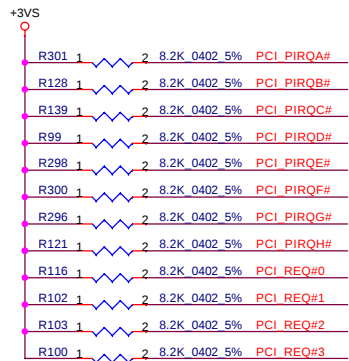
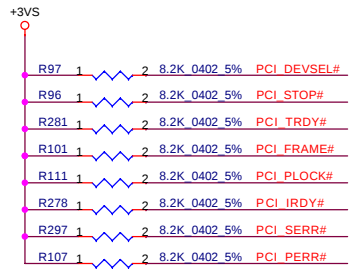


Update Footprint

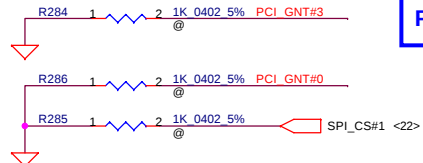
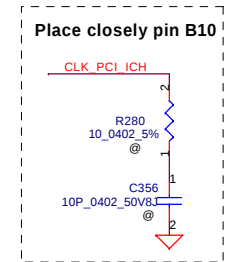
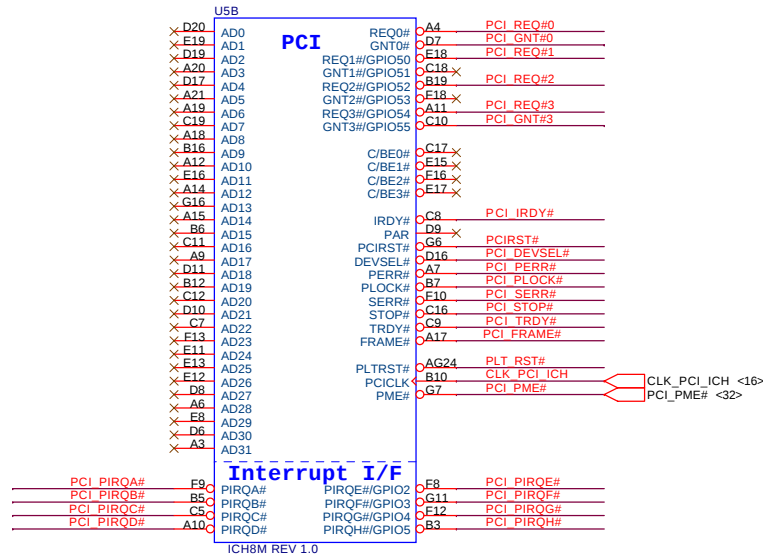


PIN ASSIGMENT

PIN	D-SUB	FUNCTION
1	9	+CRT_VCC
2	1	RED
3	6	GND
4	2	GREEN
5	7	GND
6	3	BLUE
7	8	GND
8	14	VSYNC
	10	GND
9	13	HSYNC
	11	SENSE
10	12	SM_DAT
11	15	SM_CLK
12	4	PIN4

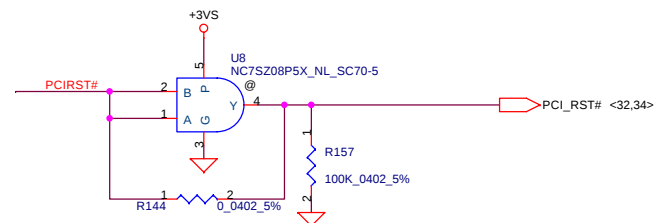
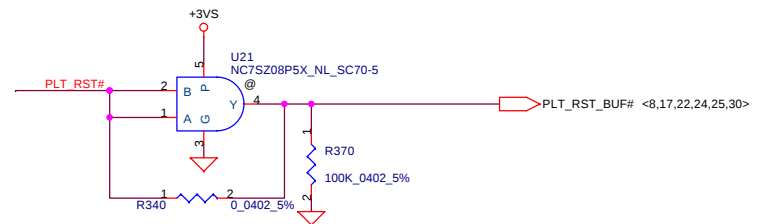


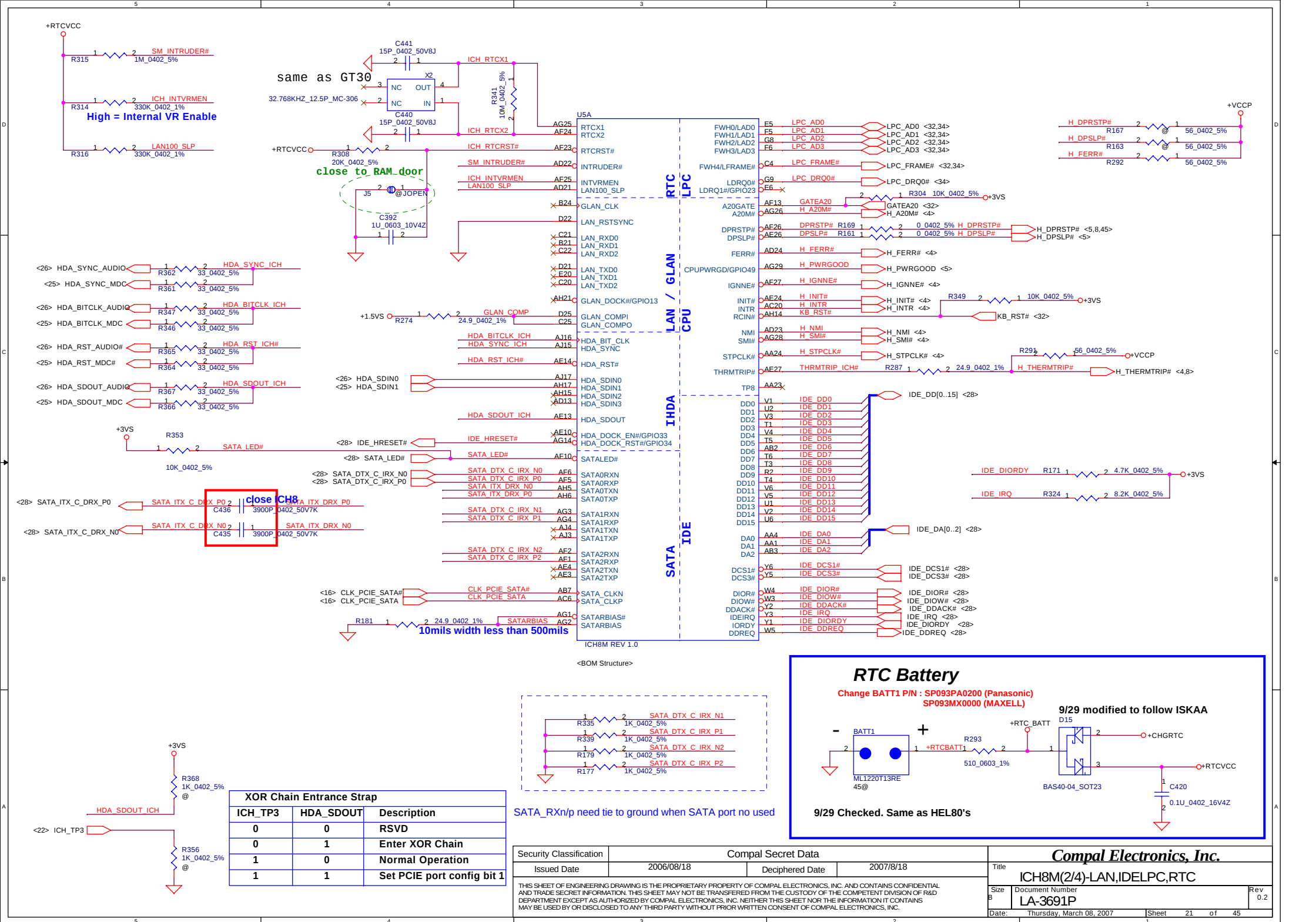
10/17 : Change P/N from SA000010G00 to SA00001JU10
 10/17 : FootPrint : SA000010G00
 BOM : SA00001JU10

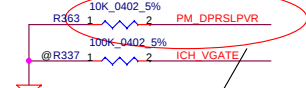
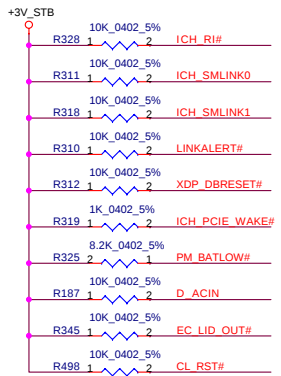
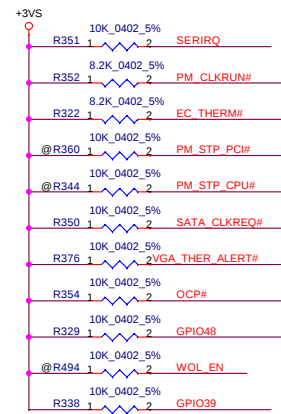


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

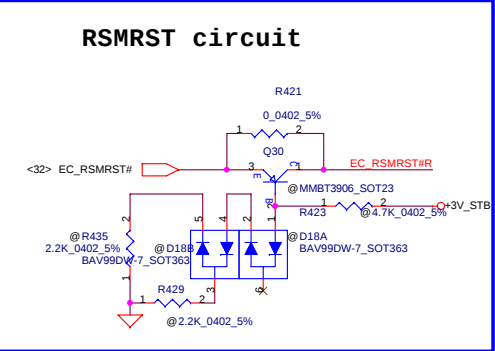
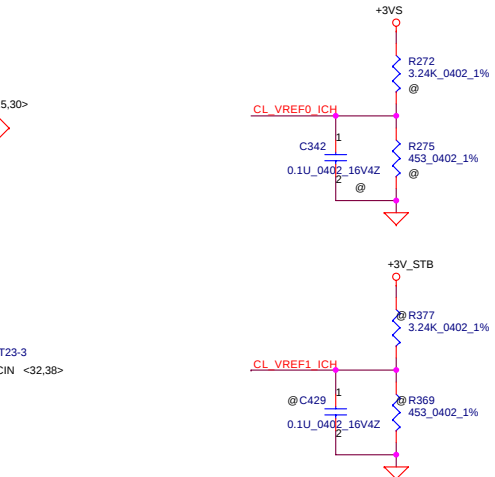
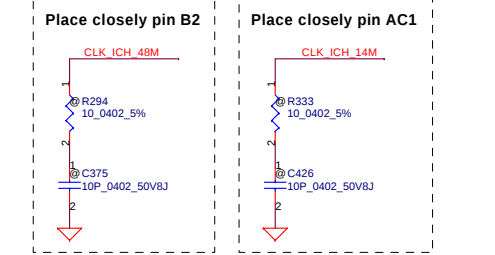
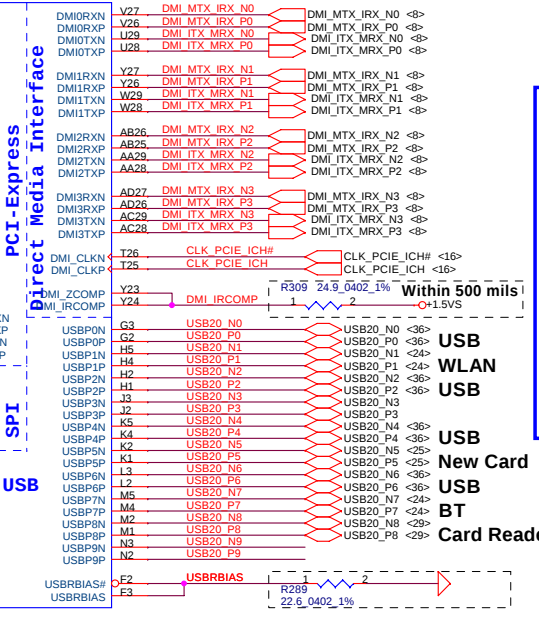
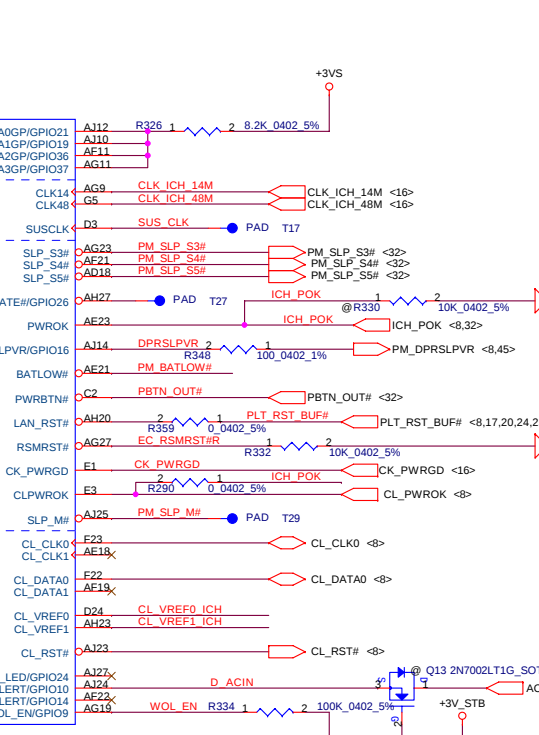
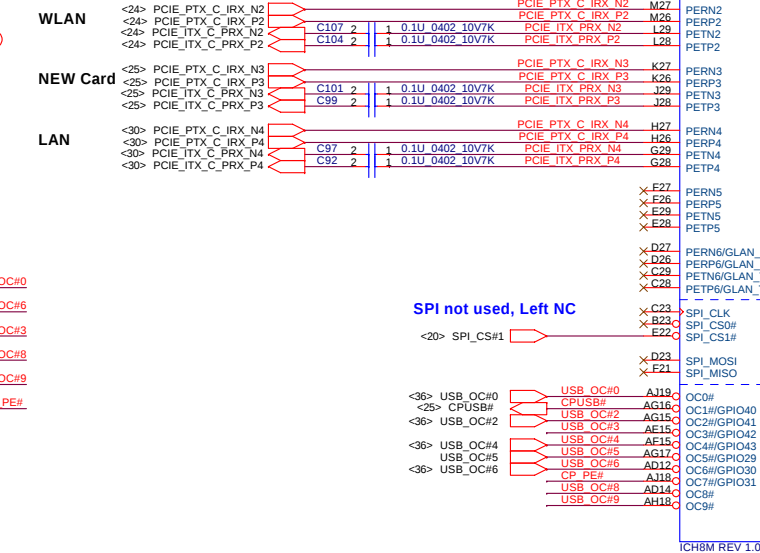
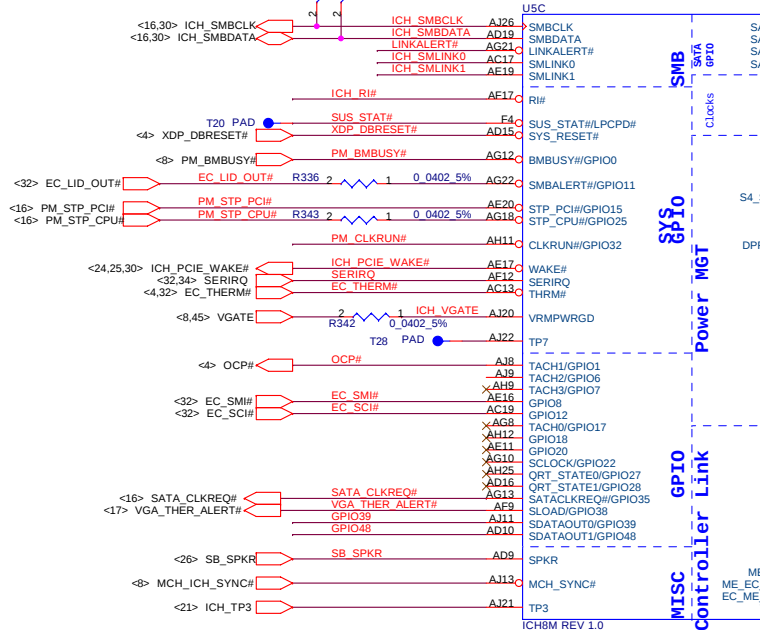
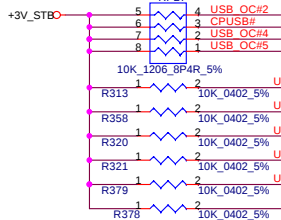
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*





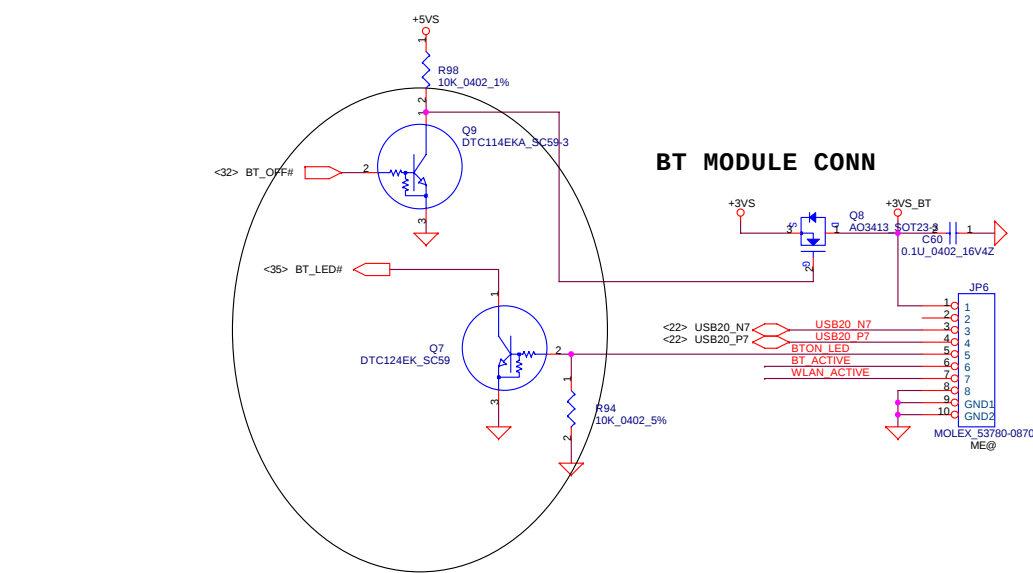
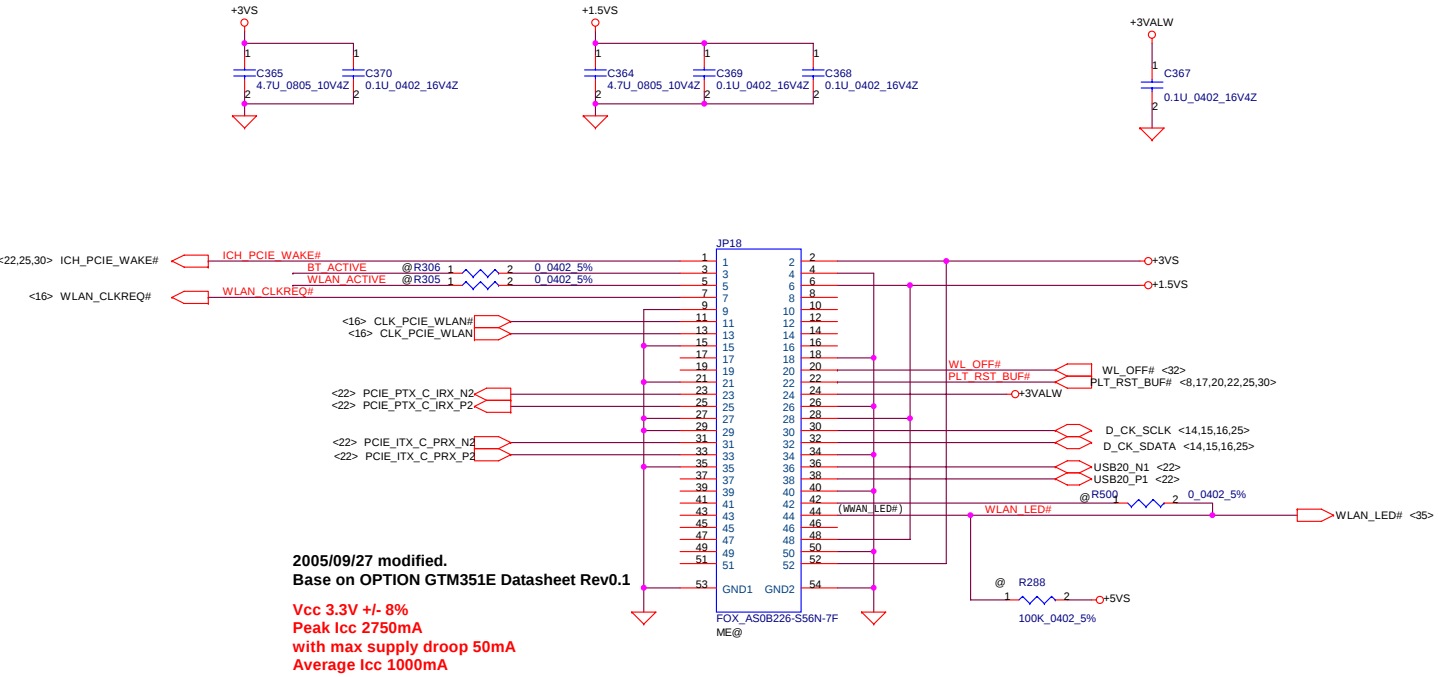


Not in CRB, Keep!

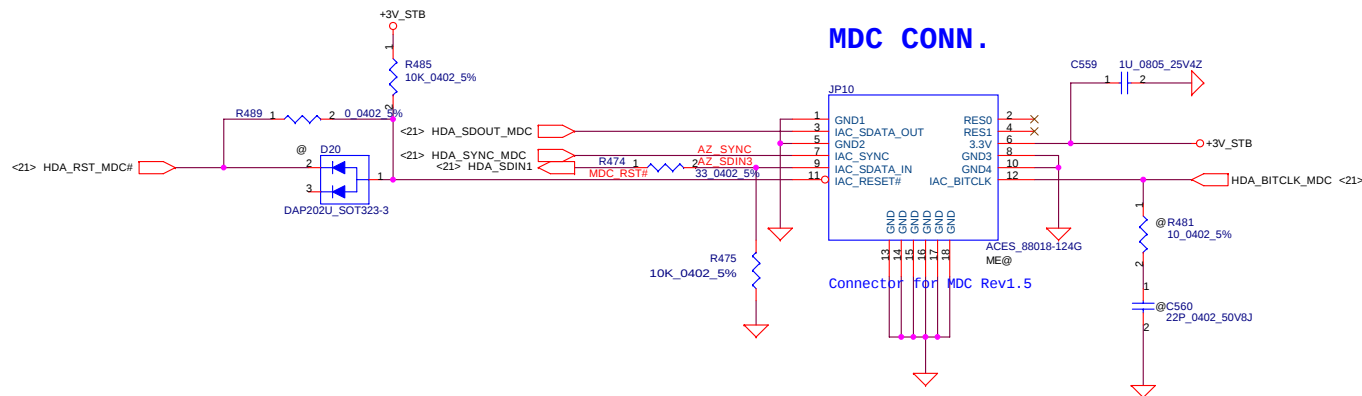
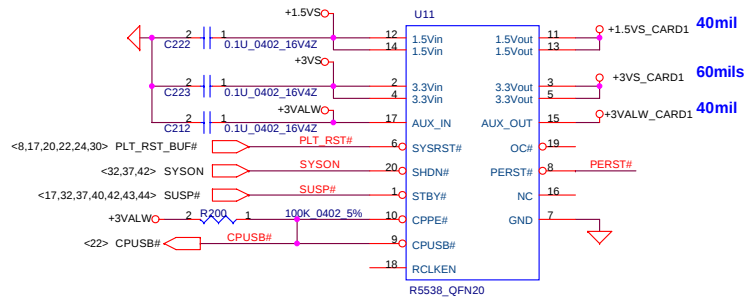


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Issued Date	2006/08/18	Deciphered Date	2007/8/18	ICH8M(3/4)-USB,GPIO,PCIE	
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				Customer	LA-3691P
				Date	Thursday, March 08, 2007
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Mini-Express Card for 3G Or TV Tuner
Mini-Express Card for WLAN

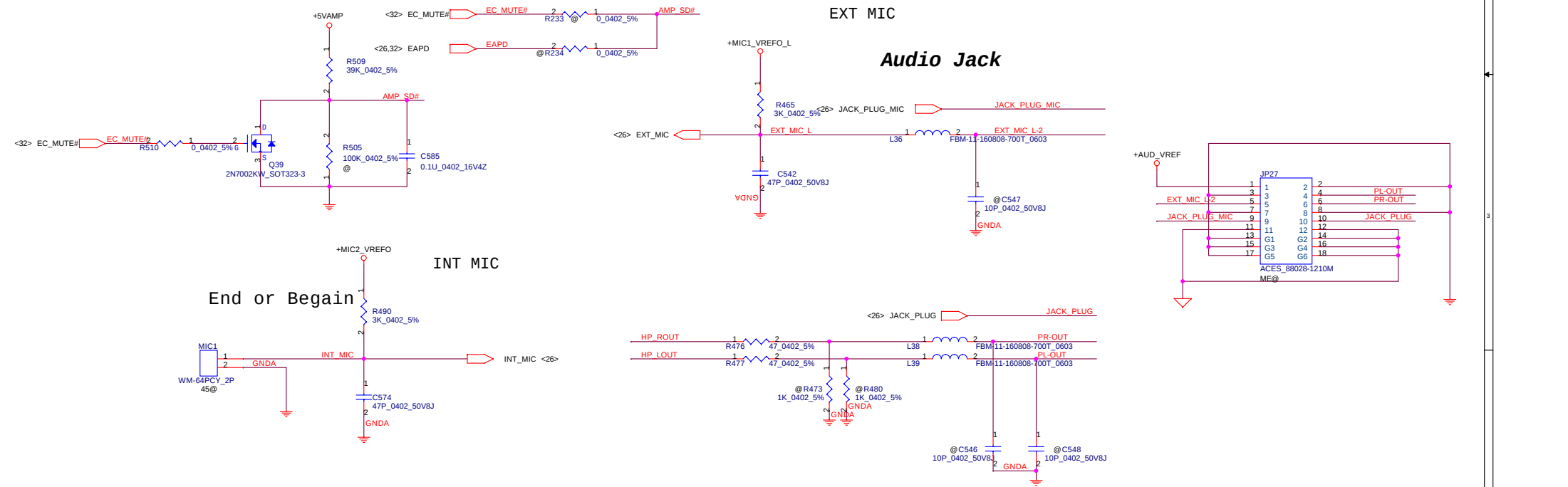
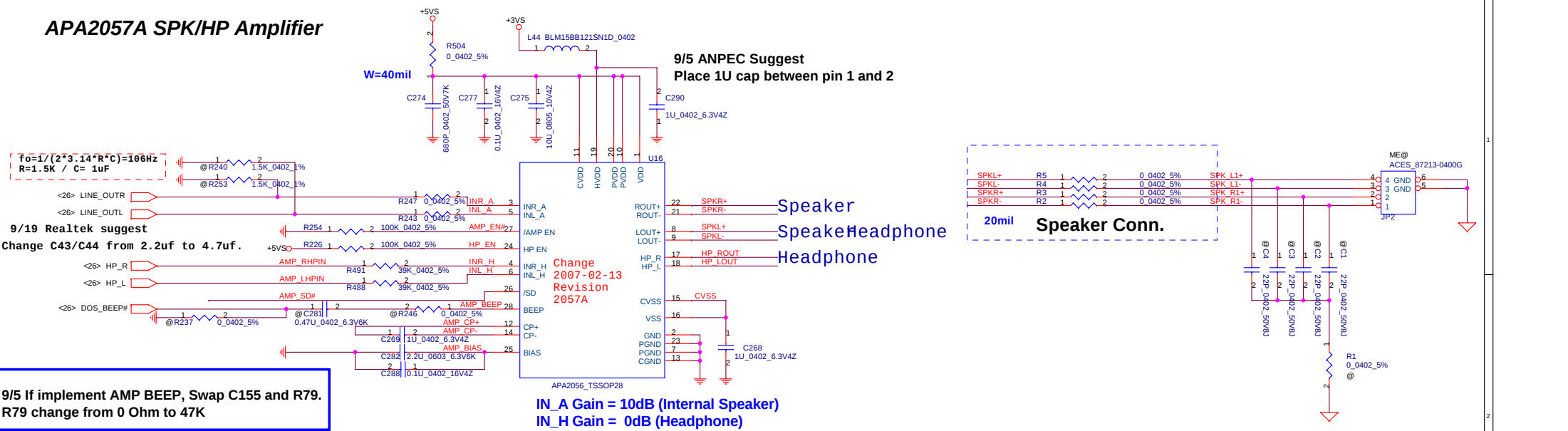


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Issued Date		2006/08/05	Deciphered Date	2007/08/05	Mini-Card/3G/FeliCa/FP
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Size		Document Number		Rev	
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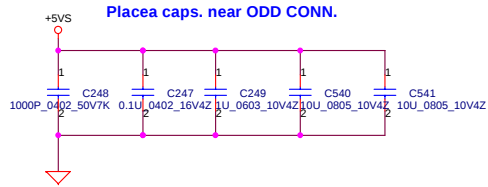


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	NEW CARD & USB Connector	
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				LA-3691P		
				Date: Thursday, March 08, 2007	Sheet 25 of 45	

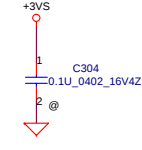
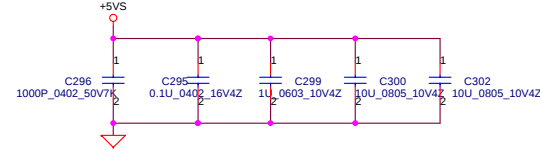
APA2057A SPK/HP Amplifier



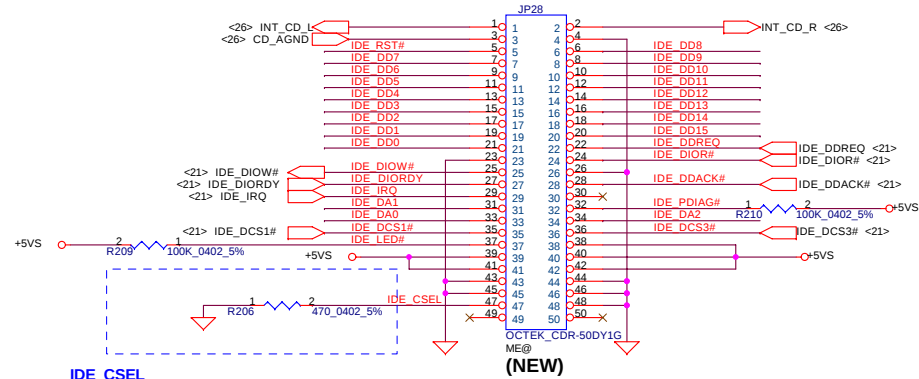
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Issued Date	2006/08/05	Deciphered Date	2007/08/05	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
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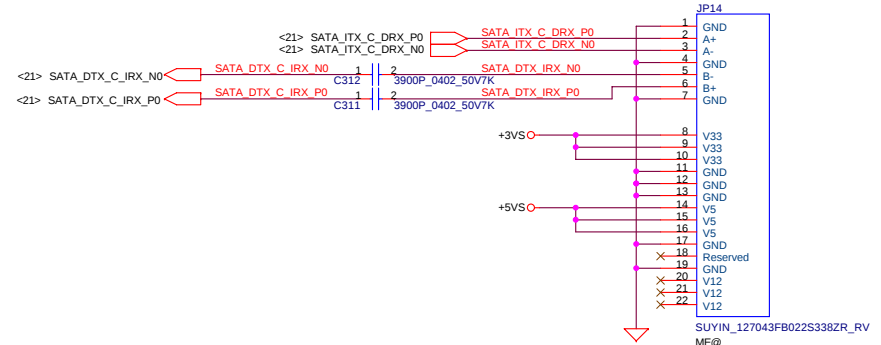
<21> IDE_DD[0..15] IDE_DD[0..15]
<21> IDE_DA[0..2] IDE_DA[0..2]



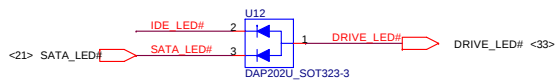
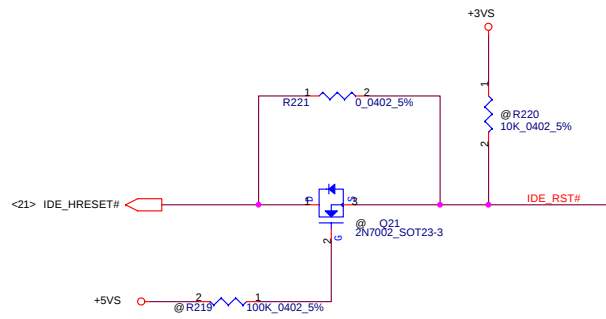
SATA HDD Conn.



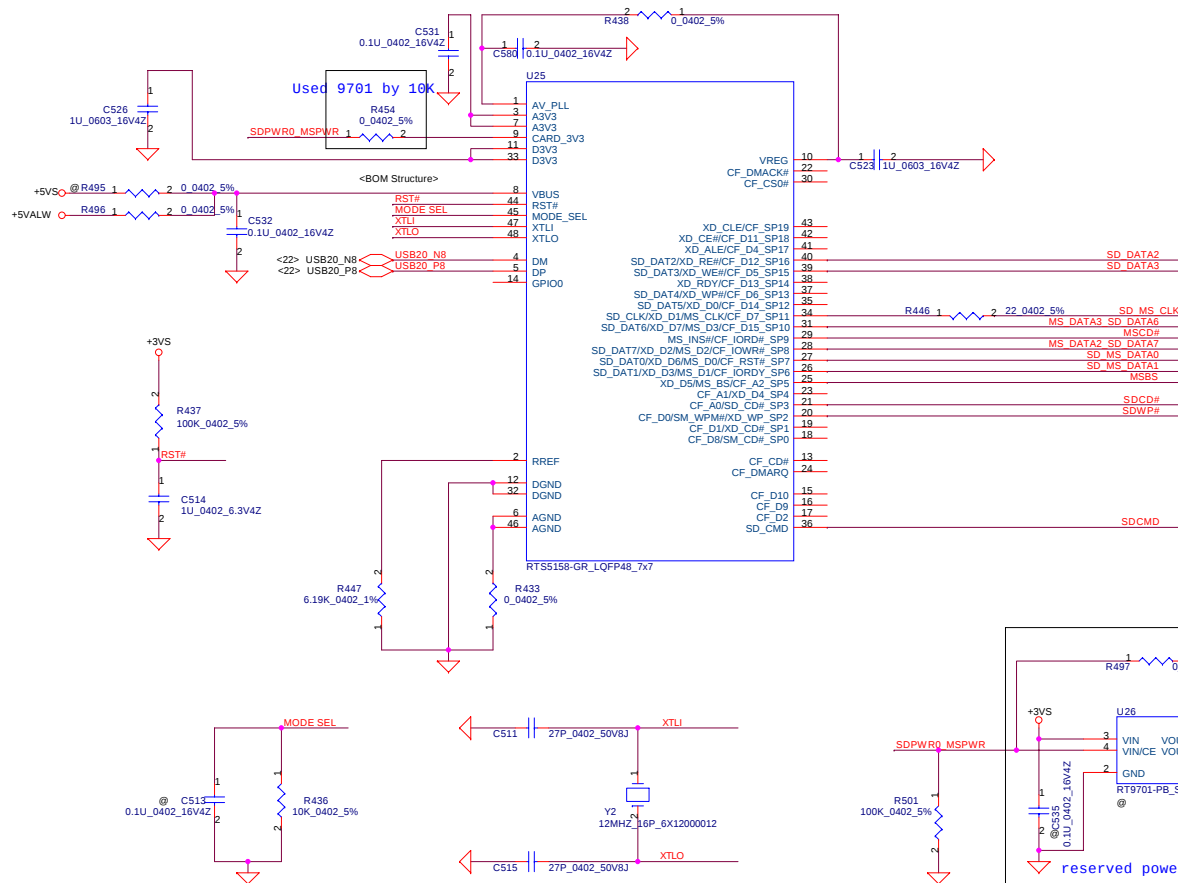
IDE_CSEL
Grounding for Master (When use SATA HDD)
Open or High for Slaver (Normal)



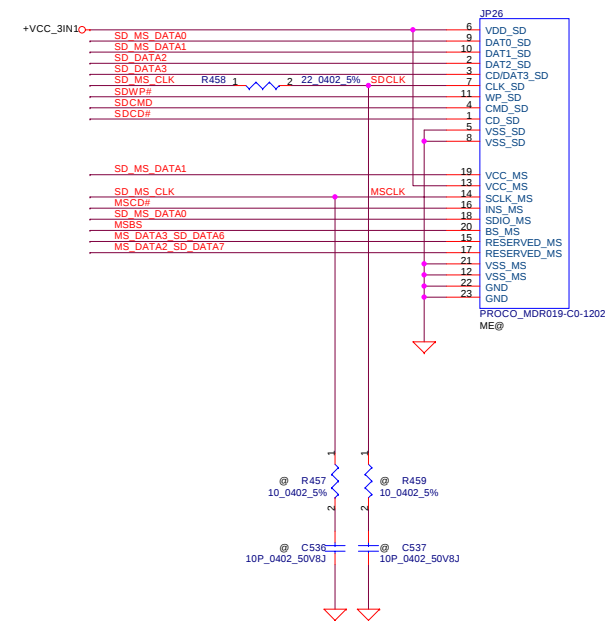
(NEW)
Change Library



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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size B	Document Number	LA-3691P		Rev	0.2
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3 in 1 Card Reader

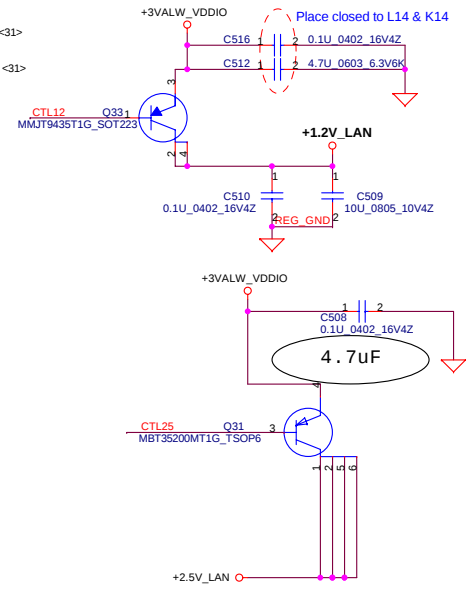
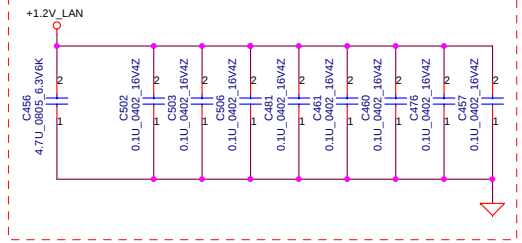
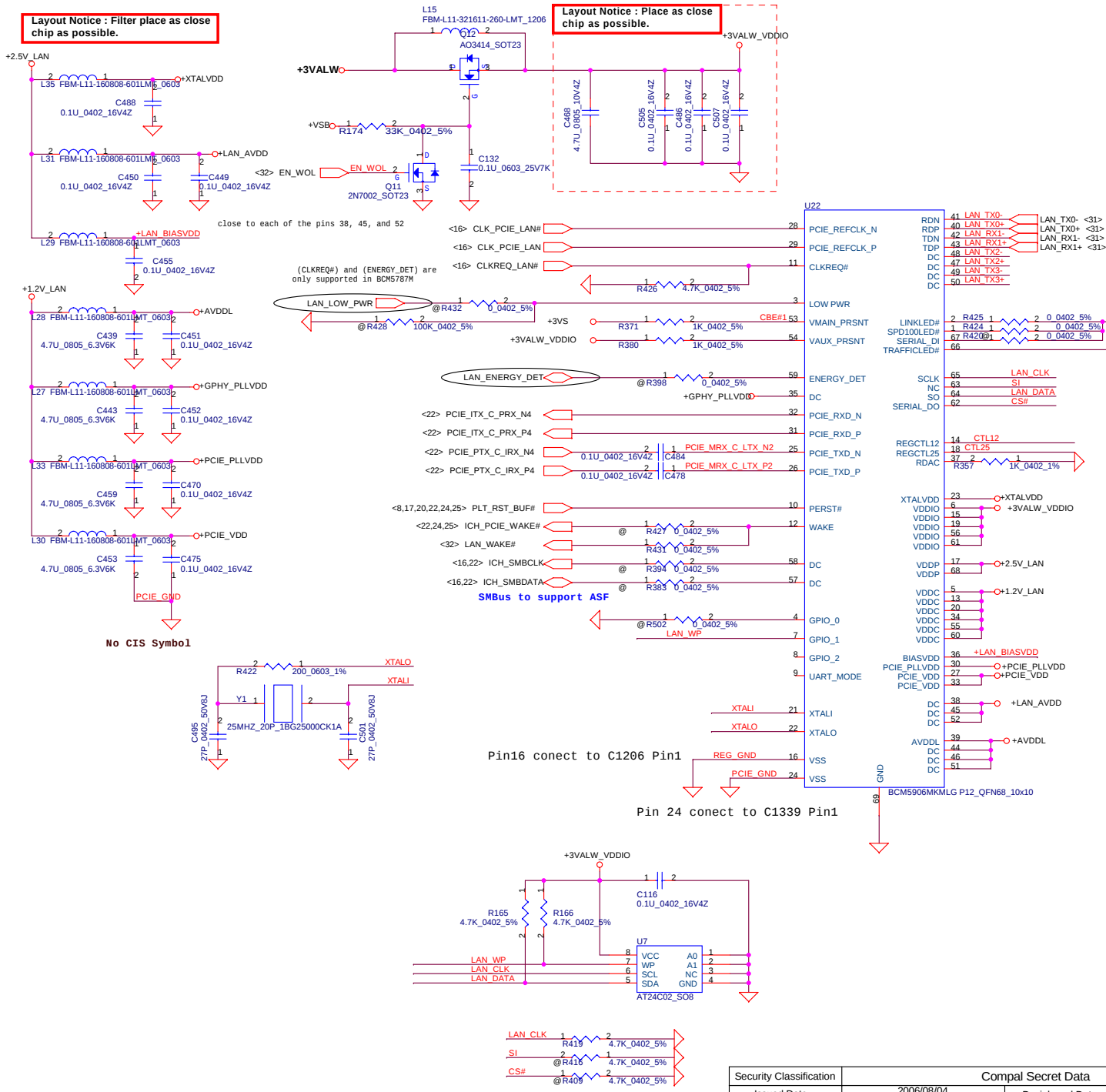


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Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title	1394+3 in 1 Card
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				Document Number	LA-3691P
				Date:	Thursday, March 08, 2007
				Sheet	29 of 45

Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

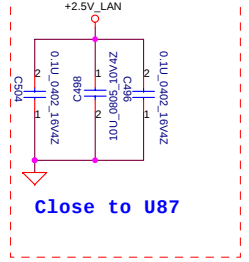
Layout Notice : 1.2V filter. Place as close chip as possible.



Notice : 4.7u 6.3V capacitor Thickness 1.25mm

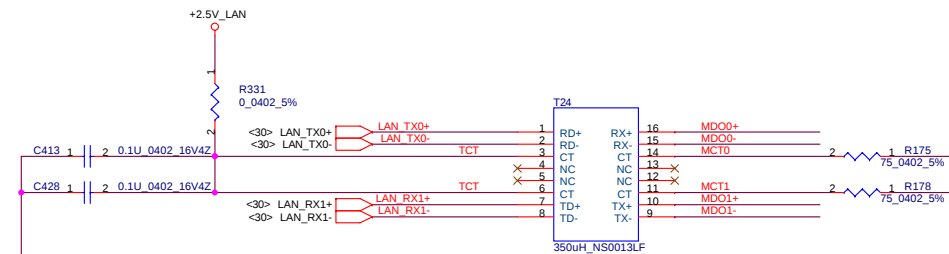
Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

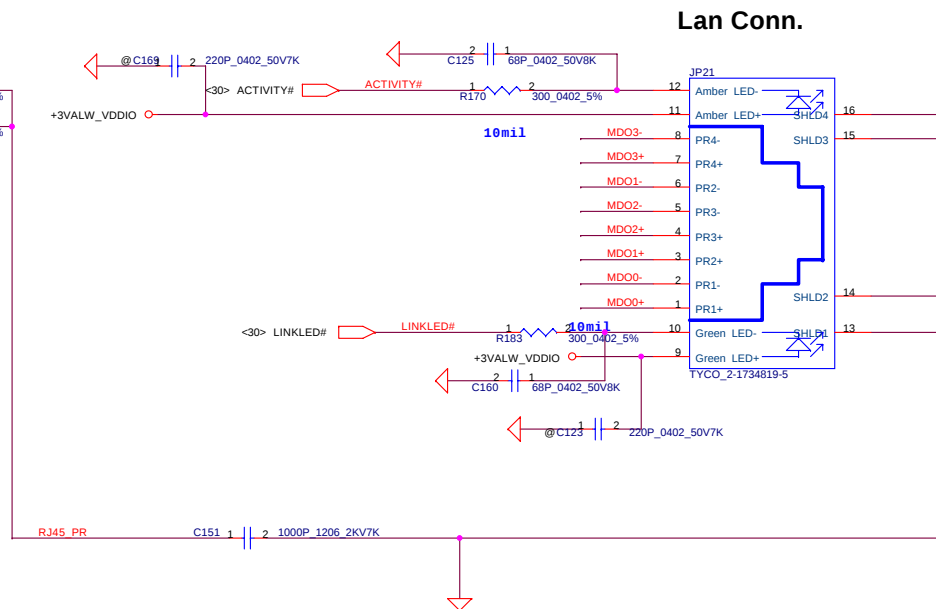
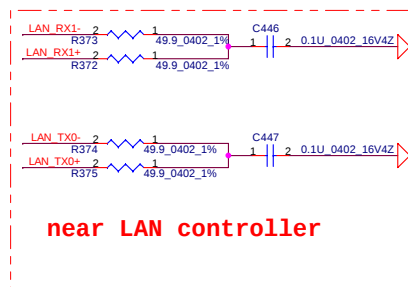


Security Classification		Compal Secret Data	
Issued Date	2006/08/04	Deciphered Date	2006/10/06
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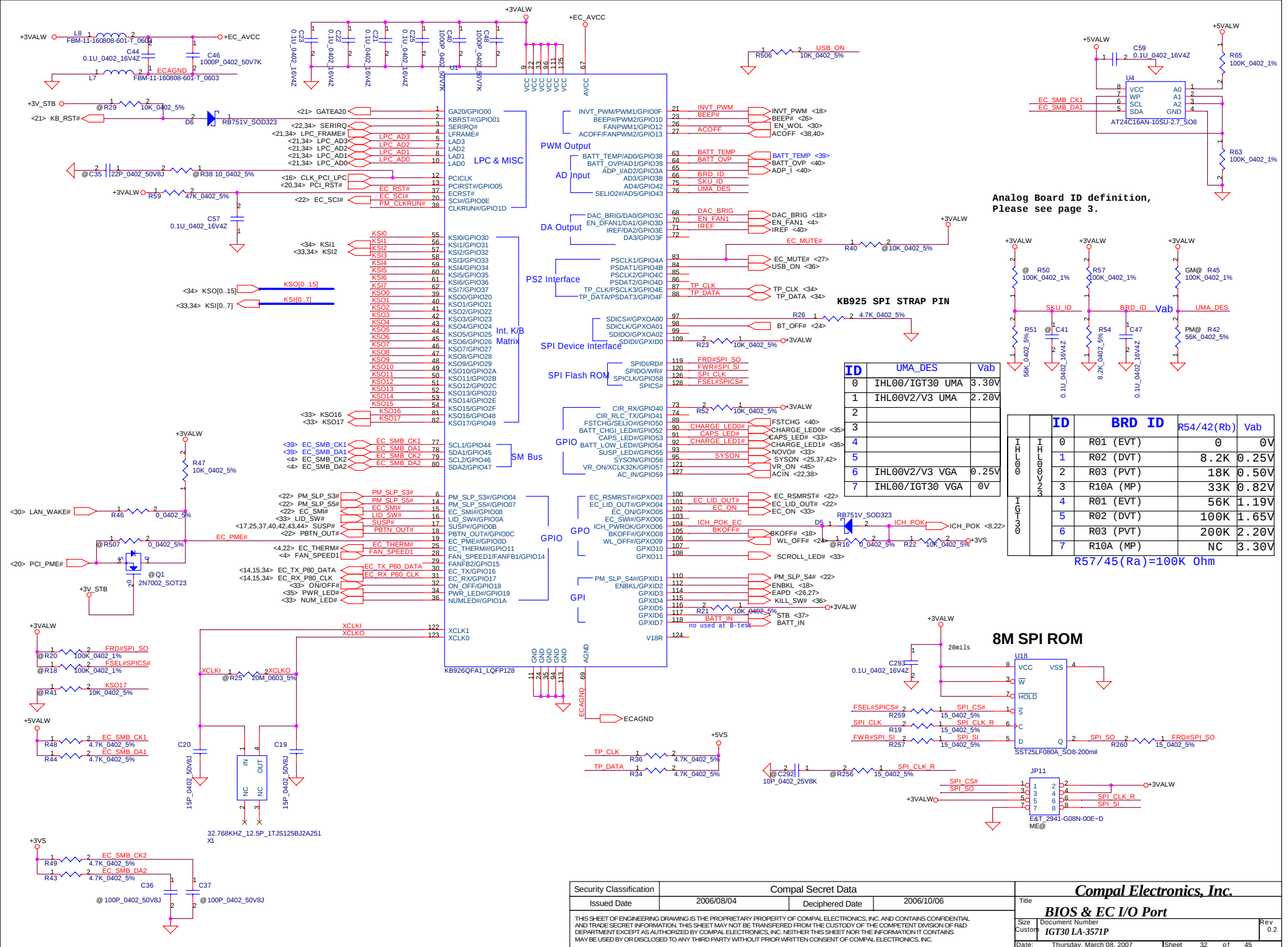
Compal Electronics, Inc.			
Title			
BCM5787M-GLAN			
Size	Document Number	Rev	
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Date:	Thursday, March 08, 2007	Sheet	30 of 45



Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF



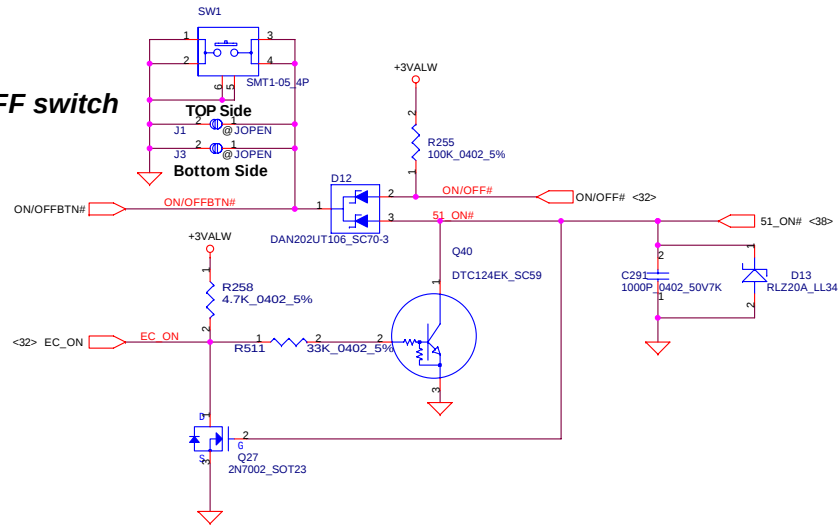
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Issued Date	2006/08/04	Deciphered Date	2006/10/06	LAN CONTROLLER	
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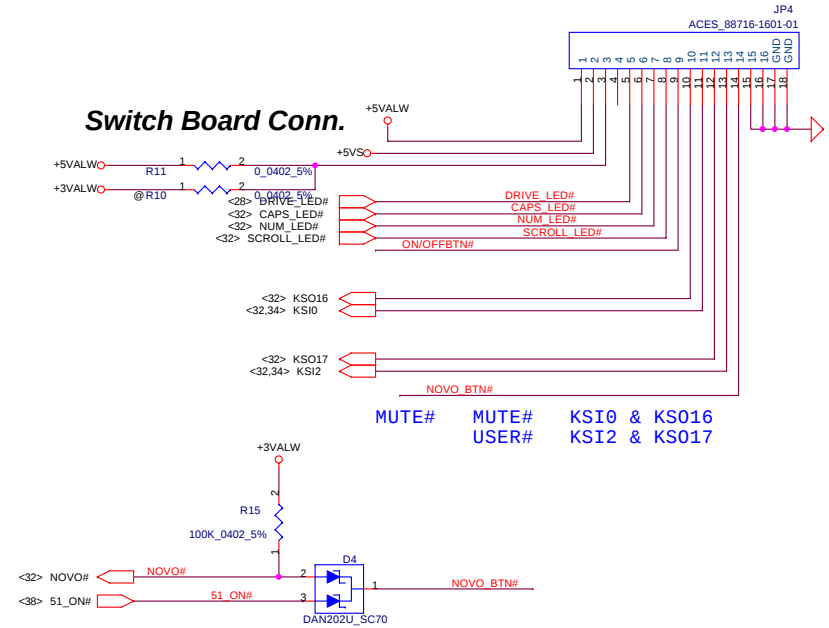
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Issued Date		2006/08/04	Deciphered Date	2006/10/06		Title	
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					Size	Document Number	Rev
					Custom	IGT30 LA-3571P	0.2
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Power Button

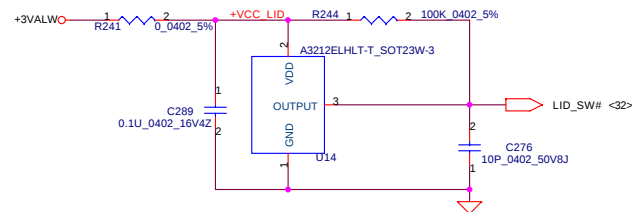
ON/OFF switch



Switch Board Conn.

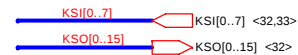


Lid Switch

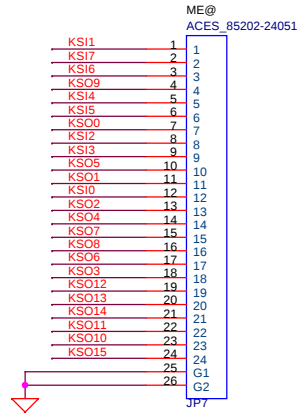
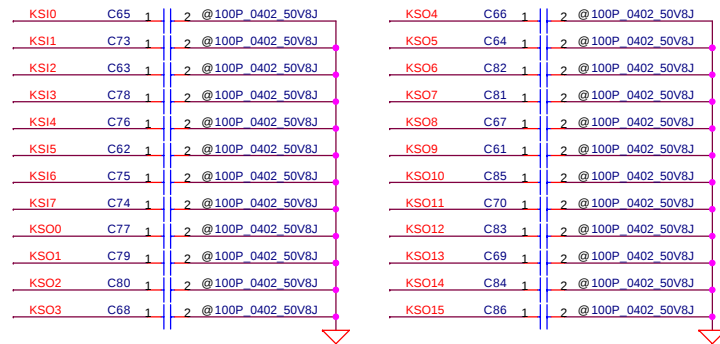


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				Size B	Document Number LA-3691P	Rev 0.2
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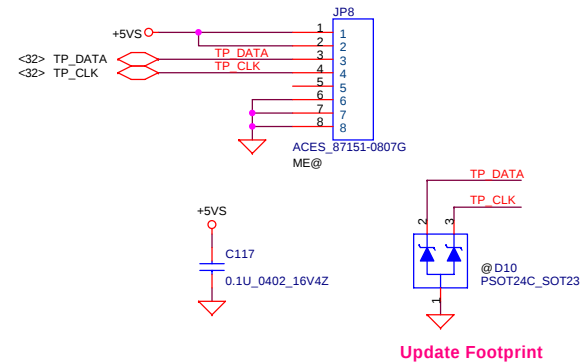
INT_KBD Conn.



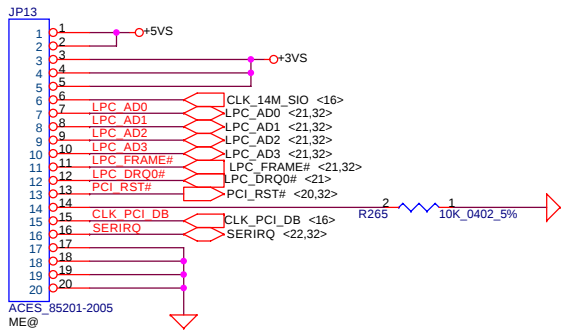
For IHL00



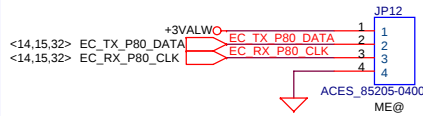
To TP/B Conn.



FOR LPC SIO DEBUG PORT

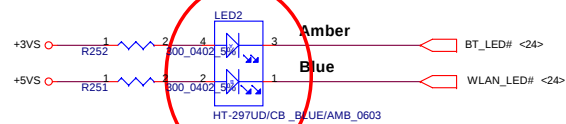
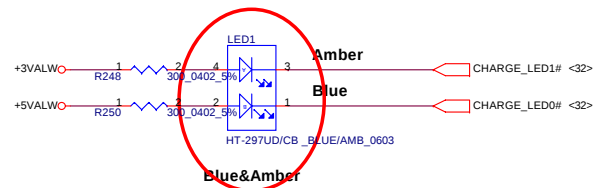
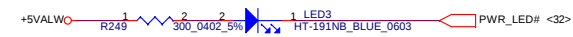


EC DEBUG PORT



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LED

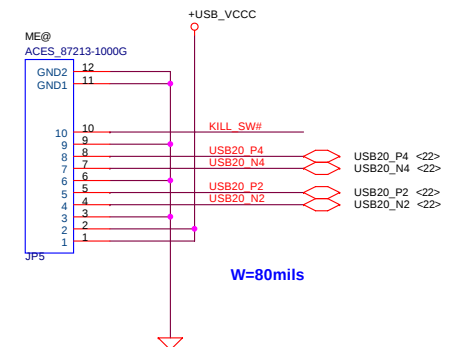
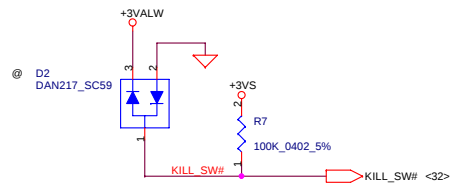


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Size B		Document Number LA-3691P			0.2
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USB Conn.

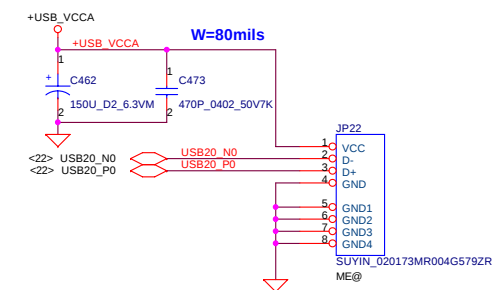
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Kill SWITCH



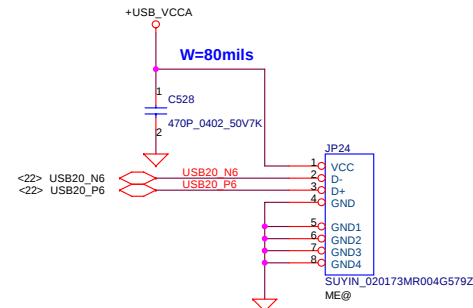
W=80mils

USB CONN. 1



W=80mils

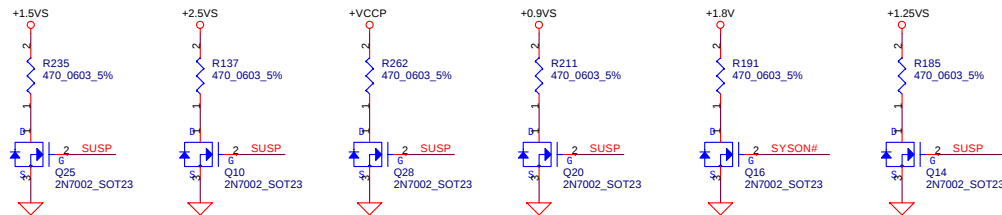
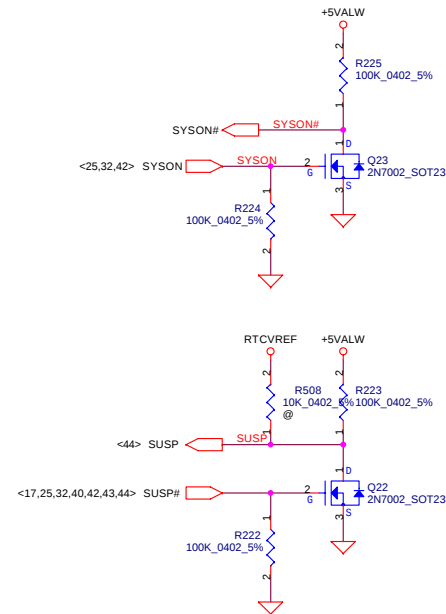
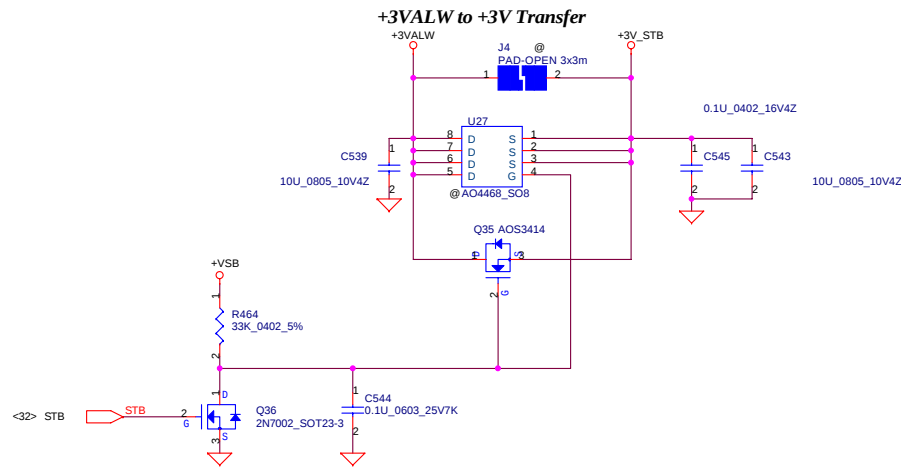
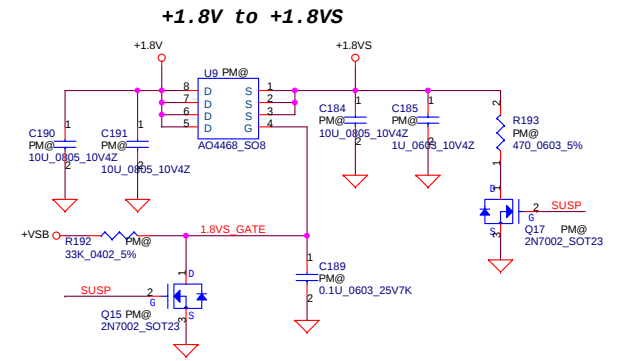
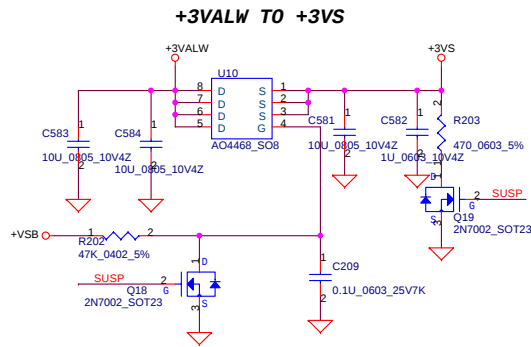
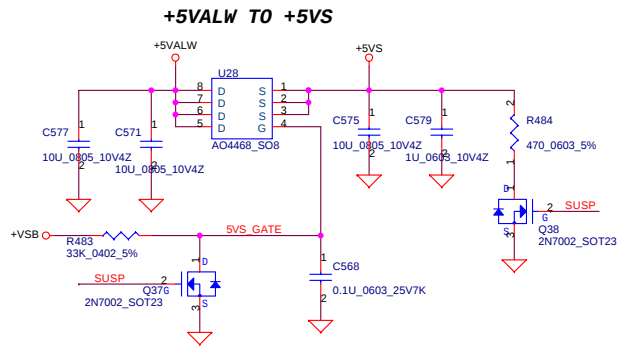
USB CONN. 2



W=80mils

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				Deciphered Date				Power OK, Reset and RTC Circuit, TP			
				2007/8/18				Size B			
								Document Number			
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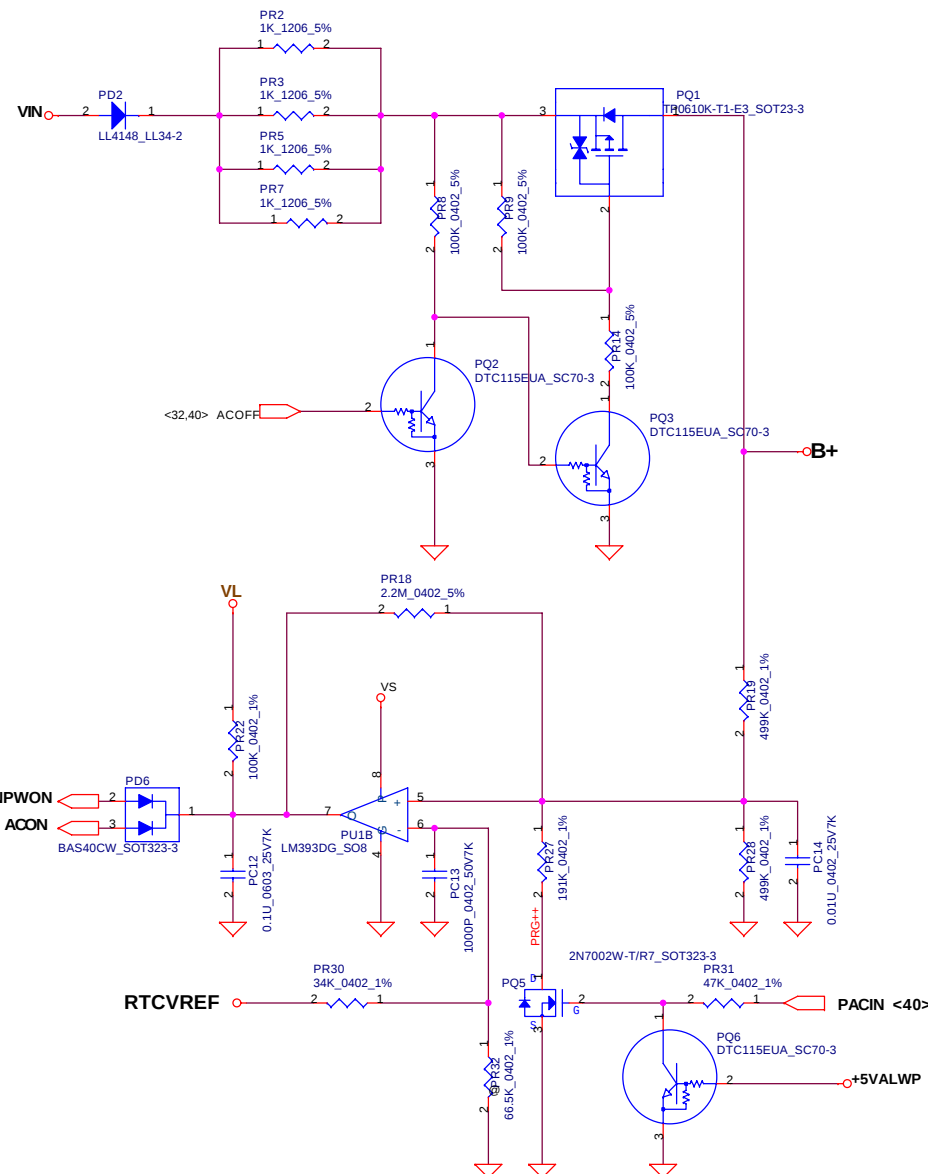
Vin Detector

Vin	High	Low
ACIN	18.764	17.745
PACIN	17.9	16.9

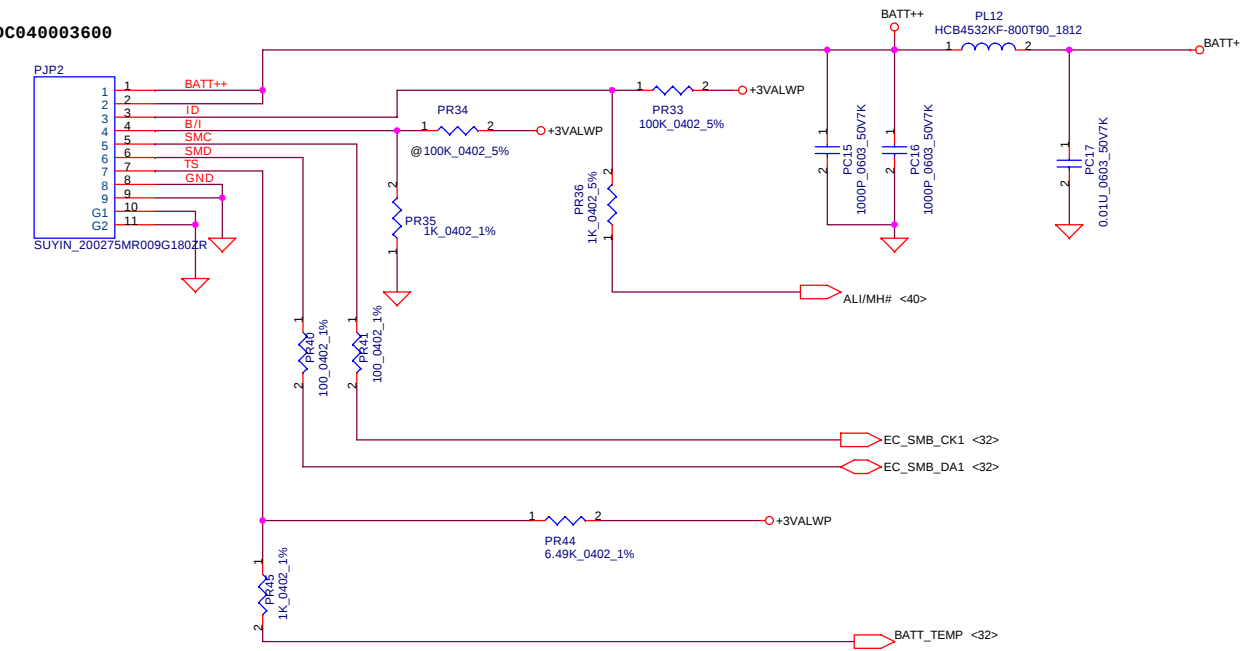
High	18.764	17.901	17.063
Low	17.745	16.9	16.03

	Precharge detector		
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

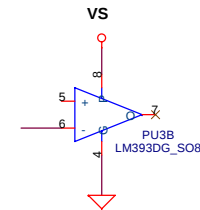
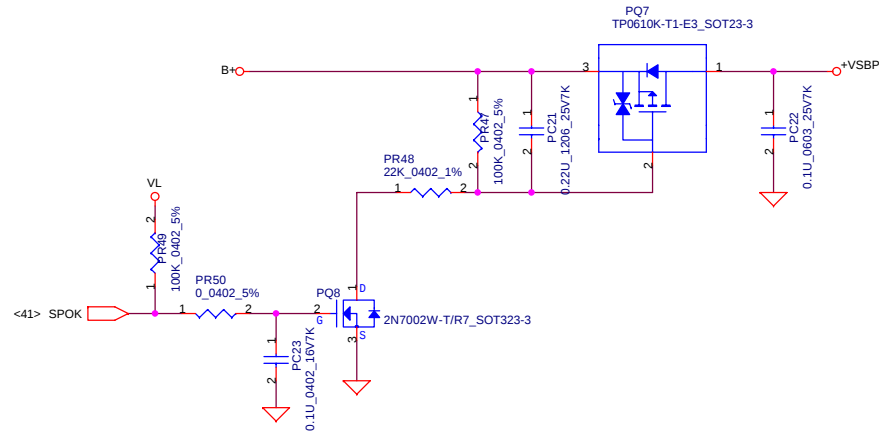
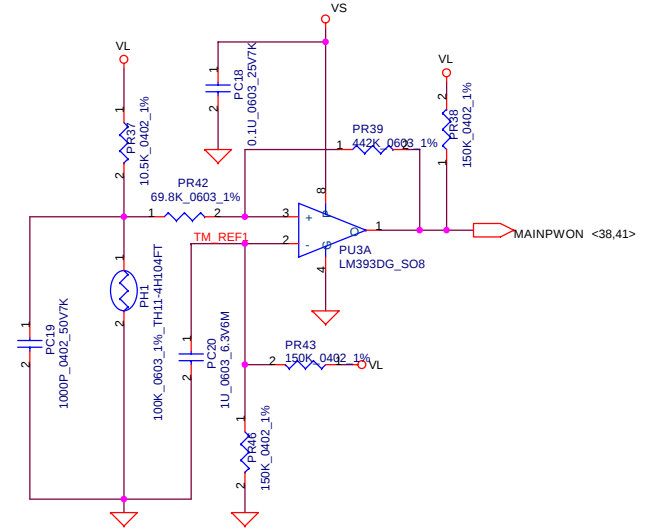
	Precharge detector		
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



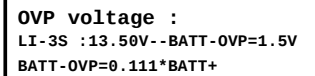
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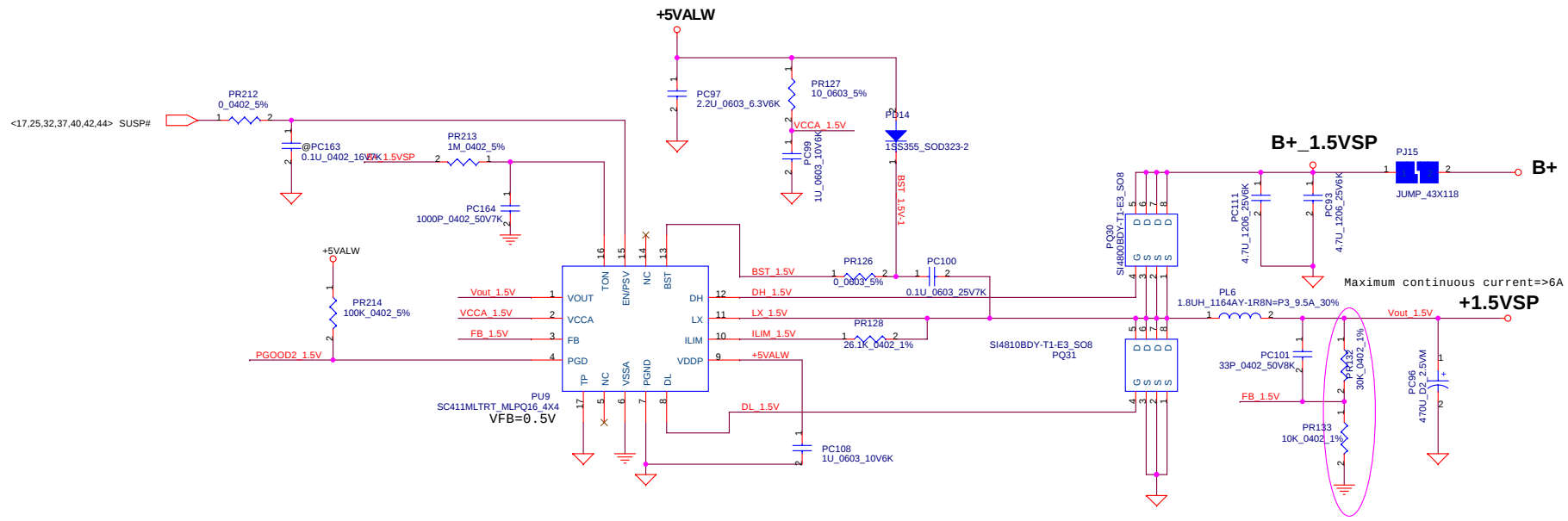
PH1 under CPU bottom side :
CPU thermal protection at 87 degree C
Recovery at 70 degree C



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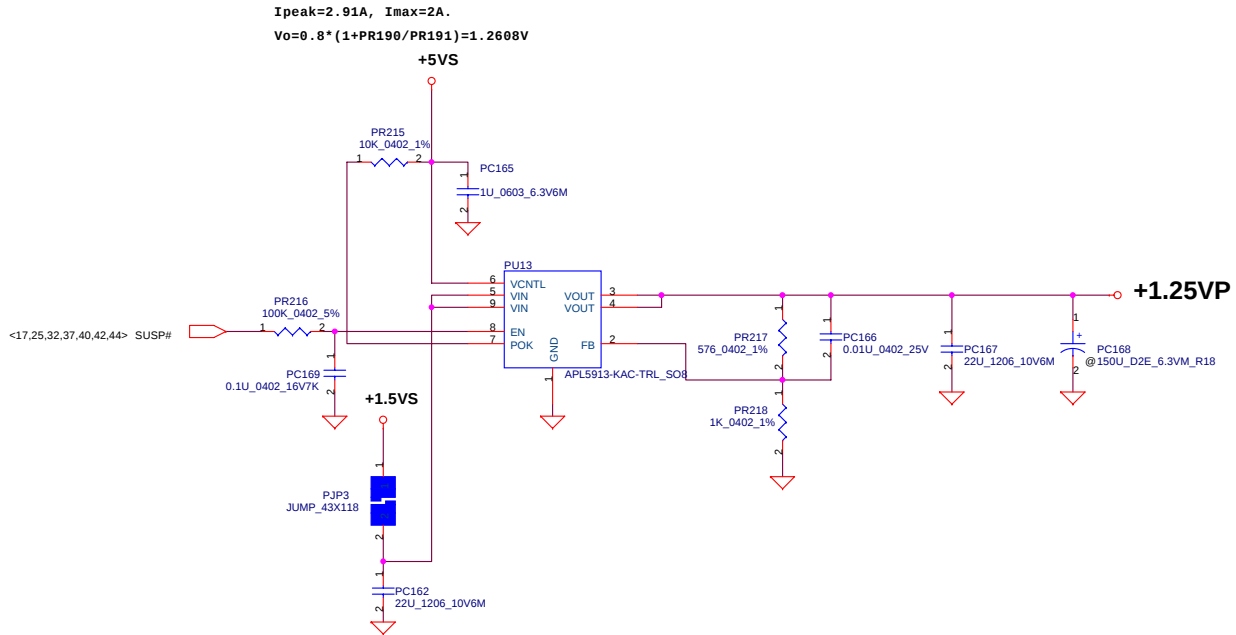
$$ADP_I = 19.9 \cdot I_{\text{adapter}} \cdot R_{\text{sense}}$$


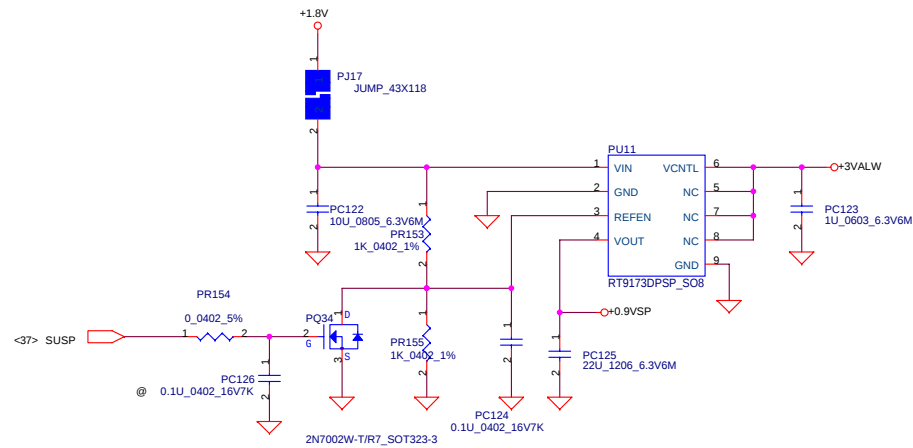
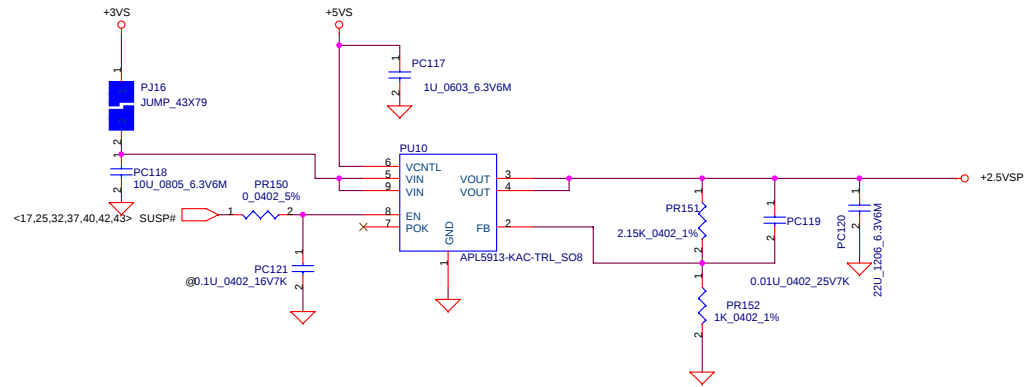
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Close to IC Side
Differential routing of feedback to VSSA2 and VOUT2 PIN

VFB=0.5V, Ipeak=14.02A, Imax=9.814A
 The current rating of +1.05VSP include +VCC_GFX current.
 $V_o = V_{FB} * (1 + PR146 / PR147) = 1.05V$
 $Ton = (3.3E-12 * (PR142 + 37K) * (Vout / VBat)) + 50ns = 0.2391us$
 $SI4810BDY: Rds(on) = Typ: 9mOhm$
 $Max: 11.5 mOhm$
 $Ivalleymin = 9 * 10E-6 * (PR145 / Rds(ON))_{max} * 1.5$
 $= 9 * 10E-6 * (26.1K / (0.0115 * 1.5)) = 13.617A$
 $Ivalleymax = 11 * 10E-6 * (PR145 / Rds(ON))_{min} * 1.2$
 $= 11 * 10E-6 * (26.1K / (0.009 * 1.3)) = 20.076A$
 $Iripple = (vin - vout) * (Ton / L) = 4.292A, 1/2 Iripple = 2.146A$
 $Iocp = Ivalley + Iripple / 2$
OCP ==> 15.763A ~ 22.222A





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